













SWRS211C - MAY 2017-REVISED OCTOBER 2018

**IWR1443** 

## IWR1443 Single-Chip 76- to 81-GHz mmWave Sensor

#### **Device Overview**

#### 1.1 **Features**

- FMCW Transceiver
  - Integrated PLL, Transmitter, Receiver, Baseband, and A2D
  - 76- to 81-GHz Coverage With 4-GHz Continuous Bandwidth
  - Four Receive Channels
  - Three Transmit Channels (Two Can be Used Simultaneously)
  - Ultra-Accurate Chirp Engine Based on Fractional-N PLL
  - TX Power: 12 dBm
  - RX Noise Figure:
    - 14 dB (76 to 77 GHz)
    - 15 dB (77 to 81 GHz)
  - Phase Noise at 1 MHz:
    - 95 dBc/Hz (76 to 77 GHz)
    - 93 dBc/Hz (77 to 81 GHz)
- **Built-in Calibration and Self-Test** 
  - ARM<sup>®</sup> Cortex<sup>®</sup>-R4F-Based Radio Control System
  - Built-in Firmware (ROM)
  - Self-calibrating System Across Frequency and Temperature
- On-Chip Programmable Core for Embedded User Application
  - Integrated Cortex®-R4F Microcontroller Clocked at 200 MHz
  - On-Chip Bootloader Supports Autonomous Mode (Loading User Application From QSPI Flash Memory)
  - Integrated Peripherals
    - Internal Memories With ECC
    - Radar Hardware Accelerator (FFT, Logmagnitude Computations, and others)
    - Integrated Timers (Watch Dog and up to Four 32-Bit or Two 64-Bit Timers)

- I2C (Master and Slave Modes Supported)
- Two SPI Ports
- CAN Port
- Up to Six General-Purpose ADC Ports
- High-Speed Data Interface to Support Distributed **Applications**
- Host Interface
  - Control Interface With External Processor Over
  - Data Interface With External Processor Over MIPI D-PHY and CSI2 V1.1
  - Interrupts for Fault Reporting
- IWR1443 Advanced Features
  - Embedded Self-monitoring With No Host Processor Involvement
  - Complex Baseband Architecture
  - Embedded Interference Detection Capability
- Power Management
  - Built-in LDO Network for Enhanced PSRR
  - I/Os Support Dual Voltage 3.3 V/1.8 V
- Clock Source
  - Supports External Oscillator at 40 MHz
  - Supports Externally Driven Clock (Square/Sine) at 40 MHz
- Easy Hardware Design
  - 0.65-mm Pitch, 161-Pin 10.4 mm × 10.4 mm Flip Chip BGA Package for Easy Assembly and Low-Cost PCB Design
  - Small Solution Size
- Operating Conditions
  - Junction Temp Range: –40°C to 105°C

#### 1.2 Applications

- Industrial Sensor for Measuring Range, Velocity, and Angle
- Tank Level Probing Radar
- Displacement Sensing
- Field Transmitters

- Traffic Monitoring
- Proximity and Position Sensing
- Security and Surveillance
- **Factory Automation**
- Safety Guards

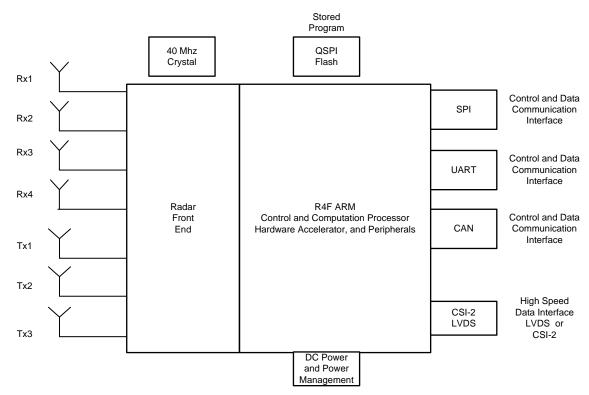


Figure 1-1. Autonomous Sensor For Industrial Applications

### 1.3 Description

The IWR1443 device is an integrated single-chip mmWave sensor based on FMCW radar technology capable of operation in the 76- to 81-GHz band with up to 4 GHz continuous chirp. The device is built with Tl's low-power 45-nm RFCMOS process, and this solution enables unprecedented levels of integration in an extremely small form factor. The IWR1443 is an ideal solution for low-power, self-monitored, ultra-accurate radar systems in the industrial applications such as building automation, factory automation, drones, material handling, traffic monitoring, and surveillance.

The IWR1443 device is a self-contained, single-chip solution that simplifies the implementation of mmWave sensors in the band of 76 to 81 GHz. The IWR1443 includes a monolithic implementation of a 3TX, 4RX system with built-in PLL and A2D converters. The device includes fully configurable hardware accelerator that supports complex FFT and CFAR detection. Additionally, the device includes two ARM R4F-based processor subsystems: one processor subsystem is for master control, and additional algorithms; a second processor subsystem is responsible for front-end configuration, control, and calibration. Simple programming model changes can enable a wide variety of sensor implementation with the possibility of dynamic reconfiguration for implementing a multimode sensor. Additionally, the device is provided as a complete platform solution including reference hardware design, software drivers, sample configurations, API guide, training, and user documentation.

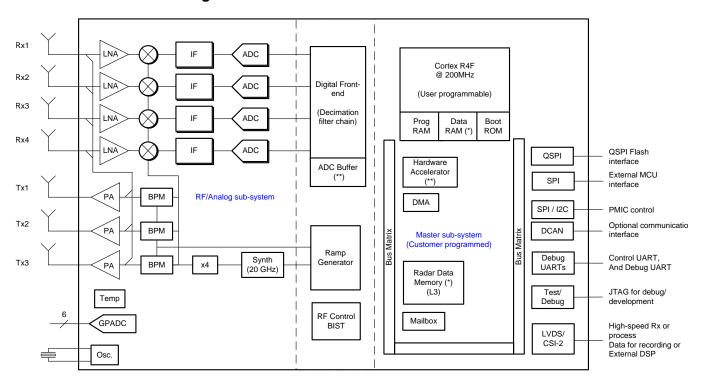
#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE
IWR1443FQAGABLR (Tape and Reel)	FCDCA (464)	10.4 mm 10.4 mm
IWR1443FQAGABL (Tray)	FCBGA (161)	10.4 mm × 10.4 mm

(1) For more information, see Section 9, Mechanical Packaging and Orderable Information.



### 1.4 Functional Block Diagram



<sup>(\*)</sup> Total RAM available in Master subsystem is divided into ARM-Data RAM, Tightly Coupled Memory, Radar Data Memory, Patch Memory

<sup>(\*\*)</sup> Shared Memory for ADC Buffer and Hardware Accelerator



### **Table of Contents**

1	Devi	ice Overview	. <u>1</u>		6.1	Overview	<u>51</u>
	1.1	Features	. <u>1</u>		6.2	Functional Block Diagram	51
	1.2	Applications	. <u>1</u>		6.3	External Interfaces	52
	1.3	Description	. <u>2</u>		6.4	Subsystems	52
	1.4	Functional Block Diagram	. <u>3</u>		6.5	Accelerators and Coprocessors	<u>57</u>
2	Revi	ision History	. <u>5</u>		6.6	Other Subsystems	<u>58</u>
3	Devi	ice Comparison	. <u>7</u>		6.7	Identification	62
	3.1	Related Products	<u>8</u>		6.8	Boot Modes	62
4	Tern	ninal Configuration and Functions	. <u>9</u>	7	App	lications, Implementation, and Layout	65
	4.1	Pin Diagram	<u>9</u>		7.1	Application Information	65
	4.2	Signal Descriptions	<u>13</u>		7.2	Reference Schematic	65
	4.3	Pin Multiplexing	<u>16</u>		7.3	Layout	66
5	Spe	cifications	<u>21</u>	8	Devi	ice and Documentation Support	67
	5.1	Absolute Maximum Ratings	<u>21</u>		8.1	Device Nomenclature	67
	5.2	ESD Ratings	<u>21</u>		8.2	Tools and Software	68
	5.3	Power-On Hours (POH)	<u>21</u>		8.3	Documentation Support	68
	5.4	Recommended Operating Conditions	<u>22</u>		8.4	Community Resources	69
	5.5	Power Supply Specifications	<u>22</u>		8.5	Trademarks	69
	5.6	Power Consumption Summary	<u>23</u>		8.6	Electrostatic Discharge Caution	69
	5.7	RF Specification	<u>24</u>		8.7	Export Control Notice	69
	5.8	Thermal Resistance Characteristics for FCBGA			8.8	Glossary	69
		Package [ABL0161]		9		hanical, Packaging, and Orderable	
	5.9	Timing and Switching Characteristics	_		Info	rmation	70
6	Deta	niled Description	<u>51</u>		9.1	Packaging Information	70



### 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Chan	ges from February 20, 2018 to October 31, 2018 (from B Revision (February 2018) to C Revision)	Page
•	Updated RX Noise Figure from "15 dB (76 to 77 GHz)" to "14 dB (76 to 77 GHz)"	1
•	Updated RX Noise Figure from "16 dB (77 to 81 GHz)" to "15 dB (77 to 81 GHz)"	
•	Updated Phase Noise at 1 MHz from "-94 dBc/Hz (76 to 77 GHz)" to "-95 dBc/Hz (76 to 77 GHz)"	1
•	Updated Phase Noise at 1 MHz from "-91 dBc/Hz (77 to 81 GHz)" to "-93 dBc/Hz (77 to 81 GHz)"	
•	Removed "(Namely, Intermediate Data)" from "High-Speed Data Interface" bullet	1
•	Removed 50 MHz from Externally Driven Oscillator and Externally Driven Clock	1
•	Updated Device Information	
•	Removed VMON block from Functional Block Diagram	
•	Added table note to "Number of transmitters" in Device Features Comparison	
•	Updated IWR1443 and IWR1642 Product status from AI to PD	<u>7</u>
•	Updated OSC_CLKOUT	<u>13</u>
•	Updated P7 from "Open Drain" to "Pull Up'	
•	Updated B10 DESCRIPTION	
•	Updated A10, A13, A2, and B2 DESCRIPTION	
•	Removed footnote from Flash programming and RS232 UART	
•	Updated ESD Ratings	<u>21</u>
•	Updated/Changed Power-On Hours (POH)	
•	Updated VIOIN in Recommended Operating Conditions	
•	Updated V <sub>IL</sub> 1.8V MAX from "3*VIOIN" to "0.3*VIOIN"	
•	Updated V <sub>OH</sub> in Recommended Operating Conditions	
•	Updated V <sub>OH</sub> in Recommended Operating Conditions	
•	Updated Recommended Operating Conditions	
•	Added "VNWA" to 1.2 V Supply in Power Supply Rails Characteristics	
•	Completely updated Ripple Specifications table	
•	Updated Receiver Noise figure values in RF Specification	
•	Updated Receiver 1-dB compression point value from "-5" to "-8"	
•	Updated "IQ gain mismatch" to "Image Rejection Ratio (IMRR)"	
•	Removed IQ phase mismatch from RF Specification	
•	Updated RF Specification table	
•	Updated footnote in RF Specification	
•	Removed 1v4 signal from Device Wakeup	
•	Updated Device Wake-up Sequence	
•	Updated Synchronized Frame Triggering text	
•	Added Synchronized Frame Triggering subsection	
•	Removed T <sub>Lag</sub> from Frame Trigger Timing table	
•	Updated Crystal Implementation note	
•	Updated/Changed f <sub>P</sub> Parallel resonance crystal frequency from " 40, 50" to "40"	
•	Completely updated External Clock Mode Specifications	
•	Updated SPI Slave Mode Timing Requirements	
•	Added LVDS Interface Configuration	
•	Updated LVDS Interface Lane Config image	
•	Updated Timing Parameters	
•	Updated LVDS Electrical Characteristics	
•	Updated Timing Requirements for QSPI Input (Read) Timings	
•	Added Q12, Q13, Q14, and Q15 to QSPI Switching Characteristics	
•	Updated Data bit rate from 900 Mbps to 600 Mbps	
•	Removed T <sub>CLK-SETTLE</sub> and T <sub>HS-SETTLE</sub>	
•	Updated Clock Subsystem diagram	
•	Updated/Changed Transmit Subsystem (Per Channel)	
•	Removed Master System Memory Map	
•	Updated Host Interface	
•	Updated text in "A2D Data Format Over CSI2 Interface"	
•	Updated text in ADC Channels (Service) for User Application	
•	Completely upualed Gr-ADO raidifield table	00



•	Updated text in Functional Mode	64
•	Updated Application Information	65
•	Updated Device Nomenclature	<u>68</u>



## 3 Device Comparison

**Table 3-1. Device Features Comparison** 

FUNCTION		IWR1443	IWR1642	
Number of receivers	S	4	4	
Number of transmitt	ers	3	2	
On-chip memory		576KB	1.5MB	
Max I/F (Intermedia	te Frequency) (MHz)	15	5	
Max real sampling r	ate (Msps)	37.5	12.5	
Max complex sampl	ing rate (Msps)	18.75	6.25	
Processor				
MCU (R4F)		Yes	Yes	
DSP (C674x)		_	Yes	
Peripherals				
Serial Peripheral Int	erface (SPI) ports	1	2	
Quad Serial Periphe	eral Interface (QSPI)	Yes	Yes	
Inter-Integrated Circ	uit (I <sup>2</sup> C) interface	1	1	
Controller Area Net	work (DCAN) interface	Yes	Yes	
Trace		_	Yes	
PWM		_	Yes	
Hardware In Loop (I	HIL/DMM)	_	Yes	
GPADC		Yes	Yes	
LVDS/Debug		Yes	Yes	
CSI2		Yes	_	
Hardware accelerate	or	Yes	_	
1-V bypass mode		Yes	Yes	
JTAG		Yes	Yes	
Product status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD <sup>(1)</sup>	PD <sup>(1)</sup>	

<sup>(1)</sup> PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



#### 3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

- mmWave Sensors TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for industrial applications.
- mmWave IWR The Texas Instruments IWR1xxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 76- to 81-GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis, includes a built-in radio processor (BIST) for RF calibration and safety monitoring. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from long range to ultra short range can be realized using these devices.
- Companion Products for IWR1443 Review products that are frequently purchased or used in conjunction with this product.
- IWR1443 Reference Designs The IWR1443 TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.
- Power Optimization for IWR1443 77GHz-Level Transmitter Reference Design The TIDEP-0091 highlights strategies for power optimization of a IWR1443 76- to 81-GHz mmWave sensor in tank level-probing applications, displacement sensors, 4- to 20-mA sensors, and other low-power applications for detecting range with high accuracy in minimal power envelope.



### **Terminal Configuration and Functions**

#### Pin Diagram 4.1

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.

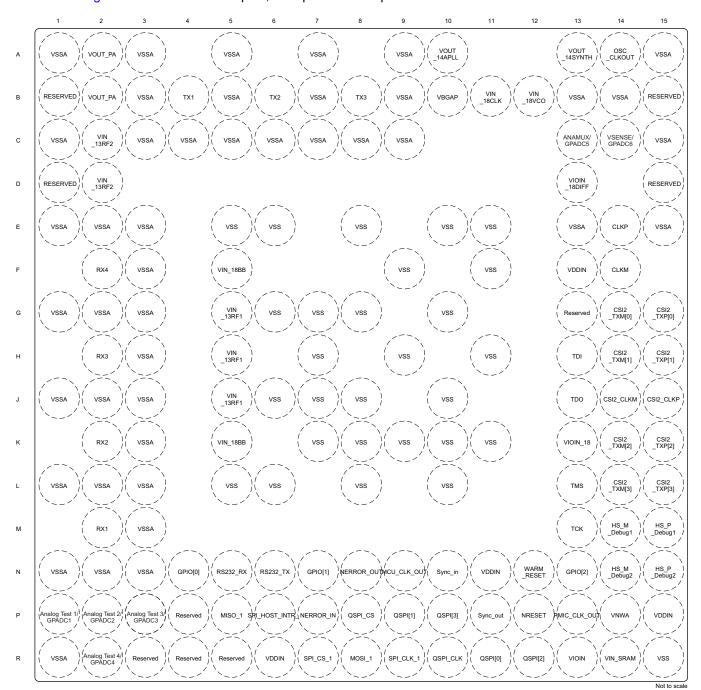


Figure 4-1. Pin Diagram

Submit Documentation Feedback Product Folder Links: IWR1443



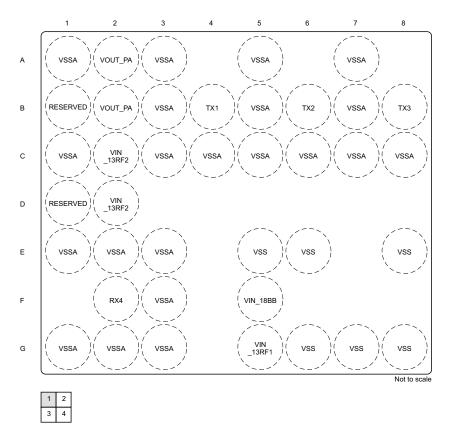


Figure 4-2. Top Left Quadrant

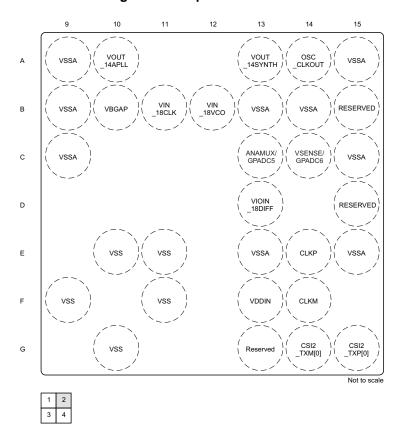


Figure 4-3. Top Right Quadrant



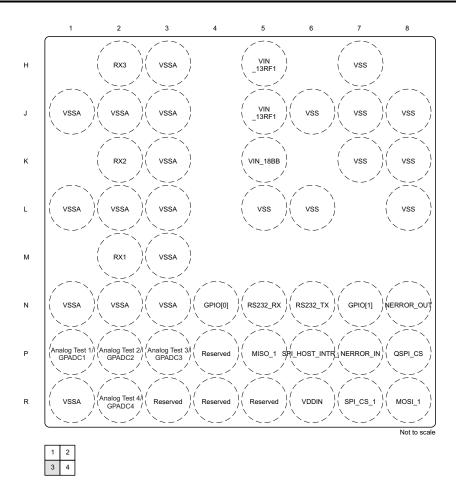


Figure 4-4. Bottom Left Quadrant

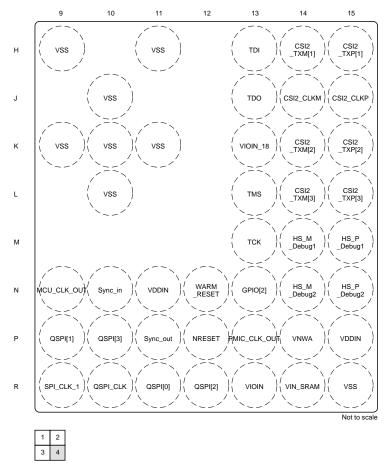


Figure 4-5. Bottom Right Quadrant



## 4.2 Signal Descriptions

**Table 4-1. Signal Descriptions** 

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
	TX1	B4	0	_	Single-ended transmitter1 o/p
Transmitters	TX2	B6	0	_	Single-ended transmitter2 o/p
	TX3	B8	0	_	Single-ended transmitter3 o/p
	RX1	M2	I	_	Single-ended receiver1 i/p
Doggivers	RX2	K2	I	_	Single-ended receiver2 i/p
Receivers	RX3	H2	I	_	Single-ended receiver3 i/p
	RX4	F2	I	_	Single-ended receiver4 i/p
	CSI2_TXP[0]	G15	0	_	Differential data Out – Lane 0
	CSI2_TXM[0]	G14	0	_	Differential data Out – Lane 0
	CSI2_CLKP	J15	0	_	Differential alack Out
	CSI2_CLKM	J14	0	_	Differential clock Out
	CSI2_TXP[1]	H15	0	_	Differential data Out. Lanc. 4
	CSI2_TXM[1]	H14	0	_	Differential data Out – Lane 1
CSI2 TX/LVDS	CSI2_TXP[2]	K15	0	_	Differential data Out I ama 2
TX	CSI2_TXM[2]	K14	0	_	Differential data Out – Lane 2
	CSI2_TXP[3]	L15	0	_	Differential data Out. Lane 2
	CSI2_TXM[3]	L14	0	_	Differential data Out – Lane 3
	HS_DEBUG1_P	M15	0	_	Difference (i.e.) and the second of
	HS_DEBUG1_M	M14	0	_	Differential debug port 1
	HS_DEBUG2_P	N15	0	_	Differential deliver ment 0
	HS_DEBUG2_M	N14	0	_	Differential debug port 2
	RESERVED	B1, B15, D1, D15		_	
Reference clock	OSC_CLKOUT	A14	0	_	Reference clock output from clocking subsystem after cleanup PLL.
System	SYNC_OUT	P11	0	Pull Down	Low-frequency frame synchronization signal output. Can be used by slave chip in multichip cascading
synchronization	SYNC_IN	N10	I	Pull Down	Low-frequency frame synchronization signal input.
	SPI_CS_1	R7	I	Pull Up	SPI chip select
SPI control interface from	SPI_CLK_1	R9	I	Pull Down	SPI clock
external MCU	MOSI_1	R8	I	Pull Up	SPI data input
(default slave mode)	MISO_1	P5	0	Pull Up	SPI data output
modo)	SPI_HOST_INTR_1	P6	0	Pull Down	SPI interrupt to host
	RESERVED	R3, R4, R5, P4		_	
	NRESET	P12	I	Open Drain	Power on reset for chip. Active low
Reset	WARM_RESET	N12	Ю	Open Drain	Open-drain fail-safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.
Safaty	NERROR_OUT	N8	0	Open Drain	Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.
Safety	NERROR_IN	P7	I	Pull Up	Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware

<sup>(1)</sup> Status of PULL structures associated with the IO after device POWER UP.



**Table 4-1. Signal Descriptions (continued)** 

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
	TMS	L13	ı	Pull Up	
1740	TCK	M13	I	Pull Down	J.T.A.O
JTAG	TDI	H13	I	Pull Up	JTAG port for standard boundary scan
	TDO	J13	0	_	
	CLKP	E14	I	_	In XTAL mode: Differential port for reference crystal
Reference oscillator	CLKM	F14	0		In External clock mode: Single ended input reference clock port (Output CLKM is grounded in this case)
Band-gap voltage	VBGAP	B10	0	_	Internal voltage reference 0.9V
	VDDIN	F13,N11,P1 5,R6	POW	_	1.2-V digital power supply
	VIN_SRAM	R14	POW	_	1.2-V power rail for internal SRAM
	VNWA	P14	POW	_	1.2-V power rail for SRAM array back bias
	VIOIN	R13	POW	_	I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply.
	VIOIN_18	K13	POW	_	1.8-V supply for CMOS IO
	VIN_18CLK	B11	POW	_	1.8-V supply for clock module
	VIOIN_18DIFF	D13	POW	_	1.8-V supply for CSI2 port
	Reserved	G13	POW	_	No connect
	VIN_13RF1	G5,J5,H5	POW	_	1.3-V Analog and RF supply,VIN_13RF1 and VIN 13RF2 could be shorted on the board
	VIN_13RF2	C2,D2	POW	ĺ	1.0-V Analog and RF supply input if RFLDO is bypassed
	VIN_18BB	K5,F5	POW	_	1.8-V Analog baseband power supply
	VIN_18VCO	B12	POW	_	1.8-V RF VCO supply
Power supply	vss	E5,E6,E8,E 10,E11,F9,F 11,G6,G7,G 8,G10,H7,H 9,H11,J6,J7 ,J8,J10,K7, K8,K9,K10, K11,L5,L6,L 8,L10,R15	GND	_	Digital ground
	VSSA	A1,A3,A5,A 7,A9,A15,B 3,B5,B7,B9, B13,B14,C1, C3,C4,C5, C6,C7,C8,C 9,C15,E1,E 2,E3,E13,E 15,F3,G1,G 2,G3,H3,J1, J2,J3,K3,L1, L2,L3, M3,N1,N2,N 3,R1	GND	<del>-</del>	Analog ground
	VOUT_14APLL	A10	0	_	1.4V internal regulator
Internal LDO	VOUT_14SYNTH	A13	0	_	1.4V internal regulator
output/inputs	VOUT_PA	A2,B2	0	_	1.0V internal regulator
	PMIC_CLK_OUT	P13	0	_	Dithered clock input to PMIC
External clock out	MCU_CLK_OUT	N9	0	_	Programmable clock given out to external MCU or the processor



**Table 4-1. Signal Descriptions (continued)** 

		1 45.0 4 1	. 0.9	Descriptions (o	Jiminaoa,
FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
	GPIO[0]	N4	Ю	Pull Down	General-purpose IO
General- purpose I/Os	GPIO[1]	N7	Ю	Pull Down	General-purpose IO
purpose 1/Os	GPIO[2]	N13	Ю	Pull Down	General-purpose IO
	QSPI_CS	P8	0	Pull Up	Chip-select output from the device. Device is a master connected to serial flash slave.
OSDI for Social	QSPI_CLK	R10	0	Pull Down	Clock output from the device. Device is a master connected to serial flash slave.
QSPI for Serial Flash	QSPI[0]	R11	Ю	Pull Down	Data IN/OUT
	QSPI[1]	P9	Ю	Pull Down	Data IN/OUT
	QSPI[2]	R12	Ю	Pull Up	Data IN/OUT
	QSPI[3]	P10	Ю	Pull Up	Data IN/OUT
Flash	RS232_TX	N6	0	Pull Down	
programming and RS232 UART	RS232_RX	N5	I	Pull Up	UART pins for programming external flash in preproduction/debug hardware.
	Analog Test1 / GPADC1	P1	Ю	_	GP ADC channel 1
Test and Debug output for	Analog Test2 / GPADC2	P2	Ю	_	GP ADC channel 2
preproduction phase. Can be pinned out on production hardware for	Analog Test3 / GPADC3	P3	Ю		GP ADC channel 3
	Analog Test4 / GPADC4	R2	Ю	_	GP ADC channel 4
field debug	ANAMUX / GPADC5	C13	Ю	_	GP ADC channel 5
	VSENSE / GPADC6	C14	Ю	_	GP ADC channel 6

### 4.3 Pin Multiplexing

**Table 4-2. Pin Multiplexing** 

PIN NAME	SIGNAL DESCRIPTION  General Purpose IO  General Purpose IO [IWR14xx]  General Purpose IO  General Purpose IO  Dithered Clock Output for PMIC  General Purpose IO  General Purpose IO	IO O IO IO	Hi-Z	INTERNAL WEAK PULL STATE Weak Pull Down Weak Pull Down
EA00h GPIO_12 P6 1 SPI_HOST1_INTR  0 GPIO_13  EA04h GPIO_0 N4 1 GPIO_0 2 PMIC_CLKOUT 0 GPIO_16	General Purpose IO [IWR14xx] General Purpose IO General Purpose IO Dithered Clock Output for PMIC General Purpose IO General Purpose IO	0 10 10		
1 SPI_HOST1_INTR 0 GPIO_13  EA04h GPIO_0 N4 1 GPIO_0 2 PMIC_CLKOUT 0 GPIO_16	General Purpose IO General Purpose IO Dithered Clock Output for PMIC General Purpose IO General Purpose IO	10 10 0	Hi-Z	Weak Pull Down
EA04h GPIO_0 N4 1 GPIO_0 2 PMIC_CLKOUT 0 GPIO_16	General Purpose IO  Dithered Clock Output for PMIC  General Purpose IO  General Purpose IO	IO O	Hi-Z	Weak Pull Down
2 PMIC_CLKOUT  0 GPIO_16	Dithered Clock Output for PMIC General Purpose IO General Purpose IO	0		
0 GPIO_16	General Purpose IO General Purpose IO			
1 CDIO 1	General Purpose IO	10		
EA08h GPIO_1 N7 1 GPIO_1	•		Hi-Z	Weak Pull Down
2A0011 0110_1 147		Ю		
2 SYNC_OUT	Low Frequency Synchronization Signal output	0		
0 GPIO_19	General Purpose IO	Ю	Hi-Z	Weak Pull Up
EA0Ch MOSI_1 R8 1 MOSI_1	SPI Channel#1 Data Input	Ю		
2 CAN_RX	CAN Interface	I		
0 GPIO_20	General Purpose IO	Ю	Hi-Z	Weak Pull Up
EA10h MISO_1 P5 1 MISO_1	SPI Channel#1 Data Output	Ю		
2 CAN_TX	CAN Interface	0		
0 GPIO_3	General Purpose IO	Ю	Hi-Z	Weak Pull Up
EA14h	SPI Channel#1 Clock	Ю		
RCOSC_CLK		0		
0 GPIO_30	General Purpose IO	Ю	Hi-Z	Weak Pull Up
EA18h	SPI Channel#1 Chip Select	Ю		
RCOSC_CLK		0		
0 GPIO_21	General Purpose IO	Ю	Hi-Z	
EA1Ch MOSI_2 R3 1 MOSI_2	SPI Channel#2 Data Input	Ю		
2 I2C_SDA	I2C Data	Ю		
0 GPIO_22	General Purpose IO	Ю	Hi-Z	
EA20h MISO_2 P4 1 MISO_2	SPI Channel#2 Data Output	Ю		
2 I2C_SCL	I2C Clock	IO		

<sup>(1)</sup> Register addresses are of the form FFFF XXXXh, where XXXX is listed here.



REGISTER	PIN NAME	PIN	DIGITAL PIN MUX CONFIG		FUNCTION			PAD STATE nReset = 0 [ASSERTED]					
ADDRESS <sup>(1)</sup>	PIN NAME	PIN	VALUE [Bits3:0]	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE					
			0	GPIO_5	General Purpose IO	Ю	Hi-Z						
					1	SPI_CLK_2	SPI Channel#2 Clock	Ю					
EA24h	SPI_CLK_2	R5		MSS_UARTA_RX		Ю							
				6	MSS_UARTB_TX	Debug: Firmware Trace	0						
			7	BSS_UART_TX	Debug: Firmware Trace	0							
			0	GPIO_4	General Purpose IO	Ю	Hi-Z						
			1	SPI_CS_2	SPI Channel#2 Chip Select	Ю							
EA28h S	SPI_CS_2	R4		MSS_UARTA_TX		Ю							
			6	MSS_UARTB_TX	Debug: Firmware Trace	0							
			7	BSS_UART_TX	Debug: Firmware Trace	0							
EA2Ch QSPI[0]		QSPI[0] R11	0	GPIO_8	General Purpose IO	Ю	Hi-Z	Weak Pull Down					
	QSPI[0]		R11	R11	R11	R11	1	QSPI[0]	QSPI Data IN/OUT	Ю			
			2	MISO_2	SPI Channel#1 Data Output	10							
	QSPI[1]		P9	1] P9	0	GPIO_9	General Purpose IO	Ю	Hi-Z	Weak Pull Down			
EA30h		SPI[1] P9			P9	P9	P9	P9	P9	1	QSPI[1]	QSPI Data IN/OUT	Ю
			2	MOSI_2	SPI Channel#2 Data Input	Ю							
EAG4b	000101	D40	0	GPIO_10	General Purpose IO	Ю	Hi-Z	Weak Pull Down					
EA34h	QSPI[2]	R12	1	QSPI[2]	QSPI Data IN/OUT	10							
E A COL	0001101	D40	0	GPIO_11	General Purpose IO	10	Hi-Z	Weak Pull Down					
EA38h	QSPI[3]	P10	1	QSPI[3]	QSPI Data IN/OUT	I							
			0	GPIO_7	General Purpose IO	10	Hi-Z	Weak Pull Down					
EA3Ch	QSPI_CLK	R10	1	QSPI_CLK	QSPI Clock output from the device. Device operates as a master with the serial flash being a slave	0							
			2	SPI_CLK_2	SPI Channel#2 Clock	10							
			0	GPIO_6	General Purpose IO	Ю	Hi-Z	Weak Pull Up					
EA40h	QSPI_CS	P8	1	QSPI_CS	QSPI Chip Select output from the device. Device operates as a master with the serial flash being a slave	0							
			2	SPI_CS_2	SPI Channel#2 Chip Select	IO							

REGISTER	PIN NAME	PIN	DIGITAL PIN MUX CONFIG		FUNCTION		PAD STATE nReset = 0 [ASSERTED]						
ADDRESS <sup>(1)</sup>	PIN NAME	PIN	VALUE [Bits3:0]	SIGNAL NAME SIGNAL DESCRIPTION		SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE					
	NERROR_IN	P7		NERROR_IN	Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware	I	Hi-Z						
	WARM_RESET	N12		WARM_RESET	Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.	Ю	Hi-Z Input	Open Drain					
	NERROR_OUT	N8		NERROR_OUT	Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.	0	Hi-Z	Open Drain					
			0	GPIO_17	General Purpose IO	Ю	Hi-Z	Weak Pull Down					
EA50h	тск	M13	M13	1	TCK	JTAG Clock	I						
LAJOH		1010		WITS	WITS	WITO	WITO	WITO	2	MSS_UARTB_TX	Debug: Firmware Trace	0	
			6	BSS_UART_RX	Debug: Firmware Trace	I							
		L13		0	GPIO_18	General Purpose IO	Ю	Hi-Z	Weak Pull Up				
EA54h	TMS		1	TMS	JTAG Test Mode Select	Ю							
			2	BSS_UART_TX	Debug: Firmware Trace	0							
			0	GPIO_23	General Purpose IO	Ю	Hi-Z	Weak Pull Up					
EA58h	TDI	H13	1	TDI	JTAG Test Data In	I							
				MSS_UARTA_RX		Ю							
			0	GPIO_24	General Purpose IO	Ю	Hi-Z						
			1	TDO	JTAG Test Data Out	0							
				MSS_UARTA_TX		Ю							
EA5Ch	TDO	J13	6	MSS_UARTB_TX	Debug: Firmware Trace	0							
				BSS_UART_TX	Debug: Firmware Trace	0							
			7	SOP0	Sense On Power [Reset] Line Impacts boot mode	I							



REGISTER	PIN NAME	PIN	DIGITAL PIN MUX CONFIG		FUNCTION			PAD STATE et = 0 [ASSERTED]				
ADDRESS <sup>(1)</sup>	PIN NAME		VALUE [Bits3:0]	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE				
			0	GPIO_25	General Purpose IO	Ю	Hi-Z	Weak Pull Down				
EA60h	MCU_CLKOUT	N9	1	MCU_CLKOUT	Programmable clock given out to external MCU or the processor	0						
			10	BSS_UART_RX	Debug: Firmware Trace	I						
			0	GPIO_26	General Purpose IO	Ю	Hi-Z	Weak Pull Down				
			1	GPIO_2	General Purpose IO	Ю						
			7	MSS_UARTB_TX	Debug: Firmware Trace	0						
EA64h	GPIO_2	N13	8	BSS_UART_TX	Debug: Firmware Trace	0						
			9	SYNC_OUT	Low frequency Synchronization signal output	0						
			10	PMIC_CLKOUT	Dithered clock input to PMIC	0						
	PMIC_CLKOUT	_KOUT P13			0	GPIO_27	General Purpose IO	Ю	Hi-Z	Weak Pull Down		
EA68h			1	PMIC_CLKOUT	Dithered Clock Output for PMIC	0						
27.0011				SOP2	Sense On Power [Reset] Line Impacts boot mode	I						
		SYNC_IN N10	N10		0	GPIO_28	General Purpose IO	Ю	Hi-Z	Weak Pull Down		
EA6Ch	SYNC_IN			1	SYNC_IN	Low frequency Synchronization signal input	1					
			6	MSS_UARTB_RX	Debug: Firmware Trace	I						
			0	GPIO_29	General Purpose IO	Ю	Hi-Z	Weak Pull Down				
F 4.70b	SVNC OUT			1	SYNC_OUT	Low frequency Synchronization signal output	0					
EA70h	SYNC_OUT	P11		RCOSC_CLK		0						
								SOP1	Sense On Power [Reset] Line Impacts boot mode	I		
			0	GPIO_15	General Purpose IO	Ю	Hi-Z	Weak Pull Up				
		.S232_RX N5	1	RS232_RX	Debug: Firmware load to RAM	Ю						
EA74h	RS232_RX		RS232_RX N5	2	MSS_UARTA_RX	FLASH Programming Bootloader Controlled	1					
			6	BSS_UART_TX	Debug: Firmware Trace	0						
			7	MSS_UARTB_RX	Debug: Firmware Trace	1						

REGISTER	PIN NAME	PIN	DIGITAL PIN MUX CONFIG	FUNCTION		FUNCTION		FUNCTION		PAD STATE = 0 [ASSERTED]	
ADDRESS <sup>(1)</sup>	FIN NAME	FIIN	VALUE [Bits3:0]	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE			
			0	GPIO_14	General Purpose IO	Ю					
						1	RS232_TX	Debug: Firmware load to RAM	O		
EA78h	RS232_TX	N6	5	MSS_UARTA_TX	FLASH Programming Bootloader Controlled	0					
			6	MSS_UARTB_TX	Debug: Firmware Trace	0					
			7	BSS_UART_TX	Debug: Firmware Trace	0					



### 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating Tj temperature range (unless otherwise noted)

	PARAMETERS	MIN	MAX	UNIT	
VDDIN	1.2 V digital power supply	-0.5	1.4	V	
VIN_SRAM	1.2 V power rail for internal SRAM	-0.5	1.4	V	
VNWA	1.2 V power rail for SRAM array back bias	-0.5	1.4	V	
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	-0.5	3.8	V	
VIOIN_18	1.8 V supply for CMOS IO	-0.5	2	V	
VIN_18CLK	1.8 V supply for clock module	-0.5	2	V	
VIOIN_18DIFF	1.8 V supply for CSI2 port	-0.5	2	V	
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could	-0.5	1.45	V	
VIN_13RF2	be shorted on the board.	orted on the board.		V	
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode where				
VIN_13RF2	external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	-0.5	1.4	V	
VIN_18BB	1.8-V Analog baseband power supply	-0.5	2	V	
VIN_18VCO supply	1.8-V RF VCO supply	-0.5	2	V	
I and and admit	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	-0.3V	VIOIN + 0.3		
Input and output voltage range	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input	VIOIN + 20% up to 20% of signal period		V	
CLKP, CLKM	Input ports for reference crystal	-0.5	2	V	
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	-20	20	mA	
T <sub>J</sub>	Operating junction temperature range	-40	105	°C	
T <sub>STG</sub>	Storage temperature range after soldered onto PC board	-55	150	°C	

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

				VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM)		±2000		
	Electrostatic discharge	Channel device model (CDM)	All other pins	±500	V
		Charged-device model (CDM)	Corner pins	±750	

## 5.3 Power-On Hours (POH)<sup>(1)</sup>

JUNCTION TEMPERATURE (T <sub>j</sub> )	NOMINAL CVDD VOLTAGE (V)		POWER-ON HOURS [POH] (HOURS)		
90% at 85℃ T <sub>j</sub> 10% at 105℃ T <sub>j</sub>	50% duty cycle	1.2	80,000		
100% at 85°C T <sub>j</sub>			100,000		

<sup>(1)</sup> This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

<sup>(2)</sup> All voltage values are with respect to V<sub>SS</sub>, unless otherwise noted.



### 5.4 Recommended Operating Conditions

Tjunction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V)	3.15	3.3	3.45	V
VIOIN	I/O supply (1.8 V)	1.14 1.2 3.15 3.3 1.71 1.8 1.71 1.8 1.71 1.8 1.71 1.8 1.71 1.8 1.71 1.8 1.171 1.8 1.171 1.8 1.71 1.8 1.71 1.8 1.71 1.8 1.71 1.8 1.71 1.8 1.71 1.8	1.89	V	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2	4.00	4.0	4.00	.,
VIN_13RF2	could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF1 (1-V Internal LDO bypass mode) VIN_13RF2 (1-V Internal LDO bypass mode)	Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	0.95	1	1.05	٧
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
.,	Voltage Input High (1.8 V mode)	1.17		.,	
V <sub>IH</sub>	Voltage Input High (3.3 V mode)	2.25			V
.,	Voltage Input Low (1.8 V mode)			0.3*VIOIN	.,
$V_{IL}$	Voltage Input Low (3.3 V mode)			0.62	V
	High-level output threshold (I <sub>OH</sub> = 6 mA) (1.8V)	85%*VIOIN			
V <sub>OH</sub>	s configuration, the internal LDO of the device would be of bypassed.  S-V Analog baseband power supply  1.71  1.8  1.9  Itage Input High (1.8 V mode)  Itage Input Low (1.8 V mode)  Itage Input Low (1.8 V mode)  O.3*VIOIN  Itage Input Low (3.3 V mode)  O.3*VIOIN  Itage Input Low (3.3 V mode)  O.62  Itage Input Low (1.8 V mode)  O.62  Itage Input Low (3.3 V mode)  O.62	mV			
V <sub>OL</sub>	Low-level output threshold (I <sub>OL</sub> = 6 mA)			450	mV
	V <sub>IL</sub> (1.8V Mode)			0.2	
NRESET	V <sub>IH</sub> (1.8V Mode)	0.96			
SOP[2:0]	V <sub>IL</sub> (3.3V Mode)			0.3	V
	V <sub>IH</sub> (3.3V Mode)	1.57			

### 5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the IWR1443 device.

**Table 5-1. Power Supply Rails Characteristics** 

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM, VNWA



The 1.3V (1.0V) and 1.8V power supply ripple specifications mentioned in Table 5-2 are defined to meet a target spur level of -105dBc (RF Pin = -15dBm) at the RX. The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to a  $\sim$ 1dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

**Table 5-2. Ripple Specifications** 

	RF RAI	VCO/IF RAIL	
FREQUENCY (kHz)	1.0 V (INTERNAL LDO BYPASS) (µV <sub>RMS</sub> )	1.3 V (μV <sub>RMS</sub> )	1.8 V (μV <sub>RMS</sub> )
137.5	744	648	83
275	4	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

### 5.6 Power Consumption Summary

Table 5-3 and Table 5-4 summarize the power consumption at the power terminals.

**Table 5-3. Maximum Current Ratings at Power Terminals** 

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			500	
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V rail			2000	m Λ
Current consumption	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	mA
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50	

**Table 5-4. Average Power Consumption at Power Terminals** 

PARAMETER	CONDITION		DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption	1.0-V internal	1TX, 4RX	Sampling: 16 66 MSps compley		1.73		
	LDO bypass mode	2TX, 4RX	Sampling: 16.66 MSps complex Transceiver, 40-ms frame time, 512 chirps, 512 samples/chirp, 8.5-µs interchirp time (50% duty cycle)		1.88		w
	1.3-V internal	1TX, 4RX			1.92		VV
	LDO enabled mode 2TX, 4RX		Data Port: MIPI-CSI-2		2.1		



### 5.7 RF Specification

over recommended operating conditions (unless otherwise noted)

	PARAMETER		MIN	TYP	MAX	UNIT
	Nation Course	76 to 77 GHz		14		ī
	Noise figure	77 to 81 GHz		15		dB
	1-dB compression point <sup>(1)</sup>			-8		dBm
	Maximum gain			48		dB
	Gain range			24		dB
	Gain step size			2		dB
	Image Rejection Ratio (IMRR)			30		dB
	IF bandwidth <sup>(2)</sup>				15	MHz
	A2D sampling rate (real)				37.5	Msps
Possivor	A2D sampling rate (complex)			18.75	Msps	
Receiver	A2D resolution		12		Bits	
	Return loss (S11)			-10		dB
	Gain mismatch variation (over temper	ature)		±0.5		dB
	Phase mismatch variation (over temperature)		±3		0	
	In-band IIP2	RX gain = 30dB IF = 1.5, 2 MHz at -12 dBFS		16		dBm
	Out-of-band IIP2	RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm		24		dBm
	Idle Channel Spurs			-90		dBFS
T	Output power			12		dBm
Transmitter	Amplitude noise		-145		dBc/Hz	
Receiver  Transmitter  Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				100	MHz/µs
subsystem				15 -8 48 24 2 30 15 37.5 18.75 12 -10 ±0.5 ±3 16 24 -90 12 -145 81	dBa/U=	
	Phase noise at 1-MHz offset	77 to 81 GHz		-93		dBc/Hz

<sup>(1) 1-</sup>dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone below the lowest HPF cut-off frequency (50 kHz).

Available HPF Corner Frequencies (kHz)

HPF1 HPF2

175, 235, 350, 700 350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- · Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

<sup>(2)</sup> The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Figure 5-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

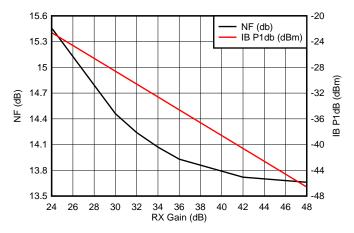


Figure 5-1. Noise Figure, In-band P1dB vs Receiver Gain

### 5.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161]<sup>(1)</sup>

THERMAL I	°C/W <sup>(3)</sup> (4)	
$R\Theta_{JC}$	Junction-to-case	4.92
$R\Theta_{JB}$	Junction-to-board	6.57
$R\Theta_{JA}$	Junction-to-free air	22.3
RΘ <sub>JMA</sub>	Junction-to-moving air	N/A <sup>(1)</sup>
Psi <sub>JT</sub>	Junction-to-package top	4.92
Psi <sub>JB</sub>	Junction-to-board	6.4

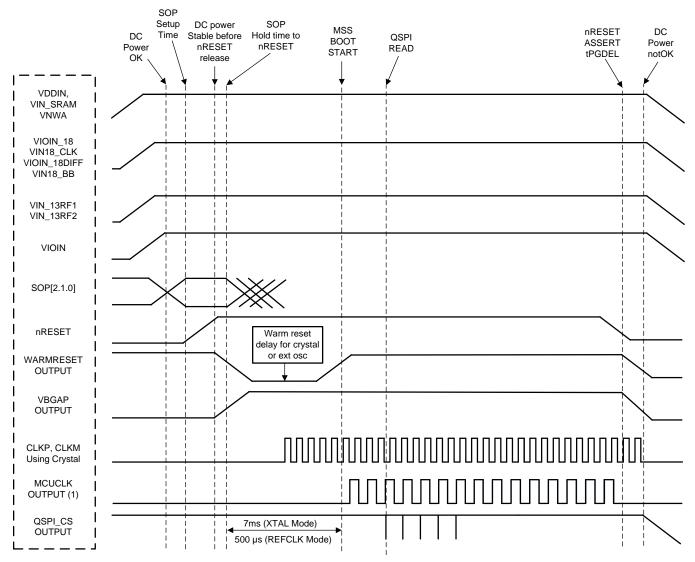
- (1) N/A = not applicable
- 2) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
- (3) °C/W = degrees Celsius per watt.
- (4) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RΘ<sub>JC</sub>] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
  - JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions Natural Convection (Still Air)
  - JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
  - JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
  - JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements
  - A junction temperature of 105°C is assumed.

### 5.9 Timing and Switching Characteristics

### 5.9.1 Power Supply Sequencing and Reset Timing

The IWR1443 device expects all external voltage rails to be stable before reset is deasserted. Figure 5-2 describes the device wake-up sequence.





(1) MCU\_CLK\_OUT in autonomous mode, where IWR1443 application is booted from the serial flash, MCU\_CLK\_OUT is not enabled by default by the device bootloader.

Figure 5-2. Device Wake-up Sequence

#### 5.9.2 Synchronized Frame Triggering

The IWR1443 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC\_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.



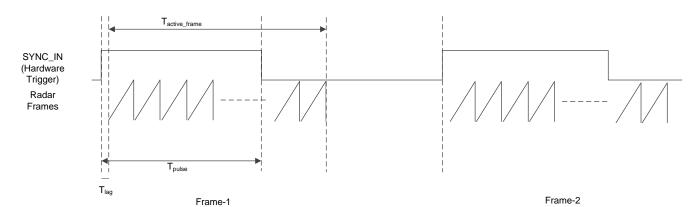


Figure 5-3. Sync In Hardware Trigger

**Table 5-5. Frame Trigger Timing** 

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T <sub>active_frame</sub>	Active frame duration	User defined		20
T <sub>pulse</sub>		25	< T <sub>active_frame</sub>	ns

#### 5.9.3 Input Clocks and Oscillators

#### 5.9.3.1 Clock Specifications

An external crystal is connected to the device pins. Figure 5-4 shows the crystal implementation.

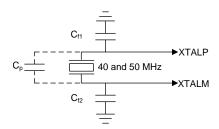


Figure 5-4. Crystal Implementation

#### NOTE

The load capacitors,  $C_{11}$  and  $C_{12}$  in Figure 5-4, should be chosen such that Equation 1 is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

$$C_{L} = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_{P}$$
(1)

Table 5-6 lists the electrical characteristics of the clock crystal.

Table 5-6. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
$f_P$	Parallel resonance crystal frequency	40			MHz
C <sub>L</sub>	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	-40		105	°C
Frequency tolerance	Crystal frequency tolerance (1)(2)(3)	-50		50	ppm
Drive level			50	200	μW

- (1) The crystal manufacturer's specification must satisfy this requirement.
- (2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
- (3) Crystal tolerance affects radar sensor accuracy.



In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. Table 5-7 lists the electrical characteristics of the external clock signal.

**Table 5-7. External Clock Mode Specifications** 

PARAMETER		SPECIFICATION			LIMIT
		MIN	TYP	MAX	UNIT
	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
Input Clock:	Phase Noise at 1 kHz			-132	dBc/Hz
Input Clock: External AC-coupled sine wave or DC-	Phase Noise at 10 kHz			-143	dBc/Hz
coupled square wave Phase Noise referred to 40 MHz	Phase Noise at 100 kHz			-152	dBc/Hz
Phase Noise referred to 40 MHz	Phase Noise at 1 MHz			-153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	-50		50	ppm

#### 5.9.4 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

#### 5.9.4.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

#### 5.9.4.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

Table 5-9 to assume the operating conditions stated in Table 5-8.

**Table 5-8. SPI Timing Conditions** 

		MIN	TYP MAX	UNIT
Input Cond	litions			
t <sub>R</sub>	Input rise time	1	3	ns
t <sub>F</sub>	Input fall time	1	3	ns
Output Conditions				
C <sub>LOAD</sub>	Output load capacitance	2	15	pF



# Table 5-9. SPI Master Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input) $^{(1)(2)(3)}$

NO.		PARAMETER		MIN	TYP MAX	UNIT
1	t <sub>c(SPC)M</sub>	Cycle time, SPICLK <sup>(4)</sup>		25	256 <sub>tc(VCLK)</sub>	ns
2 <sup>(4)</sup>	t <sub>w(SPCH)M</sub>	Pulse duration, SPICLK high (clock polarity = 0	)	0.5t <sub>c(SPC)M</sub> - 4	$0.5t_{c(SPC)M} + 4$	5
2. '	t <sub>w(SPCL)M</sub>	Pulse duration, SPICLK low (clock polarity = 1)	Cclock polarity = 0   Cclock polarity = 1   Cclock polarity = 1   Cclock polarity = 0   Cclock polarity = 1   Cclock polarity = 0   Cclock polarity = 0   Cclock polarity = 0   Cclock polarity = 0   Cclock polarity = 1   Cclock polarity = 0   Cclock polarity = 0	$0.5t_{c(SPC)M} - 4$	$0.5t_{c(SPC)M} + 4$	ns
3 <sup>(4)</sup>	t <sub>w(SPCL)M</sub>	Pulse duration, SPICLK low (clock polarity = 0)	le time, SPICLK (4) se duration, SPICLK high (clock polarity = 0) se duration, SPICLK low (clock polarity = 1) se duration, SPICLK low (clock polarity = 0) se duration, SPICLK low (clock polarity = 0) se duration, SPICLK high (clock polarity = 1) se duration, SPICLK high (clock polarity = 1) se duration, SPICLK high (clock polarity = 1) se duration, SPISIMO valid before SPICLK low, (clock polarity = 0) se duration, SPISIMO valid before SPICLK high, (clock polarity = 1) se duration, SPISIMO valid before SPICLK high, (clock polarity = 1) se duration, SPISIMO valid before SPICLK low, (clock polarity = 1) se duration, SPISIMO valid before SPICLK high, (clock polarity = 1) se duration, SPISIMO valid before SPICLK low control of time, SPICLK low until SPICLK low control of time, SPISIOMI before SPICLK low control of time, SPISIOMI before SPICLK high control of time, SPISIOMI before SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low control of time, SPISIOMI data valid after SPICLK low	$0.5t_{c(SPC)M} - 4$	$0.5t_{c(SPC)M} + 4$	ns
3`'	t <sub>w(SPCH)M</sub>	Pulse duration, SPICLK high (clock polarity = 1	)	$0.5t_{c(SPC)M} - 4$	$0.5t_{c(SPC)M} + 4$	115
4 <sup>(4)</sup>	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low,	(clock polarity = 0)	$0.5t_{c(SPC)M} - 3$		ns
4.7	t <sub>d(SPCL-SIMO)M</sub>	Delay time, SPISIMO valid before SPICLK high	n, (clock polarity = 1)	$0.5t_{c(SPC)M} - 3$		115
5 <sup>(4)</sup>	t <sub>v</sub> (SPCL-SIMO)M	Valid time, SPISIMO data valid after SPICLK lo	O data valid after SPICLK low, (clock polarity = 0)			ns
3\ /	t <sub>v(SPCH-SIMO)M</sub>	Valid time, SPISIMO data valid after SPICLK h	igh, (clock polarity = 1)	$0.5t_{c(SPC)M} - 10.5$		115
	<sup>t</sup> C2TDELAY	Setup time CS active until SPICLK high	CSHOLD = 0	(C2TDELAY+2)*t <sub>c(VCLK</sub>	$(C2TDELAY+2) * t_{c(VCLK)} + 7$	
6 <sup>(5)</sup>		(clock polarity = 0)	CSHOLD = 1	(C2TDELAY +3) * t <sub>c(VCLK)</sub> - 7.5	$\begin{array}{c} \text{(C2TDELAY+3) *} \\ \text{t}_{\text{c(VCLK)}} + 7 \end{array}$	
6(0)		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	(C2TDELAY+2)*t <sub>c(VCLK</sub>	$(C2TDELAY+2) * t_{c(VCLK)} + 7$	ns
			CSHOLD = 1	(C2TDELAY +3) * t <sub>c(VCLK)</sub> - 7.5	$(C2TDELAY+3) * t_{c(VCLK)} + 7$	
7 <sup>(5)</sup>	(5)	Hold time, SPICLK low until CS inactive (clock polarity = 0)  Hold time, SPICLK high until CS inactive (clock polarity = 1)		0.5*t <sub>c(SPC)M</sub> + (T2CDELAY + 1) *t <sub>c(VCLK)</sub> - 7	$0.5^*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$	l
7(5)	†T2CDELAY			0.5*t <sub>c(SPC)M</sub> + (T2CDELAY + 1) *t <sub>c(VCLK)</sub> - 7	$0.5^*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$	ns
8 <sup>(4)</sup>	t <sub>su(SOMI-SPCL)M</sub>	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5		20
8\''	t <sub>su(SOMI-SPCH)M</sub>	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5		ns
9(4)	t <sub>h</sub> (SPCL-SOMI)M	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		3		no
917	t <sub>h</sub> (SPCH-SOMI)M	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3		ns

<sup>(1)</sup> The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).

<sup>(2)</sup> t<sub>c(MSS\_VCLK)</sub> = master subsystem clock time = 1 / f<sub>(MSS\_VCLK)</sub>. For more details, see the Technical Reference Manual.

When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: t<sub>c(SPC)M</sub> ≥ (PS +1)t<sub>c(MSS\_VCLK)</sub> ≥ 25ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: t<sub>c(SPC)M</sub> = 2t<sub>c(MSS\_VCLK)</sub> ≥ 25ns.

<sup>(4)</sup> The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

<sup>(5)</sup> C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

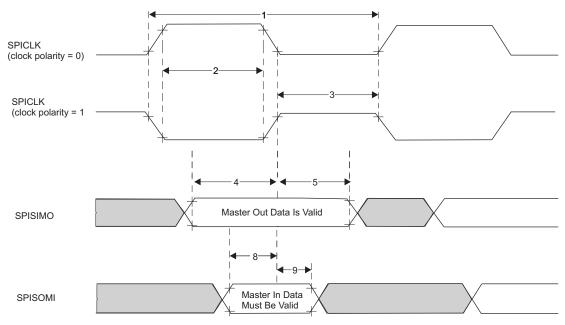


Figure 5-5. SPI Master Mode External Timing (CLOCK PHASE = 0)

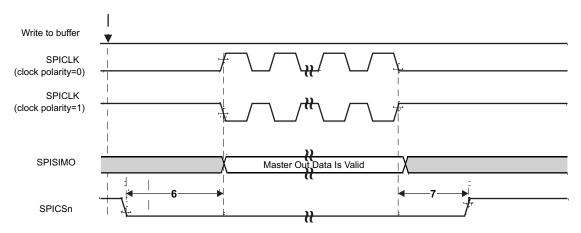


Figure 5-6. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)



# Table 5-10. SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input) $^{(1)(2)(3)}$

NO.		PARAMETER		MIN	TYP MAX	UNIT	
1	t <sub>c(SPC)M</sub>	Cycle time, SPICLK <sup>(4)</sup>		25	256t <sub>c(VCLK)</sub>	ns	
2(4)	t <sub>w(SPCH)M</sub>	Pulse duration, SPICLK high (clock polarity = 0	)	$0.5t_{c(SPC)M} - 4$	$0.5t_{c(SPC)M} + 4$	nc	
2( /	t <sub>w(SPCL)M</sub>	Pulse duration, SPICLK low (clock polarity = 1)		0.5t <sub>c(SPC)M</sub> - 4	$0.5t_{c(SPC)M} + 4$	ns	
3 <sup>(4)</sup>	t <sub>w(SPCL)M</sub>	Pulse duration, SPICLK low (clock polarity = 0)		0.5t <sub>c(SPC)M</sub> - 4	$0.5t_{c(SPC)M} + 4$	no	
3\'/	t <sub>w(SPCH)M</sub>	Pulse duration, SPICLK high (clock polarity = 1)		0.5t <sub>c(SPC)M</sub> - 4	$0.5t_{c(SPC)M} + 4$	ns	
4 (4)	t <sub>d(SPCH-SIMO)M</sub>	Delay time, SPISIMO valid before SPICLK low,	(clock polarity = 0)	$0.5t_{c(SPC)M} - 3$		ns	
4\'/	t <sub>d(SPCL-SIMO)M</sub>	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		0.5t <sub>c(SPC)M</sub> - 3		115	
5 <sup>(4)</sup>	t <sub>v(SPCL-SIMO)M</sub>	Valid time, SPISIMO data valid after SPICLK lo	w, (clock polarity = 0)	$0.5t_{c(SPC)M} - 10.5$		ns	
5.7	t <sub>v(SPCH-SIMO)M</sub>	Valid time, SPISIMO data valid after SPICLK h	igh, (clock polarity = 1)	$0.5t_{c(SPC)M} - 10.5$		115	
		Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5^*t_{c(SPC)M} + (C2TDELAY + 2)^*t_{c(VCLK)} - 7$	$\begin{array}{c} 0.5^*t_{\text{c(SPC)M}} + \\ (\text{C2TDELAY+2}) * \\ t_{\text{c(VCLK)}} + 7.5 \end{array}$		
6 <sup>(5)</sup>	t <sub>C2TDELAY</sub>		CSHOLD = 1	$0.5*t_{\text{c(SPC)M}} + (C2TDELAY + 2)*t_{\text{c(VCLK)}} - 7$	$\begin{array}{c} 0.5^*t_{\text{c(SPC)M}} + \\ (\text{C2TDELAY+2}) * \\ t_{\text{c(VCLK)}} + 7.5 \end{array}$		
0.7		Setup time CS active until SPICLK low	CSHOLD = 0	$0.5^*t_{c(SPC)M} + (C2TDELAY+2)^*t_{c(VCLK)} - 7$	$\begin{array}{c} 0.5^*t_{\text{c(SPC)M}} + \\ (\text{C2TDELAY+2}) * \\ t_{\text{c(VCLK)}} + 7.5 \end{array}$	ns	
		(clock polarity = 1)	CSHOLD = 1	0.5*t <sub>c(SPC)M</sub> + (C2TDELAY+3)*t <sub>c(VCLK)</sub> - 7	$0.5*t_{c(SPC)M} + (C2TDELAY+3)* t_{c(VCLK)} + 7.5$		
7 <sup>(5)</sup>	<b>t</b>	Hold time, SPICLK low until CS inactive (clock	polarity = 0)	(T2CDELAY + 1) *t <sub>c(VCLK)</sub> - 7.5	(T2CDELAY + 1) *t <sub>c(VCLK)</sub> + 7	ns	
7	T2CDELAY	trzcdelay  Hold time, SPICLK high until CS inactive (clock polarity =		Hold time, SPICLK high until CS inactive (clock polarity = 1)	(T2CDELAY + 1) *t <sub>c(VCLK)</sub> - 7.5	(T2CDELAY + 1) *t <sub>c(VCLK)</sub> + 7	115
8 <sup>(4)</sup>	$t_{\text{su(SOMI-SPCL)M}} \qquad \begin{array}{c} \text{Setup time, SPISOMI before SPICLK low} \\ \text{(clock polarity = 0)} \end{array}$			5		ns	
0	t <sub>su(SOMI-SPCH)M</sub>	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5		115	
9(4)	t <sub>h(SPCL-SOMI)M</sub>	Hold time, SPISOMI data valid after SPICLK lo (clock polarity = 0)	w	3		20	
9.7	t <sub>h(SPCH-SOMI)M</sub>	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3		ns	

<sup>(1)</sup> The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set ( where x = 0 or 1 ).

<sup>(2)</sup> t<sub>c(MSS\_VCLK)</sub> = master subsystem clock time = 1 / f<sub>(MSS\_VCLK)</sub>. For more details, see the Technical Reference Manual.

<sup>(3)</sup> When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: t<sub>c(SPC)M</sub> ≥ (PS +1)t<sub>c(MSS\_VCLK)</sub> ≥ 25 ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: t<sub>c(SPC)M</sub> = 2t<sub>c(MSS\_VCLK)</sub> ≥ 25 ns.

<sup>(4)</sup> The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

<sup>(5)</sup> C2TDELAY and T2CDELAY is programmed in the SPIDELAY register



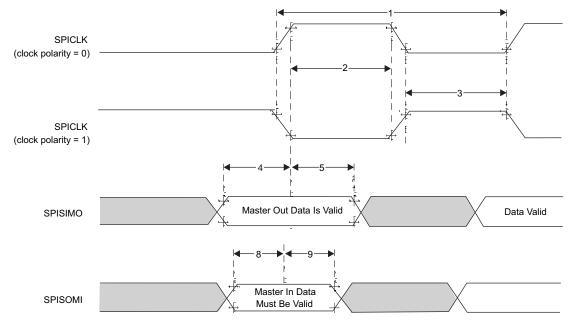


Figure 5-7. SPI Master Mode External Timing (CLOCK PHASE = 1)

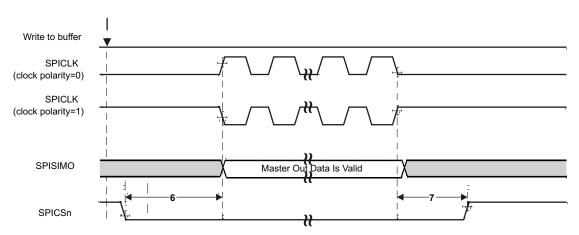


Figure 5-8. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)



#### 5.9.4.3 **SPI Slave Mode I/O Timings**

# Table 5-11. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output) $^{(1)(2)(3)}$

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	t <sub>c(SPC)S</sub>	Cycle time, SPICLK <sup>(4)</sup>	25			ns
2 <sup>(5)</sup>	t <sub>w(SPCH)S</sub>	Pulse duration, SPICLK high (clock polarity = 0)	10			no
2(*)	t <sub>w(SPCL)S</sub>	Pulse duration, SPICLK low (clock polarity = 1)	10			ns
3 <sup>(5)</sup>	t <sub>w(SPCL)S</sub>	Pulse duration, SPICLK low (clock polarity = 0)	10			no
3` ′	t <sub>w(SPCH)S</sub>	Pulse duration, SPICLK high (clock polarity = 1)	10			ns
<b>4</b> <sup>(5)</sup>	t <sub>d(SPCH-SOMI)S</sub>	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	20
4(*)	t <sub>d(SPCL-SOMI)S</sub>	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	ns
5 <sup>(5)</sup>	t <sub>h(SPCH-SOMI)S</sub>	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			
5(-7	t <sub>h(SPCL-SOMI)S</sub>	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			ns
6 <sup>(5)</sup>	t <sub>su(SIMO-SPCL)S</sub>	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	3			
<b>6</b> (e)	t <sub>su(SIMO-SPCH)S</sub>	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	3			ns
7 <sup>(5)</sup>	t <sub>h</sub> (SPCL-SIMO)S	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			
1 1-1	t <sub>h</sub> (SPCL-SIMO)S	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			ns

The MASTER bit (SPIGCRx.0) is cleared ( where x = 0 or 1 ).

The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.

 $t_{c(MSS\_VCLK)}$  = master subsystem clock time = 1 /  $f_{(MSS\_VCLK)}$ . For more details, see the Technical Reference Manual. When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255:  $t_{c(SPC)S} \ge (PS + 1)t_{c(MSS\_VCLK)} \ge 25$  ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0:  $t_{c(SPC)S} = 2t_{c(MSS\_VCLK)} \ge 25$  ns. The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

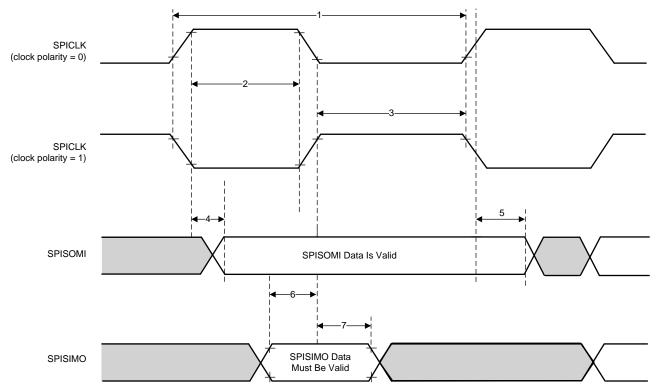


Figure 5-9. SPI Slave Mode External Timing (CLOCK PHASE = 0)

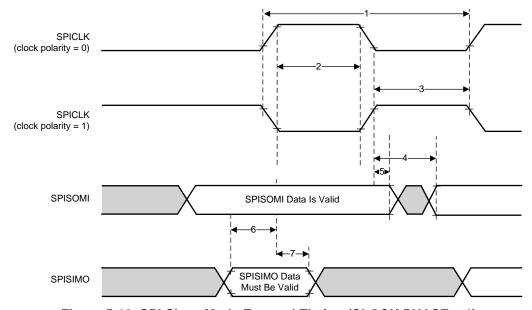


Figure 5-10. SPI Slave Mode External Timing (CLOCK PHASE = 1)



## 5.9.4.4 Typical Interface Protocol Diagram (Slave Mode)

- 1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
- 2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-11 shows the SPI communication timing of the typical interface protocol.

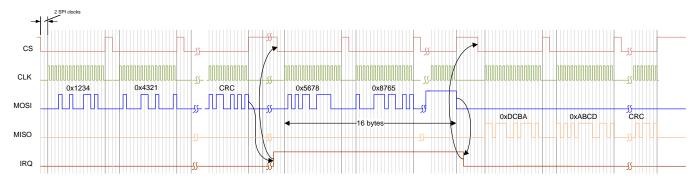


Figure 5-11. SPI Communication

### 5.9.5 LVDS Interface Configuration

The IWR1443 supports seven differential LVDS IOs/Lanes. The lane configuration supported is four Data lanes (LVDS\_TXP/M), one Bit Clock lane (LVDS\_CLKP/M) and one Frame clock lane (LVDS\_FRCLKP/M), and one HS\_DEBUG LVDS pair. The LVDS interface is used for debugging. The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

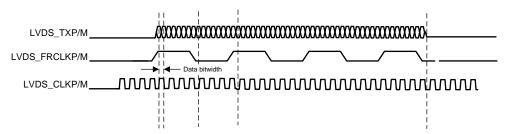


Figure 5-12. LVDS Interface Lane Configuration And Relative Timings

### 5.9.5.1 LVDS Interface Timings

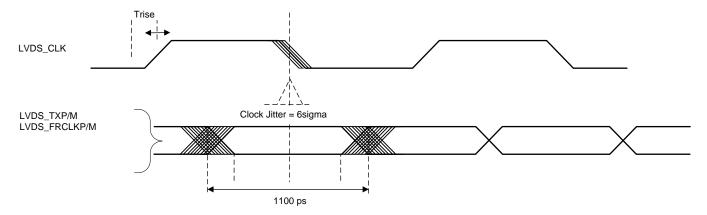


Figure 5-13. Timing Parameters



## **Table 5-12. LVDS Electrical Characteristics**

PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%	52%	
Output Differential Voltage	peak-to-peak single-ended with 100 $\Omega$ resistive load between differential pairs	250	450	mV
Output Offset Voltage		1125	1275	mV
Trise and Tfall	20%-80%, 900 Mbps		500	ps
Jitter (pk-pk)	900 Mbps		80	ps



## 5.9.6 General-Purpose Input/Output

Table 5-13 lists the switching characteristics of output timing relative to load capacitance.

Table 5-13. Switching Characteristics for Output Timing versus Load Capacitance  $(C_L)^{(1)(2)}$ 

	PARAMETER TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT	
			C <sub>L</sub> = 20 pF	2.8	3.0	
t <sub>r</sub>	Max rise time		$C_L = 50 pF$	6.4	6.9	ns
		01	C <sub>L</sub> = 75 pF	9.4	10.2	
		Slew control = 0	C <sub>L</sub> = 20 pF	2.8	2.8	
t <sub>f</sub>	Max fall time		$C_L = 50 pF$	6.4	6.6	ns
			C <sub>L</sub> = 75 pF	9.4	9.8	
			C <sub>L</sub> = 20 pF	3.3	3.3	
t <sub>r</sub>	Max rise time		C <sub>L</sub> = 50 pF	6.7	7.2	ns
		Slew control = 1	C <sub>L</sub> = 75 pF	9.6	10.5	
		Siew Control = 1	C <sub>L</sub> = 20 pF	3.1	3.1	
t <sub>f</sub>	Max fall time		C <sub>L</sub> = 50 pF	6.6	6.6	ns
			C <sub>L</sub> = 75 pF	9.6	9.6	

Slew control, which is configured by PADxx\_CFG\_REG, changes behavior of the output driver (faster or slower output slew rate).

40

The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.



### 5.9.7 Controller Area Network Interface (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring.

The DCAN has the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- · Configurable Message objects
- Individual identifier masks for each message object
- · Programmable FIFO mode for message objects
- Suspend mode for debug support
- · Programmable loop-back modes for self-test operation
- Direct access to Message RAM in test mode
- · Supports two interrupt lines Level 0 and Level 1
- Automatic Message RAM initialization

Table 5-14. Dynamic Characteristics for the DCANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
t <sub>d(CAN_tx)</sub>	Delay time, transmit shift register to CAN_tx pin <sup>(1)</sup>			15	ns
t <sub>d(CAN rx)</sub>	Delay time, CAN_rx pin to receive shift register <sup>(1)</sup>			10	ns

<sup>(1)</sup> These values do not include rise/fall times of the output buffer.

describes the CSI-2 DPHY electrical specifications.

#### 5.9.8 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- · Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232\_RX and RS232\_TX

#### **Table 5-15. SCI Timing Requirements**

	MIN	TYP	MAX	UNIT
f(baud) Supported baud rate at 20 pF		921.6		kHz



## 5.9.9 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I<sup>2</sup>C-bus<sup>™</sup>. This module will support any slave or master I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-master transmitter/ slave receiver mode
  - Multi-master receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- · Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

### **NOTE**

This I2C module does not support:

- High-speed (HS) mode
- · C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)



## Table 5-16. I2C Timing Requirements<sup>(1)</sup>

		STANDARD MODE MIN MAX		FAST MC	DE	LINUT
				MIN	MAX	UNIT
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		μS
t <sub>su(SCLH-SDAL)</sub>	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		μS
t <sub>h(SCLL-SDAL)</sub>	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		μS
t <sub>w(SCLL)</sub>	Pulse duration, SCL low	4.7		1.3		μS
t <sub>w(SCLH)</sub>	Pulse duration, SCL high	4		0.6		μS
t <sub>su(SDA-SCLH)</sub>	Setup time, SDA valid before SCL high	250		100		μS
t <sub>h(SCLL-SDA)</sub>	Hold time, SDA valid after SCL low	0	3.45 <sup>(1)</sup>	0	0.9	μS
t <sub>w(SDAH)</sub>	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		μS
t <sub>su(SCLH-SDAH)</sub>	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		μS
t <sub>w(SP)</sub>	Pulse duration, spike (must be suppressed)			0	50	ns
C <sub>b</sub> (2)(3)	Capacitive load for each bus line		400		400	pF

- The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
- (3)  $C_b = \text{total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.}$

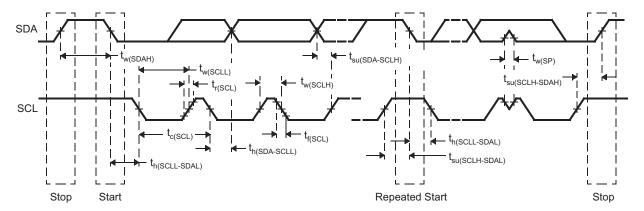


Figure 5-14. I2C Timing Diagram

#### **NOTE**

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t<sub>su(SDA-SCLH)</sub> ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + t<sub>su(SDA-SCLH)</sub>.



## 5.9.10 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI<sup>TM</sup>) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- · Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Table 5-18 and Table 5-19 assume the operating conditions stated in Table 5-17.

Table 5-17. QSPI Timing Conditions

		MIN	TYP MAX	UNIT		
Input Conditions						
$t_R$	Input rise time	1	3	ns		
t <sub>F</sub>	Input fall time	1	3	ns		
Output Con	Output Conditions					
C <sub>LOAD</sub>	Output load capacitance	2	15	pF		

Table 5-18. Timing Requirements for QSPI Input (Read) Timings<sup>(1)(2)</sup>

		MIN	TYP MAX	UNIT
t <sub>su(D-SCLK)</sub>	Setup time, d[3:0] valid before falling sclk edge	7.3		ns
t <sub>h(SCLK-D)</sub>	Hold time, d[3:0] valid after falling sclk edge	1.5		ns
t <sub>su(D-SCLK)</sub>	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 – P <sup>(3)</sup>		ns
t <sub>h(SCLK-D)</sub>	Hold time, final d[3:0] bit valid after final falling sclk edge	1.5 + P <sup>(3)</sup>		ns

<sup>(1)</sup> Clock Mode 0 (clk polarity = 0; clk phase = 0) is the mode of operation.

(3) P = SCLK period in ns.

<sup>(2)</sup> The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.

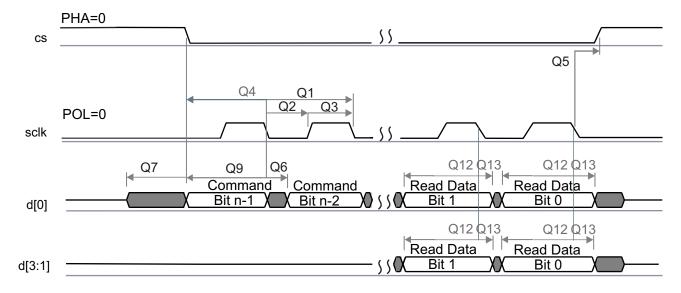


<b>Table 5-19</b>	. QSPI	Switching	Charact	eristics
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NO.		PARAMETER		TYP MAX	UNIT
Q1	t <sub>c(SCLK)</sub> Cycle time, sclk		25		ns
Q2	t <sub>w(SCLKL)</sub>	Pulse duration, sclk low	Y*P - 3 <sup>(1)(2)</sup>		ns
Q3	t <sub>w(SCLKH)</sub>	Pulse duration, sclk high	$Y*P - 3^{(1)}$		ns
Q4	$t_{d(CS\text{-}SCLK)}$ Delay time, sclk falling edge to cs active edge $-M^*P - 1^{(1)(3)}$		-M*P + 2.5 <sup>(1)(3)</sup>	ns	
Q5	t <sub>d(SCLK-CS)</sub>	Delay time, sclk falling edge to cs inactive edge	N*P - 1 <sup>(1)(3)</sup>	N*P + 2.5 <sup>(1)(3)</sup>	ns
Q6	t <sub>d(SCLK-D1)</sub>	Delay time, sclk falling edge to d[1] transition	-3.5	7	ns
Q7	t <sub>ena(CS-D1LZ)</sub>	Enable time, cs active edge to d[1] driven (lo-z)	$-P - 4^{(3)}$	–P +1 <sup>(3)</sup>	ns
Q8	t <sub>dis(CS-D1Z)</sub>	Disable time, cs active edge to d[1] tri-stated (hi-z)	$-P - 4^{(3)}$	–P +1 <sup>(3)</sup>	ns
Q9	t <sub>d(SCLK-D1)</sub>	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	-3.5 - P <sup>(3)</sup>	7 – P <sup>(3)</sup>	ns
Q12	t <sub>su(D-SCLK)</sub>	Setup time, d[3:0] valid before falling sclk edge	7.3		ns
Q13	t <sub>h(SCLK-D)</sub>	Hold time, d[3:0] valid after falling sclk edge	1.5		ns
Q14	t <sub>su(D-SCLK)</sub>	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 — P <sup>(3)</sup>		ns
Q15	th(SCLK-D) Hold time, final d[3:0] bit valid after final falling sclk edge		1.5 + P <sup>(3)</sup>		ns

<sup>(1)</sup> The Y parameter is defined as follows: If DCLK\_DIV is 0 or ODD then, Y equals 0.5. If DCLK\_DIV is EVEN then, Y equals (DCLK\_DIV/2) / (DCLK\_DIV+1). For best performance, it is recommended to use a DCLK\_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2\_H13 output of DPLL\_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK\_DIV can be found in the device-specific Technical Reference Manual.

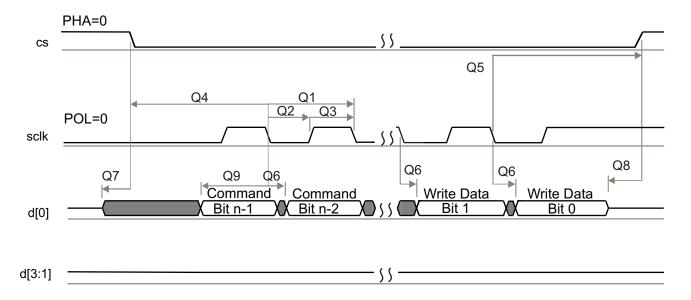
- (2) P = SCLK period in ns.
- (3)  $M = QSPI\_SPI\_DC\_REG.DDx + 1, N = 2$



SPRS85v\_TIMING\_OSPI1\_02

Figure 5-15. QSPI Read (Clock Mode 0)





SPRS85v\_TIMING\_OSPI1\_04

Figure 5-16. QSPI Write (Clock Mode 0)

46



### 5.9.11 JTAG Interface

Table 5-21 and Table 5-22 assume the operating conditions stated in Table 5-20.

## **Table 5-20. JTAG Timing Conditions**

		MIN	TYP MAX	UNIT		
Input Conditions						
t <sub>R</sub>	Input rise time	1	3	ns		
t <sub>F</sub>	Input fall time	1	3	ns		
Output Conditions						
C <sub>LOAD</sub>	Output load capacitance	2	15	pF		

## Table 5-21. Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	TYP	MAX	UNIT
1	t <sub>c(TCK)</sub>	Cycle time TCK	66.66			ns
1a	t <sub>w(TCKH)</sub>	Pulse duration TCK high (40% of tc)	26.67			ns
1b	t <sub>w(TCKL)</sub>	Pulse duration TCK low(40% of tc)	26.67			ns
2	t <sub>su(TDI-TCK)</sub>	Input setup time TDI valid to TCK high	2.5			ns
3	t <sub>su(TMS-TCK)</sub>	Input setup time TMS valid to TCK high	2.5			ns
4	t <sub>h(TCK-TDI)</sub>	Input hold time TDI valid from TCK high	18			ns
4	t <sub>h(TCK-TMS)</sub>	Input hold time TMS valid from TCK high	18			ns

Table 5-22. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	t <sub>d(TCKI-TDOV)</sub>	Delay time. TCK low to TDO valid	0		25	ns

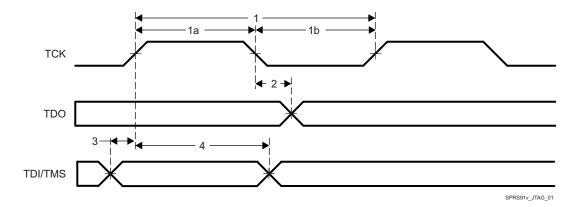


Figure 5-17. JTAG Timing



## 5.9.12 Camera Serial Interface (CSI)

The CSI is a MIPI D-PHY compliant interface for connecting this device to a camera receiver module. This interface is made of four differential lanes; each lane is configurable for carrying data or clock. The polarity of each wire of a lane is also configurable. Table 5-23, Figure 5-18, Figure 5-19, and Figure 5-20 describe the clock and data timing of the CSI.

### **Table 5-23. CSI Switching Characteristics**

over operating Tj temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT			
HPTX							
HOTY	5	(1 or 2 data lane PHY)	150		600		
HSTX <sub>DBR</sub>	Data bit rate	(4 data lane PHY)	150		600	Mbps	
	DDD start (seeman	(1 or 2 data lane PHY)	75		450	N 41 1-	
f <sub>CLK</sub>	DDR clock frequency	(4 data lane PHY)	75		300	MHz	
$\Delta_{\text{VCMTX(LF)}}$	Common-level variation from 75 t frequency	o 450 MHz of CSI2 clock	-50		50	mVpeak	
to and to	20% to 80% rise time and fall time	۵	150			ns	
tR and t	R and t <sub>F</sub> 20% to 80% rise time and fall time				0.3	UI	
LPTX DRIVER							
$t_{\text{RLP}}$ and $t_{\text{FLP}}$	15% to 85% rise time and fall time	e			25	ns	
t <sub>EOT</sub> <sup>(1)</sup>	Time from start of THS-TRAIL per	riod to start of LP-11 state			105 + 12*UI	ns	
	Slew rate. $C_{LOAD} = 0$ to 5 pF	Slew rate. C <sub>LOAD</sub> = 0 to 5 pF			500		
$\delta V/\delta t_{SR}^{(2)(3)(4)}$	Slew rate. $C_{LOAD} = 5$ to 20 pF				200	mV/ns	
	Slew rate. $C_{LOAD} = 20$ to 70 pF				100		
C <sub>LOAD</sub> <sup>(2)</sup>	Load capacitance	Load capacitance			70	pF	
DATA-CLOCK Timing	Specification						
UINOM	Nominal Unit Interval (1, 2, or 3 d	Nominal Unit Interval (1, 2, or 3 data lane PHY)			13.33	ne	
Olivoivi	NOM Nominal Unit Interval (4 data lane PHY) 1.67			13.33	ns		
UIINST,MIN	Minimum instantaneous Unit Interval (1, 2, or 3 data lane PHY)  0.975*U  1.033 INOM –  0.05			ns			
	Minimum instantaneous Unit Inter	Minimum instantaneous Unit Interval (4 data lane PHY)					
TSKEW[TX]	Data to clock skew measured at t	Data to clock skew measured at transmitter -0.15				UIINST, MIN	
CSI2 TIMING SPECIF	FICATION						
T <sub>CLK-MISS</sub>	Time-out for receiver to detect ab disable the clock lane HS-RX.	Time-out for receiver to detect absence of clock transitions and disable the clock lane HS-RX.				ns	
T <sub>CLK-POST</sub>	last associated data lane has tran	Time that the transmitter continues to send HS clock after the last associated data lane has transitioned to lp mode. Interval is defined as the period from the end of T <sub>HS-TRAIL</sub> to the beginning of T <sub>CLK-TRAIL</sub> .				ns	
T <sub>CLK-PRE</sub>		Time that the HS clock shall be driven by the transmitter before any associated data lane beginning the transition from LP to HS mode.				ns	
T <sub>CLK-PREPARE</sub>		Time that the transmitter drives the clock lane LP-00 line state immediately before the HS-0 line state starting the HS 38 transmission.			95	ns	
T <sub>CLK-TERM-EN</sub>		Time for the clock lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.  Time for Dn to reach VTERM-EN				ns	

- 1) With an additional load capacitance CCM of 0 to 60 pF on the termination center tap at RX side of the lane
- (2) While driving C<sub>LOAD</sub>. Load capacitance includes 50 pF of transmission line capacitance, and 10 pF each for TX and RX.
- When the output voltage is from 15% to 85% of the fully settled LP signal levels
- (4) Measured as average across any 50 mV segment of the output signal transition



# Table 5-23. CSI Switching Characteristics (continued)

over operating Tj temperature range (unless otherwise noted)

	MIN	TYP MAX	UNIT	
T <sub>CLK-TRAIL</sub>	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		ns
T <sub>CLK-PREPARE</sub> + T <sub>CLK-ZERO</sub>	$T_{\text{CLK-PREPARE}}$ + time that the transmitter drives the HS-0 state before starting the clock.	300		ns
T <sub>D-TERM-EN</sub>	Time for the data lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN	35 ns + 4*Ul	ns
T <sub>EOT</sub>	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLKTRAIL}$ , to the start of the LP-11 state following a HS burst.		105 ns + n*12*UI	ns
T <sub>HS-PREPARE</sub>	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission	40 + 4*UI	85 + 6*UI	ns
T <sub>HS-PREPARE</sub> + T <sub>HS-ZERO</sub>	T <sub>HS-PREPARE</sub> + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI		ns
T <sub>HS-SKIP</sub>	Time interval during which the HS-RX should ignore any transitions on the data lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	55 ns + 4*Ul	ns
T <sub>HS-EXIT</sub>	Time that the transmitter drives LP-11 following a HS burst.	100		ns
T <sub>HS-TRAIL</sub>	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI) <sup>(5)(6)</sup>		ns
T <sub>LPX</sub>	Transmitted length of any low-power state period	50 <sup>(7)</sup>		ns

- If a > b then max(a, b) = a, otherwise max(a, b) = b. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode (6)
- $T_{\mathsf{LPX}}$  is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

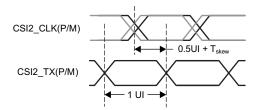


Figure 5-18. Clock and Data Timing in HS Transmission

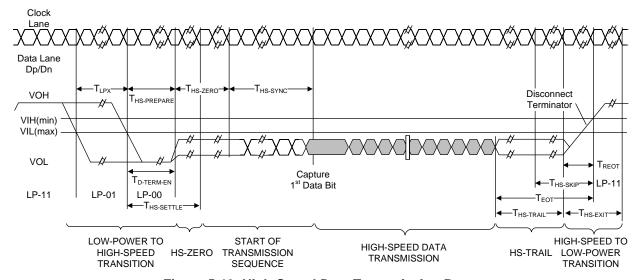
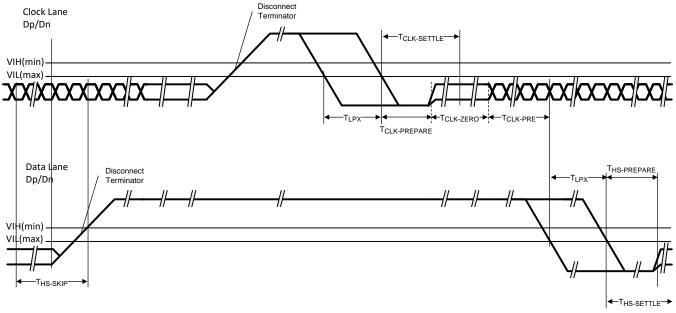


Figure 5-19. High-Speed Data Transmission Burst



(1) The HS to LP transition of the CLK does not actually take place since the CLK is always ON in HS mode.

Figure 5-20. Switching the Clock Lane Between Clock Transmission and Low-Power Mode



## 6 Detailed Description

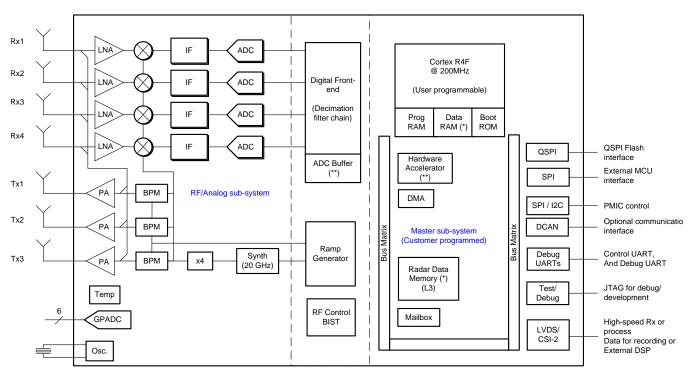
#### 6.1 Overview

The IWR1443 device includes the entire Millimeter Wave blocks and analog baseband signal chain for three transmitters (two usable at the same instance) and four receivers, as well as a customer-programmable MCU with a hardware accelerator for radar signal processing. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity and application code size. These could be cost-sensitive industrial radar sensing applications. Examples are:

- Industrial level sensing
- Industrial automation sensor fusion with radar
- traffic intersection monitoring with radar
- Industrial radar-proximity monitoring.

In terms of scalability, the IWR1443 device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces. Because the IWR1443 device also provides high speed data interfaces like MIPI-CSI2, it is suitable for interfacing with more capable external processing blocks. Here system designers can choose the IWR1443 to provide raw ADC data or use the on-chip Hardware Accelerator for partial processing viz. first stage Fast Fourier Transform.

## 6.2 Functional Block Diagram



(\*) Total RAM available in Master subsystem is divided into ARM-Data RAM, Tightly Coupled Memory, Radar Data Memory, Patch Memory

(\*\*) Shared Memory for ADC Buffer and Hardware Accelerator

### 6.3 External Interfaces

The IWR1443 device provides the following external interfaces:

- Reference Clock Reference clock available for Host Processor after device wakeup.
- · Low speed control information
  - Up to two 4-line standard SPI interface
  - One I<sup>2</sup>C interface (Pin multiplexed with one of the SPI ports)
- One Controller Area Network (CAN) Port for Industrial Interfacing
- Data High-Speed serial port following the MIPI CSI2 format. 4 data and 1 clock lane (all differential). Data from different receive channels can be multiplexed on a single data lane in order to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset Active Low reset for device wakeup from host General Purpose IOs
- Error Signaling Used for notifying the host in case the Radio Controller detects a fault

The IWR1443 device comprises of three main blocks – Radar (or the Millimeter Wave) System, Master (or the Control) System and Processing System.

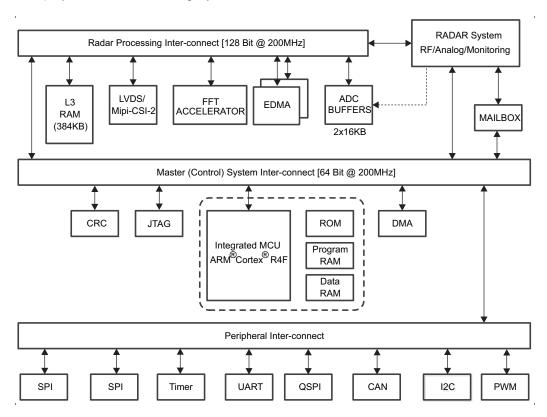


Figure 6-1. System Interconnect

### 6.4 Subsystems

### 6.4.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.



### 6.4.1.1 Clock Subsystem

The IWR1443 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal or external clock. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-2 describes the clock subsystem.

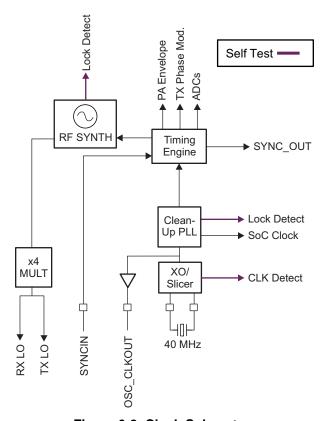


Figure 6-2. Clock Subsystem

### 6.4.1.2 Transmit Subsystem

The IWR1443 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of 2 transmit chains can be operational at the same time. However all 3 chains can be operated together in a time multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 6-3 describes the transmit subsystem.

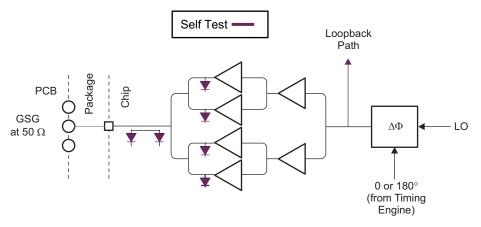


Figure 6-3. Transmit Subsystem (Per Channel)

#### 6.4.1.3 Receive Subsystem

The IWR1443 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the IWR1443 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The IWR1443 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 15 MHz.

Figure 6-4 describes the receive subsystem.

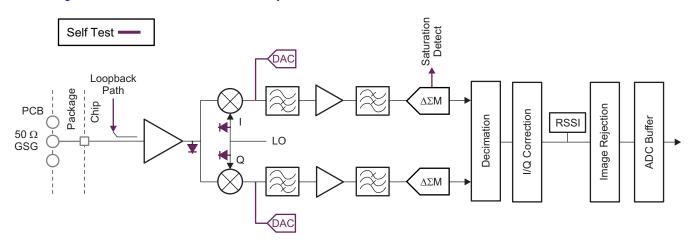


Figure 6-4. Receive Subsystem (Per Channel)



### 6.4.1.4 Radio Processor Subsystem

The Radio Processor subsystem (also referred to as BIST Subsystem in this document) includes the digital front-end, the ramp generator and an internal processor for control / configuration of the low-level RF/analog and ramp generator registers. The Radar Processor also schedules periodic monitoring tasks. User applications, running on

Master (Control) System, do not have direct access to Radar System; access is based on well-defined API messages (over a hardware channel) from the master subsystem.

#### **NOTE**

This radio processor is programmed by TI and takes care of RF calibration and self-test/monitoring functions (BIST). This processor is not available directly for customer use/application.

The digital front-end takes care of filtering and decimating the raw sigma-delta ADC output and provides the final ADC data samples at a programmable sampling rate.

## 6.4.2 Master (Control) System

The Master (Control) System includes ARM's Cortex-R4F processor clocked at 200 MHz, which is user programmable. User applications executing on this processor control the overall operation of the device, including Radar Control via well-defined API messages, radar signal processing (assisted by the radar hardware accelerator) and peripherals for external interface.

The Master (Control) System plays a big role in enabling autonomous operation of IWR1443 as a radar-on-a-chip sensor. The device includes a quad serial peripheral interface (QSPI) which can be used to download customer code directly from a serial flash. A (classic) CAN interface is included that can be used to communicate directly from the device to a CAN bus. An SPI/I2C interface is available for power management IC (PMIC) control when the IWR1443 is used as an autonomous sensor.

For more complex applications, the device can operate under the control of an external MCU, which can communicate with IWR1443 device over an SPI interface. In this case, it is possible to use the IWR14xx as a radar sensor, providing raw detected objects to the external MCU. External MCU could reduce the application code complexity residing in the device and makes more memory available for radar data cube inside the IWR1443. This configuration also eliminates the need for a separate serial flash to be connected to the IWR1443.



The IWR1443 provides for several digital communications outputs; CSI-2 Clk, 4 data formats – can be connected to a remote processor for additional processing. Note: CSI-2 data is from the digital front end or accelerator. When the MSS is used for preprocessing / or another MCU is used in industrial settings the Serial Tx/Rx or CAN bus can provide lower speed communication than CSI-2. The IWR1443 has additional serial Tx/Rx for HART protocol for industrial sensors, or Modbus serial protocol. The SPI port can also provide additional communications or IO control. Additional industrial IO can be Industrial Ethernet or Wifi.

Note that although four interfaces – one CAN, one I2C and two SPI interfaces – are present in the IWR1443 device for external communication and PMIC control, only two of these interfaces are usable at any point in time.

The total memory (RAM) available in the master subsystem is 576 KB. This is partitioned between the R4F program RAM, R4F data RAM and radar data memory. The maximum usable size for R4F is 448 KB and this is partitioned between the R4F's tightly coupled interfaces TCMA (320 KB) and TCMB (128 KB). Although the complete 448 KB is unified memory and can be used for program or data, typical applications use TCMA as program and TCMB as data memory.

The remaining memory, starting at a minimum of 128 KB, is available to be used as radar data memory for storing the 'radar data cube'. It is possible to increase the radar data memory size in 64 KB increments, at the cost of corresponding reduction in R4F program or data RAM size. The maximum size of radar data memory possible is 384 KB. A few example configurations supported are listed in Table 6-1.

Table 6-1. R4F RAM<sup>(1)</sup>

OPTION	R4F PROGRAM RAM	R4F DATA RAM	RADAR DATA MEMORY
1	320KB	128KB	128KB
2	256KB	128KB	192KB
3	256KB	64KB	256KB
4	128KB	64KB	384KB

For IWR1443 ES1.0 and ES2.0, available RAM is 448 KB instead of 576KB.

The Master Subsystem Memory Map is shown in the Technical Reference Manual.



#### 6.4.3 Host Interface

The IWR1443 device communicates with the host radar processor over the following main interfaces:

- Reference Clock Reference clock available for host processor after device wakeup
- Control 4-port standard SPI (slave) for host control. Control UART or CAN can be used as a control
  interface
  - . All radio control commands (and response) flow through this interface.
- Data High-speed serial port following the MIPI CSI2 format (LVDS format can also be used). Four
  data and one clock lane (all differential). Data from different receive channels can be multiplexed on a
  single data lane to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset Active-low reset for device wakeup from host
- Out-of-band interrupt
- Error Used for notifying the host in case the radio controller detects a fault

## 6.5 Accelerators and Coprocessors

The Processing System in the IWR1443 device is an accelerator for FFT operations. The Radar Hardware Accelerator is an IP that enables off-loading the burden of certain frequently used computations in FMCW radar signal processing from the main processor. It is well-known that FMCW radar signal processing involves the use of FFT and Log-Magnitude computations in order to obtain a radar image across the range, velocity and angle dimensions. Some of the frequently used functions in FMCW radar signal processing can be done within the Radar Hardware Accelerator, while still retaining the flexibility of implementing other proprietary algorithms in the Master System processor.

Key features of the Radar Processing Accelerator are:

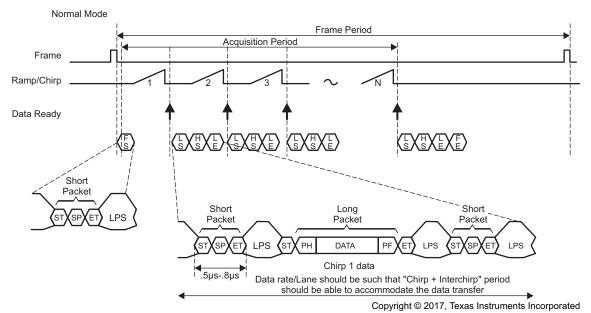
- FFT computation, with programmable FFT sizes (powers of 2) up to 1024-pt complex FFT
- Internal FFT bit-width of 24 bits (each for I and Q) for good SQNR performance, with fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for simple pre-FFT processing specifically, programmable windowing, basic interference zeroing-out and basic BPM removal
- · Magnitude (absolute value) and Log-Magnitude computation capability
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses as required
- Chaining and Looping mechanism to sequence a set of accelerator operations one-after-another with minimal intervention from the main processor
- CFAR-CA detector support (linear and logarithmic)
- Miscellaneous other capabilities of the accelerator
  - Stitching two or four 1024-point FFTs to get the equivalent of 2048-point or 4096-point FFT for industrial level sensing applications where large FFT sizes are required
  - Slow DFT mode, with resolution equivalent to 16K size FFT, for FFT peak interpolation (eg. range interpolation) purpose
  - Complex Vector Multiplication and Dot product capability for vectors of size up to 512

## 6.6 Other Subsystems

### 6.6.1 A2D Data Format Over CSI2 Interface

The IWR1443 device uses MIPI D-PHY / CSI2-based format to transfer the raw A2D samples to the external MCU. This is shown in Figure 6-5.

- Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 600 Mbps per lane
- Virtual channel based
- CRC generation



Frame Start – CSi2 VSYNC Start Short Packet Line Start – CSI2 HSYNC Start Short Packet Line End – CSI2 HSYNC End Short Packet Frame End – CSi2 VSYNC End Short Packet

Figure 6-5. CSI-2 Transmission Format



The data payload is constructed with the following three types of information:

- Chirp profile information
- The actual chirp number
- · A2D data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in Figure 6-6

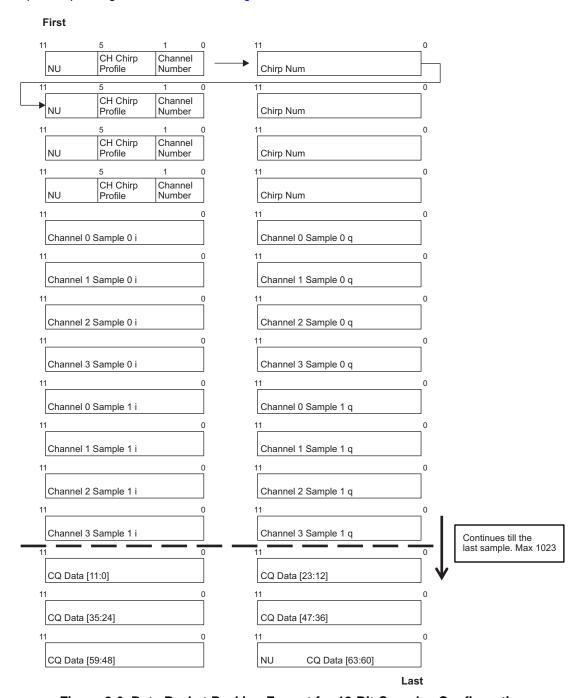


Figure 6-6. Data Packet Packing Format for 12-Bit Complex Configuration



## 6.6.2 ADC Channels (Service) for User Application

The IWR1443 device includes provision for an ADC service for user application, where the

GPADC engine present inside the device can be used to measure up to six external voltages. The GPADC1, GPADC2, GPADC3, GPADC4, GPADC5, and GPADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on the Master R4.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog
  monitoring operations. The API allows configuring the settling time (number of ADC samples to skip)
  and number of consecutive samples to take. At the end of a frame, the minimum, maximum and
  average of the readings will be reported for each of the monitored voltages.

#### **GPADC Specifications:**

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer (0.4-1.3V input range) is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (ADC channel mapped to C14, the internal buffer is not available).

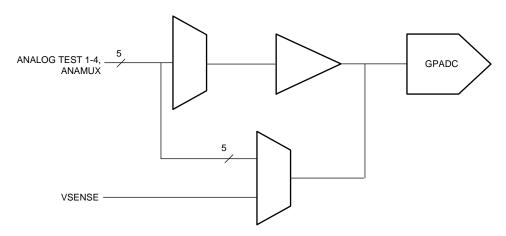


Figure 6-7. ADC Path

Table 6-2. GP-ADC Parameter

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range <sup>(1)</sup>	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	-1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate (2)	625	Ksps
ADC sampling time (2)	400	ns
ADC internal cap		pF
ADC buffer input capacitance		pF

(1) Outside of given range, the buffer output will become nonlinear.

(2) ADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.



# Table 6-2. GP-ADC Parameter (continued)

PARAMETER	TYP	UNIT
ADC input leakage current	3	uA



#### 6.7 Identification

The JTAG identification code is described in the IWR1443 Errata.

The JTAG interface provides the XDS emulator and boundary scan connectivity to the IWR1443.

Table 6-3. JTAG Interface

Signal	SoC Pin	Name	Туре	Function
TCK	M13	Test Clock	Input	Free Running clock when used with emulators viz. Spectrum Digital's XDS200 or TI's XDS110
TMS	L13	Test Mode Select	Input	Directs the next state of the JTAG state machine
TDI	H13	Test Data Input	Input	Scan Data Input to the device
TDO	J13	Test Data Output	Output	Scan Data Output of the device

### 6.8 Boot Modes

As soon as device reset is de-asserted, the R4F processor of the Master (Control) system starts executing its bootloader from an on-chip ROM memory.

The bootloader of the Master system operates in two basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as "Sense on Power" (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

Table 6-4 enumerates the relevant SOP combinations and how these map to bootloader operation.

**Table 6-4. SOP Combinations** 

SOP2 (P13)	SOP1 (P11)	SOP0 (J13)	BOOTLOADER MODE AND OPERATION
0	0	1	Functional Mode Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it
1	0	1	Flashing Mode Device Bootloader spins in loop to allow flashing of user application (or device firmware patch – Supplied by TI) to the serial flash
0	1	1	Debug Mode Bootloader is bypassed and R4F processor is halted. This allows user to connect emulator at a known point



### 6.8.1 Flashing Mode

In Flashing Mode, the Master System's bootloader enables the UART driver and expects a data stream comprising of User Application (Binary Image) and Device Firmware (referred to as Device Firmware Patch or Service Pack) from an external flashing utility. Figure 6-8 shows the flashing utility executing on a PC platform, but the protocol can be accomplished on an embedded platform as well.

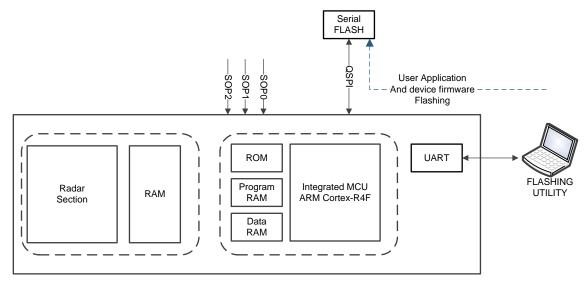


Figure 6-8. Figure 5. Bootloader Flashing Mode

#### 6.8.2 Functional Mode

In Functional Mode, the Master System's bootloader looks for a valid image in the serial flash memory, interfaced over the QSPI port. If a valid image is found, the bootloader transfers the same to Master System's memory subsystem. The image format contains the MSS application code and the radar subsystem patch code.

If a valid image (or the QSPI Serial Flash is not found), the bootloader initializes the SPI port and awaits for the image transfer. This operation comes handy for configurations where the IWR1443 is interfaced to an external processor which has its own nonvolatile storage hence can store the user application and the IWR1443 device's firmware image.

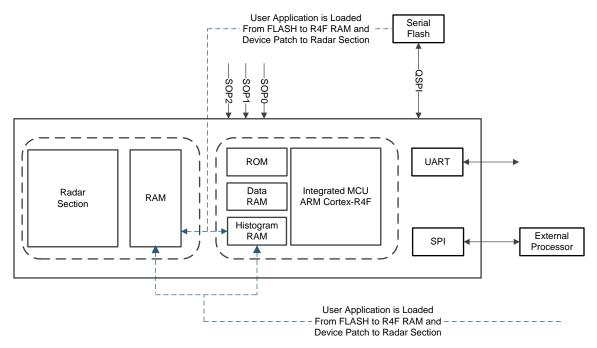


Figure 6-9. Bootloader's Functional Mode

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# 7 Applications, Implementation, and Layout

### **NOTE**

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Application Information

Application information can be found on IWR Application web page.

### 7.2 Reference Schematic

The reference schematic and power supply information can be found in the IWR1443 EVM Documentation.

## 7.3 Layout

## 7.3.1 Layout Guidelines

General layout guidelines can be found in the IWR1443 EVM Documentation, IWR1443BOOST Layout and Design Files, and IWR1443BOOST Schematics, Assembly Files, and BOM.

### 7.3.2 Layout Example

The IWR1443 EVM, RF layout can be found in the IWR1443BOOST Layout and Design Files and IWR1443BOOST Schematics, Assembly Files, and BOM.

## 7.3.3 Stackup Details

Layout Stackup details can be found in the IWR1443BOOST Layout and Design Files and IWR1443BOOST Schematics, Assembly Files, and BOM.

There are specific RF guidelines for the RF Tx and Rx. There are additional layout guidelines for other sections in the IWR1443 Checklist for Schematic Review, Layout Review, Bringup/Wakeup.



# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

### 8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *IWR1443*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal

qualification testing.

**TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. Tl's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). Figure 8-1 provides a legend for reading the complete device name for any *IWR1443* device.

For orderable part numbers of *IWR1443* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *IWR1443 Device Errata*.

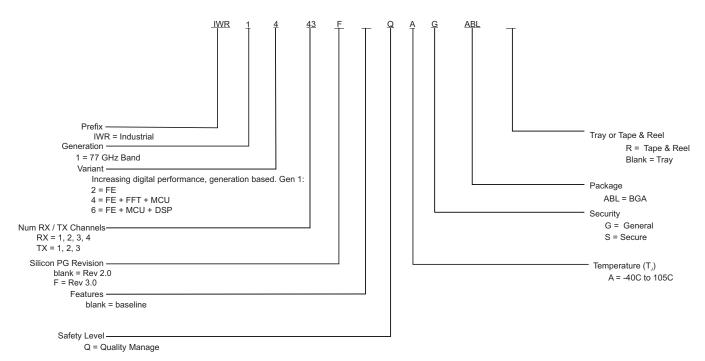


Figure 8-1. Device Nomenclature

#### 8.2 Tools and Software

#### Models

IWR1443 BSDL Model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

IWR1443 IBIS Model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

IVR1443 Checklist for Schematic Review, Layout Review, Bringup/Wakeup A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

## 8.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (IWR1443). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

#### **Errata**

IWR1443 Device Errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.



### 8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

### 8.5 Trademarks

E2E is a trademark of Texas Instruments.
ARM, Cortex are registered trademarks of ARM Limited.
All other trademarks are the property of their respective owners.

## 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

### 8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 9 Mechanical, Packaging, and Orderable Information

## 9.1 Packaging Information

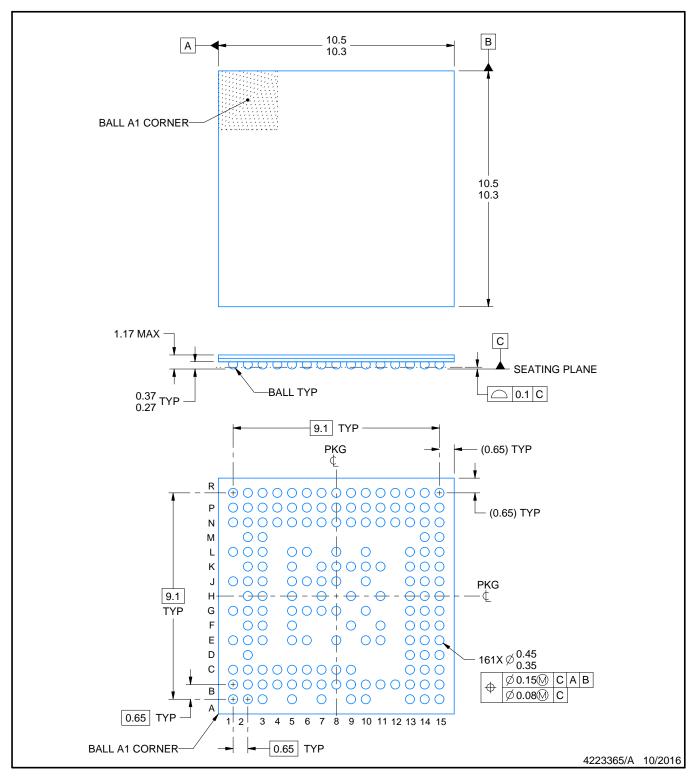
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

#### **CAUTION**

The following package information is subject to change without notice.



PLASTIC BALL GRID ARRAY

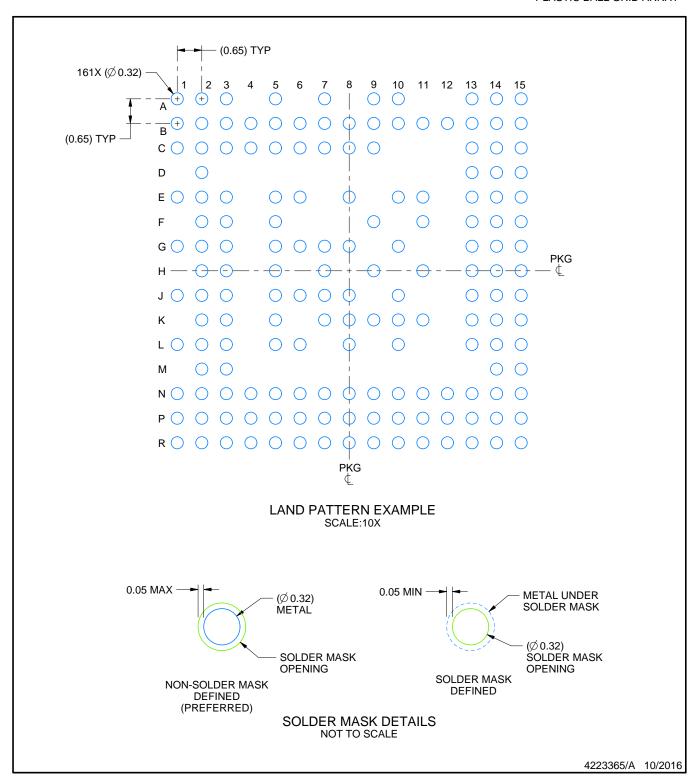


### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC BALL GRID ARRAY

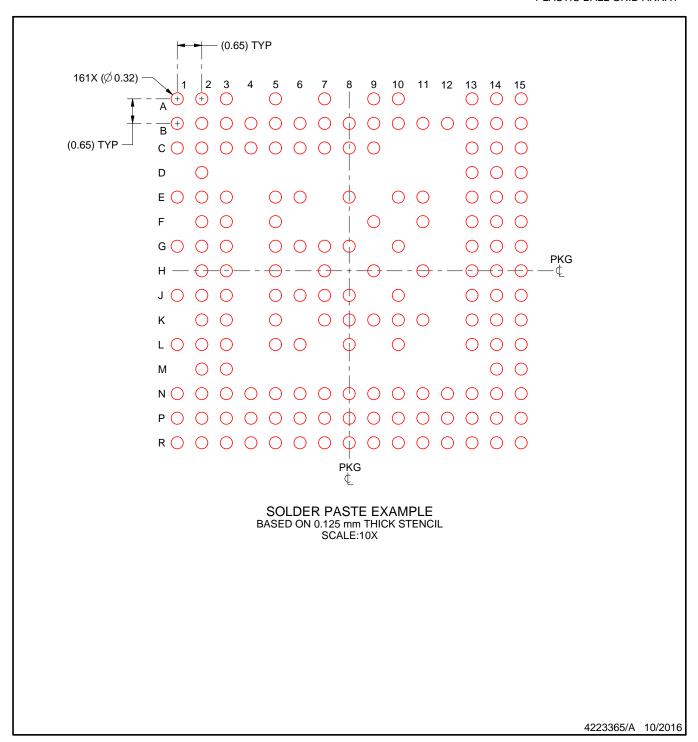


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



PLASTIC BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
IWR1443FQAGABL	ACTIVE	FCCSP	ABL	161	176	RoHS & Green	Call TI   SNAGCU	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC	Samples
IWR1443FQAGABLR	ACTIVE	FCCSP	ABL	161	1000	RoHS & Green	Call TI   SNAGCU	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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### **TRAY**



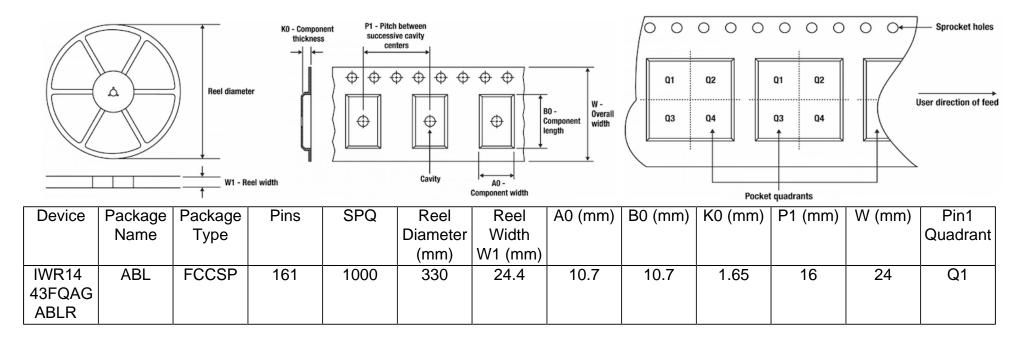
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
IWR1443FQAGABL	ABL	FCCSP	161	176	8 x 22	150	315	135.9	7620	13.4	16.8	17.2



# Carrier Material Report for IWR1443FQAGABLR

# Tape And Reel Information:

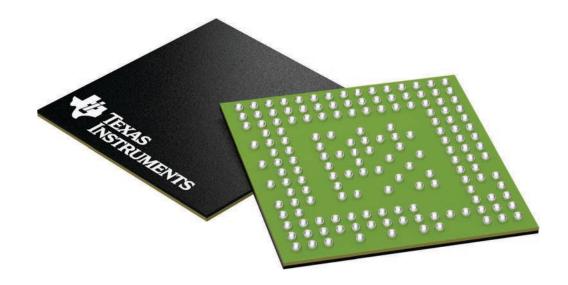


Images above are just a representation of the carrier. Actual carrier may vary. Please reference the dimensions provided in the table.

10.4 x 10.4, 0.65 mm pitch

PLASTIC BALL GRID ARRAY

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
IWR1443FQAGABL	ACTIVE	FCCSP	ABL	161	176	RoHS & Green	Call TI   SNAGCU	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC	Samples
IWR1443FQAGABLR	ACTIVE	FCCSP	ABL	161	1000	RoHS & Green	Call TI   SNAGCU	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC	Samples

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RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
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- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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### **TRAY**



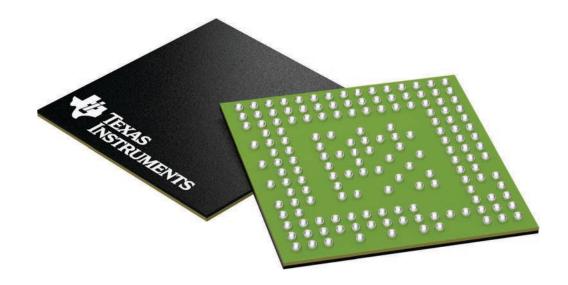
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
IWR1443FQAGABL	ABL	FCCSP	161	176	8 x 22	150	315	135.9	7620	13.4	16.8	17.2

10.4 x 10.4, 0.65 mm pitch

PLASTIC BALL GRID ARRAY

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
IWR1443FQAGABL	Active	Production	FCCSP (ABL)   161	176   JEDEC TRAY (10+1)	·		Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC
IWR1443FQAGABL.B Active Production		FCCSP (ABL)   161	176   JEDEC TRAY (10+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC	
IWR1443FQAGABLR	Active	Production	FCCSP (ABL)   161	1000   LARGE T&R	-	Call TI   Snagcu	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC
IWR1443FQAGABLR.B	Active	Production	FCCSP (ABL)   161	1000   LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## **PACKAGE MATERIALS INFORMATION**

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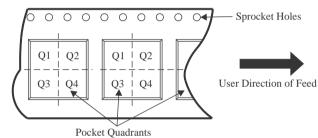
### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
IWR1443FQAGABLR	FCCSP	ABL	161	1000	330.0	24.4	10.7	10.7	1.65	16.0	24.0	Q1

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025



Ì	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	IWR1443FQAGABLR	FCCSP	ABL	161	1000	336.6	336.6	41.3



www.ti.com 23-May-2025

### **TRAY**



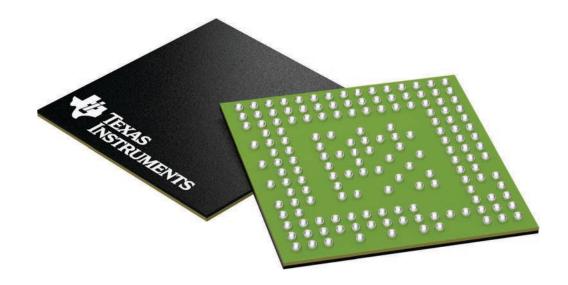
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
IWR1443FQAGABL	ABL	FCCSP	161	176	8 x 22	150	315	135.9	7620	13.4	16.8	17.2
IWR1443FQAGABL.B	ABL	FCCSP	161	176	8 x 22	150	315	135.9	7620	13.4	16.8	17.2

10.4 x 10.4, 0.65 mm pitch

PLASTIC BALL GRID ARRAY

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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