ISOW1050 Robust-EMC, Isolated CAN FD Transceiver With Integrated DC-DC Converter

ADVANCE INFORMATION

1 Features

- Meets the requirements of ISO 11898-2:2016 physical layer standards
  - Support of Classical CAN: 1Mbps
  - Optimized for CAN FD: 2Mbps and 5Mbps
- Integrated low noise DC-DC converter
  - Meets CISPR 32 and EN 55032 Class B with margin on a two-layer PCB
- High efficiency output power
  - Typical efficiency: 41.5%
  - Isolated output voltage accuracy: ± 5%
- Independent power supply for CAN and DC-DC
  - Logic supply (V_{DDL}): 2.25V to 5.5V
  - Power converter supply (V_{DD}): 4.5V to 5.5V
- Fault-Protected CAN FD Transceiver
  - DC Bus fault protection voltage: ± 58V
  - Receiver common mode input voltage: ±12V
- Max Loop delay: 210ns
- Reinforced and Basic isolation options
- High ESD bus protection with respect to GND2
  - HBM ESD: ±12 kV
- Operating temperature range: -55°C to 125°C
- Current limit and thermal shutdown
- 16-pin wide SOIC package
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1-2011 certifications

2 Applications

- Factory Automation
- Building Automation
- Industrial Transport
- Solar Inverters, Protection Relay
- Motor Drives

3 Description

The ISOW1050 device is a isolated controller area network (CAN) transceiver with a built-in isolated DC-DC converter that eliminates the need for a separate isolated power supply in space-constrained isolated designs. The low-emissions, isolated DC-DC meets CISPR 32 radiated emissions Class B standard on a simple two-layer PCB.

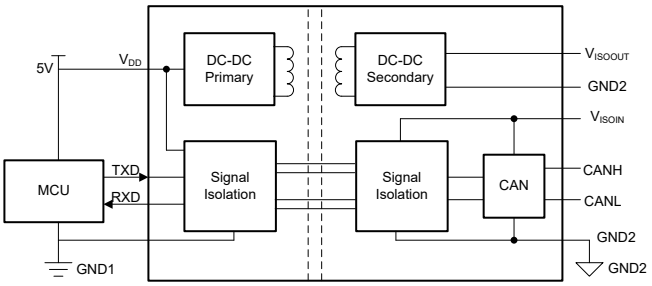
The device supports both classical CAN and CAN FD networks up to 5 Megabits per second (Mbps) data rate. The device offers ±58V DC bus fault protection and ±12V common-mode voltage range. Both signal and power paths are $5kV_{RMS}$ isolated per UL1577 and are qualified for reinforced and basic isolation per VDE, TUV and CQC.

The ISOW1050 device can operate from a single supply voltage of 4.5V to 5.5V . This device supports a wide operating ambient temperature range from –55°C to +125°C and are available in 16-pin DWE (SOIC-16 footprint compatible package) offering a minimum of 8mm creepage and clearance.

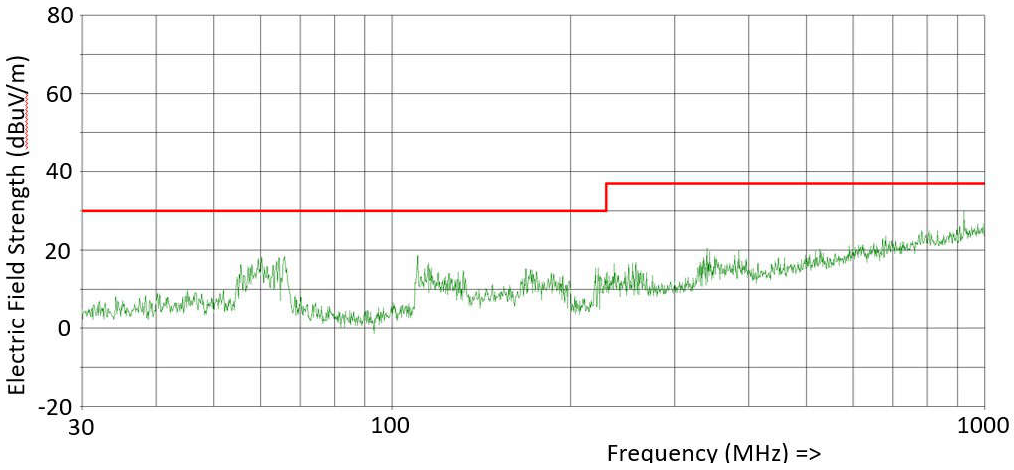
The ISOW1050 includes protection features like thermal-shutdown (TSD) and TXD dominant time-out (DTO). ISOW1050 has two variants, the part with V Suffix has an extra VDDL pin to supply the Logic Dies. So if MCU logic is at different supply rail from the power converter input then there is no need to add a level shifter just give the VDDL supply same as the MCU logic supply.

Package Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)	PACKAGE SIZE (NOM)
ISOW1050	DWE (SOIC, 16)	10.30mm × 7.5mm	10.3mm × 10.30mm
ISOW1050V	DWE (SOIC, 16)	10.30mm × 7.5mm	10.3mm × 10.30mm



Simplified Schematic



ISOW1050 CISPR-32 Radiated Emission Curve With 60Ω Load

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4 Pin Configuration and Functions

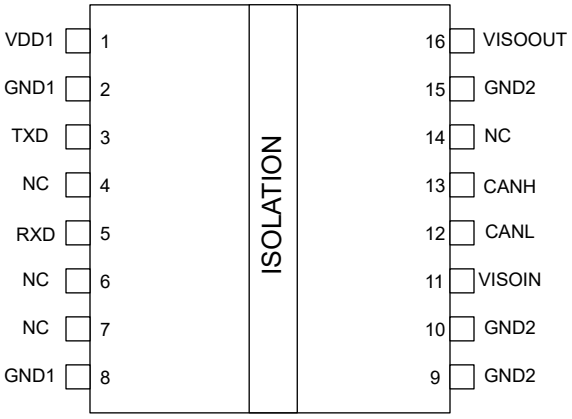

Figure 4-1. ISOW1050 16-pin DWE Top View

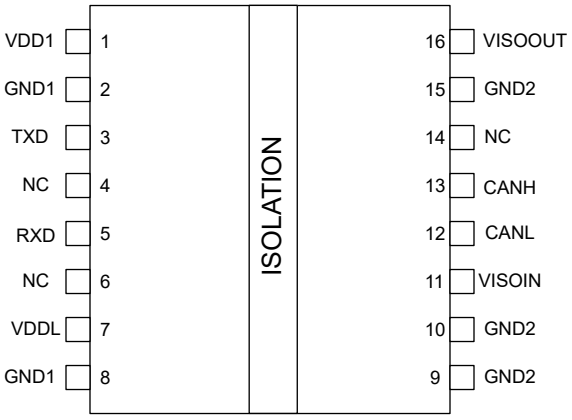

Figure 4-2. ISOW1050V 16-pin DWE Top View

Table 4-1. Pin Functions

PIN			TYPE [1]	DESCRIPTION
NO.	ISOW1050	ISOW1050V		
1	V_{DD}		--	Side 1 Power supply.
3	TXD		I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states).
5	RXD		O	CAN receive data output (LOW for dominant and HIGH for recessive bus states).
2	GND1		--	Ground connection on side 1.
4, 6, 14	NC		--	Not connected internally.
7	NC	V_{DDL}		Logic Pins Power Supply.
8	GND1		--	Ground connections on side for V_{DD}.
9, 10	GND2		--	Ground connections on side for V_{ISOOUT} . V_{ISOOUT} and V_{ISOIN} need be shorted directly on PCB.
16	V_{ISOOUT}		--	Isolated power converter output voltage. V_{ISOOUT} and V_{ISOIN} need be shorted directly on PCB.
11	V_{ISOIN}		I	CAN Power supply. Pin 16 and pin 11 need be shorted directly on PCB.
9, 10, 15	GND2		--	Ground connections for side 2.

Table 4-1. Pin Functions (continued)

PIN			TYPE [1]	DESCRIPTION
NO.	ISOW1050	ISOW1050V		
12	CANL		I/O	Low-level CAN bus line.
13	CANH		I/O	High-level CAN bus line.

(1) I = Input, O = Output; I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Power converter supply voltage	–0.5	6	V
V_{ISOIN}	Isolated supply voltage, input supply for CAN transceiver	–0.5	6	V
V_{ISOOUT}	Isolated supply voltage, Power converter output	–0.5	6	V
V_{DDL}	Logic supply voltage	–0.5	6	V
V_{BUS}	Voltage on bus pins (CANH, CANL with respect to GND2)	–58	58	V
V_{BUS_DIFF}	Max Differential voltage on bus pins (CANH-CANL)	–45	45	V
V_{logic_IO}	Logic Input voltage level (TXD)	–0.5	6	V
V_{logic_IO}	Logic Output voltage level (RXD)(3)	–0.5	V_{CCX} + 0.5V	V
I_O	Output current on RXD pin	–15	15	mA
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.
(3) V_{CCX} = Output side supply;The maximum voltage must not be greater than 6V.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except bus pins	±2000	V
			CANH, CANL Bus pins with respect to GND2 (pin15/16/17)	±12000	
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22C101(2)		±1500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD controlprocess.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD controlprocess.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DDL}	Logic supply voltage	2.25		5.5	V
V_{DD}	Power converter supply voltage	4.75		5.25	V
$V_{DD(UVLO+)}$	Supply threshold when Power converter supply is rising		2.65	2.86	V
$V_{DD(UVLO-)}$	Supply threshold when Power converter supply is falling	2.44	2.56		V
$V_{HYS1(UVLO)}$	Power converter supply voltage hysteresis	78			mV
$V_{DDL(UVLO+)}$	Rising threshold of Logic supply voltage		1.95	2.24	V
$V_{DDL(UVLO-)}$	Falling threshold of Logic supply voltage	1.6	1.78		V
$V_{DDL(UVLO)}$	Logic supply voltage hysteresis	100			mV
V_{IH}	High-level input voltage (TXD input)	0.7 × V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (TXD input)	0		0.3 × V_{IO}	V

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
I_{OH}	High-level output current RXD	V_{IO} = 5V	-4			mA
		V_{IO} = 3.3V	-2			mA
		V_{IO} = 2.5V	-1			mA
I_{OL}	Low-level output current RXD	V_{IO} = 5V			4	mA
		V_{IO} = 3.3V			2	mA
		V_{IO} = 2.5V			1	mA
$1/t_{UI}$	Signaling rate	CAN			5	Mbps
Tpwrup	Power up time after applying input supply (Isolated output supply reaches 90% of setpoint and data transmission can start after this)			5		ms
T_A	Ambient operating temperature	≤ 50% of bits are dominant	–55		125	°C
		> 50% of bits are dominant	–55		105	°C

5.4 Thermal Information

THERMAL METRIC(1)		ISOW1050 DWE 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{IO} = V_{DD} = 5.5V, CAN Bus load R_L= 60Ω, TXD=repetitive pattern of 1ms time period with 990µs LOW time, 10µs HIGH time			901.5	mW
P_{D1}	Maximum power dissipation (side-1)				621.7	mW
P_{D2}	Maximum power dissipation by (side-2)				279.8	mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – signal isolation)	>17	µm
DTI	Distance through the insulation	Minimum internal gap (internal clearance- transformer power isolation)	>100	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage Category	Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1061	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage ISOW1050	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW1050(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW1050(3)	$V_{IOSM} \geq 1.3x\ V_{IMP}$; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; ISOW1050: $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s.	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; ISOW1050: $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2πft), f = 1MHz	3.5	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation (ISOW1050)* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

5.7 Safety-Related Certifications

VDE	UL	TUV	CQC
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned

5.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 70°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			323	mA
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 70°C/W, T_J = 150°C, T_A = 25°C			1.78	W
T_S	Safety temperature(1)				150	°C

(1) The maximum safety temperature,T_S, has the same value as the maximum junction temperature,T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$,where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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5.9 Electrical Characteristics

over recommended operating conditions, typical values are at V_{DD} = 5V and T_A =25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device						
V_{ISOOUT}	Isolated Output supply voltage	TXD floating	4.75	5	5.25	V
TXD TERMINAL						
I_I	Input leakage current	TXD = V_{DD} or GND1	–25		25	µA
C_I	Input capacitance	VIN = 0.4 × sin(2 × π × 1E+6 × t) + 1.65V		2		pF
RXD TERMINAL						
V_{OH}	High level output voltage	I_O = -4mA for 4.5V ≤ V_{DD} ≤ 5.5V, See Figure 6-4	V_{DD} – 0.4	V_{DD} – 0.2		V
V_{OL}	Low level output voltage	I_O = 4mA for 4.5V ≤ V_{DD} ≤ 5.5V, See Figure 6-4		0.2	0.4	V
DRIVER ELECTRICAL CHARACTERISTICS						
$V_{O(DOM)}$	Bus output voltage (Dominant), CANH	TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, and C_L = open, See Figure 6-1 and Figure 6-2	2.75		4.5	V
	Bus output voltage (Dominant), CANL	TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, and C_L = open, See Figure 6-1 and Figure 6-2	0.5		2.25	V
$V_{O(REC)}$	Bus output voltage (recessive), CANH and CANL	TXD = V_{DD} and R_L = open, See Figure 6-1and Figure 6-2	2.0	0.5 × V_{ISOOUT}	3.0	V
$V_{OD(DOM)}$	Differential output voltage (dominant)	TXD = 0V, 45Ω ≤ R_L ≤ 70Ω, and C_L = open, See Figure 6-1 and Figure 6-2	1.4		3.3	V
	Differential output voltage (dominant)	TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, and C_L = open, See Figure 6-1 and Figure 6-2	1.5		3.0	V
	Differential output voltage (dominant)	TXD = 0V, R_L = 2240Ω, and C_L = open, See Figure 6-1 and Figure 6-2	1.5		5.0	V
$V_{OD(REC)}$	Differential output voltage (recessive)	TXD = V_{DD}, R_L = 60Ω, and C_L = open, See Figure 6-1 and Figure 6-2	–120.0		12.0	mV
	Differential output voltage (recessive)	TXD = V_{DD}, R_L = open, and C_L = open, See Figure 6-1 and Figure 6-2	–50.0		50.0	mV
V_{SYM_DC}	Output symmetry (V_{ISOIN} - $V_{O(CANH)}$ - $V_{O(CANL)}$)	R_L = 60Ω and C_L = open, TXD = V_{DD} or GND1, See Figure 6-1 and Figure 6-2	–400.0		400.0	mV
$I_{OS(SS\_DOM)}$	Short circuit current steady state output current, dominant	-15V < CANH < 40V, CANL = open, and TXD = 0V, See Figure 6-8	–115.0			mA
		-15V < CANH < 40V, CANL = open, and TXD = 0V, See Figure 6-8			115.0	mA
$I_{OS(SS\_REC)}$	Short circuit current steady state output current, recessive	−27V < VBUS < 32V, VBUS = CANH = CANL, and TXD = V_{DD}, See Figure 6-8	–5.0		5.0	mA
RECEIVER ELECTRICAL CHARACTERISTICS						
V_{CM}	Input common mode range	See Figure 6-4 and Table 6-1	–12		12	V
V_{IT}	Differential input threshold voltage, normal mode	-12V ≤ V_{CM} ≤ 12V, See Figure 6-4 and Table 6-1	500.0		900.0	mV
V_{HYS}	Hysteresis voltage for differential input threshold, normal mode	-12V ≤ V_{CM} ≤ 12V		80		mV
$V_{DIFF(DOM)}$	Dominant state differential input voltage range, normal mode	-12V ≤ V_{CM} ≤ 12V, See Figure 6-4 and Table 6-1	0.9		9	V
$V_{DIFF(REC)}$	Recessive state differential input voltage range, normal mode	-12V ≤ V_{CM} ≤ 12V, See Figure 6-4 and Table 6-1	–4		0.5	V
$I_{OFF(LKG)}$	power-off bus input leakage current	CANH = CANL = 5V, V_{DD} = GND1			5	µA

over recommended operating conditions, typical values are at V_{DD} = 5V and T_A =25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{DD}			25	pF
C_{ID}	Differential input capacitance	TXD = V_{DD}			11	pF
R_{ID}	Differential input resistance	TXD = V_{DD} ; –12V ≤ V_{CANH} ≤ 12V; –12V ≤ V_{CANH} ≤ 12V	18		90	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD = V_{DD} ; –12V ≤ V_{CANH} ≤ 12V; –12V ≤ V_{CANL} ≤ 12V;	9		45	kΩ
$R_{IN(M)}$	Input resistance matching: (1 - $R_{IN(CANH)}/R_{IN(CANL)}$) × 100%	V_{CANH} = V_{CANL} = 5V	–2		2	%

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5.10 Supply Current Characteristics

Typical values are at V_{DD}=5V, V_{DDL}= 5V, Min/Max over recommended operating conditions, V_{DD} = 4.5V to 5.5V(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} (1)	Power converter supply current	TXD = GND1, Bus dominant, R_L= 60 Ω		123	190	mA
I_{VISOIN}	VISOIN Current	TXD = GND1, Bus dominant, R_L= 60Ω		50	62	mA
I_{DD} (1)	Power converter supply current	TXD = V_{IO}, Bus recessive, R_L = 60Ω		25	44	mA
I_{VISOIN}	VISOIN Current	TXD = V_{IO}, Bus recessive, R_L = 60Ω		7	10	mA
I_{DD} (1)	Power converter supply current	TXD = 1Mbps 50% duty square wave, R_L = 60Ω		75	117	mA
I_{VISOIN}	VISOIN Current	TXD = 1Mbps 50% duty square wave, R_L= 60Ω		29	36	mA
I_{DD} (1)	Power converter supply current	TXD = 5Mbps 50% duty square wave, R_L= 60Ω		76	118	mA
I_{VISOIN}	VISOIN Current	TXD = 5Mbps 50% duty square wave, R_L= 60Ω		29	37	mA
I_{VDDL}	Logic supply current	TXD = GND1, Bus dominant, V_{DDL} = 2.25 to 5.5V (For ISOW1050V)		4.9	6.8	mA
		TXD = V_{IO}, Bus recessive, V_{DDL} = 2.25 to 5.5V (For ISOW1050V)		3.2	4	mA
		TXD = 1Mbps square wave 50% duty, V_{DDL} = 2.25 to 5.5V (For ISOW1050V)		4.1	5.8	mA
		TXD = 5Mbps square wave 50% duty, V_{DDL} = 2.25 to 5.5V (For ISOW1050V)		4.3	6	mA

(1) I_{DD} is the total supply current including the I_{VDDL} for ISOW1050

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5.11 Switching Characteristics

Typical specifications are at V_{DD} = 5V, Min/Max are over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver RXD, recessive to dominant	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns; 4.5V < V_{DD} <5.5V, See Figure 6-6		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver RXD, dominant to recessive	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD =1ns; 4.5V < V_{DD} <5.5V, See Figure 6-6		150	210	ns
DRIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, LOW to HIGH TXD edge to driver recessive (dominant to recessive)	R_L = 60Ω and C_L = 100pF; input rise/fall time (10% to 90%) on TXD =1ns, See Figure 6-3		85	105	ns
t_{pLD}	Propagation delay time, HIGH TO LOW TXD edge to driver dominant (recessive to dominant)			70	105	
$t_{sk(p)}$	pulse skew (|tpHR - tpLD|)			15		
t_R	Differential output signal rise time			26		
t_F	Differential output signal fall time			42		
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}	R_{TERM} = 60Ω, C_L = open, C_{SPLIT} = 4.7nF, TXD = Dominant or recessive or toggling at 250khz, 1Mhz	0.9		1.1	V/V
t_{TXD_DTO}	Dominant time out	R_L = 60Ω and C_L = open, See Figure 6-7	1.2		3.8	ms
RECEIVER SWITCHING CHARACTERISTICS						
t_{pRH}	Propagation delay time, bus dominant to recessive transition to RXD high output (dominant to recessive)	$C_{L(RXD)}$ = 15pF, See Figure 6-5		90	130	ns
t_{pDL}	Propagation delay time, bus recessive to dominant transition to RXD low output (recessive to dominant)			80	105	ns
t_R	Output signal rise time(RXD)			2.5		ns
t_F	Output signal fall time(RXD)			2.5		ns
FD TIMING PARAMETERS						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500ns	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD =1ns, See Figure 6-6	455		510	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200ns	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD =1ns, See Figure 6-6	155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD bus output pins with $t_{BIT(TXD)}$ = 500ns	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD =1ns, See Figure 6-6	420		520	ns
	Bit time on RXD bus output pins with $t_{BIT(TXD)}$ = 200ns	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD =1ns, See Figure 6-6	120		220	ns
ΔtREC	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD =1ns; ΔtREC = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$, See Figure 6-6	-45		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD =1ns; ΔtREC = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$, See Figure 6-6	-45		15	ns

ADVANCE INFORMATION

6 Parameter Measurement Information

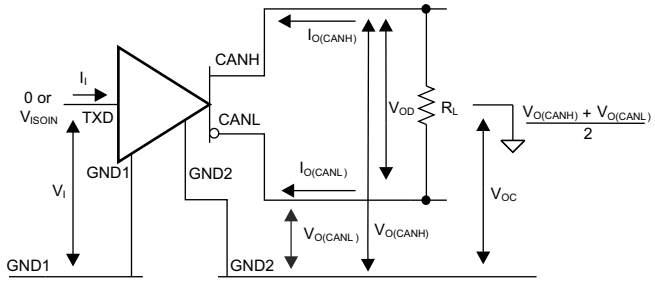


Figure 6-1. Driver Voltage, Current and Test Definitions

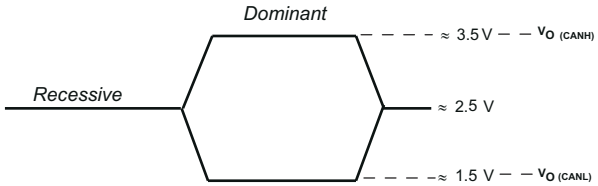
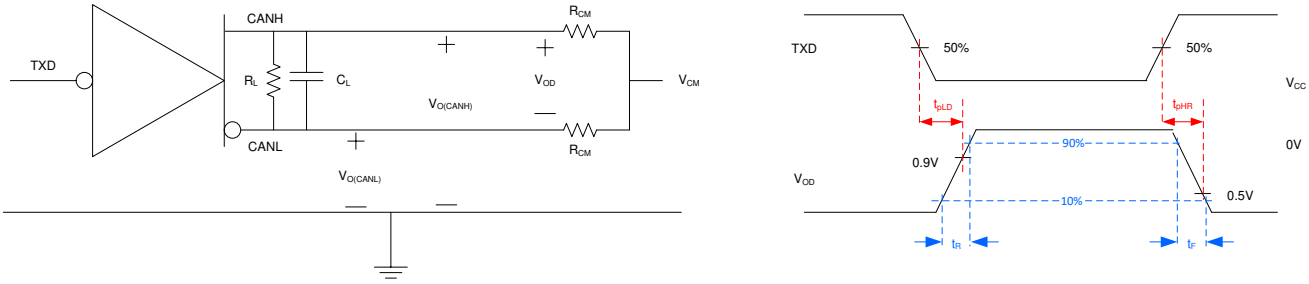


Figure 6-2. Bus Logic State Voltage Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, ZO = 50Ω.

Figure 6-3. Driver Test Circuit and Voltage Waveforms

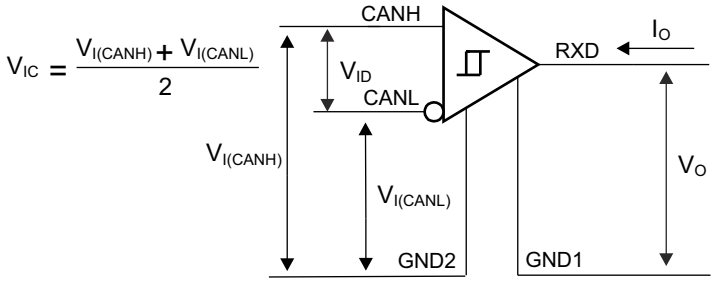
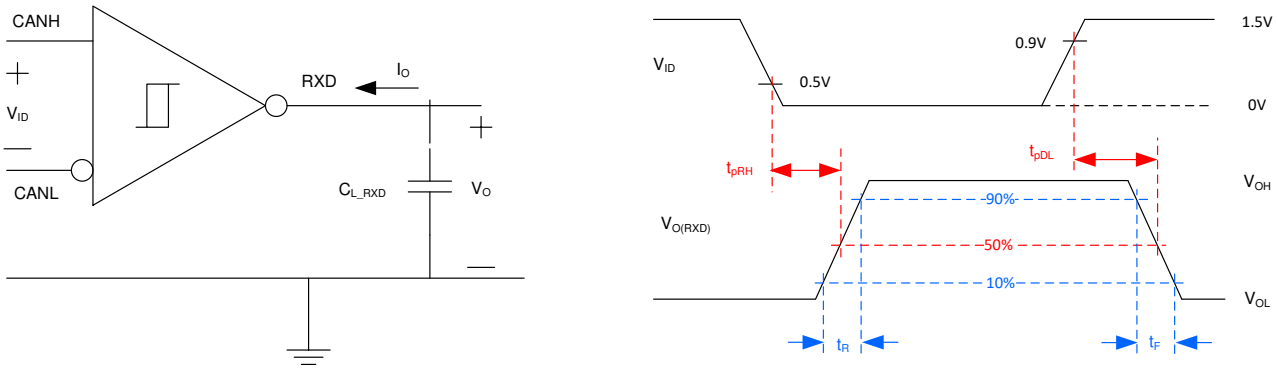


Figure 6-4. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-5. Receiver Test Circuit and Voltage Waveforms

Table 6-1. Receiver Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	RXD	
-11.5V	-12.5V	1000mV	L	V_{OL}
12.5V	11.5V	1000mV	L	
-8.55V	-9.45V	900mV	L	
9.45V	8.55V	900mV	L	
-8.75V	-9.25V	500mV	H	V_{OH}
9.25V	8.75V	500mV	H	
-11.8V	-12.2V	400mV	H	
12.2V	11.8V	400mV	H	
Open	Open	X	H	

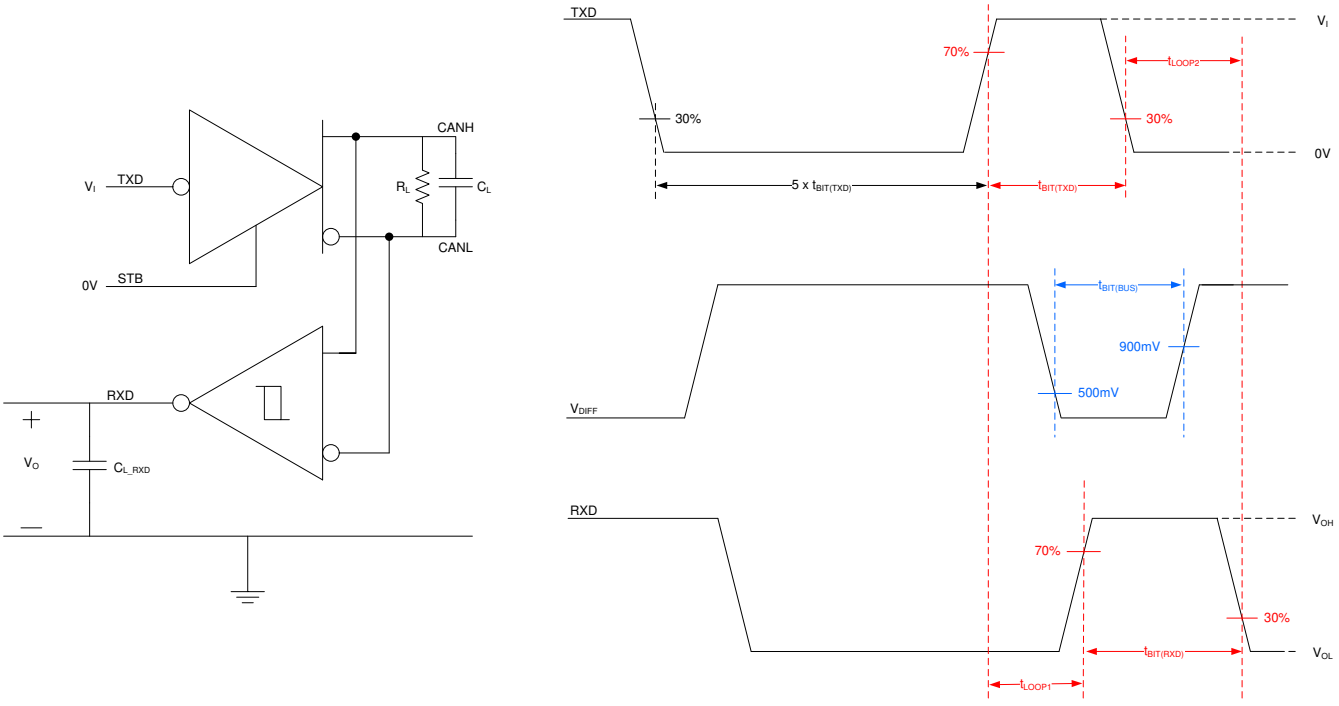


Figure 6-6. t_{LOOP} and CAN FD Timing Parameter Measurement

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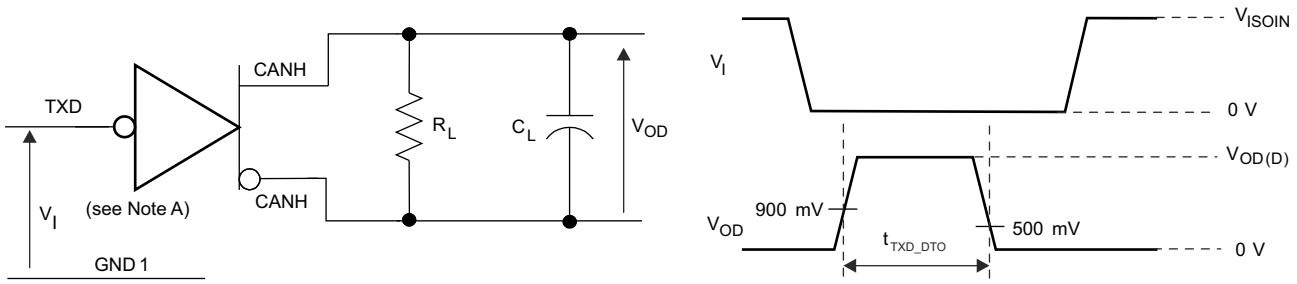

A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-7. Dominant Time-out Test Circuit and Voltage Waveforms

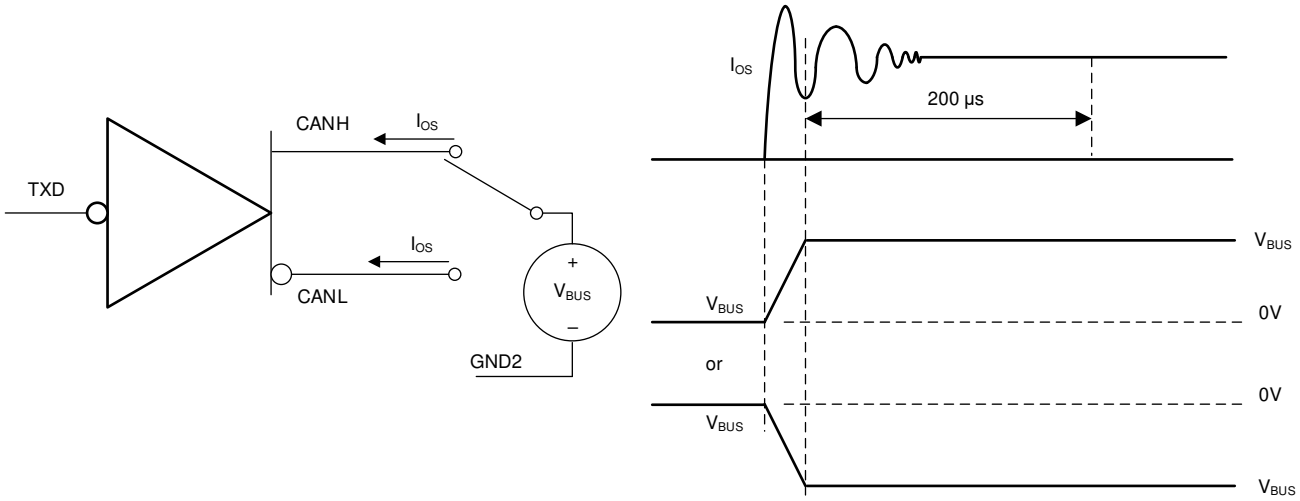

Figure 6-8. Driver Short-Circuit Current Test Circuit and Waveforms

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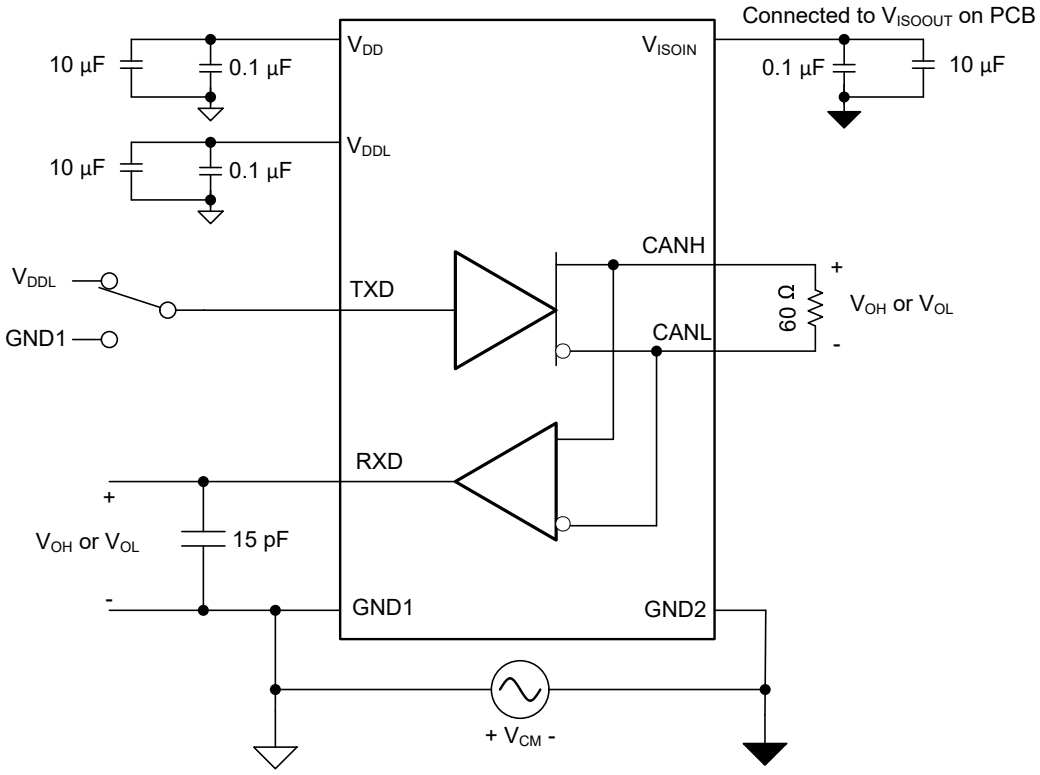

Figure 6-9. Common-Mode Transient Immunity Test Circuit

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7 Detailed Description

7.1 Overview

The ISOW1050 has signal isolation channels, power isolation with integrated transformer and CAN transceiver all integrated in one package. ISOW1050 supports maximum signaling rate up to 1Mbps for CAN, and 5Mbps for CAN FD. Functional Block Diagram shows functional block diagram of ISOW1050.

7.2 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve up to 43.5% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. The output voltage, V_{ISOOUT}, is monitored and feedback information is conveyed to the primary side. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter provides low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{DD} and V_{ISOOUT} supplies which provides robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism provides controlled inrush current and avoids any overshoot on the output during power up.

7.3 Signal Isolation

The integrated signal isolation channels for CAN transceiver employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. Figure 7-2 shows a functional block diagram of a typical signal isolation channel.

7.4 CAN Transceiver

The ISOW1050 device includes a digitally isolated CAN transceiver that offers ±58V DC bus fault protection and ±12V common-mode voltage range. The device supports up to 5Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. The power converter operates from a 5V supply on side 1 (V_{DD}) and a 5V supply on side 2 (V_{ISOOUT}).

7.5 Functional Block Diagram

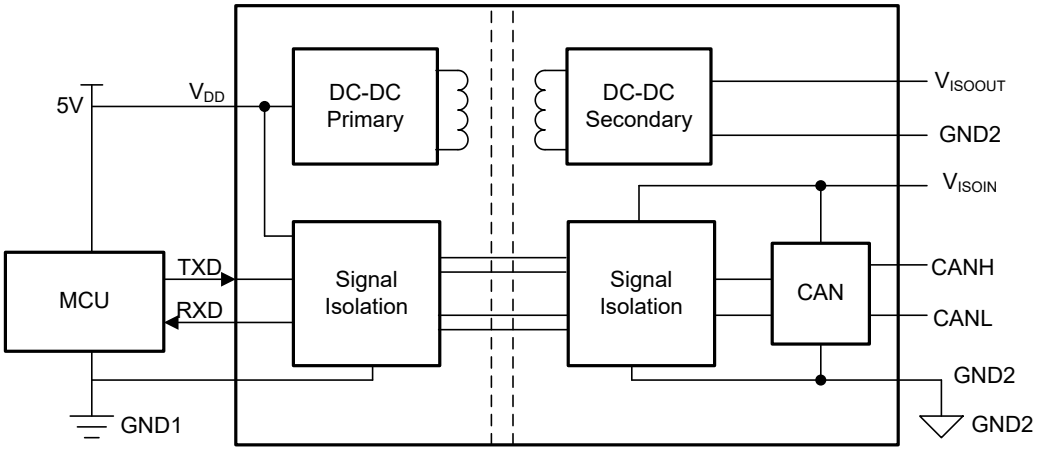

Figure 7-1. Block Diagram

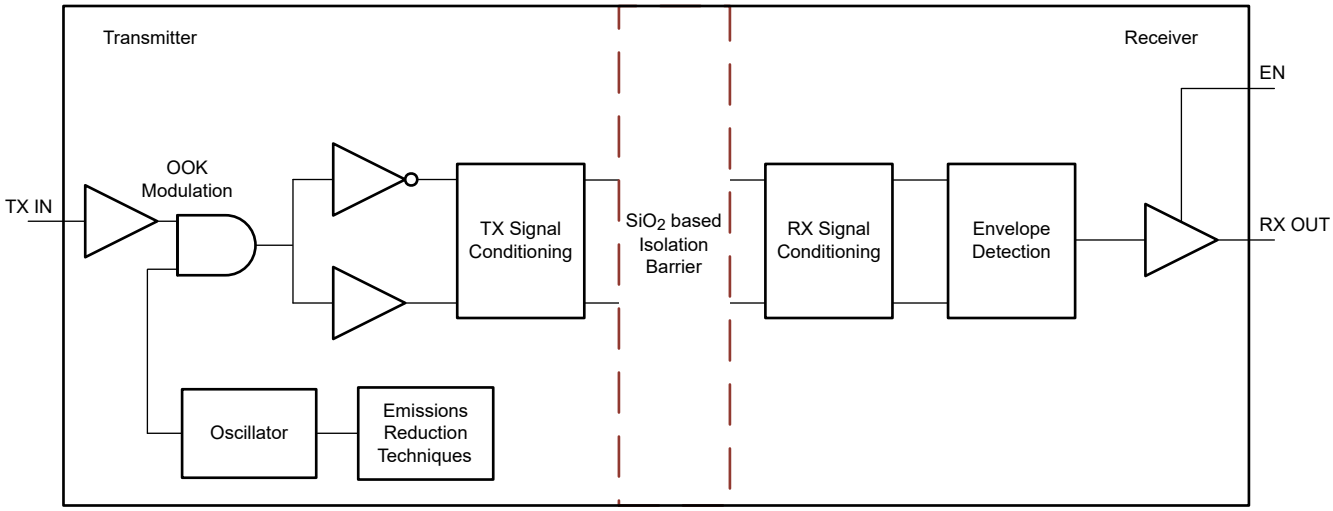

Figure 7-2. Signal Isolation channel

7.6 Feature Description

7.6.1 CAN Bus States

The CAN bus has two logical states during operation: *recessive* and *dominant*. A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes can be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

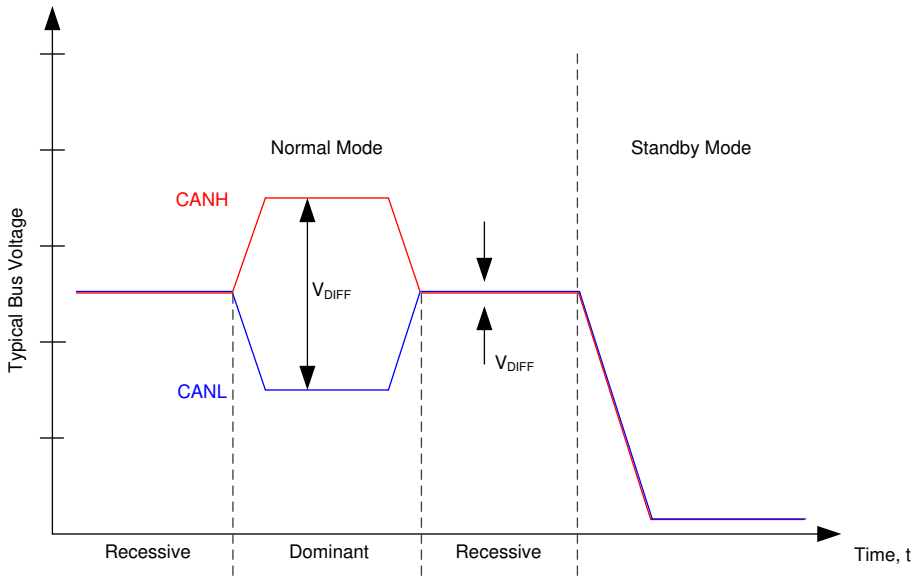

Figure 7-3. Bus States (Physical Bit Representation)

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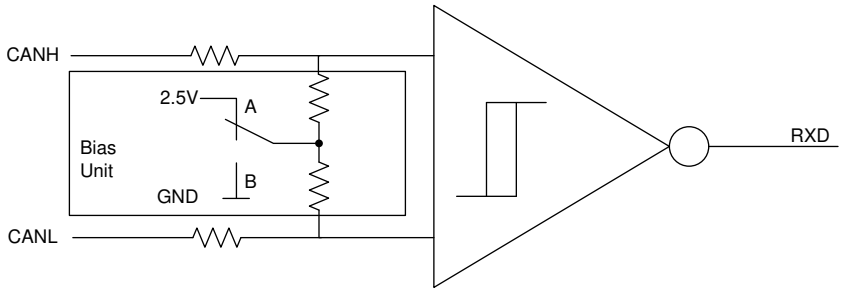

Figure 7-4. Simplified Recessive Common Mode Bias and Receiver

A. A - Normal Mode B - Standby Mode

7.6.2 Digital Inputs and Outputs: TXD (Input) and RXD (Output)

The V_{IO} supply for the isolated digital input and output side of the device can be supplied by 5V supplies and therefore the digital inputs and outputs are 5V compatible.

7.6.3 TXD Dominant Timeout (DTO)

The TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where the TXD pin is held dominant longer than the timeout period, t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on the TXD pin. The DTO circuit disables the CAN bus driver if no rising edge occurs before the timeout period expires, which frees the bus for communication between other nodes on the network. The CAN driver is activated again when a recessive signal occurs on the TXD pin, clearing the TXD DTO condition. The receiver and RXD pin still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

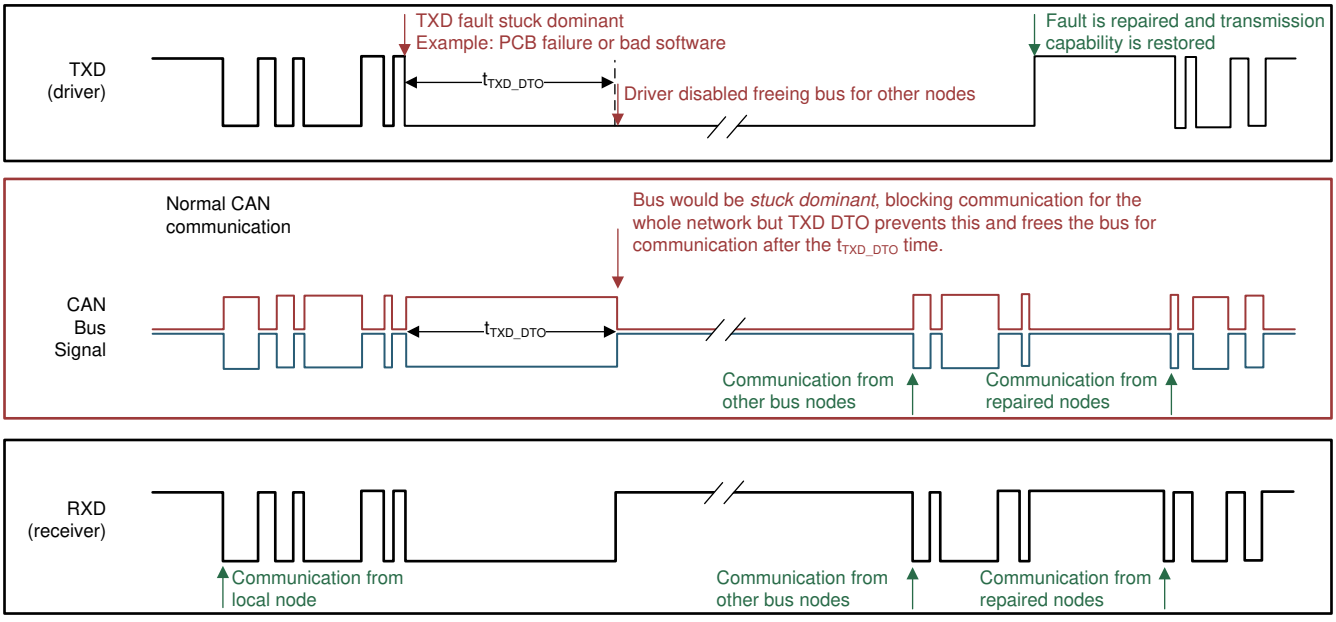

Figure 7-5. Example Timing Diagram for TXD DTO

Note

The minimum dominant TXD time (t_{TXD_DTO}) allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate with Equation 1.

$$\text{Minimum Data Rate} = 11 / t_{TXD\_DTO} \quad (1)$$

7.6.4 Power-Up and Power-Down Behavior

The ISOW1050 has built-in under-voltage lockout (UVLO) on all supplies (V_{DD} and V_{ISOOUT}) with positive-going and negative-going thresholds and hysteresis.

When the V_{DD} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{DD} supply and charges the V_{ISOOUT} output in a controlled manner, avoiding overshoots. CAN BUS is in high impedance state in this duration. When the UVLO positive-going threshold is crossed on the secondary side V_{ISOOUT} pin, feedback is provided to the primary controller. The regulation loop takes over and CAN drive output, Received data output (RXD) take the respective states defined by the inputs to the device like Driver data to be transmitted TXD. Designers must consider a sufficient time margin (typically 5ms with 10µF load capacitance) to allow this power up sequence before any usable system functionality.

When V_{DD} is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISOOUT} capacitor then discharges depending on the isolation channels and BUS load.

7.6.5 Protection Features

The ISOW1050 device has multiple protection features to create a robust system level design.

- In cases of overload or short on power converter output V_{ISOOUT}, maximum duty cycle of power converter is limited. In cases of driver bus short circuit due to the external power supply cable shorting to the bus cable, short circuit current protection on CAN chip restricts the bus current to ±115mA maximum.
- Thermal protection is integrated to help prevent the device from getting damaged under such scenarios. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 165℃ (typical), thus disabling the short condition. The device is re-enabled when the junction temperature becomes 155℃ (typical). If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care must be taken in the system design to prevent repeated or prolonged exposure to bus shorts as this exposes the device to high junction temperatures for extreme amounts of time affecting device reliability.

7.6.6 Floating Pins, Unpowered Device

The ISOW1050 is designed to be passive or have no load to the CAN bus if the device is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus which is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The device has internal pull-ups on critical pins (TXD) which places the device into known states if the pin floats. This internal bias must not be relied upon by design though, especially in noisy environments, but instead must be considered a failsafe protection feature. When a CAN controller supporting open drain outputs is used, an adequate external pullup resistor must be used to verify that the TXD output of the CAN controller maintains adequate bit timing to the input of the CAN transceiver. See Table 7-3 for more details.

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7.6.7 Glitch-Free Power Up and Power Down

Communication on the bus that already exist between a controller node and target node in a CAN network must not be disturbed when a new node is swapped in or out of the network. No glitches on the bus must occur when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and recessive state
- Powered up or powered down in a recessive state when already connected to the bus

The ISOW1050 device meets above criteria and does not cause any false data toggling on the bus when powered up or powered down in a recessive state with supply ramp rates ≥50µs.

7.7 Device Functional Modes

Table 7-1 lists the supply configuration for these devices:

Table 7-1. Supply configuration Function Table

INPUTS	OUTPUTS		
V_{DD}	BUS OUTPUT (CANH/CANL)	RXD	V_{ISOOUT} (1)
< $V_{DD(UVLO+)}$	High-Z	Recessive (Default High)	OFF
5V	Bus Output follows TXD	Mirrors Bus	5V

(1) V_{ISOOUT} shorted to V_{ISOIN} on PCB.

Table 7-2 shows the different driver functional modes:

Table 7-2. Driver Functional Table

INPUTS		OUTPUTS		
V_{DD} (1)	INPUT TXD	CANH (2)	CANL (2)	DRIVEN BUS STATE
PU	L	H	L	Dominant
	H or Open	Z	Z	Recessive
	X	Hi-Z	Hi-Z	Weak pull-down to ground
PD	X	Hi-Z	Hi-Z	Weak pull-down to ground
PU	X	Invalid Operation		

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Z = common-mode (recessive) biased to $V_{ISOIN}/2$, Hi-Z=High impedance state
(2) V_{ISOOUT} shorted to V_{ISOIN} on PCB

The CAN outputs follow the logic states at data input, TXD. A logic low at the TXD input causes the CAN output to go dominant. Therefore the differential output voltage defined by Equation 2 is positive. A logic high at the TXD input causes the CAN BUS to go recessive. Therefore the differential output voltage defined by Equation 2 is negative.

$$V_{OD} = V_{CANH} - V_{CANL} \quad (2)$$

Table 7-3. Receiver Functional Table

INPUTS			OUTPUT
V_{DD} (1)	CAN DIFFERENTIAL INPUTS V_{ID} = V_{CANH}- V_{CANL}	BUS STATE	RXD (2)
PU	V_{ID} > 0.9V	Dominant	L
	0.5V< V_{ID} < 0.9V	Undefined	Undefined
	V_{ID} < 0.5V	Recessive	H
PD	X	X	Hi-Z

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state
(2) V_{ISOOUT} shorted to V_{ISOIN} on PCB.

The receiver output, RXD, goes low when the differential input voltage defined by Equation 3 is greater than the positive input threshold, V_{IT+}. The receiver output, RXD, goes high when the differential input voltage defined by Equation 3 is less than the negative input threshold, V_{IT-} . If the V_{ID} voltage is between the V_{IT+} and V_{IT-} thresholds, the output is indeterminate.

$$V_{ID} = V_{CANH} - V_{CANL} \quad (3)$$

7.8 Device I/O Schematics

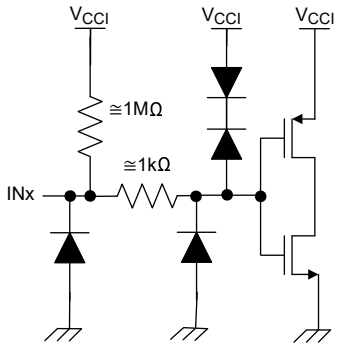

Figure 7-6. Input (TXD) Schematics

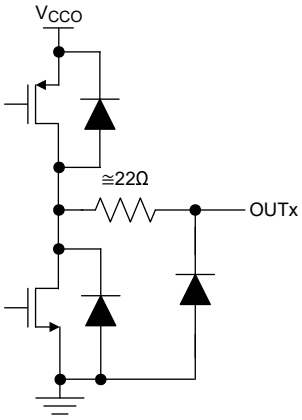

Figure 7-7. Output (RXD) Schematics

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISOW1050 device can be used with other components from Texas Instruments such as a microcontroller and a linear voltage regulator to form a fully isolated CAN interface. Typically two power supplies isolated from each other are needed to power up both sides of Isolated CAN device. Due to the integrated DC-DC converter in the device, the isolated supply is generated inside the device that can be used to power isolated side of the CAN device and peripherals on isolated side, thus saving board space.

8.2 Typical Application

The ISOW1050 device is designed for applications that have limited board space and applications that need require more integration. The device is also designed for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The device can be used in applications with a host micro-controller or FPGA that includes the link layer portion of the CAN protocol. Figure 8-1 shows a typical application configuration for 5V controller applications. The bus termination is shown for illustrative purposes.

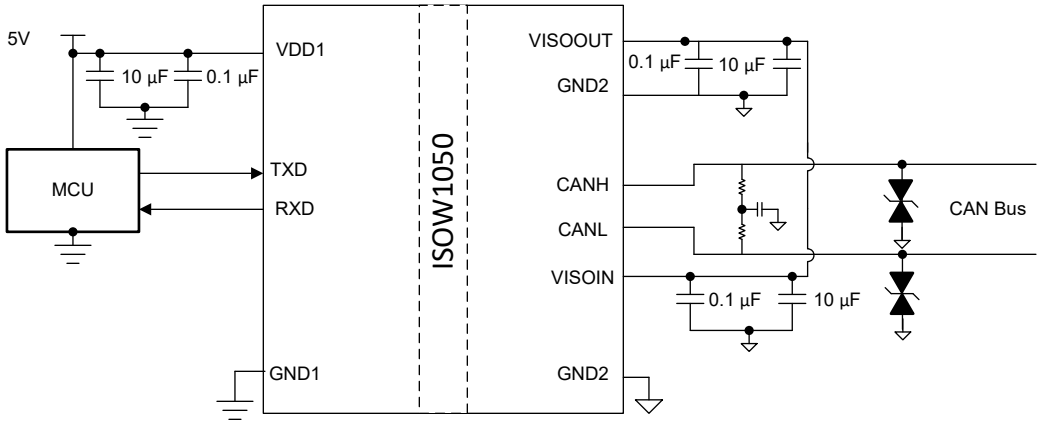

Figure 8-1. Application Circuit for ISOW1050

8.2.1 Design Requirements

Unlike an optocoupler-based design, which requires several external components to improve performance, provide bias, or limit current, the ISOW1050 device only requires external bypass capacitors to operate as shown in above application diagram.

Because of very-high current flowing through the device V_{DD} and V_{ISOOUT} supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10µF capacitor is adequate, higher decoupling capacitors (such as 47µF) on both the V_{DD} and V_{ISOOUT} pins to the respective grounds are strongly recommended to achieve the best performance.

8.2.2 Detailed Design Procedure

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8.2.2.1 Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the ISOW1050 transceiver.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 Standard. These organizations and standards have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet, and NMEA2000.

The ISOW1050 device is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the device is a minimum of 30kΩ. If 100 ISOW1050 transceivers are in parallel on a bus, this requirement is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the ISOW1050 device theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity, therefore a practical maximum number of nodes is typically much lower. Bus length can also be extended beyond the original ISO 11898 standard of 40m by careful system design and data-rate tradeoffs. For example, CAN open network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes, and a significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. Using this flexibility requires the responsibility of good network design and balancing these tradeoffs.

8.2.2.2 *CAN Termination*

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination can be in a node, but if nodes are removed from the bus, the termination must be carefully placed so that the termination is not removed from the bus.

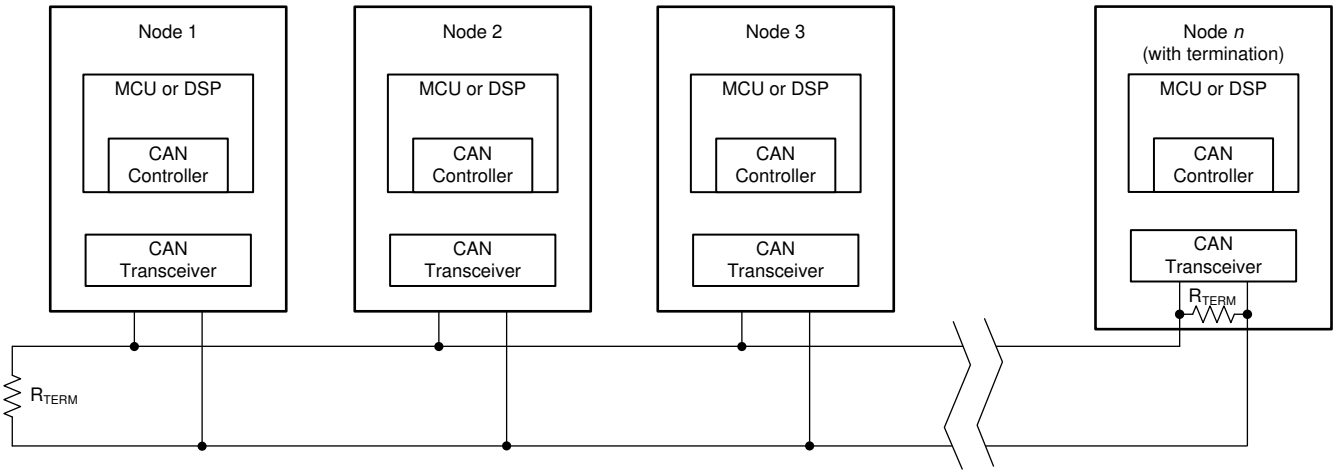

Figure 8-2. Typical CAN Bus

Termination can be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used as below termination concepts. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

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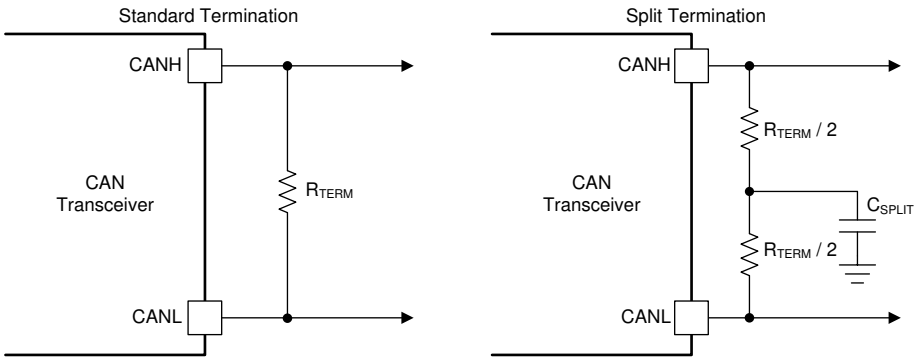

Figure 8-3. CAN Bus Termination Concepts

8.3 Power Supply Recommendations

To verify that operation is reliable at all data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. Power converter input V_{DD} and output V_{ISOOUT} supply pins must have high frequency ceramic capacitors 10nF and bulk capacitors 10µF at least close to the pins. Signal path supply pins, V_{IO} and V_{ISOIN} , must have 100nF or higher value ceramic bypass capacitors close to device pins. ISOW1050 can consume typical peak pulse currents of up to 250mA under fully loaded conditions for short durations (10s of µs) from the power source that is powering V_{DD} of ISOW1050. Verify that the current limit of upstream power device is at least 300mA, typical. For the best input ripple performance, implement multiple large decoupling capacitors in the VDD1 supply path. A total supply capacitance of 150µF with voltage rating greater than 25V is recommended. Distribute these capacitors strategically along the supply rail to achieve best ripple suppression results.

8.4 Layout

8.4.1 Layout Guidelines

Below guidelines must be followed to achieve low emissions design:

1. High frequency bypass capacitors 100nF must be placed close to V_{DD} and V_{ISOOUT} pins, within 1mm distance away from device pins. This is very essential for optimised radiated emissions performance. Verify that these capacitors are 0402 size so that the capacitors offer the least inductance (ESL).
2. Bulk capacitors of at least 10µF must be placed on power converter input (V_{DD}) and output (V_{ISOOUT}) supply pins after the 100nF capacitor with a distance of 2 - 4mm, as shown in Layout Example.
3. Traces on V_{DD} and GND1 must be symmetric till bypass capacitors. Similarly traces on V_{ISOOUT} and GND2 must be symmetric.
4. Do not have any metal traces or ground pour within 4mm of power converter output terminals V_{ISOOUT} and GND2.
5. Place the CAN BUS protection and filtering circuitry close to the bus connector to prevent transients, ESD, and noise from propagating onto the board.
6. Common mode choke or ferrite beads on bus terminals (CANH/CANL) can minimise any high frequency noise that can couple of CAN bus cable which can act as antenna and amplify that noise. This improves radiated emissions performance on a system level.
7. For optimal input ripple performance, implement multiple large decoupling capacitors in the VDD1 supply path. A total supply capacitance of 150µF with voltage rating greater than 25V is recommended. Distribute these capacitors strategically along the supply rail to achieve best ripple suppression results.
8. For Best EMC performance the GND pins must be well shorted using board ground layout.
9. Following the layout guidelines of EVM as much as possible is highly recommended for a low-radiated emissions design. EVM Link is available in Related Documentation.

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

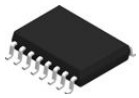
DATE	REVISION	NOTES
March 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

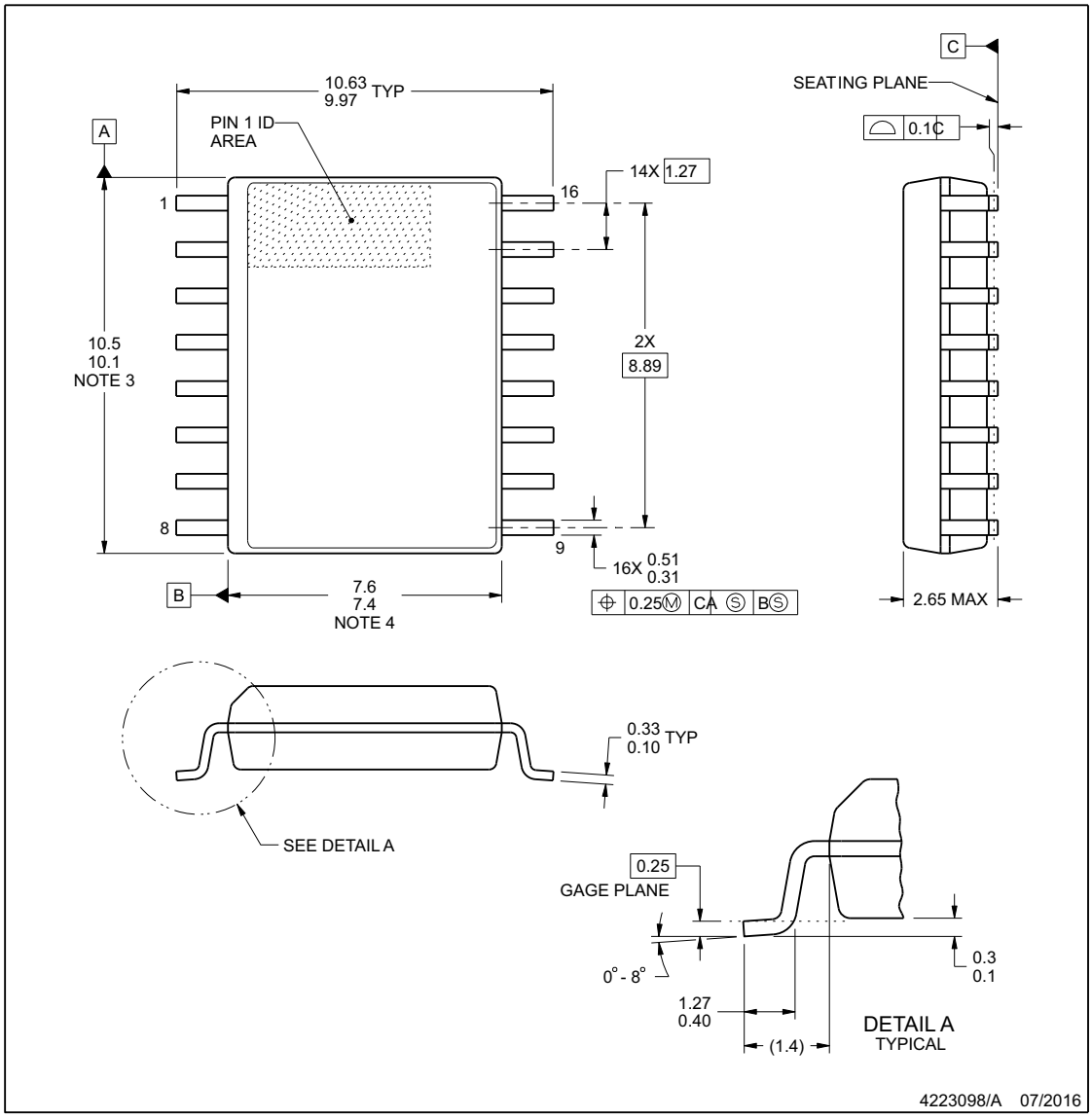


PACKAGE OUTLINE

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

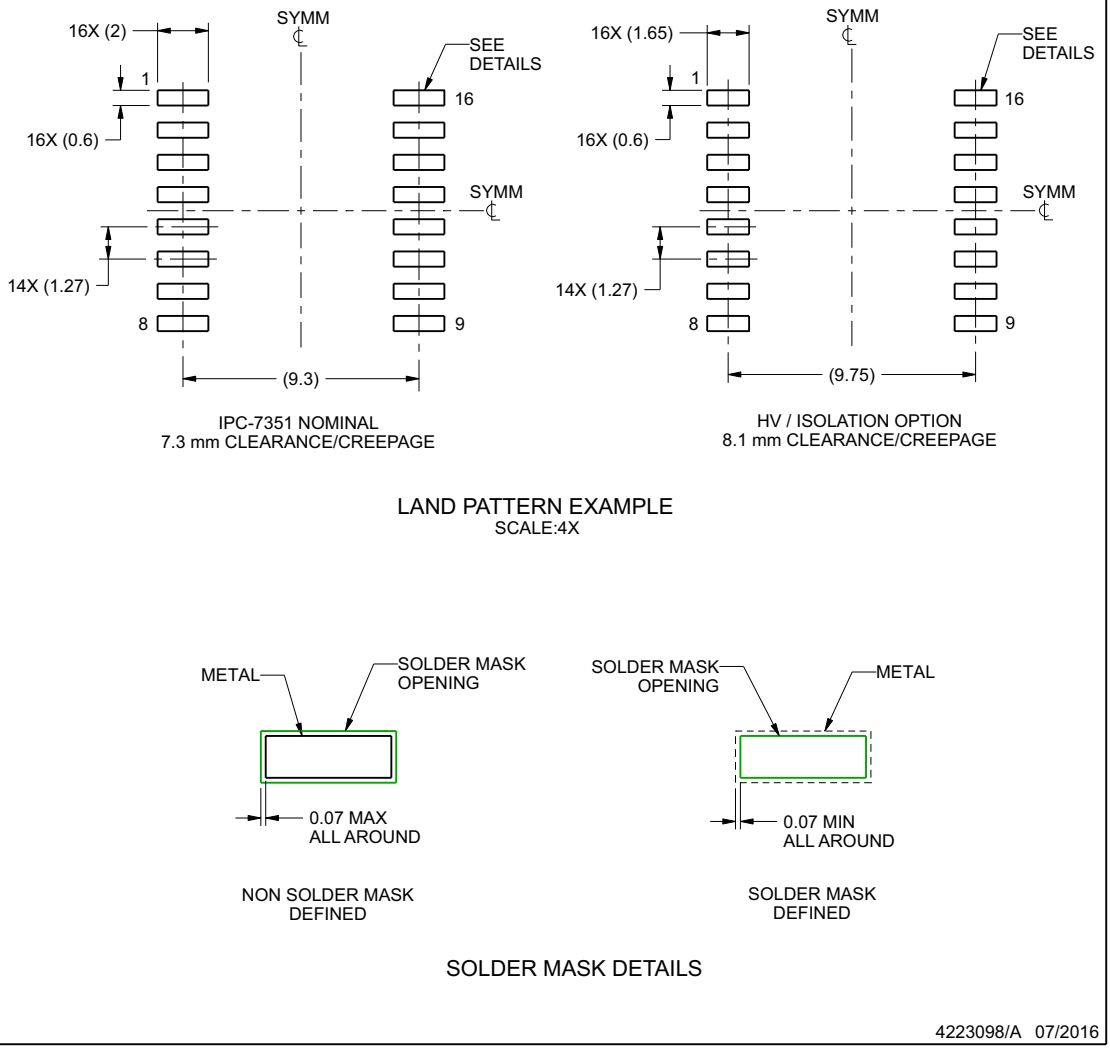
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

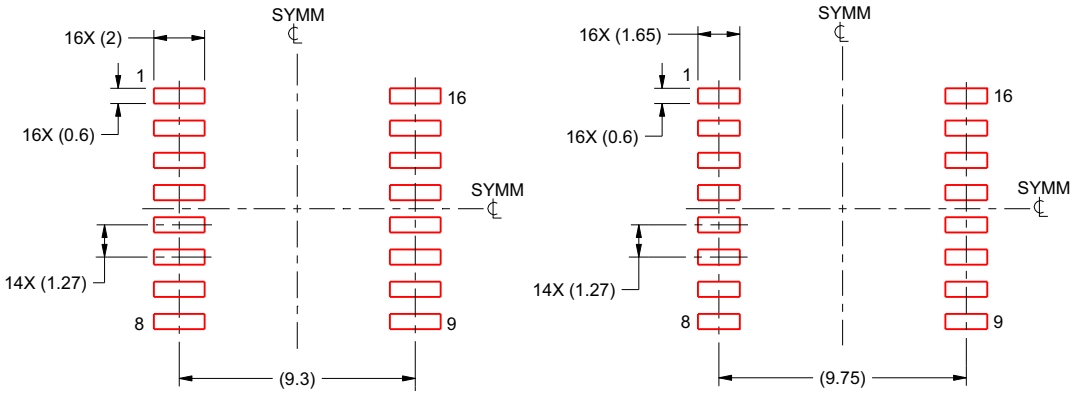
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DWE0016A — SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
XISOW1050DWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW1050
XISOW1050VDWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW1050V

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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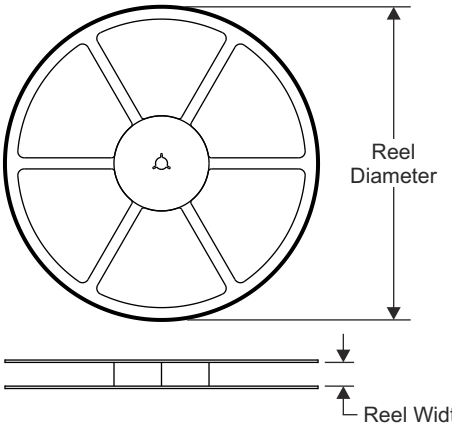
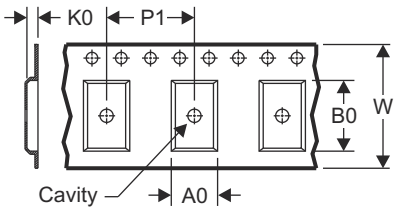
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

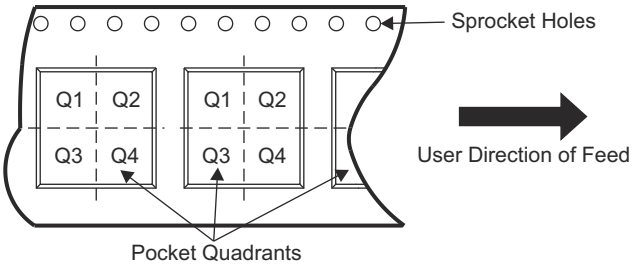


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

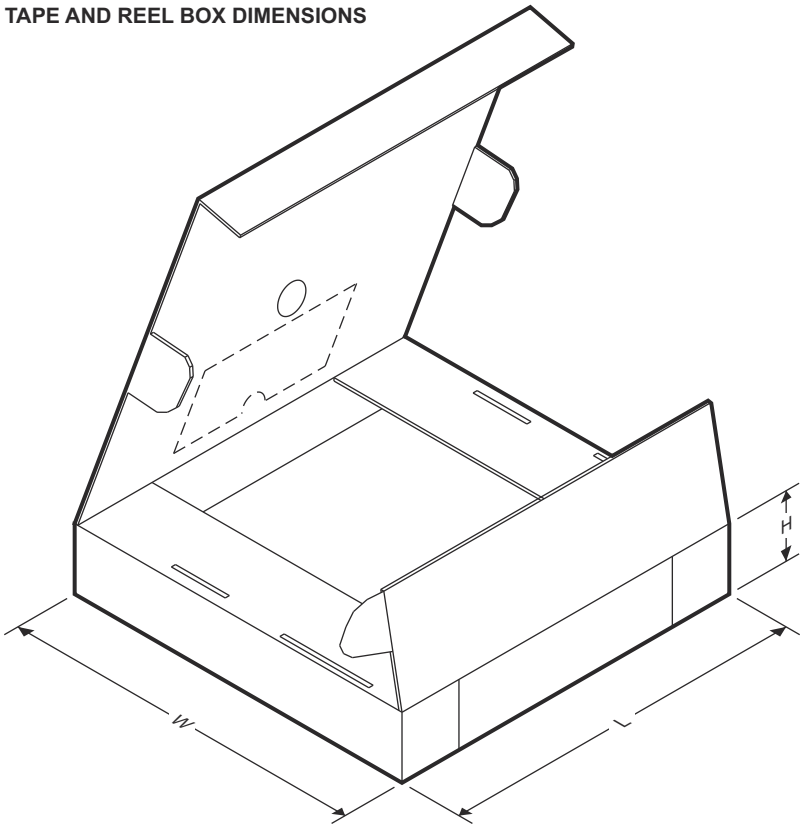
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOW1050DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISOW1050VDWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOW1050DWER	SOIC	DWE	16	2000	350.0	350.0	43.0
ISOW1050VDWER	SOIC	DWE	16	2000	350.0	350.0	43.0

ADVANCE INFORMATION

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Last updated 10/2025