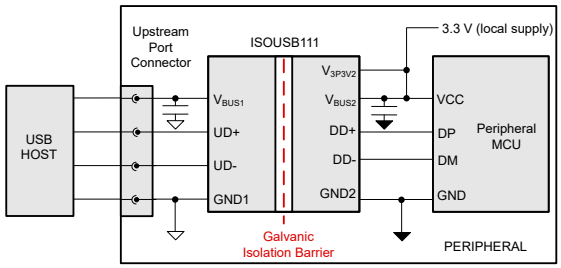
ISOUSB111 Full/Low Speed Isolated USB Repeater

1 Features

- Compliant to USB 2.0
- Supports low speed (1.5 Mbps) and full speed (12Mbps) signaling
- Automatic speed and connection detection
- Supports L1 (sleep) and L2 (suspend) low-power states
- Supports automatic role reversal for USB On-The-Go (OTG) and Type-C® Dual Role Port (DRP) designs
- High CMTI: 100kV/µs
- V_{BUS} voltage range: 4.25V to 5.5V
  - 3.3V internal LDO
- Meets CISPR32 class B emissions limits
- Ambient temperature range: –40°C to 125°C
- 16-SOIC and 16-SSOP package options
- Safety-related certifications:
  - 8000V_{PK} V_{IOTM} and 2121V_{PK} V_{IORM} (Reinforced) per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5000V_{RMS} isolation for 1 minute per UL 1577
  - IEC 62368-1, IEC 60601-1 and IEC 61010-1 certifications
  - CQC, TUV and CSA certifications
  - 16-SOIC certifications complete; 16-SSOP certifications planned

2 Applications

- USB Hub, Host, Peripheral and Cable Isolation
- Medical
- Factory automation
- Motor drives
- Grid infrastructure
- Power delivery
- USB Audio



Application Diagram

3 Description

ISOUSB111 is a galvanically-isolated USB 2.0 compliant repeater supporting low speed (1.5Mbps) and full speed (12Mbps) signaling rates. The device supports automatic connect and speed detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. The device also supports automatic role reversal - if after disconnect, a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. This feature enables the device to support USB On-The-Go (OTG) and Type-C Dual Role Port (DRP) implementations. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of up to 5000V_{RMS} and a working voltage of 1500V_{RMS}. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. The ISOUSB111 device is available for reinforced isolation. The device supports a wide ambient temperature range of –40°C to 125°C. The device is available in the standard SOIC-16 (16-DW) package and a smaller SSOP-16 (16-DWX) package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ISOUSB111	SOIC (16) DW	10.30mm × 7.50mm
	SSOP (16) DWX	5.85mm × 7.50mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	FEATURE	RATING
ISOUSB111 (1)	Protection Level	Reinforced
	Surge Isolation Voltage	12800V_{PK}
	Isolation Rating	5000V_{RMS}
	Isolation Working Voltage	1500V_{RMS} / 2121V_{PK}

(1) Reinforced Isolation Option.

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4 Pin Configuration and Functions

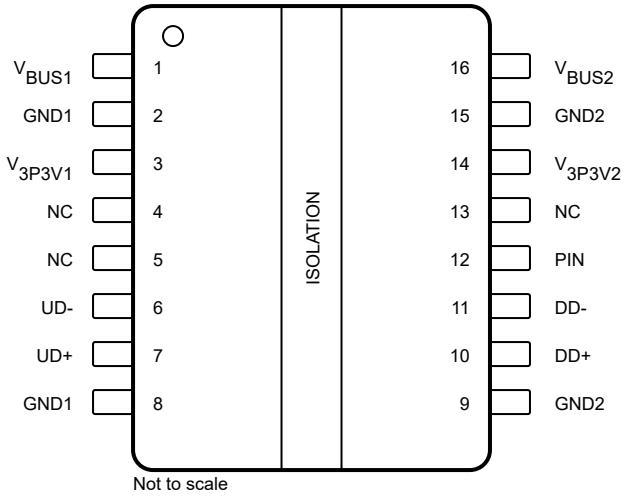

Figure 4-1. DW Package 16-Pin SOIC Top View

Table 4-1. Pin Functions—16 DW

PIN		Type [1]	DESCRIPTION
NO.	NAME		
1	V_{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect the supply to V_{BUS1}. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
2	GND1	—	Ground 1. Ground reference for Isolator Side 1.
3	V_{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V_{BUS1} connect a bypass capacitor between V_{3P3V1} and GND1. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
4	NC	—	Preferably leave floating or connect to V_{3P3V1}. Connecting to GND1 is also acceptable.
5	NC	—	Preferably leave floating or connect to V_{3P3V1}. Connecting to GND1 is also acceptable.
6	UD-	I/O	Upstream facing port D-.
7	UD+	I/O	Upstream facing port D+.
8	GND1	—	Ground 1. Ground reference for Isolator Side 1.
9	GND2	—	Ground 2. Ground reference for Isolator Side 2.
10	DD+	I/O	Downstream facing port D+.
11	DD-	I/O	Downstream facing port D-.
12	PIN	I	Upstream pull-up enable. If this pin is low, pull-up on DD+ and DD- is not recognized.
13	NC	—	Preferably leave floating or connect to V_{3P3V2}. Connecting to GND2 is also acceptable.
14	V_{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V_{BUS2} connect a bypass capacitor between V_{3P3V2} and GND1. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.
15	GND2	—	Ground 2. Ground reference for Isolator Side 2.
16	V_{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect the supply to V_{BUS2}. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.

(1) I = Input, O = Output

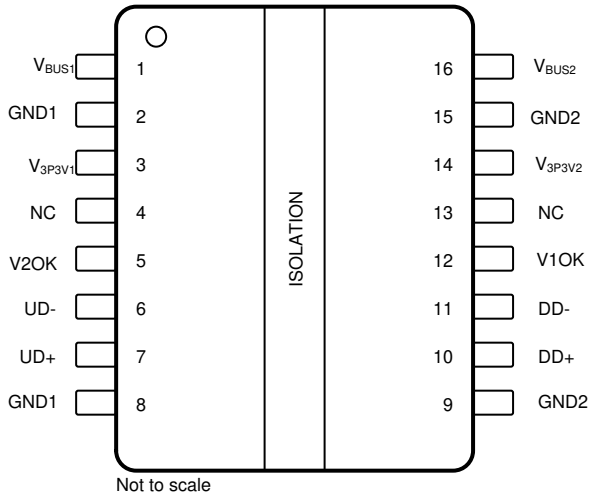

Figure 4-2. DWX Package 16-Pin SSOP Top View

Table 4-2. Pin Functions—16 DWX

PIN		Type [1]	DESCRIPTION
NO.	NAME		
1	V_{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect the supply to V_{BUS1}. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
2	GND1	—	Ground 1. Ground reference for Isolator Side 1.
3	V_{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V_{BUS1} connect a bypass capacitor between V_{3P3V1} and GND1. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
4	NC	—	Leave floating or connect to V_{3P3V1}.
5	V2OK	O	High level on this pin indicates that side 2 is powered up.
6	UD-	I/O	Upstream facing port D-.
7	UD+	I/O	Upstream facing port D+.
8	GND1	—	Ground 1. Ground reference for Isolator Side 1.
9	GND2	—	Ground 2. Ground reference for Isolator Side 2.
10	DD+	I/O	Downstream facing port D+.
11	DD-	I/O	Downstream facing port D-.
12	V1OK	—	High level on this pin indicates that side 1 is powered up.
13	NC	—	Leave floating or connect to V_{3P3V2}.
14	V_{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V_{BUS2} connect a bypass capacitor between V_{3P3V2} and GND1. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.
15	GND2	—	Ground 2. Ground reference for Isolator Side 2.
16	V_{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect the supply to V_{BUS2}. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.

(1) I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{BUS1}, V_{BUS2}	V_{BUS} supply voltage	-0.3	6	V
V_{3P3V1}, V_{3P3V2}	3.3-V input supply voltage	–0.3	4.25	V
V_{DPDM}	Voltage on bus pins (UD+, UD-, DD+, DD-) 1000 total number of short events and cumulative duration of 1000 hrs.	–0.3	6	V
V_{IO}	IO voltage range (PIN, V*OK)	–0.3	V_{3P3Vx}+0.3(3)	V
I_O	Output current on output pins (V*OK)	-10	10	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 4.25 V

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, DW package, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, DWX package, all pins(1)	±1500	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BUSx}	V_{BUS} input voltage (inclusive of any ripple)	4.25	5	5.5	V
V_{3P3Vx}	3.3-V input supply voltage (inclusive of any ripple)	3.0	3.3	3.6	V
T_A	Operating free-air temperature	-40		125	°C
T_J	Junction temperature	–55		150	°C

5.4 Thermal Information

THERMAL METRIC1[(1)]		ISOUSB111		UNIT
		DW (SOIC)	DWX (SSOP)	
		16 PINS	16 PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	53.4	60.6	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	19.6	22.5	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	22.3	27	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.6	26.1	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOUSB111						
P_D	Maximum power dissipation (both sides)	V_{BUS1} = V_{BUS2} = 5.5 V, T_J = 150°C, C_L = 50 pF each on DD- and DD+, Input a 6-MHz 50% duty cycle differential 3.3-V square wave on UD- and UD+			157	mW
P_{D1}	Maximum power dissipation (side-1)				72	mW
P_{D2}	Maximum power dissipation (side-2)				85	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS		UNIT
			DW-16	DWX-16	
IEC 60664-1					
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8	>8	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	>8	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	1500	1500	V_{RMS}
		DC voltage	2121	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	8000	8000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8000	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	12800	V_{PK}
q_{pd}	Apparent charge(5)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	≤ 5	
		Method b: At routine test (100% production) and preconditioning (type test); Vini = 1.2 × VIOTM, tini = 1 s; Vpd(m) = 1.875 × VIORM, tm = 1 s (method b1) or Vpd(m) = Vini, tm = tini (method b2)	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 pft), f = 1 MHz	0.8	0.7	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	> 10^{12}	W
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	> 10^9	
	Pollution degree		2	2	
	Climatic category		40/125/21	40/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	5000	V_{RMS}

(1) Care must be taken during board design so that the mounting pads of the isolator on the printed-circuit board (PCB) do not reduce creepage and clearance. Inserting grooves, ribs or both can help increase creepage distance on the PCB.
(2) ISOUSB111 is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Reinforced Insulation; Maximum transient isolation voltage, ISOUSB111: 7071 V_{PK} Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, ISOUSB111: 12800 V_{PK} (Reinforced)	Reinforced insulation per CSA 62368-1 and IEC 62368-1 ISOUSB111: 800 V_{RMS} Maximum working voltage (pollution degree 2, material group I); ISOUSB111: 2 MOPP ---------- (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V_{RMS} maximum working voltage	Single protection, ISOUSB111: 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced insulation per EN 61010-1 up to working voltage of 600 V_{RMS} ---------- 5000 V_{RMS} Reinforced insulation per EN 62368-1 up to working voltage of 800 V_{RMS}
Certificate number: 40040142	Master contract: 220991	File number: E181974	Certificate: CQC15001121716	Client ID: 77311

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 53.4°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 5-1			425	mA
		$R_{\theta JA}$ = 53.4°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 5-1			650	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 53.4°C/W, T_J = 150°C, T_A = 25°C, see Figure 5-3			2340	mW
T_S	Maximum safety temperature				150	°C
DWX-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 60.6°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 5-2			374	mA
		$R_{\theta JA}$ = 60.6°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 5-2			572	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 60.6°C/W, T_J = 150°C, T_A = 25°C, see Figure 5-4			2062	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

5.9 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		12	15.3	mA
		Transmit side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		9.5	13	mA
		Receive side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		11	13.5	mA
		Transmit side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		9.5	13	mA
		FS/LS Idle State (US side or DS side)		7.4	11	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L1 Sleep mode	Upstream Facing side		7.5	9.8	mA
		Downstream Facing side		7.3	9.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L2 Suspend mode	Upstream Facing side		1.07	1.55	mA
		Downstream Facing side		5.6	7.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Not attached	Upstream Facing side		6.2	8.5	mA
		Downstream Facing side		6.2	8.9	mA
$UV+_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is rising, V_{BUS}				4.0	V
$UV-_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is falling, V_{BUS}		3.6			V
$UVHYS_{(VBUSx)}$ (1)	Under voltage threshold hysteresis, V_{BUS}			0.08		V
$UV+_{(V3P3Vx)}$	Under voltage threshold when supply voltage is rising, V_{3P3V}				2.95	V
$UV-_{(V3P3Vx)}$	Under voltage threshold when supply voltage is falling, V_{3P3V}		1.95			V
$UVHYS_{(V3P3Vx)}$	Under voltage threshold hysteresis, V_{3P3V}			0.11		V
DIGITAL INPUTS						
V_{IH}	High-level input voltage		0.7 x V_{3PV3x}			V
V_{IL}	Low-level input voltage				0.3 x V_{3PV3x}	V
V_{IHYS}	Input transition threshold hysteresis		0.3			V
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				10	µA
DIGITAL OUTPUTS (V1OK, V2OK)						
V_{OH}	High-level output voltage	I_O = -3 mA for 3.0 V ≤ V_{3P3Vx} ≤ 3.6 V	V_{3P3Vx} - 0.2			V
V_{OL}	Low-level output voltage	I_O = 3 mA for 3.0 V ≤ V_{3P3Vx} ≤ 3.6 V			0.2	V
UDx, DDx, INPUT CAPACITANCE AND TERMINATION						
Z_{INP_xDx}	Impedance to GND, no pull up/down	Vin=3.6 V, V_{3P3Vx}=3.0 V, T_J < 125 °C, USB 2.0 Spec Section 7.1.6	300			kΩ
C_{IO_xDx}	Capacitance to GND	Measured with VNA at 240MHz, Driver Hi-Z			10	pF
R_{PUI}	Bus Pull up Resistor on Upstream Facing Port (idle)	USB 2.0 Spec Section 7.1.5	0.9	1.1	1.575	kΩ

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PUR}	Bus Pull up Resistor on Upstream Facing Port (receiving)	USB 2.0 Spec Section 7.1.5	1.5	2.2	3	kΩ
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Spec Section 7.1.5	14.25	19	24.8	kΩ
V_{TERM}	Termination voltage for Upstream facing port pullup (RPU)	USB 2.0 Spec Section 7.1.5, measured on D+ or D- with pull up enabled on upstream port with external load disconnected.	3		3.6	V
UDx, DDx, INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Spec Section 7.1.4 (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Spec Section 7.1.4 (Host downstream port pull down resistor enabled and Device pulled up to 3.0 V - 3.6 V).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Spec Section 7.1.4			0.8	V
V_{DI}	Differential Input Sensitivity	|(xD+)-(xD-)|; USB 2.0 Spec Figure 7-19; (measured at connector)	0.2			V
V_{CM}	Common Mode Range	Includes VDI range; USB 2.0 Spec Figure 7-19; (measured at connector)	0.8		2.5	V
UDx, DDx, OUTPUT LEVELS LS/FS						
V_{OL}	Low	USB 2.0 Spec Section 7.1.1, (measured at connector with RL of 0.9 kΩ to 3.6 V.)	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Spec Section 7.1.1 (measured at connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
V_{OSE1}	SE1	USB 2.0 Spec Section 7.1.1	0.8			V
Z_{FSTERM}	Driver Series Output Resistance	USB 2.0 Spec Section 7.1.1 and Figure 7-4, Measured during VOL or VOH	28		44	Ω
V_{CRS}	Output Signal Crossover Voltage	Measured as in USB 2.0 Spec Section 7.1.1 Figures 7-8, 7-9 and 7-10; Excluding the first transition from the Idle state	1.3		2	V
THERMAL SHUTDOWN						
TSD+	Thermal shutdown turn-on temperature		160	170	180	°C
TSD-	Thermal shutdown turn-off temperature		150	160	170	°C
TSD_{HYS}	Thermal shutdown hysteresis			10		°C

(1) If V_{BUSx} pins are externally connected to the corresponding V_{3P3Vx} pins, then UVLO thresholds on V_{BUSx} are governed by $UV+_{(V3P3Vx)}$, $UV-_{(V3P3Vx)}$ and $UVHYS_{(V3P3Vx)}$

5.10 Switching Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-UP TIMING						
$T_{SUPRAMP}$	Allowed power supply ramp-up times on V_{BUSx} and V_{3P3Vx} external power supplies		0.005		100	ms
T_{PWRUP}	Time taken for the device to power up, and recognize USB signaling, after valid power supply is provided on both side 1 and side 2.	All external power supplies are ramped up together with 5 µs power up time.		3.6	8	ms
UDx, DDx, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, C_L = 50 pF	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, C_L = 50 pF	4		20	ns
T_{FRFM}	Differential Rise and Fall Time Matching (T_{FR}/T_{FM})	USB 2.0 Spec 7.1.2, Excluding the first transition from the Idle state, Figure 7-9, C_L = 50 pF	90		111.1	%
UDx, DDx, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LRFM}	Rise and Fall Time Matching (TLR/TFM), Excluding first transition from idle state.	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	80		125	%
REPEATER TIMING - CONNECT, DISCONNECT, RESET, L1, L2						
$T_{FILTCONN}$	Debounce filter on FS or LS Connect Detection		45	70	80	µs
T_{DDIS}	Time to detect disconnect at the DS facing port in LS/FS L0 mode.		2		7	µs
T_{DETRST}	Time taken to detect reset on US port in LS/FS L0 mode		0		7	µs
T_{2SUSP}	Time taken by the US side to detect suspend mode (L2) and draw less than 2.5 mA current when bus is continuously in idle state.		3		10	ms
$t_{DRESUMEL1}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from sleep/L1 state.				1	µs
$t_{DRESUMEL2}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from suspend/L2 state.				130	µs
$t_{DWAKEL1}$	Maximum time to detect and propagate remote wake when in sleep/L1 state.				5	µs
$t_{DWAKEL2}$	Maximum pulse width of remote wake that is guaranteed to be detected when in suspend/L2 state.				900	µs
$t_{DRSMPROP}$	Minimum duration of resume driven upstream and downstream after detecting remote wake when in suspend/L2 state.		1			ms
CMTI	Common mode transient immunity	PK-PK common mode noise, V_{CMPKPK} = 1200 V during USB data transmission, see Figure 6-2	75	100		kV/µs

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REPEATER TIMING - LS, FS						
T_{LSDD}	Low-speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			358	ns
T_{LSOP}	LS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-40		25	ns
T_{LSJP}	LS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–5		5	ns
T_{LSJN}	LS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–7.0		7.0	ns
T_{LST}	Minimum width of SE0 interval during LS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	210			ns
T_{LEOPD}	Repeater EOP delay relative to T_{LSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		200	ns
T_{LESK}	SE0 skew caused by the repeater during LS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-100		100	ns
T_{FSDD}	Full-Speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			70	ns
T_{FSOP}	FS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-10		10	ns
T_{FSJP}	FS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–2		2	ns
T_{FSJN}	FS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–6.0		6.0	ns
T_{FST}	Minimum width of SE0 interval during FS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	14			ns
T_{FEOPD}	Repeater EOP delay relative to T_{FSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		17	ns
T_{FESK}	SE0 skew caused by the repeater during FS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-15		15	ns

5.11 Insulation Characteristics Curves

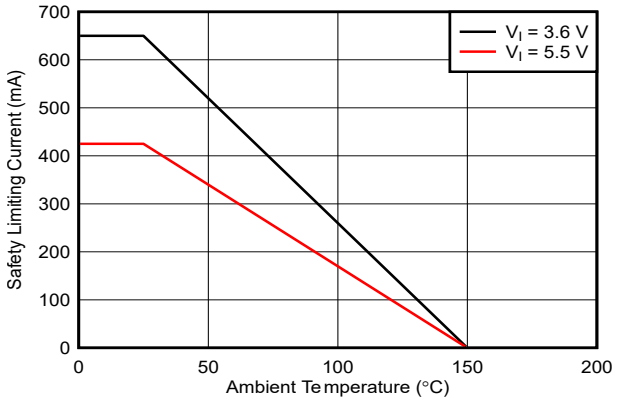

Figure 5-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

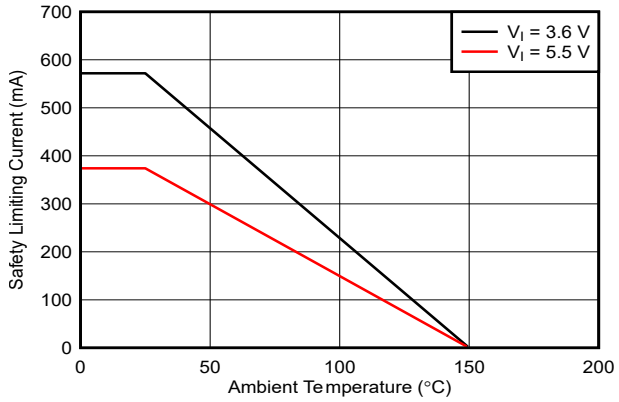

Figure 5-2. Thermal Derating Curve for Limiting Current per VDE for DWX-16 Package

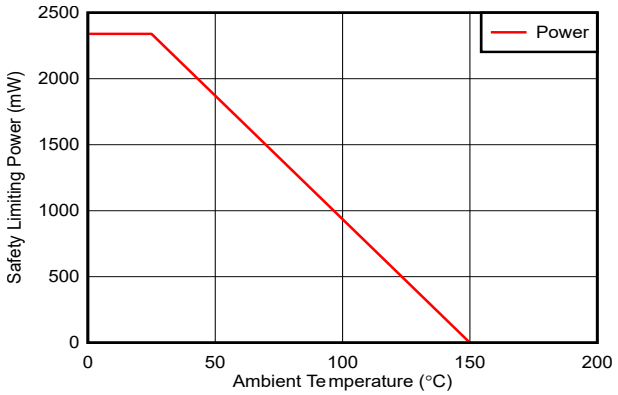

Figure 5-3. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

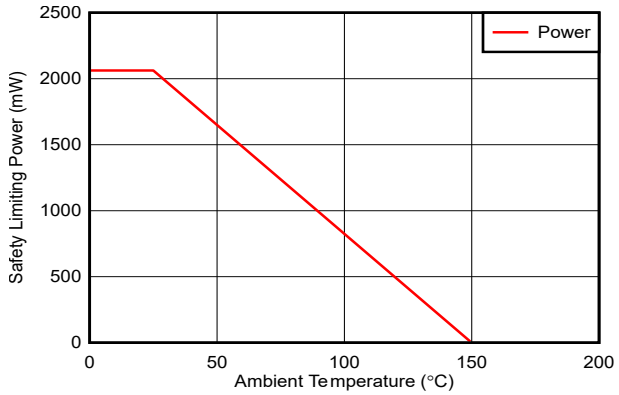

Figure 5-4. Thermal Derating Curve for Limiting Power per VDE for DWX-16 Package

5.12 Typical Characteristics

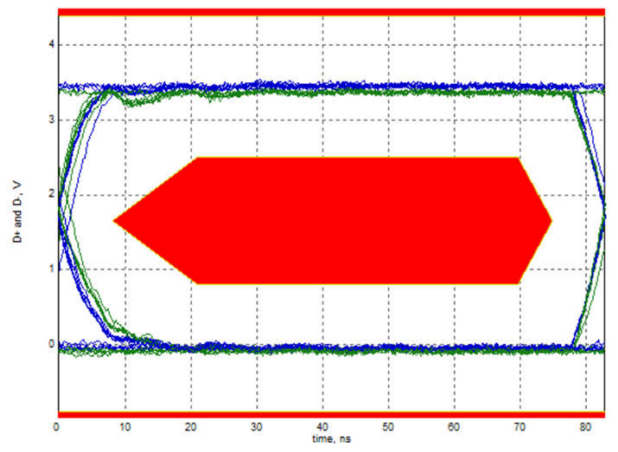

Figure 5-5. Typical Full-Speed (12 Mbps) Eye-Diagram through ISOUSB111

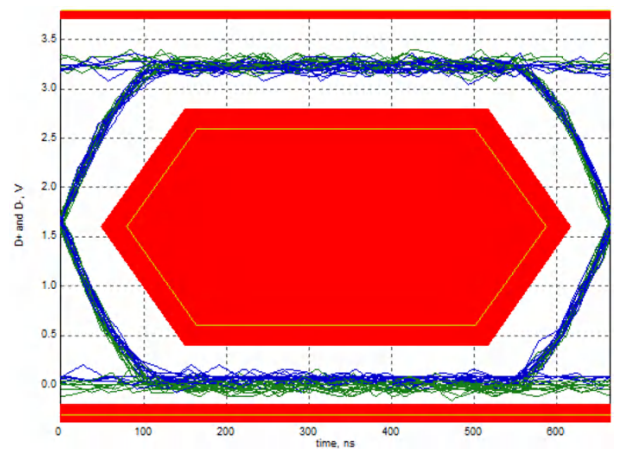

Figure 5-6. Typical Low-Speed (1.5 Mbps) Eye-Diagram through ISOUSB111

6 Parameter Measurement Information

6.1 Test Circuits

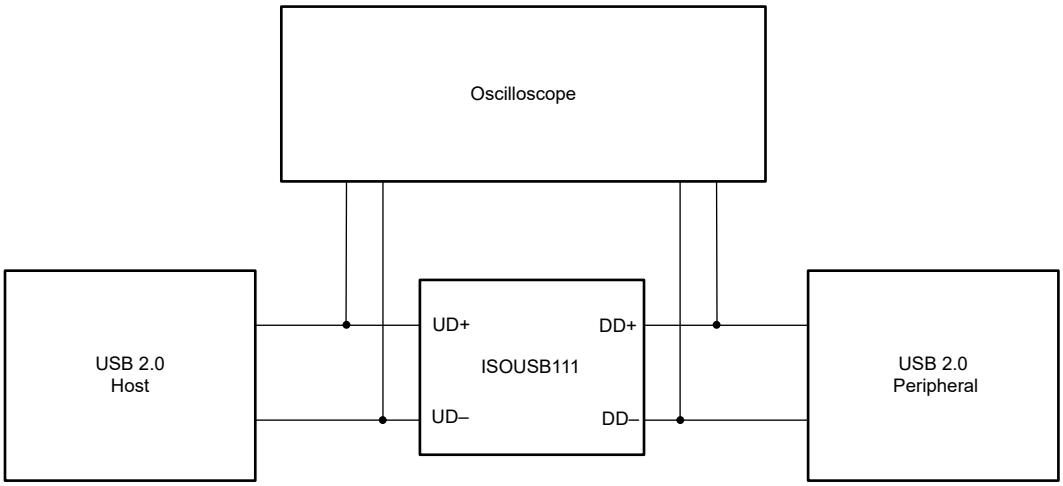

Figure 6-1. Upstream and Downstream Packet Parameter and Eye-Diagram Measurements

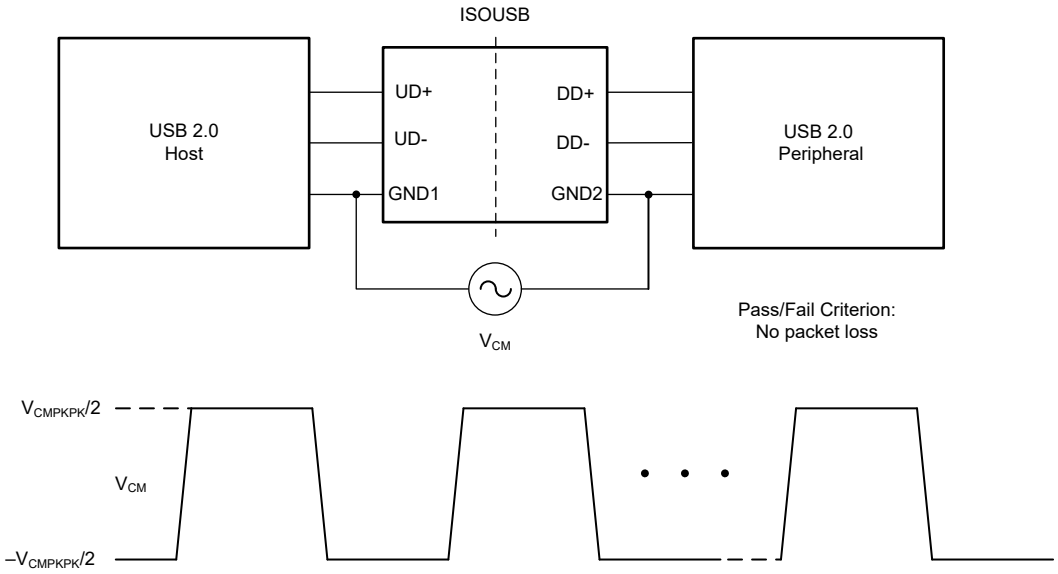

Figure 6-2. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

ISOUSB111 is a galvanically-isolated USB2.0 compliant repeater supporting Low Speed (1.5 Mbps) and Full Speed (12 Mbps) signaling rates. The device supports automatic speed and connection detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. Most microcontrollers integrate the USB PHY, and so offer only D+ and D- bus lines as external pins. ISOUSB111 can isolate these pins from the USB bus without needing any other intervention from the microcontroller. The device also supports automatic role reversal - if after disconnect, if a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. The ISOUSB211 has inbuilt programmable equalization to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. High Speed (HS) Test Mode entry is also automatically detected, as required by the USB2.0 standard, to enable HS compliance tests.

ISOUSB111 is available in reinforced isolation option with isolation withstand voltage of 5000 V_{RMS} respectively, and with surge test voltage of 12.8 kV_{PK} respectively. The device can operate completely off a 4.25 V to 5.5 V supply (USB VBUS power) or from local 3.3-V supply, if available, on both side 1 and side 2. This flexibility in supply voltages allows optimization for thermal performance based on power rails available in the system.

7.2 Functional Block Diagram

A simplified functional block diagram of ISOUSB111 is shown in Figure 7-1. The device comprises the following:

1. Transmit and receive circuits and pull-up and pull-down resistors according to the USB standard.
2. Digital logic to handle bi-directional communication, and various state-transitions.
3. Internal LDOs to generate V_{3P3Vx} supplies from the V_{BUSx} supplies.
4. Galvanic isolation.

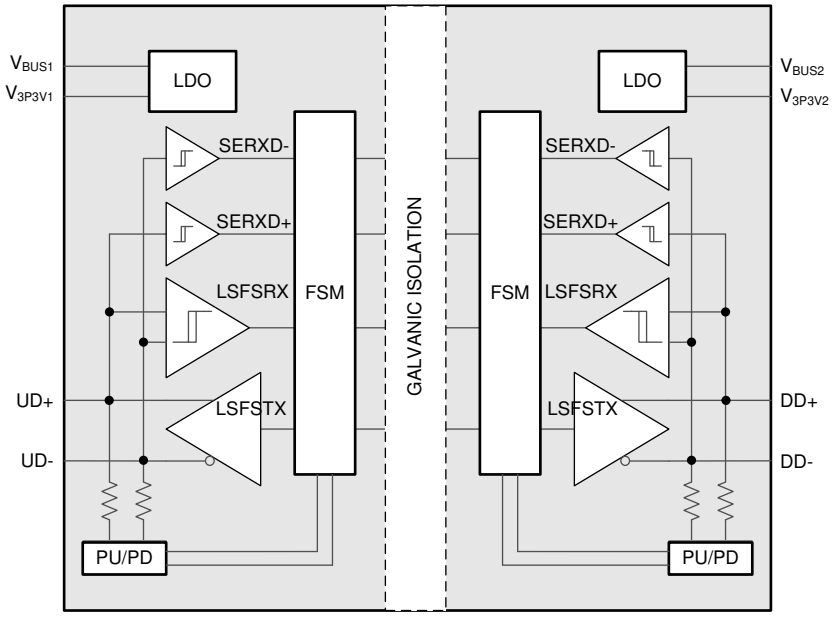

Figure 7-1. ISOUSB111 Simplified Functional Block Diagram

7.3 Feature Description

7.3.1 Power Supply Options

The ISOUSB111 can be powered by connecting a 4.25 V to 5.5 V supply on V_{BUSx} pins, in which case an internal LDO generates V_{3P3Vx} voltage. This option is suitable for the side facing the USB connector, where a 5-V VBUS supply is available. Alternatively, V_{BUSx} and V_{3P3Vx} pins can be shorted together and an external 3.3-

V power supply can be connected to both. This second option is suitable for the side facing the microcontroller, where a 5-V supply is not always available.

7.3.2 Power Up

Until all power supplies on both sides of ISOUSB111 are above the respective UVLO thresholds, the device ignores any activity on the bus lines on both upstream and downstream side. Once the power supplies are above the UVLO thresholds, the device is ready to respond to activity on the bus lines.

7.3.3 Symmetric Operation, Dual-Role Port, and Role-Reversal

ISOUSB111 supports symmetric operation. Normally, UD+ and UD- are upstream facing ports and connect to a host or hub. DD+ and DD- are downstream facing ports and connect to a peripheral. However, connecting UD+ and UD- to a peripheral and DD+ and DD- to a host or hub is also possible. Whichever side sees a connect first (D+ or D- pulled up to 3.3 V) becomes the downstream facing side. This feature enables implementation of dual-role port (for example Type-C dual-role port) and role-reversal (for example OTG Host Negotiation Protocol - HNP). Refer to *How to Implement an Isolated USB 2.0 High-Speed, Type-C® DRP* application note for details. In the rest of this document, DD+/DD- are treated as downstream facing ports, and UD+/UD- as upstream facing ports, but the various operations and features described are equally applicable if this assignment is swapped.

7.3.4 Connect and Speed Detection

When there is no peripheral device connected to the downstream side of ISOUSB111, internal 15 kΩ pulldown resistors on DD+ and DD- pins pull the bus lines to zero, creating an SE0 state. When either the DD+ or DD- lines is pulled up higher than the V_{IH} threshold, for a time period higher than $T_{FILTCONN}$, the ISOUSB111 device treats this as a connect. The ISOUSB111 device configures internal pull-up on the upstream side to match the pull-up detected on the downstream side. After connect is detected, the ISOUSB111 device waits for a reset to be asserted by the host/hub on the upstream side. Depending on whether DD+ or DD- is pulled up at the start of reset, the speed of the ISOUSB111 repeater is set. Once set, the speed of the repeater can only be changed after a power down or disconnect event.

7.3.5 Disconnect Detection

When in Full-speed (FS) and Low-speed (LS) modes, disconnection of a peripheral is indicated when the host/hub is not driving any signal on the upstream side, and when the downstream bus is in the SE0 state (Both DD+ and DD- are below the V_{IL}threshold) for a time period higher than T_{DDIS}. Upon disconnect detection in FS and LS modes, the ISOUSB111 device removes the pull-up resistor from the upstream side, thus allowing the upstream UD+ and UD- lines to discharge to zero. The ISOUSB111 then waits for the next connect event to occur.

7.3.6 Reset

The ISOUSB111 device detects Reset assertion (prolonged SE0 state) on the upstream facing side, and transmits the same to the downstream facing side.

7.3.7 LS/FS Message Traffic

The ISOUSB111 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the LS/FS idle state first (J to K transition). After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues until either an End-of-Packet (EOP) or a long idle is seen. At this point, the ISOUSB111 device tri-states the LS/FS transmitters, and waits for the next transition from the LS/FS idle state.

7.3.8 L2 Power Management State (Suspend) and Resume

The ISOUSB111 device supports Suspend low power state, also called L2 state in the USB 2.0 Link Power Management engineering change notice (ECN). Suspend mode is detected if the bus stays in the LS/FS idle state for more than 3 ms. When Suspend is detected from LS and FS idle state, the ISOUSB111 continues in the LS or FS idle state, at the same time reducing internal power consumption. The transition to the L2 low-power mode is completed within 10 ms.

Exit from L2 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB111, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB111 followed by Resume signaling from the host/hub on the upstream facing side. Start of Resume or Wake are signaled by a ‘K’ state by the host or the device respectively. The end of resume is signaled by the host by driving two low-speed bit times of SE0 followed by a 'J' state. ISOUSB111 is able to replicate the resume and wake signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS or FS idle state depending on the state prior to entering the L2 state.

7.3.9 L1 Power Management State (Sleep) and Resume

The ISOUSB111 device supports the additional L1 or Sleep low power state defined in the USB 2.0 Link Power Management ECN. When L1 entry is detected from the LS and FS idle state, the ISOUSB111 continues in the LS or FS idle state, at the same time reducing internal power consumption. The transition to the L1 low-power mode is completed within 50 µs.

Exit from L1 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB111, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB111 followed by Resume signaling from the host/hub on the upstream facing side. Start of Resume or Wake are signaled by a ‘K’ state by the host or the device respectively. The end of resume is signaled by the host by driving two low-speed bit times of SE0 followed by a 'J' state. ISOUSB111 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS or FS idle state depending on the state prior to entering the L1 state.

7.4 Device Functional Modes

Table 7-1 lists the functional modes for the ISOUSB111 device.

Table 7-1. Function Table

SIDE 1 SUPPLY V_{BUS1}, V_{3P3V1} (1)	BUS1 (UD+, UD-)	SIDE 2 SUPPLY V_{PIN}	SIDE 2 SUPPLY V_{BUS2}, V_{3P3V2}	BUS2 (DD+, DD-)	COMMENTS
Powered	Active	H	Powered	Active	When both sides are powered, the state-of the bus is reflected correctly from upstream to downstream and reciprocally.
Powered	15-kΩ PD	L	Powered	15-kΩ PD	Disconnected state is presented on both upstream and downstream
Powered	15-kΩ PD	X	Unpowered	Z	If a side is not powered, the bus lines on that side are in high-impedance state.
Unpowered	Z	X	Powered	15-kΩ PD	
Unpowered	Z	X	Unpowered	Undetermined	

(1) Powered = ($V_{BUSx} \geq UV+_{(VBUSx)}$) || ($V_{BUSx} = V_{3P3Vx} \geq UV+_{(V3P3Vx)}$) ; Unpowered = ($V_{BUSx} < UV-_{(VBUSx)}$) & ($V_{3P3Vx} < UV-_{(V3P3Vx)}$) ; X = Irrelevant; H = High level; L = Low level; Z = High impedance

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

8.1.1 Isolated Host or Hub

Figure 8-1 shows an application for isolating a host or a hub using ISOUSB111. In this example, on the microcontrollers side, V_{3P3V1} and V_{BUS1} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS2} and the V_{3P3V2} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the Power Supply Recommendations section. An isolated DC-DC converter (such as the SN6505) is to provide power to the VBUS using the 3.3-V local supply. Note that, for a host or hub, the USB standard requires a 120-µF capacitor to be placed on the VBUS so as to be able provide in-rush current when a downstream peripheral is attached. In addition, a 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, can be placed on D+ and D- lines. A ferrite bead, with DC resistance less than 100 mΩ, can be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

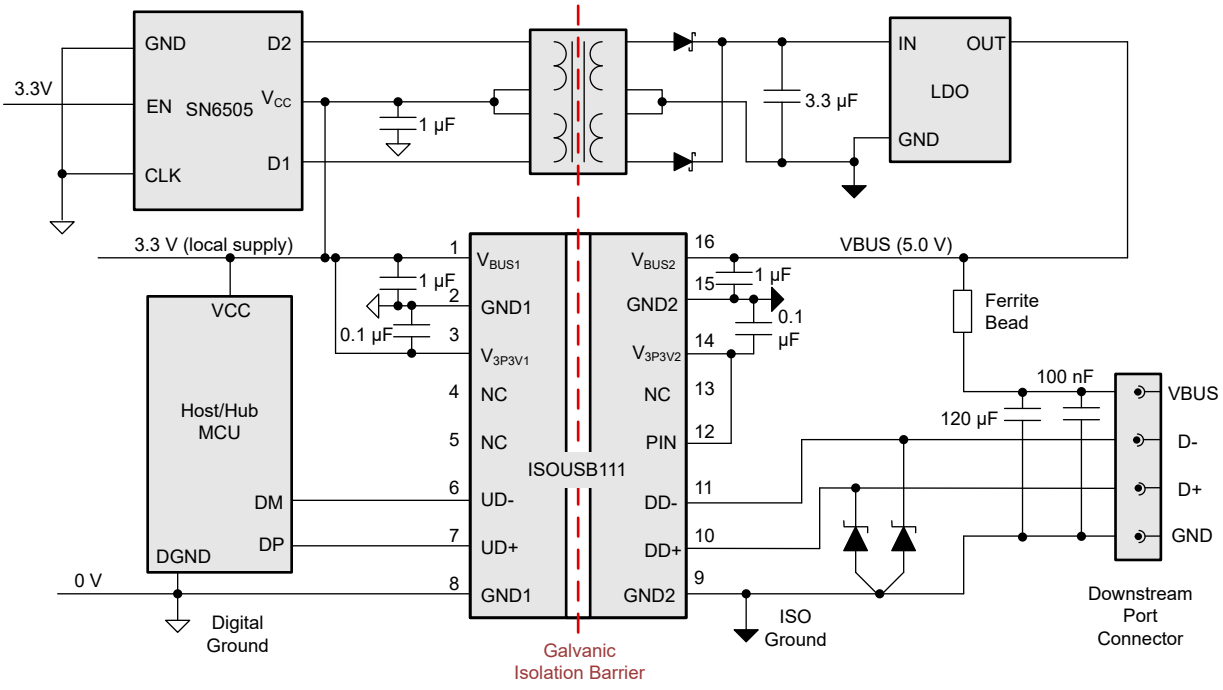

Figure 8-1. Isolated Host or Hub With ISOUSB111

8.1.2 Isolated Peripheral - Self-Powered

Figure 8-2 shows an application for isolating a self-powered peripheral using ISOUSB111. In this example, on the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS must be less than 10-µF. A 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, can be placed on D+ and D- lines. A ferrite bead, with DC resistance less than 100 mΩ, can be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

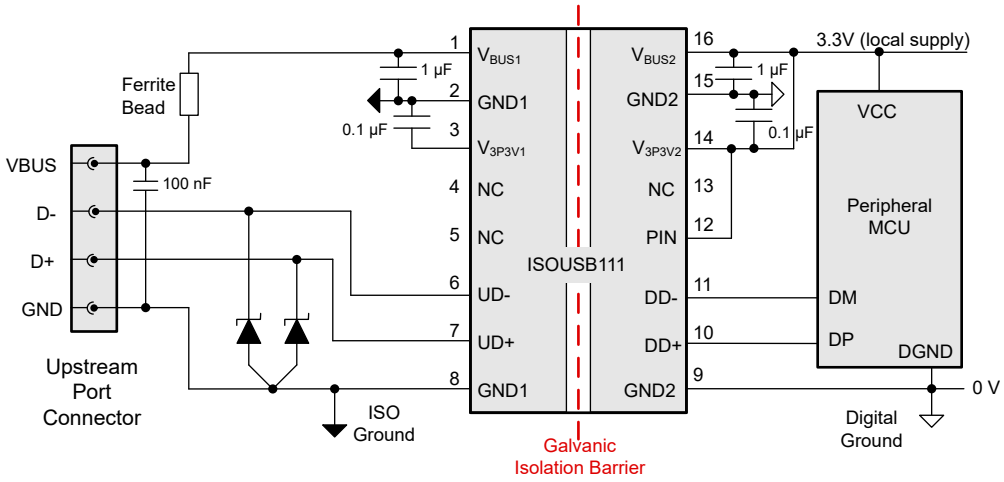

Figure 8-2. Isolated Self-Powered Peripheral With ISOUSB111

8.1.3 Isolated Peripheral - Bus-Powered

Figure 8-3 shows an application for isolating a self-powered peripheral using ISOUSB111. In this example, an isolated DC-DC converter (for example: SN6505) is used to create a 3.3-V local supply while deriving power from the USB VBUS. On the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS, including any decoupling capacitors reflected from the secondary side through the isolated DC-DC converter, must be less than 10-µF. A 100-nF capacitor is recommended close to the VBUS connector to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, can be placed on D+ and D- lines. A ferrite bead, with DC resistance less than 100 mΩ, can be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

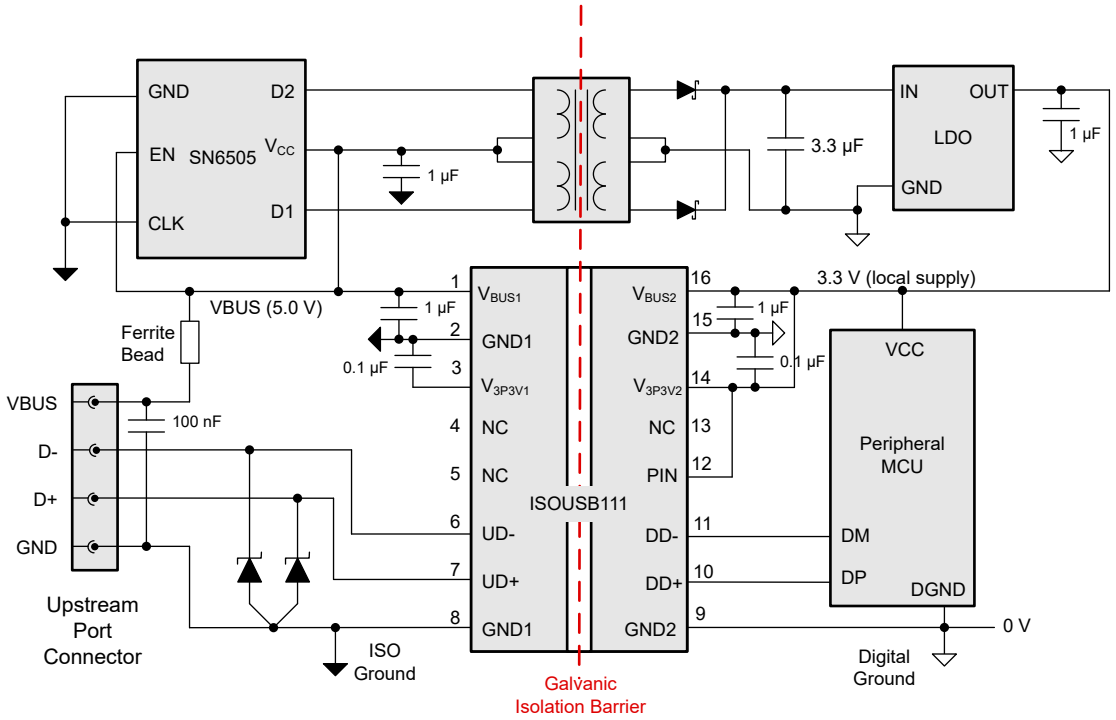

Figure 8-3. Isolated Bus-Powered Peripheral Using ISOUSB111

8.1.4 Application Curve

8.1.4.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 8-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 8-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 169 years. Other factors, such as package size, pollution degree, material group, and more, can further limit the working voltage of the component. The working voltage of DW-16 and DWX-16 packages is specified up to 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 169 years.

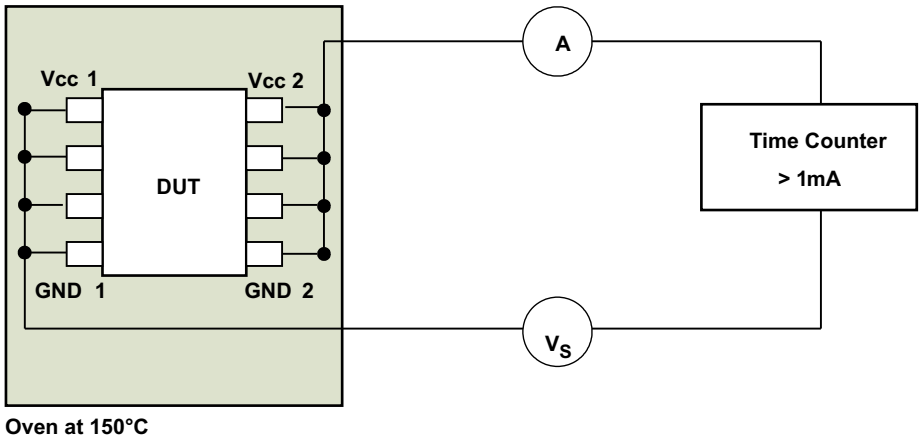

Figure 8-4. Test Setup for Insulation Lifetime Measurement

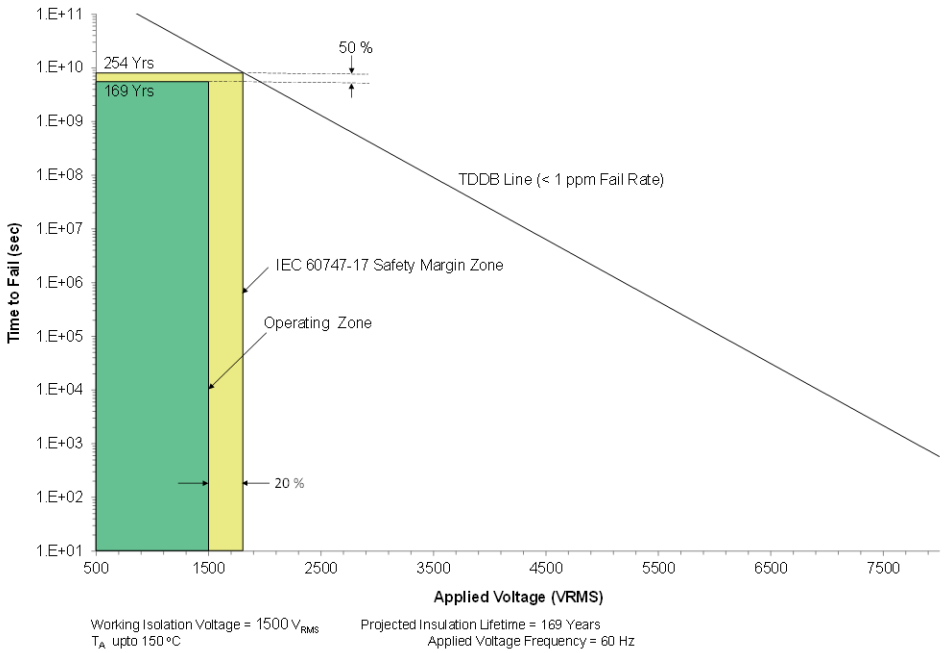

Figure 8-5. Insulation Lifetime Projection Data

8.2 Power Supply Recommendations

0.1 µF capacitors are recommended to be placed close to V_{3P3Vx} pins to GNDx. 1-µF capacitors are recommended to be placed close to V_{BUSx} pins to GNDx.

These decoupling capacitor recommendations are irrespective of whether the 3.3 V supplies are provided externally or generated using internal LDOs.

Refer to the Section 8.3.1.1 section for recommended placement of the decoupling capacitors. Small footprint capacitors (0402/0201) are recommended so that these can be placed close to the supply pins and corresponding ground pins on the top layer without the use of vias.

While isolating a host/hub or bus-powered peripherals, isolated power is needed and can be generated with the help of a transformer driver such as TI's SN6505B. For such applications, detailed power supply design, and transformer selection recommendations are available in the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

8.3 Layout

8.3.1 Layout Guidelines

Two layers are sufficient to accomplish a low EMI PCB design.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, minimizing the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector is recommended. Vias and stubs on D+/D- lines must be avoided.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90-Ω differential impedance and as close to 45-Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer. There must not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- ESD structures must be placed on the top layer, close to the connector, and right on the D+/D- traces without vias. Ground routing for the ESD structures must be made in the top layer if possible, else must have a strong connection to the ground plane with multiple vias.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

8.3.1.1 Layout Example

The layout example in this section shows the recommended placement for de-coupling capacitors and ESD protection diodes. A continuous ground plane is recommended below the D+/D- signal traces. Small footprint capacitors (0402/0201) are recommended so that these can be placed very close to the supply pins and corresponding ground pins and connected using the top layer. There must not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins. The ESD protection diodes must be placed close to the connector with a strong connection to the ground plane. The example shown is for an isolated host or hub, but similar considerations apply for isolated peripherals also. The 120-µF capacitor on VBUS only applies to host or hub and must not be used for peripherals. A ferrite bead, with DC resistance less than 100 mΩ, can be optionally placed on the VBUS route, after the 100-nF (and 120-µF) capacitors to prevent transients such as ESD from affecting the rest of the circuits.

For best performance, minimizing the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector is recommended. Vias and stubs on D+/D- lines must be avoided.

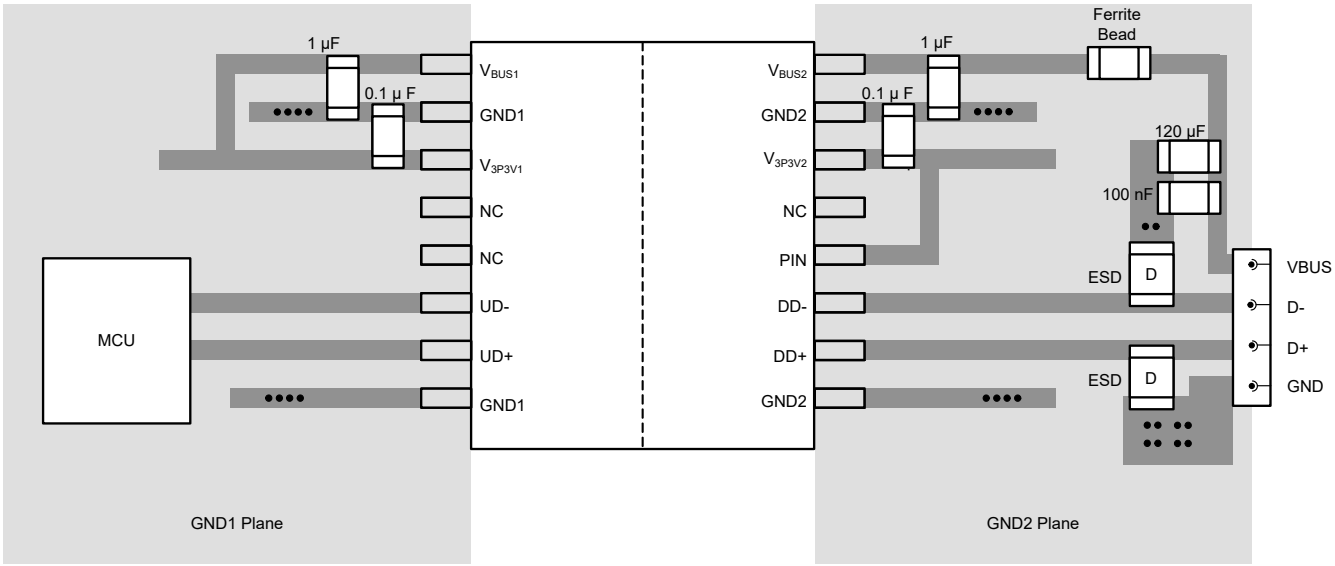

Figure 8-6. Layout Example for ISOUSB111

8.3.1.2 PCB Material

For digital circuit boards operating at less than 500 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*, application note.
- Texas Instruments, *Isolation Glossary*, application note.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2023) to Revision E (July 2025)	Page
• Updated the number format for tables, figures, and cross-references throughout the document	1
• VIOTM updated to 8000Vpk	7

Changes from Revision C (September 2022) to Revision D (January 2023)	Page
• Removed "Basic" option from data sheet	1

Changes from Revision B (July 2022) to Revision C (September 2022)	Page
• Updated ESD specifications.	5

Changes from Revision A (April 2022) to Revision B (July 2022)	Page
• Updated device status to Production Data	1

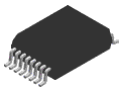
Changes from Revision * (November 2021) to Revision A (April 2022)	Page
• T_A Max value updated to 125°C	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

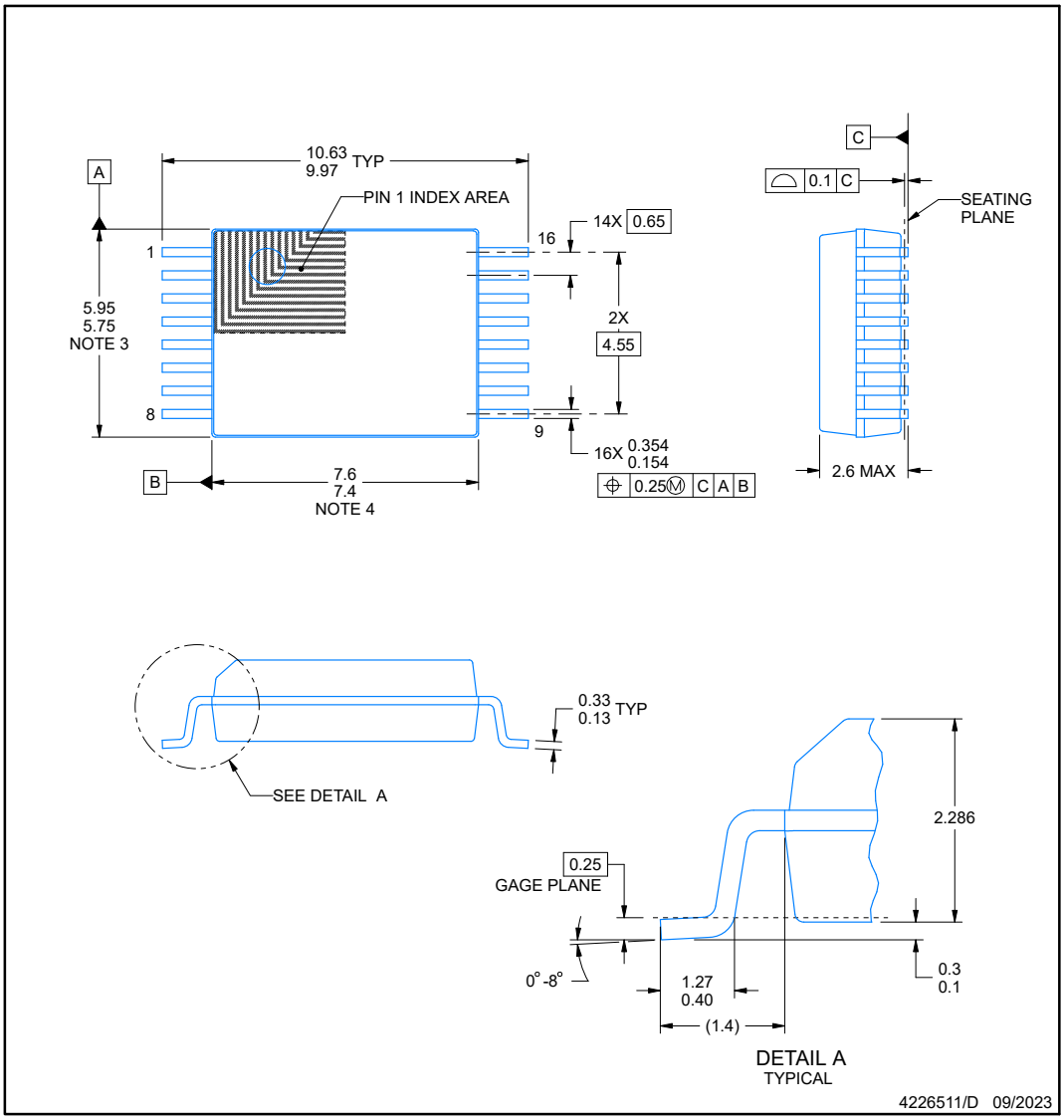
PACKAGE OUTLINE

DWX0016A



SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



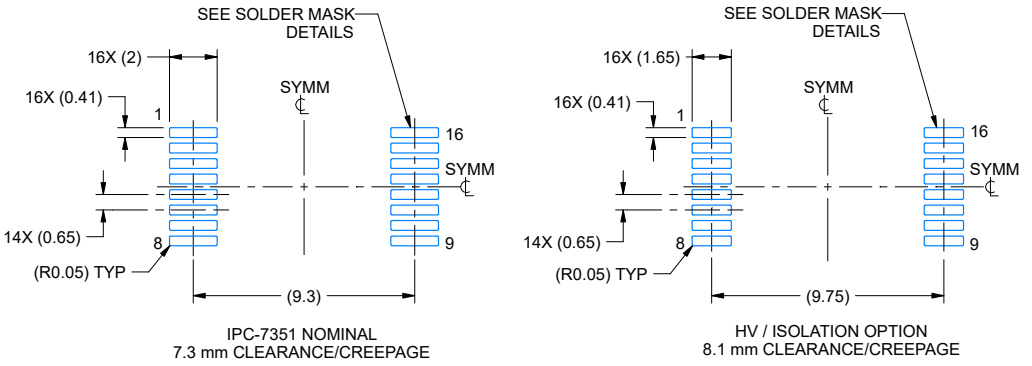
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

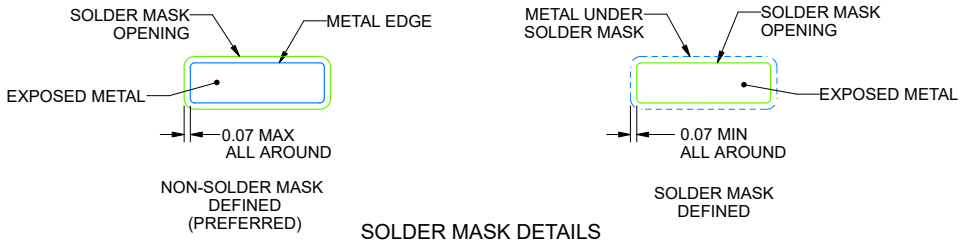
EXAMPLE BOARD LAYOUT

DWX0016A — **SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE: 4X



SOLDER MASK DETAILS

4226511/D 09/2023

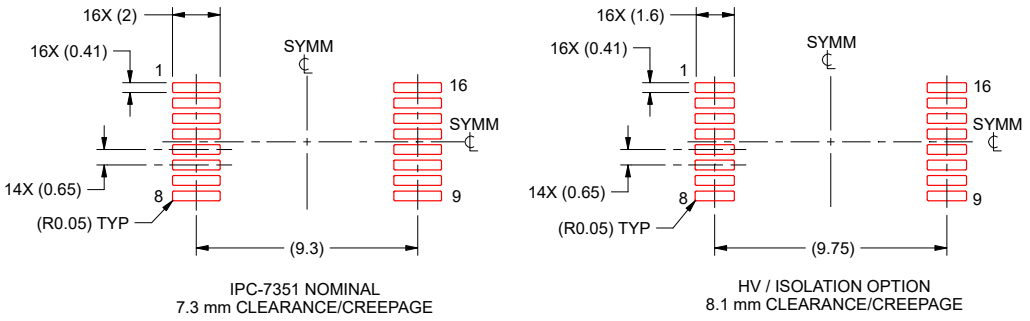
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWX0016A — **SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLES
BASED ON 0.125 mm THICK STENCIL
SCALE: 4X

4226511/D 09/2023

NOTES: (continued)

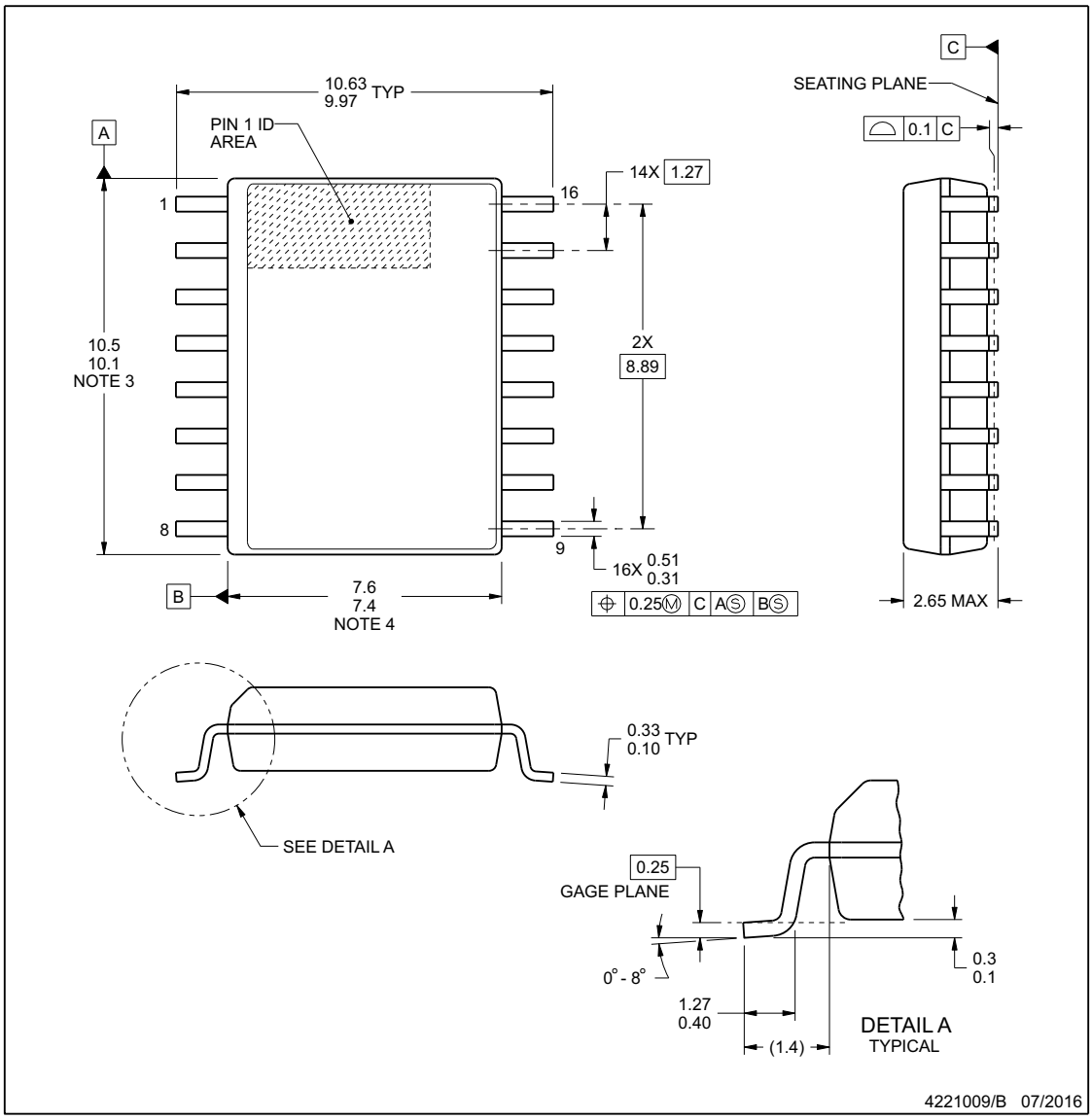
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

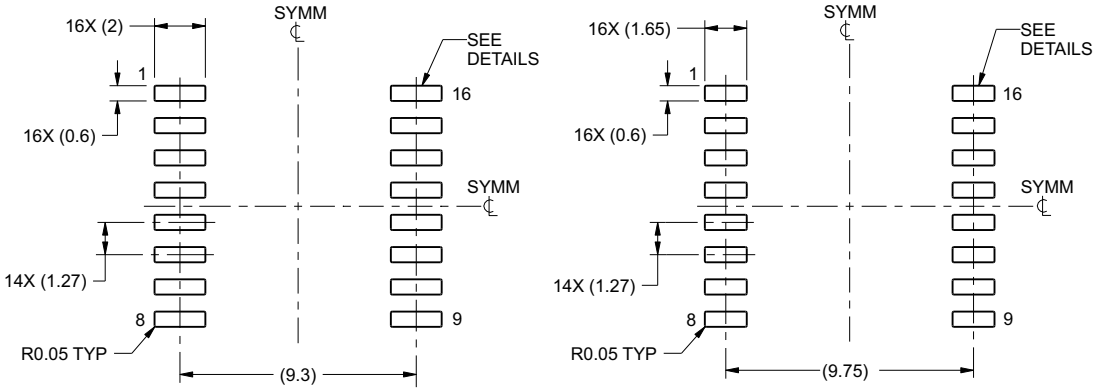
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

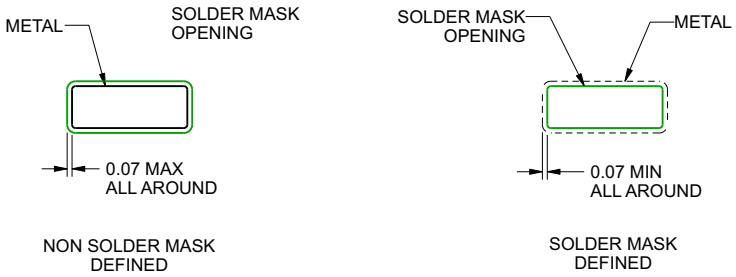
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

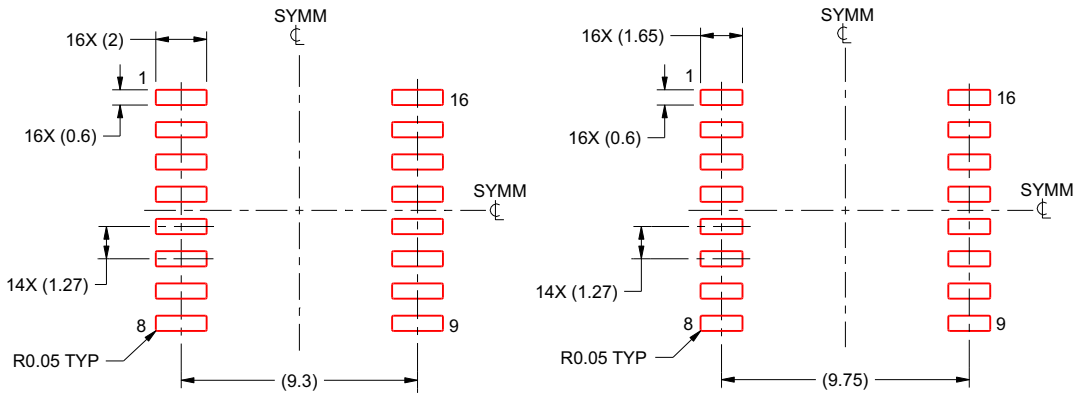
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

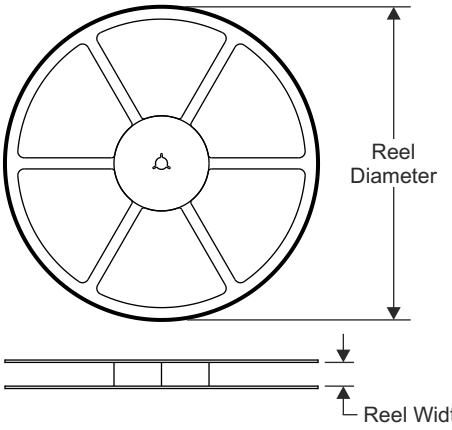
4221009/B 07/2016

NOTES: (continued)

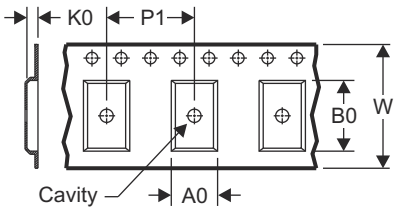
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

11.1 Tape and Reel Information

REEL DIMENSIONS

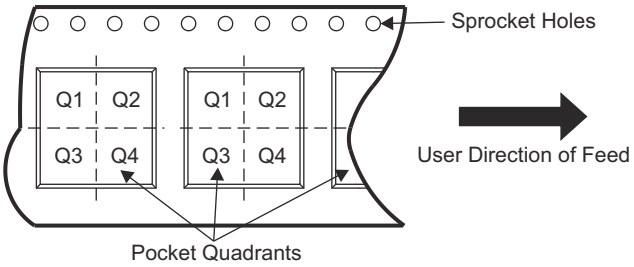


TAPE DIMENSIONS



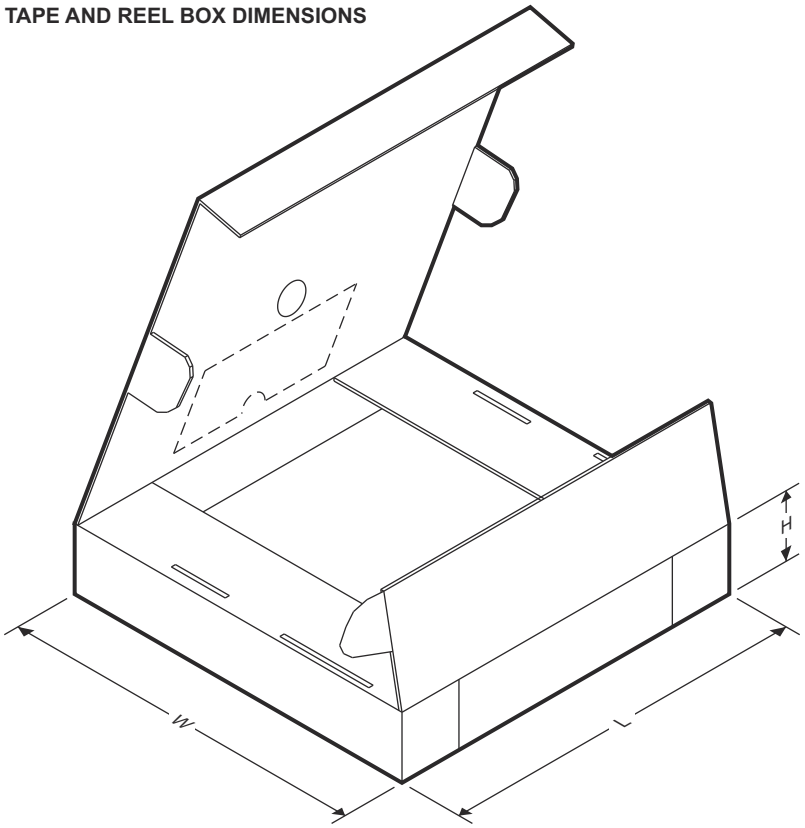
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOUSB111DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISOUSB111DWXR	SSOP	DWX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOUSB111DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISOUSB111DWXR	SSOP	DWX	16	1000	350.0	350.0	43.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOUSB111DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOUSB111
ISOUSB111DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOUSB111
ISOUSB111DWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOUSB111DWXR	Active	Production	SSOP (DWX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOU111
ISOUSB111DWXR.A	Active	Production	SSOP (DWX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOU111
ISOUSB111DWXR.B	Active	Production	SSOP (DWX) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

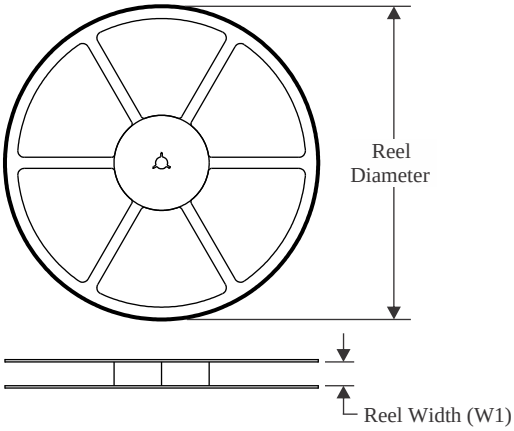
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

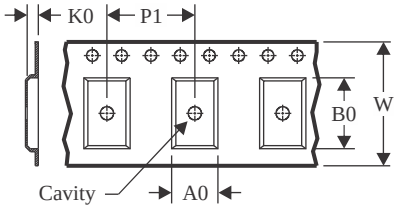
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

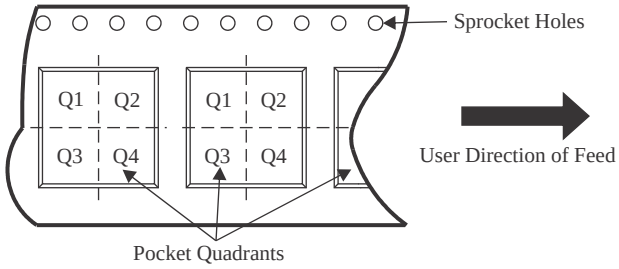


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

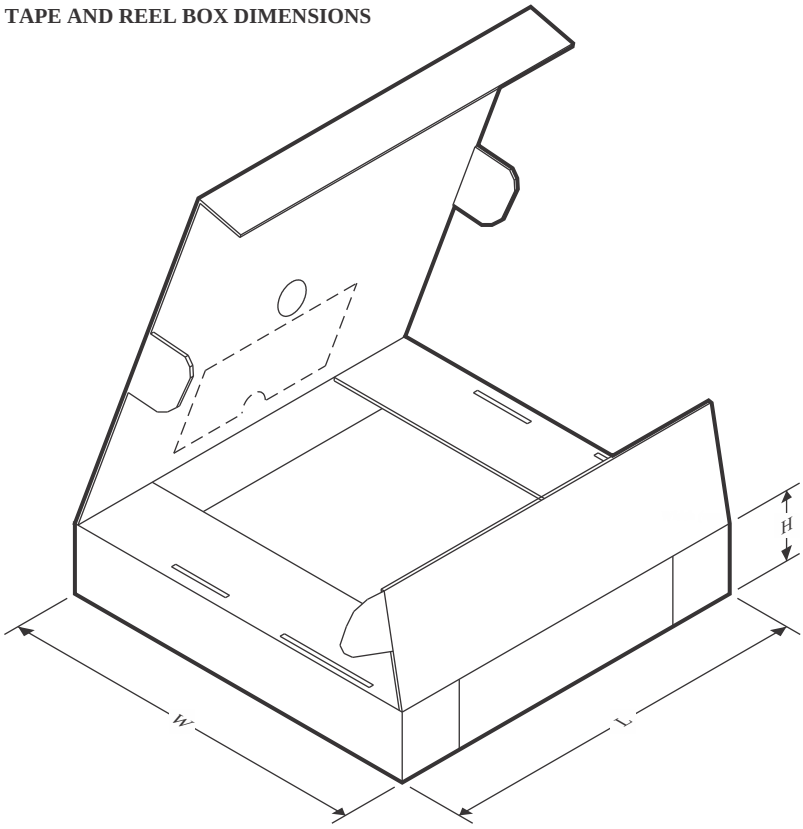
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOUSB111DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISOUSB111DWXR	SSOP	DWX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOUSB111DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISOUSB111DWXR	SSOP	DWX	16	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

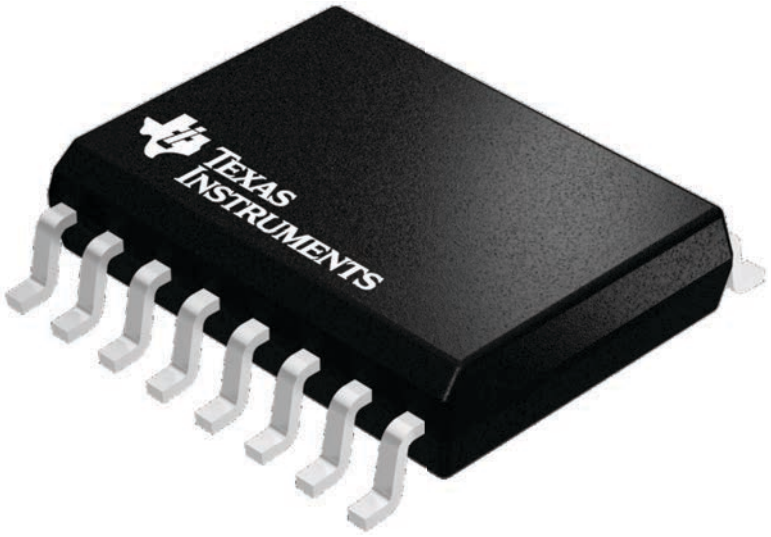
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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