ISOS510-SP Radiation Hardened, Current-Driven Analog Isolator With Transistor Output

1 Features

- Radiation Performance
  - Total Ionizing Dose (TID) characterized up to 100krad(Si)
  - TID RLAT/RHA up to 100krad(Si)
  - Single-Event Latch-up (SEL) Immune to LET up to 75MeV-cm^2/mg at 125°C
  - Single-event transient (SET) characterized LET up to 75MeV-cm^2/mg
- SMD# 5962R2620601PXE
- QML Class P
  - Meets NASA ASTM E595 Outgassing Spec
  - Military Temp Range (-55°C to 125°C)
- 1-channel diode input
- Current transfer ratio (CTR) at I_F = 5mA, V_{CE} = 5V: 95% to 164%
- High collector-emitter voltage: V_{CE} (max) = 30V
- Robust SiO_2 isolation barrier
  - Isolation rating: 3750V_{RMS}
  - Working voltage: 500V_{RMS}, 707V_{PK}
  - Surge capability: up to 10kV
- Response time: 3µs (typical) at V_{CE} = 10V, I_C = 2mA, R_L = 100Ω
- Small 4-pin package (DFG)

2 Applications

- Satellite electrical power systems (EPS)
- Communications Payload
- Radar Imaging Payload

3 Description

The ISOS510-SP radiation-hardened device is a single-channel, current-driven, analog isolator with transistor output. The device offers significant reliability and performance advantages compared to other current-driven analog isolators, including high bandwidth, low turn-off delay, low power consumption, wider temperature ranges, flat current transfer ratio (CTR), and tight process controls resulting in small part-to-part skew. These performance advantages stay stable across radiation, temperature, and lifetime.

ISOS510-SP is offered in small a SOIC-4 package with 2.54mm pin pitch, supporting a 3.75kV_{RMS} isolation rating . The high performance and reliability of ISOS510-SP enables these devices to be used in aerospace and defense applications such as feedback loops in isolated DC/DC modules, satellite propulsion power processing units, spacecraft battery management systems, and more.

Package Information

PART NUMBER	GRADE	PACKAGE (1)	PACKAGE SIZE(2)
ISOS510-SP	QMLP	DFG (SO-4) 4-pin plastic	7.0mm × 3.5mm Mass = 89.6mg

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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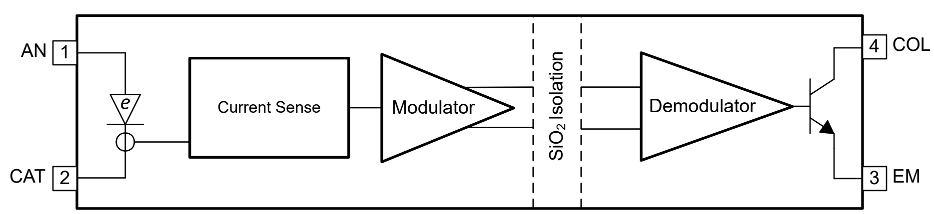

Simplified Schematic

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4 Pin Configuration and Functions

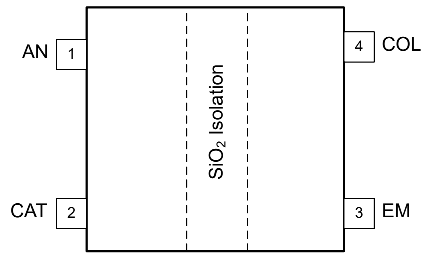

Figure 4-1. ISOS510-SP 4-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE [(1)]	DESCRIPTION
NO.	NAME		
1	AN	I	Anode connection of diode input
2	CAT	I	Cathode connection of diode input
3	EM	O	Emitter for transistor
4	COL	O	Collector for transistor

(1) I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range of -55℃ to +125℃ (unless otherwise noted)(1)

		MIN	MAX	UNIT
$I_{F(max)}$	Maximum Input forward current		15	mA
V_{CEO}	Collector-emitter voltage		35	V
V_{ECO}	Emitter-collector voltage		7	V
I_{FP}	Input pulse forward current (1µs width)		1	A
V_R	Input reverse voltage		7	V
P_I	Input power dissipation		86	mW
I_C	Collector current		15	mA
P_C	Collector power dissipation		86	mW
P_T	Total power dissipation		172	mW
T_A	Ambient temperature	–55	125	°C
T_J	Junction temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under the operational sections of this document. If used outside the listed operational conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range of -55℃ to +125℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$I_{F(ON)}$	Input ON-state forward current	0.7		10	mA
V_R	Input reverse voltage			5	V
V_{CEO}	Collector-emitter voltage	-5		30	V
T_A	Ambient temperature	-55		125	°C

5.4 Thermal Information

THERMAL METRIC (1)		ISOS510-SP	UNIT
		DFG (SOIC)	
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	283.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	173.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	201.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	125.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	198.0	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics application note.

5.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE 4-DFG	UNIT
PACKAGE				
CLR	External clearance[1]	Side 1 to side 2 distance through air	> 5	mm
CPG	External creepage[1]	Side 1 to side 2 distance across package surface	> 5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	V
ELECTRICAL				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test.	500	V_{RMS}
		DC voltage	707	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	5303	V_{PK}
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	3750	V_{RMS}
V_{IMP}	Maximum impulse voltage [2]	Tested in air, 1.2/50μs waveform per IEC 62368-1	7200	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{ISOM} \geq 1.3 \times V_{IMP}$; tested in oil (qualification test), 1.2/50μs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge[4]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1MHz	1	pF
R_{IO}	Insulation resistance, input to output[5]	V_{IO} = 500V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the surge immunity of the package.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

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5.6 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SO-4 PACKAGE (DFG)						
I_S	Safety limiting input current	$R_{θJA}$= 283.9℃/W, V_F = 1.4V, T_J = 150℃, T_A = 25℃			300	mA
		$R_{θJA}$=283.9℃/W, V_{CEO} = 40V, T_J = 150℃, T_A = 25℃			10.5	mA
		$R_{θJA}$= 283.9℃/W, V_{CEO} = 24V, T_J =150℃, T_A = 25℃			17.5	mA
		$R_{θJA}$= 283.9℃/W, V_{CEO} = 15V, T_J = 150℃, T_A = 25℃			28	mA
P_S	Safety limiting total power	$R_{θJA}$= 283.9℃/W, T_J = 150℃, T_A = 25℃			420	mW
T_S	Maximum safety temperature				150	℃

(1) The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{θJA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{θJA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{θJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

5.7 Electrical Characteristics

over recommended operating conditions unless otherwise noted; includes RLAT at TA = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_F	Input forward voltage	I_F = 5mA		1.2	1.6	V
I_R	Input reverse current	V_R = 5V			10	µA
C_{IN}	Input capacitance	At 1MHz, V_F = 0V, T_A = 25℃		20		pF
OUTPUT						
C_{CE}	Collector-emitter capacitance	1MHz, V_F = 0V, T_A = 25℃		15		pF
$V_{CE(SAT)}$	Collector-emitter saturation voltage	I_F = 10mA, I_C = 1mA			0.3	V
I_{C_DARK}	Collector dark current	V_{CE} = 20V, I_F = 0mA			100	nA
I_{EC}	Reverse current	V_{EC} = 5V, I_F = 0mA			50	µA
I_{C_OFF}	OFF_state collector current	V_F = 0.7V, V_{CE} = 30V			10	µA
CTR						
CTR[(1)]	Current Transfer Ratio	I_F = 2mA, V_{CE} = 5V	80	130	180	%
		I_F = 5mA, V_{CE} = 5V	95	127	164	%

(1) CTR (%) = (I_C / I_F) x 100%

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5.8 Switching Characteristics

All specifications are at T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC						
t_r	Rise time, see Figure 6-2 and Figure 6-3	V_{CC} = 10V, I_C = 2mA, R_L= 100Ω, C_L = 50pF		3.2		µs
t_f	Fall time, see Figure 6-2 and Figure 6-3	V_{CC} = 10V, I_C = 2mA, R_L= 100Ω, C_L = 50pF		4.0		µs
T_{ON}	Turn on time, see Figure 6-2 and Figure 6-3	V_{CC} = 10V, I_C = 2mA, R_L= 100Ω, C_L = 50pF		5.7		µs
		V_{CC}=5V, R_L=4.7kΩ, I_F=1.6mA, C_L=50pF		3.5		µs
		V_{CC}=5V, R_L=1.9kΩ, I_F=16mA, C_L=50pF		0.62		µs
T_{OFF}	Turn off time, see Figure 6-2 and Figure 6-3	V_{CC} = 10V, I_C = 2mA, R_L= 100Ω, C_L = 50pF		3.6		µs
		V_{CC}=5V, R_L=4.7kΩ, I_F=1.6mA, C_L=50pF		8		µs
		V_{CC}=5V, R_L=1.9kΩ, I_F=16mA, C_L=50pF		10		µs
t_s	Storage time; time required for the output waveform to change from 0% (100%) to 10% (90%) when input is turned on and back off, see Figure 6-3	V_{CC} = 5V, I_F = 1.6mA, R_L = 4.7kΩ			21	µs
BW	Bandwidth, see Figure 6-4	V_{IN_DC} = 5V, V_{IN_AC} = 1Vpk, R_{IN} = 2kΩ V_{CC}= 5V, R_{LOAD} = 100Ω, C_L = 50pF, measured at V_{CE} –3dB sinewave		680		kHz

6 Parameter Measurement Information

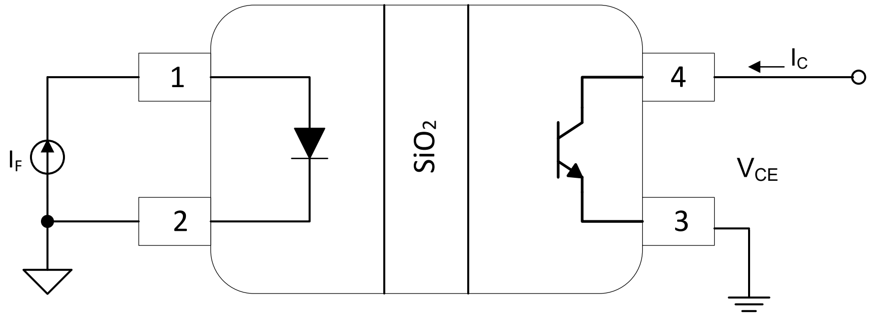

Figure 6-1. ISOS510-SP Test Circuit for CTR

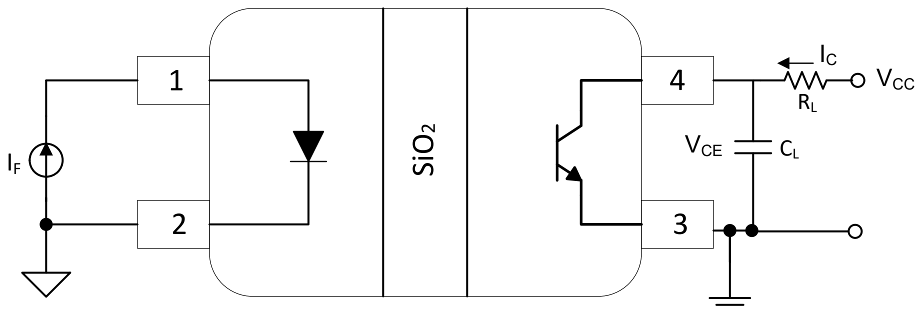

Figure 6-2. ISOS510-SP Test Circuit for Switching Timing

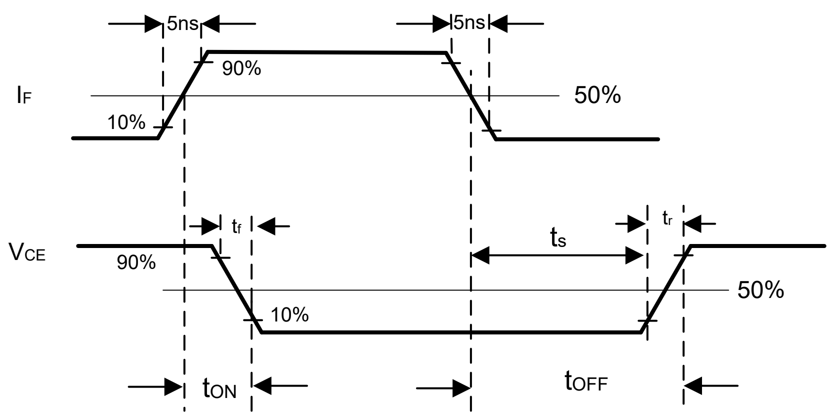

Figure 6-3. ISOS510-SP Switching Timing Waveforms

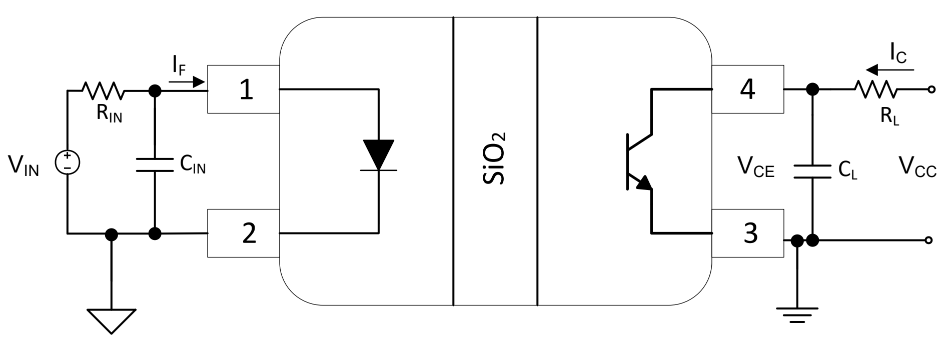

Figure 6-4. ISOS510-SP Test Circuit for Bandwidth

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7 Detailed Description

7.1 Overview

The functional block diagram of ISOS510-SP device is shown in Section 7.2. The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier that contains information on how much current is flowing through the input pins. The receiver demodulates the signal after advanced signal conditioning and drives the transistor in the output stage. This device also incorporates advanced circuit techniques to maximize bandwidth and minimize radiated emissions. Figure 7-2 shows conceptual details of how the OOK scheme works.

7.2 Functional Block Diagram

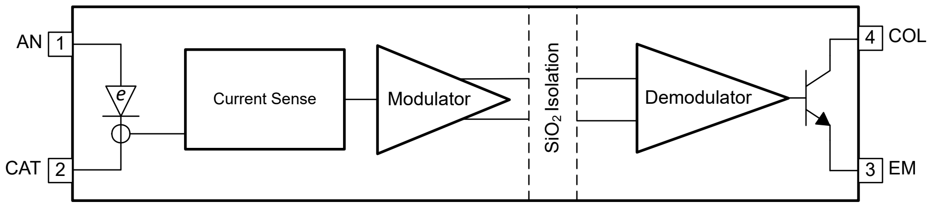

Figure 7-1. Conceptual Block Diagram of an Opto-emulator ISOS510-SP

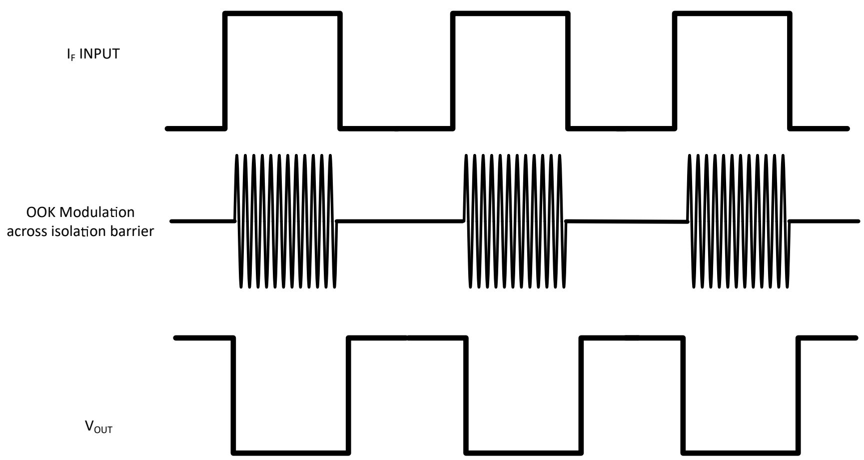

Figure 7-2. On-off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

The ISOS510-SP device can isolate both analog and digital signals due to the current-driven input stage. When supplied an input current (I_F) of at least 0.7mA to the AN pin, this powers the internal modulator which includes the modulator and current sense blocks. The I_F is sensed and converted into a high frequency carrier that is passed across the isolation barrier. Once demodulated on the secondary side of the device, this is used to bias the output transistor which tries to sink current from an external source into the COL pin (I_C) proportional to the I_F value. The ratio of I_C to I_F is the current transfer ratio (CTR).

7.4 Device Functional Modes

7.4.1 Active Mode

If the external source or circuit connected to the COL pin can supply enough current to satisfy the CTR of the device for a given I_F value, then the device is considered in "active mode". This is how analog signals can be transmitted through this device.

7.4.2 Saturation Mode

If the external source or circuit connected to the COL pin cannot supply enough current to satisfy the CTR of the device for a given I_F value (For example, I_C = 1mA when I_F = 10mA), then the output transistor saturates and goes into a low impedance state. The device is considered in "saturation mode". This is how digital signals can be transmitted through this device.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

ISOS510-SP is commonly used in the feedback control loops of isolated power supplies. This device is used to solve the problem of feeding back current while isolating the primary and secondary domains to regulate the output voltage.

In power supplies, the output voltage is isolated from main input voltage using a transformer (for example: flyback converter). For analog power supply units, the controller IC is typically on the primary side of the transformer. For closed loop control, measuring the output voltage on the secondary side and feeding the voltage back to the controller on the primary is necessary. The most common method of achieving this design is using an isolator such as ISOS510-SP, error amplifier (commonly TL1431SP), and a voltage comparator to form a feedback loop across the isolation barrier

Figure 8-1 illustrates a typical isolated power supply. In this implementation, the output voltage is sensed by an error amplifier using the resistor divider (R1 and R2). Depending on the voltage level that the error amplifier senses, the TL1431SP can drive the current of the ISOS510-SP higher or lower which is then compared to a voltage reference. The information is passed across the isolation barrier through ISOS510-SP to the primary side, where the PWM control circuit modulates the power stage to regulate the output voltage. The TL1431SP and ISOS510-SP play an important role for stable feedback and control loop.

The ISOS510-SP devices enable improvements in transient response, reliability, and stability as compared to commonly used optocoupler as the CTR is stable over wide temperature range providing a small, low-cost, highly reliable, and easy-to-design implementation.

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8.1.1 Typical Application

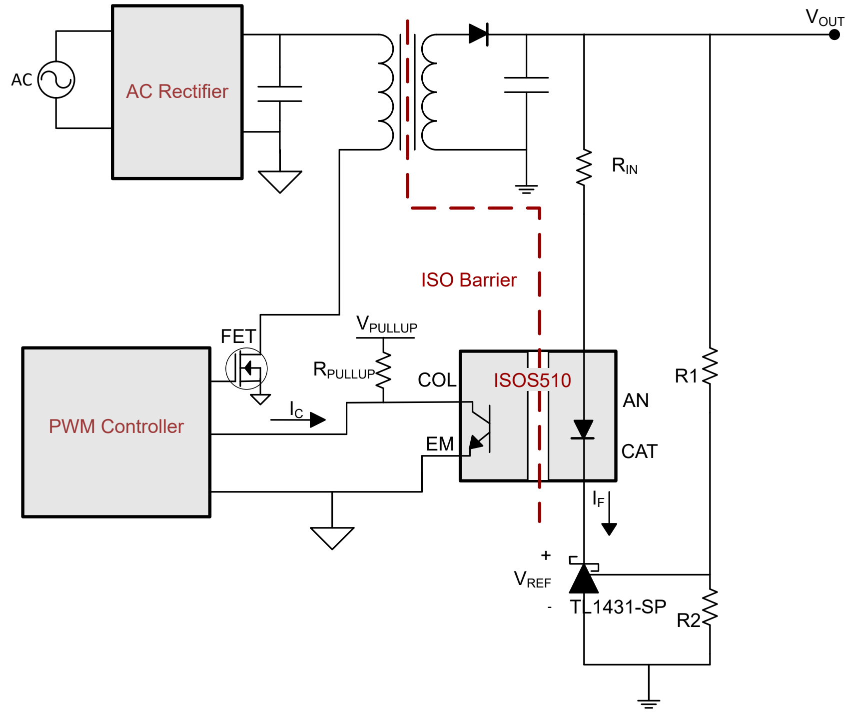


Figure 8-1. Typical Isolated Power Supply Application Using ISOS510-SP

8.1.1.1 Design Requirements

To design with ISOS510-SP, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input forward current range, I_F	0.7mA (min), 10mA (max)
Current transfer ratio at I_F = 5mA, CTR	100% to 155%
Collector current tolerance, I_C	30mA (max)
Collector-emitter voltage (saturation), $V_{CE(SAT)}$	0.3V (max)
Input forward voltage, V_F	1.2V (typ)

8.1.1.2 Detailed Design Procedure

This section presents the design procedure for using the ISOS510-SP device. External components must be selected to operate ISOS510-SP within the *Recommended Operating Conditions*. The following recommendations on component selection focus on the design of a typical feedback control loop for an isolated flyback converter.

When using an isolator in a feedback control loop for an isolated power supply, many variables can affect how to properly use the isolator, including the output voltage of the power supply and the type of controller the feedback signal is being sent to. For this example, assume that the output voltage of this power supply, V_{OUT}, is 5V, and the PWM controller being used has an integrated error amplifier with a COMP pin that acts as the output of this amplifier.

8.1.1.2.1 Sizing R_{PULLUP}

The transistor output of ISOS510-SP operates in active, saturation, reverse, and cut-off regions, just like a regular transistor. To verify that the output does not get damaged when the output is saturated, the minimum value of R_{PULLUP} can be calculated for a given pull-up voltage, V_{PULLUP}, in Equation 1:

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{CE(SAT)}}{I_{C(MAX)}} \tag{1}$$

For the example of a feedback loop application, we can calculate the minimum required value for R_{PULLUP} for a given V_{PULLUP} of 10V, the maximum output voltage of the error amplifier ($V_{COMP(MAX)}$ of 2.5V, and the maximum output current of the error amplifier is internally clamped at 1.6mA. The equation to calculate R_{PULLUP} is shown in Equation 2:

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{COMP(MAX)}}{I_{COMP(CLAMP)}} = \frac{10V - 2.5V}{1.6mA} = 4.66k\Omega \tag{2}$$

8.1.1.2.2 Sizing R_{IN}

The input side of ISOS510-SP is current-driven. To limit the amount of current flowing into the AN pin, placing a series resistor, R_{IN}, in series with the input as shown in Figure 8-1 is recommended.

Depending on how the ISOS510-SP device is being used, the value of R_{IN} can vary quite a bit. However, at a high level, to make sure the input does not get damaged, the minimum value of R_{IN} can be calculated for a given input voltage, V_{IN}, in Equation 3:

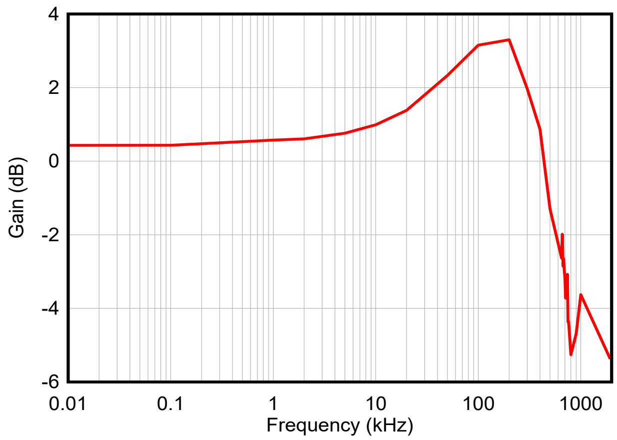
$$R_{IN} > \frac{V_{IN} - V_F}{I_{C(MAX)}} \tag{3}$$

However, in the use case of a feedback loop, R_{IN} directly affects the mid-band gain of the loop. Assuming that the TL1431SP has been configured to give a reference voltage, V_{REF}, of 2.5V and R_{PULLUP} is 5kΩ, Equation 4 is used to calculate the maximum value of R_{IN} verifying that the V_{COMP} voltage on the primary side can be pulled to the saturation voltage of the ISOS510-SP, $V_{CE(SAT)}$.

$$R_{IN} < \frac{(V_{OUT} - V_{REF} - V_F) \times R_{PULLUP} \times CTR_{MIN}}{V_{PULLUP} - V_{CE(SAT)}} = \frac{(5V - 2.5V - 1.2V) \times 5k\Omega \times 100\%}{10V - 0.3V} = 670\Omega \tag{4}$$

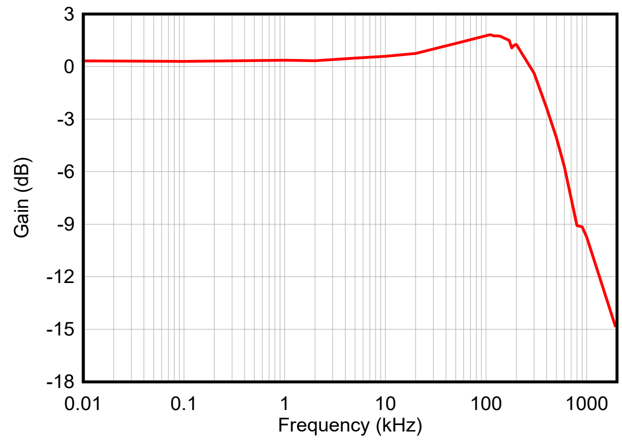
8.1.1.3 Application Curves

The following curves shows ISOS510-SP bandwidth performance over different loading conditions where V_{IN} = $5V_{DC}$ + $2V_{PK}$. See Figure 6-4 for setup details.



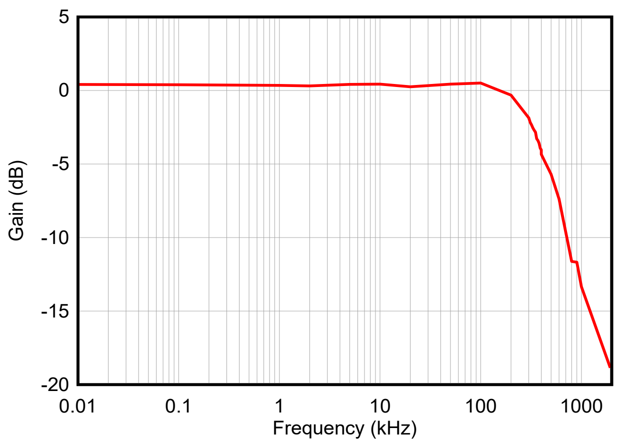
C_{IN} = 5pF R_{IN} = 2kΩ C_L = 50pF R_L = 100Ω V_{CC} = 5V

Figure 8-2. Bandwidth at R_L = 100Ω



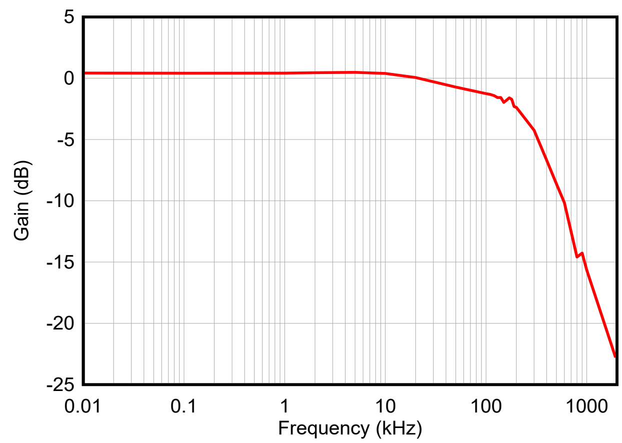
C_{IN} = 5pF R_{IN} = 2kΩ C_L = 50pF R_L = 1kΩ V_{CC} = 8V

Figure 8-3. Bandwidth at R_L = 1kΩ



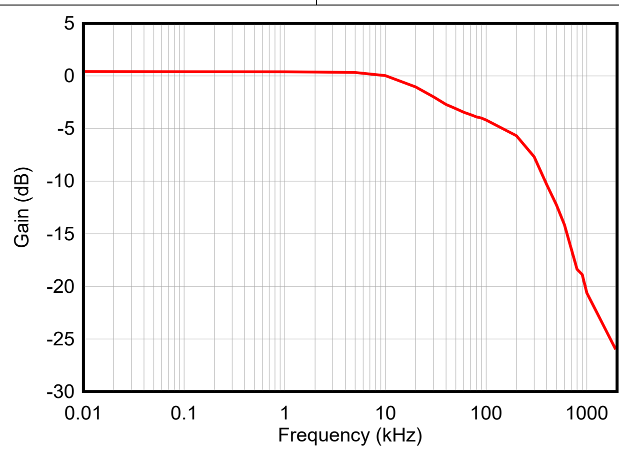
C_{IN} = 5pF R_{IN} = 2kΩ C_L = 50pF R_L = 2kΩ V_{CC} = 10V

Figure 8-4. Bandwidth at R_L = 2kΩ



C_{IN} = 5pF R_{IN} = 2kΩ C_L = 50pF R_L = 4.7kΩ V_{CC} = 10V

Figure 8-5. Bandwidth at R_L = 4.7kΩ



C_{IN} = 5pF R_{IN} = 2kΩ C_L = 50pF R_L = 10kΩ V_{CC} = 45V

Figure 8-6. Bandwidth at R_L = 10kΩ

8.2 Power Supply Recommendations

ISOS510-SP does not require a dedicated power supply to operate since there is no supply pin. Take care to not violate recommended I/O specifications, such as the minimum I_F, for proper device functionality.

8.3 Layout

8.3.1 Layout Guidelines

- The device connections to ground must be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane must use a direct connection or two vias for minimum inductance.

8.3.2 Layout Example

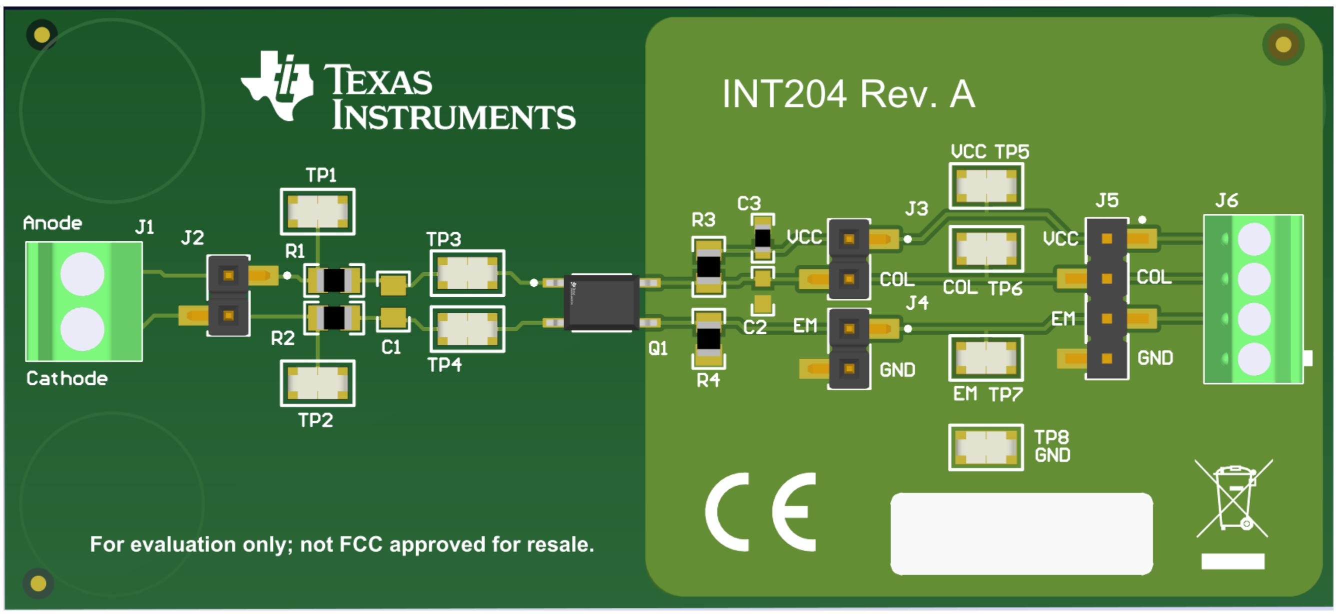


Figure 8-7. Layout Example of ISOS510-SP With a Single Layer Board

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary,* application note
- Texas Instruments, *Introduction to Opto-Emulators,* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

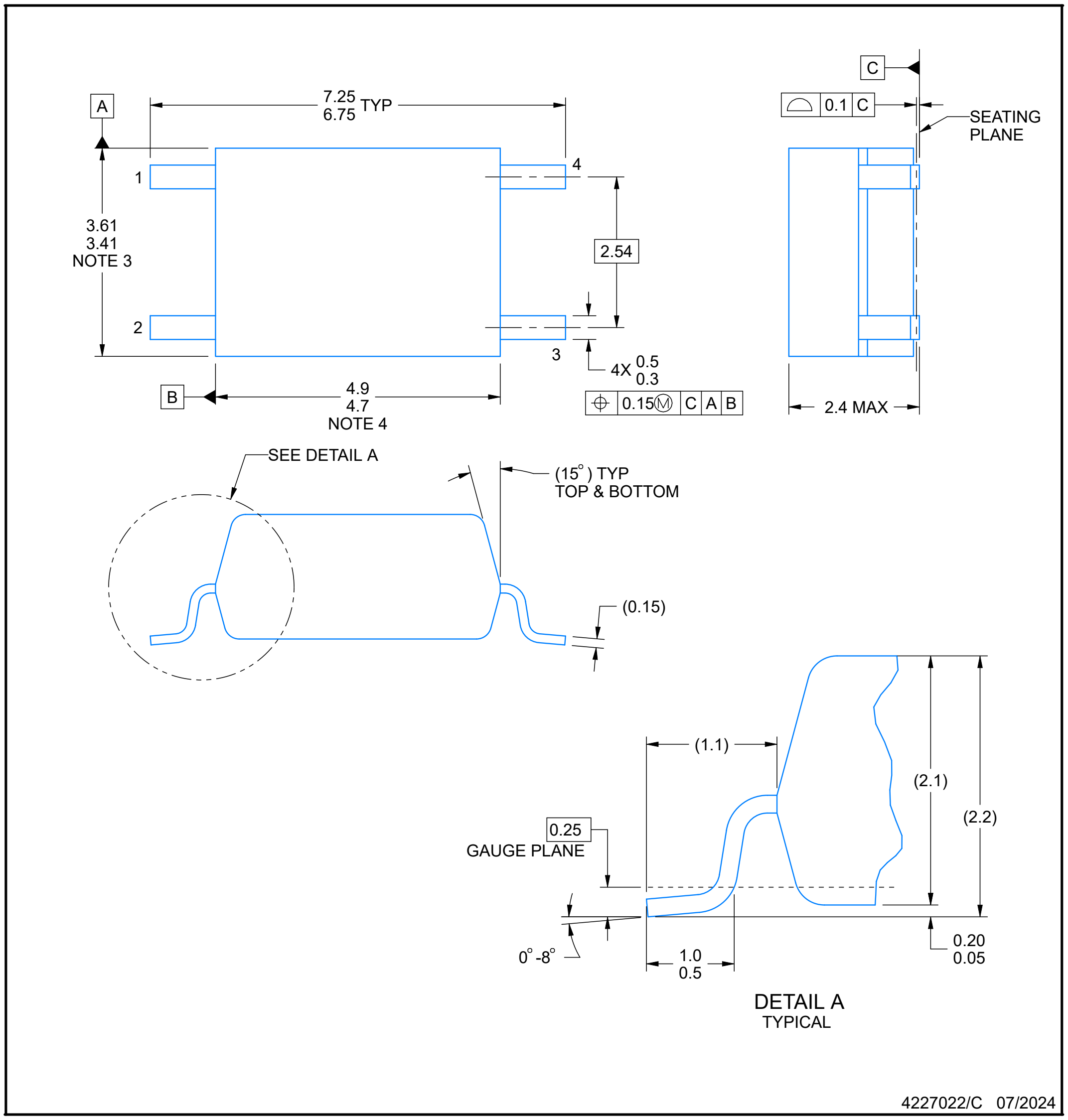
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

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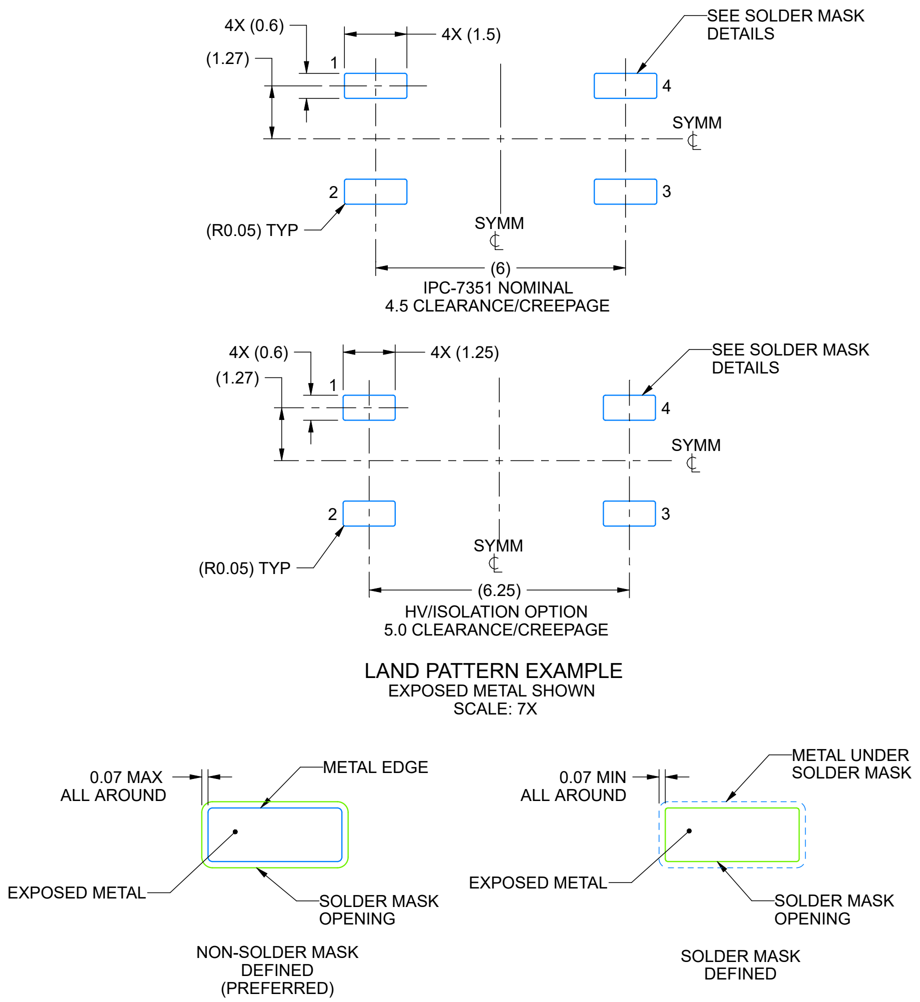
EXAMPLE BOARD LAYOUT

DFG0004A **SOIC - 2.4 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X

SOLDER MASK DETAILS

4227022/C 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

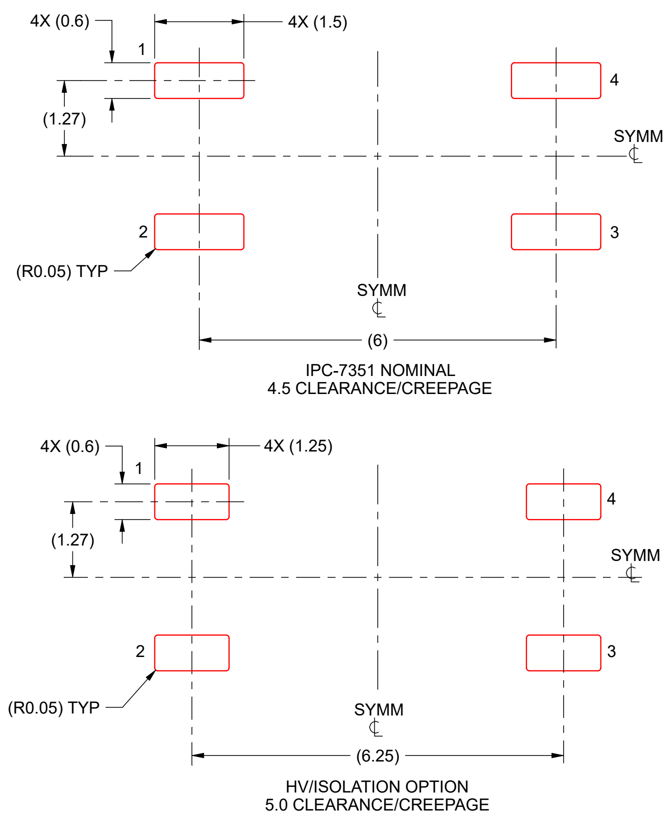
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4227022/C 07/2024

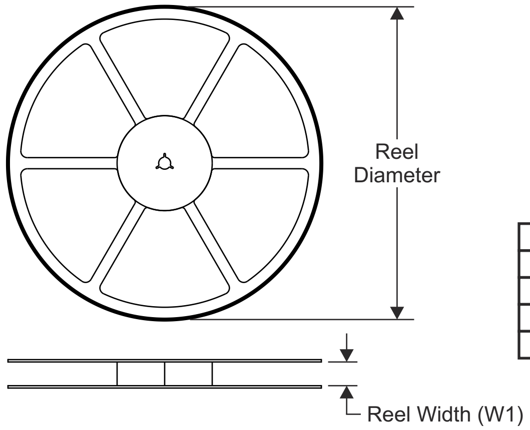
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

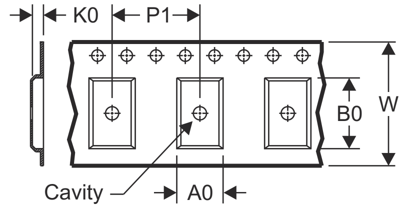
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

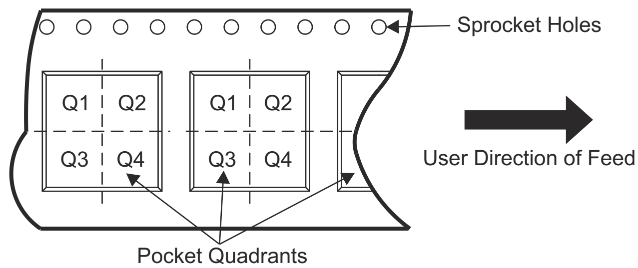


TAPE DIMENSIONS



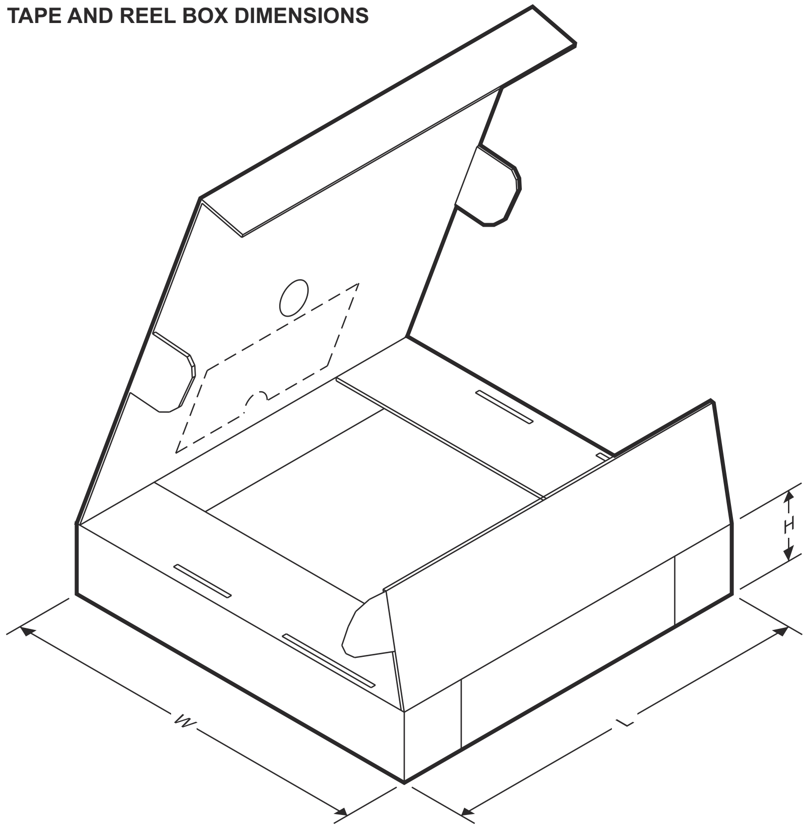
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XISOS510DFGTSP	SO-4	DFG	4	250	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XISOS510DFGTSP	SO-4	DFG	4	250	356.0	356.0	35.0

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