











ISO7420FCC

SLLSED3C -JUNE 2013-REVISED JULY 2015

ISO7420FCC Low-Power Dual Channel Digital Isolator

1 Features

- Signaling Rate: 50 Mbps (5-V Supplies)
- · Output is Low in Default Mode
- · Integrated Noise Filter on the Input Pins
- Low Power Consumption: Typical I_{CC} per Channel
 - 1.8 mA at 1 Mbps, 3.9 mA at 25 Mbps (5-V Supplies)
 - 1.4 mA at 1 Mbps, 2.6 mA at 25 Mbps (3.3-V Supplies)
- Low Propagation Delay: 20 ns Typical (5-V Supplies)
- Channel-to-Channel Output Skew: 2 ns Maximum
- 3.3-V and 5-V Level Translation
- Wide T_A Range Specified: –40°C to 125°C
- 60-KV/µs Transient Immunity, Typical (5-V Supplies)
- Low Emissions
- Isolation Barrier Life: > 25 Years
- Operates from 2.7-V to 5.5-V Supply Levels
- Narrow Body SOIC-8 Package
- Safety and Regulatory Approvals
 - 4242 V_{PK} Isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
 - 2.5 KV_{RMS} Isolation for 1 Minute per UL 1577
 - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
 - GB4943.1-2011 CQC Certification

2 Applications

- Opto-Coupler Replacement in:
 - Industrial FieldBus
 - ProfiBus
 - ModBus
 - DeviceNet™ Data Buses
 - Servo Control Interface
 - Motor Control
 - Power Supplies
 - Battery Packs

3 Description

ISO7420FCC provides galvanic isolation up to 2500 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. This device has two isolated channels. Each channel has a logic input and output buffer separated by a silicon dioxide (SiO₂) insulation barrier. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix F indicates low-output option in fail-safe conditions (see Table 2). This device has integrated noise filter for harsh environments where short noise pulses may be present at the device input pins.

ISO7420FCC has TTL input thresholds and operates from 2.7-V to 5.5-V supplies. All inputs are 5-V tolerant when supplied from a 2.7-V or 3.3-V supply.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7420FCC	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

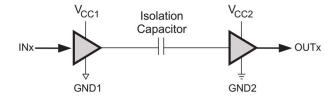




Table of Contents

1	Features 1	7	Parameter Measurement Information	10
2	Applications 1	8	Detailed Description	<mark>1</mark> 1
3	Description 1		8.1 Overview	11
4	Revision History2		8.2 Functional Block Diagram	11
5	Pin Configuration and Functions3		8.3 Feature Description	12
6	Specifications		8.4 Device Functional Modes	15
•	6.1 Absolute Maximum Ratings	9	Application and Implementation	16
	6.2 ESD Ratings		9.1 Application Information	16
	6.3 Recommended Operating Conditions		9.2 Typical Application	16
	6.4 Thermal Information	10	Power Supply Recommendations	19
	6.5 Electrical Characteristics: V _{CC1} and V _{CC2} = 5 V ±	11	Layout	
	10%5		11.1 Layout Guidelines	
	6.6 Electrical Characteristics: V_{CC1} and V_{CC2} = 3.3 V ±		11.2 Layout Example	19
	10%5	12	Device and Documentation Support	
	6.7 Electrical Characteristics: V _{CC1} and V _{CC2} = 2.7 V 6		12.1 Documentation Support	
	6.8 Power Dissipation Characteristics 6		12.2 Community Resources	
	6.9 Switching Characteristics: V_{CC1} and $V_{CC2} = 5 \text{ V} \pm \frac{100}{3}$		12.3 Trademarks	
	10%		12.4 Electrostatic Discharge Caution	20
	6.10 Switching Characteristics: V _{CC1} and V _{CC2} = 3.3 V ± 10%		12.5 Glossary	
	6.11 Switching Characteristics: V_{CC1} and $V_{CC2} = 2.7 \text{ V} \cdot 7$	13	Mechanical, Packaging, and Orderable	
	6.12 Typical Characteristics		Information	<mark>2</mark> 0

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2014) to Revision C

Page

•	Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional
	Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section
•	VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
•	Changed VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
•	Changed Note 1 Figure 12
•	Changed Figure 13

Changes from Revision A (July 2013) to Revision B

Page

	· ·	
•	Changed the V _{IH} MAX value From: V _{CC} To: 5.5V in the RECOMMENDED OPERATING CONDITIONS table	4
•	Changed the V _{PR} and V _{IOTM} parameter From: DIN EN 60747-5-2 To: DIN EN 60747-5-5 in the INSULATION CHARACTERISTICS table	13
•	Changed the REGULATORY INFORMATION table	13
•	Changed the title of Figure 16 From: A ₁₀ Thermal Denating Curve per DIN FN 60747-5-2 To: A ₁₀ Thermal Denating	

Changes from Original (June 2013) to Revision A

Changed High-level output voltage MIN Value From: V_{CCx} To: V_{CC2} 5

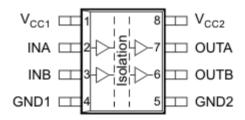
Submit Documentation Feedback

Copyright © 2013-2015, Texas Instruments Incorporated



5 Pin Configuration and Functions





Pin Functions

	PIN	1/0	DECORIDATION	
NAME	NO.	I/O	DESCRIPTION	
GND1	4	_	Ground connection for V _{CC1}	
GND2	5	_	Ground connection for V _{CC2}	
INA	2	I	Input, channel A	
INB	3	I	Input, channel B	
OUTA	7	0	Output, channel A	
OUTB	6	0	Output, channel B	
V _{CC1}	1	_	Power supply, V _{CC1}	
V _{CC2}	8	_	Power supply, V _{CC2}	

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
V _{CC1} , V _{CC2}	Supply voltage (2)	-0.5	6	٧
V_{IO}	Voltage at INx, OUTx	-0.5	$V_{CC} + 0.5^{(3)}$	٧
Io	Output current	-15	15	mA
$T_{J(Max)}$	Maximum junction temperature		150	٥°
T _{stg}	Storage temperature	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2013–2015, Texas Instruments Incorporated

Submit Documentation Feedback

⁽³⁾ Maximum voltage must not exceed 6 V.



6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC1} , V _{CC2}	Supply voltage		2.7		5.5	V
	High-level output current (V _{C0}	₂ ≥ 3 V)	-4			mA
I _{OH}	High-level output current (V _{C0}	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	mA			
I _{OL}	Low-level output current	Low-level output current			4	mA
V _{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		0		8.0	V
		≥ 4.5-V Operation	20			
t _{ui}	input pulse duration	< 4.5-V Operation	25			ns
4 / 4	Cincoline rate	≥ 4.5-V Operation	0		50	Mbps
1 / t _{ui}	Signaling rate	< 4.5-V Operation	0		40	
T _J ⁽¹⁾	Junction temperature		-40		136	°C
T _A	Ambient temperature		-40	25	125	°C

⁽¹⁾ To maintain the recommended operating conditions for T_J , see the *Power Dissipation Characteristics* table.

6.4 Thermal Information

		ISO7420FCC	
	THERMAL METRIC ⁽¹⁾	D (SOIC) 8 PINS 115.1 60.1 56.4 17.2	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	17.2	°C/W
ΨЈВ	Junction-to-board characterization parameter	55.8	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

Submit Documentation Feedback

Copyright © 2013–2015, Texas Instruments Incorporated



6.5 Electrical Characteristics: V_{CC1} and V_{CC2} = 5 V ± 10%

 $T_{\Delta} = -40^{\circ}\text{C}$ to 125°C

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		$I_{OH} = -4 \text{ mA}$; se	e Figure 12.	V _{CC2} - 0.5	4.8		
V _{OH}	High-level output voltage	$I_{OH} = -20 \mu A$; se	ee Figure 12.	V _{CC2} - 0.1	5	0.4 0.1 10 1.1 4.6 1.5 6 2.5 8.5	V
		I _{OL} = 4 mA; see	Figure 12.		0.2	0.4	
V_{OL}	Low-level output voltage	TEST CONDITIONS $I_{OH} = -4 \text{ mA; see Figure 12.}$ $I_{OH} = -20 \text{ µA; see Figure 12.}$ $I_{OL} = 4 \text{ mA; see Figure 12.}$ $I_{OL} = 20 \text{ µA; see Figure 12.}$ $INX = V_{CC1}$ $INX = 0 \text{ V}$ $V_1 = V_{CC1} \text{ or 0 V; see Figure 14.}$ $DC \text{ to 1 Mbps}$ $DC \text{ Input: } V_1 = V_{CC1} \text{ or 0 V,}$ $AC \text{ Input: } C_L = 15 \text{pF}$		0	0.1	V	
$V_{I(HYS)}$	Input threshold voltage hysteresis				450		mV
I _{IH}	High-level input current	INx = V _{CC1}				10	μA
I _{IL}	Low-level input current	INx = 0 V		-10			μA
CMTI	Common-mode transient immunity	V _I = V _{CC1} or 0 V	; see Figure 14.	25	60		kV/μs
SUPPL	Y CURRENT (ALL INPUTS SWITCHING	WITH SQUARE WA	AVE CLOCK SIGNAL FOR DYNAMIC	C ICC MEASUREMENT)		
I _{CC1}		DO to 4 Mb	DC Input: $V_1 = V_{CC1}$ or 0 V,		0.5	1.1	
I _{CC2}		DC to 1 Mbps			3	4.6	
I _{CC1}		40.14			1	1.5	
I _{CC2}		10 Mbps			4	6	
I _{CC1}	Supply current for V _{CC1} and V _{CC2}	05.14	0 45 5		1.7	2.5	mA
I _{CC2}		25 Mbps	$C_L = 15pF$		6	8.5	
I _{CC1}		50.14	1		2.7	4	
I _{CC2}		50 Mbps			8.5	12	

6.6 Electrical Characteristics: V_{CC1} and V_{CC2} = 3.3 V ± 10%

 $T_{\Lambda} = -40^{\circ}\text{C}$ to 125°C

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V	High level systems with an	$I_{OH} = -4 \text{ mA}$; see	e Figure 12.	V _{CC2} - 0.5	3		
V _{OH}	High-level output voltage	$I_{OH} = -20 \mu A$; se	ee Figure 12.	V _{CC2} - 0.1	3.3	0.4 0.1 10 0.8 3.3 1.2 4.5 2 6.1 2.3	V
.,		I _{OL} = 4 mA; see	Figure 12.		0.2	0.4	
V_{OL}	Low-level output voltage	$I_{OL} = 20 \mu A$; see	$_{H}$ = -4 mA; see Figure 12. $_{H}$ = -20 μ A; see Figure 12. $_{L}$ = 4 mA; see Figure 12. $_{L}$ = 20 μ A; see Figure 12.		0	0.1	V
V _{I(HYS)}	Input threshold voltage hysteresis				425		mV
I _{IH}	High-level input current	INx = V _{CC1}				10	μA
I _{IL}	Low-level input curre	INx = 0 V		-10			μA
CMTI	Common-mode transient immunity	V _I = V _{CC1} or 0 V	; see Figure 14.	25	40		kV/µs
SUPPL	Y CURRENT (ALL INPUTS SWITCHING	WITH SQUARE V	WAVE CLOCK SIGNAL FOR DYNAMI	C I _{CC} MEASUREMENT)		'	
I _{CC1}		20	DC Input: $V_1 = V_{CC1}$ or 0 V.		0.3	8.0	
I _{CC2}		DC to 1 Mbps			2.4	3.3	
I _{CC1}	1	40.14			0.6	1.2	
I _{CC2}		10 Mbps			3.1	4.5	
I _{CC1}	Supply current for V _{CC1} and V _{CC2}	05.14			1	2	mA
I _{CC2}	1	25 Mbps	G _L = 15pF		4.2	6.1	
I _{CC1}	7	40.14			1.3	2.3	
I _{CC2}	1	40 Mbps			5.3	7.5	



6.7 Electrical Characteristics: V_{CC1} and $V_{CC2} = 2.7 \text{ V}$

 $T_{\Delta} = -40^{\circ}\text{C}$ to 125°C

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
.,	18.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	$I_{OH} = -2 \text{ mA}$; see	e Figure 12.	V _{CC2} - 0.3	2.5		
V _{OH}	High-level output voltage	$I_{OH} = -20 \mu A$; se	e Figure 12.	V _{CC2} - 0.1	2.7	0.4 0.1 10 0.4 3.1 0.7 4 1.2 5	V
.,		I _{OL} = 4 mA; see	Figure 12.		0.2	0.4	.,
V_{OL}	Low-level output voltage	I _{OL} = 20 μA; see	Figure 12.		0	0.1	V
V _{I(HYS)}	Input threshold voltage hysteresis				350		mV
I _{IH}	High-level input current	INx = V _{CC1}				10	μA
I _{IL}	Low-level input current	INx = 0 V		-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CC1}$ or 0 V	; see Figure 14.	25	35		kV/μs
SUPPL	Y CURRENT (ALL INPUTS SWITCHING	WITH SQUARE V	WAVE CLOCK SIGNAL FOR DYNAMI	C I _{CC} MEASUREMENT)		'	
I _{CC1}		20	DC Input: $V_I = V_{CC1}$ or 0 V,		0.15	0.4	
I _{CC2}	1	DC to 1 Mbps	AC Input: C _L = 15pF		2.1	3.1	
I _{CC1}		40.14			0.4	0.7	
I _{CC2}	1	10 Mbps			2.7	4	
I _{CC1}	Supply current for V _{CC1} and V _{CC2}				0.7	1.2	mA
I _{CC2}	1	25 Mbps	$C_L = 15pF$		3.6	5	
I _{CC1}	7	40.14			1	1.7	
I _{CC2}	1	40 Mbps			4.4	6.3	

6.8 Power Dissipation Characteristics

	THERMAL METRIC			
P _D	Device power dissipation	$V_{\rm CC1} = V_{\rm CC2} = 5.5 \text{ V}, T_{\rm J} = 150 ^{\circ}\text{C}, C_{\rm L} = 15 \text{ pF},$ Input a 50-Mbps 50% duty-cycle square wave	120	mW

Product Folder Links: ISO7420FCC



6.9 Switching Characteristics: V_{CC1} and $V_{CC2} = 5 \text{ V} \pm 10\%$

 $T_A = -40$ °C to 125°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	H, t _{PHL} Propagation delay time				37	ns
PWD ⁽¹⁾	Pulse width distortion t _{PHL} - t _{PLH}	See Figure 12.		2.5	5	ns
t _{sk(o)} (2)	Channel-to-channel output skew time				2	ns
t _{sk(pp)} (3)	Part-to-part skew time				12	ns
t _r	Output signal rise time	See Figure 40		2.5		ns
t _f	Output signal fall time	See Figure 12.		2.5		ns
t _{GS}	Pulse width of glitches suppressed by the input filter			12		ns
t _{fs}	Fail-safe output delay time from input data or power loss	See Figure 13.		8		μs

⁽¹⁾ Also known as pulse skew.

6.10 Switching Characteristics: V_{CC1} and V_{CC2} = 3.3 V ± 10%

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay time	Can Figure 40	10	22	40	ns
PWD ⁽¹⁾	Pulse width distortion t _{PHL} - t _{PLH}	See Figure 12.			3	ns
t _{sk(o)} (2)	Channel-to-channel output skew time				2	ns
t _{sk(pp)} (3)	Part-to-part skew time				19	ns
t _r	Output signal rise time	See Figure 12.		3		ns
t _f	Output signal fall time			3		ns
t _{GS}	Pulse width of glithes suppressed by the input filter			12.5		ns
t _{fs}	Fail-safe output delay time from input power loss	See Figure 13.		8		μs

⁽¹⁾ Also known as pulse skew.

6.11 Switching Characteristics: V_{CC1} and $V_{CC2} = 2.7 \text{ V}$

 $T_A = -40$ °C to 125°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay time	See Figure 42	15	26	45	ns
PWD ⁽¹⁾	Pulse width distortion t _{PHL} - t _{PLH}	See Figure 12.			3	ns
t _{sk(o)} (2)	Channel-to-channel output skew time				2	ns
t _{sk(pp)} (3)	Part-to-part skew time				22	ns
t _r	Output signal rise time	See Figure 42		3		ns
t _f	Output signal fall time	See Figure 12.		3		ns
t _{GS}	Pulse width of glitches suppressed by the input filter			13.5		ns
t _{fs}	Fail-safe output delay time from input power loss	See Figure 13.		8		μs

⁽¹⁾ Also known as pulse skew.

Product Folder Links: ISO7420FCC

⁽²⁾ t_{sk(o)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

⁽³⁾ t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

t_{sk(o)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

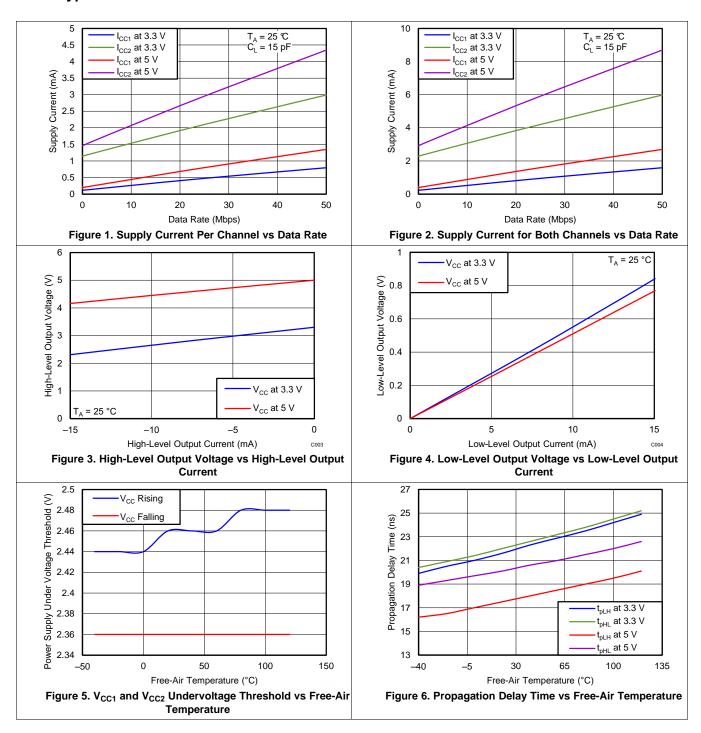
⁽³⁾ t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

⁽²⁾ t_{sk(o)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

⁽³⁾ t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

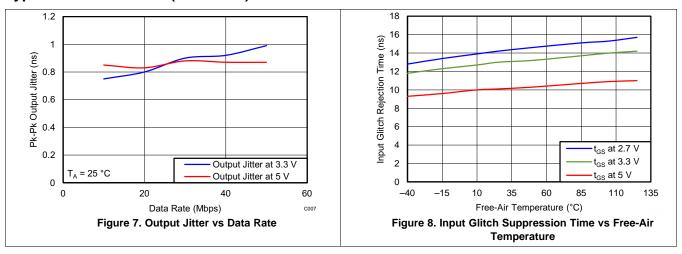


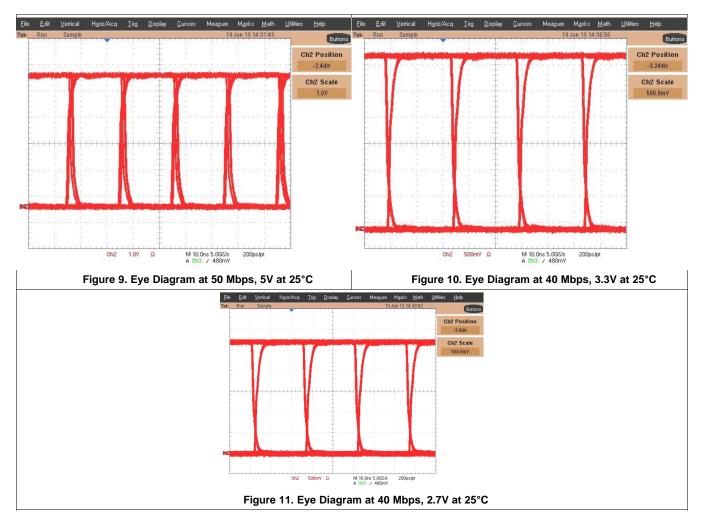
6.12 Typical Characteristics





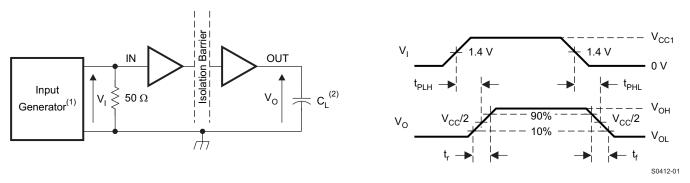
Typical Characteristics (continued)





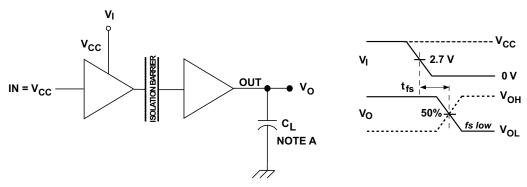
TEXAS INSTRUMENTS

7 Parameter Measurement Information



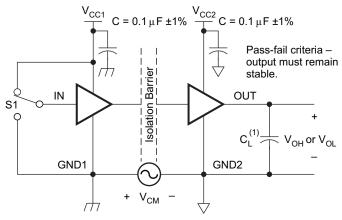
- (1) The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O =$ 50 Ω . At the input, a 50- Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.
- (2) $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 12. Switching Characteristic Test Circuit and Voltage Waveforms



A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 13. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 14. Common-Mode Transient Immunity Test Circuit

Product Folder Links: ISO7420FCC

10



8 Detailed Description

8.1 Overview

The isolator in Figure 15 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 50 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

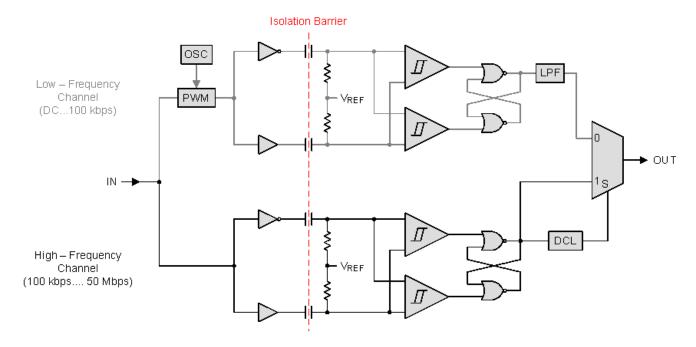


Figure 15. Conceptual Block Diagram of a Digital Capacitive Isolator

Copyright © 2013–2015, Texas Instruments Incorporated



8.3 Feature Description

8.3.1 Insulation and Safety-Related Specifications for SOIC-8 Package

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4			mm
L(102)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4			mm
СТІ	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.014			mm
5	Isolation resistance, input to	V _{IO} = 500 V, T _A = 25°C		>10 ¹²		Ω
R _{IO}	output ⁽¹⁾	V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C		>10 ¹¹		Ω
C _{IO}	Barrier capacitance, input to output ⁽¹⁾	V _{IO} = 0.4 sin (2πft), f = 1 MHz		1		pF
C _I	Input capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \sin(2\pi ft), f = 1 \text{ MHz}, V_{CC} = 5 \text{ V}$		1		pF

⁽¹⁾ All pins on each side of the barrier tied together creating a two-terminal device.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

Product Folder Links: /SO7420FCC

⁽²⁾ Measured from input pin to ground.



8.3.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	SPECIFICATION	UNIT
DIN V VI	DE V 0884-10 (VDE V 0884-10):2006-12 ⁽¹⁾			
V_{IORM}	Maximum working isolation voltage		566	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, $t = 10$ s, Partial Discharge < 5 pC	906	
V_{PR}	Input-to-output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% Production test) Partial discharge < 5 pC	1062	V _{PK}
		After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, $t = 10$ s, Partial discharge < 5 pC	680	
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} t = 60 sec (qualification) t= 1 sec (100% production)	4242	V _{PK}
R _S	Isolation resistance	V _{IO} = 500 V at T _S = 150°C	>10 ⁹	Ω
	Pollution degree		2	
UL 1577				•
V _{ISO}	Isolation voltage	$\begin{array}{c} V_{TEST}=V_{ISO}=2500~V_{RMS},~t=60~sec~(qualification)\\ V_{TEST}=1.2~x~V_{ISO}=3000~V_{RMS},~t=1~sec~(100\%\\ production) \end{array}$	2500	V _{RMS}

⁽¹⁾ Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

	_	
PARAMETER TEST CONDITIONS		SPECIFICATION
Material group		II
Installation plansification	Rated mains voltage ≤ 150 V _{RMS}	I–IV
Installation classification	Rated mains voltage ≤ 300 V _{RMS}	I–III

8.3.3 Regulatory Information

VDE	CSA	UL	cqc
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950- 1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Isolation voltage, 4242 V _{PK} ; Maximum Working Isolation Voltage, 566 V _{PK}	3000 V _{RMS} Isolation Rating; 400 V _{RMS} Basic and 200 V _{RMS} Reinforced Insulation maximum working voltage per CSA 60950-1- 07+A1 and IEC 60950-1 (2nd Ed)+A1; 300 V _{RMS} Basic and 150 V _{RMS} Reinforced Insulation maximum working voltage per CSA 61010-1- 12 and IEC 61010-1 (3rd Ed)	Single Protection, 2500 V _{RMS} ⁽¹⁾	Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 250 V _{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109540

⁽¹⁾ Production tested \geq 3000 V_{RMS} for 1 second in accordance with UL 1577.

Product Folder Links: ISO7420FCC



8.3.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		$\theta_{JA} = 115.1^{\circ}\text{C/W}, \ V_I = 5.5 \ V, \ T_J = 150^{\circ}\text{C}, \ T_A = 25^{\circ}\text{C}$			197	
Is Safety input, output, or supply current	$\theta_{JA} = 115.1^{\circ}\text{C/W}, \ V_I = 3.6 \ V, \ T_J = 150^{\circ}\text{C}, \ T_A = 25^{\circ}\text{C}$			302	mA	
	Guilone	$\theta_{JA} = 115.1^{\circ}\text{C/W}, \ V_{I} = 2.7 \ \text{V}, \ T_{J} = 150^{\circ}\text{C}, \ T_{A} = 25^{\circ}\text{C}$			402	
T_S	Maximum Safety temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

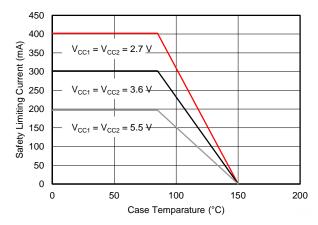


Figure 16. θ_{JC} Thermal Derating Curve per VDE

Submit Documentation Feedback



8.4 Device Functional Modes

Table 2. Function Table⁽¹⁾

V _{CC1}	V _{CC2}	INPUT INA, INB	OUTPUT OUTA, OUTB
		Н	Н
PU	PU	L	L
		Open	L ⁽²⁾
PD	PU	Х	L ⁽²⁾
Х	PD	Х	Undetermined

- (1) PU = Powered up (V_{CC} ≥ 2.7 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level
 (2) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematics

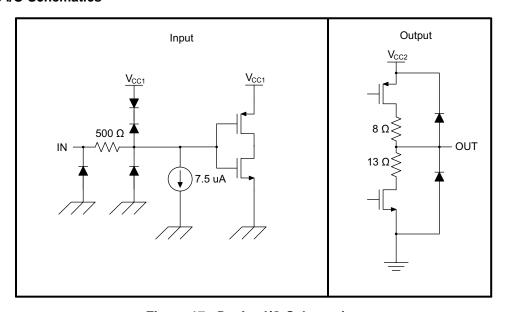


Figure 17. Device I/O Schematics

Copyright © 2013–2015, Texas Instruments Incorporated

Submit Documentation Feedback



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO7420FCC utilize single-ended TTL-logic switching technology. Its supply voltage range is from 2.7 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (i.e. μ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

ISO7420FCC can be used to isolate power MOSFETs from sensitive logic circuitry in Switch Mode Power Supplies (SMPS) as shown in Figure 18. Low default output of ISO7420FCC is critical for proper operation of power MOSFETs in such applications.

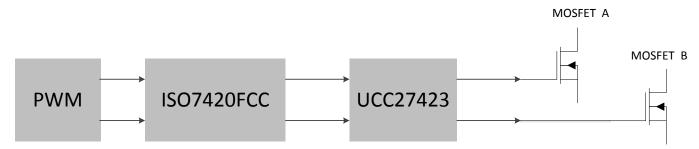


Figure 18. Isolated Switch Mode Power Supply

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7420FCC only requires two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

9.2.2.1 Supply Current Equations

9.2.2.1.1 Maximum Supply Current Equations

(Calculated over recommended operating temperature range and Silicon process variation).

At
$$V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$$
:

$$I_{CC1}(max) = 1.1 + 5.80E-02 \times f$$
 (1)

$$I_{CC2}(max) = 4.6 + 6.55E-02 \times f + 5.5E-03 \times f \times C_{L}$$
(2)

At $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$:

$$I_{CC1}(max) = 0.8 + 3.40E-02 \times f$$
 (3)

$$I_{CC2}(max) = 3.3 + 4.60E-02 \times f + 3.6E-03 \times f \times C_L$$
 (4)

At $V_{CC1} = V_{CC2} = 2.7 \text{ V}$:

$$I_{CC1}(max) = 0.4 + 3.20E-02 \times f$$
 (5)

$$I_{CC2}(max) = 3.1 + 3.75E-02 \times f + 2.7E-03 \times f \times C_{L}$$
(6)

Product Folder Links: ISO7420FCC



Typical Application (continued)

f is data rate of each channel measured in Mbps; C_L is the capacitive load of each channel measured in pF; I_{CC1} (maximum) and I_{CC2} (max) are measured in mA.

9.2.2.1.2 Typical Supply Current Equations

(Calculated for $T_A = 25$ °C and nominal Silicon process material).

At
$$V_{CC1} = V_{CC2} = 5 \text{ V}$$
:

$$I_{CC1}(typical) = 0.5 + 4.40E-02 \times f$$
 (7)

$$I_{CC2}(typical) = 3 + 3.50E-02 \times f + 5.0E-03 \times f \times C_L$$
 (8)

At $V_{CC1} = V_{CC2} = 3.3 \text{ V}$:

$$I_{CC1}(typical) = 0.3 + 2.60E-02 \times f$$
 (9)

$$I_{CC2}(typical) = 2.4 + 2.25E-02 \times f + 3.3E-03 \times f \times C_1$$
 (10)

At $V_{CC1} = V_{CC2} = 2.7 \text{ V}$:

$$I_{CC1}(typical) = 0.15 + 2.10E-02 \times f$$
 (11)

$$I_{CC2}(typical) = 2.1 + 1.75E-02 \times f + 2.7E-03 \times f \times C_L$$
 (12)

f is Data Rate of each channel measured in Mbps; C_L is the Capacitive Load of each channel measured in pF; $I_{CC1}(typ)$ and $I_{CC2}(typ)$ are measured in mA.

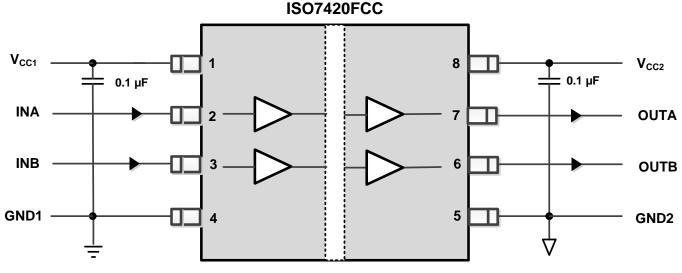


Figure 19. ISO7420FCC Typical Circuit Hook-Up



Typical Application (continued)

9.2.3 Application Curves

Figure 20 shows the INA input on Channel 1 and OUTA output on Channel 2 of an oscilloscope.

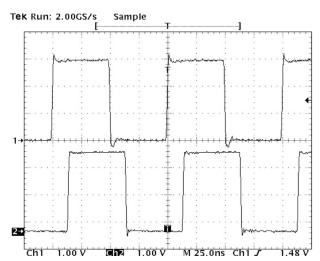


Figure 20. Typical Input and Output Waveforms



10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 μ F bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 21). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links
 usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note Digital Isolator Design Guide, SLLA284.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

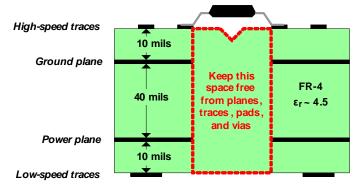


Figure 21. Recommended Layer Stack

Copyright © 2013–2015, Texas Instruments Incorporated

Submit Documentation Feedback



12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- SN6501 Transformer Driver for Isolated Power Supplies (SLLSEA0)
- LVDS Application and Data Handbook (SLLD009)
- Digital Isolator Design Guide (SLLA284)
- Isolation Glossary (SLLA353)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community T's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

DeviceNet, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

0 Submit Documentation Feedback

10-Nov-2025

www.ti.com

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
ISO7420FCCD	Active	Production	SOIC (D) 8	75 TUBE	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCD.B	Active	Production	SOIC (D) 8	75 TUBE	-	Call TI	Call TI	-40 to 125	
ISO7420FCCDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 18-Jul-2025

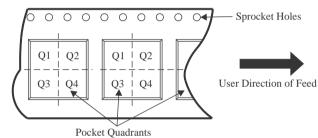
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7420FCCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 18-Jul-2025



*All dimensions are nominal

	Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
Г	ISO7420FCCDR	SOIC	D	8	2500	350.0	350.0	43.0	

PACKAGE MATERIALS INFORMATION

www.ti.com 18-Jul-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7420FCCD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7420FCCD.A	D	SOIC	8	75	505.46	6.76	3810	4



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025