INA597 High-Precision, Wide-Bandwidth e-trim™ Difference Amplifier

1 Features

- Low offset voltage: 200 µV (maximum)
- Low offset voltage drift: ±5 µV/°C (maximum)
- Low noise: 18 nV/√Hz at 1 kHz
- Low gain error: ±0.03% (maximum)
- High common-mode rejection: 88 dB (minimum)
- Wide bandwidth: 2-MHz GBW
- Low quiescent current: 1.1 mA per amplifier
- High slew rate: 18 V/µs
- High capacitive load drive capability: 500 pF
- Wide supply range:
  - Single-supply: 4.5 V to 36 V
  - Dual-supply: ±2.25 V to ±18 V
- Specified temperature range: –40°C to +125°C
- Packages: 8-pin SOIC and VSSOP, 10-pin VSON

2 Applications

- Data acquisition (DAQ)
- Sensor modules and tags for asset tracking
- Flow transmitter
- Optical module
- Power supply module
- AC drive position feedback
- Servo drive position feedback
- Voltage conditioning module

3 Description

The INA597 is a low-power, wide-bandwidth, difference amplifier for cost-sensitive applications. The INA597 consists of a precision operational amplifier (op amp) and a precision resistor network. Excellent tracking of resistors maintains gain accuracy and common-mode rejection over temperature. Unique features such as low offset (200 µV, maximum), low offset drift (5 µV/°C maximum) high slew rate (18 V/µs), and high capacitive load drive of up to 500 pF make the INA597 a robust, high-performance difference amplifier for high-voltage industrial applications.

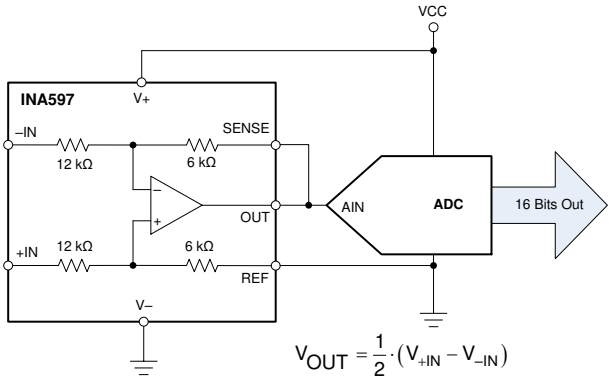
The common-mode range of the internal op amp extends to the negative supply, and enables the device to operate in single-supply applications. The device operates on single (4.5 V to 36 V) or dual supplies (±2.25 V to ±18 V).

The difference amplifier is the foundation of many commonly used circuits. The INA597 provides this circuit function without using an expensive precision resistor network.

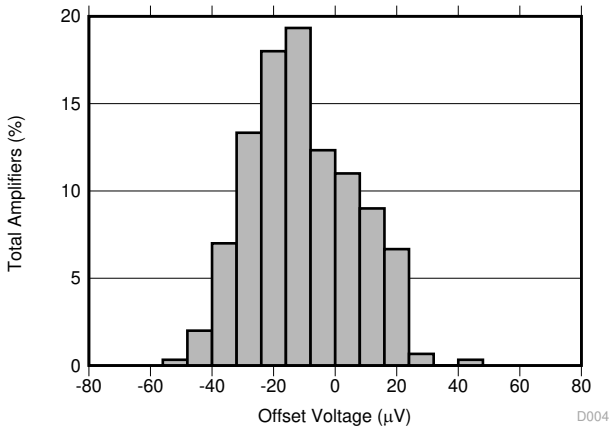
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
INA597	SOIC (8)	4.90 mm × 3.91 mm
	VSON (10)	3.00 mm × 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Differential Input Data Acquisition



Typical Distribution of Offset Voltage (RTO)
G = 1/2, V_S = ±18 V

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2021) to Revision B (April 2021)	Page
• Added DRC package and associated content	1

Changes from Revision * (August 2019) to Revision A (February 2021)	Page
• Added D package and associated content	1
• Added input current (max) to *Absolute Maximum Ratings*	4
• Deleted input voltage (max) from *Absolute Maximum Ratings*	4
• Changed common-mode voltage (min and max) in *Electrical Characteristics*	4
• Added input impedance specifications to *Electrical Characteristics*	4
• Changed Fig. 6-39, *Positive Output Voltage vs Output Current (sourcing) G = ½*, Y-axis unit from µV to V	7

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION
INA597	Cost-effective, wide-bandwidth e-trim™ difference amplifier	G = 0.5 V/V or 2 V/V
INA592	High-precision, wide-bandwidth e-trim™ difference amplifier	G = 0.5 V/V or 2 V/V
INA159	High-speed, precision, gain of 0.2 level translation difference amplifier	G = 0.2 V/V
INA137	Audio differential line receiver ±6 dB (G = 1/2 or 2)	G = 0.5 V/V or 2 V/V
INA132	Low-power, single-supply difference amplifier	G = 1 V/V
INA819	35-µV offset, 0.4 µV/°C V_{OS} drift, 8-nV/$\sqrt{Hz}$ noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG
INA821	35-µV offset, 0.4 µV/°C V_{OS} drift, 7-nV/$\sqrt{Hz}$ noise, high-bandwidth, precision instrumentation amplifier	G = 1 + 49.4 kΩ / RG
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA	G = 1 + 100 kΩ / RG
PGA280	20-mV to ±10-V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ±18 V	Digital programmable
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable

6 Pin Configuration and Functions

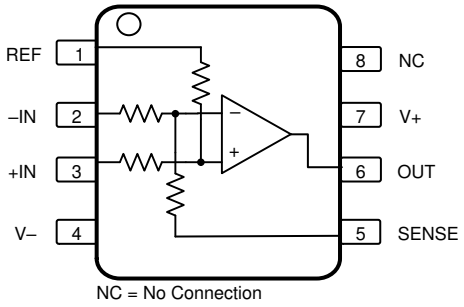

Figure 6-1. D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

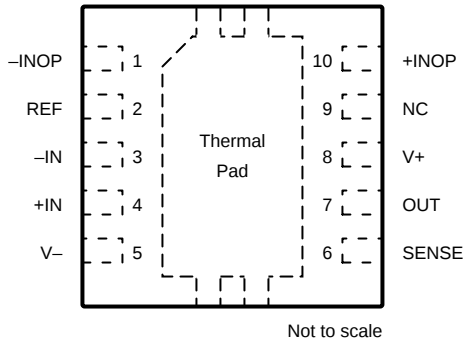

Figure 6-2. DRC (10-Pin VSON With Thermal Pad) Package, Top View

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	D (SOIC), DGK (VSSOP)	DRC (VSON)		
+IN	3	4	I	12-kΩ resistor to noninverting terminal of op amp. Used as positive input in G = ½ configuration. Used as reference pin in G = 2 configuration.
–IN	2	3	I	12-kΩ resistor to inverting terminal of op amp. Used as negative input in G = ½ configuration. Connect to output in G = 2 configuration.
+INOP	—	10	I	Direct connection to noninverting terminal of op amp
–INOP	—	1	I	Direct connection to inverting terminal of op amp
NC	8	9	—	No internal connection (can be left floating)
OUT	6	7	O	Output
REF	1	2	I	6-kΩ resistor to noninverting terminal of op amp. Used as reference pin in G = ½ configuration. Used as positive input in G = 2 configuration.
SENSE	5	6	I	6-kΩ resistor to inverting terminal of op amp. Connect to output in G = ½ configuration. Used as negative input in G = 2 configuration.
V+	7	8	—	Positive (highest) power supply
V–	4	5	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V±	Single supply, (V+) to (V–)		36	V
	Dual supply, (V+) – (V–)		±18	V
I_{IN}	Input current		10	mA
I_S	Output short circuit (to ground)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature	–55	125	°C
T_{stg}	Storage temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Section 7.3*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V±	Supply voltage	Single supply, V_S = (V+) to (V–)	4.5		36	V
		Dual supply, V_S = (V+) – (V–)	±2.25		±18	V
T_A	Specified temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA597			UNIT
		D	DGK	DRC	
		8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158	115	47.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.6	52.4	49.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	59.2	21.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	9.5	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.3	58.3	20.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: G = 1/2

at V_S = ±2.25 V to ±18 V, T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ connected to ground, and REF pin connected to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE (RTO)							
V_{OS}	Input offset voltage	G = 1/2, RTO, T_A = 25°C, V_S = ±2.25 V to ±3 V, V_{CM} = –3V			±14	±200	µV
		G = 1/2, RTO, T_A = 25°C, V_S = ±3 V to ±18 V, V_{CM} = V_S / 2			±14	±200	µV
dV_{OS}/dT	Input offset voltage drift				±0.7	±5.0	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±3 V to ±18 V			±0.5	±5	µV/V
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	V_{OUT} = 0 V		3[(V–)–0.1] –2V_{REF}		3(V+)–2V_{REF}	V
CMRR	Common-mode rejection ratio	RTO, 3 [(V–) – 0.1 V)] ≤ V_{CM} ≤ 3 [(V+) – 3 V]	T_A = 25°C	88	100		dB
			T_A = –40°C to +125°C	82	90		dB
		RTO, 3 [(V+) - 1.5 V)] ≤ V_{CM} ≤ 3 [(V+))]	T_A = 25°C	88	100		dB
			T_A = –40°C to +125°C	72	90		dB
INPUT IMPEDANCE							
z_{id}	Differential	V_O = 0 V			24		kΩ
z_{ic}	Common-mode				9		kΩ
GAIN							
G	Initial				1/2		V/V
GE	Gain error	V_{OUT} = –10 V to +10 V, V_S = ±15 V			±0.01	±0.03	%
	Gain error drift(1)				±0.2	±0.5	ppm/°C
	Gain nonlinearity	V_{OUT} = –10 V to +10 V, V_S = ±15 V			1		ppm
OUTPUT							
V_O	Output voltage swing	Positive rail			170	220	mV
		Negative rail			190	220	mV
I_{SC}	Short-circuit current				±65		mA
NOISE							
V_n	Output voltage noise	f = 0.1 Hz to 10 Hz, RTO			3		µVpp
	Output voltage noise density	f = 1 kHz, RTO			18		nV/√Hz
FREQUENCY RESPONSE							
GBW	Small signal bandwidth	Amplitude = –3 dB			2.0		MHz
SR	Slew rate				18		V/µs
t_S	Settling time	To 0.1%	V_{OUT} = 10-V step		1		µs
		To 0.01%	V_{OUT} = 10-V step		1.3		µs
THD+N	Total harmonic distortion + noise	f = 1 kHz, V_{OUT} = 2.8 V_{RMS}			0.00038		%
	Noise floor, RTO	80-kHz bandwidth, V_{OUT} = 3.5 V_{RMS}			–116		dB
t_{DR}	Overload recovery time				200		ns

7.5 Electrical Characteristics: G = 1/2 (continued)

at V_S = ±2.25 V to ±18 V, T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ connected to ground, and REF pin connected to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_Q	Quiescent current	I_{OUT} = 0 mA	T_A = 25°C		1.1	1.2	mA
			T_A = –40°C to +125°C			1.5	mA

(1) Specified by wafer test to 95% confidence level.

7.6 Electrical Characteristics: G = 2

at V_S = ±2.25 V to ±18 V, T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ connected to ground, and REF pin connected to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE (RTO)							
V_{OS}	Input offset voltage	G = 2, RTO, T_A = 25°C, V_S = ±2.25 V to ±3 V, V_{CM} = –1.5V			±28	±400	µV
		G = 2, RTO, T_A = 25°C, V_S = ±3 V to ±18 V, V_{CM} = V_S / 2			±28	±400	µV
dV_{OS}/dT	Input offset voltage drift				±1.4	±10	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V			±1	±5	µV/V
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	V_{OUT} = 0 V		3/2[(V–)–0.1]–0.5V_{REF}		3/2(V+)–0.5V_{REF}	V
CMRR	Common-mode rejection ratio	RTO, 1.5 [(V–) – 0.1 V)] ≤ V_{CM} ≤ 1.5 [(V+) – 3 V)]	T_A = 25°C	82	94		dB
			T_A = –40°C to +125°C	80	84		dB
		RTO, 1.5 [(V+) - 1.5 V)] ≤ V_{CM} ≤ 1.5 [(V+))]	T_A = 25°C	82	94		dB
			T_A = –40°C to +125°C	65	84		dB
INPUT IMPEDANCE							
z_{id}	Differential	V_O = 0 V			12		kΩ
z_{ic}	Common-mode				9		kΩ
GAIN							
G	Initial				2		V/V
GE	Gain error	V_{OUT} = –10 V to +10 V, V_S = ±15 V			±0.01	±0.03	%
	Gain error drift (1)				±0.25	±0.5	ppm/°C
	Gain nonlinearity	V_{OUT} = –10 V to +10 V, V_S = ±15 V			1		ppm
OUTPUT							
V_O	Output voltage swing	Positive rai			130	180	mV
		Negative rail			140	180	mV
I_{SC}	Short-circuit current				±65		mA
NOISE							
V_n	Output voltage noise	f = 0.1 Hz to 10 Hz, RTO			6		µVpp
	Output voltage noise density	f = 1 kHz, RTO			36		nV/√Hz
FREQUENCY RESPONSE							
GBW	Small signal bandwidth	Amplitude = –3 dB			0.8		MHz
SR	Slew rate				18		V/µs
t_S	Settling time	To 0.1%	V_{OUT} = 10-V step		1.0		µs
		To 0.01%	V_{OUT} = 10-V step		1.7		µs

7.6 Electrical Characteristics: G = 2 (continued)

at V_S = ±2.25 V to ±18 V, T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ connected to ground, and REF pin connected to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion + noise	f = 1 kHz, V_{OUT} = 2.8 V_{RMS}			0.00066		%
	Noise floor, RTO	80-kHz bandwidth, V_{OUT} = 3.5 V_{RMS}			–110		dB
t_{DR}	Overload recovery time				200		ns
POWER SUPPLY							
I_Q	Quiescent current	I_{OUT} = 0 mA	T_A = 25°C		1.1	1.2	mA
			T_A = –40°C to +125°C			1.5	mA

(1) Specified by wafer test to 95% confidence level.

7.7 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)

Table 7-1. Table of Graphs

DESCRIPTION	FIGURE
Typical Distribution of Offset Voltage (RTO) G= 1/2, V_S = ±2.25 V	Figure 7-1
Typical Distribution of Offset Voltage (RTO) G= 2, , V_S = ±2.25 V	Figure 7-2
Typical Distribution of Offset Voltage (RTO) G= 1/2, , V_S = ±18 V	Figure 7-3
Typical Distribution of Offset Voltage (RTO) G= 2, V_S = ±18 V	Figure 7-4
Typical Distribution of Offset Voltage Drift (RTO) G = 1/2	Figure 7-5
Typical Distribution of Offset Voltage Drift (RTO) G = 2	Figure 7-6
Output Offset Voltage vs Temperature G = 1/2	Figure 7-7
Output Offset Voltage vs Temperature G = 2	Figure 7-8
Offset Voltage vs Common-Mode Voltage G = 1/2	Figure 7-9
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PSRR vs Frequency (RTI) G = 2	Figure 7-26
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Typical Distribution of Gain Error G = 2, V_S = ±2.25 V	Figure 7-28
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Closed-Loop Gain vs Frequency G = 1/2	Figure 7-31
Closed-Loop Gain vs Frequency G = 2	Figure 7-32
Voltage Noise Spectral Density vs Frequency (RTI) G = 1/2	Figure 7-33

7.7 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)

Table 7-1. Table of Graphs (continued)

DESCRIPTION	FIGURE
Voltage Noise Spectral Density vs Frequency (RTI) G = 2	Figure 7-34
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0.1-Hz to 10-Hz RTI Voltage Noise G = 2	Figure 7-36
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Integrated Output Voltage Noise vs Noise Bandwidth G = 2	Figure 7-38
Positive Output Voltage vs Output Current (sourcing) G = 1/2	Figure 7-39
Positive Output Voltage vs Output Current (sourcing) G = 2	Figure 7-40
Negative Output Voltage vs Output Current (sinking) G = 1/2	Figure 7-41
Negative Output Voltage vs Output Current (sinking) G = 2	Figure 7-42
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Settling Time G = 2	Figure 7-44
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Input Common-Mode Voltage vs Output Voltage G = 1/2, 5-V Supply	Figure 7-69
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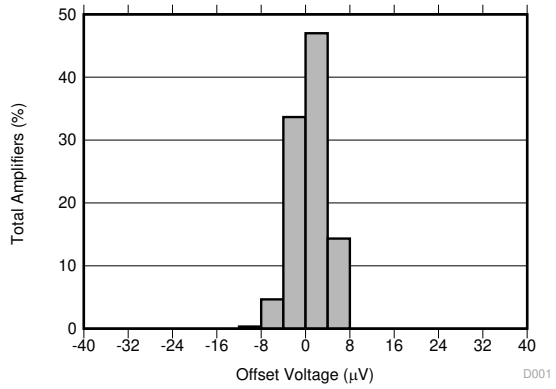
Input Common-Mode Voltage vs Output Voltage G = 1/2, 36-V Supply	Figure 7-71
Input Common-Mode Voltage vs Output Voltage G = 2, 36-V Supply	Figure 7-72
Closed-Loop Output Impedance vs Frequency	Figure 7-73

7.7 Typical Characteristics (continued)

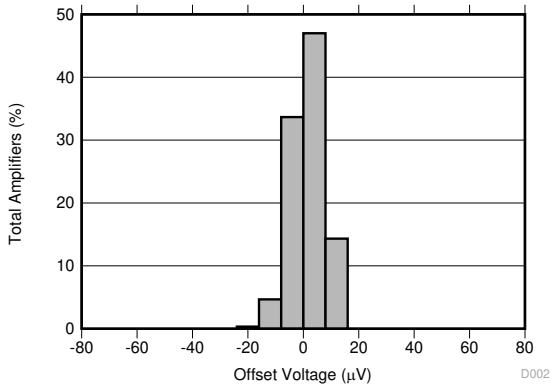
at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



N = 470 Mean = 0.82 µV Std. Dev. = 2.91 µV

G = 1/2 V_S = ±2.25 V V_{CM} = –3 V

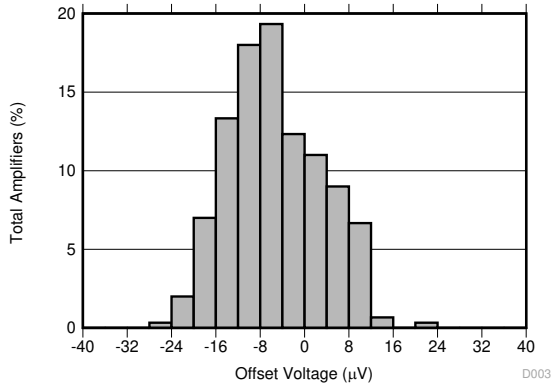
Figure 7-1. Typical Distribution of Offset Voltage (RTO)



N = 470 Mean = 1.64 µV Std. Dev. = 5.82 µV

G = 2 V_S = ±2.25 V V_{CM} = –3 V

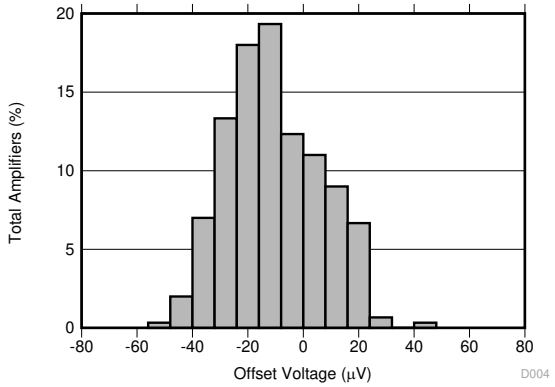
Figure 7-2. Typical Distribution of Offset Voltage (RTO)



N = 470 Mean = –5.22 µV Std. Dev. = 8.38 µV

G = 1/2

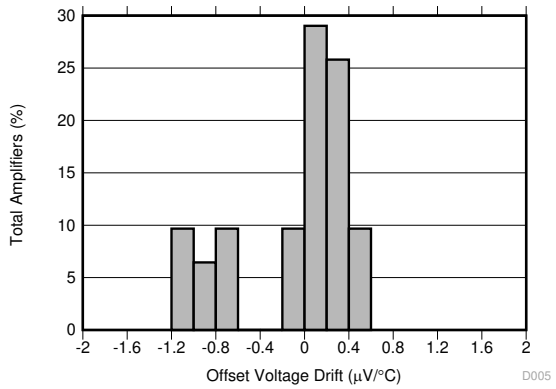
Figure 7-3. Typical Distribution of Offset Voltage (RTO)



N = 470 Mean = –10.43 µV Std. Dev. = 16.77 µV

G = 2

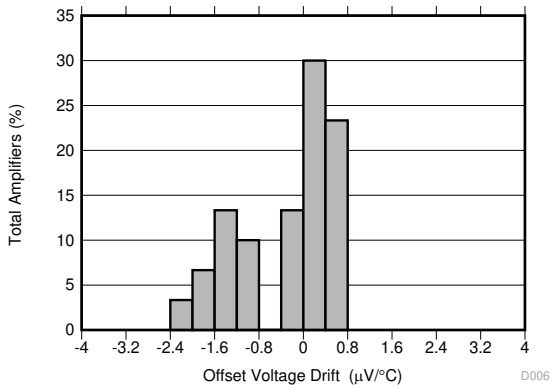
Figure 7-4. Typical Distribution of Offset Voltage (RTO)



N = 30 Mean = –0.075 µV/°C Std. Dev. = 0.502 µV/°C

G = 1/2

Figure 7-5. Typical Distribution of Offset Voltage Drift (RTO)



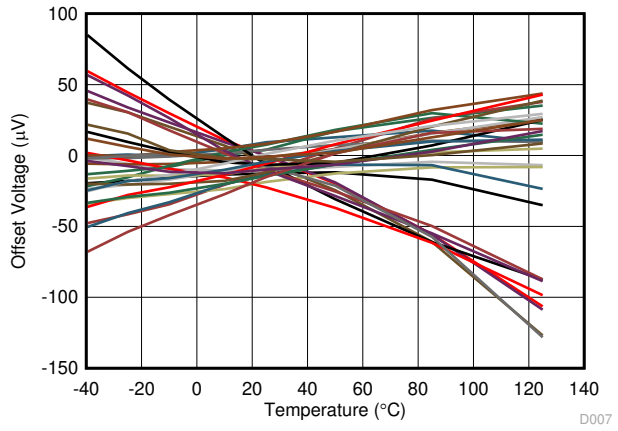
N = 30 Mean = –0.325 µV/°C Std. Dev. = 0.887 µV/°C

G = 2

Figure 7-6. Typical Distribution of Offset Voltage Drift (RTO)

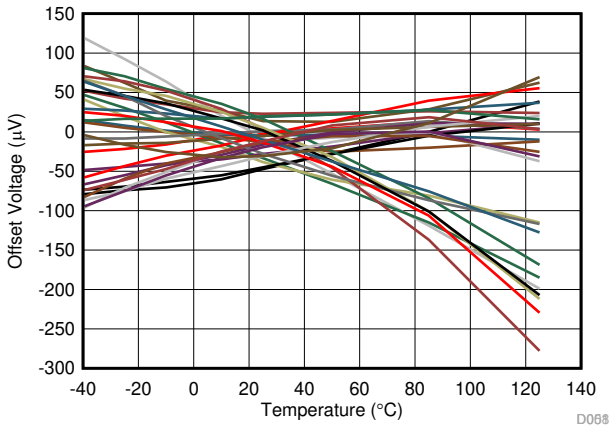
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



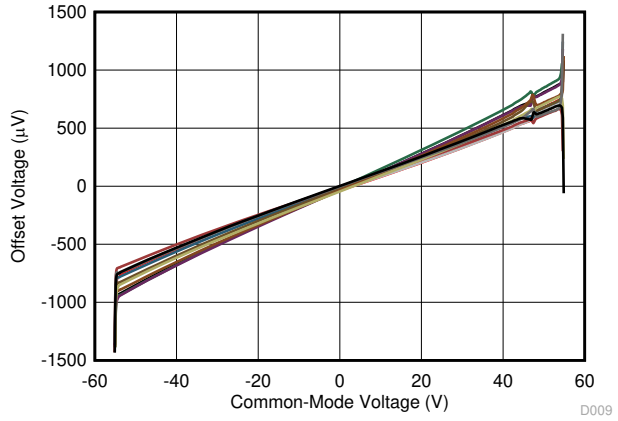
G = 1/2 30 units

Figure 7-7. Output Offset Voltage vs Temperature



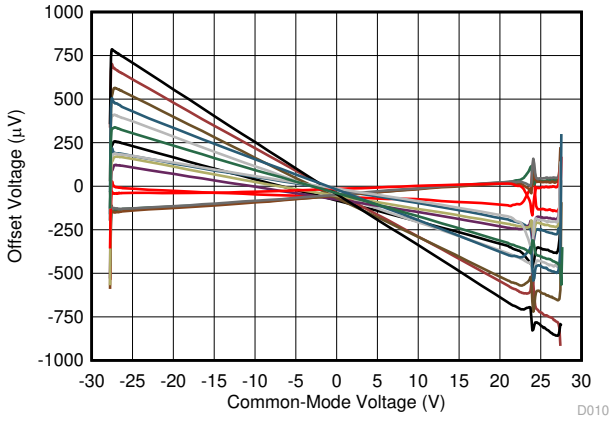
G = 2 30 units

Figure 7-8. Output Offset Voltage vs Temperature



G = 1/2 12 units

Figure 7-9. Offset Voltage vs Common-Mode Voltage



G = 2 12 units

Figure 7-10. Offset Voltage vs Common-Mode Voltage

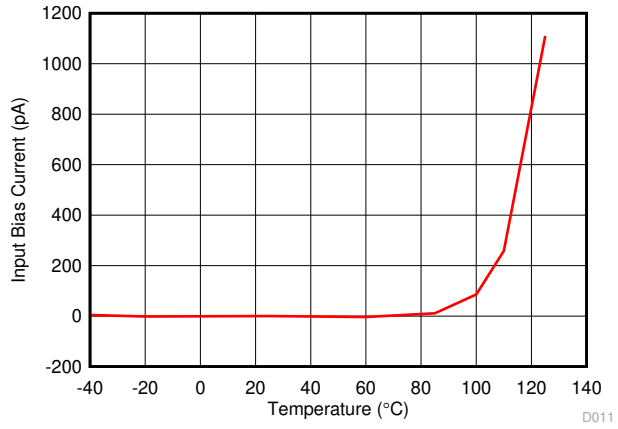


Figure 7-11. Input Bias Current vs Temperature

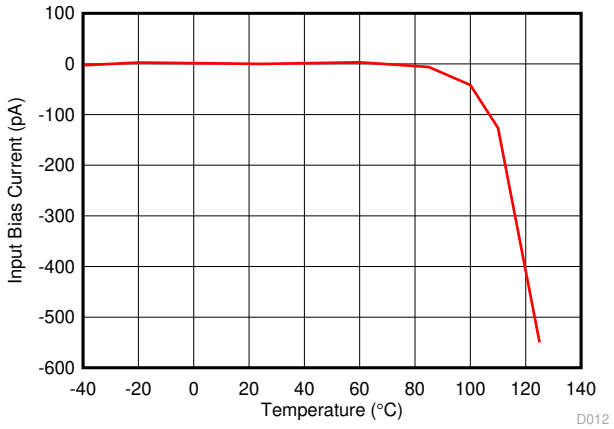
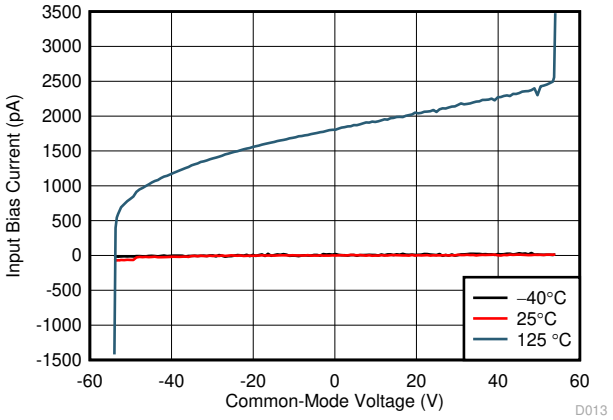


Figure 7-12. Input Offset Current vs Temperature

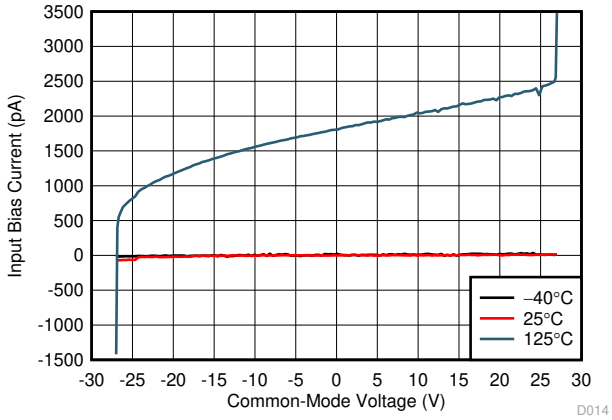
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



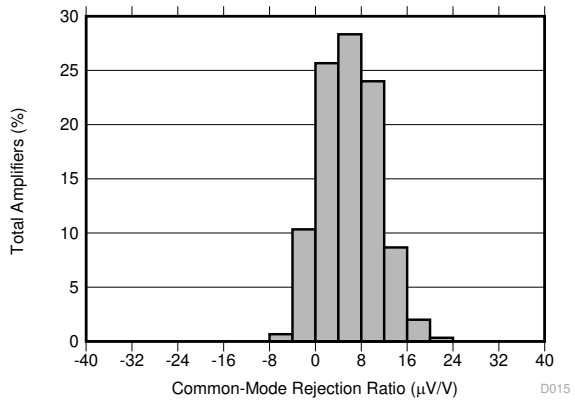
G = 1/2

Figure 7-13. Input Bias Current vs Common-Mode Voltage



G = 2

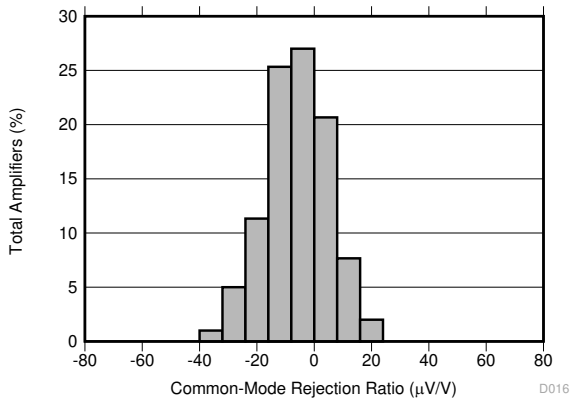
Figure 7-14. Input Bias Current vs Common-Mode Voltage



N = 470 Mean = 6.01 µV/V Std. Dev. = 4.85 µV/V

G = 1/2 V_S = ±2.25 V

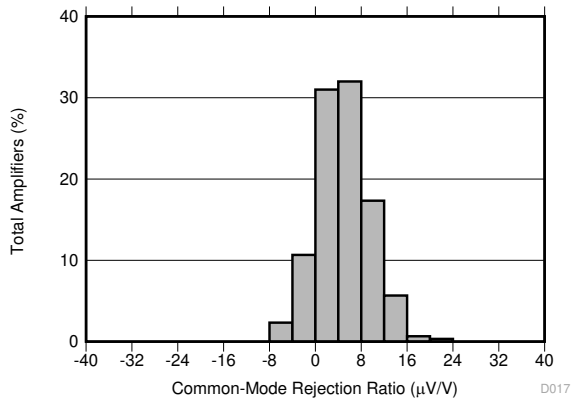
Figure 7-15. Typical CMRR Distribution



N = 470 Mean = –6.22 µV/V Std. Dev. = 10.74 µV/V

G= 2 V_S = ±2.25 V

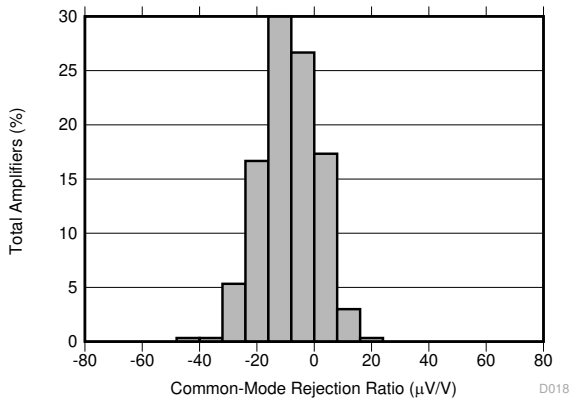
Figure 7-16. Typical CMRR Distribution



N = 470 Mean = 4.86 µV/V Std. Dev. = 4.75 µV/V

G = 1/2

Figure 7-17. Typical CMRR Distribution



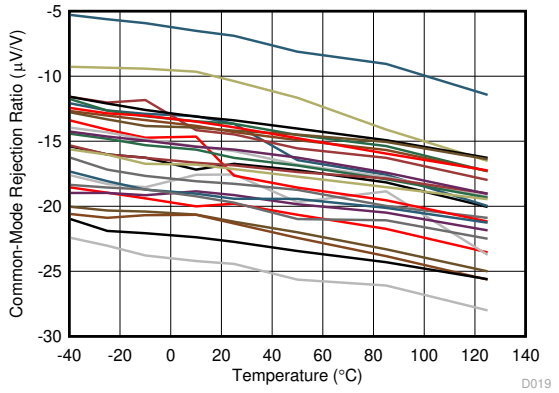
N = 470 Mean = –8.64 µV/V Std. Dev. = 9.70 µV/V

G = 2

Figure 7-18. Typical CMRR Distribution

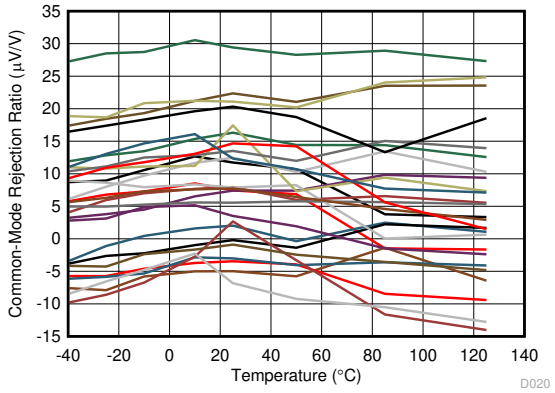
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



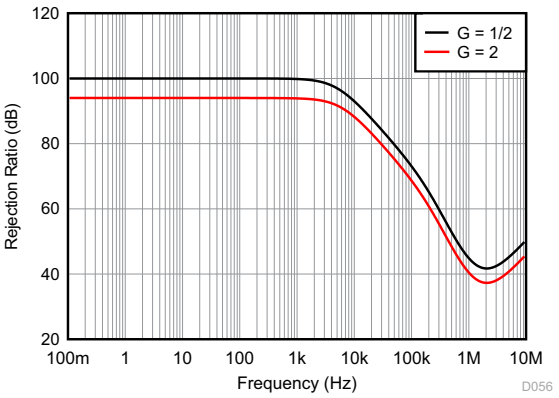
G = 1/2 24 units

Figure 7-19. CMRR vs Temperature



G = 2 24 units

Figure 7-20. CMRR vs Temperature



G = 1/2 and G = 2

Figure 7-21. Common-Mode Rejection Ratio vs Frequency, Referred-to-Input

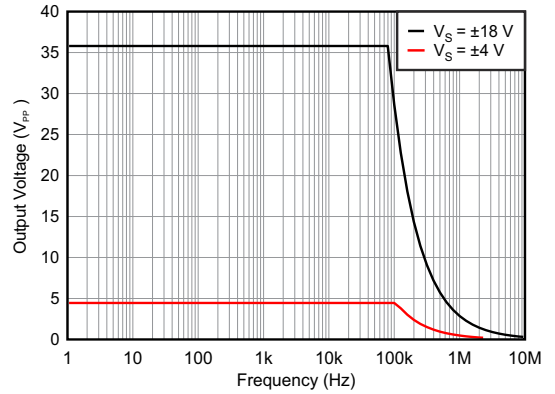
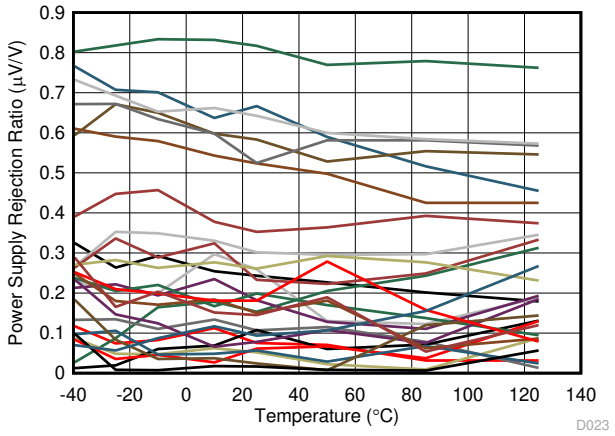
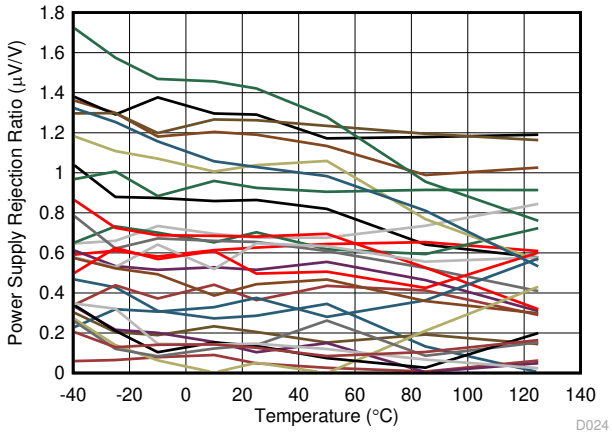


Figure 7-22. Maximum Output Voltage vs Frequency



G = 1/2 24 units

Figure 7-23. PSRR vs Temperature

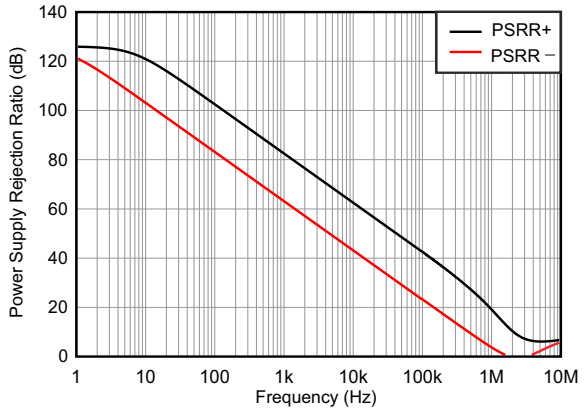


G = 2 24 units

Figure 7-24. PSRR vs Temperature

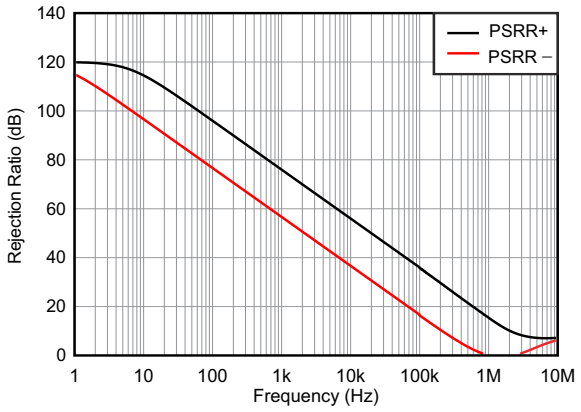
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



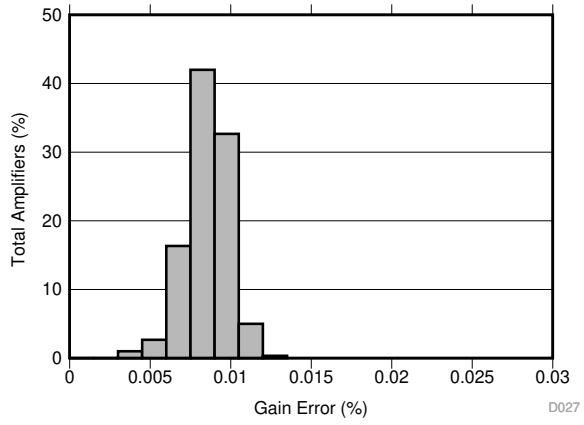
G = 1/2

Figure 7-25. PSRR vs Frequency (RTI)



G = 2

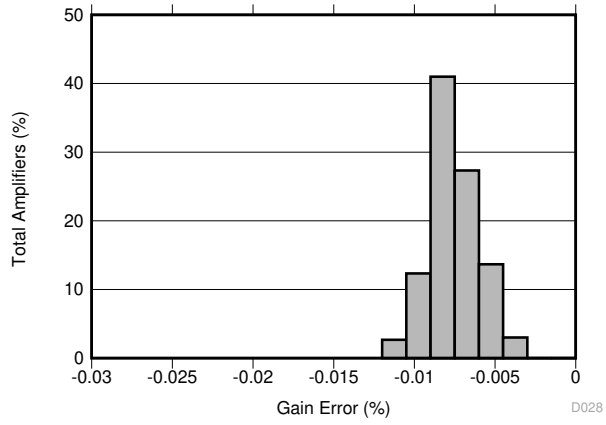
Figure 7-26. PSRR vs Frequency (RTI)



N = 470 Mean = 0.0085% Std. Dev. = 0.0014%

G = 1/2

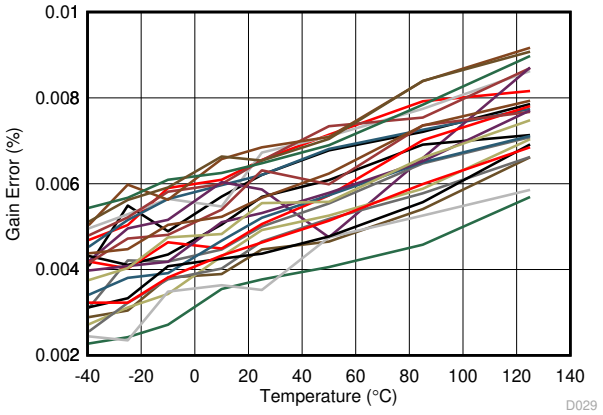
Figure 7-27. Typical Distribution of Gain Error



N = 470 Mean = –0.0076% Std. Dev. = 0.0015%

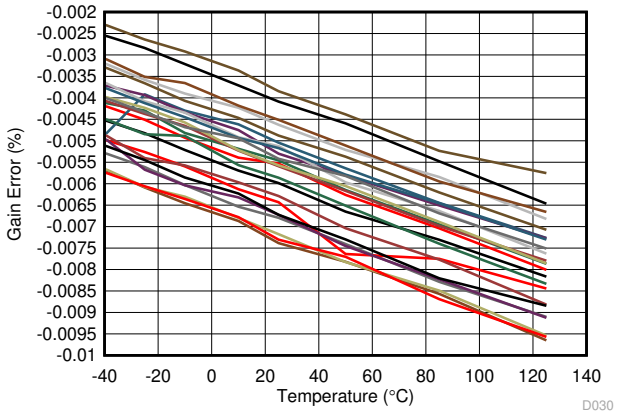
G = 2

Figure 7-28. Typical Distribution of Gain Error



G = 1 /2 30 units

Figure 7-29. Gain Error vs Temperature

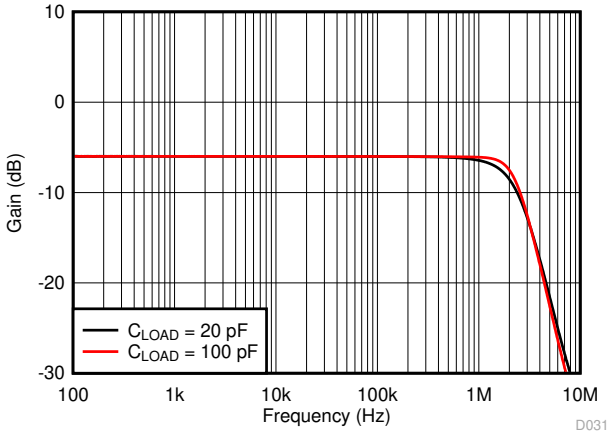


G = 2 30 units

Figure 7-30. Gain Error vs Temperature

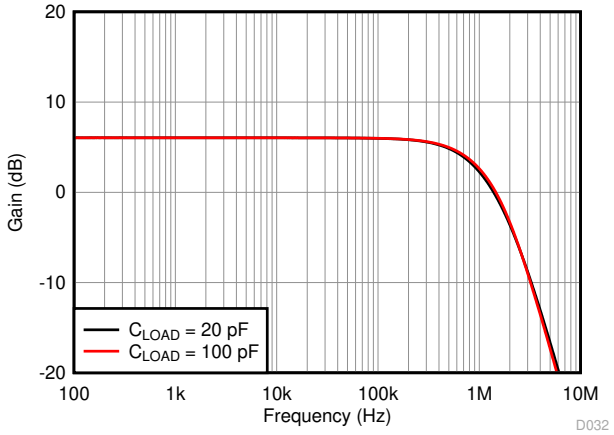
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



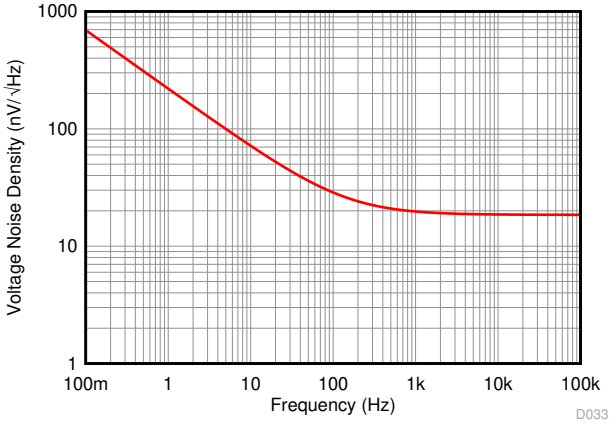
G = 1/2

Figure 7-31. Closed-Loop Gain vs Frequency



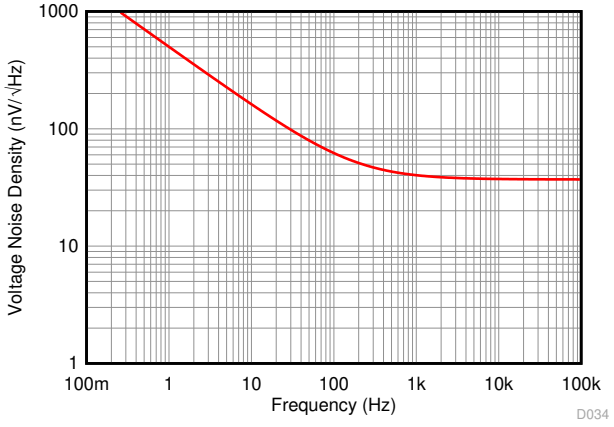
G = 2

Figure 7-32. Closed-Loop Gain vs Frequency



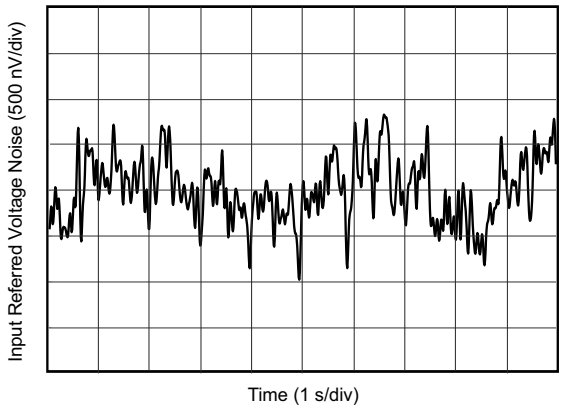
G = 1/2

Figure 7-33. Voltage Noise Spectral Density vs Frequency (RTI)



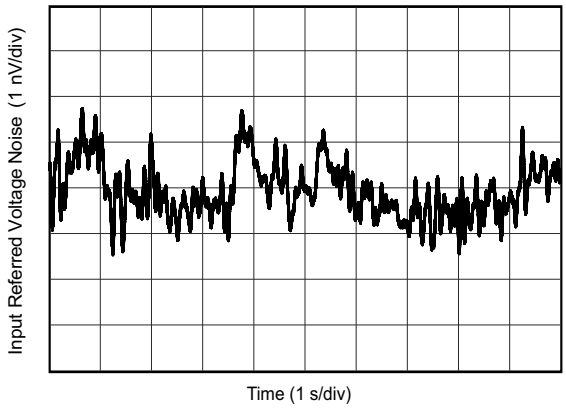
G = 2

Figure 7-34. Voltage Noise Spectral Density vs Frequency (RTI)



G = 1/2

Figure 7-35. 0.1-Hz to 10-Hz RTI Voltage Noise

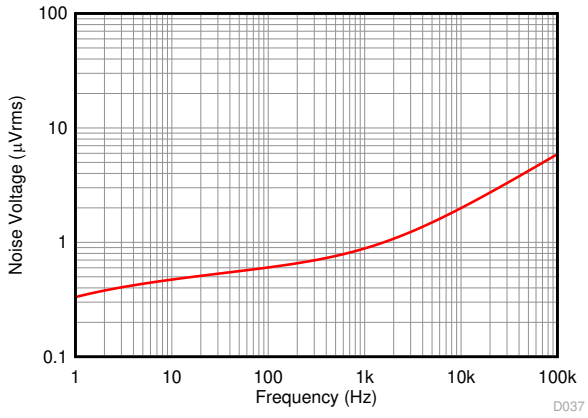


G = 2

Figure 7-36. 0.1-Hz to 10-Hz RTI Voltage Noise

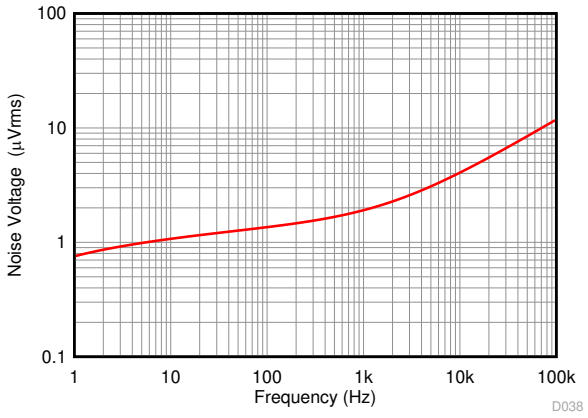
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



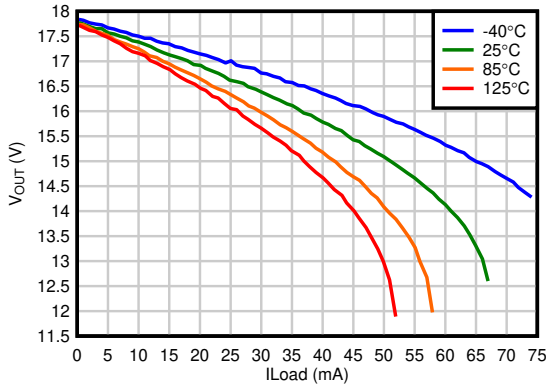
G = 1/2

Figure 7-37. Integrated Output Voltage Noise vs Noise Bandwidth



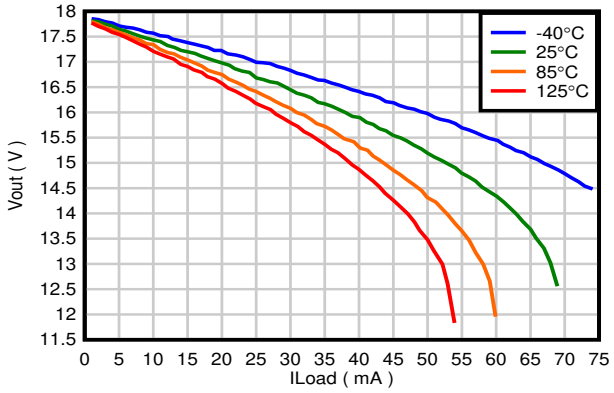
G = 2

Figure 7-38. Integrated Output Voltage Noise vs Noise Bandwidth



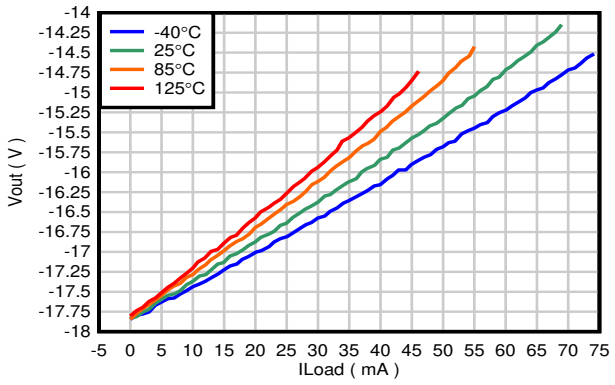
G = 1/2

Figure 7-39. Positive Output Voltage vs Output Current (Sourcing)



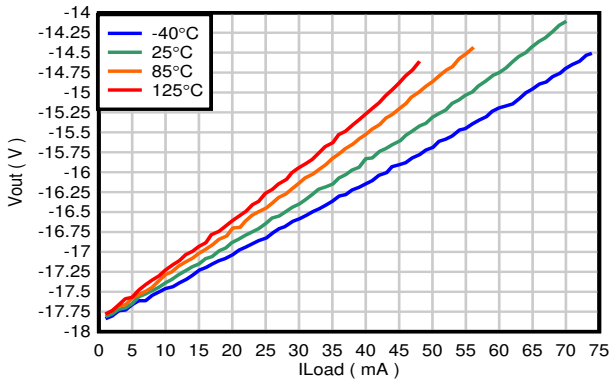
G = 2

Figure 7-40. Positive Output Voltage vs Output Current (Sourcing)



G = 1/2

Figure 7-41. Negative Output Voltage vs Output Current (Sinking)

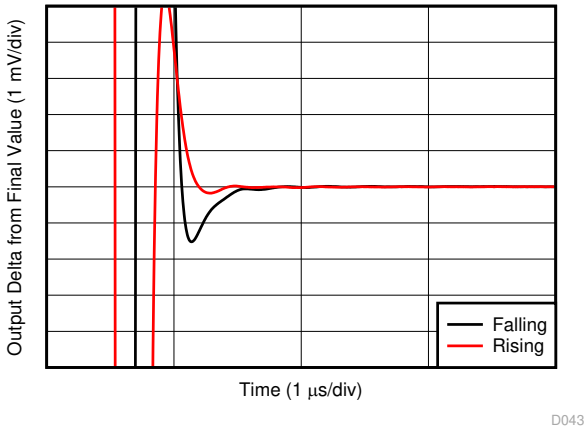


G = 2

Figure 7-42. Negative Output Voltage vs Output Current (Sinking)

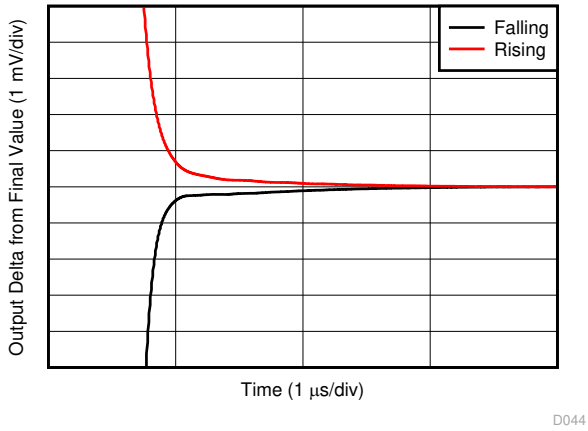
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



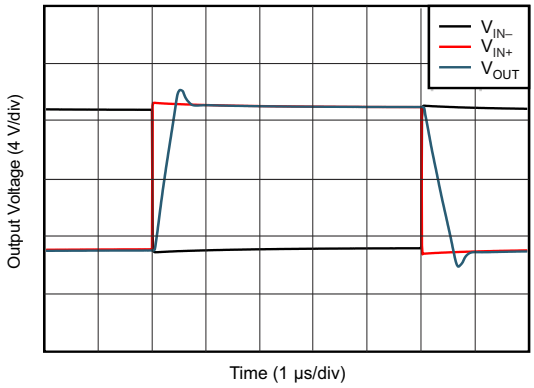
G = 1/2

Figure 7-43. Settling Time



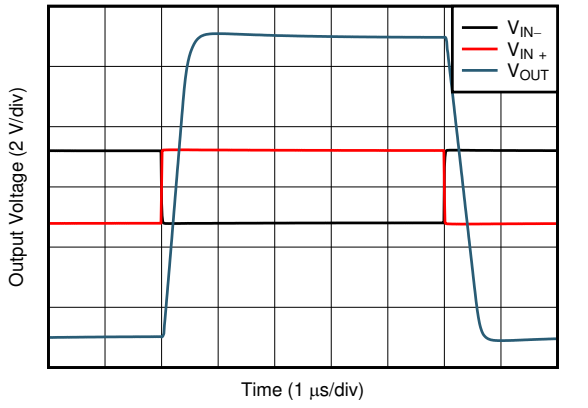
G = 2

Figure 7-44. Settling Time



G = 1/2

Figure 7-45. Large-Signal Step Response



G = 2

Figure 7-46. Large-Signal Step Response

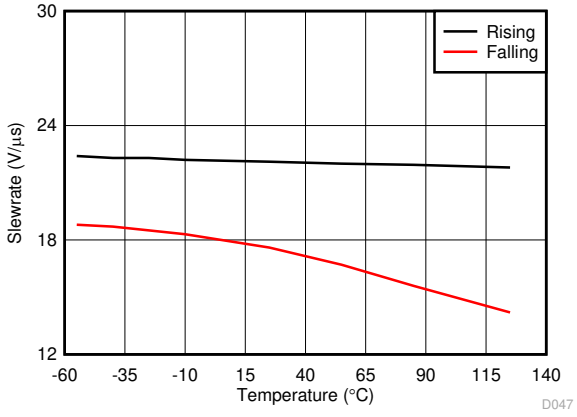


Figure 7-47. Slew Rate Over Temperature

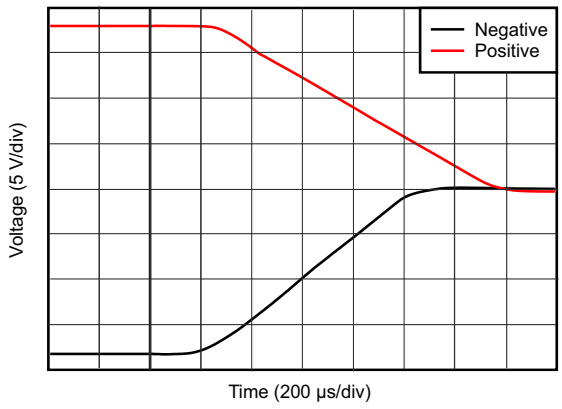
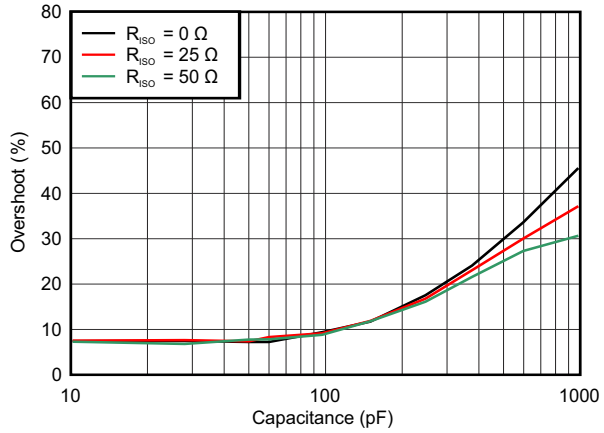


Figure 7-48. Overload Recovery (Normalized to 0 V)

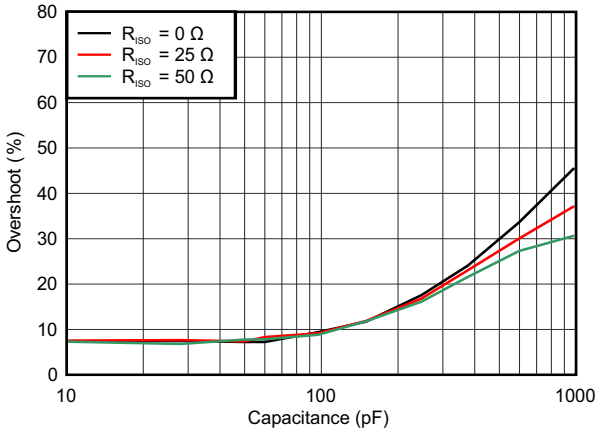
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



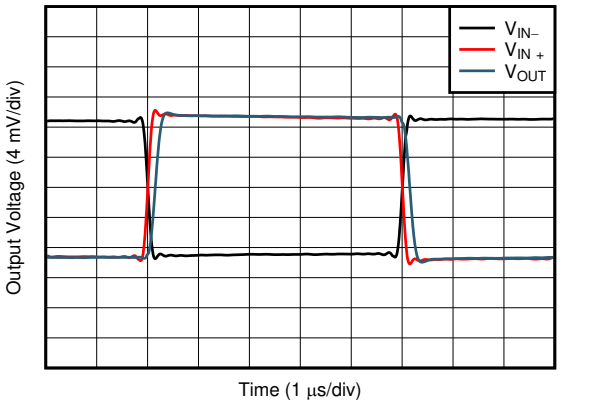
G = 1/2

Figure 7-49. Small-Signal Overshoot vs Capacitive Load



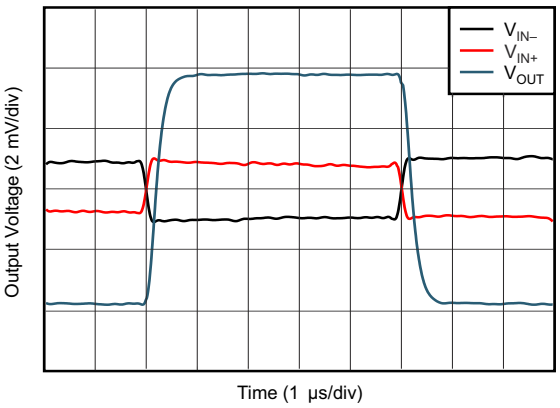
G = 2

Figure 7-50. Small-Signal Overshoot vs Capacitive Load



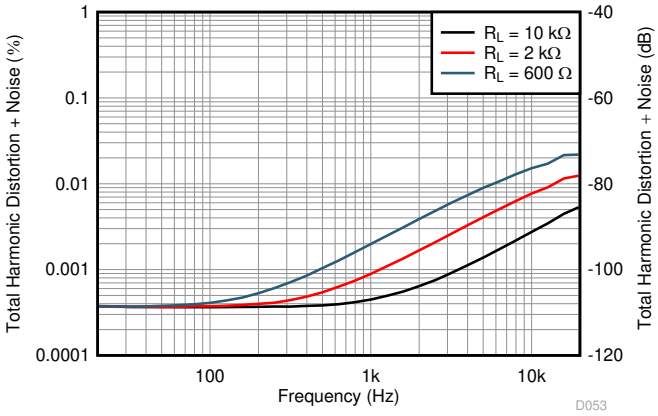
G = 1/2

Figure 7-51. Small-Signal Step Response



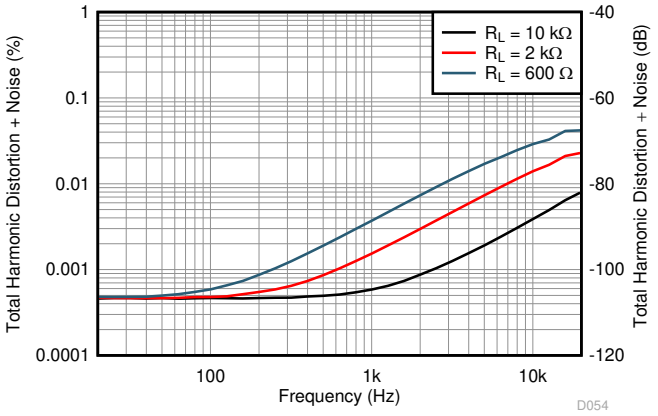
G = 2

Figure 7-52. Small-Signal Step Response



G = 1/2 V_{OUT} = 3.5 V_{RMS}

Figure 7-53. THD+N vs Frequency

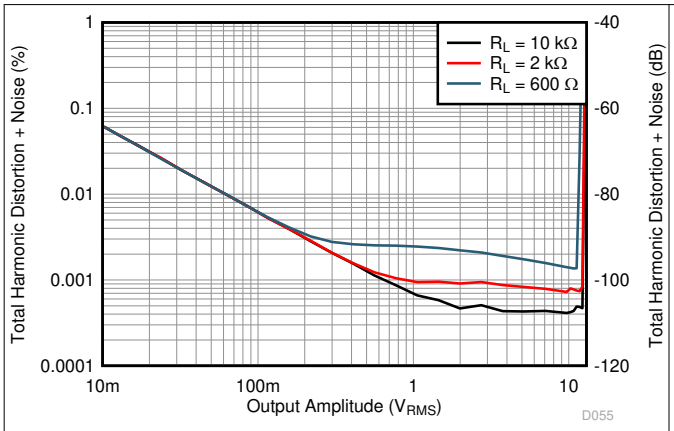


G = 2 V_{OUT} = 3.5 V_{RMS}

Figure 7-54. THD+N vs Frequency

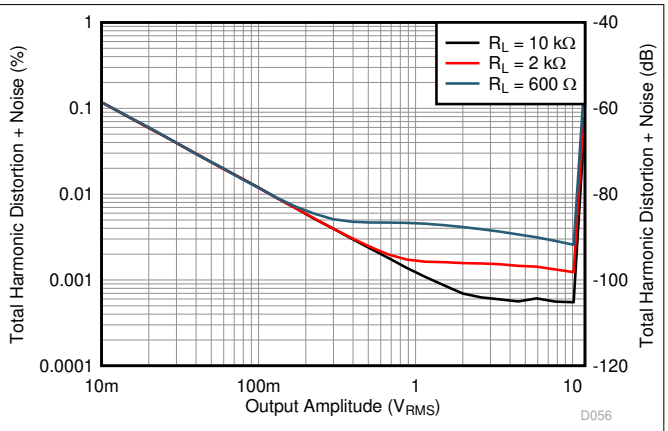
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



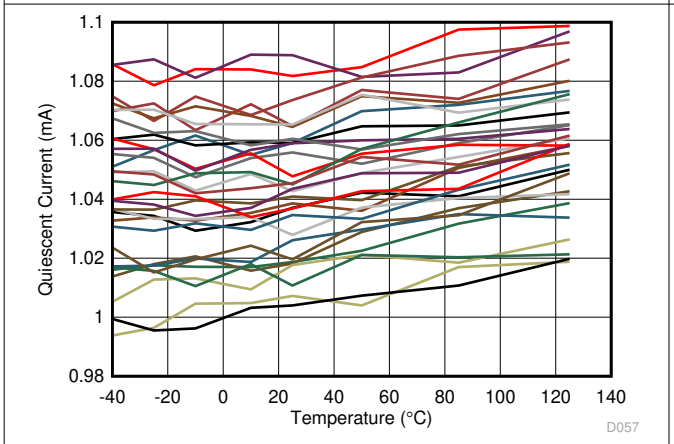
G = 1/2

Figure 7-55. THD+N Ratio vs Output Amplitude



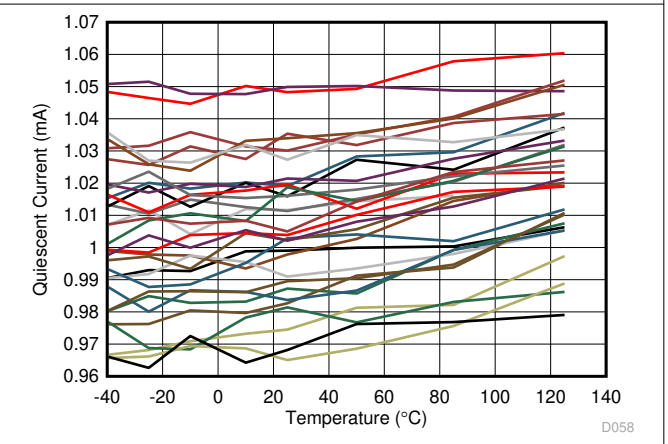
G = 2

Figure 7-56. THD+N Ratio vs Output Amplitude



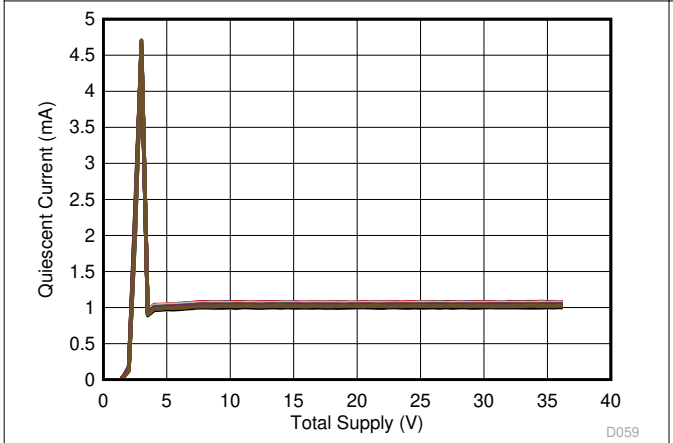
G = 1/2 30 units

Figure 7-57. Supply Current vs Temperature



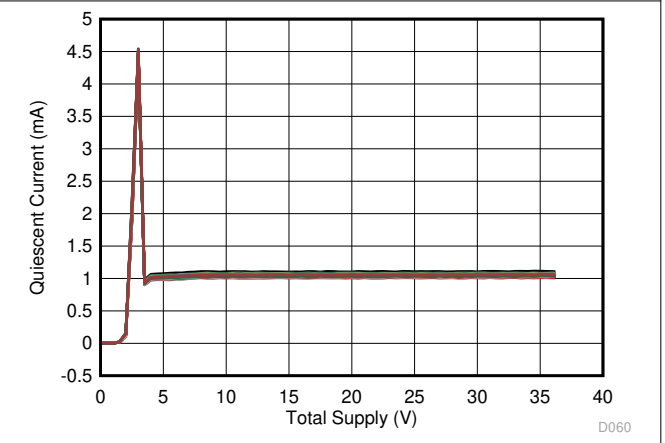
G = 2 30 units

Figure 7-58. Supply Current vs Supply Voltage



G = 1/2 30 units

Figure 7-59. Supply Current vs Supply Voltage

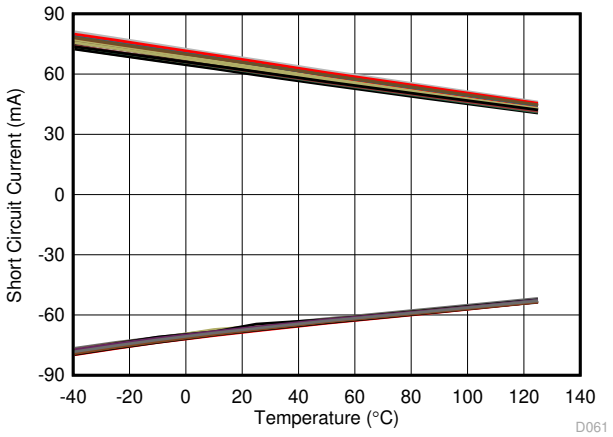


G = 2 30 units

Figure 7-60. Supply Current vs Supply Voltage

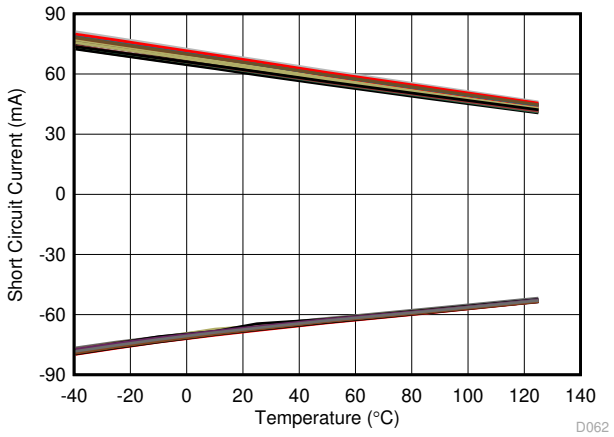
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



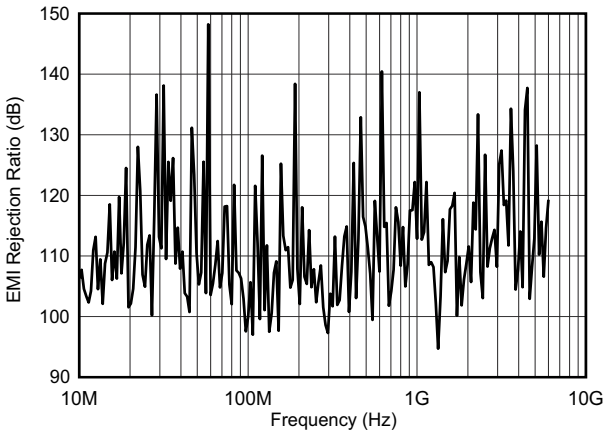
G = 1/2 30 units

Figure 7-61. Short Circuit Current vs Temperature



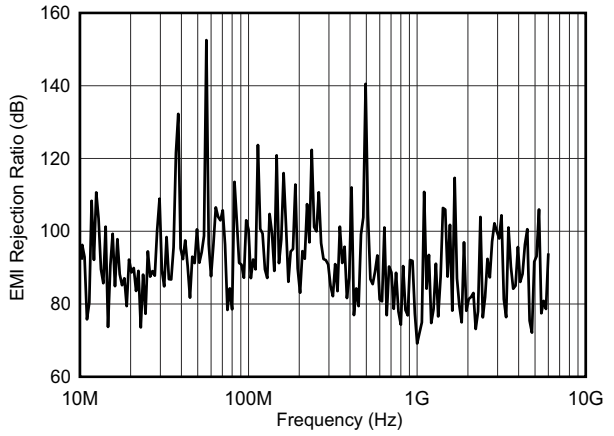
G = 2 30 units

Figure 7-62. Short Circuit Current vs Temperature



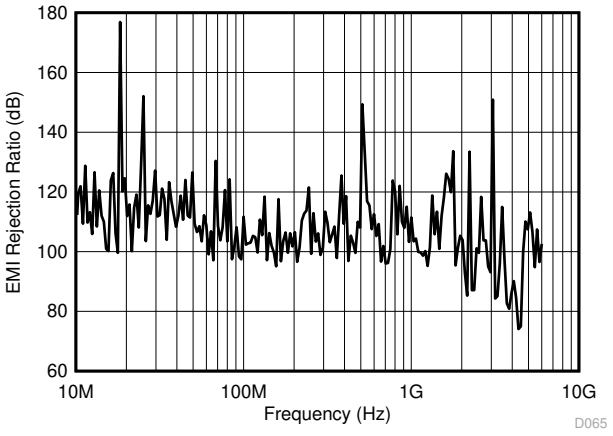
G = 1/2

Figure 7-63. Differential-Mode EMI Rejection Ratio



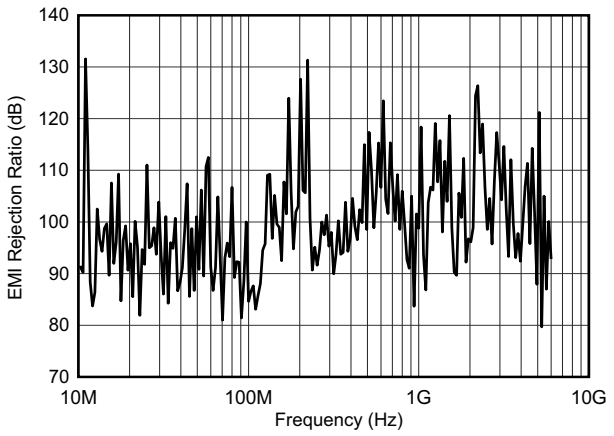
G = 2

Figure 7-64. Differential-Mode EMI Rejection Ratio



G = 1/2

Figure 7-65. Common-Mode EMI Rejection Ratio

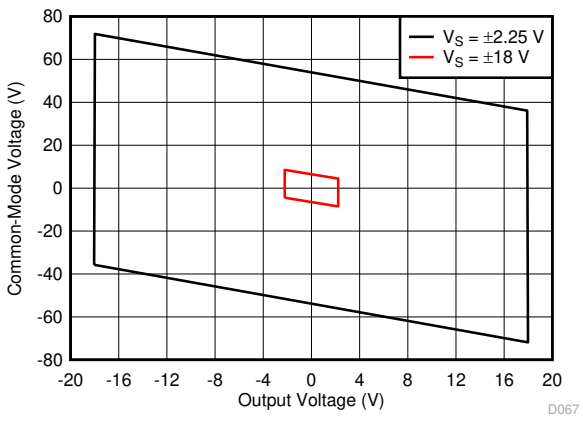


G = 2

Figure 7-66. Common-Mode EMI Rejection Ratio

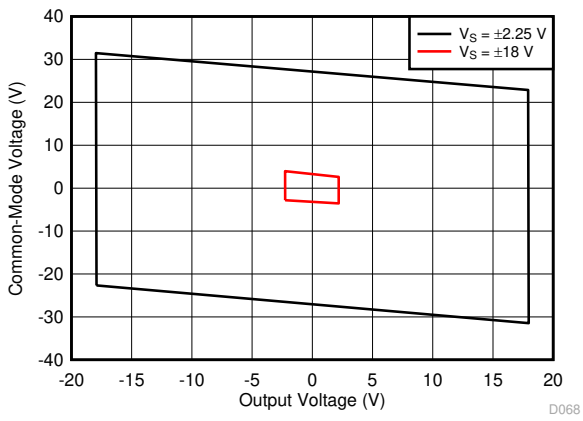
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)



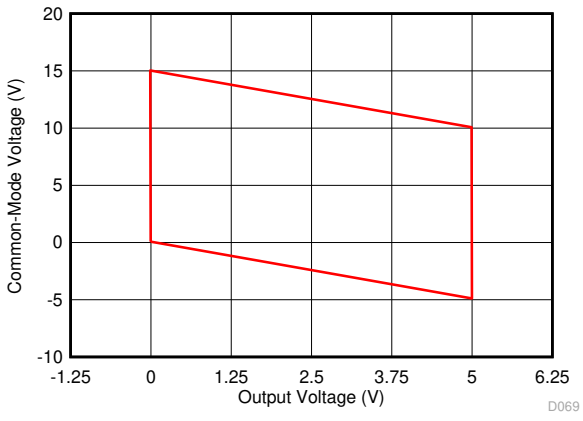
G = 1/2 Bipolar supply V_{REF} = 0 V

Figure 7-67. Input Common-Mode Voltage vs Output Voltage



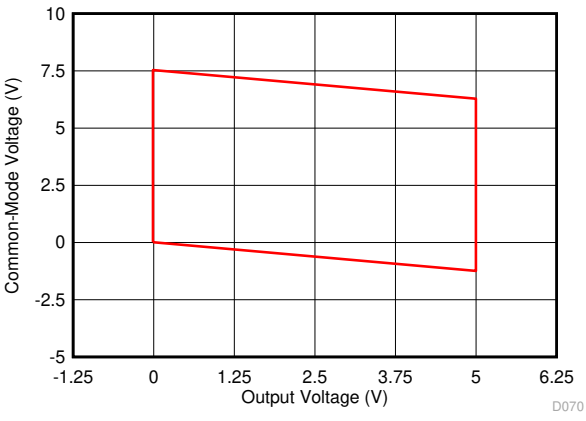
G = 2 Bipolar supply V_{REF} = 0 V

Figure 7-68. Input Common-Mode Voltage vs Output Voltage



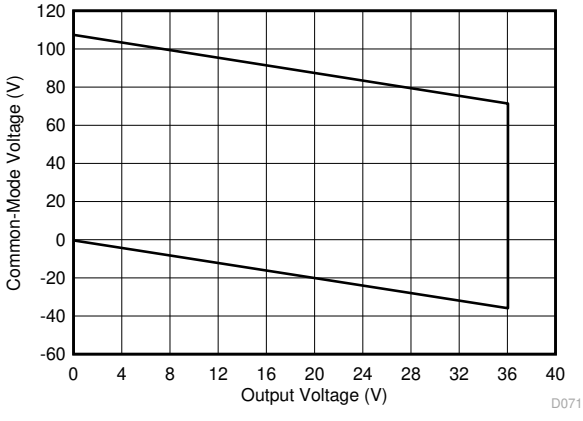
G = 1/2 5-V supply V_{REF} = 0 V

Figure 7-69. Input Common-Mode Voltage vs Output Voltage



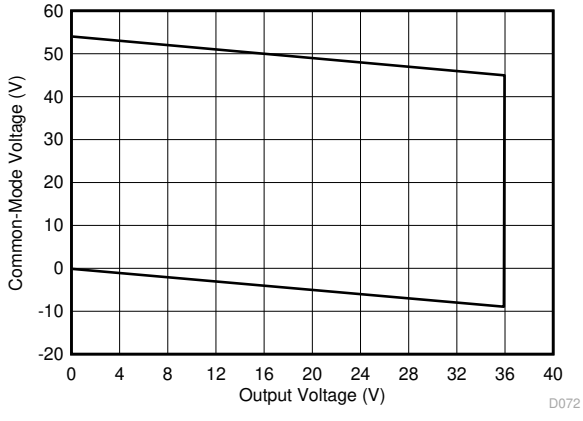
G = 2 5-V supply V_{REF} = 0 V

Figure 7-70. Input Common-Mode Voltage vs Output Voltage



G = 1/2 36-V supply V_{REF} = 0 V

Figure 7-71. Input Common-Mode Voltage vs Output Voltage



G = 2 36-V supply V_{REF} = 0 V

Figure 7-72. Input Common-Mode Voltage vs Output Voltage

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = V_S / 2, R_L = 10 kΩ, REF pin connected to ground, G = 1/2 (unless otherwise noted)

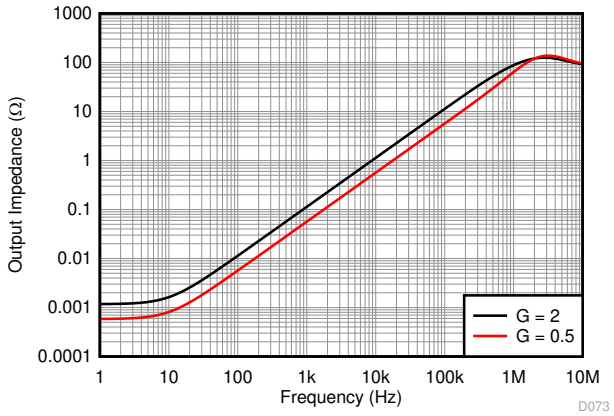


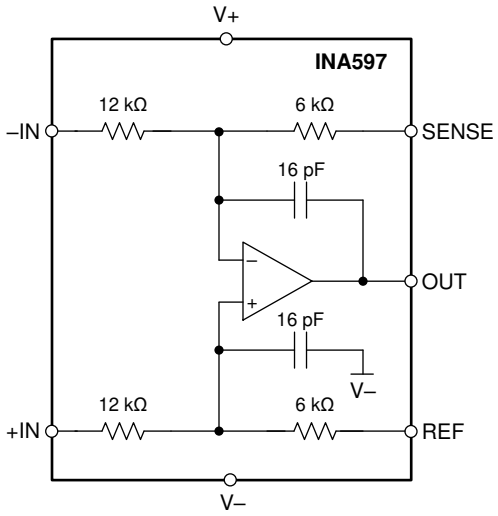
Figure 7-73. Closed-Loop Output Impedance vs Frequency

8 Detailed Description

8.1 Overview

The INA597 consists of a high-precision, e-trim™ operational amplifier and four trimmed resistors. These resistors can be connected to make a wide variety of amplifier configurations, including difference, noninverting, and inverting configurations. Using the on-chip resistors of the INA597 provides the designer with several advantages over a discrete design. The INA597 also includes internal compensation capacitors, as shown in *Section 8.2*.

8.2 Functional Block Diagram



8.3 Feature Description

Much of the dc performance of op-amp circuits depends on the accuracy of the surrounding resistors. The resistors on the INA597 are laid out to be tightly matched. The resistors of each part are matched on-chip and tested for their matching accuracy. As a result of this trimming and testing, the INA597 provides high accuracy for specifications such as gain drift, common-mode rejection, and gain error.

8.4 Device Functional Modes

The INA597 measures voltages beyond the rails. For the G = ½ and G = 2 difference amplifier configurations, see the input voltage range in *Section 7* for details. The INA597 can be configured in several ways; see Figure 9-5 to Figure 9-9. These configurations rely on the internal, matched resistors; therefore, all of these configurations have excellent gain accuracy and gain drift.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Figure 9-1 shows the basic connections required for operation of the INA597. Connect power supply bypass capacitors close to the device pins.

The differential input signal is connected to pins 2 and 3, as shown. The source impedances connected to the inputs must be nearly equal to provide good common-mode rejection. An 8-Ω mismatch in source impedance degrades the common-mode rejection of a typical device to approximately 80 dB. Gain accuracy is also slightly affected. If the source has a known impedance mismatch, use an additional resistor in series with one input to preserve good common-mode rejection.

9.2 Typical Applications

9.2.1 Basic Power-Supply and Signal Connections

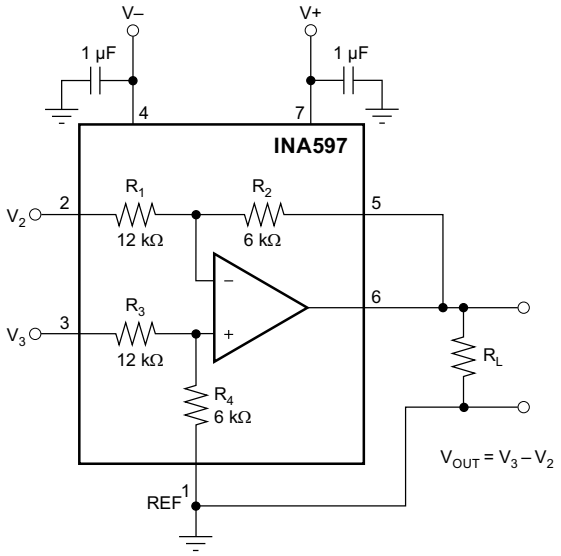


Figure 9-1. Basic Power-Supply and Signal Connections

9.2.1.1 Design Requirements

For the application shown in Figure 9-1, the design requirements are:

- Gain of G = ½
- V_{REF} = 0 V

9.2.1.2 Detailed Design Procedure

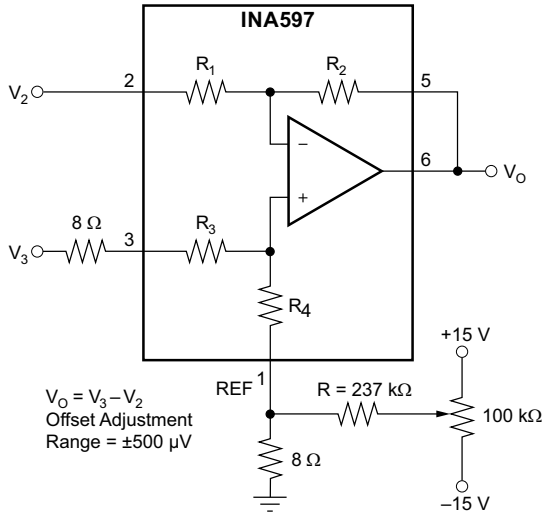
9.2.1.2.1 Operating Voltage

The INA597 operates from single (4.5 V to 36 V) or dual (±2.25 V to ±18 V) supplies with excellent performance. Specifications are production tested with +5-V and ±15-V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in *Section 7.7*. The internal op amp in the INA597 is a single-supply design. This design allows linear operation with the op amp common-mode voltage equal to, or slightly less than V– (or single-supply ground). Although input voltages on pins 2 and 3 that are less than the negative supply voltage do not damage the device, operation in this region is not recommended. Transient conditions at the inverting input terminal less than the negative supply can cause a positive feedback condition that could lock the device output to the negative rail.

The INA597 accurately measures differential signals that are greater than the positive power supply. For example with G = ½, the linear common-mode range extends to nearly three times the positive power supply voltage; see *Section 7.7*, as well as *Section 9.2.1.2.3*.

9.2.1.2.2 Offset Voltage Trim

The INA597 is production trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 9-2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the REF pin is summed with the output signal. This configuration can be used to null offset voltage. To maintain good common-mode rejection, make sure the source impedance of a signal applied to the REF pin is less than 8 Ω. For low impedance at the REF pin, the trim voltage can be buffered with an op amp, such as the OPA177.



NOTE: For ±750-µV range, R = 158 kΩ.

Figure 9-2. Offset Adjustment

9.2.1.2.3 Input Voltage Range

The INA597 measures input voltages beyond the supply rails. The internal resistors divide down the voltage before the voltage reaches the internal op amp and provide protection to the op amp inputs. Figure 9-3 shows an example of how the voltage division works in a difference-amplifier configuration. For the INA597 to measure correctly, the input voltages at the input nodes of the internal op amp must stay less than 0.1 V of the positive supply rail, and can exceed the negative supply rail by 0.1 V. See *Section 10* for more details.

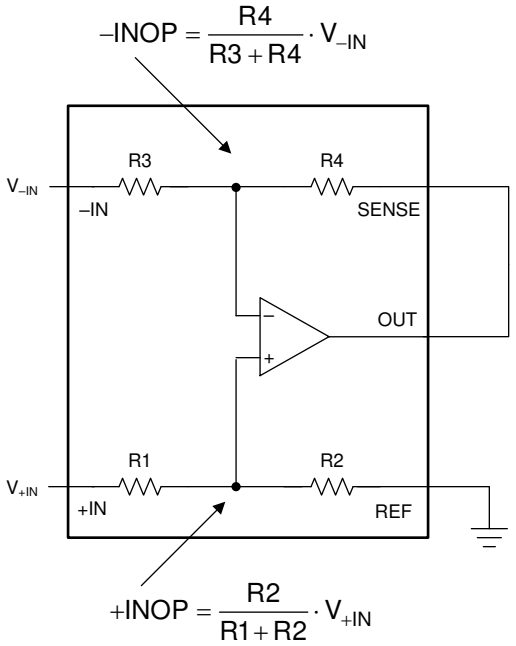


Figure 9-3. Voltage Division in the Difference Amplifier Configuration

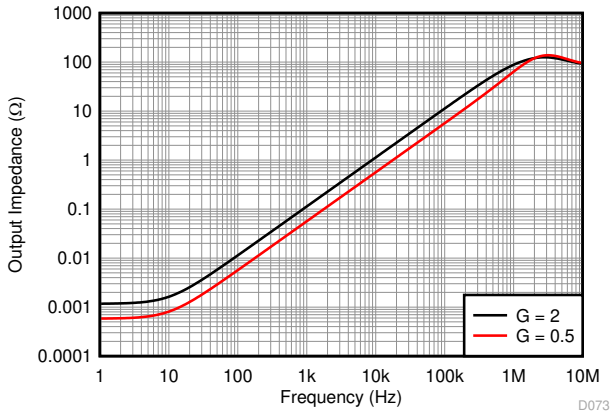
The INA597 has integrated ESD diodes at the inputs that provide overvoltage protection. This feature simplifies system design by eliminating the need for additional external protection circuitry, and enables a more robust system. The voltages at any of the inputs of the parts in G = ½ configuration with ±18 V supplies can safely range from $+V_S$ − 54 V up to $-V_S$ + 54 V. For example, on ±10-V supplies, the input voltages can go as high as ±30 V.

9.2.1.2.4 Capacitive Load Drive Capability

The INA597 can drive large capacitive loads, even at low supplies. The device is stable with a 500-pF load; see *Section 7.7*.

9.2.1.3 Application Curve

The interaction between the output stage of an operational amplifier (op amp) and capacitive loads can impact the stability of the circuit. Throughout the industry, op-amp output-stage requirements have changed greatly since their original creation. Classic output stages with the class-AB common-emitter bipolar junction transistor (BJT) have now been replaced with common-collector BJT and common-drain complementary metal-oxide semiconductor (CMOS) devices. Both of these technologies enable rail-to-rail output voltages for single-supply and battery-powered applications. A result of changing these output-stage structures is that the op-amp open-loop output impedance (Zo) changed from the largely resistive behavior of early BJT op amps to a frequency-dependent Z_O that features capacitive, resistive, and inductive portions. Proper understanding of Z_O over frequency—and also the resulting closed-loop output impedance over frequency—is crucial for the understanding of loop gain, bandwidth, and stability analysis. Figure 9-4 shows how the INA597 closed-loop output impedance varies over frequency.



V_S = ±18 V

Figure 9-4. Closed-Loop Output Impedance vs Frequency

9.2.2 Precision Instrumentation Amplifier

The INA597 can be combined with op amps to form a complete instrumentation amplifier (IA) with specialized performance characteristics, as shown in Figure 9-5.

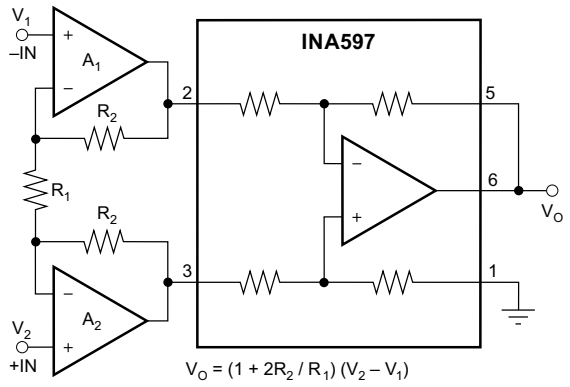


Figure 9-5. Precision Instrumentation Amplifier

9.2.3 Low Power, High-Output Current, Precision, Difference Amplifier

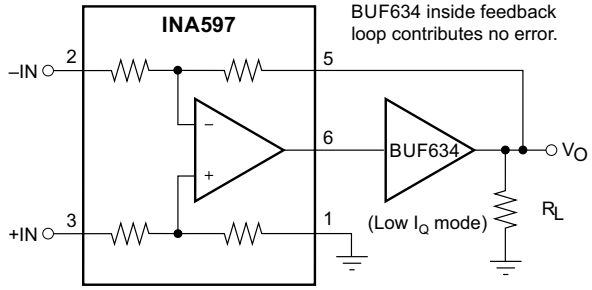


Figure 9-6. Low Power, High-Output Current, Precision, Difference Amplifier

9.2.4 Pseudoground Generator

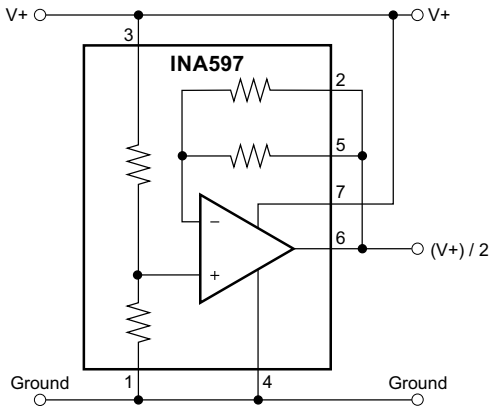


Figure 9-7. Pseudoground Generator

9.2.5 Differential Input Data Acquisition

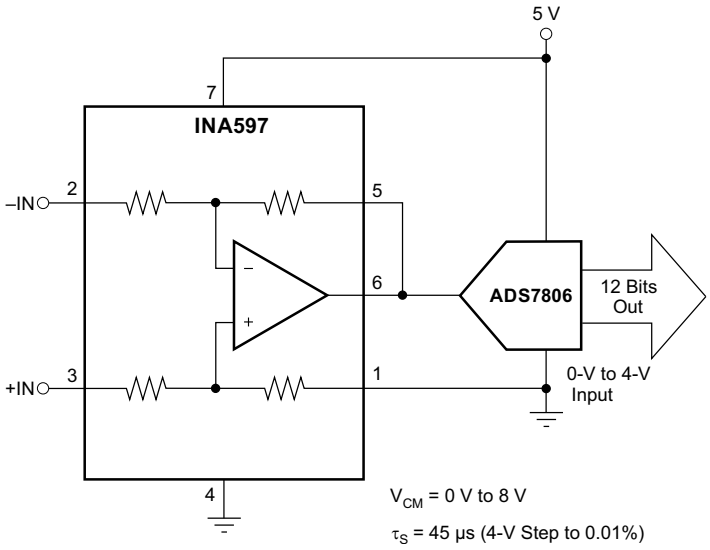
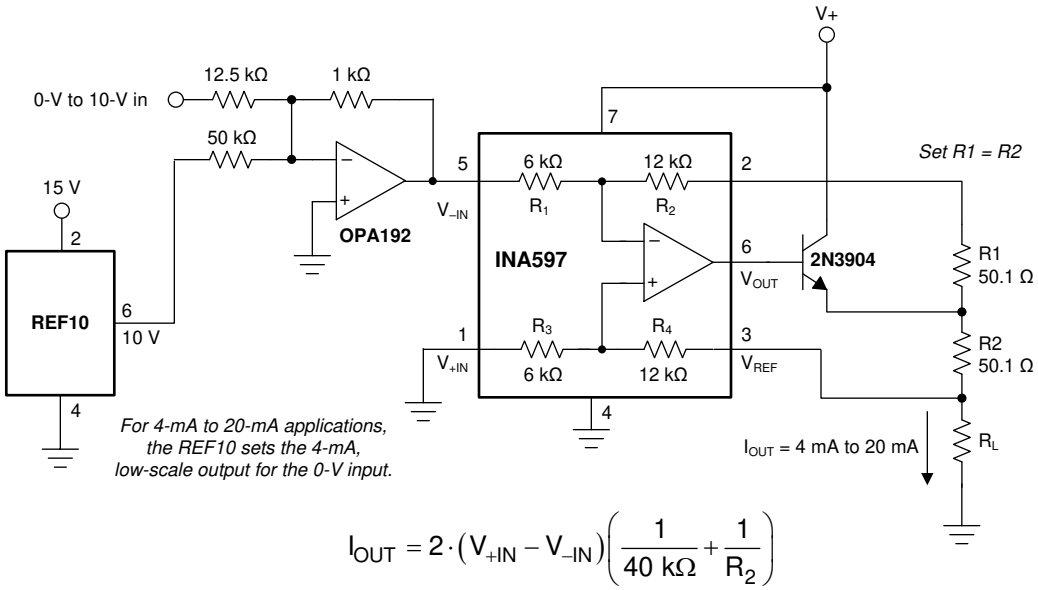


Figure 9-8. Differential Input Data Acquisition

9.2.6 Precision Voltage-to-Current Conversion



$$I_{OUT} = 2 \cdot (V_{+IN} - V_{–IN}) \left(\frac{1}{40\ k\Omega} + \frac{1}{R_2} \right)$$

Figure 9-9. Precision Voltage-to-Current Conversion

9.2.7 Additional Applications

Texas Instruments offers many complete high-performance instrumentation amplifiers. See Table 9-1 for some of the products with related performance.

Table 9-1. Recommended Op Amp Products to Use With the INA597

A1, A2	FEATURE	SIMILAR TI IA
OPA27	Low noise	INA103
OPA129	Ultra-low bias current (fA)	INA116
OPA177	Low offset drift, low noise	INA114, INA128
OPA2130	Low power, FET-input (pA)	INA111
OPA2234	Single supply, precision, low power	INA122. INA118
OPA2237	SIngle supply, low power, 8-pin MSOP	INA122, INA126

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current receiver with compliance to rails
- Precision unity-gain inverting amplifier
- ±10-V precision voltage reference
- ±5-V precision voltage reference
- Precision unity-gain buffer
- Precision average value amplifier
- Precision G = 2 amplifier
- Precision summing amplifier
- Precision G = 1/2 amplifier
- Precision bipolar offsetting
- Precision summing amplifier with gain
- Instrumentation amplifier guard drive generator
- Precision summing instrumentation amplifier
- Precision absolute value buffer
- Precision voltage-to-current converter with differential inputs
- Differential input voltage-to-current converter for low IOUT
- Isolating current source
- Differential output difference amplifier
- Isolating current source with buffering amplifier for greater accuracy
- Window comparator with window span and window center inputs
- Precision voltage-controlled current source with buffered differential inputs and gain
- Digitally controlled gain of ±1 amplifier

10 Power Supply Recommendations

The nominal performance of the INA597 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device operates using power supplies from ±2.25 V (4.5 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in *Section 7.7*.

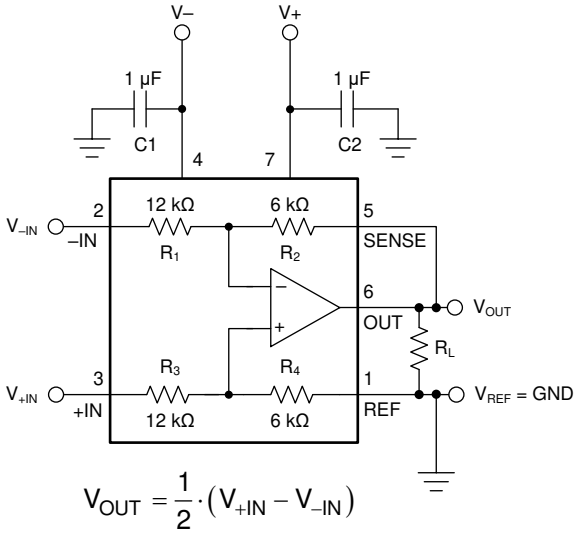
11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

11.2 Layout Example



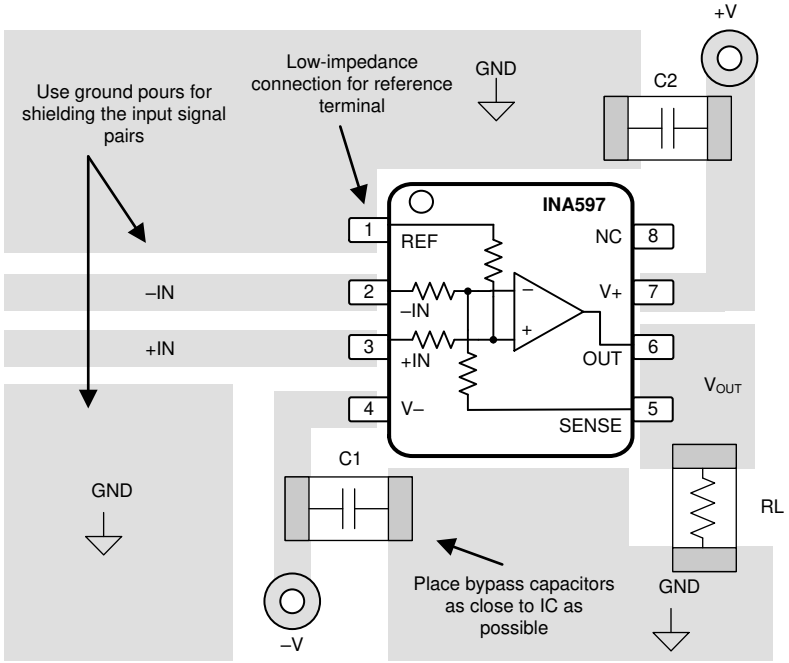
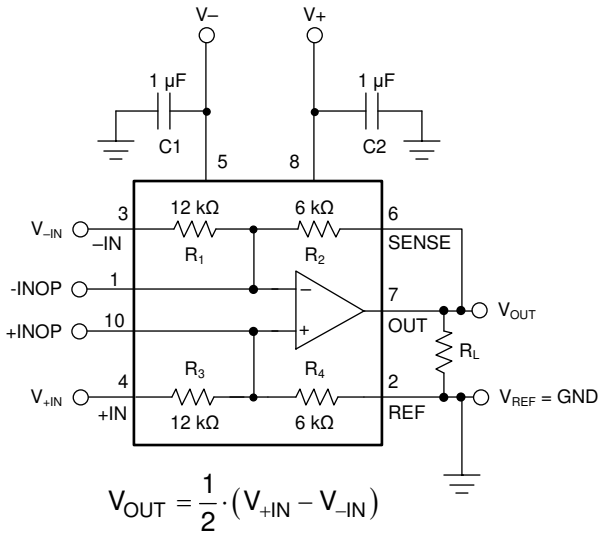


Figure 11-1. Example Schematic and Associated PCB Layout for SOIC and VSSOP Packages



$$V_{OUT} = \frac{1}{2} \cdot (V_{+IN} - V_{-IN})$$

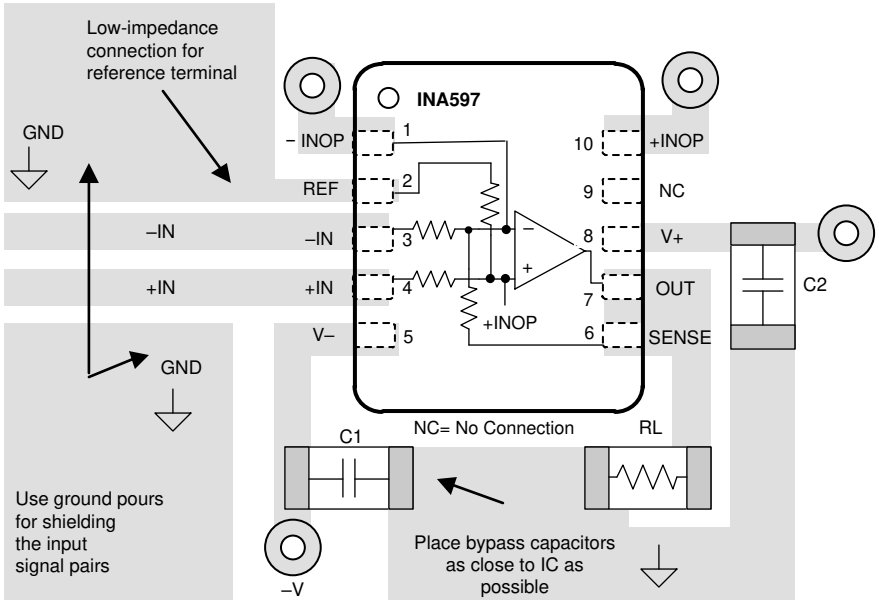


Figure 11-2. Example Schematic and Associated PCB Layout with VSON Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Universal Difference Amplifier Evaluation Module* user's guide
- Texas Instruments, *Precision Signal-Conditioning Solutions for Motor-Control Position Feedback* technical brief

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA597IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1WT6
INA597IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1WT6
INA597IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1WT6
INA597IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1WT6
INA597IDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA597
INA597IDR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA597
INA597IDRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN597
INA597IDRCR.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN597
INA597IDRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN597
INA597IDRCT.B	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN597
INA597IDT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA597
INA597IDT.B	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA597

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

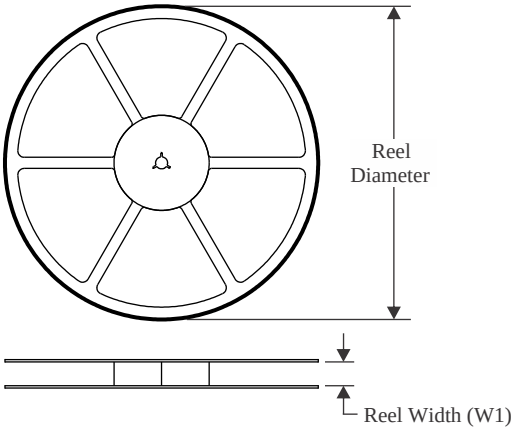
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

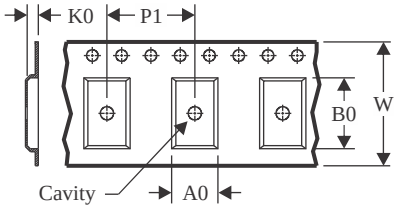
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

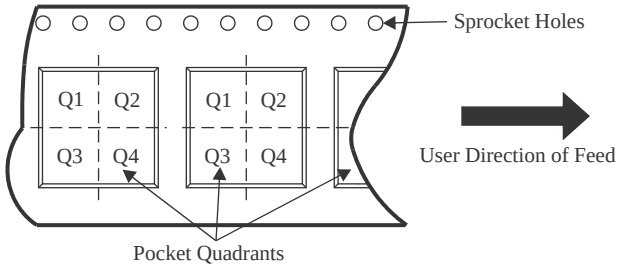


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

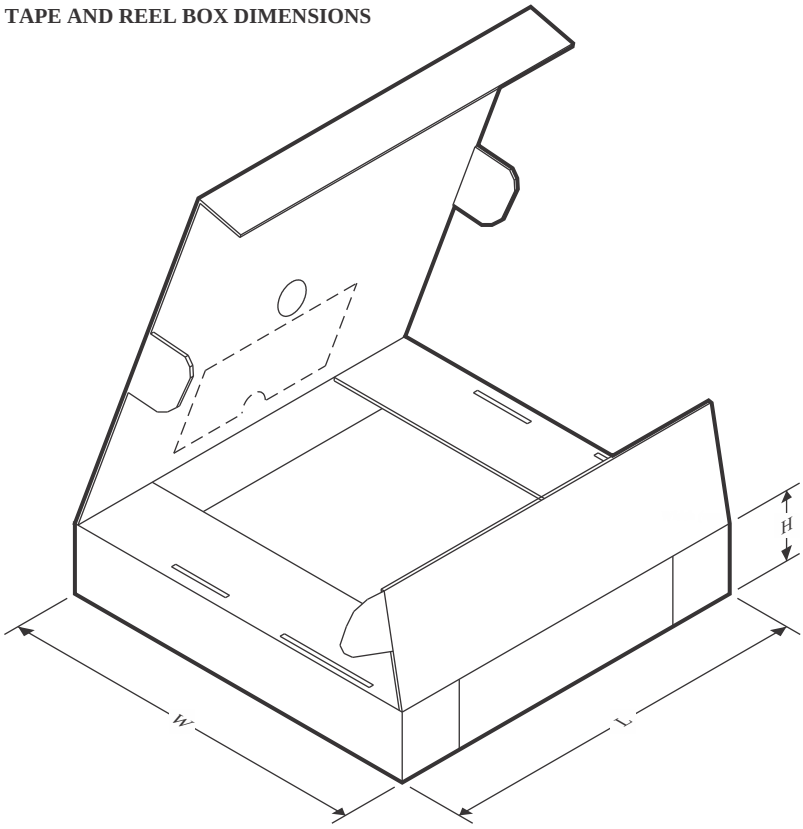
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA597IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA597IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA597IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA597IDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA597IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA597IDT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

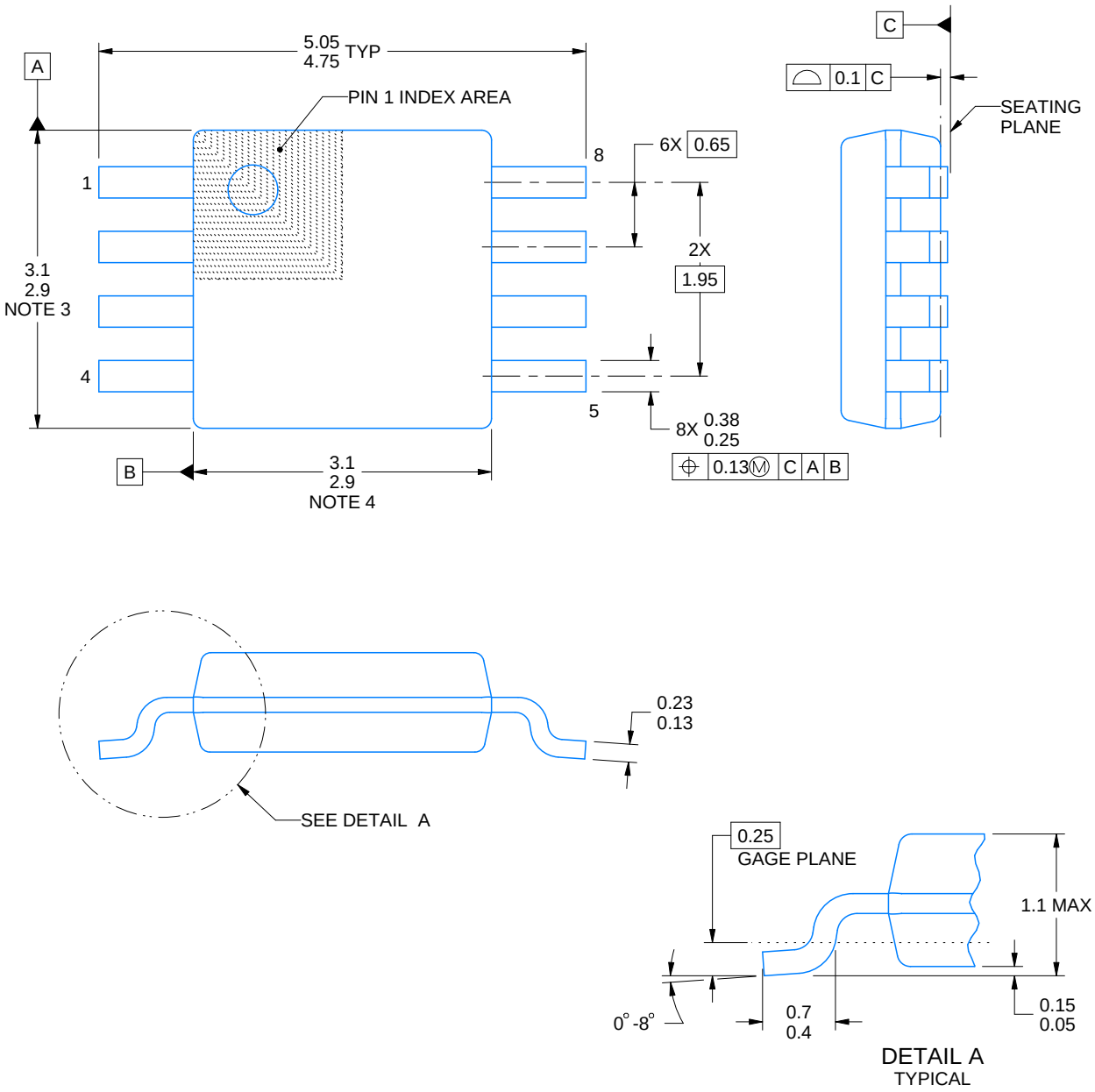
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA597IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA597IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA597IDR	SOIC	D	8	3000	353.0	353.0	32.0
INA597IDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
INA597IDRCT	VSON	DRC	10	250	210.0	185.0	35.0
INA597IDT	SOIC	D	8	250	213.0	191.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

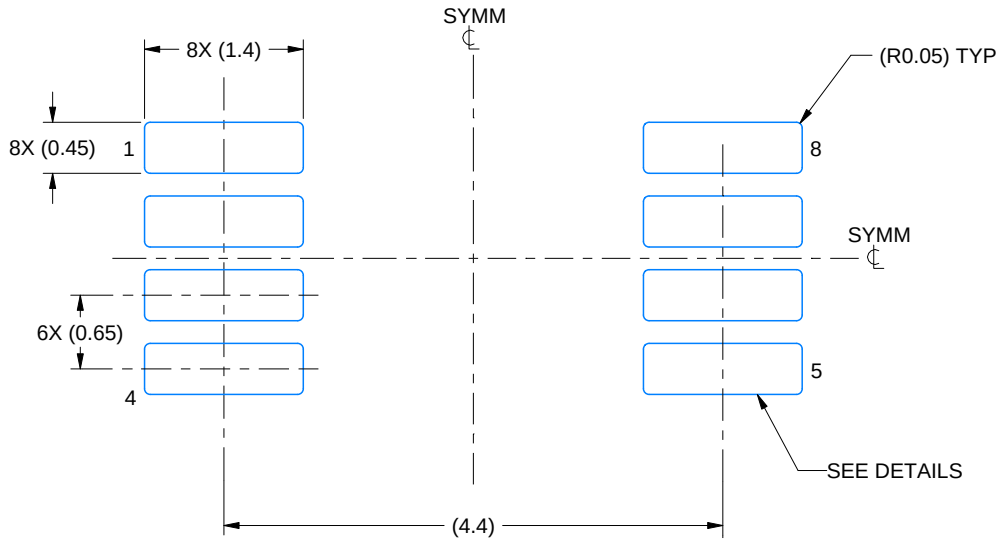
SMALL OUTLINE PACKAGE



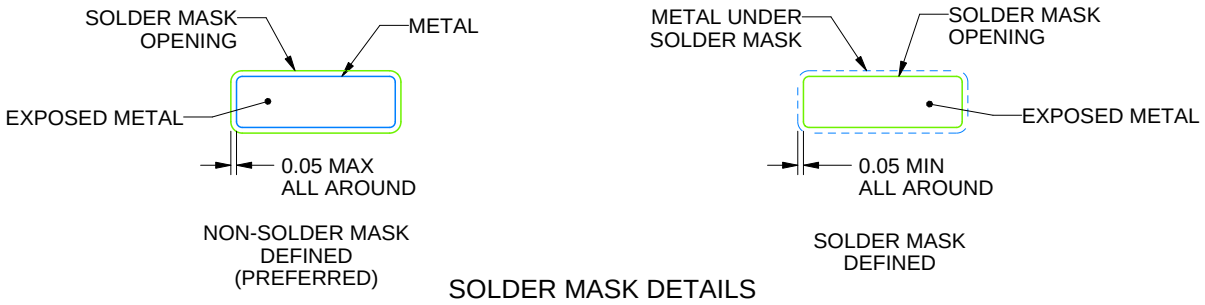
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

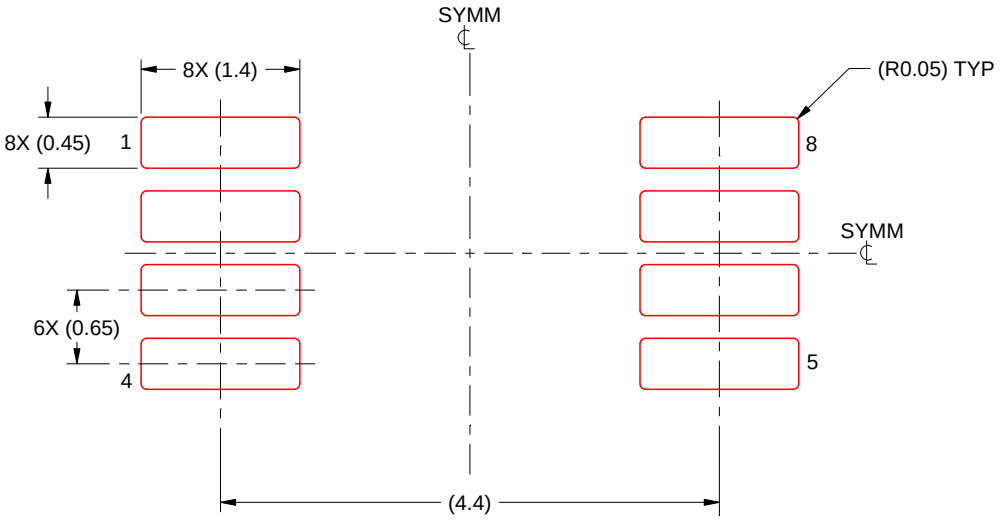


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

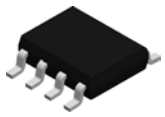


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

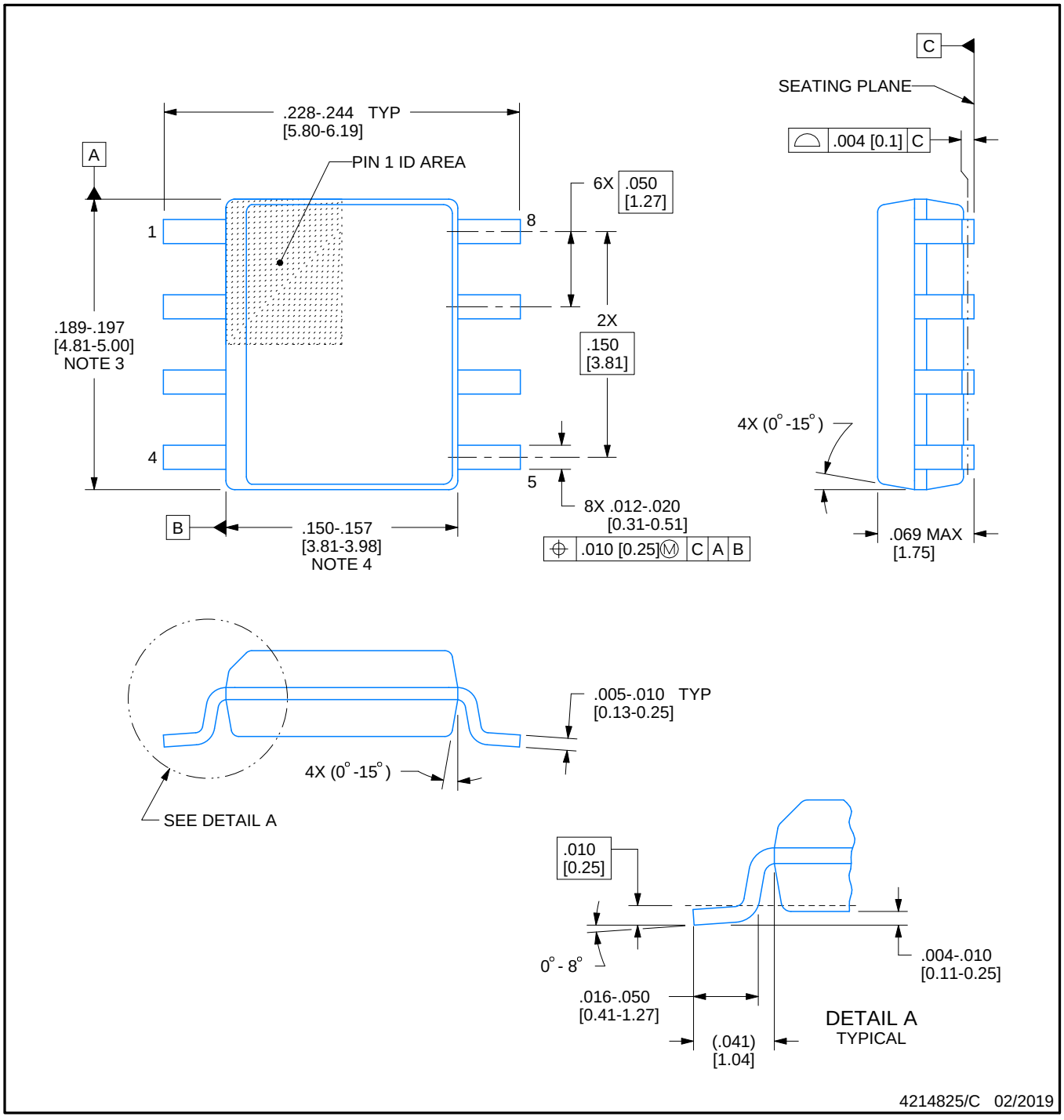


PACKAGE OUTLINE

D0008A

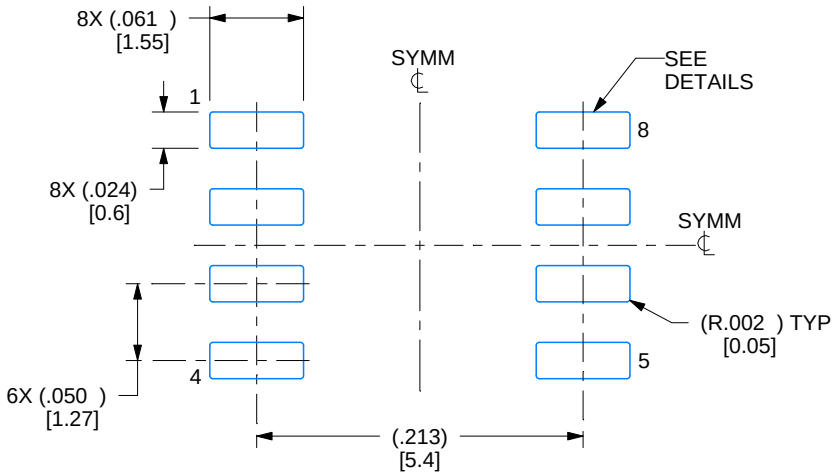
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

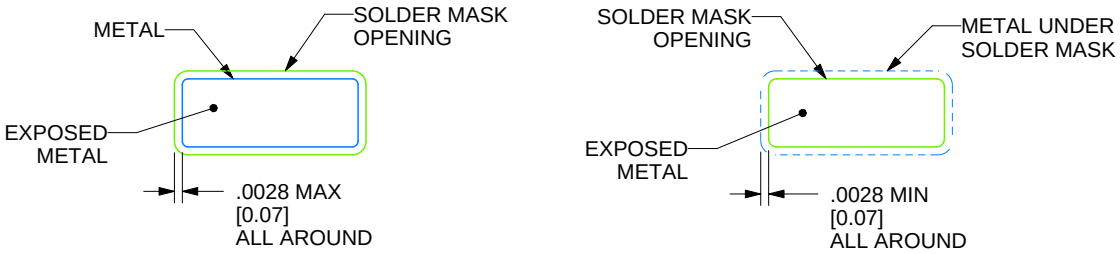


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

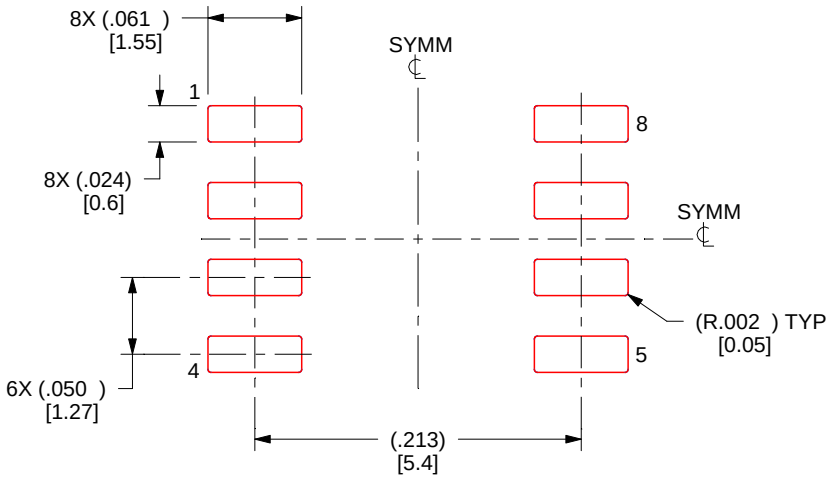
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

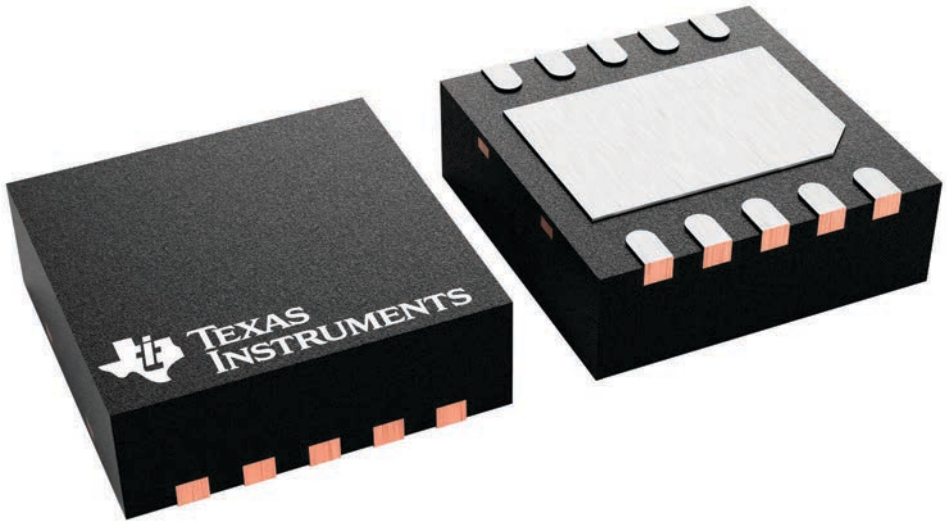
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



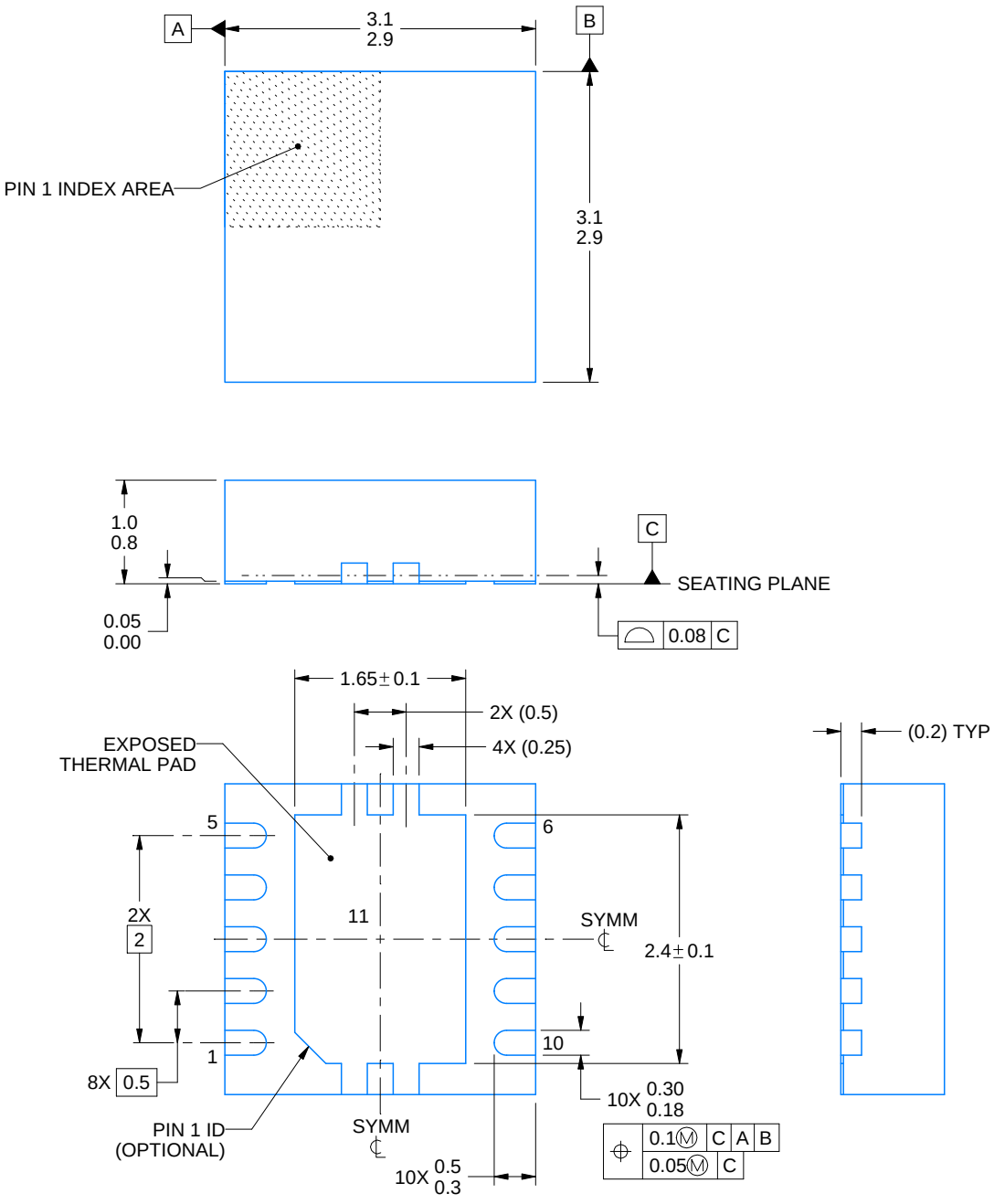
4226193/A

DRC0010J

PACKAGE OUTLINE

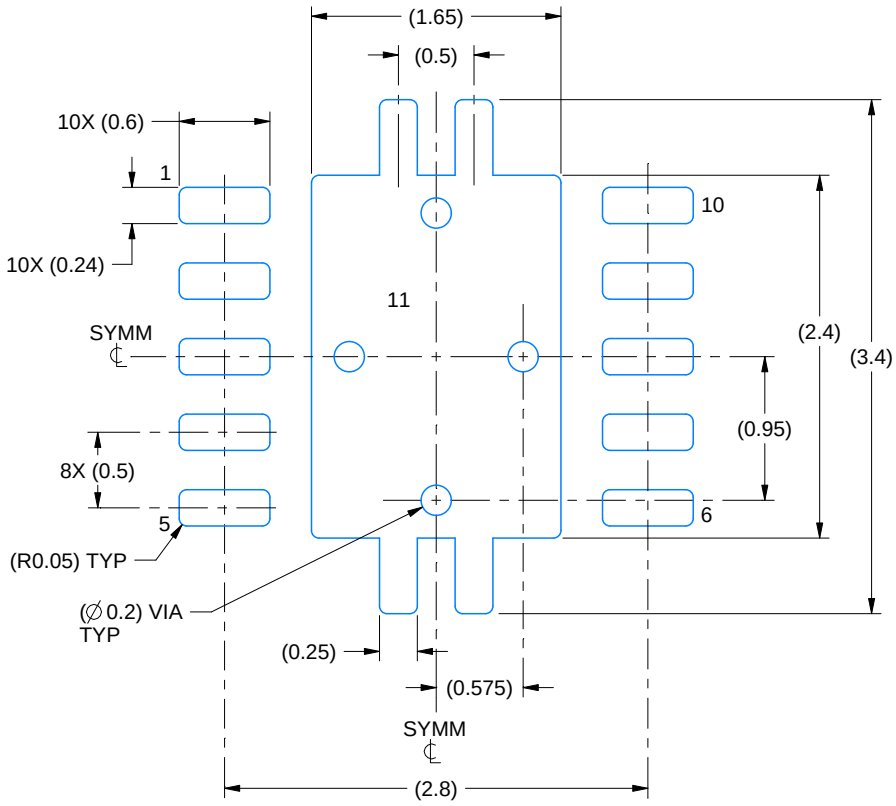
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

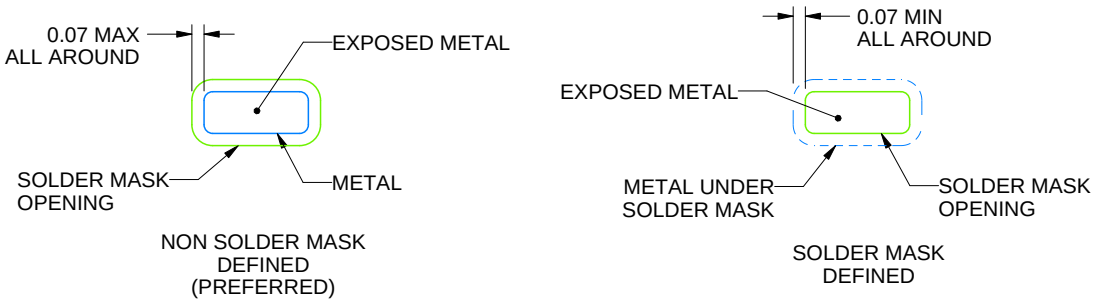


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

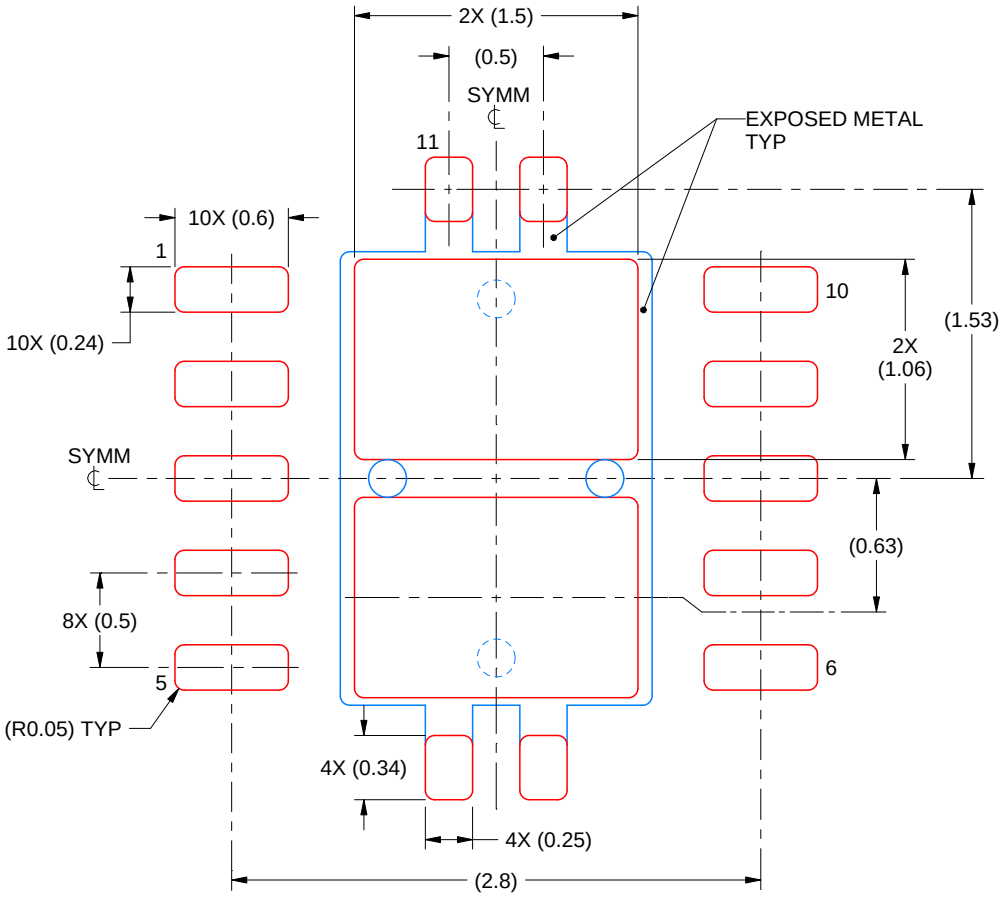
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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