INA28x-Q1 Automotive Grade, –14-V to +80-V, Bidirectional, High Accuracy, Low- or High-Side, Voltage Output, Current Shunt Monitor

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Wide Common-Mode Range: –14 V to +80 V
- Offset Voltage: ±20 µV
- CMRR: 140 dB
- Accuracy:
  - ±1.4% Gain Error (Maximum)
  - 0.3 µV/°C Offset Drift
  - 0.005%/°C Gain Drift (Maximum)
- Available Gains:
  - 50 V/V: INA282-Q1
  - 100 V/V: INA286-Q1
  - 200 V/V: INA283-Q1
  - 500 V/V: INA284-Q1
  - 1000 V/V: INA285-Q1
- Quiescent Current: 900 µA (Maximum)

2 Applications

- EV and HEV Battery Management
- EV and HEV Chargers
- Electric Power Steering (EPS) Systems
- Body Control Modules
- Brake Systems
- Electronic Stability Control (ESC) Systems

3 Description

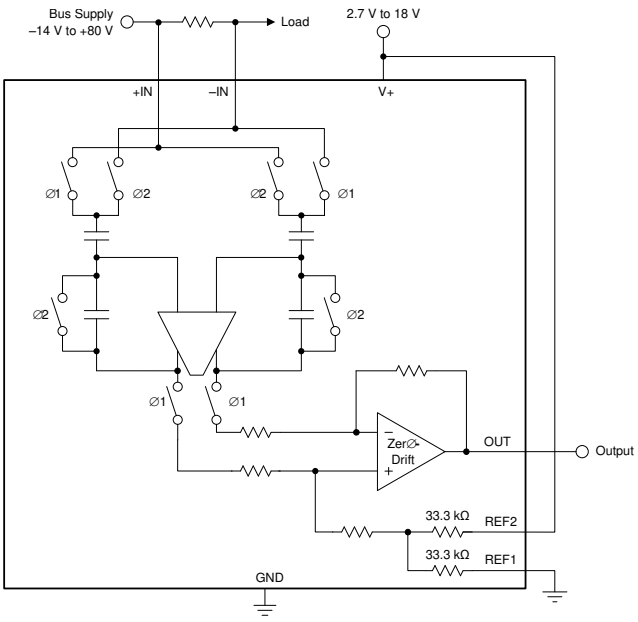
The INA28x-Q1 family includes the INA282-Q1, INA283-Q1, INA284-Q1, INA285-Q1, and INA286-Q1 devices. These devices are voltage output current shunt monitors that can sense drops across shunts at common-mode voltages from –14 V to +80 V, independent of the supply voltage. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10 mV full-scale.

These current sense amplifiers operate from a single 2.7-V to 18-V supply, drawing a maximum of 900 µA of supply current. These devices are specified over the extended operating temperature range of –40°C to +125°C, and offered in SOIC-8 and VSSOP-8 packages.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA28x-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Detailed Block Diagram

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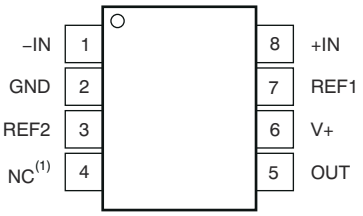
4 Revision History

Changes from Revision B (December 2015) to Revision C (January 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added Functional-Safety Capable bullets	1

Changes from Revision A (July 2015) to Revision B (December 2015)	Page
• Changed VSSOP package from product preview to production data	1

Changes from Revision * (March 2012) to Revision A (May 2015)	Page
• Changed data sheet title from *High-Accuracy, Wide Common-Mode Range, Bi-Directional CURRENT SHUNT MONITOR Zerø-Drift Series* to *INA28x-Q1 Automotive Grade, –14-V to 80-V, Bidirectional, High Accuracy, Low- or High-Side, Voltage Output Current Shunt Monitor*	1
• Added DGK (VSSOP) package to data sheet	1
• Changed *Applications*	1
• Changed front page diagram	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	3
• Added RVRR as symbol for reference rejection ratio	5
• Changed order of figures in *Typical Characteristics* section	7
• Changed Figure 6-16	7
• Changed V_{DRIVE} condition in Figure 6-20 and Figure 6-21	7
• Added functional block diagram	13
• Changed Figure 7-1 and Figure 7-2	15
• Changed Figure 7-3 and Figure 7-4	16
• Changed Figure 7-5 and Figure 7-6	16
• Changed Figure 7-7	17
• Changed *Reference Common-Mode Rejection* to *Reference Voltage Rejection Ratio*	18
• Changed R_{CMR} to RVRR in Table 7-1 and Table 7-2	19
• Changed Figure 8-1	20
• Changed Figure 8-2	21
• Changed Figure 8-4	23

5 Pin Configuration and Functions



A. NC: This pin is not internally connected. The NC pin should either be left floating or connected to GND.

Figure 5-1. D and DGK Package 8-Pin SOIC and VSSOP Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	–IN	Analog input	Connection to negative side of shunt resistor.
2	GND	Analog	Ground
3	REF2	Analog input	Reference voltage, 0 V to V+. See Section 7.4.1 for connection options.
4	NC	—	This pin is not internally connected. The NC pin should either be left floating or connected to GND.
5	OUT	Analog output	Output voltage
6	V+	Analog	Power supply, 2.7 V to 18 V
7	REF1	Analog input	Reference voltage, 0 V to V+. See Section 7.4.1 for connection options.
8	+IN	Analog input	Connection to positive side of shunt resistor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage, V+			18	V
Analog inputs, V_{+IN}, $V_{–IN}$ (2)	Differential (V_{+IN}) – ($V_{–IN}$)(3)	–5	5	V
	Common-Mode	–14	80	V
REF1, REF2, OUT		GND–0.3	(V+) + 0.3	V
Input current into any pin			5	mA
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{+IN} and $V_{–IN}$ are the voltages at the +IN and –IN pins, respectively.
(3) Input voltages must not exceed common-mode rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V+	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA28x-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.9	164.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.9	56.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.3	85.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.9	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	83.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset Voltage, RTI[1]	V_{SENSE} = 0 mV			±20	±70	µV
dV_{OS}/dT	vs Temperature	T_A = –40°C to 125°C			±0.3	±1.5	µV/°C
PSRR	vs Power Supply	V_S = 2.7 V to 18 V, V_{SENSE} = 0 mV			3		µV/V
V_{CM}	Common-Mode Input Range	T_A = –40°C to 125°C		–14		+80	V
CMRR	Common-Mode Rejection	V_{+IN} = –14 V to 80 V, V_{SENSE} = 0 mV T_A = –40°C to 125°C		120	140		dB
I_B	Input Bias Current per Pin[2]	V_{SENSE} = 0 mV			25		µA
I_{OS}	Input Offset Current	V_{SENSE} = 0 mV			1		µA
	Differential Input Impedance				6		kΩ
REFERENCE INPUTS							
	Reference Input Gain				1		V/V
	Reference Input Voltage Range[3]			0		V_{GND} + 9	V
	Divider Accuracy[4]				±0.2%	±0.5%	
RVRR	Reference Voltage Rejection Ratio ($V_{REF}1$ = $V_{REF}2$ = 40 mV to 9 V, V+ = 18 V)	INA282-Q1			±25	±75	µV/V
			T_A = –40°C to 125°C		0.055		µV/V/°C
		INA283-Q1			±13	±30	µV/V
			T_A = –40°C to 125°C		0.040		µV/V/°C
		INA284-Q1			±6	±25	µV/V
			T_A = –40°C to 125°C		0.015		µV/V/°C
		INA285-Q1			±4	±10	µV/V
			T_A = –40°C to 125°C		0.010		µV/V/°C
		INA286-Q1			±17	±45	µV/V
			T_A = –40°C to 125°C		0.040		µV/V/°C
GAIN [6] **(GND + 0.5 V ≤ V_{OUT} ≤ (V+) – 0.5 V; V_{REF1} = V_{REF2} = (V+) / 2 for all devices)**							
G	Gain	INA282-Q1, V+ = 5 V			50		V/V
		INA283-Q1, V+ = 5 V			200		V/V
		INA284-Q1, V+ = 5 V			500		V/V
		INA285-Q1, V+ = 5 V			1000		V/V
		INA286-Q1, V+ = 5 V			100		V/V
	Gain Error	INA282-Q1, INA283-Q1, INA286-Q1			±0.4%	±1.4%	
		INA284-Q1, INA285-Q1			±0.4%	±1.6%	
		T_A = –40°C to 125°C			0.0008	0.005	%/°C

at T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Nonlinearity Error			±0.01%		
	Output Impedance			1.5		Ω
	Maximum Capacitive Load	No sustained oscillation		1		nF
VOLTAGE OUTPUT (5)						
	Swing to V+ Power-Supply Rail	V+ = 5 V, R_{LOAD} = 10 kΩ to GND T_A = –40°C to 125°C		(V+)–0.17	(V+)–0.4	V
	Swing to GND	T_A = –40°C to 125°C		GND+0.015	GND+0.04	V
FREQUENCY RESPONSE						
BW	Effective Bandwidth(7)	INA282-Q1		10		kHz
		INA283-Q1		10		
		INA284-Q1		4		
		INA285-Q1		2		
		INA286-Q1		10		
NOISE, RTI (1)						
	Voltage Noise Density	1 kHz		110		nV/√Hz
POWER SUPPLY						
V_S	Specified Voltage Range	T_A = –40°C to 125°C	2.7		18	V
I_Q	Quiescent Current			600	900	µA
TEMPERATURE RANGE						
Specified Range			–40		125	°C

(1) RTI = referred-to-input.
(2) See typical characteristic graph Figure 6-7 .
(3) The average of the voltage on pins REF1 and REF2 must be between V_{GND} and the lesser of (V_{GND}+9 V) and V+.
(4) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 7-5.
(5) See typical characteristic graphs Figure 6-16 through Figure 6-18.
(6) See typical characteristic graph Figure 6-12.
(7) See typical characteristic graph Figure 6-1 and Section 7.3.2 in the Applications Information.

6.6 Typical Characteristics

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

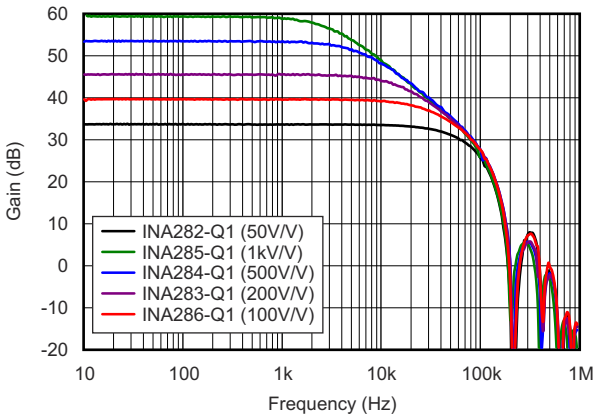


Figure 6-1. Gain vs Frequency

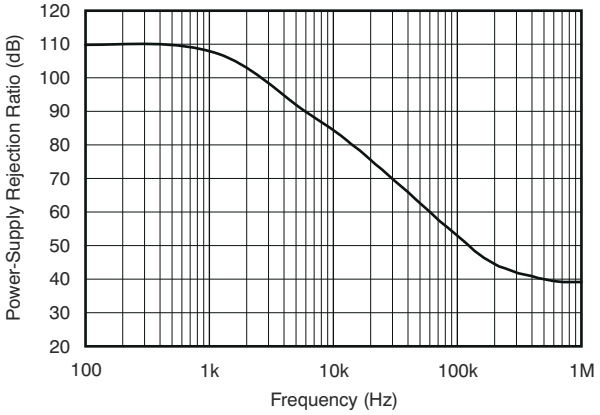


Figure 6-2. INA282-Q1 PSRR (RTI) vs Frequency

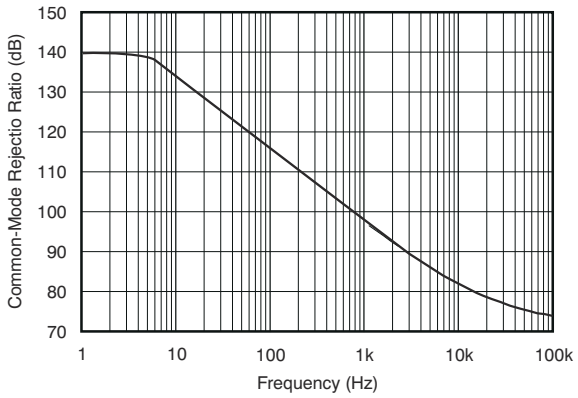


Figure 6-3. INA284-Q1 Common-Mode Rejection Ratio (RTI)

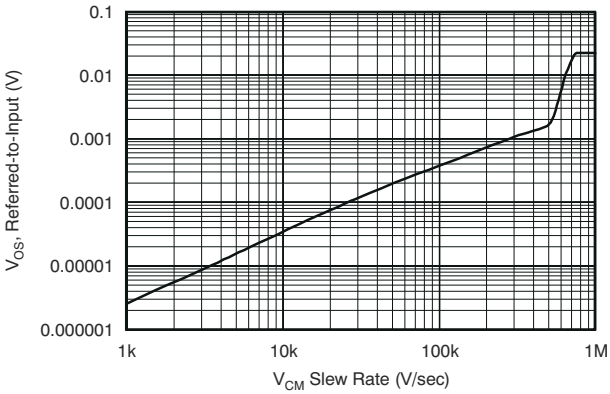


Figure 6-4. INA282-Q1 Common-Mode Slew Rate Induced Offset

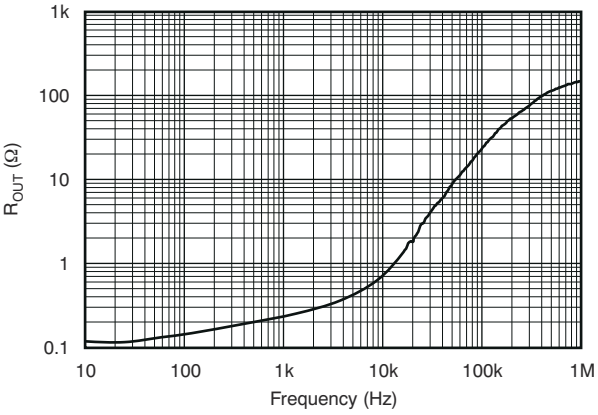


Figure 6-5. INA286-Q1 Output Impedance vs Frequency

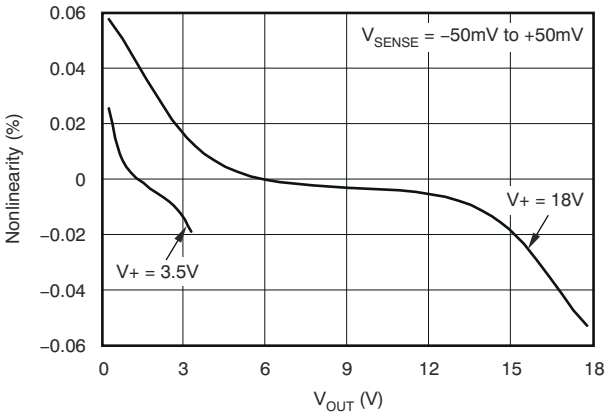


Figure 6-6. INA282-Q1 Typical Nonlinearity vs Output Voltage

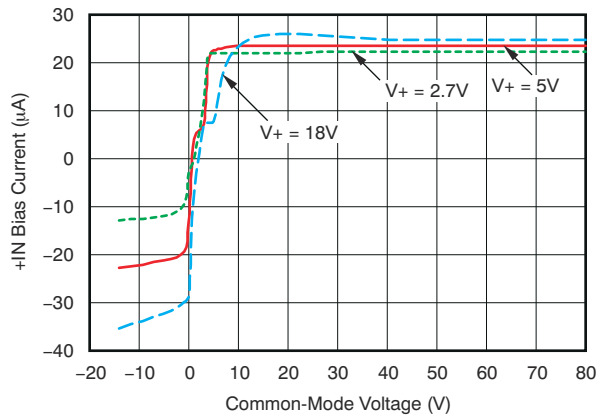


Figure 6-7. INA283-Q1 +IN BIAS Current vs Common-Mode Voltage

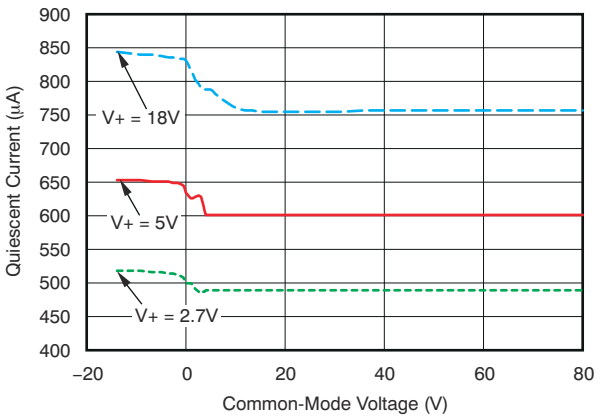


Figure 6-8. INA283-Q1 Quiescent Current vs Common-Mode Voltage

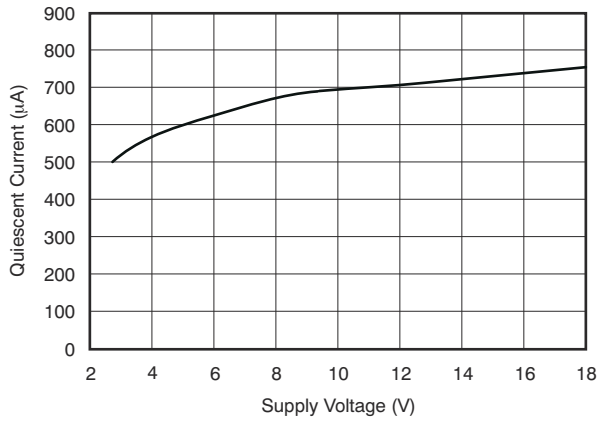


Figure 6-9. Quiescent Current vs Supply Voltage

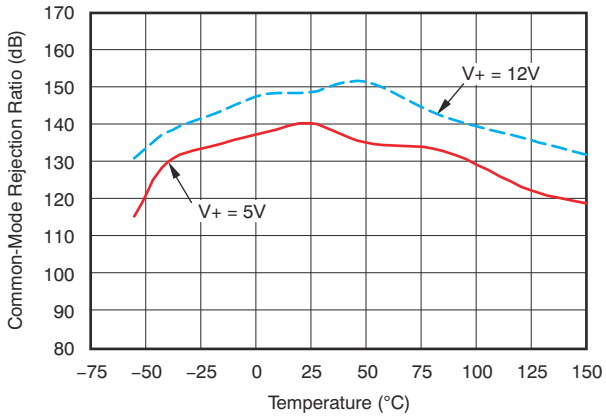


Figure 6-10. Common-Mode Rejection Ratio vs Temperature

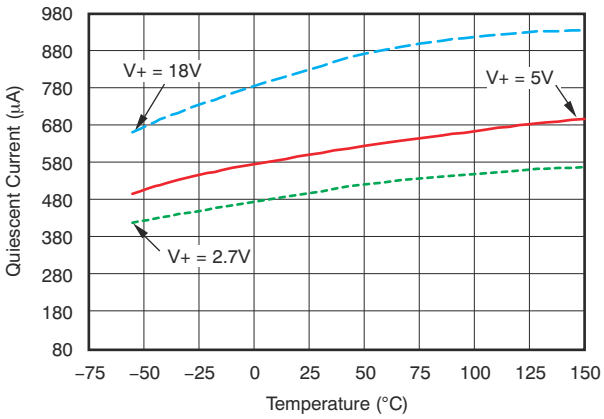


Figure 6-11. Quiescent Current vs Temperature

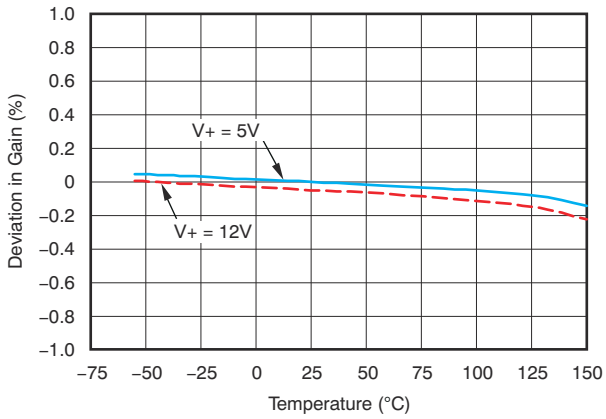


Figure 6-12. Deviation in Gain vs Temperature

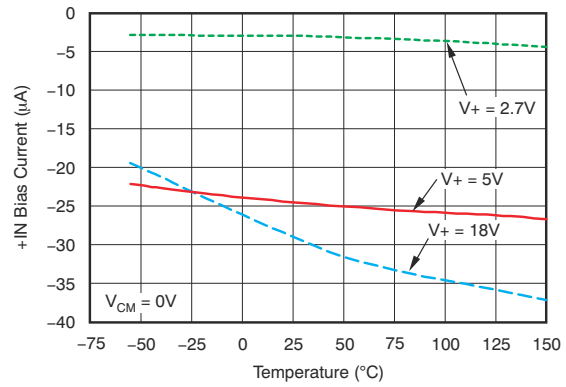


Figure 6-13. +IN BIAS Current vs Temperature

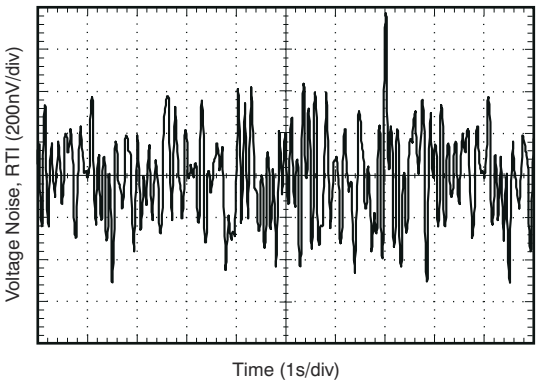


Figure 6-14. INA282-Q1 0.1-Hz to 10-Hz Voltage Noise, RTI

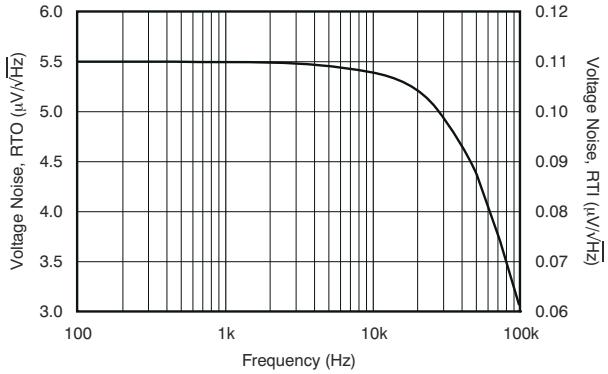


Figure 6-15. INA282-Q1 Voltage Noise vs Frequency

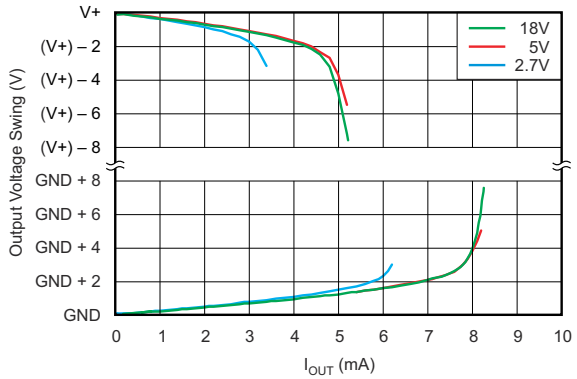


Figure 6-16. INA284-Q1 Output Voltage Swing vs Output Current

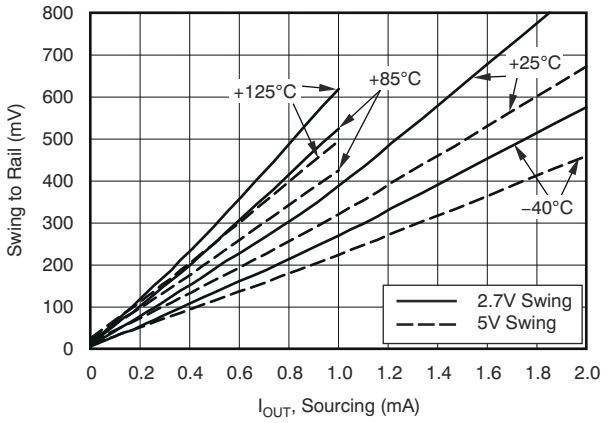


Figure 6-17. INA283-Q1 Swing to Rail vs Output Current

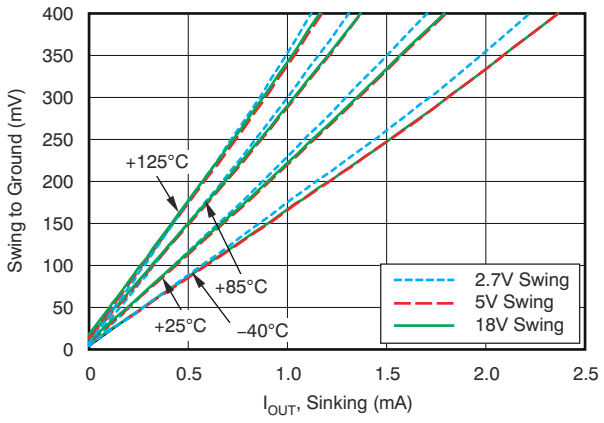


Figure 6-18. INA283-Q1 Swing to Ground vs Output Current

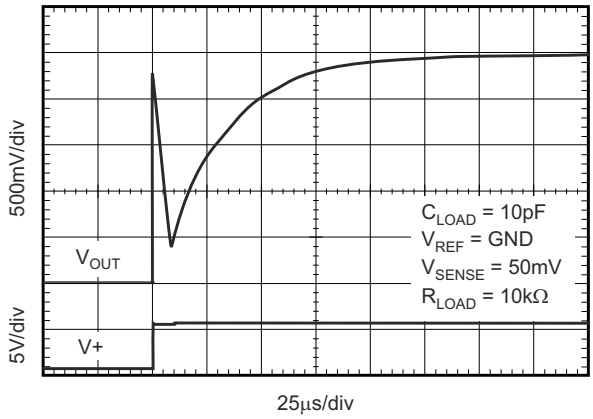


Figure 6-19. Start-Up Transient Response

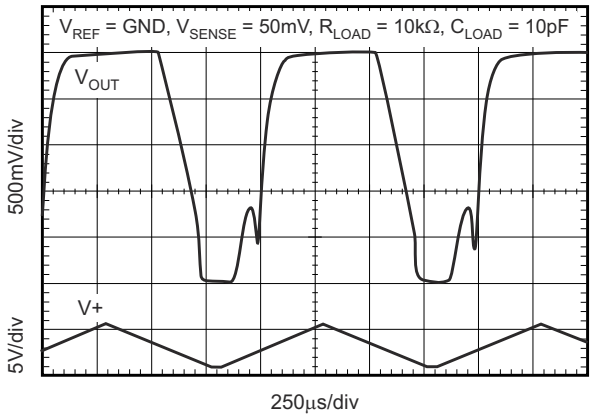


Figure 6-20. Start-Up Transient Response

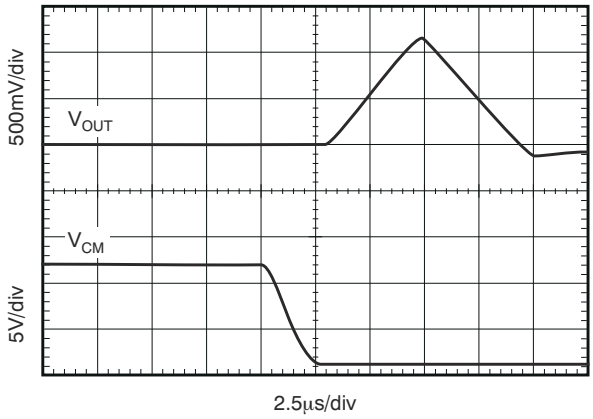


Figure 6-21. 12-V Common-Mode Step Response

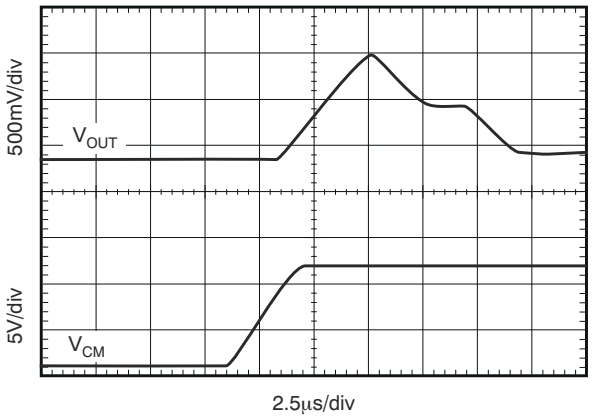


Figure 6-22. 12-V Common-Mode Step Response

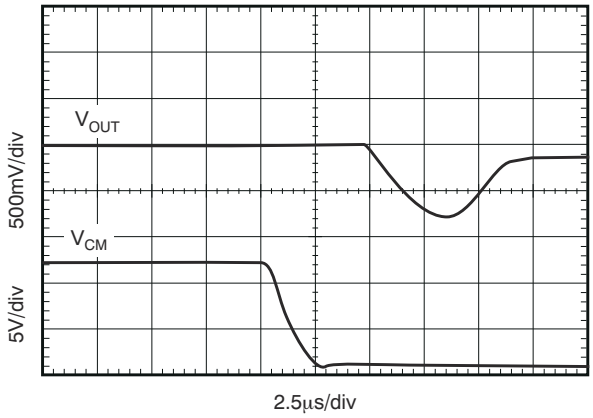


Figure 6-23. 12-V Common-Mode Step Response

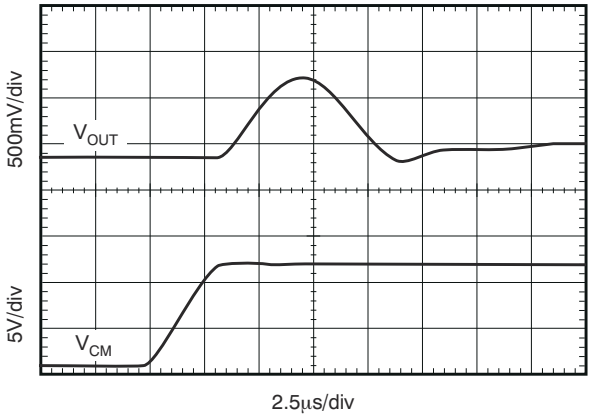


Figure 6-24. 12-V Common-Mode Step Response

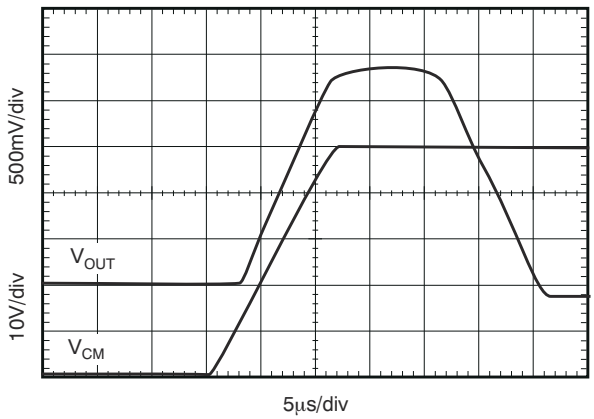


Figure 6-25. 50-V Common-Mode Step Response

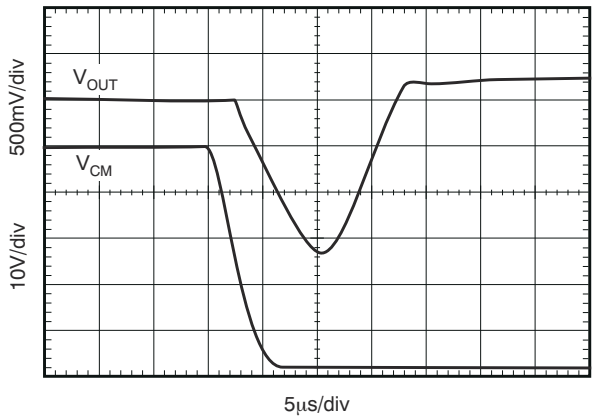


Figure 6-26. 50-V Common-Mode Step Response

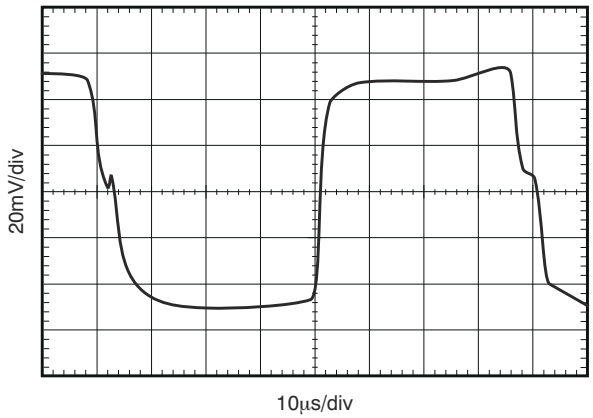


Figure 6-27. 100-mV Step Response

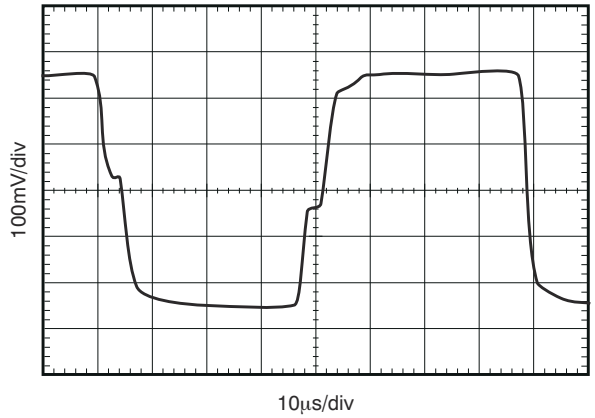


Figure 6-28. 500-mV Step Response

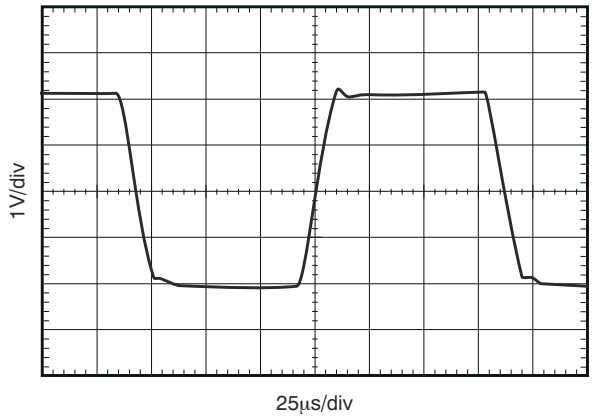


Figure 6-29. 4-V Step Response

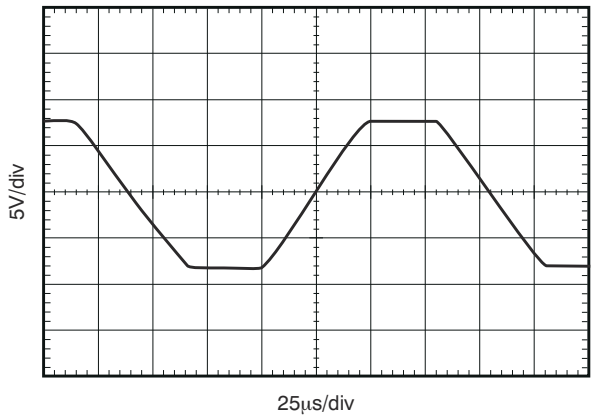


Figure 6-30. 17-V Step Response

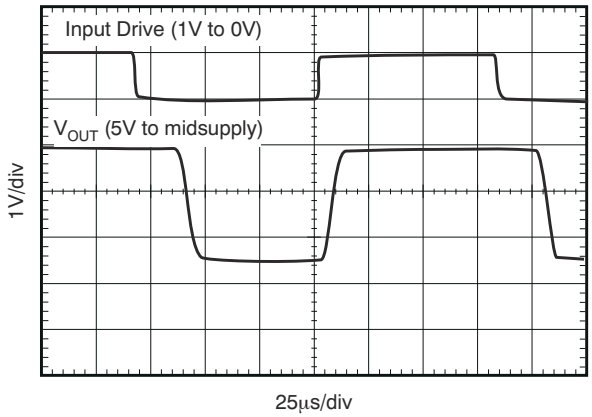


Figure 6-31. Input Overload

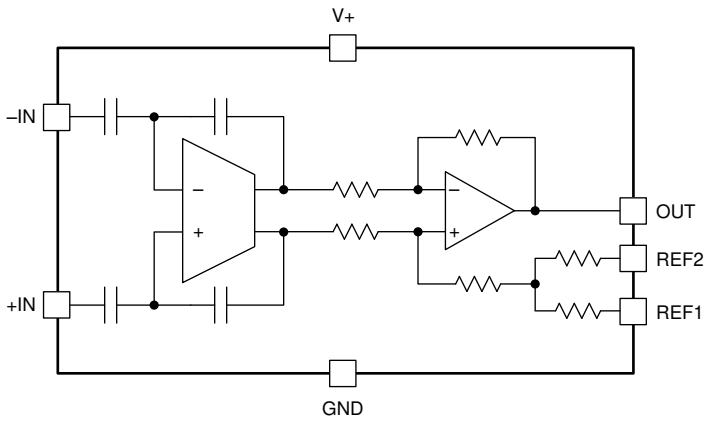
7 Detailed Description

7.1 Overview

The INA28x-Q1 family of voltage output current-sensing amplifiers are specifically designed to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the devices. This family features a common-mode range that extends 14 V less than the negative supply rail, as well as up to 80 V, allowing for either low-side or high-side current sensing while the device is powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 70 µV with a maximum temperature contribution of 1.5 µV/°C over the full temperature range of –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Selecting R_S

The zero-drift offset performance of the INA28x-Q1 family offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, nonzero-drift, current-shunt monitors typically require a full-scale range of 100 mV. The INA28x-Q1 family gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude, with many additional benefits. Alternatively, applications that must measure current over a wide dynamic range can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the INA282-Q1, INA286-Q1, or INA283-Q1 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA282-Q1 operating on a 3.3-V supply can easily handle a full-scale shunt drop of 55 mV, with only 70 µV of offset.

7.3.2 Effective Bandwidth

The extremely high DC CMRR of the INA28x-Q1 results from the switched capacitor input structure. Because of this architecture, the INA28x-Q1 exhibits discrete time system behaviors as illustrated in the gain versus frequency graph of Figure 6-3 and the step response curves of Figure 6-21 through Figure 6-28. The response to a step input depends somewhat on the phase of the internal INA28x-Q1 clock when the input step occurs. It is possible to overload the input amplifier with a rapid change in input common-mode voltage (see Figure 6-4). Errors as a result of common-mode voltage steps and/or overload situations typically disappear within 15 µs after the disturbance is removed.

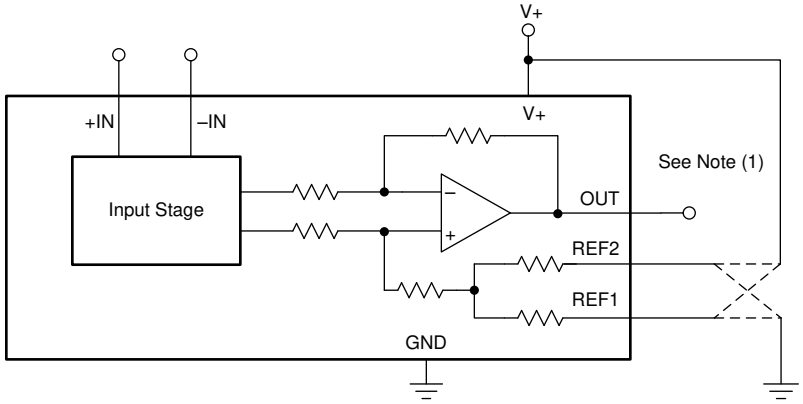
7.3.3 Transient Protection

The –14-V to 80-V common-mode range of the INA28x-Q1 is ideal for withstanding automotive fault conditions that range from 12-V battery reversal up to 80-V transients; no additional protective components are needed up to those levels. In the event that the INA28x-Q1 is exposed to transients on the inputs in excess of its ratings, then external transient absorption with semiconductor transient absorbers (Zener or *Transzorbs*) will be necessary. Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it cannot allow the INA28x-Q1 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage as a result of transient absorber dynamic impedance). Despite the use of internal zener-type electrostatic discharge (ESD) protection, the INA28x-Q1 does not lend itself to using external resistors in series with the inputs without degrading gain accuracy.

7.4 Device Functional Modes

7.4.1 Reference Pin Connection Options

Figure 7-1 illustrates a test circuit for reference divider accuracy. The output of the INA28x-Q1 can be connected for unidirectional or bidirectional operation. Neither the REF1 pin nor the REF2 pin may be connected to any voltage source lower than GND or higher than V+, and that the effective reference voltage (REF1 + REF2)/2 must be 9 V or less. This parameter means that the V+ reference output connection shown in Figure 7-3 is not allowed for V+ greater than 9 V. However, the split-supply reference connection shown in Figure 7-5 is allowed for all values of V+ up to 18 V.



A. Reference divider accuracy is determined by measuring the output with the reference voltage applied to alternate reference resistors, and calculating a result such that the amplifier offset is cancelled in the final measurement.

Figure 7-1. Test Circuit for Reference Divider Accuracy

7.4.1.1 Unidirectional Operation

Unidirectional operation allows the INA28x-Q1 to measure currents through a resistive shunt in one direction. In the case of unidirectional operation, the output could be set at the negative rail (near ground, and the most common connection) or at the positive rail (near V+) when the differential input is 0V. The output moves to the opposite rail when a correct polarity differential input voltage is applied.

The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to move the output down. If the output is set at ground, the polarity is positive to move the output up.

The following sections describe how to configure the output for unidirectional operation.

7.4.1.1.1 Ground Referenced Output

When using the INA28x-Q1 in this mode, both reference inputs are connected to ground; this configuration takes the output to the negative rail when there is 0V differential at the input (as Figure 7-2 shows).

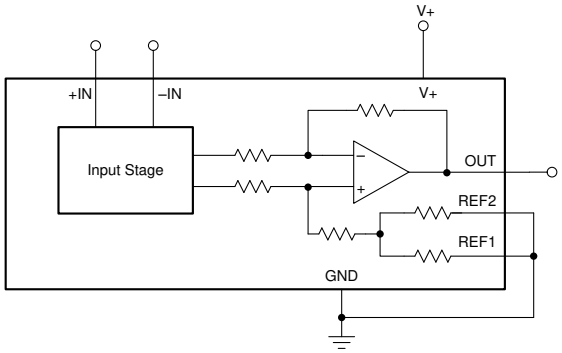


Figure 7-2. Ground Referenced Output

7.4.1.1.2 V+ Referenced Output

This mode is set when both reference pins are connected to the positive supply. It is typically used when a diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (as shown in Figure 7-3).

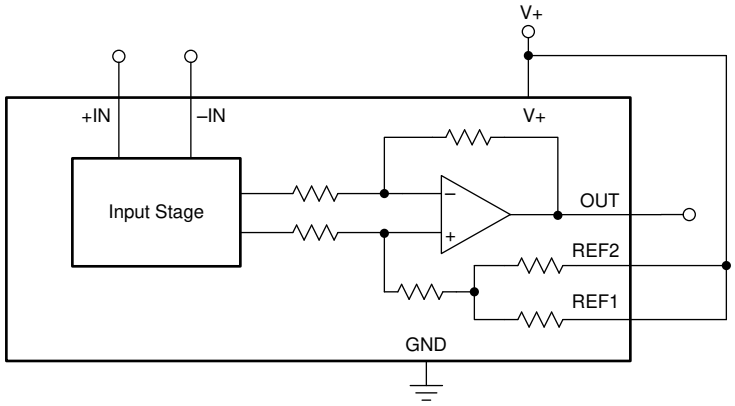


Figure 7-3. V+ Referenced Output

7.4.1.2 Bidirectional Operation

Bidirectional operation allows the INA28x-Q1 to measure currents through a resistive shunt in two directions. In this case, the output can be set anywhere within the limits of what the reference inputs allow (that is, from 0 V to 9 V, but never to exceed the supply voltage). Typically, it is set at half-scale for equal range in both directions. In some cases, however, it is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

The quiescent output voltage is set by applying voltage(s) to the reference inputs. REF1 and REF2 are connected to internal resistors that connect to an internal offset node. There is no operational difference between the pins.

7.4.1.2.1 External Reference Output

Connecting both pins together and to a reference produces an output at the reference voltage when there is no differential input; this configuration is illustrated in Figure 7-4. The output moves down from the reference voltage when the input is negative relative to the –IN pin and up when the input is positive relative to the –IN pin. This technique is the most accurate way to bias the output to a precise voltage.

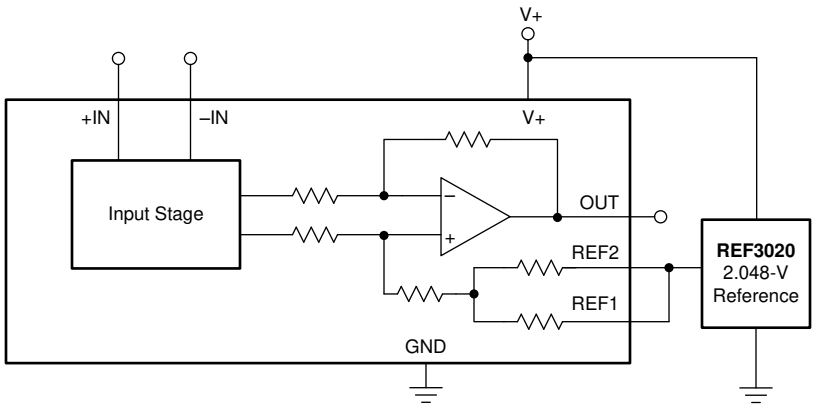


Figure 7-4. External Reference Output

7.4.1.2.2 Splitting the Supply

By connecting one reference pin to V+ and the other to the ground pin, the output is set at half of the supply when there is no differential input, as shown in Figure 7-5. This method creates a midscale offset that is

ratiometric to the supply voltage; thus, if the supply increases or decreases, the output remains at half the supply.

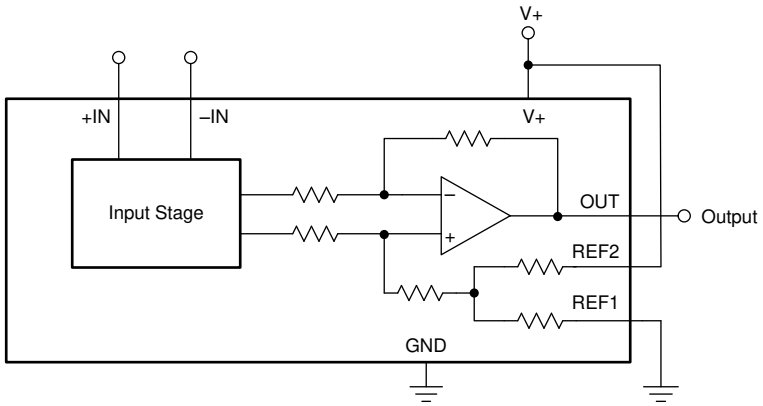


Figure 7-5. Split-Supply Output

7.4.1.2.3 Splitting an External Reference

In this case, an external reference is divided by 2 with an accuracy of approximately 0.5% by connecting one REF pin to ground and the other REF pin to the reference (as Figure 7-6 illustrates).

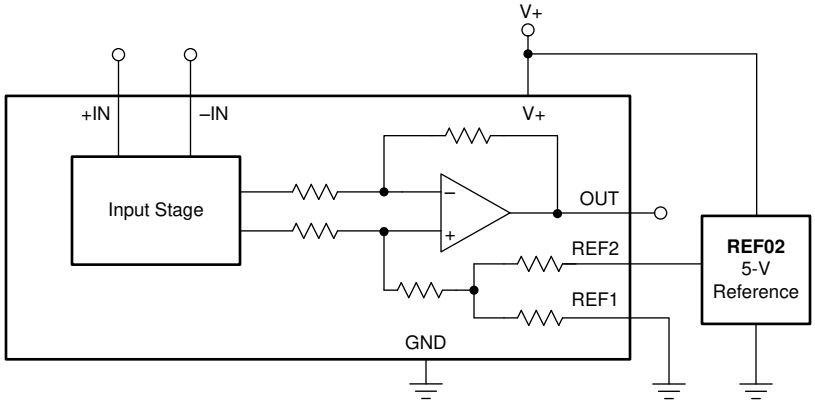


Figure 7-6. Split Reference Output

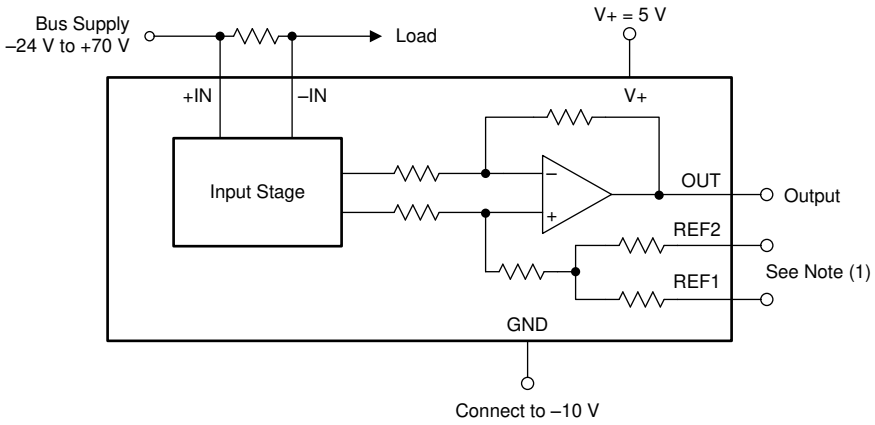
7.4.2 Shutdown

While the INA28x-Q1 family does not provide a shutdown pin, the quiescent current of 600 µA enables the device to be powered from the output of a logic gate. Take the gate low to shut down the INA28x-Q1 family devices.

7.4.3 Extended Negative Common-Mode Range

Using a negative power supply can extend the common-mode range 14 V more negative than the supply used. For instance, a –10 V supply allows up to –24-V negative common-mode. Remember to keep the total voltage between the GND pin and V+ pin to less than 18 V. The positive common-mode decreases by the same amount.

The reference input simplifies this type of operation because the output quiescent bias point is always based on the reference connections. Figure 7-7 shows a circuit configuration for common-mode ranges from –24 V to 70 V.



A. Connect the REF pins as desired; however, they cannot exceed 9 V greater than the GND pin voltage.

Figure 7-7. Circuit Configuration for Common-Mode Ranges from –24 V to 70 V

7.4.4 Calculating Total Error

The electrical specifications for the INA28x-Q1 family of devices include the typical individual errors terms such as gain error, offset error, and nonlinearity error. Total error including all of these individual error components is not specified in Section 6.5. To accurately calculate the expected error of the device, the operating conditions of the device must first be known. Some current shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this one point has little practical value because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources, with information on how to apply them to calculate the total error value for the device under any normal operating conditions.

The typical error sources that have the largest impact on the total error of the device are input offset voltage, common-mode rejection ratio, gain error, and nonlinearity error. For the INA28x-Q1, an additional error source referred to as *reference voltage rejection ratio* is also included in the total error value.

The nonlinearity error of the INA28x-Q1 is relatively low compared to the gain error specification. This low error results in a gain error that can be expected to be relatively constant throughout the linear input range of the device. While the gain error remains constant across the linear input range of the device, the error associated with the input offset voltage does not. As the differential input voltage developed across a shunt resistor at the input of the INA28x-Q1 decreases, the inherent input offset voltage of the device becomes a larger percentage of the measured input signal resulting in an increase in error in the measurement. This varying error is present among all current shunt monitors, given the input offset voltage ratio to the voltage being sensed by the device. The relatively low input offset voltages present in the INA28x-Q1 devices limit the amount of contribution the offset voltage has on the total error term.

The term *reference voltage rejection ratio* refers to the amount of error induced by applying a reference voltage to the INA28x-Q1 device that deviates from the inherent bias voltage present at the output of the first stage of the device. The output of the switched-capacitor network and first-stage amplifier has an inherent bias voltage of approximately 2.048 V. Applying a reference voltage of 2.048 V to the INA28x-Q1 reference pins results in no additional error term contribution. Applying a voltage to the reference pins that differs from 2.048 V creates a voltage potential in the internal difference amplifier, resulting in additional current flowing through the resistor network. As a result of resistor tolerances, this additional current flow causes additional error at the output because of resistor mismatches. Additionally, as a result of resistor tolerances, this additional current flow causes additional error at the output based on the common-mode rejection ratio of the output stage amplifier. This error term is referred back to the input of the device as additional input offset voltage. Increasing the difference between the 2.048-V internal bias and the external reference voltage results in a higher input offset voltage. Also, as the error at the output is referred back to the input, there is a larger impact on the input-referred offset, V_{OS}, for the lower-gain versions of the device.

Two examples are provided that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well, to provide the user more information on how much error variance is present from device to device.

7.4.4.1 Example 1 INA282-Q1

Table 7-1. V+ = 5 V; V_{CM} = 12 V; V_{REF1} = V_{REF2} = 2.048 V; V_{SENSE} = 10 mV

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial input offset voltage	V_{OS}	—	20 µV	70 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \times (V_{CM} - 12V)$	0 µV	0 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times (2.048\ V - V_{REF})$	0 µV	0 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	20 µV	70 µV
Error from input offset voltage	$Error\_V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.20%	0.70%
Gain error	Error_Gain	—	0.40%	1.40%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
Total error	—	$\sqrt{(Error\_V_{OS})^2 + (Error\_Gain)^2 + (Error\_Lin)^2}$	0.45%	1.56%

7.4.4.2 Example 2 INA286-Q1

Table 7-2. V+ = 5 V; V_{CM} = 24 V; V_{REF1} = V_{REF2} = 0 V; V_{SENSE} = 10 mV

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial input offset voltage	V_{OS}	—	20 µV	70 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \times (V_{CM} - 12V)$	1.2 µV	12 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times (2.048\ V - V_{REF})$	34.8 µV	92.2 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	40.2 µV	116.4 µV
Error from input offset voltage	$Error\_V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.40%	1.16%
Gain error	Error_Gain	—	0.40%	1.40%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
Total error	—	$\sqrt{(Error\_V_{OS})^2 + (Error\_Gain)^2 + (Error\_Lin)^2}$	0.57%	1.82%

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INA28x-Q1 family of devices measure the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pins to adjust the functionality of the output signal is shown in multiple configurations.

8.1.1 Basic Connections

Figure 8-1 shows the basic connection of an INA28x-Q1 family device. Connect the input pins, +IN and –IN, as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

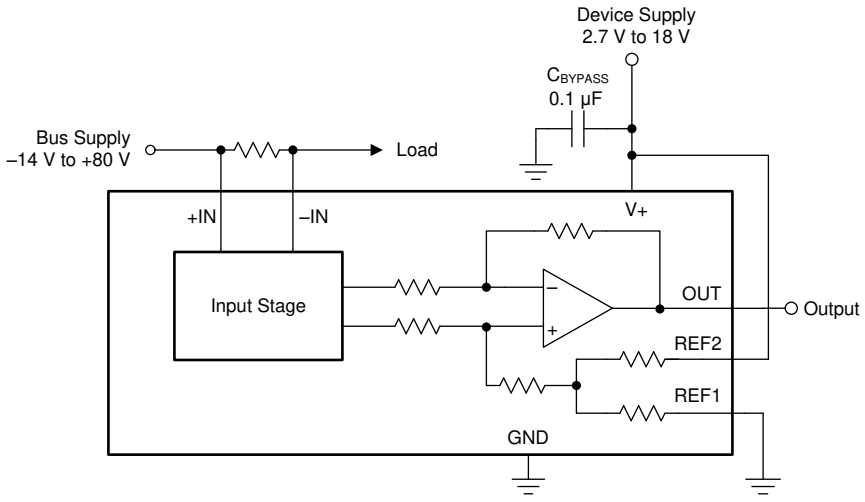


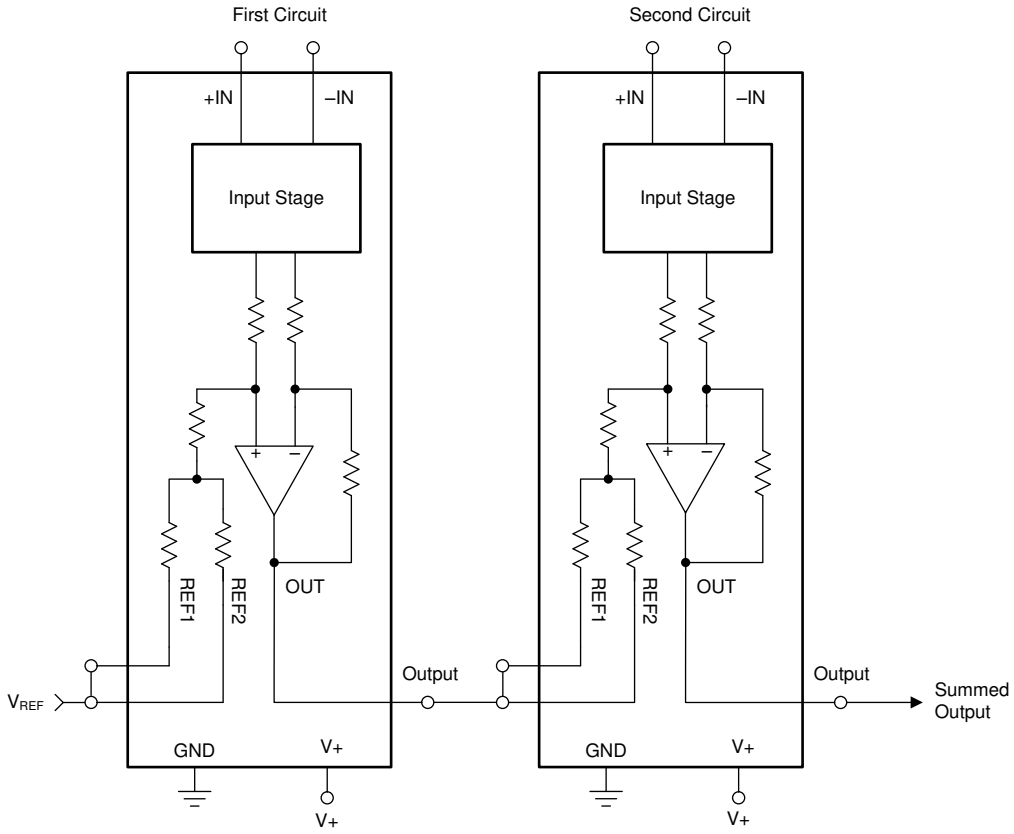
Figure 8-1. Basic Connections

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

8.2 Typical Applications

8.2.1 Current Summing

The outputs of multiple INA28x-Q1 family devices are easily summed by connecting the output of one INA28x-Q1 family device to the reference input of a second INA28x-Q1 family device. The circuit configuration shown in Figure 8-1 is an easy way to achieve current summing.



NOTE: The voltage applied to the reference inputs must not exceed 9 V.

Figure 8-2. Summing the Outputs of Multiple INA28x-Q1 Family Devices

8.2.1.1 Design Requirements

In order to sum multiple load currents, multiple INA28x-Q1 devices must be connected. Figure 8-2 shows summing for two devices. Summing beyond two devices is possible by repeating this connection. The reference input of the first INA28x-Q1 family device sets the output quiescent level for all the devices in the string.

8.2.1.2 Detailed Design Procedures

Connect the output of one INA28x-Q1 family device to the reference input of the next INA28x-Q1 family device in the chain. Use the reference input of the first circuit to set the reference of the final summed output. The currents sensed at each circuit in the chain are summed at the output of the last device in the chain.

8.2.1.3 Application Curve

Figure 8-3 shows an example output response of a summing configuration. The reference pins of the first circuit are connected to ground, and sine waves at different frequencies are applied to the two circuits to produce a summed output as shown. The sine wave voltage input for the first circuit is offset so that the whole wave is above GND.

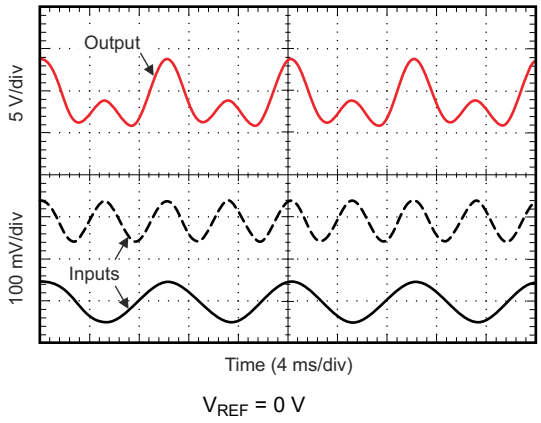
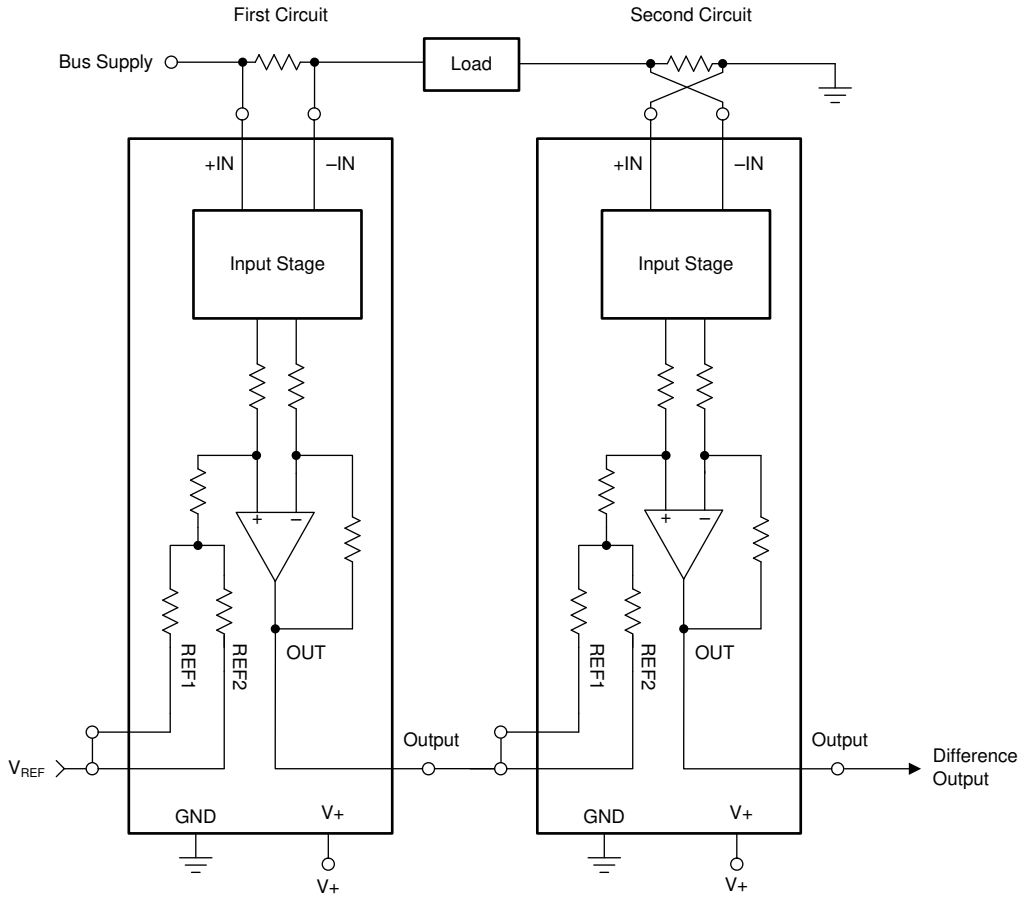


Figure 8-3. Current Summing Application Output Response

8.2.2 Current Differencing

Occasionally, the need arises to confirm that the current into a load is identical to the current out of a load, usually as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing except that the two amplifiers have the inputs connected opposite of each other.



NOTE: The voltage applied to the reference inputs must not exceed 9 V.

Figure 8-4. Current Differencing Using an INA28x-Q1 Device

8.2.2.1 Design Requirements

For current differencing, connect two INA28x-Q1 devices, and connect the inputs opposite to each other, as shown in Figure 8-4. The reference input of the first INA28x-Q1 family device sets the output quiescent level for all the devices in the string.

8.2.2.2 Detailed Design Procedure

Connect the output of one INA28x-Q1 family device to the reference input of the second INA28x-Q1 family device. The reference input of the first circuit sets the reference at the output. This circuit example is identical to the current summing example, except that the two shunt inputs are reversed in polarity. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. This current differencing circuit is useful in detecting when current into and out of a load do not match.

8.2.2.3 Application Curve

Figure 8-5 shows an example output response of a difference configuration. The reference pins of the first circuit are connected to a reference voltage of 2.048 V. The inputs to each circuit is a 100-Hz sine wave, 180° out of phase with each other, resulting in a zero output as shown. The sine wave input to the first circuit is offset so that the input wave is completely above GND.

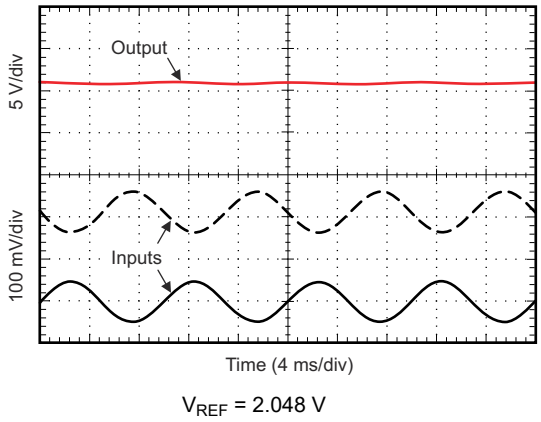


Figure 8-5. Current Differencing Application Output Response

9 Power Supply Recommendations

The INA28x-Q1 can make accurate measurements well outside of its own power-supply voltage, V+, because its inputs (+IN and –IN) may operate anywhere from –14 V to 80 V independent of V+. For example, the V+ power supply can be 5 V while the common-mode voltage being monitored by the shunt may be as high as 80 V. Of course, the output voltage range of the INA28x-Q1 is constrained by the supply voltage that powers it on V+. When the power to the INA28x-Q1 is off (that is, no voltage is supplied to the V+ pin), the input pins (+IN and –IN) are high impedance with respect to ground and typically leak less than ±1 µA over the full common-mode range of –14 V to 80 V.

10 Layout

10.1 Layout Guidelines

Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance causes significant measurement errors.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends a bypass capacitor with a value of 0.1 uF. Add additional decoupling capacitance to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

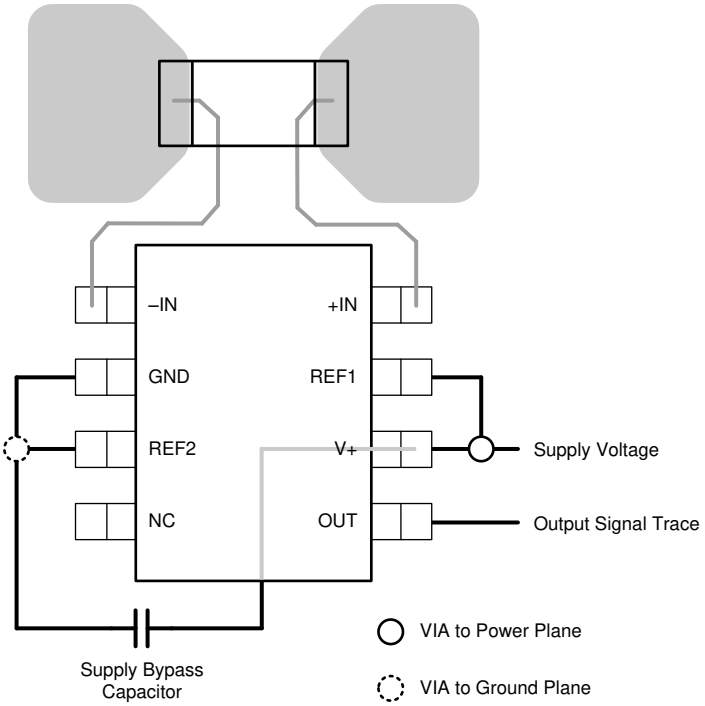


Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA282AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11GF
INA282AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11GF
INA282AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	282Q1
INA282AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	282Q1
INA283AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11FF
INA283AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11FF
INA283AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	283Q1
INA283AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	283Q1
INA284AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11HF
INA284AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11HF
INA284AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	284Q1
INA284AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	284Q1
INA285AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11IF
INA285AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11IF
INA285AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	285Q1
INA285AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	285Q1
INA286AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11JF
INA286AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11JF
INA286AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	286Q1
INA286AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	286Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF INA282-Q1, INA283-Q1, INA284-Q1, INA285-Q1, INA286-Q1 :

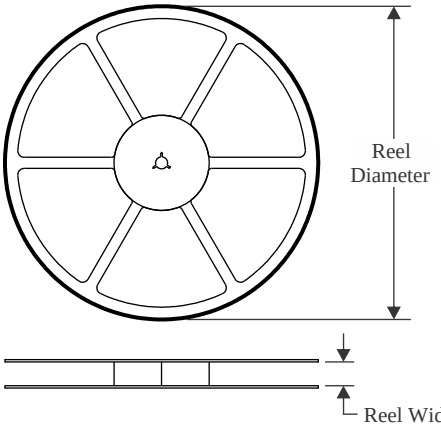
- Catalog : INA282, INA283, INA284, INA285, INA286

NOTE: Qualified Version Definitions:

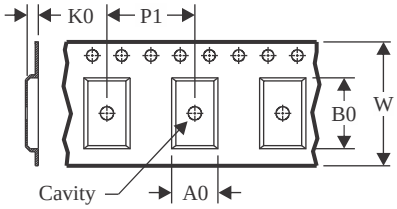
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

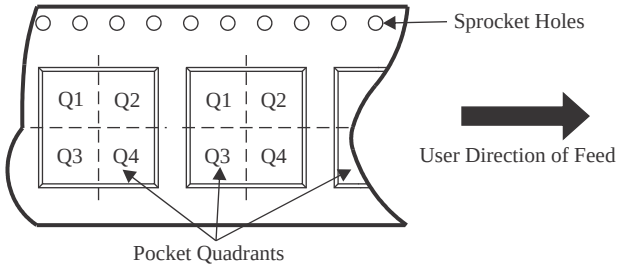


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

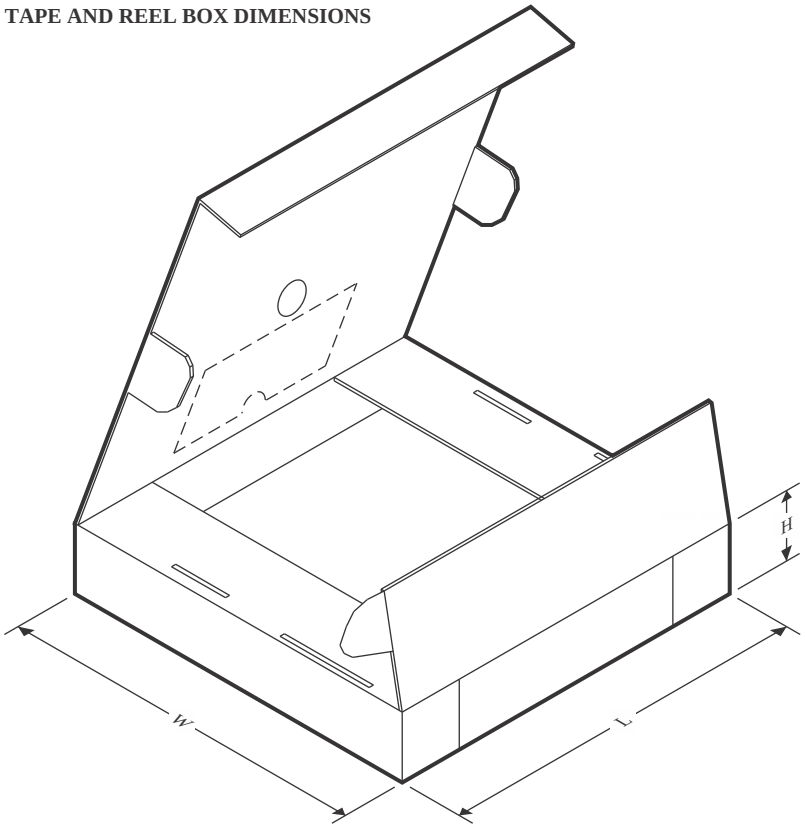
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

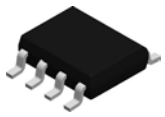
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA282AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA282AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA283AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA283AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA284AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA284AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA285AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA285AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA286AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA286AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA282AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA282AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
INA283AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA283AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
INA284AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA284AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
INA285AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA285AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
INA286AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA286AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

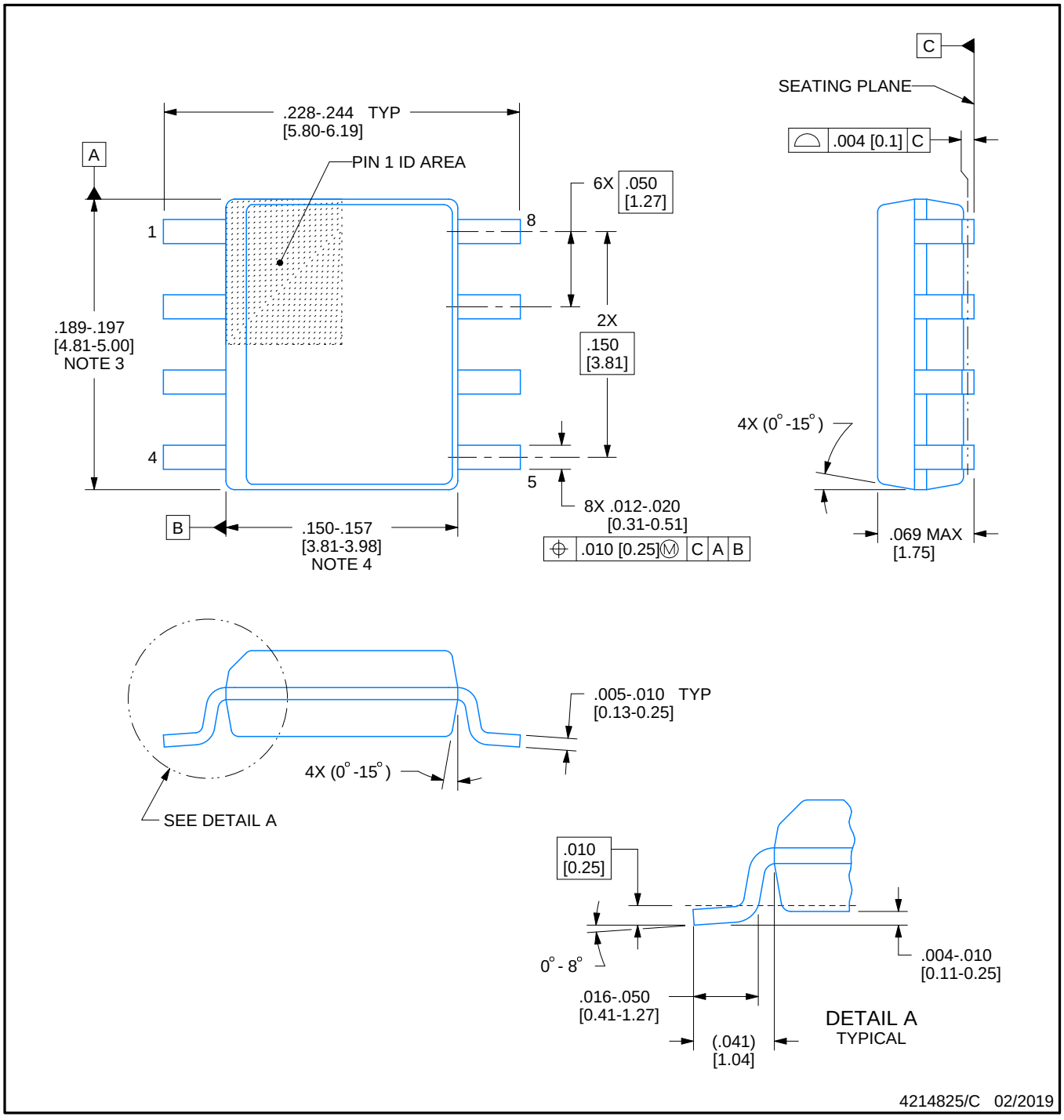


PACKAGE OUTLINE

D0008A

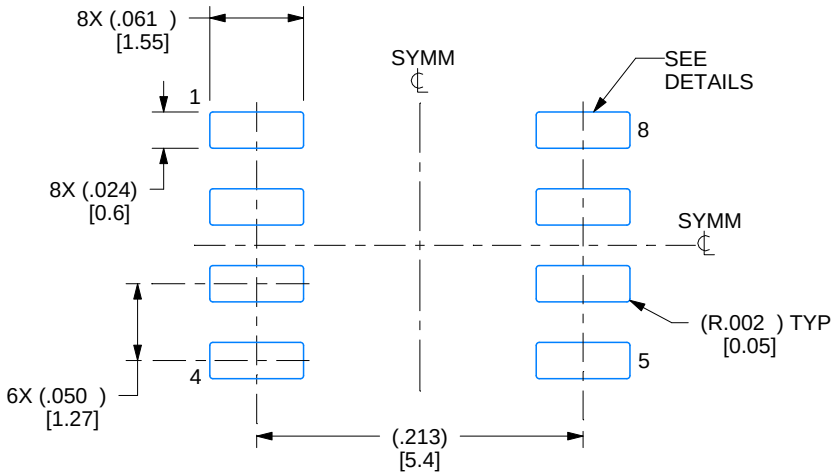
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

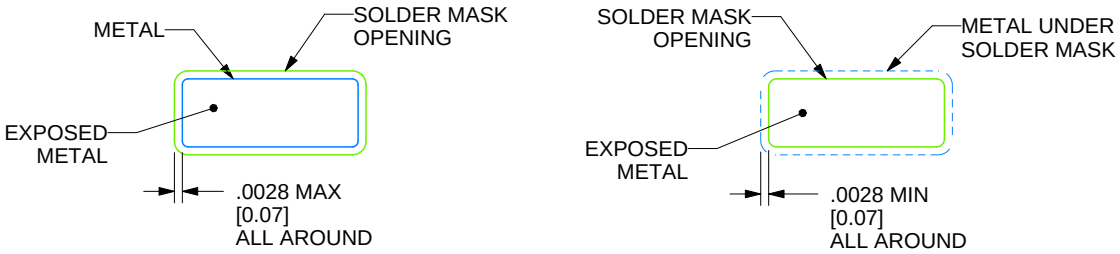


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

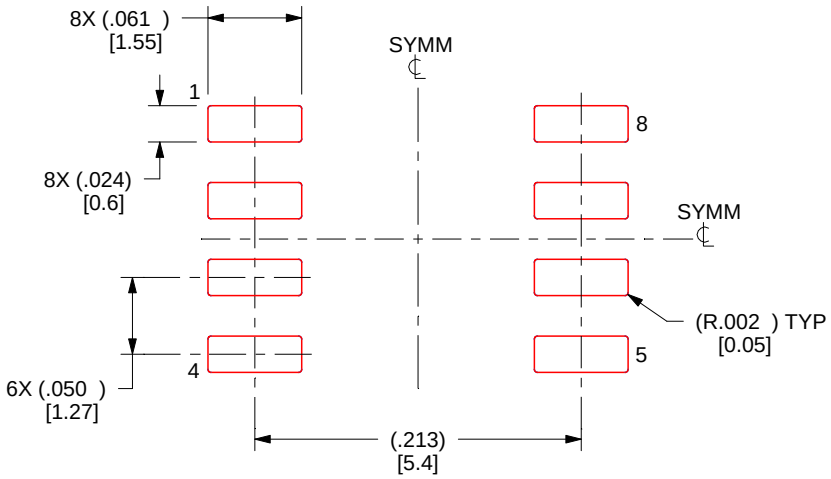
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

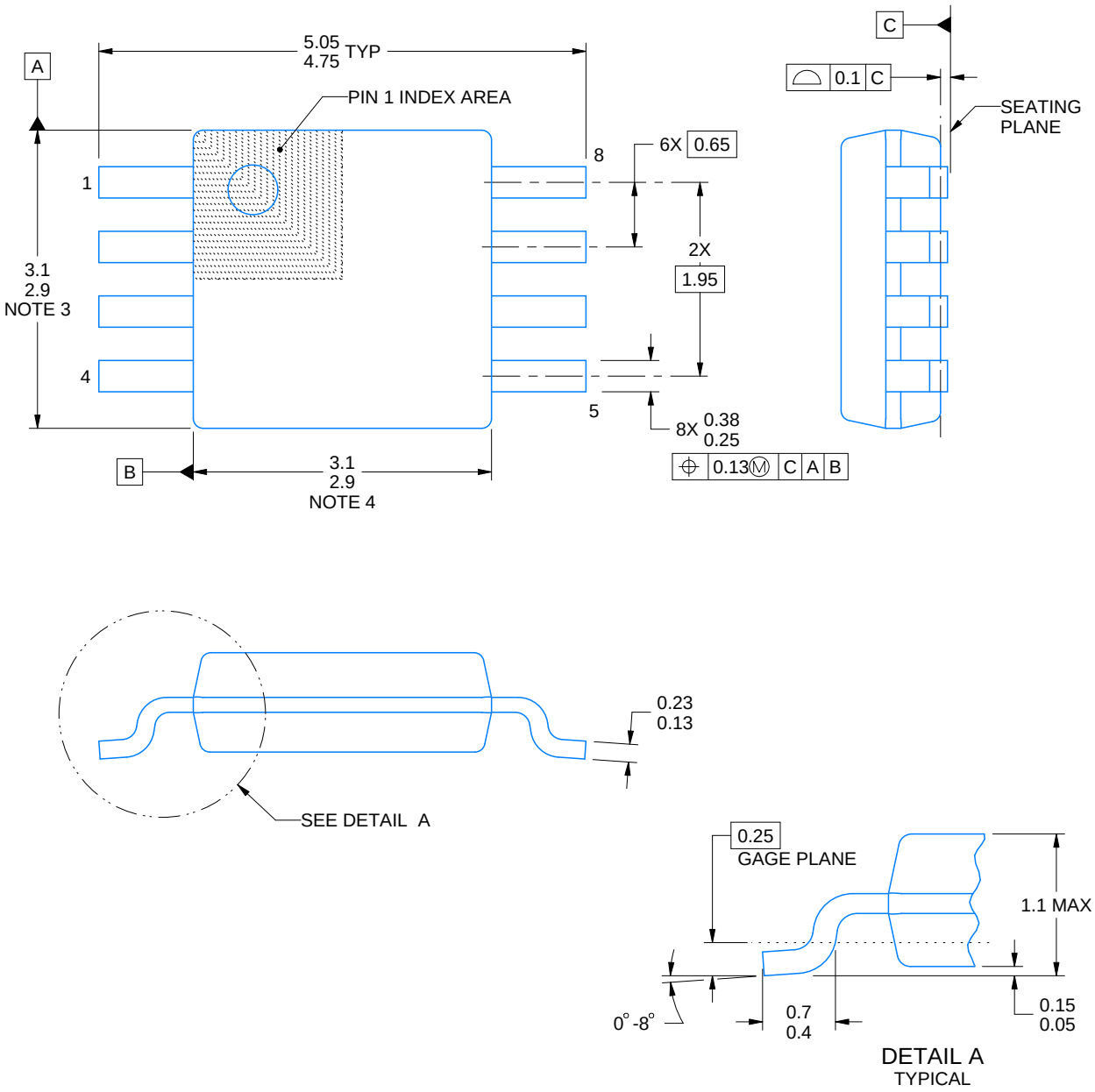
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

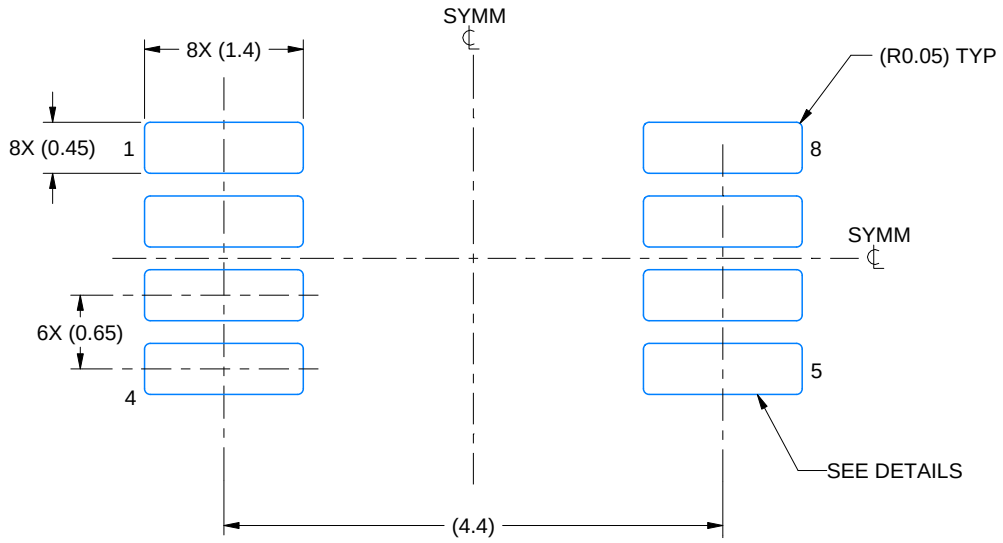
SMALL OUTLINE PACKAGE



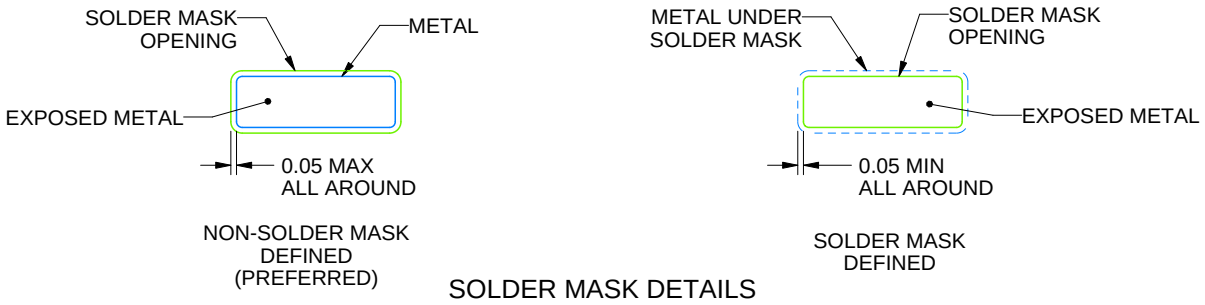
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

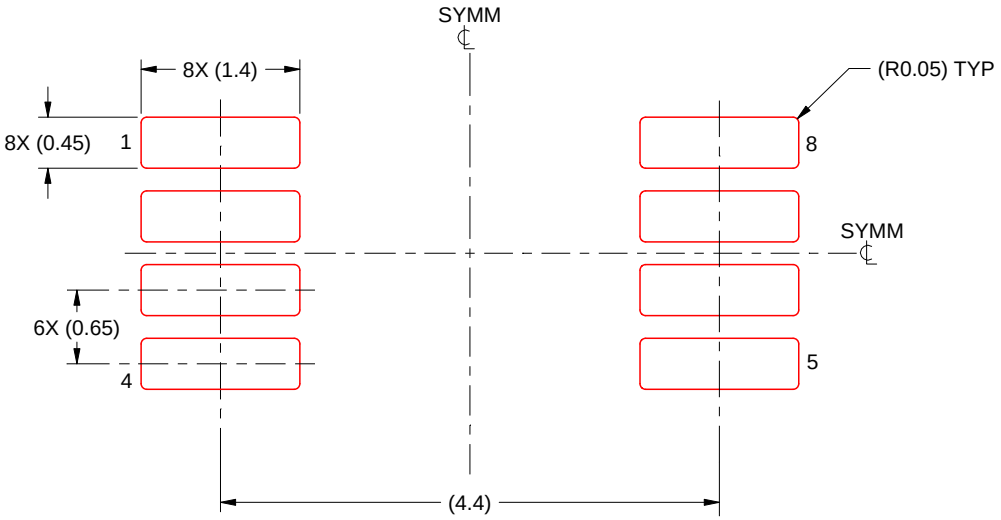


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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