INA2128 Dual, Low-Power Instrumentation Amplifier

1 Features

- Low offset voltage: 50 µV max
- Low drift: 0.5 µV/°C max
- Low input bias current: 5 nA max
- Input voltage noise: 8 nV/√Hz at 1 kHz
- High bandwidth: 1.3 MHz at G=1 V/V
- High CMR: 120 dB min
- Inputs protected to ±40 V
- Wide supply range: ±2.25 V to ±18 V
- Low quiescent current: 700 µA per channel
- Temperature range: –40°C to +85°C
- Package: 16-pin SOIC

2 Applications

- Pressure transmitter
- Temperature transmitter
- Weigh scale
- Electrocardiogram (ECG)
- Analog input module
- Data acquisition (DAQ)

3 Description

The INA2128 is a dual, low-power, general-purpose instrumentation amplifier (IA) offering excellent accuracy. The versatile three-op-amp design and small size make this device an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain (200 kHz at G = 100). A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40 V without damage.

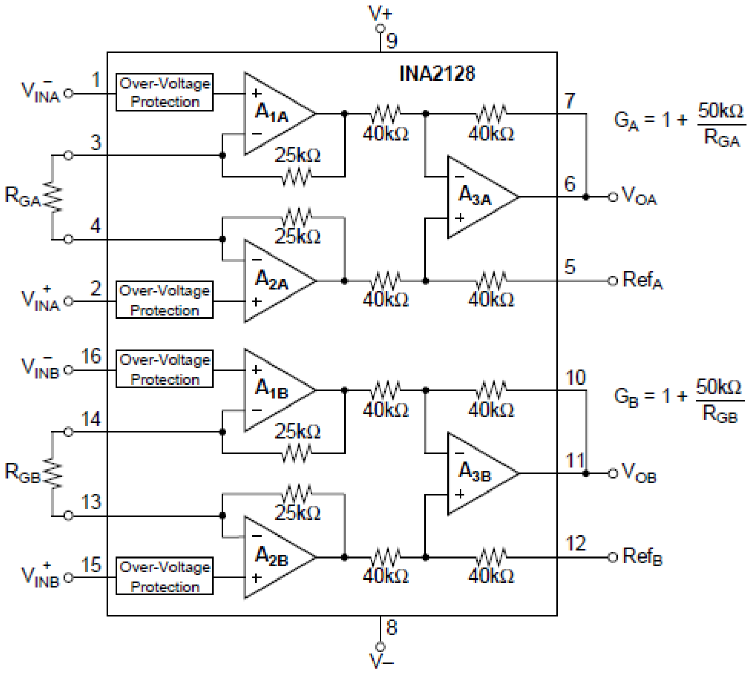
The INA2128 is laser-trimmed for very low offset voltage (50 µV), drift (0.5 µV/°C) and high common-mode rejection (120 dB at G ≥ 100). The device operates with power supplies as low as ±2.25 V, and quiescent current is only 700 µA per IA—a great choice for battery-operated and multiple-channel systems.

The INA2128 is available in an SOIC-16 package, and is specified from –40°C to +85°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA2128	DW (SOIC, 16)	10.3 mm × 10.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2007) to Revision B (May 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document... 1
- Added the *Package Information* table, and the *Pin Configuration and Functions*, *Specifications*, *Detailed Description*, *Application and Implementation*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections...1
- Added input voltage noise, high bandwidth, and temperature range bullets to *Features*...1
- Changed *Features* bullet to show correct package name... 1
- Changed *Applications* bullets to show updated links...1
- Changed Package Information table column name from BODY SIZE (NOM) to PACKAGE SIZE and added note regarding the package size... 1
- Added single supply specification to *Absolute Maximum Ratings*...5
- Added note clarifying output short-circuit to ground in *Absolute Maximum Ratings* refers to short-circuit to VS / 2...5
- Added single supply specification to *Recommended Operating Conditions*...5
- Changed input common-mode voltage range specification from V – 2 to (V–) + 2 in *Recommended Operating Conditions*...5
- Deleted INA128-HT and INA129-HT operating temperature specifications from *Recommended Operating Conditions*...5
- Added specified temperature range to *Recommended Operating Conditions*... 5
- Added test conditions below *Electrical Characterstics* title...6
- Changed test condition for offset voltage drift specification in *Electrical Characteristics* from "TA = TMIN to TMAX" to " TA = –40℃ to +85℃" for clarity...6
- Changed "±0.5±0/G" to "±0.5±20/G" in MAX column of Offset voltage RTI vs temperature row of *Electrical Characteristics*...6
- Changed typical long-term stability specification from ±0.1±3/GμV/mo to ±0.2±3/GμV/mo in *Electrical Characteristics*...6
- Deleted typical specification and changed common-mode voltage specification from (V–) + 2 V minimum and (V+) – 2 V maximum across one row in Electrical Characteristics... 6
- Deleted typical VCM specifications in *Electrical Characteristics*... 6
- Added test condition of "RS = 0 Ω" to safe input voltage specification in *Electrical Characteristics* for clarity.....6
- Changed parameter name to Input bias current and added test condition "TA = –40°C to +85°C" to input bias current drift specification in *Electrical Characteristics* for clarity...6
- Changed parameter name to Input offset current drift and added test condition "TA = –40°C to +85°C" to input offset current drift specification in *Electrical Characteristics* for clarity... 6
- Changed maximum gain error specification for INA128PA/UA and INA129PA/UA with G = 1 from ±0.01% to ±0.1% in *Electrical Characteristics*... 6

- Changed parameter name to Gain drift and added test condition "TA = –40°C to +85°C" for gain drift in *Electrical Characteristics* for clarity..6
- Changed parameter names from "Voltage - Positive" to "Positive output voltage swing" and from "Voltage - Negative" to "Negative output voltage swing" in *Electrical Characteristics* 6
- Deleted typical positive and negative output voltage swing specifications in *Electrical Characteristics* 6
- Added test condition "Continuous to VS / 2" short-circuit current specification in *Electrical Characteristics* for clarity.. 6
- Changed typical bandwidth specification for G = 10 from 700 kHz to 600 kHz in *Electrical Characteristics* 6
- Changed typical slew rate specification from 4 V/µs to 1.2 V/µs in *Electrical Characteristics* 6
- Changed typical settling time specification for G = 1, G = 10, from 7 µs to 9 µs in *Electrical Characteristics* 6
- Deleted parameter "Temperature Range" as made redundant by *"Recommended Operating Conditions"* and *"Absolute Maximum Ratings"* 6
- Changed parameter name to "Total quiescent current" and deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics* 6
- Added test conditions below the *Typical Characteristics* title..8
- Changed Figure 6-1, *Gain vs Frequency* 8
- Changed Figure 6-3, *Positive Power Supply Rejection vs Frequency* 8
- Changed Figure 6-4, *Negative Power Supply Rejection vs Frequency* 8
- Changed Figure 6-7, *Crosstalk vs Frequency* 8
- Changed Figure 6-8, *Input-Referred Voltage Noise vs Frequency* 8
- Changed Figure 6-9, *Settling Time vs Gain* 8
- Changed Figure 6-11, *Input Overvoltage V/I Characteristics* 8
- Changed Figure 6-12, *Offset Voltage Warm-Up* 8
- Changed *Output Voltage Swing vs Output Current*, into two separate plots, one for positive (Figure 6-14) and one for negative (Figure 6-15).. 8
- Changed Figure 6-22 to Figure 6-24, *Large-Signal Step Response* 8

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5 Pin Configuration and Functions

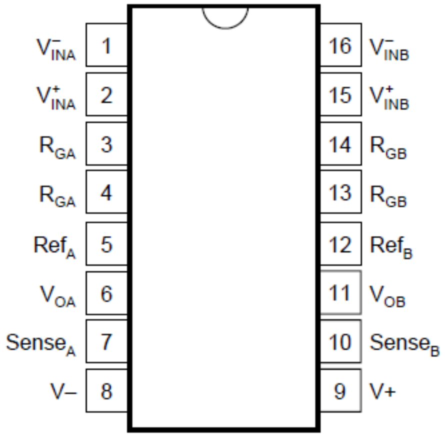

Figure 5-1. DW Package, 16-Pin SOIC (Top View)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0 V		36	
	Analog input voltage			±40	V
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–40	125	°C
	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			300	°C
T_{stg}	Storage temperature		–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±50	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
	Input common-mode voltage range for V_O = 0 V		(V–) + 2		(V+) – 2	V
T_A	Specified temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA12x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	11.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage (RTI)	INA2128U				±10 ±100 / G	±50 ±500 / G	μV
		INA2128UA				±25 ±100 / G	±125 ±1000 / G	
	Offset voltage drift (RTI)	T_A = –40°C to +85°C	INA2128U			±0.2 ±2 / G	±0.5 ±20 / G	μV/°C
			INA2128UA			±0.2 ±5 / G	±1 ±20 / G	
PSRR	Power-supply rejection ratio (RTI)	V_S = ±2.25 V to ±18 V	INA2128U			±0.2 ±20 / G	±1 ±100 / G	μV/V
			INA2128UA			±0.2 ±20 / G	±2 ±200 / G	
	Long-term stability					±0.2 ±3 / G		μV/mo
	Input impedance	Differential				10 || 2		GΩ || pF
		Common-mode				100 || 9		
V_{CM}	Common-mode voltage(1)	V_O = 0 V			(V–) + 2		(V+) – 2	V
	Safe input voltage	R_S = 0 Ω					±40	V
CMRR	Common-mode rejection ratio	ΔR_S = 1 kΩ, V_{CM} = ±13 V	G = 1	INA2128U	80	86		dB
				INA2128UA	73	86		
			G = 10	INA2128U	100	106		
				INA2128UA	93	106		
			G = 100	INA2128U	120	125		
				INA2128UA	110	125		
			G = 1000	INA2128U	120	130		
				INA2128UA	110	130		
INPUT BIAS CURRENT								
I_B	Input bias current	INA2128U				±2	±5	nA
		INA2128UA				±2	±10	
	Input bias current drift	T_A = –40°C to +85°C				±30		pA/°C
I_{OS}	Input offset current	INA2128U				±1	±5	nA
		INA2128UA				±1	±10	
	Input offset current drift	T_A = –40°C to +85°C				±30		pA/°C
NOISE								
e_N	Voltage noise (RTI)	G = 1000, R_S = 0 Ω	f = 10 Hz			10		nV/√Hz
			f = 100 Hz			8		
			f = 1 kHz			8		
			f_B = 0.1 Hz to 10 Hz			0.2		μV_{PP}
	Current noise	f = 10 Hz				0.9		pA/√Hz
		f = 1 kHz				0.3		
		f_B = 0.1 Hz to 10 Hz				30		pA_{PP}

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
	Gain equation				1 + (50 kΩ / R_G)		V/V
G	Gain			1		10000	V/V
GE	Gain error	G = 1	INA2128U		±0.01	±0.024	%
			INA2128UA		±0.01	±0.1	
		G = 10	INA2128U		±0.02	±0.4	
			INA2128UA		±0.02	±0.5	
		G = 100	INA2128U		±0.05	±0.5	
			INA2128UA		±0.05	±0.7	
		G = 1000	INA2128U		±0.5	±1	
			INA2128UA		±0.5	±2	
	Gain drift(2)	T_A = –40°C to +85°C			±1	±10	ppm/°C
			50-kΩ or 49.4-kΩ resistance(3)		±25	±100	
	Gain nonlinearity	G = 1, V_O = ±13.6 V	INA2128U		±0.0001	±0.001	% of FSR
			INA2128UA		±0.0001	±0.002	
		G = 10	INA2128U		±0.0003	±0.002	
			INA2128UA		±0.0003	±0.004	
		G = 100	INA2128U		±0.0005	±0.002	
			INA2128UA		±0.0005	±0.004	
		G = 1000(4)			±0.001		
OUTPUT							
	Positive output voltage			(V+) – 1.4			V
	Negative output voltage			(V–) + 1.4			V
C_L	Load capacitance	Stable operation			1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2			+6/–15		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 1			1.3		MHz
		G = 10			600		kHz
		G = 100			200		
		G = 1000			20		
SR	Slew rate	G = 10, V_O = ±10 V			1.2		V/µs
t_S	Settling time	To 0.01%	G = 1		9		µs
			G = 10		9		
			G = 100		12		
			G = 1000		80		
	Overload recovery	50% input overload			4		µs
POWER SUPPLY							
I_Q	Total quiescent current	V_{IN} = 0 V			±1.4	±1.5	mA

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(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.
(3) Temperature coefficient of the 50-kΩ or 49.4-kΩ term in the gain equation.
(4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

6.6 Typical Characteristics

at T_A = +25°C, V_S = ±15 V, V_{REF} = 0 V, G = 1, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

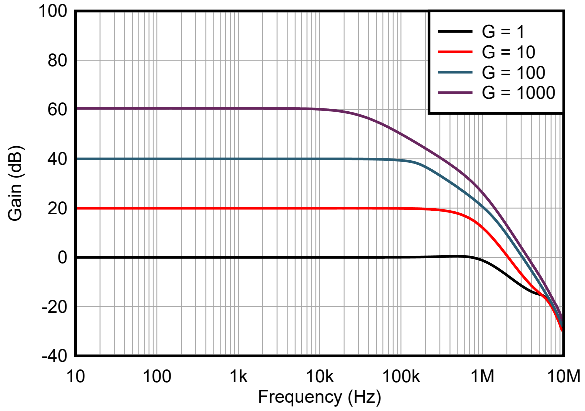


Figure 6-1. Gain vs Frequency

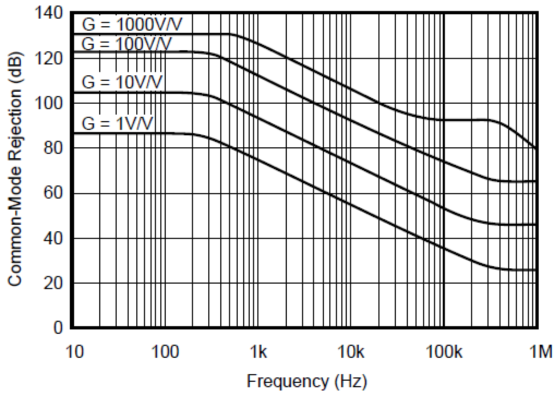


Figure 6-2. Common-Mode Rejection vs Frequency

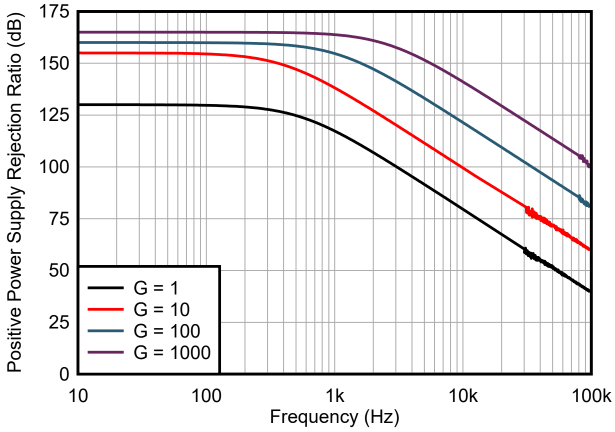


Figure 6-3. Positive Power Supply Rejection vs Frequency

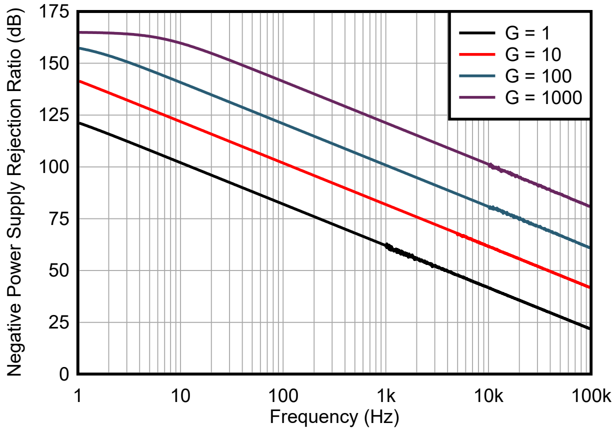
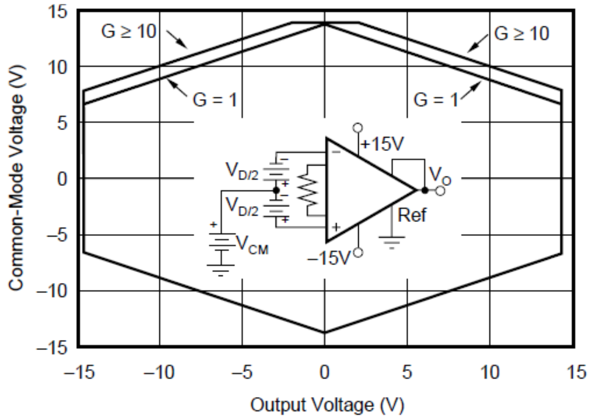
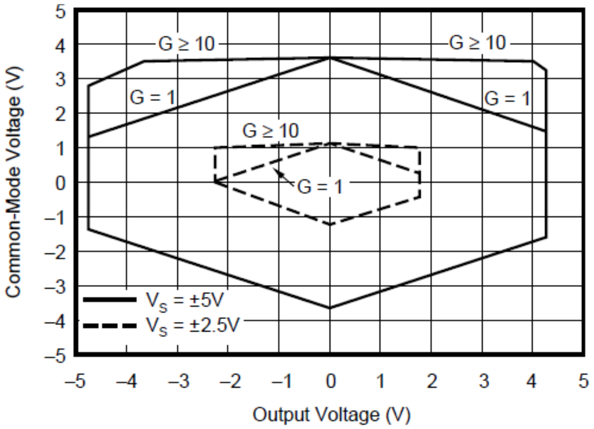


Figure 6-4. Negative Power Supply Rejection vs Frequency



V_S = ±15 V

Figure 6-5. Input Common-Mode Range vs Output Voltage



V_S = ±5, ±2.5 V

Figure 6-6. Input Common-Mode Range vs Output Voltage

6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V, V_{REF} = 0 V, G = 1, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

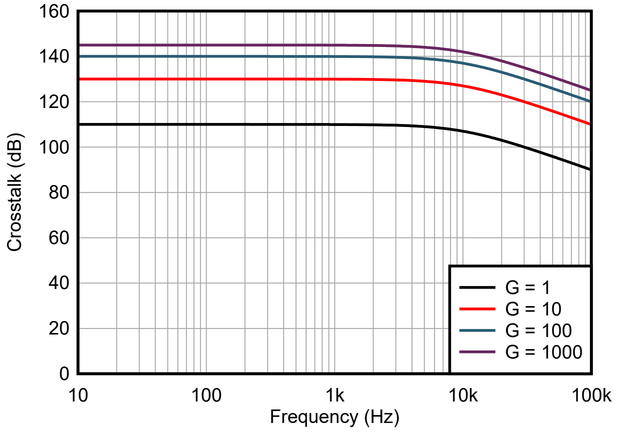


Figure 6-7. Crosstalk vs Frequency

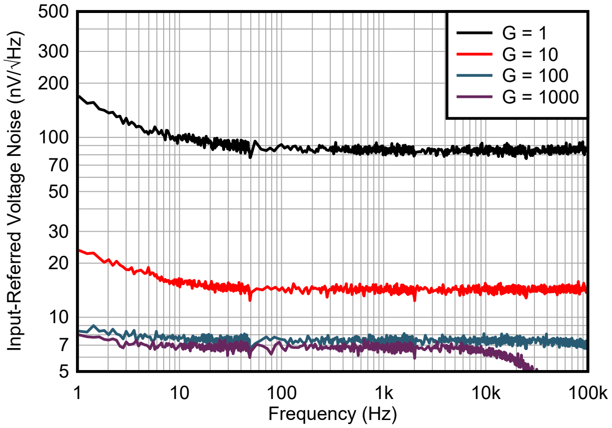


Figure 6-8. Input-Referred Voltage Noise vs Frequency

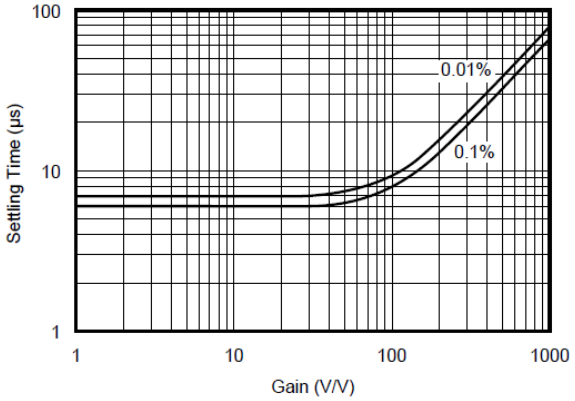


Figure 6-9. Settling Time vs Gain

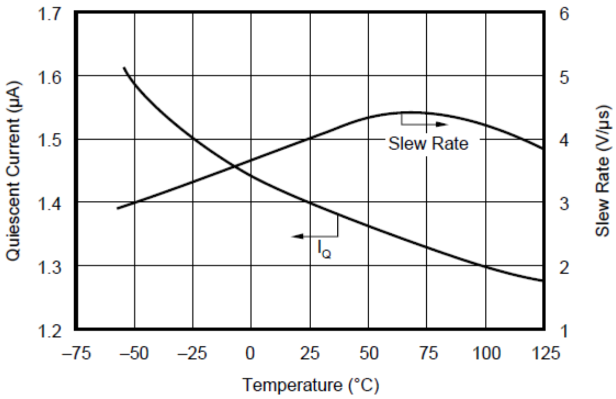


Figure 6-10. Quiescent Current and Slew Rate vs Temperature

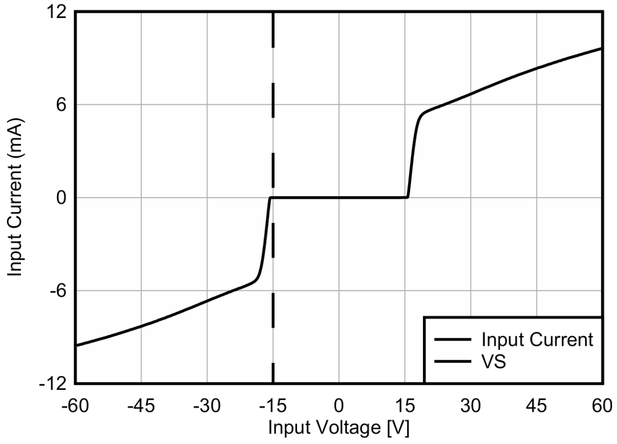


Figure 6-11. Input Overvoltage V/I Characteristics

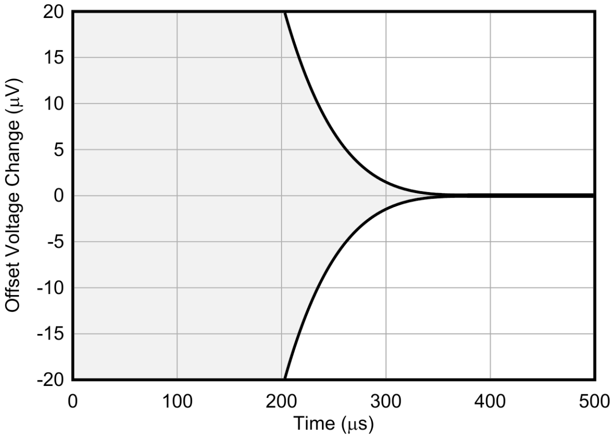


Figure 6-12. Offset Voltage Warm-Up

6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V, V_{REF} = 0 V, G = 1, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

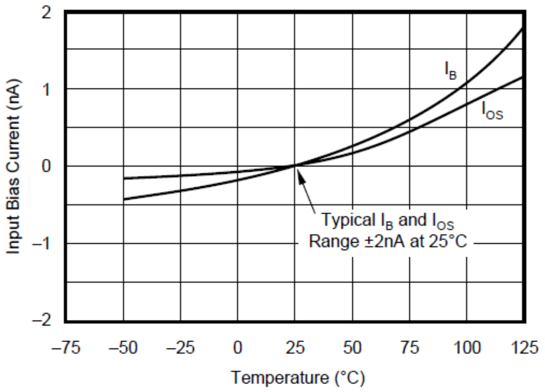


Figure 6-13. Input Bias Current vs Temperature

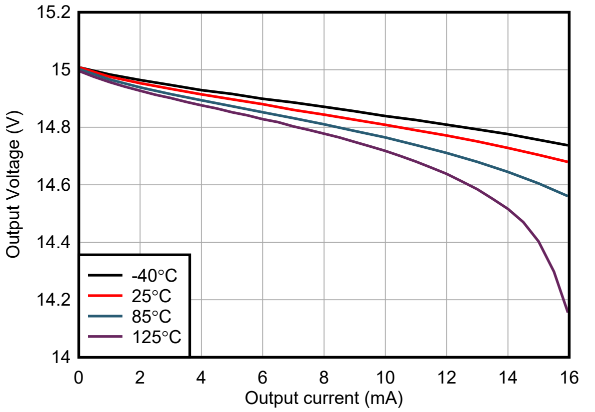


Figure 6-14. Positive Output Voltage Swing vs Output Current

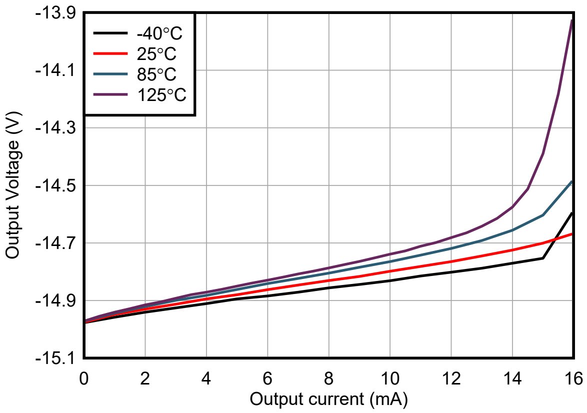


Figure 6-15. Negative Output Voltage Swing vs Output Current

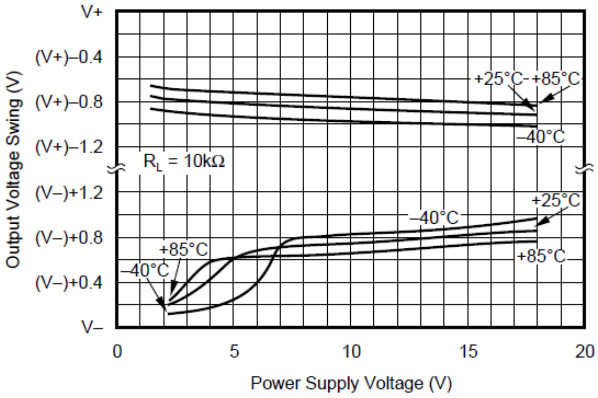


Figure 6-16. Output Voltage Swing vs Power Supply Voltage

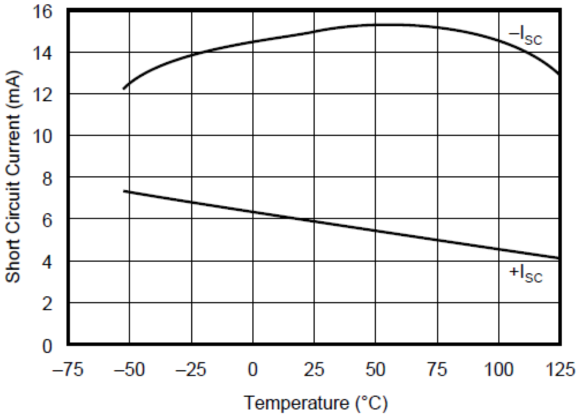


Figure 6-17. Short-Circuit Output Current vs Temperature

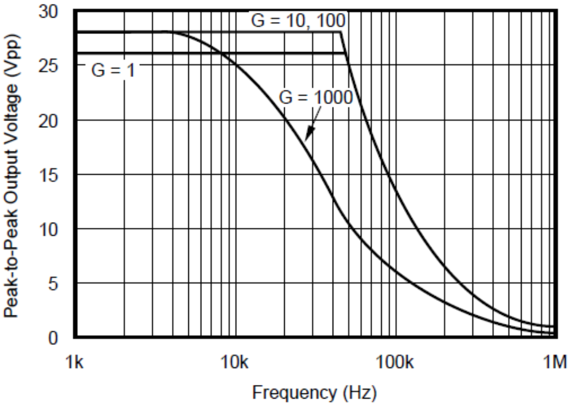


Figure 6-18. Maximum Output Voltage vs Frequency

6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V, V_{REF} = 0 V, G = 1, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

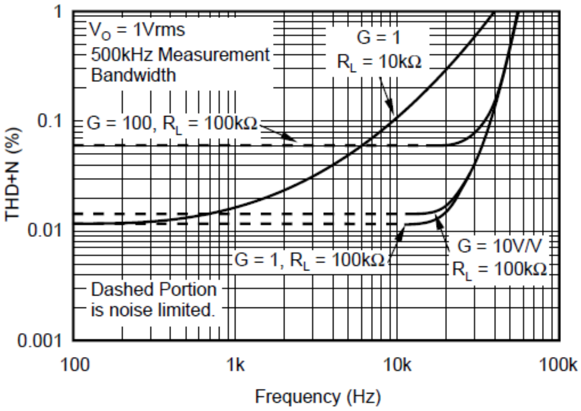
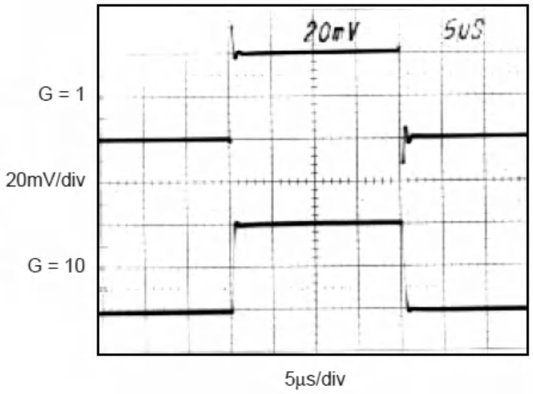
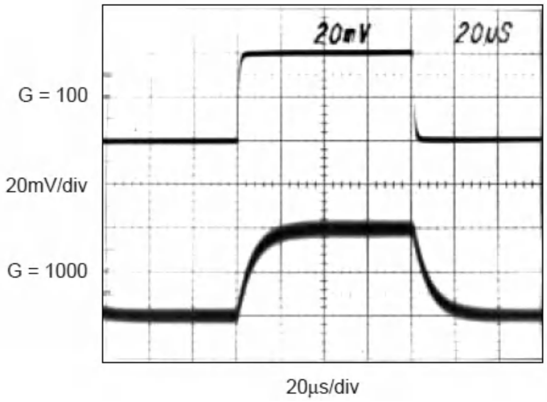


Figure 6-19. Total Harmonic Distortion + Noise vs Frequency



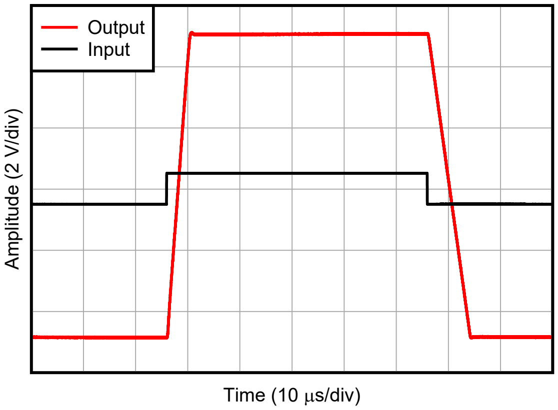
G = 1, 10

Figure 6-20. Small-Signal Step Response



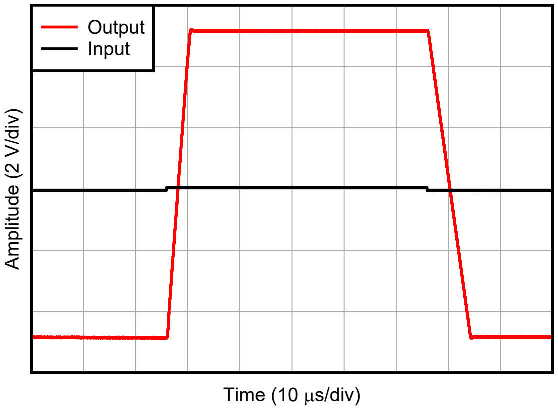
G = 100, 1000

Figure 6-21. Small-Signal Step Response



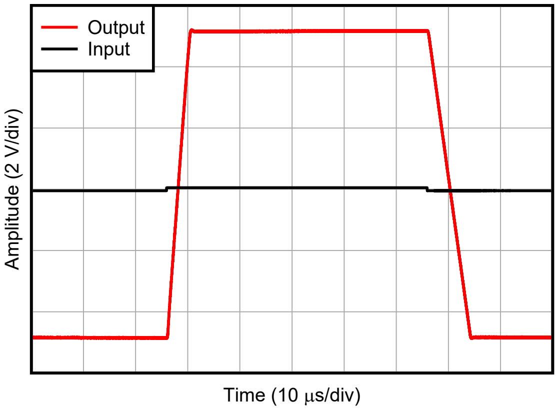
G = 1, 10

Figure 6-22. Large-Signal Step Response



G = 100

Figure 6-23. Large-Signal Step Response

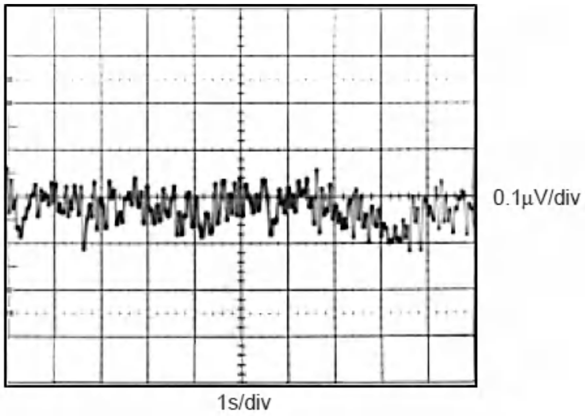


G = 1000

Figure 6-24. Large-Signal Step Response

6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V, V_{REF} = 0 V, G = 1, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)



G ≥ 100

Figure 6-25. Voltage Noise 0.1 Hz to 10 Hz Input-Referred

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Figure 7-1 shows the basic connections required for operation of the INA2128. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

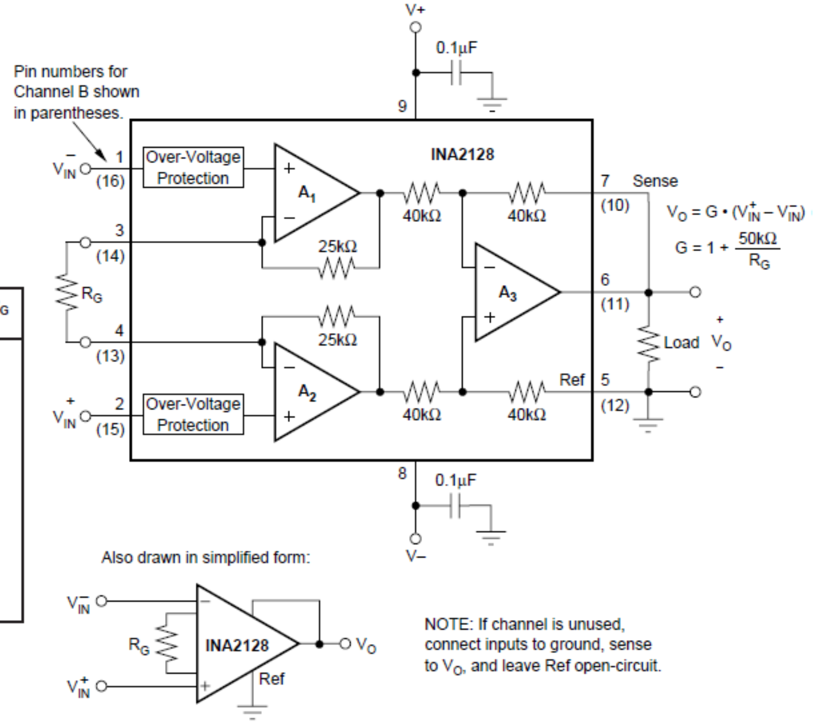
The output is referred to the output reference (Ref) terminals (Ref_A and Ref_B) which are normally grounded. These must be low-impedance connections to assure good common-mode rejection. A resistance of 8 Ω in series with a Ref pin will cause a typical device to degrade to approximately 80 dB CMR (G = 1).

The INA2128 has separate output sense feedback connections, Sense_A and Sense $_B$. These must be connected to their respective output terminals for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

7.2 Typical Application

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.



$V_O = G \cdot (V_{IN}^+ - V_{IN}^-)$

$G = 1 + \frac{50k\Omega}{R_G}$

NOTE: If channel is unused, connect inputs to ground, sense to V_O, and leave Ref open-circuit.

Figure 7-1. Basic Connections

7.2.1 Setting The Gain

Gain of the INA2128 is set by connecting a single external resistor, RG, connected as shown:

$$G = 1 + \frac{50\text{k}\Omega}{R_G} \tag{1}$$

Commonly-used gains and resistor values are shown in Figure 7-1.

The 50 kΩ term in Equation 1 comes from the sum of the two internal feedback resistors, A_1 and A_2. These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA2128.

The stability and temperature drift of the external gain setting resistor, RG, also affects gain. RG's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error in gains of approximately 100 or greater.

7.2.2 Dynamic Performance

The typical performance curve Figure 6-1 shows that despite its low quiescent current, the INA2128 achieves wide bandwidth, even at high gain. This is due to its current feedback topology. Settling time also remains excellent at high gain—see Figure 6-9.

7.2.3 Noise Performance

The INA2128 provides very low noise in most applications. Low frequency noise is approximately 0.2 μV_{pp} measured from 0.1 Hz to 10 Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

7.2.4 Offset Trimming

The INA2128 is laser-trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 7-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

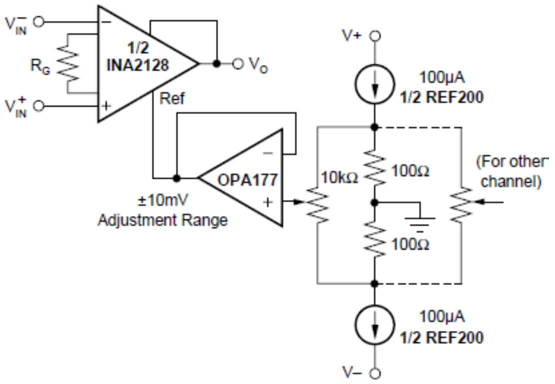


Figure 7-2. Optional Trimming of Output Offset Voltage

7.2.5 Input Bias Current Return Path

The input impedance of the INA2128 is extremely high—approximately 10^{10} Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 7-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA2128 and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 7-3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

7.2.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA2128 is from approximately 1.4 V less than the positive supply voltage to 1.7 V greater than the negative supply. As a differential input voltage causes the output voltage increase, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Therefore, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves Figure 6-6 and Figure 6-5.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA2128 is near 0 V even though both inputs are overloaded.

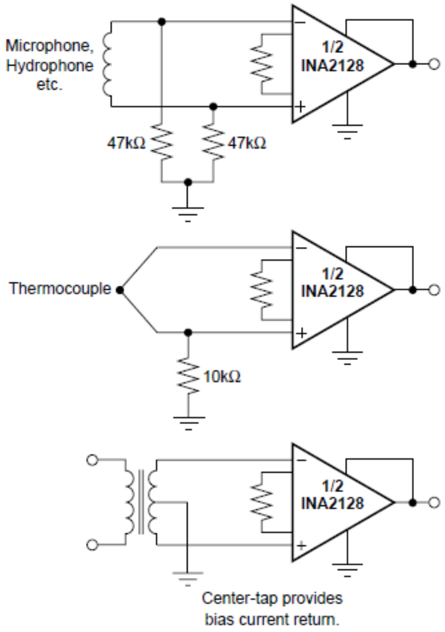


Figure 7-3. Providing an Input Common-Mode Current Path

7.2.7 Low-Voltage Operation

The INA2128 can be operated on power supplies as low as ±2.25 V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range—see Section 6.6. Operation at very low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. Typical performance curves, Figure 6-5 and Figure 6-6, show the range of linear operation for ±15-V, ±5-V, and ±2.5-V supplies.

7.2.8 Input Protection

The inputs of the INA2128 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 mA to 5 mA. The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

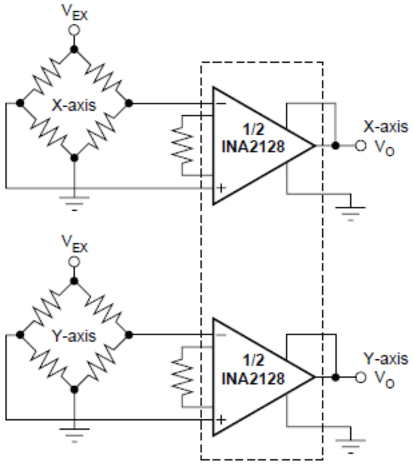


Figure 7-4. Two-Axis Bridge Amplifier

7.2.9 Channel Crosstalk

The two channels of the INA2128 are completely independent, including all bias circuitry. At dc and low frequency, there is virtually no signal coupling between channels. Crosstalk increases with frequency and depends on circuit gain, source impedance, and signal characteristics.

As source impedance increases, careful circuit layout helps achieve lowest channel crosstalk. Most crossstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Run the differential inputs of each channel parallel to each other or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal which is rejected by the IA input.

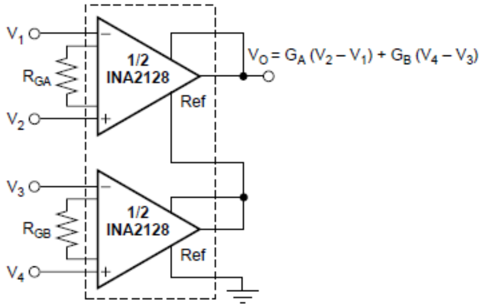
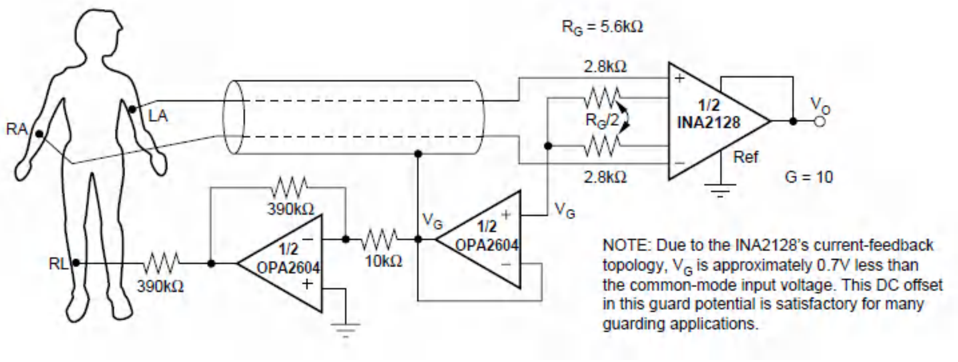


Figure 7-5. Sum of Differences Amplifier



NOTE: Due to the INA2128's current-feedback topology, V_G is approximately 0.7V less than the common-mode input voltage. This DC offset in this guard potential is satisfactory for many guarding applications.

Figure 7-6. ECG Amplifier With Right-Leg Drive

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA2128U	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2128U
INA2128U.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2128U
INA2128U/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	INA2128U
INA2128U/1K.B	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2128U
INA2128U1G4	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2128U
INA2128U1G4.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2128U
INA2128UA	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-	(INA2128U, INA2128 UA) A
INA2128UA.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(INA2128U, INA2128 UA) A
INA2128UA/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	(INA2128U, INA2128 UA) A
INA2128UA/1K.B	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(INA2128U, INA2128 UA) A
INA2128UAG4	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2128UA
INA2128UAG4.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2128UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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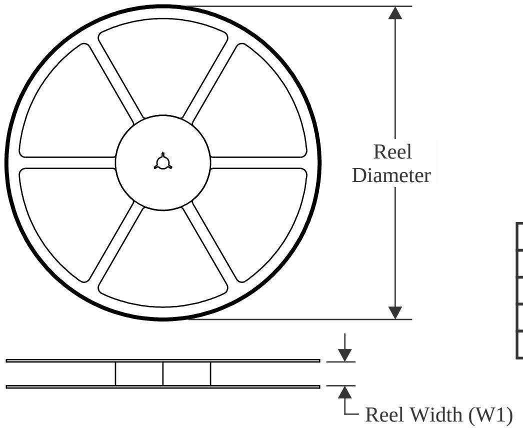
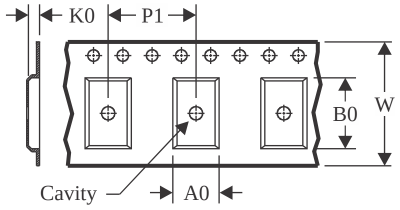
TAPE AND REEL INFORMATION

REEL DIMENSIONS

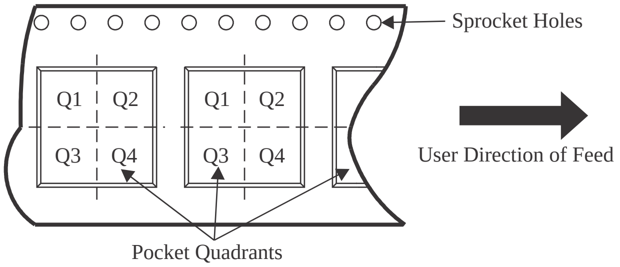


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

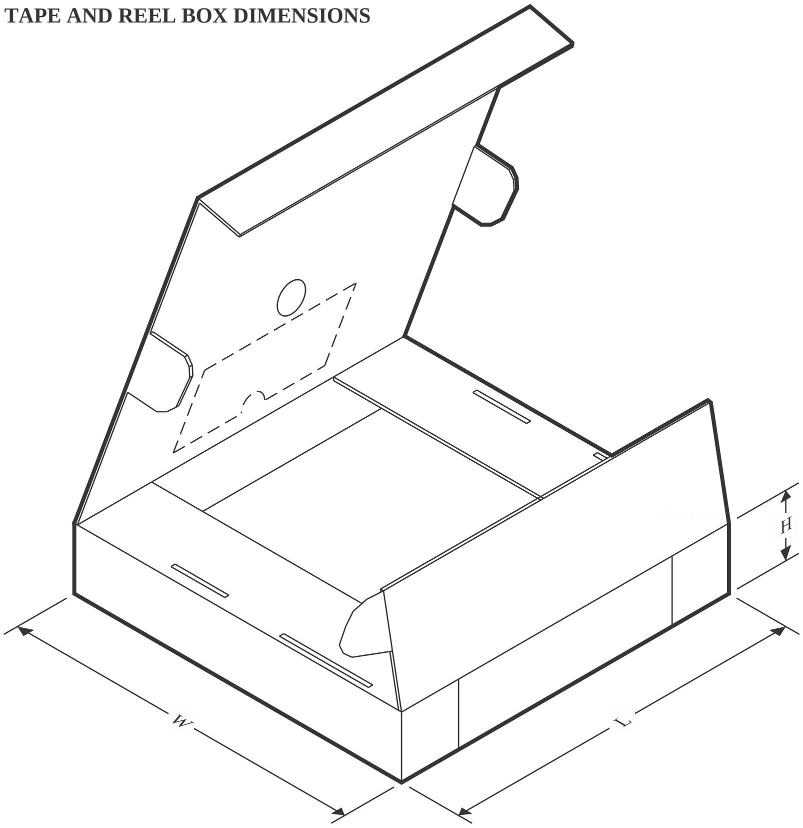
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2128U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA2128UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

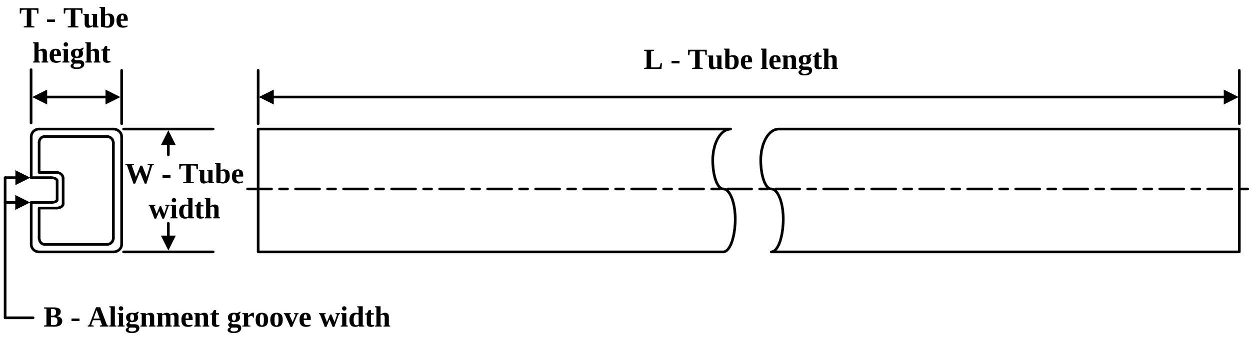
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2128U/1K	SOIC	DW	16	1000	350.0	350.0	43.0
INA2128UA/1K	SOIC	DW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA2128U	DW	SOIC	16	40	506.98	12.7	4826	6.6
INA2128U.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
INA2128U1G4	DW	SOIC	16	40	506.98	12.7	4826	6.6
INA2128U1G4.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
INA2128UA	DW	SOIC	16	40	506.98	12.7	4826	6.6
INA2128UA.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
INA2128UAG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
INA2128UAG4.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

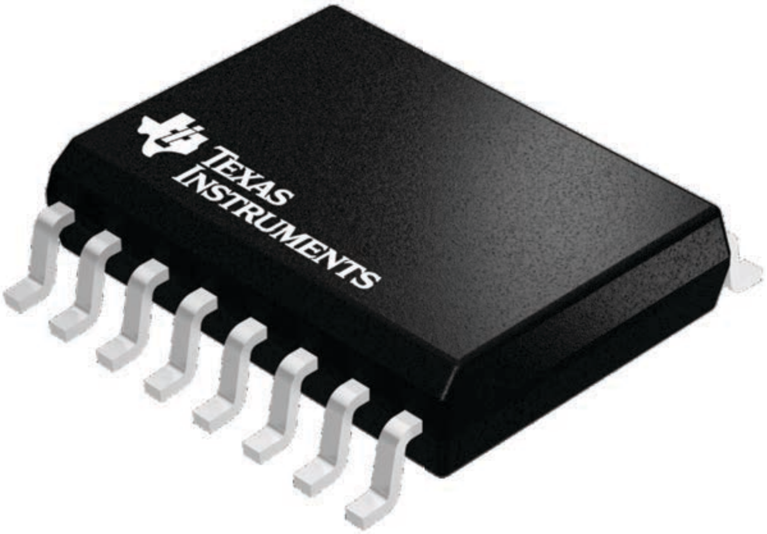
DW 16

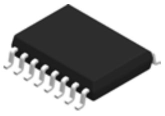
SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



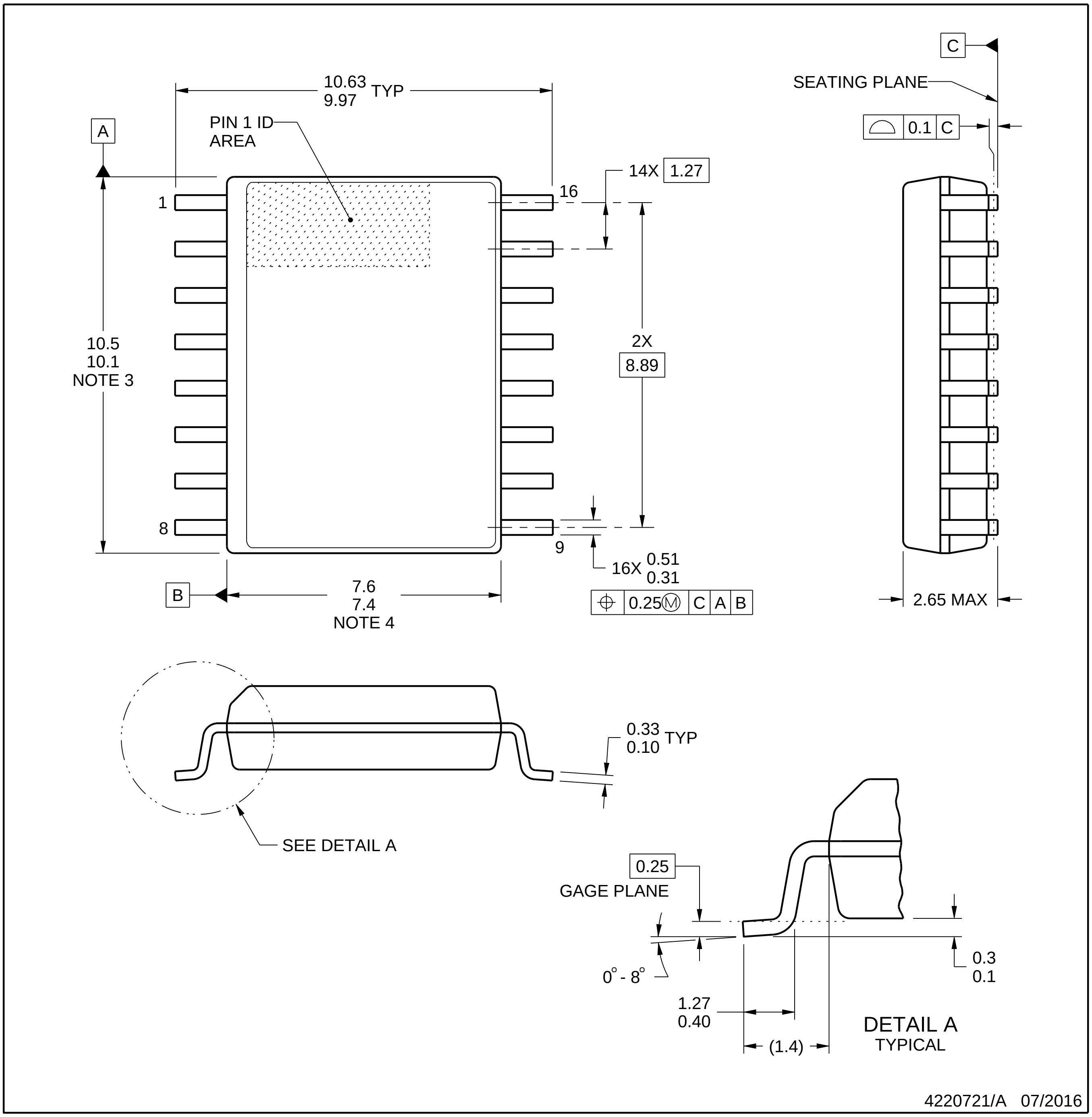


PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

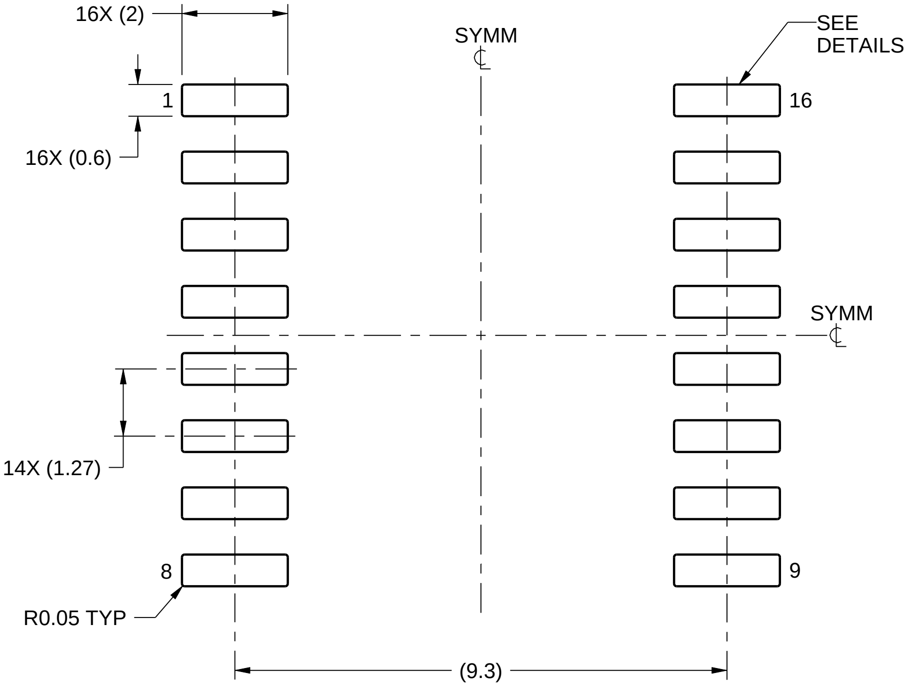
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

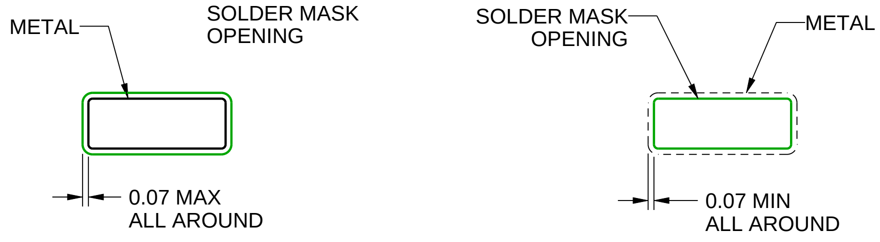
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

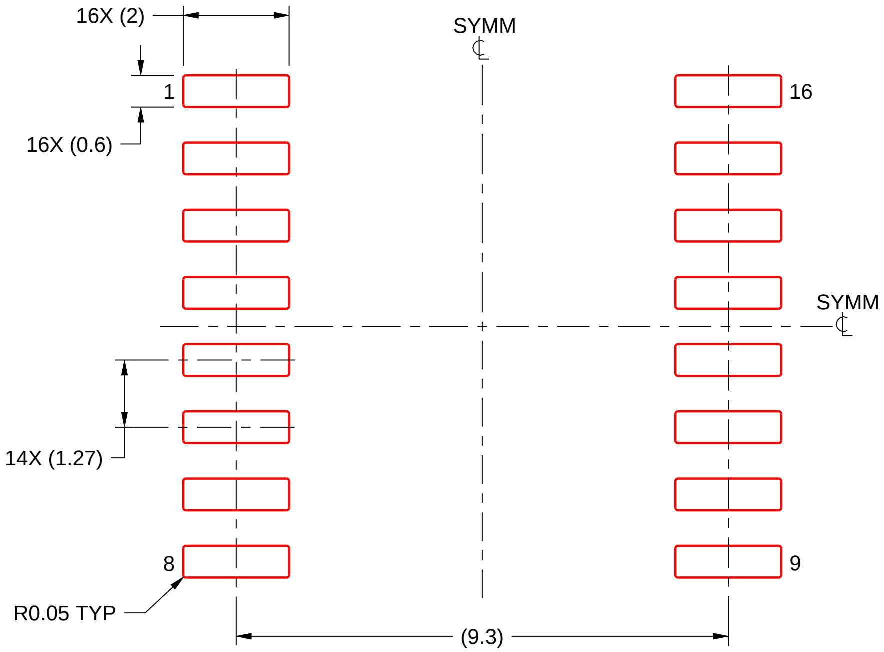
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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