INA20x-Q1 Automotive Grade, –16V to +80V, Low-Side or High-Side, High-Speed, Voltage-Output, Current-Sense Amplifier With Comparator and Reference

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C3B
- Current-sense amplifier:
  - Common-mode range: –16V to +80V
  - 3.5% maximum error over temperature
  - Bandwidth: 500kHz (INA200-Q1)
  - Three gain options:
    - 20V/V (INA200-Q1)
    - 50V/V (INA201-Q1)
    - 100V//V (INA202-Q1)
- Integrated open-drain comparator
  - Latching capability
  - 0.6V internal voltage reference
- Quiescent current: 1800µA (maximum)
- Latch-up exceeds 100mA per JESD78
- Package: VSSOP-8

2 Applications

- Electric power steering (EPS) systems
- Body control modules
- Brake systems
- Electronic stability control (ESC) systems

3 Description

The INA200-Q1, INA201-Q1, and INA202-Q1 (INA20x-Q1) are low-side or high-side, current-shunt monitors with voltage output. The INA20x-Q1 devices can sense drops across shunts at common-mode voltages from –16V to +80V. The INA20x-Q1 are available with three output voltage scales: 20V/V, 50V/V, and 100V/V, with up to a 500kHz bandwidth.

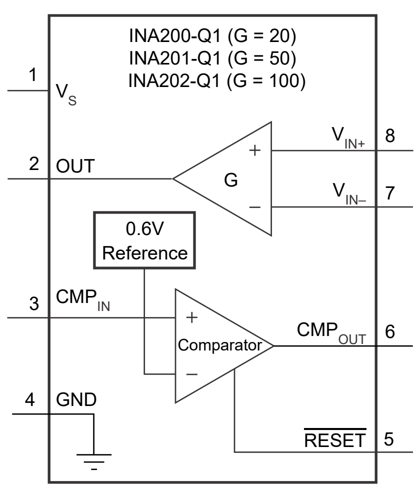
The INA20x-Q1 also incorporates an open-drain comparator and internal reference that provides a 0.6V threshold. External dividers set the current trip point. The comparator includes a latching capability, and can be made transparent by grounding (or leaving open) the $\overline{\text{RESET}}$ pin.

The INA20x-Q1 operates from a single 2.7V to 18V supply, drawing a maximum of 1800µA supply current. These devices are available in the very small VSSOP-8 package. Specifications for all devices extend over the operating temperature range of –40°C to +125°C.

Package Information [1]

PART NUMBER	PACKAGE	PACKAGE SIZE[2]
INA200-Q1	DGK (VSSOP, 8)	3mm × 4.9mm
INA201-Q1		
INA202-Q1		

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison

Table 4-1. Device Comparison

DEVICE	DESCRIPTION
INA193A-Q1	Same amplifier performance as INA200-Q1 without integrated comparator
INA203-Q1	Dual comparator alternative to the INA200-Q1 single comparator
INA282-Q1	Automotive, 80-V, bidirectional, high-accuracy, low- or high-side, voltage out current shunt monitor
INA300-Q1	Automotive, 36-V, low- or high-side, overcurrent protection comparator
INA301	Overcurrent protection, high-speed, precision, current sense amplifier with integrated comparator

5 Pin Configuration and Functions

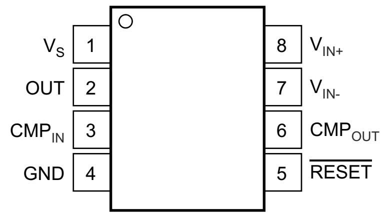


Figure 5-1. DGK Package 8-Pin VSSOP Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_s	Analog	Power supply
2	OUT	Analog output	Output voltage
3	CMP_{IN}	Analog input	Comparator input
4	GND	Analog	Ground
5	$\overline{RESET}$	Analog input	Comparator reset pin, active low
6	CMP_{OUT}	Analog output	Comparator output
7	V_{IN-}	Analog input	Negative input, connect to shunt low side
8	V_{IN+}	Analog input	Positive input, connect to shunt high side

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S		2.7	18	V
Current-shunt monitor analog inputs, V_{IN+}, V_{IN-}	Differential (V_{IN+} – V_{IN-})	–18	18	V
	Common mode(2), V_{CM} = (V_{IN+} + V_{IN-}) / 2	–16	80	V
Comparator analog input and reset pins, CMP_{IN} and $\overline{RESET}$ (2)		GND – 0.3	(V_S) + 0.3	V
Analog output, OUT(2)		GND – 0.3	(V_S) + 0.3	V
Comparator output, CMP_{OUT} (2)		GND – 0.3	18	V
Input current into any pin(2)			5	mA
Operating temperature, T_A		–40	125	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This voltage may exceed the ratings shown if the current at that pin does not exceed 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–16	12	80	V
V_S	Operating supply voltage	2.7	12	18	V
T_A	Operating free-air temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA20x-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	81.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Current-Shunt Monitor

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{SENSE}	Full-scale sense input voltage	V_{SENSE} = V_{IN+} – $V_{IN–}$			0.15	(V_S – 0.25) / Gain	V
V_{CM}	Common-mode input range	T_A = –40°C to 125°C		–16		80	V
CMR	Common-mode rejection	V_{IN+} = –16 V to 80 V		80	100		dB
		V_{IN+} = 12 V to 80 V, T_A = –40°C to 125°C.		100	123		dB
V_{OS}	Offset voltage, RTI(1)	T_A = 25°C			±0.5	±2.5	mV
		T_A = 25°C to 125°C				±3	mV
		T_A = –40°C to 25°C				±3.5	mV
dV_{OS}/dT	Offset voltage, RTI, versus temperature	T_A = –40°C to 125°C			5		µV/°C
PSR	Offset voltage, RTI, versus power supply	V_{OUT} = 2 V, V_{IN+} = 18 V, 2.7 V, T_A = –40°C to 125°C			2.5	100	µV/V
I_B	Input bias current, $V_{IN–}$ Pin	T_A = –40°C to 125°C			±9	±16	µA
OUTPUT (V_{SENSE} ≥ 20mV)							
G	Gain	INA200-Q1			20		V/V
		INA201-Q1			50		V/V
		INA202-Q1			100		V/V
	Gain error	V_{SENSE} = 20 mV to 100 mV			±0.2%	±1%	
		V_{SENSE} = 20 mV to 100 mV, T_A = –40°C to 125°C				±2%	
	Total output error(2)	V_{SENSE} = 120 mV, V_S = 16 V			±0.75%	±2.2%	
		V_{SENSE} = 120 mV, V_S = 16 V, T_A = –40°C to 125°C				±3.5%	
	Nonlinearity error(3)	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output impedance				1.5		Ω
C_{LOAD}	Maximum capacitive load	No sustained oscillation			10		nF
OUTPUT (V_{SENSE} < 20 mV)(4)							
	Output	–16 V ≤ V_{CM} < 0 V	INA20x-Q1		300		mV
		0 V ≤ V_{CM} ≤ V_S, V_S = 5 V	INA200-Q1			0.4	V
			INA201-Q1			1	V
			INA202-Q1			2	V
		V_S < V_{CM} ≤ 80 V	INA20x-Q1		300		mV
VOLTAGE OUTPUT(5)							
	Output swing to the positive rail	$V_{IN–}$ = 11 V, V_{IN+} = 12 V, T_A = –40°C to 125°C			(V_S) – 0.15	(V_S) – 0.25	V
	Output swing to GND(6)	$V_{IN–}$ = 0 V, V_{IN+} = –0.5 V, T_A = –40°C to 125°C			(V_{GND}) + 0.004	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	C_{LOAD} = 5 pF	INA200-Q1		500		kHz
			INA201-Q1		300		kHz
			INA202-Q1		200		kHz
	Phase margin	C_{LOAD} < 10 nF			40		Degrees
SR	Slew rate				1		V/µs
	Settling time (1%)	V_{SENSE} = 10 mV_{PP} to 100 mV_{PP}, C_{LOAD} = 5 pF			2		µs
NOISE, RTI							
	Voltage noise density				40		nV/√Hz

(1) Offset is extrapolated from measurements of the output at 20 mV and 100 mV V_{SENSE}.
(2) Total output error includes effects of gain error and V_{OS}.
(3) Linearity is best fit to a straight line.
(4) For details on this region of operation, see the *Accuracy Variations* section in the *Section 8.4*.
(5) See Figure 6-7.

(6) Specified by design.

6.6 Electrical Characteristics: Comparator

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and $R_{PULL\text{-}UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
	Threshold	T_A = 25°C	590	608	620	mV
		T_A = –40°C to 125°C	586		625	mV
	Hysteresis[1]	T_A = –40°C to 85°C		–8		mV
INPUT BIAS CURRENT[2]						
	CMP_{IN} pin			0.005	10	nA
		T_A = –40°C to 125°C			15	nA
INPUT VOLTAGE RANGE						
	CMP_{IN} pin			0 to V_S – 1.5		V
OUTPUT (OPEN-DRAIN)						
	Large-signal differential voltage gain	CMP_{OUT} = 1 V to 4 V, R_L ≥ 15 kΩ connected to 5 V		200		V/mV
I_{LKG}	High-level leakage current[3] [4]	V_{ID} = 0.4 V, V_{OH} = V_S		0.0001	1	µA
V_{OL}	Low-level output voltage[3]	V_{ID} = –0.6 V, I_{OL} = 2.35 mA		220	300	mV
RESPONSE TIME						
	Response time[5]	R_L to 5 V, C_L = 15 pF, 100-mV input step with 5-mV overdrive		1.3		µs
$\overline{\text{RESET}}$						
	$\overline{\text{RESET}}$ threshold[6]			1.1		V
	Logic input impedance			2		MΩ
	Minimum $\overline{\text{RESET}}$ pulse duration			1.5		µs
	$\overline{\text{RESET}}$ propagation delay			3		µs

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator; see Figure 7-1.
(2) Specified by design.
(3) V_{ID} refers to the differential voltage at the comparator inputs.
(4) Pulling the open-drain output to the range of 2.7 V to 18 V is permissible, regardless of V_S.
(5) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(6) The $\overline{\text{RESET}}$ input has an internal 2-MΩ (typical) pulldown. Leaving $\overline{\text{RESET}}$ open results in a low state, with transparent comparator operation.

6.7 Electrical Characteristics: General

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL\text{-}UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = 1 V (unless otherwise noted)

GENERAL PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current	V_{OUT} = 2 V		1350	1800	µA
		V_{SENSE} = 0 mV, T_A = –40°C to 125°C			1850	µA
	Comparator power-on reset threshold[1]			1.5		V

(1) The INA20x-Q1 devices power up with the comparator in a defined reset state as long as the $\overline{\text{RESET}}$ pin is open or grounded. The comparator is in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If $\overline{\text{RESET}}$ is high at power up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

6.8 Typical Characteristics

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

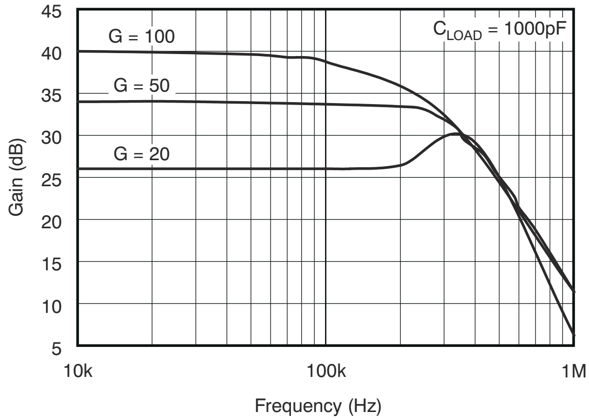


Figure 6-1. Gain vs Frequency

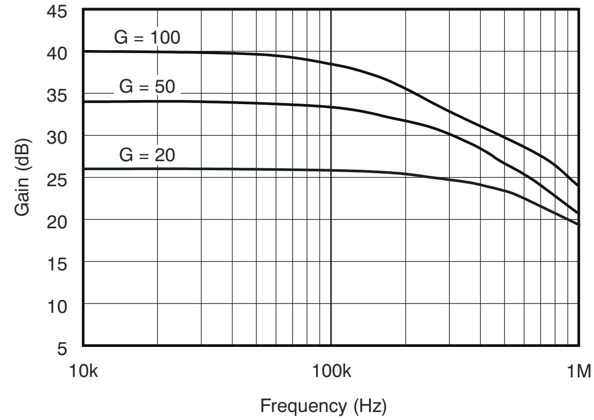


Figure 6-2. Gain vs Frequency

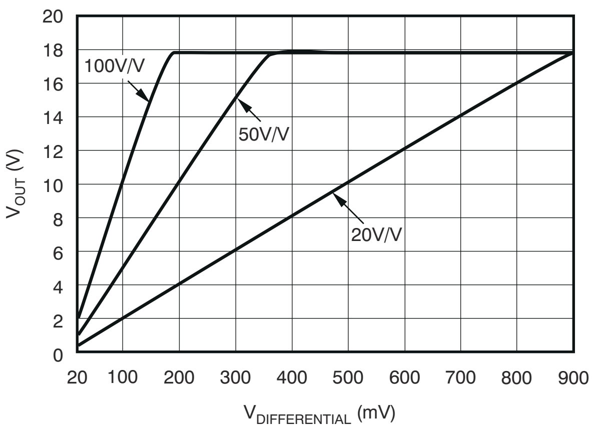


Figure 6-3. Gain Plot

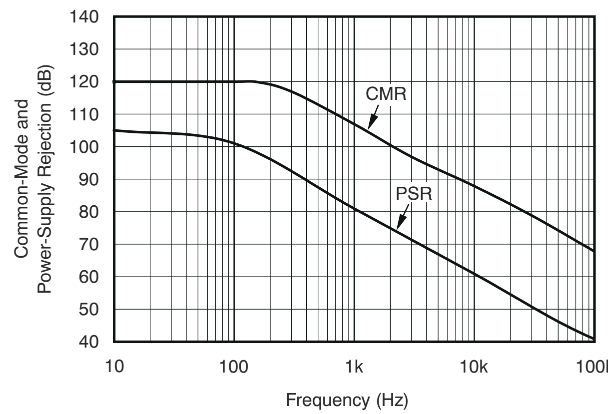


Figure 6-4. Common-Mode and Power-Supply Rejection vs Frequency

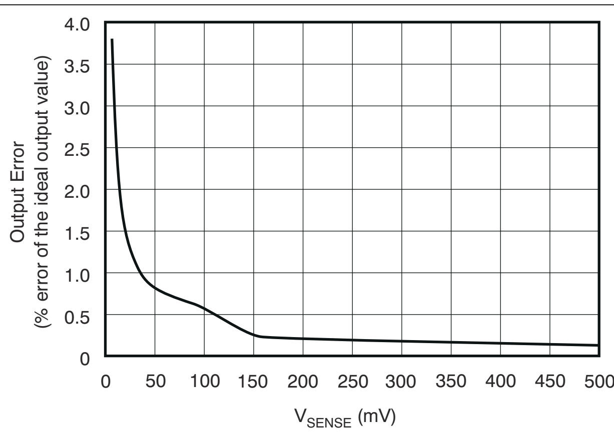


Figure 6-5. Output Error vs V_{SENSE}

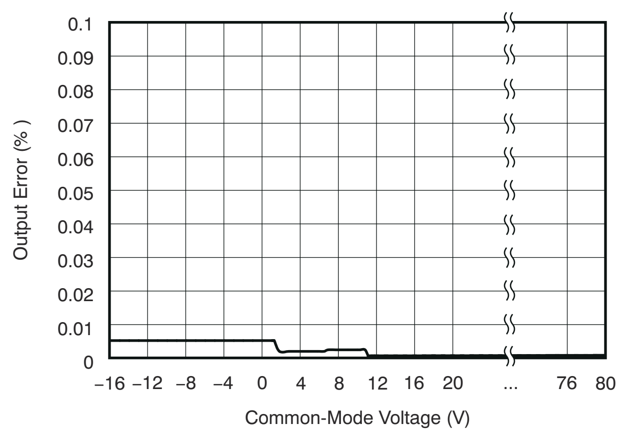


Figure 6-6. Output Error vs Common-Mode Voltage

6.8 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

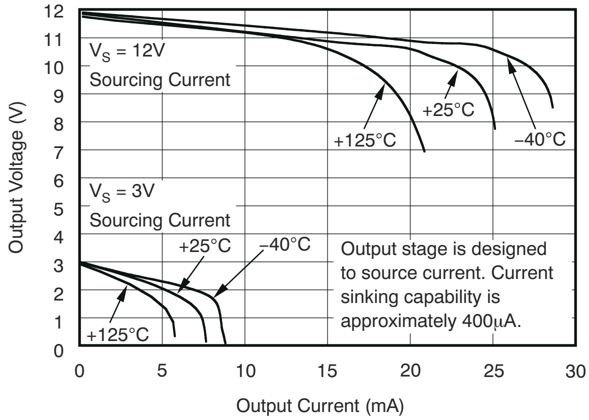


Figure 6-7. Positive Output Voltage Swing vs Output Current

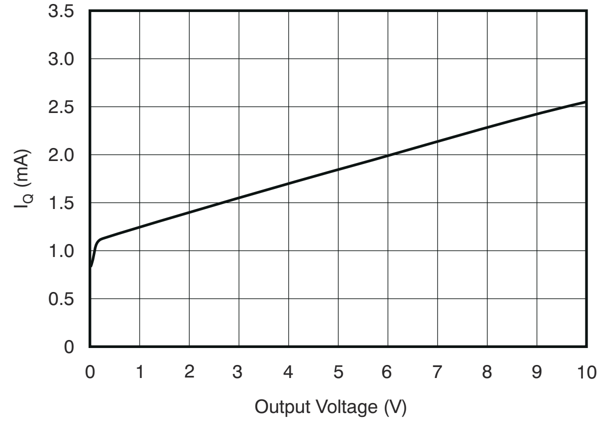


Figure 6-8. Quiescent Current vs Output Voltage

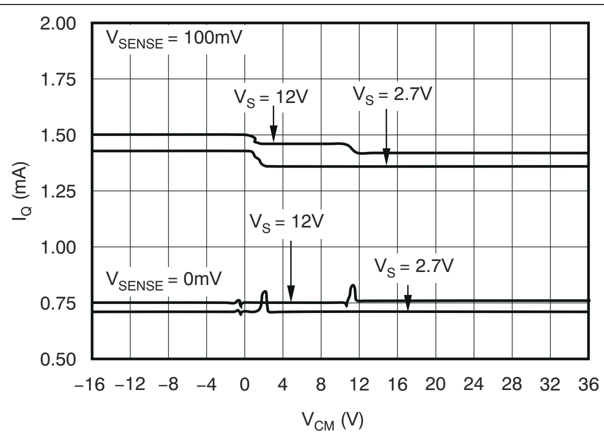


Figure 6-9. Quiescent Current vs Common-Mode Voltage

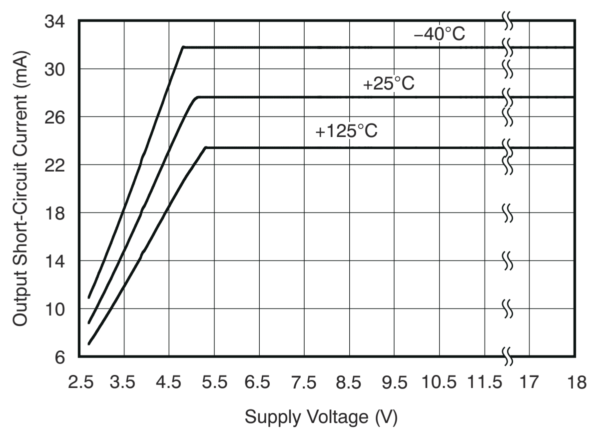


Figure 6-10. Output Short-Circuit Current vs Supply Voltage

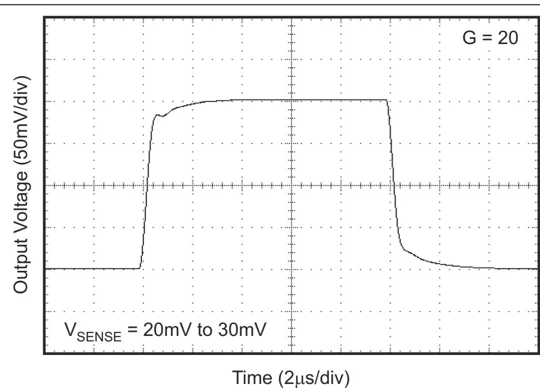


Figure 6-11. Step Response

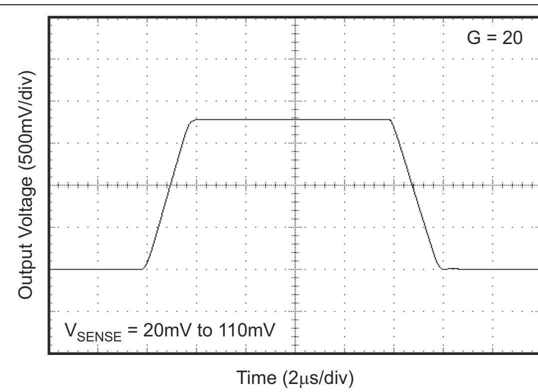


Figure 6-12. Step Response

6.8 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

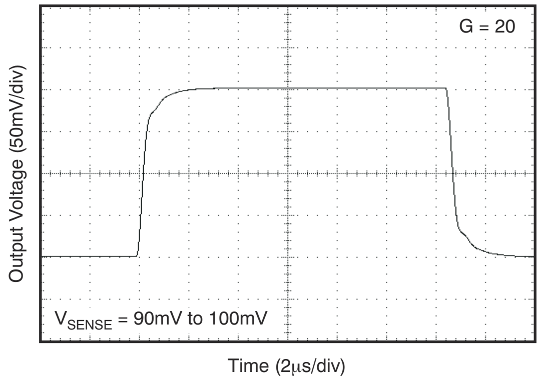


Figure 6-13. Step Response

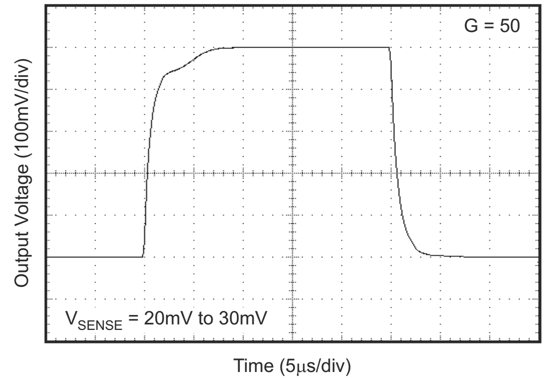


Figure 6-14. Step Response

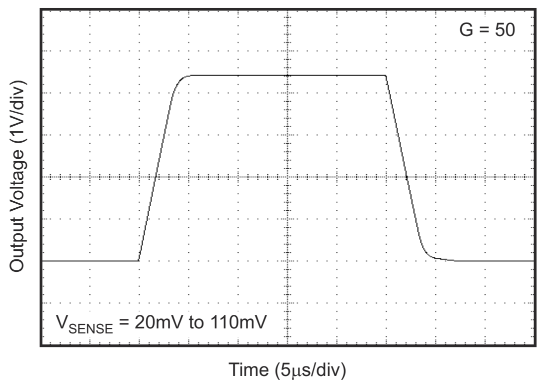


Figure 6-15. Step Response

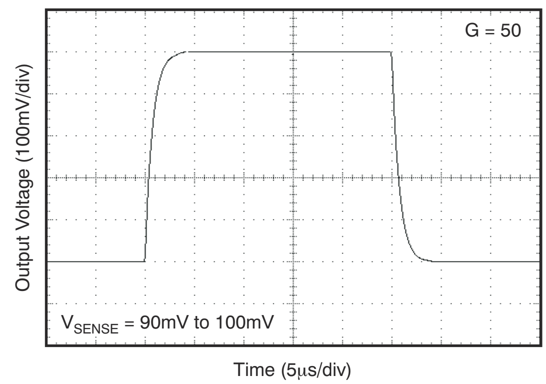


Figure 6-16. Step Response

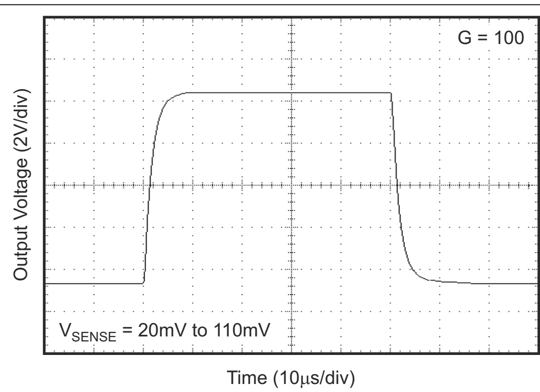


Figure 6-17. Step Response

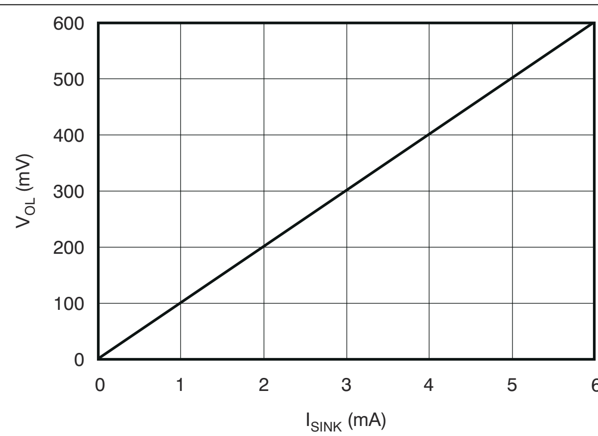


Figure 6-18. Comparator V_{OL} vs I_{SINK}

6.8 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

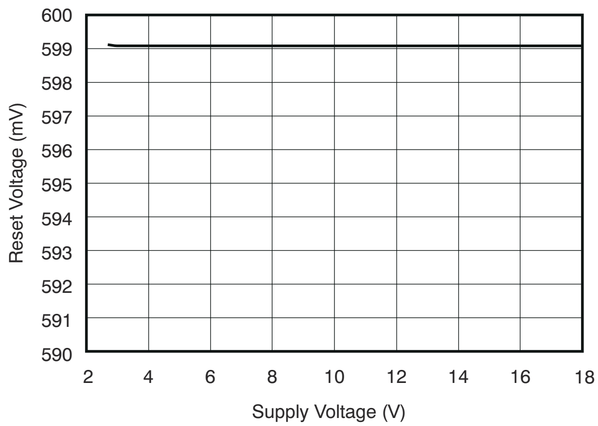


Figure 6-19. Comparator Trip Point vs Supply Voltage

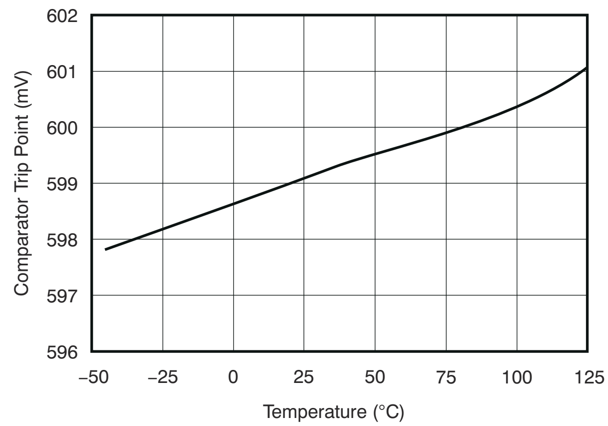


Figure 6-20. Comparator Trip Point vs Temperature

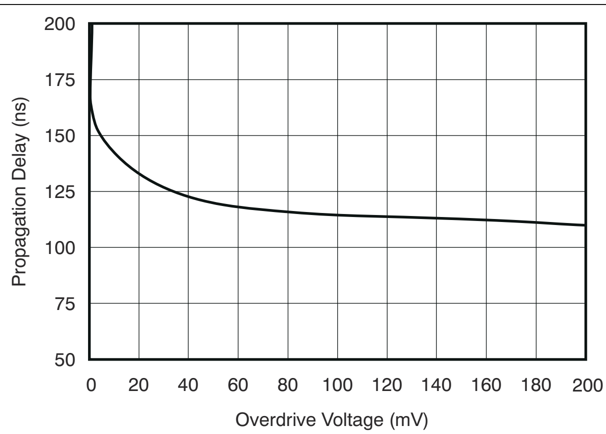


Figure 6-21. Comparator Propagation Delay vs Overdrive Voltage

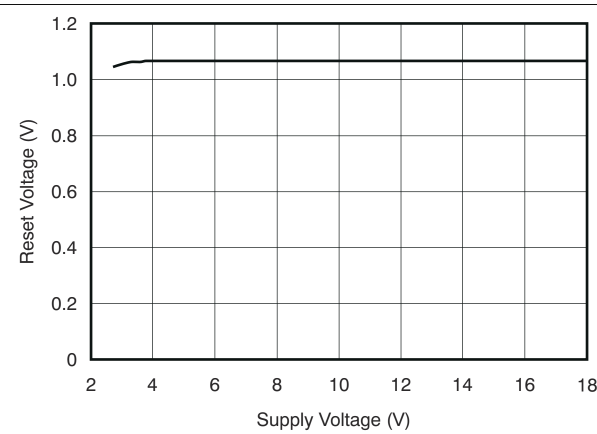


Figure 6-22. Comparator Reset Voltage vs Supply Voltage

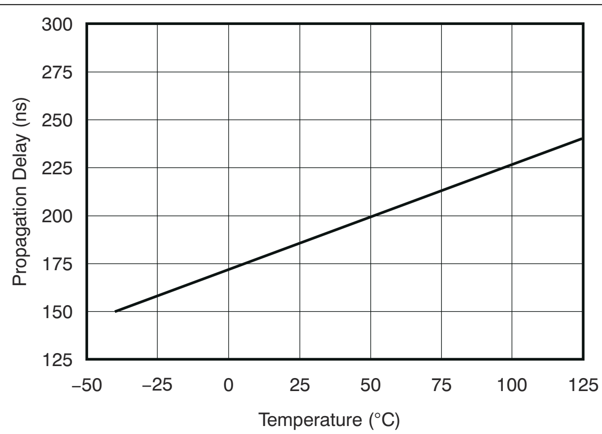


Figure 6-23. Comparator Propagation Delay vs Temperature

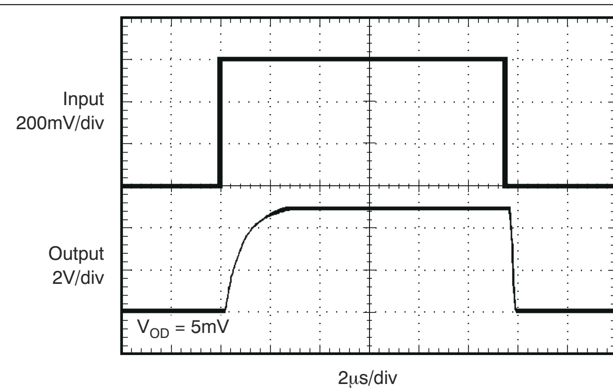


Figure 6-24. Comparator Propagation Delay

7 Parameter Measurement Information

7.1 Hysteresis

Figure 7-1 shows the typical comparator hysteresis.

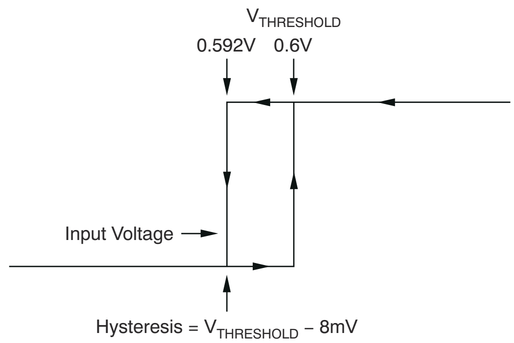


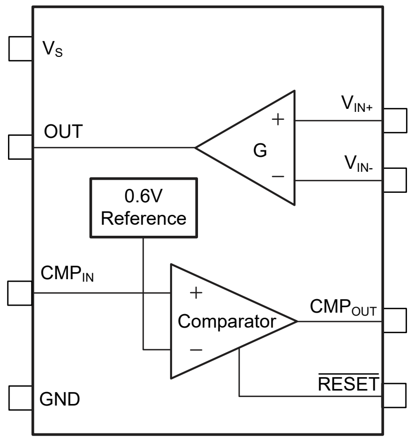
Figure 7-1. Typical Comparator Hysteresis

8 Detailed Description

8.1 Overview

The INA20x-Q1 current-shunt monitors operate over a wide common-mode voltage range (–16 V to +80 V). These devices integrate an open-drain comparator with an internal 0.6-V reference at the negative input. Use external dividers from the output of the current shunt monitor to the positive input of the comparator to set the positive input for overcurrent detection. The comparator includes a latching capability, but can also be made transparent by grounding (or floating) the $\overline{\text{RESET}}$ pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Comparator

The INA200-Q1, INA201-Q1, and INA202-Q1 devices incorporate an open-drain comparator. This comparator typically has 2 mV of offset and a 1.3 µs (typical) response time. The $\overline{\text{RESET}}$ pin latches and resets the output of the comparator; see Figure 8-1.

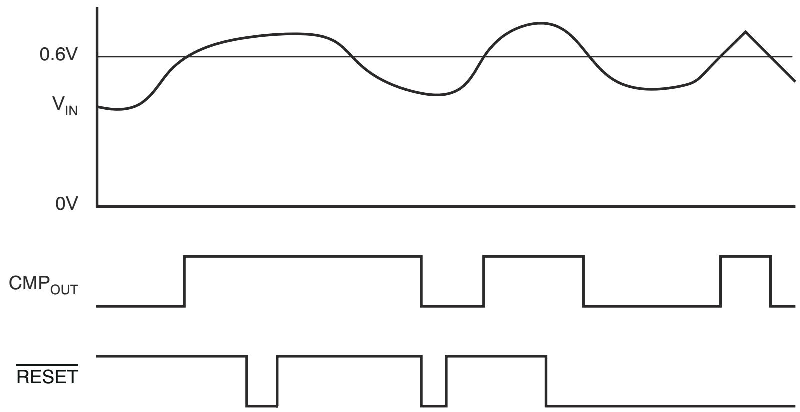


Figure 8-1. Comparator Latching Capability

8.3.2 Output Voltage Range

The output of the INA20x-Q1 is accurate within the output voltage swing range set by the power supply pin, V_S. Best illustration of this performance occurs when using the INA202-Q1 (gain-of-100 version), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of 10 V, and a power-supply voltage sufficient to achieve 10 V on the output.

8.4 Device Functional Modes

The INA20x-Q1 have a single functional mode and are operational when the power-supply voltage is greater than 2.7 V. The common-mode voltage must be between –16 V and +80 V. The maximum power supply voltage for the INA20x-Q1 is 18 V.

9 Application Information

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The INA20x-Q1 series is designed to enable easy configuration for detecting overcurrent conditions and current monitoring in an application. This device is individually targeted towards overcurrent detection of a single threshold. However, this device can also be paired with additional devices and circuitry to create more complex monitoring functional blocks.

9.1.1 Basic Connections

Figure 9-1 shows the basic connections of the INA200-Q1, INA201-Q1, and INA202-Q1. Connect the input pins, V_{IN+} and $V_{IN–}$, as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Stability requires the use of power-supply bypass capacitors. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

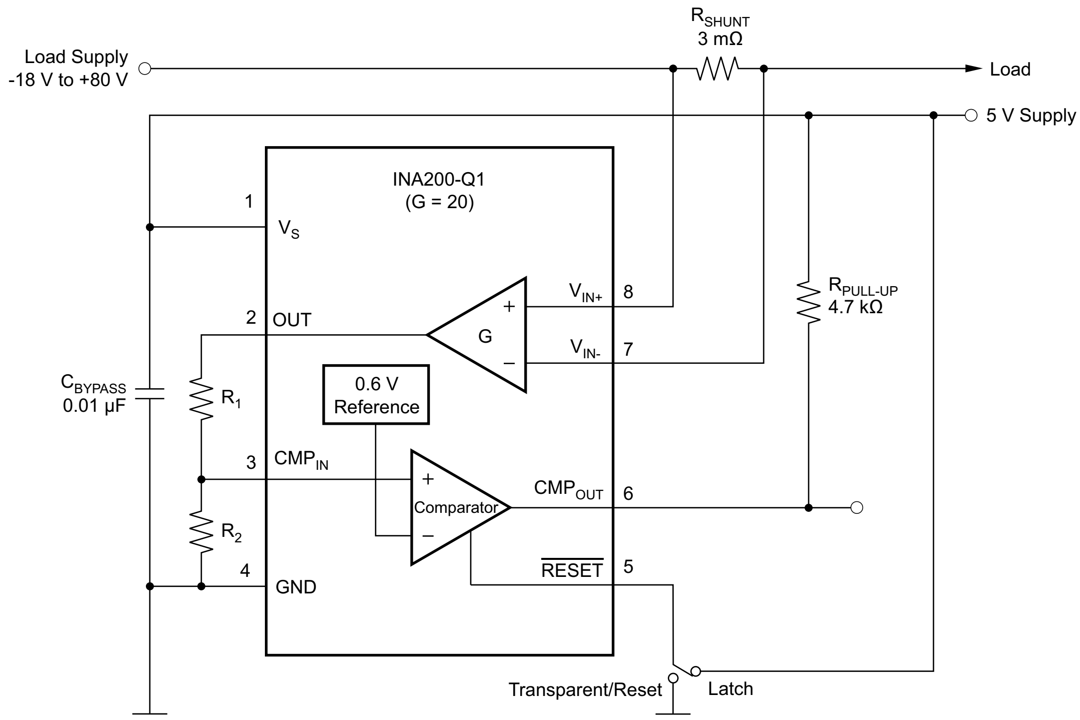


Figure 9-1. INA200-Q1 Basic Connections

9.1.2 Selecting R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, whereas low values of R_S minimize voltage loss in the supply line. Most applications attain best performance with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is 500 mV, but output voltage is limited by supply.

9.1.3 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA20x-Q1 series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA20x-Q1, but the internal 5-kΩ + 30% input impedance complicates input filtering, as illustrated in Figure 9-2. Use the lowest possible resistor values to minimize both the initial shift in gain and effects of tolerance. Equation 1 gives the effect on initial gain:

$$\text{Gain Error }\% = 100 - \left(100 \times \frac{5k\Omega}{5k\Omega + R_{FILT}}\right) \tag{1}$$

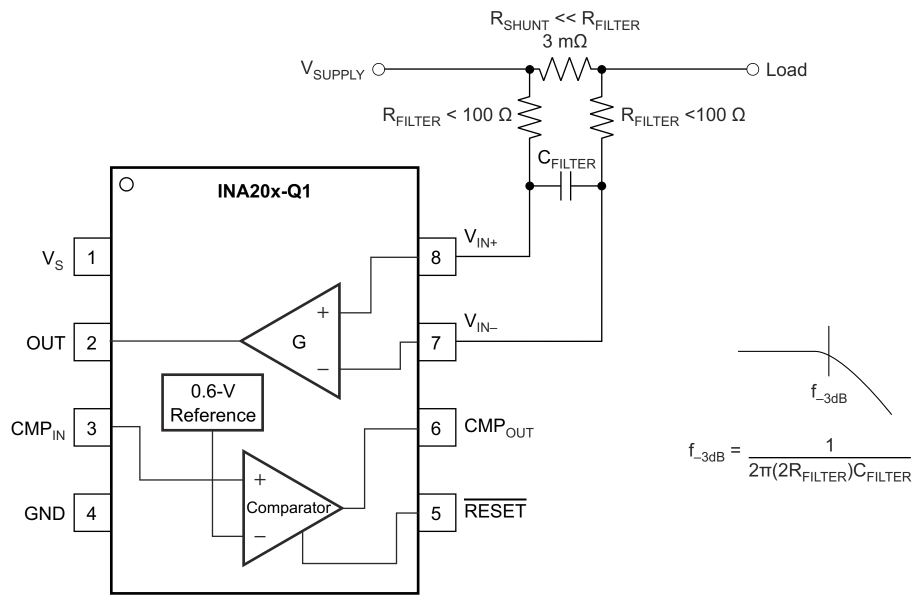


Figure 9-2. Input Filter

To calculate the total effect on gain error, replace the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). One can also be insert the tolerance extremes of R_{FILT} into the equation. If using a pair of 100-Ω 1% resistors on the inputs, the initial gain error is 1.96%. Worst-case tolerance conditions always occur at the lower excursion of the internal 5-kΩ resistor (3.5-kΩ), and the higher excursion of R_{FILT} + 3% in this case.

Note that one must then combine the specified accuracy of the INA20x-Q1 in addition to these tolerances. Although this discussion treated worst-case accuracy conditions by combining the extremes of the resistor values, it is appropriate to use geometric-mean or root-sum-square calculations to total the effects of accuracy variations.

9.1.4 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA20x-Q1 current-shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} - V_{IN-}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. The expression for V_{CM} is ($V_{IN+} + V_{IN-}$) / 2; however, in practice, V_{CM} is effectively the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, –16 V ≤ $V_{CM} < 0$

- Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0V ≤ V_{CM} ≤ V_S
- Low V_{SENSE} Case 3: V_{SENSE} < 20 mV, V_S < V_{CM} ≤ 80 V

9.1.4.1 Normal Case 1: V_{SENSE} ≥ 20 mV, V_{CM} ≥ V_S

This region of operation provides the highest accuracy. Here, use of a two-step method characterizes and measures the input offset voltage. First, Equation 2 determines the gain.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV - 20mV} \tag{2}$$

where:

V_{OUT1} = output voltage with V_{SENSE} = 100 mV

V_{OUT2} = output voltage with V_{SENSE} = 20 mV

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 3.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left(\frac{V_{OUT1}}{G}\right) - 100mV \tag{3}$$

In the *Typical Characteristics*, Figure 6-6 (*Output Error versus Common-Mode Voltage* curve) shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V; for V_{CM} ≥ 12 V, the output error is at its minimum. Using this case also creates the V_{SENSE} ≥ 20 mV output specifications in the *Electrical Characteristics: Current-Shunt Monitor* table.

9.1.4.2 Normal Case 2: V_{SENSE} ≥ 20 mV, V_{CM} < V_S

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the Figure 6-6 *(Output Error versus Common-Mode Voltage* curve). As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the output error increases as V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

9.1.4.3 Low V_{SENSE} Case 1: V_{SENSE} < 20 mV, –16 V ≤ V_{CM} < 0 V; and Low V_{SENSE} Case 3: V_{SENSE} < 20 mV, V_S < V_{CM} ≤ 80 V

Although not designed for accurate operation in either of these regions, the INA20x-Q1 family of devices may have exposure to these conditions in some applications. For example, when monitoring power supplies being switched on and off with V_S still applied to the INA20x-Q1, it is important to know what the device behavior is in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy, as specified in the *Electrical Characteristics: Current-Shunt Monitor*. Figure 9-3 illustrates this effect using the INA202-Q1 (gain = 100).

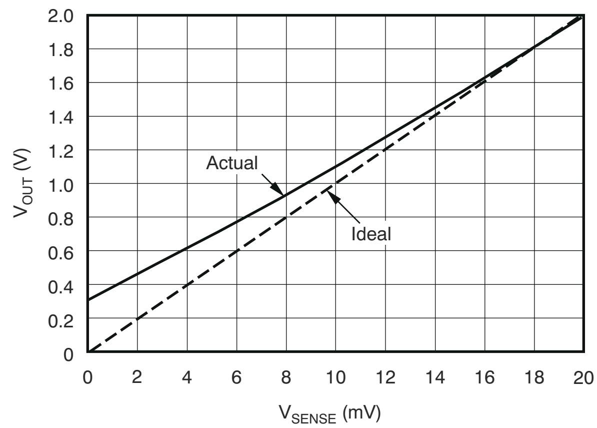
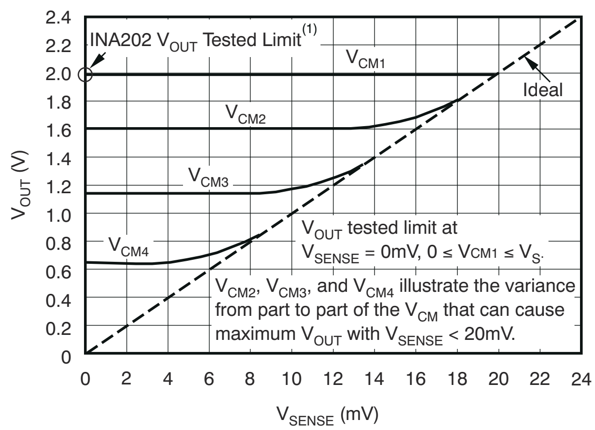


Figure 9-3. Example for Low V_{SENSE} Cases 1 and 3 (INA202-Q1, Gain = 100)

9.1.4.4 Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0 V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA20x-Q1 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive-input common-mode voltage range, and the other in the negative-input region. For this case, neither of these two internal amplifiers dominates, and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for *normal case 2*. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that described by *normal case 2*. Figure 9-4 illustrates this behavior for the INA202-Q1. To test the V_{OUT} maximum peak for this case, maintain a constant V_S, set V_{SENSE} = 0 mV, and sweep V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this test varies from part to part, but the tested V_{OUT} maximum peak for any part is less than the specified V_{OUT} test limit.



NOTE: (1) INA200 V_{OUT} Tested Limit = 0.4V. INA201 V_{OUT} Tested Limit = 1V.

Figure 9-4. Example for Low V_{SENSE} Case 2 (INA202-Q1, Gain = 100)

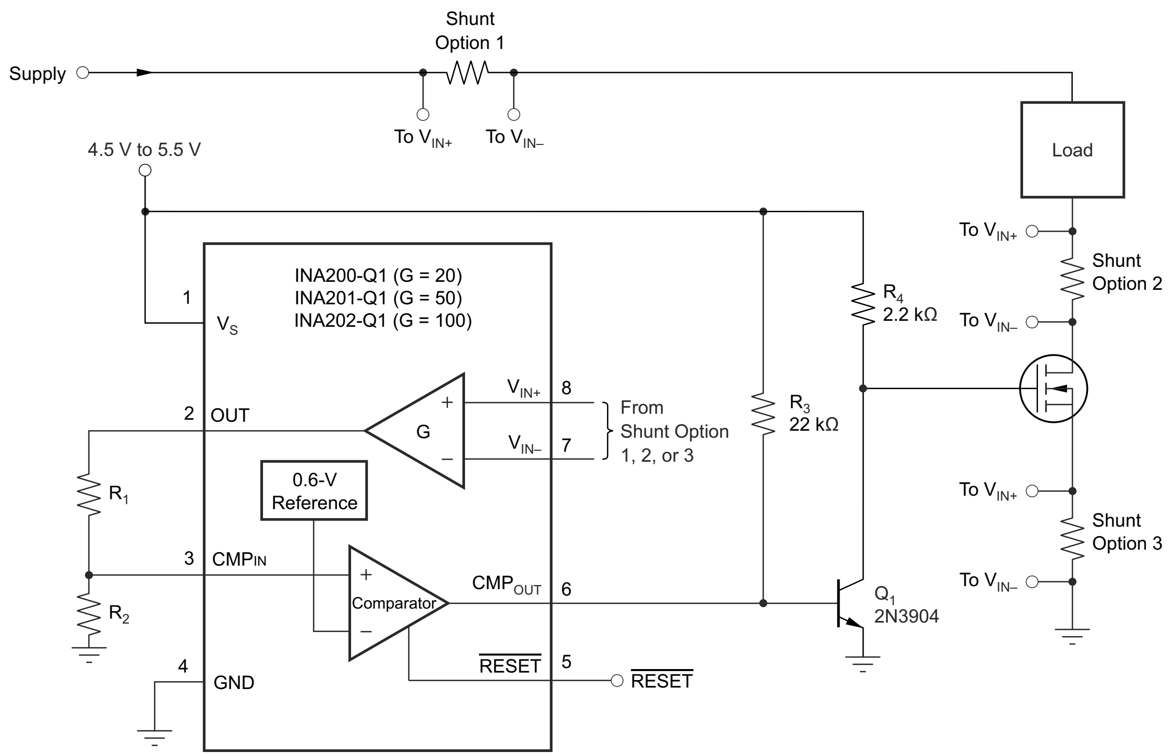
9.1.5 Transient Protection

The –16-V to +80-V common-mode range of the INA20X-Q1 is ideal for withstanding automotive fault conditions, ranging from 12-V battery reversal up to 80-V transients, because there is need for additional protective components up to those levels. In the event that the INA20x-Q1 are exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (such as Zeners) is necessary. Do not use metal-oxide varistors (MOVs) or voltage-dependent resistors (VDRs) except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it never allows exposure of the INA20X-Q1 to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage due to transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA20x-Q1 do not lend themselves to using external resistors in series with the inputs, because the internal gain resistors can vary up to ±30%. (If gain accuracy is not important, then one can add resistors in series with the INA20x-Q1 inputs with two equal resistors on each input.)

9.2 Typical Applications

9.2.1 Low-Side Switch Overcurrent Shutdown

The INA20x-Q1 measures current through a resistive shunt with current flowing in one direction, thus enabling detection of an overcurrent event only when the differential input voltage exceeds the threshold limit. When the current reaches the set limit of the divider R_1 / R_2, the output of CMP_{OUT} transitions high and Q1 turns on and pull the gate of the Pass-FET low and turn off the flow off current.



NOTE: In this case, Q1 is used to invert the comparator output.

Figure 9-5. Low-Side Switch Overcurrent Shutdown

9.2.1.1 Design Requirements

For this design example, use the input parameters shown in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, V_S	3.3 V
R_2 / R_1	1.5
R2	15 kΩ
R1	10 kΩ
Gain	20 V/V (INA200-Q1)
Shunt resistor, R_{SHUNT}	50 mΩ
Desired trip current, I_{TRIP}	1 A

9.2.1.2 Detailed Design Procedure

Figure 9-5 shows the basic connections for a low-side, switch overcurrent shutdown application. Connect input pins IN+ and IN– as close as possible to the current-sensing resistor (R_{SHUNT}) to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input pins can result in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor can differ from the voltage reaching the input pins. Connect the input pins to one of the three shunt options shown in Figure 9-5.

Use the device gain and shunt resistor value to calculate the OUT pin voltage, V_{OUT_TRIP}, for the desired trip current, as shown in Equation 4:

$$V_{OUT\_TRIP} = I_{TRIP} \times R_{SHUNT} \times Gain \quad (4)$$

where

- I_{TRIP} = Desired trip current
- R_{SHUNT} = Shunt resistor value

Configure R_1 and R_2 so that the current trip point is equal to the 0.6-V reference voltage, as shown in Equation 5:

$$R_2 / (R_1 + R_2) \times V_{OUT\_TRIP} = 0.6\ V \quad (5)$$

9.2.1.3 Application Curves

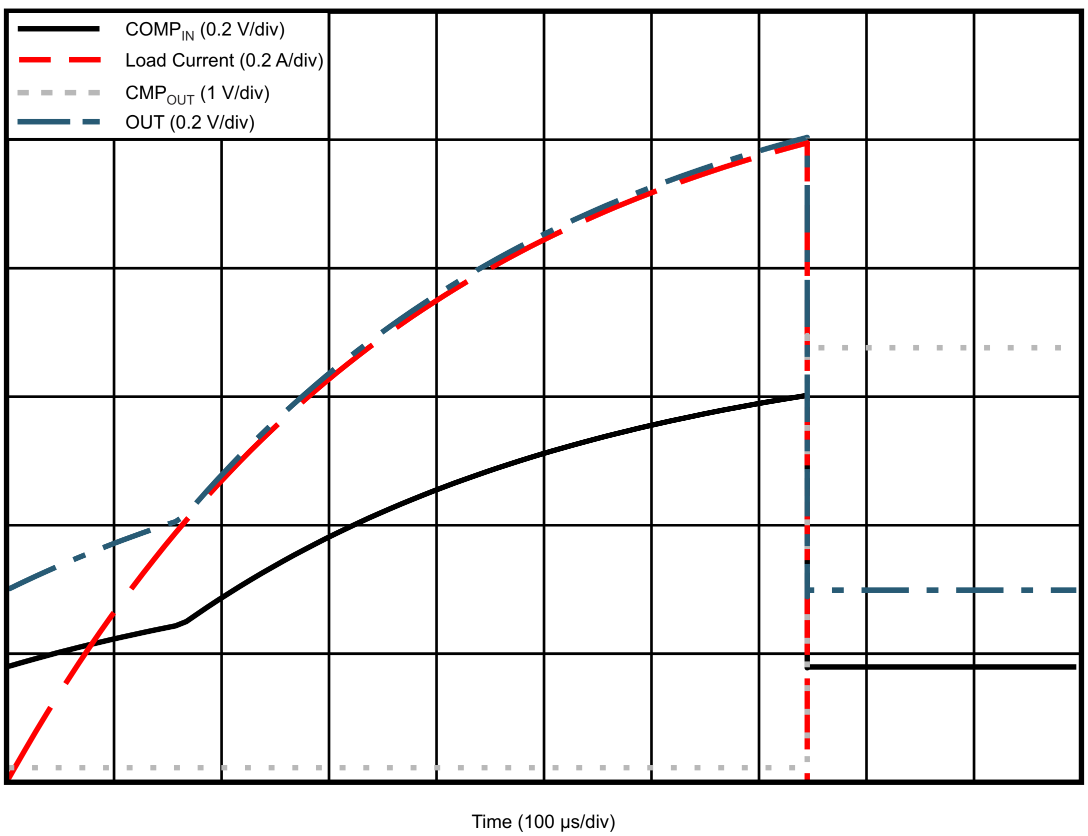
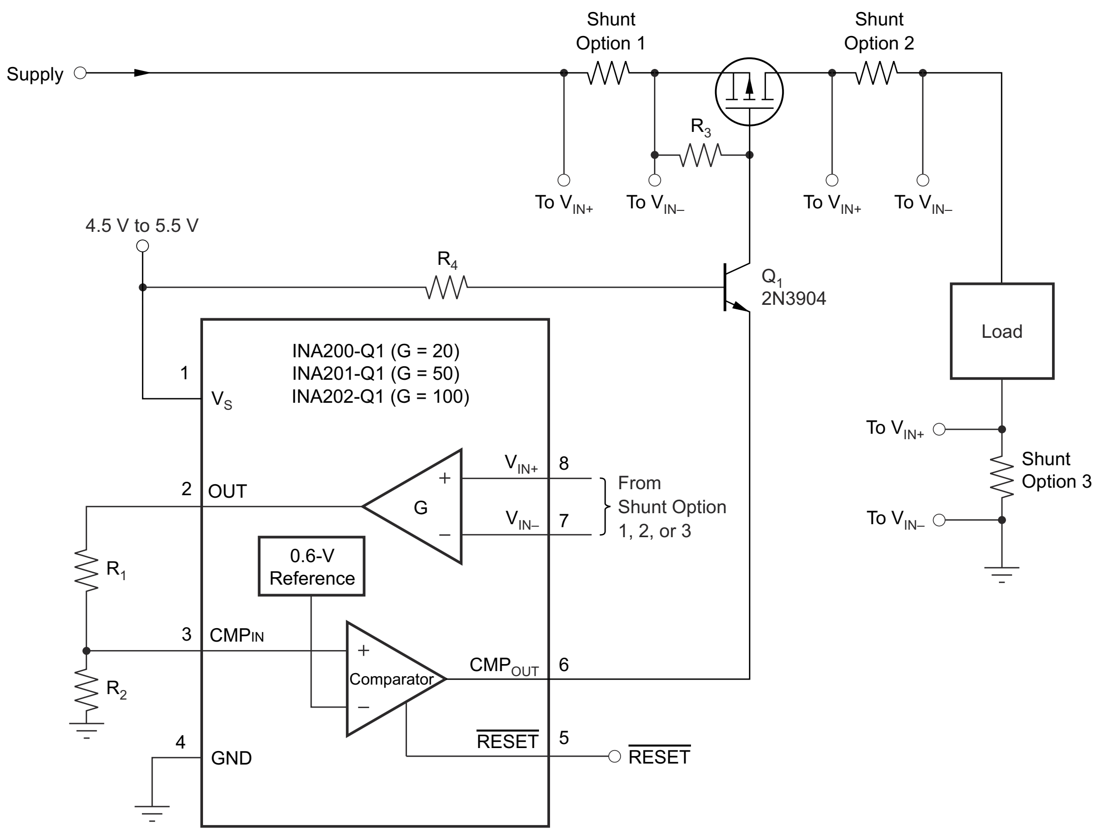


Figure 9-6. Low-Side Switch Overcurrent Shutdown Response

9.2.2 High-Side Switch Overcurrent Shutdown

Figure 9-7 shows the basic connection for a high-side, switch overcurrent shutdown application. The high-side PMOS switch disconnects when an overcurrent event occurs. The previous *Detailed Design Procedure* section describes how to apply this application example. The difference is that the current is sensed on the high side of the bus in this application, and the low side of the bus in the previous application example.

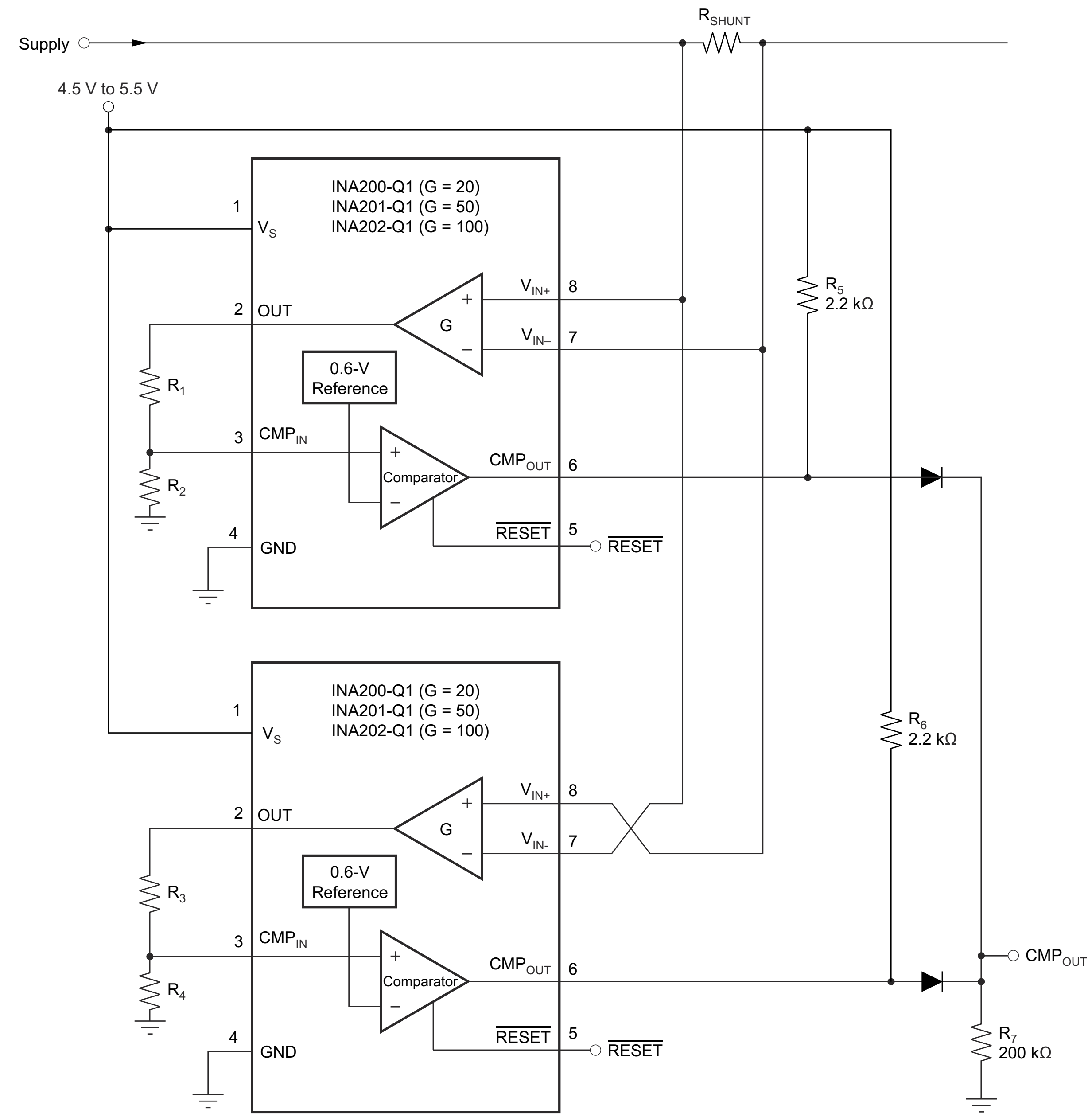


NOTE: Q cascodes the comparator output to drive a high-side FET (the 2N3904 shown is good up to 60 V). The shunt can be located in any one of the three locations shown. Use the latching capability in shutdown applications to prevent oscillation at the trip point.

Figure 9-7. High-Side Switch Overcurrent Shutdown

9.2.3 Bidirectional Overcurrent Comparator

Figure 9-8 shows the basic connection for a bidirectional overcurrent comparator using two INA20x-Q1 devices of the same gain.



NOTE: It is possible to set different limits for each direction.

Figure 9-8. Bidirectional Overcurrent Comparator

9.3 Power Supply Recommendations

The input circuitry of the INA20x-Q1 accurately measures beyond the power-supply voltage, V_S. For example, the V_S power supply can be 5 V, whereas the load power-supply voltage goes up to 80 V. However, the voltages on the power-supply pins limit the output voltage range of the OUT pin.

9.3.1 Output vs Supply Ramp Considerations

Figure 9-9, Figure 9-10, and Figure 9-11 show the typical output voltages for high and low-side configurations with the given ramp supply voltage. These fluctuations on the output during power-up may require a controller to incorporate a blanking time to disregard the artifacts.

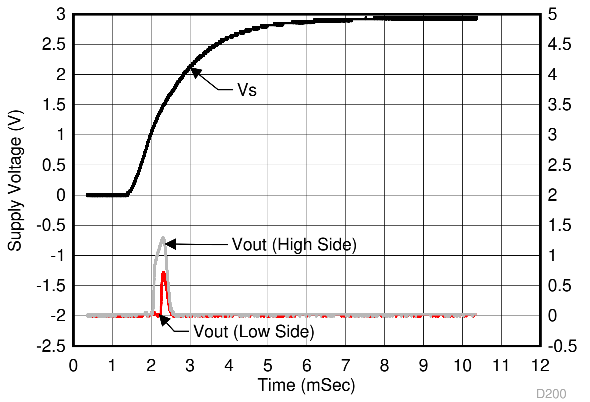


Figure 9-9. Analog Output vs Supply Ramp (INA200)

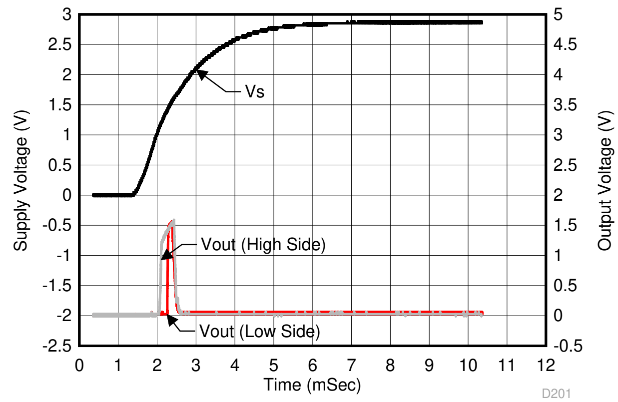


Figure 9-10. Analog Output vs Supply Ramp (INA201)

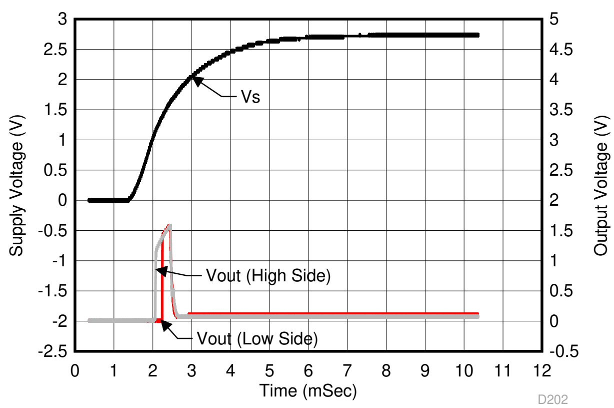


Figure 9-11. Analog Output vs Supply Ramp (INA202)

9.4 Layout

9.4.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or four-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Add additional decoupling capacitance to compensate for noisy or high-impedance power supplies.

9.4.2 Layout Example

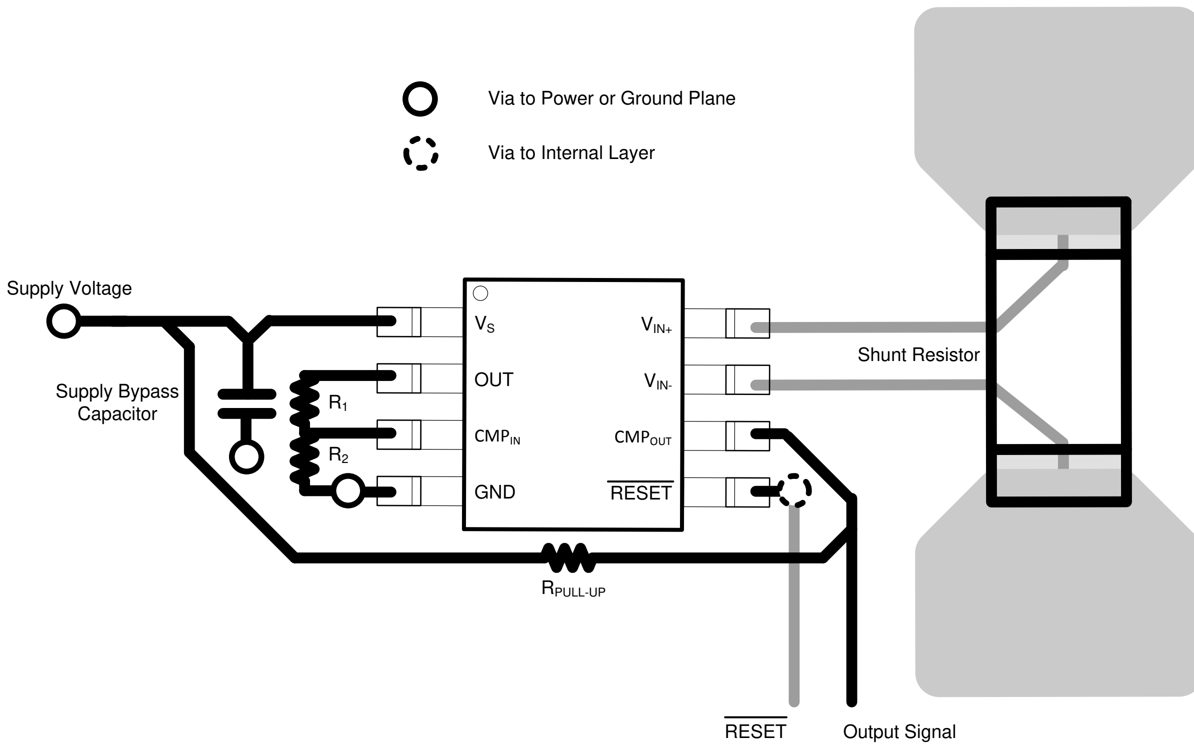


Figure 9-12. INA20x-Q1 Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2016) to Revision D (April 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *Device Information* table to *Package Information*	1
• Removed sentence from *Design Requirements*: All other register settings are default	19
• Changed Shunt resistor, R_{SHUNT} value in *Design Parameters* table from: 5 mΩ to: 50 mΩ	19
• Added *Output vs Supply Ramp Considerations* subsection to the *Power Supply Recommendations* section.	23

Changes from Revision B (November 2012) to Revision C (April 2016)	Page
• Added *Device Information* and*ESD Ratings*, and *Thermal Information* tables, and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Updated data sheet title	1
• Updated Features bullets for clarity	1
• Changed MSOP to VSSOP throughout data sheet to match industry-standard term	1
• Updated Applications bullets	1
• Updated Description section text for clarity	1
• Changed all figures in data sheet to show Q1 device names	1
• Changed pin names in Absolute Maximum Ratings to show correct names	4
• Added Operating Temperature to *Absolute Maximum Ratings* table	4
• Changed CMP V_{OUT} to CMP_{OUT} in *large-signal differential voltage gain* parameter condition	6
• Deleted package name from Figure 27	15

- Changed Figure 28 caption 15
- Changed text from "R_{FILT} – 3%" to "R_{FILT} + 3%" in 2nd paragraph of *Input Filtering* section........ 15
- Changed 22-kΩ R_1 resistor to R_3 in Figure 31........ 19

Changes from Revision A (September 2012) to Revision B (October 2012) **Page**

- Changed from Mixed Production status to Production Data........ 1
- Changed device graphic from pair to single........ 1
- Added AEC-Q100 info to *Features* bullets........ 1
- Updated Applications bullets........ 1
- Removed D package from pin configuration image........ 4

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA200AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHZ
INA200AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHZ
INA201AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 125	QWV
INA201AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	QWV
INA202AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SIA
INA202AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SIA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

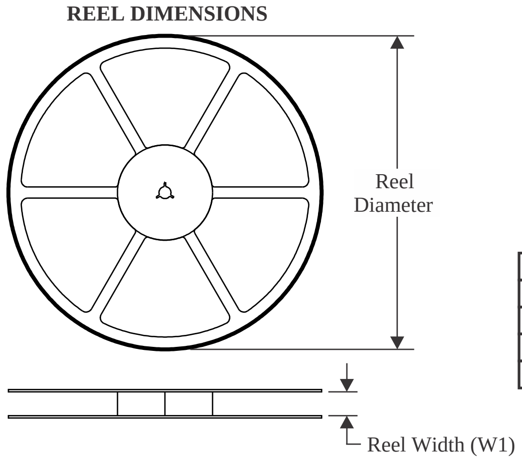
OTHER QUALIFIED VERSIONS OF INA200-Q1, INA201-Q1, INA202-Q1 :

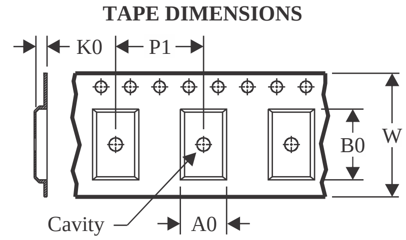
- Catalog : INA200, INA201, INA202

NOTE: Qualified Version Definitions:

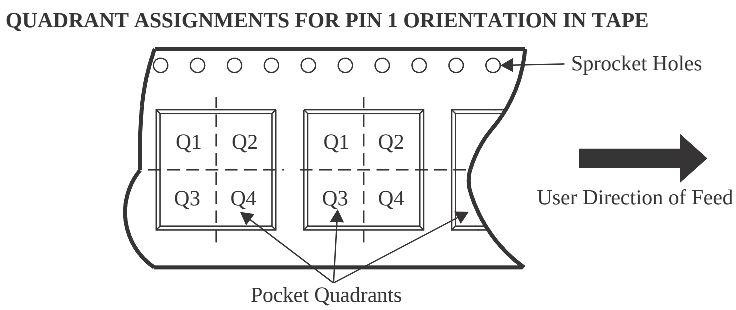
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





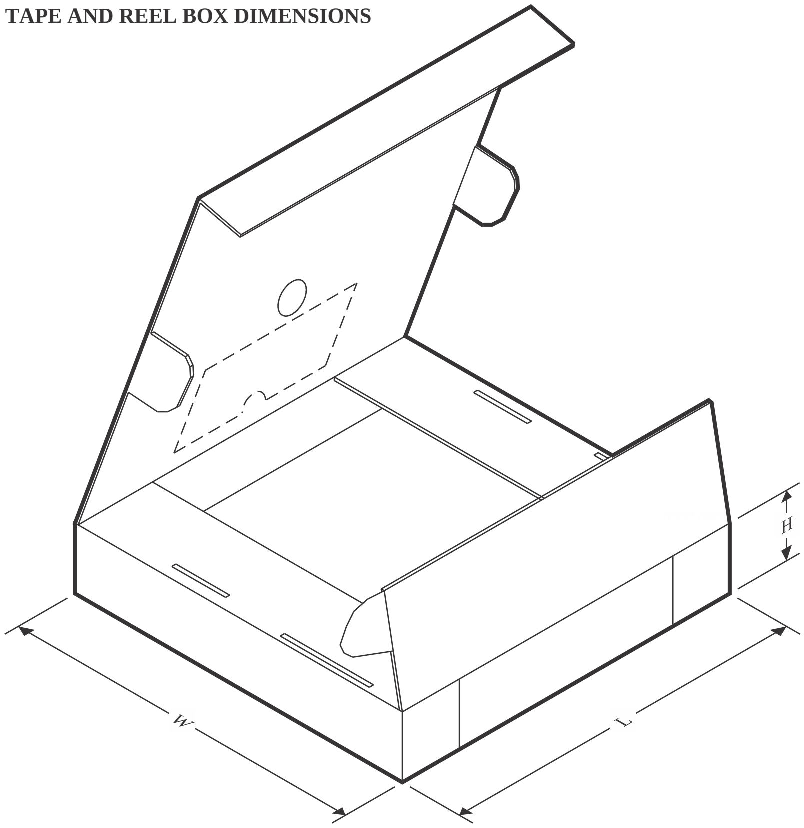
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

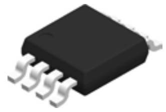
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA200AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA201AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA202AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

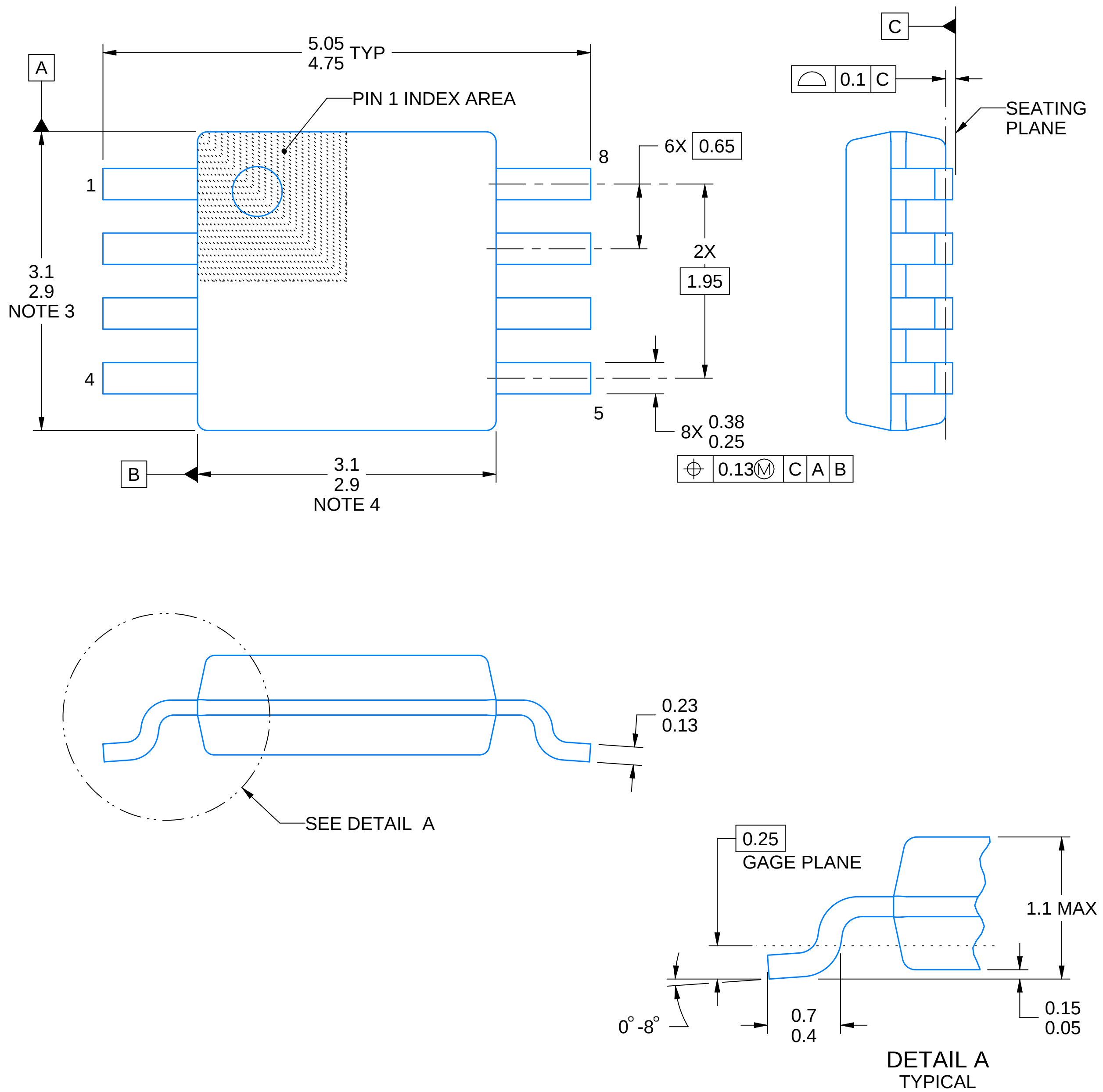
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA200AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA201AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA202AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0



DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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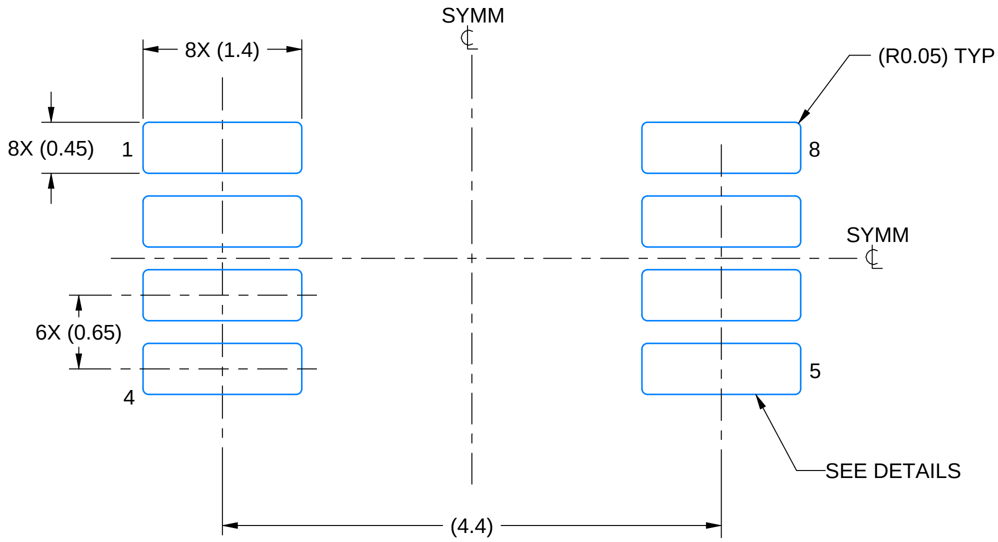
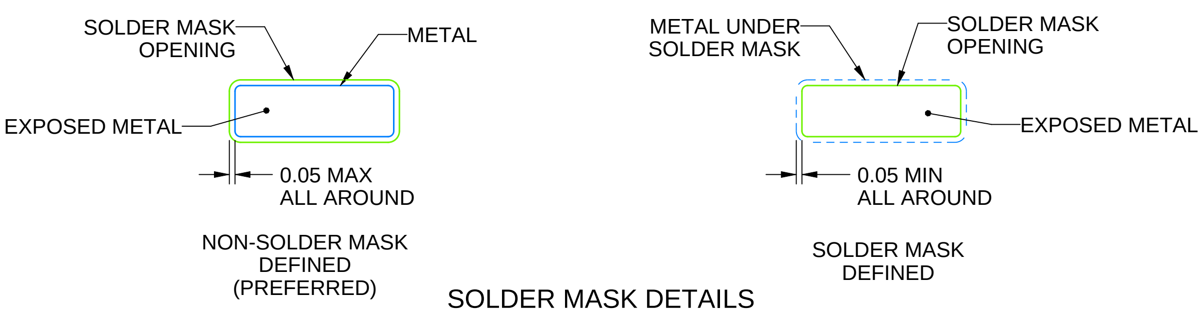
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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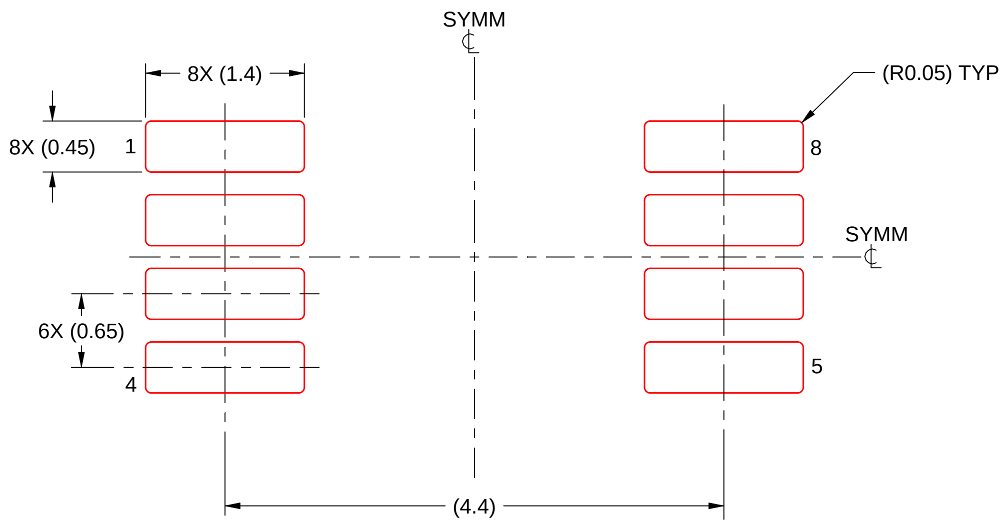
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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