INA148-Q1 ±200-V Common-Mode Voltage Difference Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C6
  - Device MM ESD Classification Level M2
- High Common-Mode Voltage
  - 75 V at V_S = 5 V
  - ±200 V at V_S = ±15 V
- Fixed Differential Gain = 1 V/V
- Low Quiescent Current: 260 µA
- Wide Supply Range
  - Single Supply: 2.7 V to 36 V
  - Dual Supplies: ±1.35 V to ±18 V
- Low Gain Error: 0.075% (Maximum)
- Low Nonlinearity: 0.002% (Maximum)
- High CMR: 86 dB
- Surface-Mount 8-pin SOIC Package

2 Applications

- HEV/EV and Powertrain
- HEV Battery Management
- Automotive Instrumentation
- Current-Shunt Measurements
- Differential Sensor Amplifiers
- Line Receivers
- Battery-Powered Systems
- Stacked-Cell Monitors

3 Description

The INA148-Q1 is a precision, low-power, unity-gain difference amplifier with a high common-mode input voltage range. The device consists of a monolithic, precision, bipolar operational amplifier with a thin-film resistor network.

The on-chip resistors are laser trimmed for an accurate 1-V/V differential gain and high common-mode rejection. Excellent temperature tracking of the resistor network maintains high gain accuracy and common-mode rejection over temperature. The INA148-Q1 operates on single or dual supplies. These features make the INA148-Q1 suitable for HEV/EV and Powertrain applications, specifically in battery management systems.

The INA148-Q1 is available in an 8-pin SOIC, surface-mount package, and is specified for operation over the temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA148-Q1	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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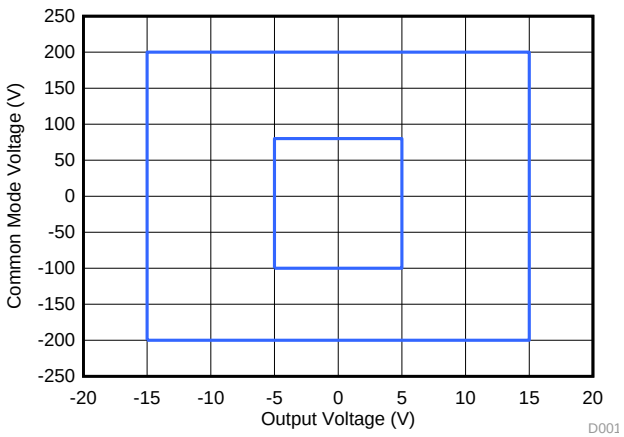
Input Common-Mode Voltage vs Output Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

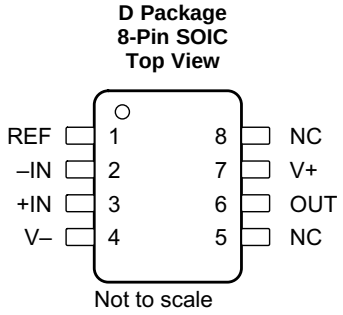
Changes from Revision A (October 2011) to Revision B **Page**

- Added *Device Information* table, *Table of Contents*, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information Table*; see POA at the end of the datasheet ... 1

Changes from Original (March 2009) to Revision A **Page**

- Features Bullet From: Low Quiescent Current: 260 mA To: Low Quiescent Current: 260 µA ... 1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	2	I	Inverting input
NC	5, 8	—	No connection
OUT	6	O	Output voltage
REF	1	I	Reference voltage input
V+	7	I	Positive supply voltage
V–	4	I	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V+ to V–		36	V
Input voltage	Continuous		±200	V
	Peak (0.1 s)		±500	
Short circuit to ground duration		Continuous		
Package thermal impedance, junction to free air			97.1	°C/W
Operating free-air temperature		–40	125	°C
Maximum operating virtual-junction temperature			150	°C
Lead temperature (soldering, 10 s)			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1500	V
		Charged-device model (CDM), per AEC Q100-011	±2000	
		Machine model	±150	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply	2.7	36	V
		Dual supply	±1.35	±18	
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA148-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics Dual Supply

V_S = ±5 V to ±15 V (dual supply), R_L = 10 kΩ to ground, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage(1)(2)	V_{CM} = 0 V	V_S = ±15 V		±1	±5	mV
			V_S = ±5 V		±1	±5	
$\Delta V_{OS}/\Delta T$	Input offset voltage drift(1)	T_A = –40°C to 125°C			±10		µV/°C
PSRR	Power supply ripple rejection(1)	V_S = ±1.35 V to ±18 V, V_{CM} = 0 V			±50	±400	µV/V
V_{CM}	Common-mode voltage range	$V_{+IN} - V_{–IN}$ = 0	V_S = ±15 V	–200		200	V
			V_S = ±5 V	–100		80	
CMRR	Common-mode rejection ratio	V_S = ±15 V, V_{CM} = –200 V to 200 V, R_S = 0 Ω		70	86		dB
		V_S = ±5 V, V_{CM} = –100 V to 80 V, R_S = 0 Ω		70	86		
	Differential input impedance				2		MΩ
	Common-mode input impedance				1		MΩ
V_n	Voltage noise(1)(3)	f = 0.1 Hz to 10 Hz			17		μV_{p-p}
	Voltage noise density(1)(3)	f = 1 kHz			880		$nV/\sqrt{Hz}$
	Initial gain(1)				1		V/V
	Gain error	V_O = (V– + 0.5) to (V+ – 1.5)			±0.01%	±0.075%	
	Gain error over temperature				±3	±10	ppm/°C
	Gain nonlinearity	V_O = (V– + 0.5) to (V+ – 1.5)	V_S = ±15 V		±0.001	±0.002	%FSR
			V_S = ±5 V		±0.001		
	Small-signal bandwidth frequency response				100		kHz
SR	Slew rate				1		V/µs
t_s	Settling time	V_S = ±15 V, 10-V step	0.1%		21		µs
			0.01%		25		
		V_S = ±5 V, 6-V step	0.1%		21		
			0.01%		25		
	Overload recovery	50% input overload			24		µs

(1) Overall difference amplifier configuration. Referred to input pins (V_{+IN} and $V_{–IN}$), gain = 1 V/V.
(2) Includes effects of amplifier's input bias and offset currents.
(3) Includes effects of input current noise and thermal noise contribution of resistor network.

Electrical Characteristics Dual Supply (continued)

V_S = ±5 V to ±15 V (dual supply), R_L = 10 kΩ to ground, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	R_L = 100 kΩ	V– + 0.25		V+ – 1	V
		R_L = 10 kΩ	V– + 0.5		V+ – 1.5	
I_O	Output current	Short-circuit current, continuous to common		±13		mA
C_L	Load capacitance	Stable operation		10		nF
I_S	Supply current	V_{IN} = 0, I_O = 0		±260	±300	µA

6.6 Electrical Characteristics Single Supply

V_S = 5 V (single supply), R_L = 10 kΩ to V_S / 2, V_{REF} = V_S / 2, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage(1)(2)	V_{CM} = V_S / 2			±1	±5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift(1)	T_A = –40°C to 125°C			±10		µV/°C
PSRR	Power supply ripple rejection(1)	V_S = 2.7 V to 36 V, V_{CM} = V_S / 2			±50	±400	µV/V
V_{CM}	Common-mode voltage range	V_{+IN} – $V_{–IN}$ = 0	V_{REF} = 0.25 V	–4		75	V
			V_{REF} = V_S / 2	–47.5		32.5	
CMRR	Common-mode rejection ratio	V_{CM} = –47.5 V to 32.5 V, R_S = 0 Ω		70	86		dB
	Differential input impedance				2		MΩ
	Common-mode input impedance				1		MΩ
V_n	Voltage noise(1)(3)	f = 0.1 Hz to 10 Hz			17		μV_{p-p}
	Voltage noise density(1)(3)	f = 1 kHz			880		nV/√Hz
	Initial gain(1)				1		V/V
	Gain error	V_O = 0.5 V to 3.5 V			±0.01%	±0.075%	
	Gain error over temperature				±3	±10	ppm/°C
	Gain nonlinearity	V_O = 0.5 V to 3.5 V			±0.001		%FSR
	Small-signal bandwidth				100		kHz
SR	Slew rate				1		V/µs
t_s	Settling time	V_S = 5 V, 3-V step	0.1%		21		µs
			0.01%		25		
	Overload recovery	50% input overload			13		µs
V_O	Output voltage	R_L = 100 kΩ		V– + 0.25		V+ – 1	V
		R_L = 10 kΩ		V– + 0.5		V+ – 1.5	
I_O	Output current	Short-circuit current, continuous to common			±8		mA
C_L	Load capacitance	Stable operation			10		nF
I_Q	Quiescent current	V_{IN} = 0, I_O = 0			260	300	µA

(1) Overall difference amplifier configuration. Referred to input pins (V_{+IN} and $V_{–IN}$), gain = 1 V/V.
(2) Includes effects of amplifier's input bias and offset currents.
(3) Includes effects of input current noise and thermal noise contribution of resistor network.

6.7 Typical Characteristics

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

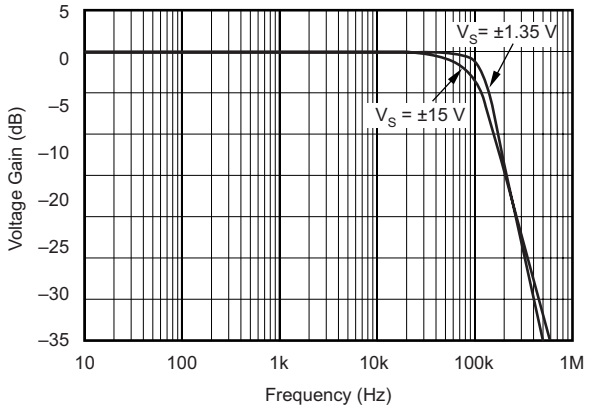


Figure 1. Gain vs Frequency

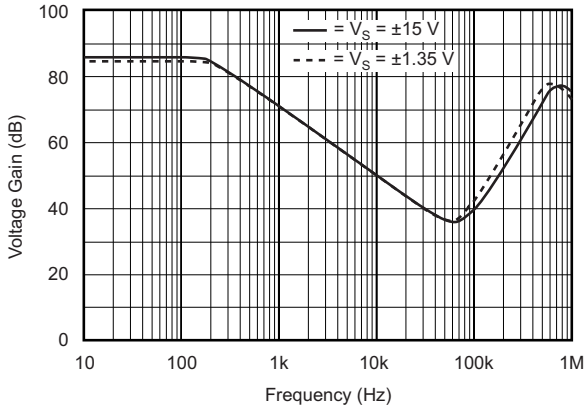


Figure 2. Common-Mode Rejection vs Frequency

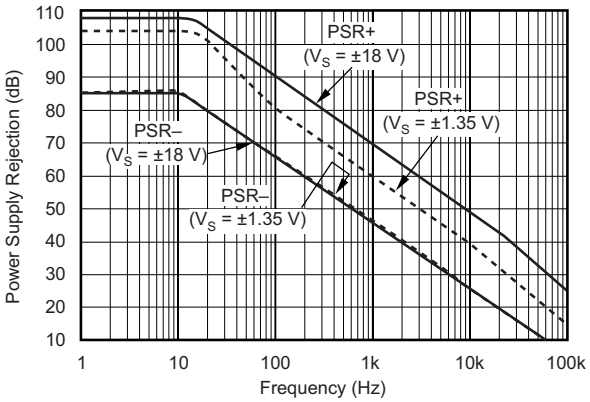


Figure 3. Power Supply Rejection vs Frequency

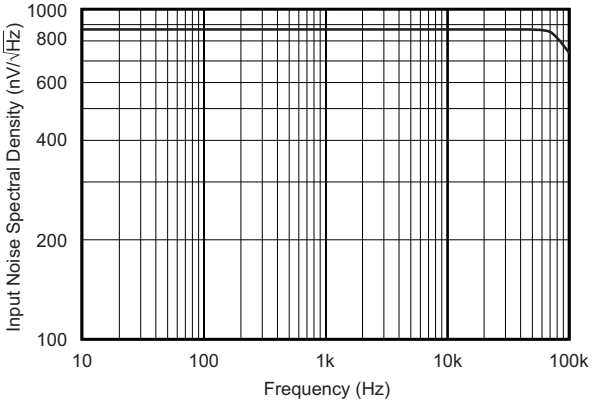


Figure 4. Input Voltage Noise Spectral Density

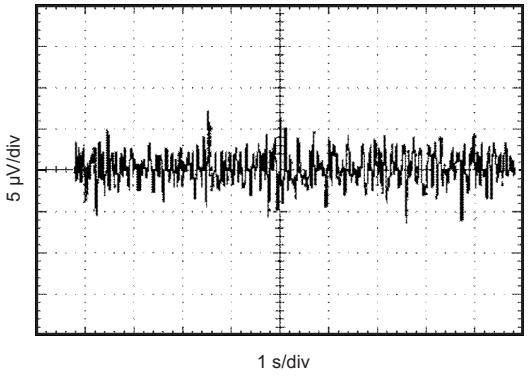


Figure 5. Voltage Noise (RTI)

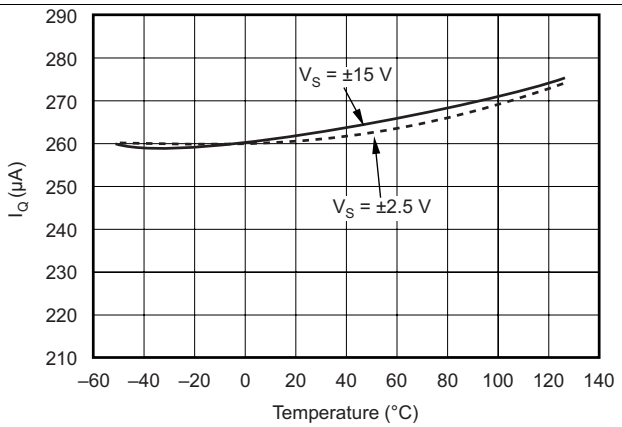


Figure 6. Quiescent Current vs Temperature

Typical Characteristics (continued)

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

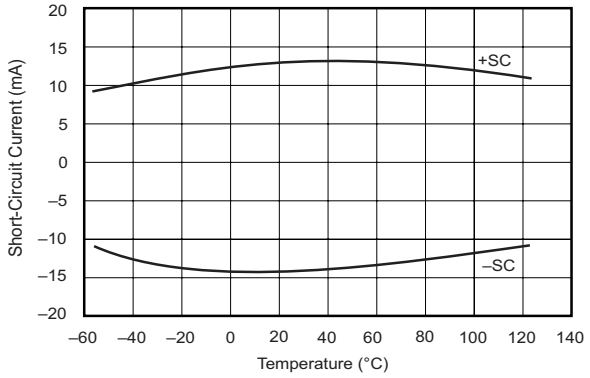


Figure 7. Short-Circuit Current vs Temperature

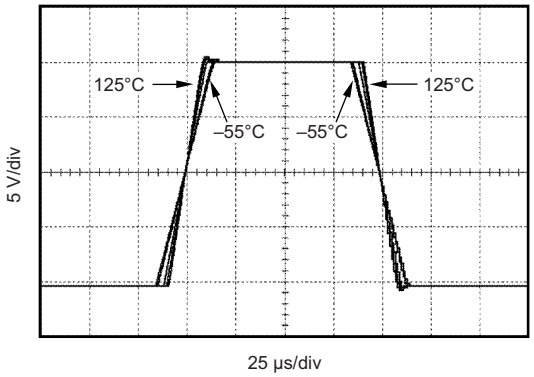


Figure 8. Large-Signal Step Response vs Temperature

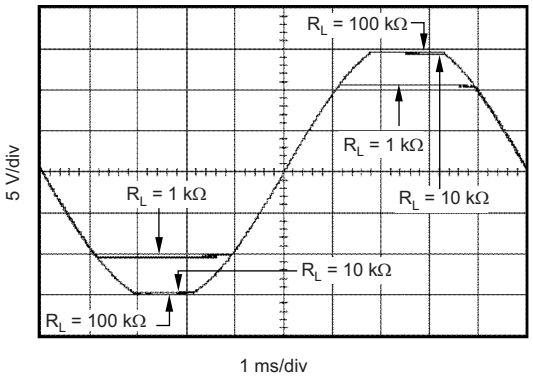


Figure 9. Output Voltage Swings vs R_L

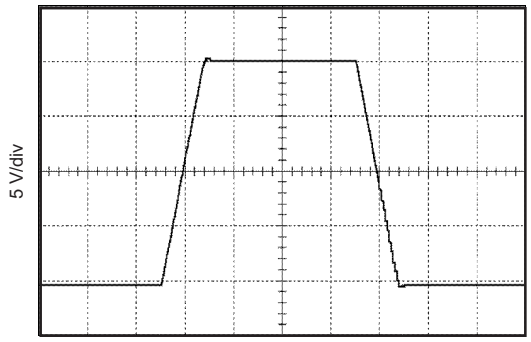


Figure 10. Large-Signal Step Response

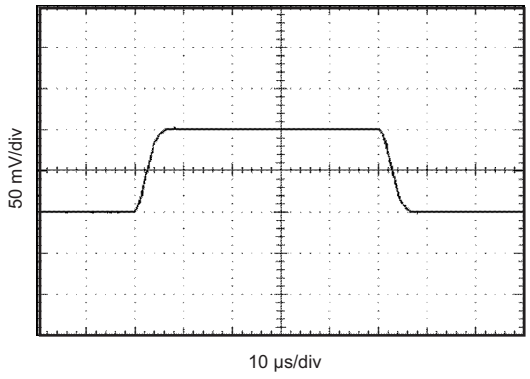


Figure 11. Small-Signal Step Response

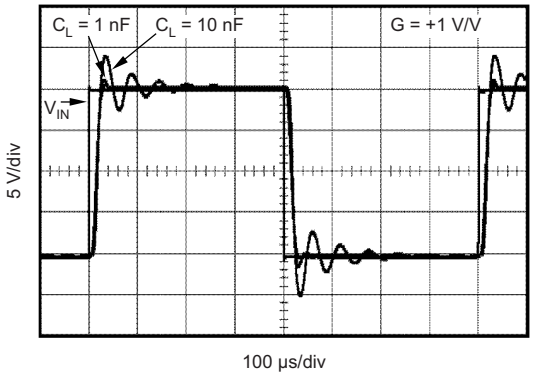


Figure 12. Large-Signal Capacitive Load Response

Typical Characteristics (continued)

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

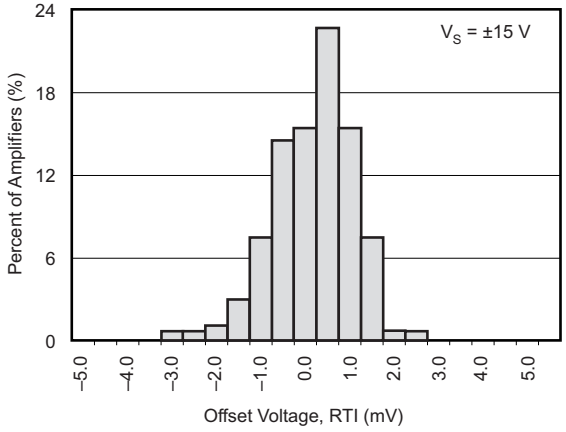


Figure 13. Offset Voltage Production Distribution

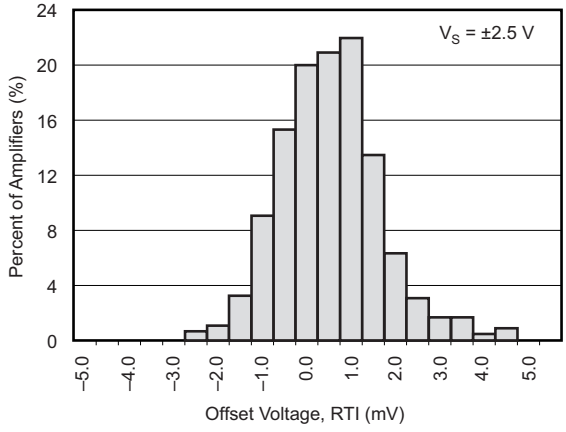


Figure 14. Offset Voltage Production Distribution

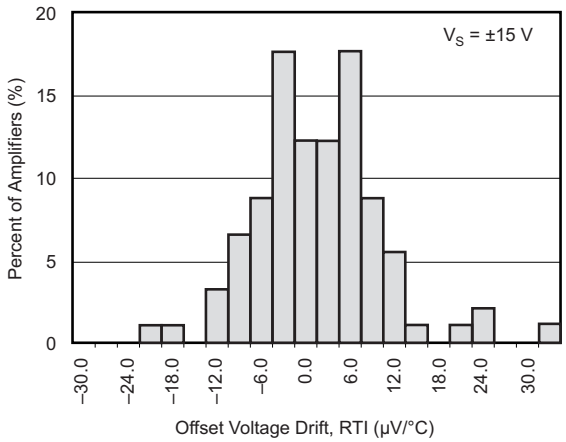


Figure 15. Offset Voltage Drift Production Distribution

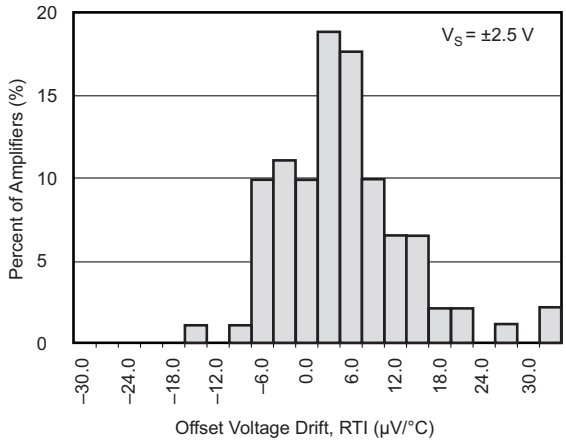


Figure 16. Offset Voltage Drift Production Distribution

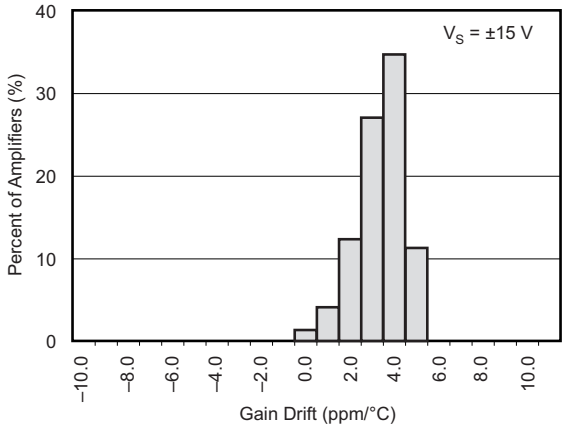


Figure 17. Gain Drift Production Distribution

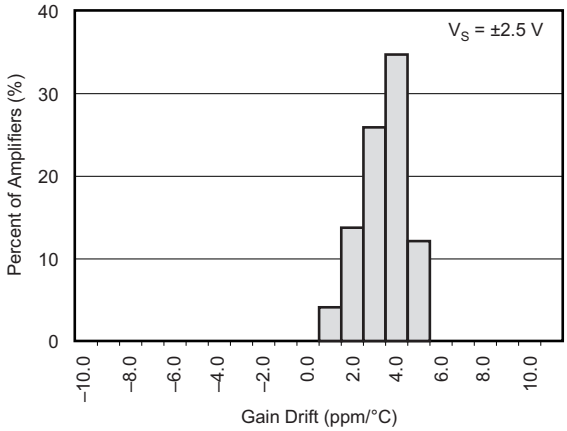


Figure 18. Gain Drift Production Distribution

Typical Characteristics (continued)

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

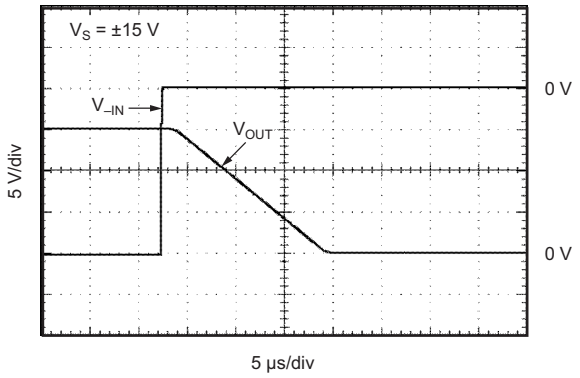


Figure 19. Inverting Input 50% Overload Recovery Time

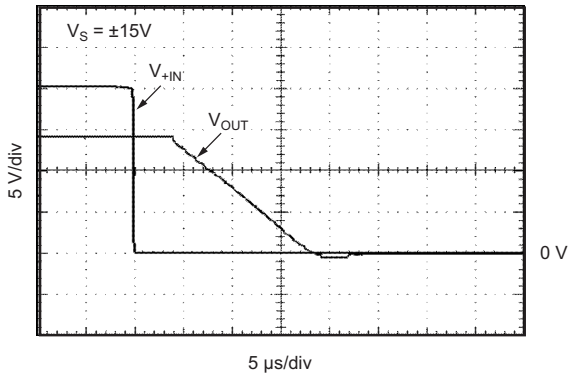


Figure 20. Noninverting Input 50% Overload Recovery Time

7 Detailed Description

7.1 Overview

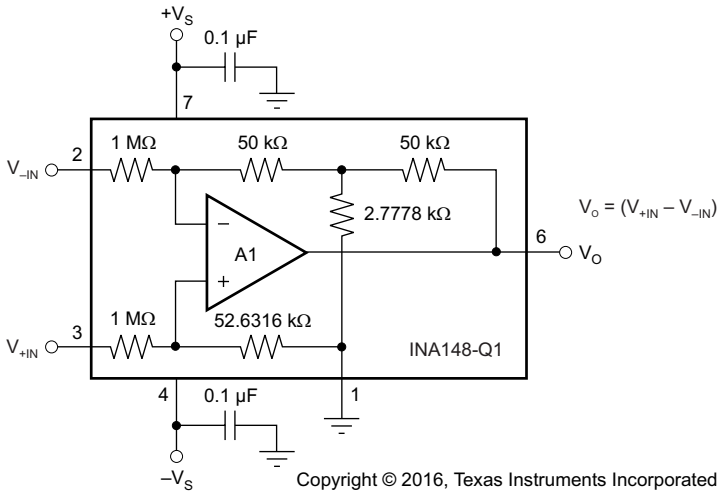
The INA148-Q1 is a unity-gain difference amplifier with a high common-mode input voltage range. To achieve its high common-mode voltage range, the INA148-Q1 features a precision, laser-trimmed, thin-film resistor network with a 20:1 input voltage divider ratio. High input voltages are thereby reduced in amplitude, delivering input voltages to the op amp that are within its linear operating range. A *Tee* network in the op amp feedback network places the amplifier in a gain of 20 V/V, restoring the overall circuit gain to unity (1 V/V).

External voltages can be summed into the amplifier's output by using the REF pin, making the differential amplifier a highly versatile design tool. Voltages on the REF pin also influence the INA148-Q1's common-mode voltage range.

In accordance with good engineering practice for linear integrated circuits, the INA148-Q1's power-supply bypass capacitors must be connected as close to the supply pins (V+ and V–) as practical. TI recommends ceramic or tantalum capacitors for use as bypass capacitors.

The input impedances are unusually high for a difference amplifier and this must be considered when routing input signal traces on a PCB. Avoid placing digital signal traces near the difference amplifier's input traces to minimize noise pickup.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The INA148-Q1 is specified for ±15-V and ±5-V dual supplies and 5-V single supplies. The INA148-Q1 can be operated with single or dual supplies with excellent performance.

The INA148-Q1 is fully characterized for supply voltages from ±1.35 V to ±18 V and over temperatures of –40°C to 125°C. Parameters that vary significantly with operating voltage, load conditions, or temperature are shown in *Typical Characteristics*.

7.3.2 Gain Equation

An internal on-chip resistor network sets the overall differential gain of the INA148-Q1 to precisely 1 V/V. Equation 1 shows the output.

$$V_O = (V_{+IN} – V_{–IN}) + V_{REF} \quad (1)$$

Feature Description (continued)

7.3.3 Common-Mode Range

The 20:1 input resistor ratio of the INA148-Q1 provides an input common-mode range that extends well beyond its power supply rails.

The exact input voltage range depends on the amplifier's power-supply voltage and the voltage applied to the REF pin. See *Typical Applications* for typical input voltage ranges at different power supply voltages.

7.3.4 Offset Trim

The INA148-Q1 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment.

Because a voltage applied to the reference (REF) pin is summed directly into the amplifier's output signal, this technique can be used to null the amplifier's input offset voltage. Figure 21 shows an optional circuit for trimming the offset voltage.

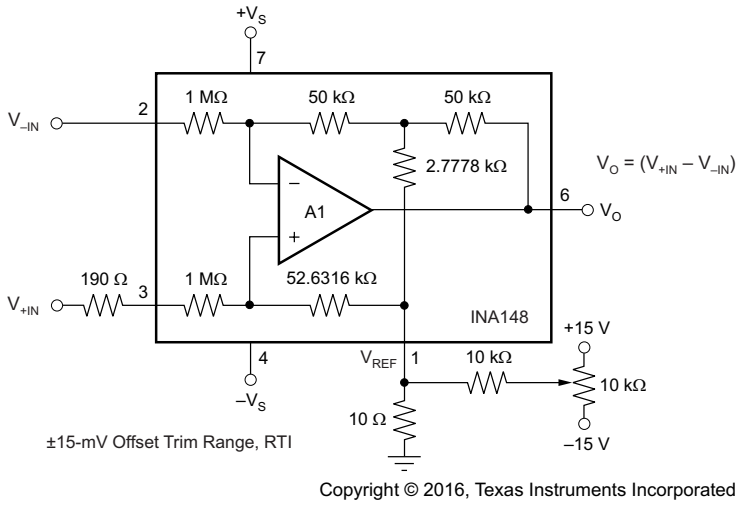


Figure 21. Optional Offset Trim Circuit

To maintain high common-mode rejection (CMR), the source impedance of any signal applied to the REF pin must be very low (≤5 Ω).

A source impedance of only 10 Ω at the REF pin reduces the INA148-Q1's CMR to approximately 74 dB. High CMR can be restored if a resistor is added in series with the amplifier's positive input pin. This resistor must be 19 times the source impedance that drives the REF pin. For example, if there is a source impedance of 10 Ω to the REF pin, a 190-Ω resistor must be added in series with the +IN pin.

Preferably, the offset trim voltage applied to the REF pin must be buffered with an amplifier such as an OPA171-Q1 (see Figure 22). In this case, the op amp output impedance is low enough that no external resistor is needed to maintain the INA148-Q1's excellent CMR.

Feature Description (continued)

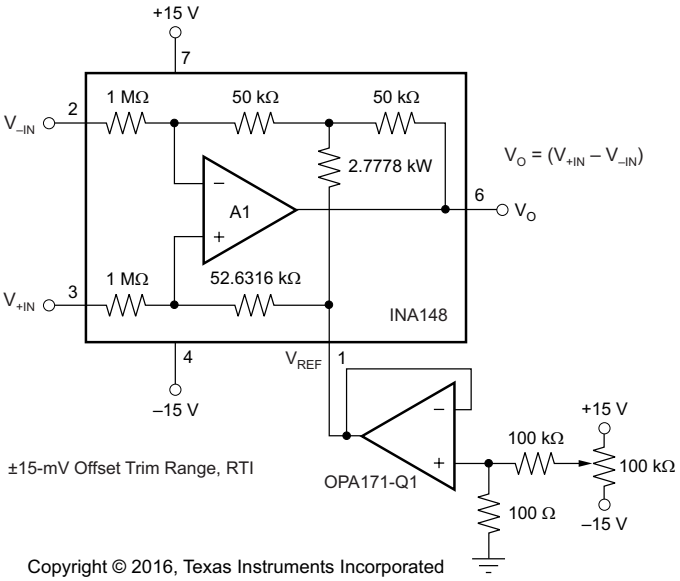


Figure 22. Preferred Offset Trim Circuit

7.3.5 Input Impedance

The input resistor network determines the impedance of each of the INA148-Q1 inputs. The impedance is approximately 1 MΩ. Unlike an instrumentation amplifier, signal source impedances at the two input pins must be nearly equal to maintain good common-mode rejection.

A mismatch between the two input source impedances causes a differential amplifier's common-mode rejection to be degraded. With a source impedance imbalance of only 500 Ω, CMR can fall to approximately 66 dB.

Figure 23 shows a common application, measuring power supply current through a shunt resistor (R_S). A shunt resistor creates an unbalanced source resistance condition that can degrade a differential amplifier's common-mode rejection.

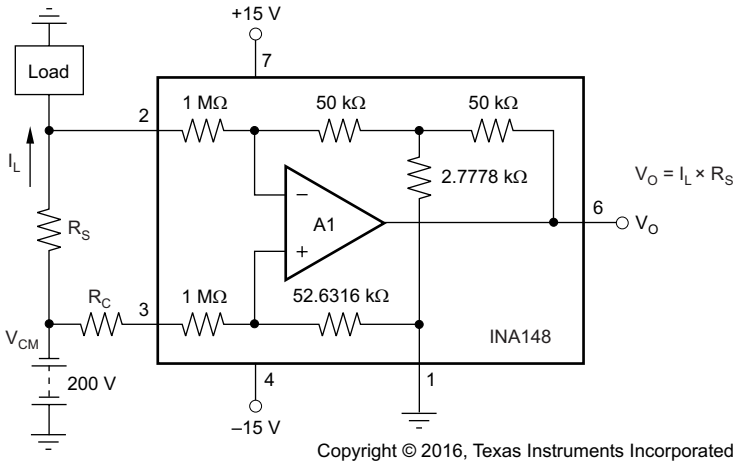


Figure 23. Shunt-Resistor Current Measurement Circuit

Unless the shunt resistor is less than approximately 100 Ω, TI recommends an additional equal compensating resistor (R_C) to maintain input balance and high CMR.

Feature Description (continued)

Source impedances (or shunts) greater than 5 kΩ are not recommended, even if they are *perfectly* compensated. This is because the internal resistor network is laser-trimmed for accurate voltage divider ratios, but not necessarily to absolute values. Input resistors are shown as 1 MΩ; however, this is only their nominal value.

In practice, the input resistors' absolute values may vary by as much as 30%. The two input resistors match to about 5%, so adding compensating resistors greater than 5 kΩ can cause a serious mismatch in the resulting resistor network voltage divider ratios, thus degrading CMR.

TI recommends not attempting to extend the INA148-Q1 input voltage range by adding external resistors for the reasons described in the previous paragraph. CMR suffers serious degradation unless the resistors are carefully trimmed for CMR and gain. This is an iterative adjustment and can be tedious and time consuming.

7.4 Device Functional Modes

The INA148-Q1 is a unity-gain, differential to single-ended amplifier that can reject high common-mode signals up to ±200 V with ±15-V supply voltage. This high common-mode rejection is achieved by internal trimmed resistive divider network. The resistive network provides an attenuation factor of 20:1.

Equation 2 shows the transfer function output to input.

$$V_O = V_{+IN} – V_{–IN} \quad (2)$$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

INA148-Q1 is a unity-gain difference amplifier with a high common-mode input voltage range. It is suitable to be used in many different applications that need bidirectional measurments in a high input common-mode environment.

8.2 Typical Applications

8.2.1 Battery Monitor Circuit

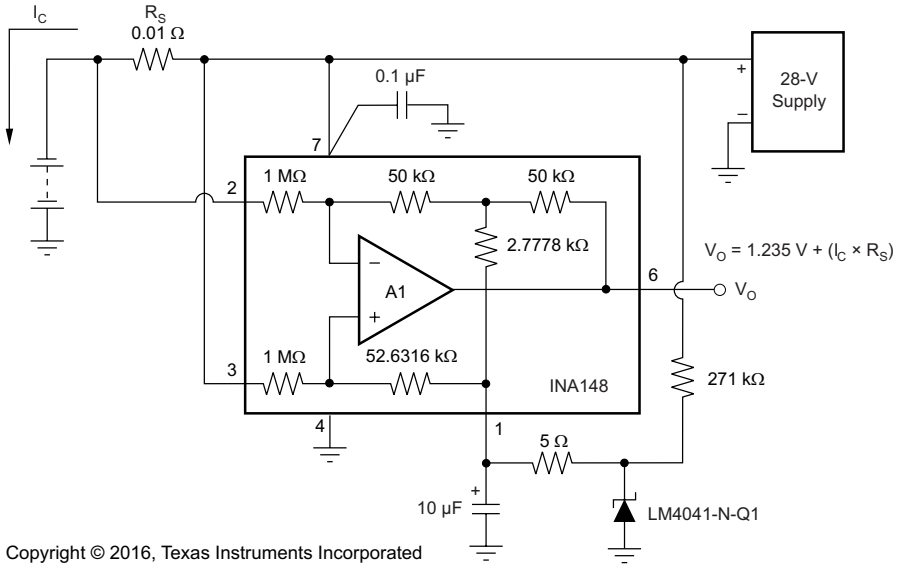


Figure 24. Battery Monitor Circuit Diagram

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Battery voltage	28 V
Sense resistor	0.01 Ω
Load current bidirectional	–50 A to 50 A
Reference voltage (LM4041-N-Q1)	1.235 V ± 0.1%

8.2.1.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current bidirectional in automotive battery monitor such as charging or body control modules with a 28-V battery or similar applications. The voltage difference amplifier REF pin is set at 1.235 V for bidirectional current measurement.

The LM4041-V-Q1 supply current is around 100 µA. It is provided from the 28-V battery through 271-kΩ resistor. The INA148-Q1 has a gain of 1 and output voltage as shown in Equation 3:

$$V_O = R_S \times I_C + 1.235\ V \quad (3)$$

The sense resistor value can be changed according to measured current range. TI recommends choosing the right value for minimizing the error and the dissipating power. The measured differential voltage is given as Equation 4 and the dissipated power is given as Equation 5.

$$R_S \times I_C \quad (4)$$

$$R_S \times I_C^2 \quad (5)$$

8.2.1.3 Application Curves

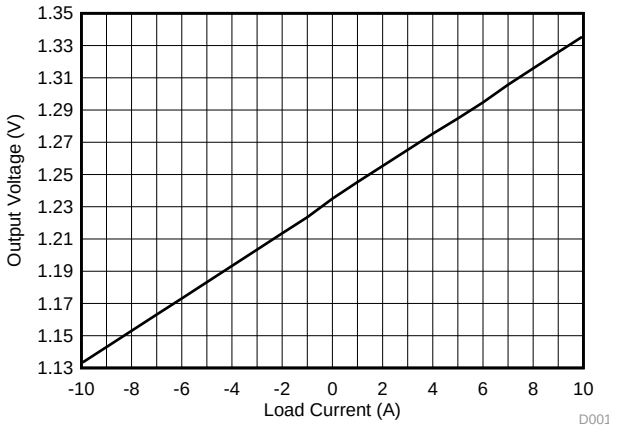


Figure 25. Output Voltage vs Load Current –10 A to 10 A

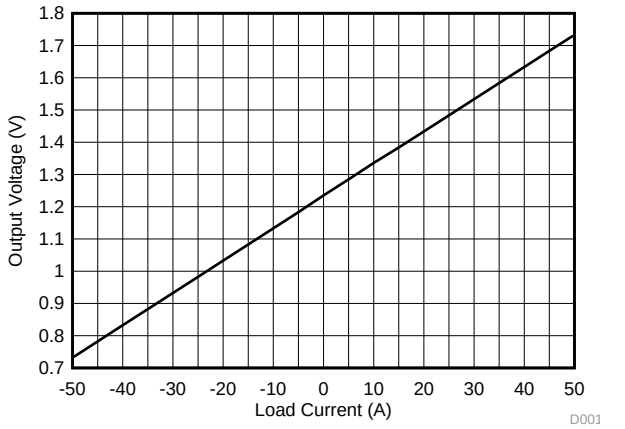


Figure 26. Output Voltage vs Load Current –50 A to 50 A

8.2.2 Quasi-AC-Coupled Differential Amplifier

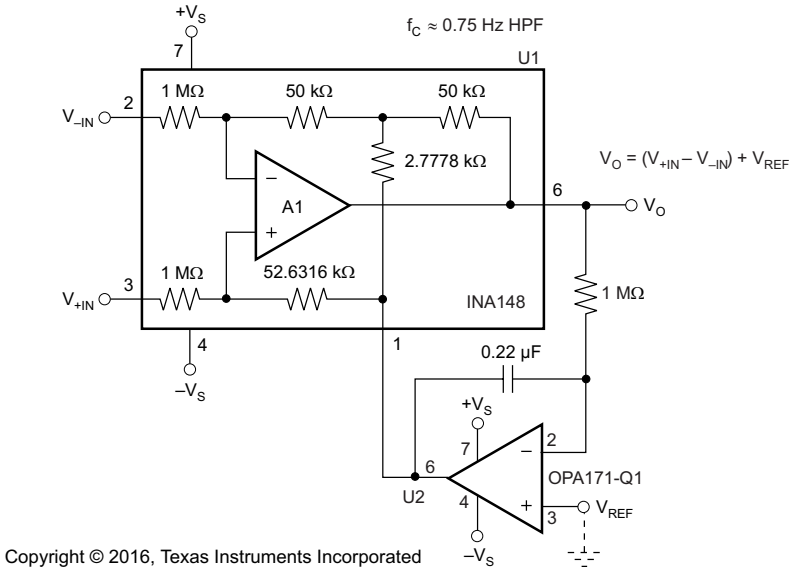


Figure 27. Quasi-AC-Coupled Differential Amplifier Diagram

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Common-mode supply voltage (–200 V to 200 V)	15 V
Common-mode supply voltage (–100 V to 750 V)	5 V
U2	OPA171-Q1
External resistor	1 MΩ
External capacitor	0.22 µF

8.2.2.2 Detailed Design Procedure

A quasi-AC coupled differential amplifier can be simply made by adding a general-purpose op amp configured as an integrator externally to the device. Equation 6 shows the output of OPA171-Q1.

$$V_O1 = \left(1 + \frac{Z_C}{R}\right) \times V_{REF} - \frac{Z_C}{R} \times V_O \quad (6)$$

where

- Z_C is the impedance of the external capacitor
- R is the value of the external resistor

Equation 7 shows the output of INA148-Q1.

$$V_O = V_O1 + V_{+IN} - V_{-IN} \quad (7)$$

Equation 8 is the result of combining the previous two equations.

$$V_O = \frac{R \times C \times S}{1 + R \times C \times S} \times (V_{+IN} - V_{-IN}) + V_{REF} \quad (8)$$

where

- $S = j \times 2\pi \times f$

The transfer function $\frac{R \times C \times S}{1 + R \times C \times S}$ has a zero and a pole at $\frac{1}{2\pi \times R \times C}$. Making a gain slope of 20 dB/decade below the cutoff frequncy and flat 0 dB above.

V_{REF} can be set to 0 V in case of dual supply.

8.2.3 Single-Supply Differential Amplifier

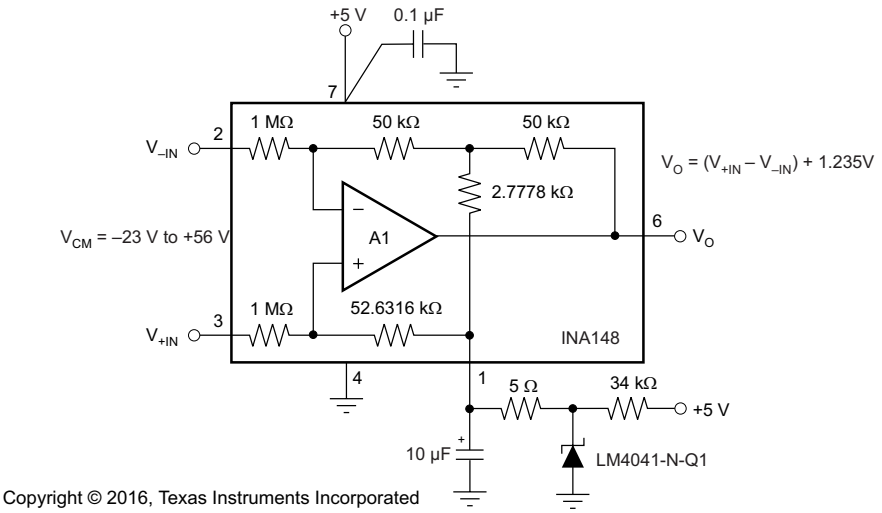


Figure 28. Single-Supply Differential Amplifier Diagram

8.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

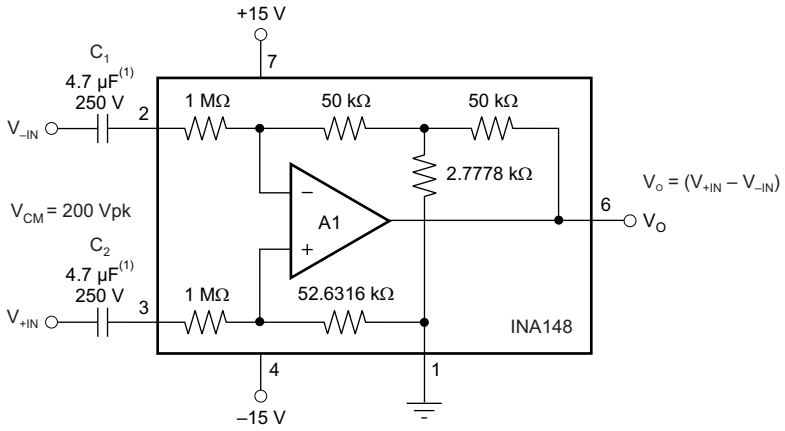
Table 3. Design Parameters

PARAMETER	EXAMPLE VALUE
Common-mode voltage	–23 V to 56 V
Load current	Bidirectional
Reference voltage (LM4041-N-Q1)	1.235 V ± 0.1%
Supply voltage (INA148-Q1)	5 V

8.2.3.2 Detailed Design Procedure

For applications that have –23-V to 56-V common-mode voltage and a single 5-V supply, the common-mode rejection ratio is in the order of 80 dB. The INA148-Q1 is not a rail-to-rail output. An external reference voltage is necessary for bidirectional measurment or low differential output. The external resistor is necessary to provide a 100-µA supply to LM4041-N-Q1.

8.2.4 AC-Coupled Difference Amplifier



(1) Metallized polypropylene, ±5% tolerance

Figure 29. AC-Coupled Difference Amplifier Circuit Diagram

8.2.4.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Decoupling capacitors	4.7 µF, 250 V ± 5%
Differential input voltage range	–14 V to 14 V

8.2.4.2 Detailed Design Procedure

An AC-coupled voltage difference amplifier requires 2 series capacitors. These capacitors must be high quality with tolerance of less than 5% and a rated voltage of 250 V at 200-V common-mode.

8.2.5 50-mV Current-Shunt Amplifier With ±200-V Common-Mode Voltage Range

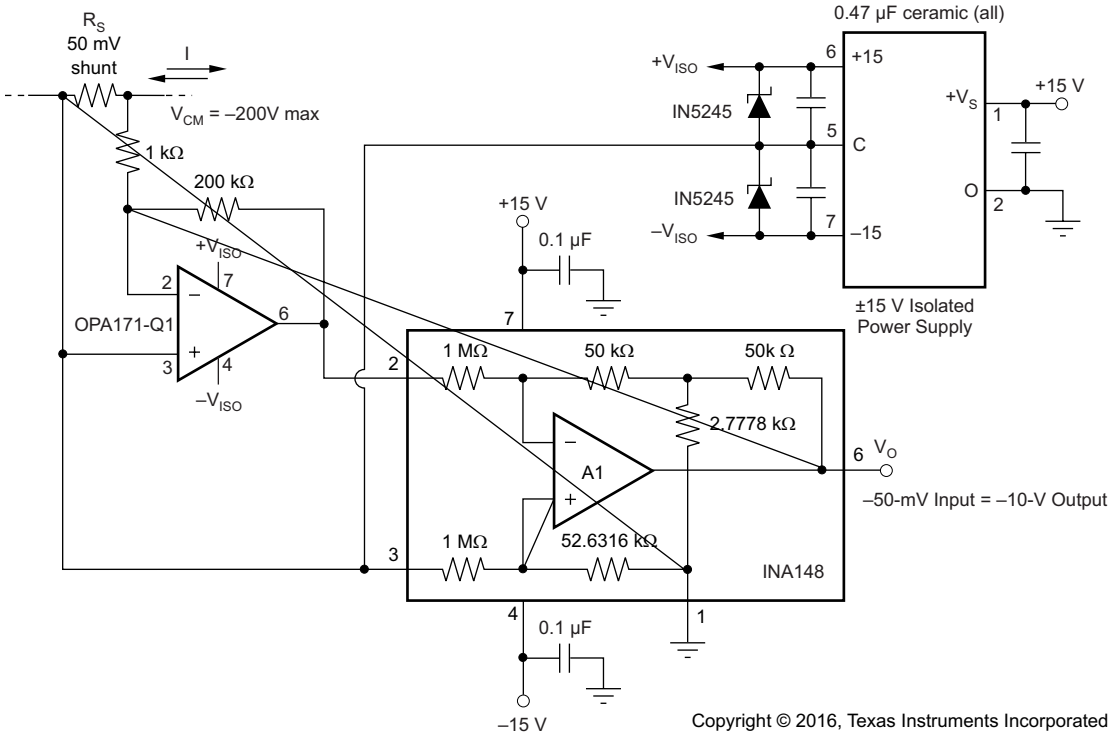


Figure 30. 50-mV Current-Shunt Amplifier With ±200-V Common-Mode Voltage Range Diagram

8.2.5.1 Design Requirements

For this design example, use the parameters listed in Table 5 as the input parameters.

Table 5. Design Parameters

PARAMETER	EXAMPLE VALUE
Common-mode voltage	±200 V
Differential input voltage	–50 mV to 50 mV
Gain (OPA171-Q1)	200
Isolated power supply	±15 V

8.2.5.2 Detailed Design Procedure

The OPA171-Q1 gain is 200, set by 1 kΩ and 200 kΩ resistors. The OPA171-Q1 positive input and the INA148-Q1 are both tied to the isolated power supply common ground. The OPA171-Q1 output is calculated by Equation 9.

$$V_O = –200 \times V_{SENSE}$$

where

- V_{SENSE} is the voltage across the shunt resistor (9)

The INA148-Q1 output is calculated by Equation 10.

$$V_O = –(–200 \times V_{SENSE}) = 200 \times V_{SENSE} \quad (10)$$

9 Power Supply Recommendations

Supply voltage is 2.7 V to 36 V for single supply and ±1.35 V to ±18 V for dual supplies. The input common-mode voltage range is higher at higher supply voltage, 75 V at V_S = 5 V and ±200 V at V_S = ±15 V.

10 Layout

10.1 Layout Guidelines

The INA148-Q1 is a precision voltage difference amplifier. To realize the full operational performance of the device, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1-µF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces must be designed for minimum inductance.

10.2 Layout Example

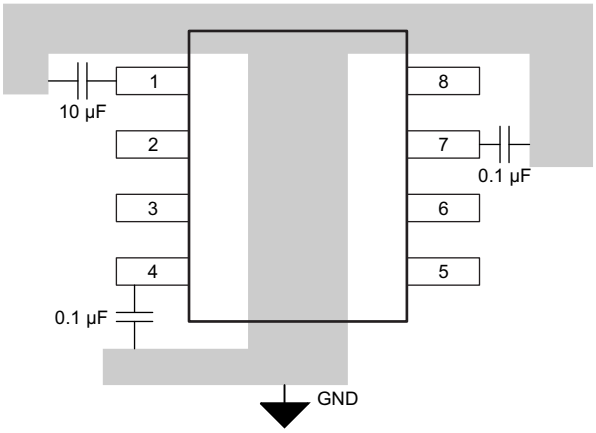


Figure 31. INA148-Q1 Layout Diagram

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

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11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA148QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 125	148Q1
INA148QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	148Q1
INA148QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	148Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF INA148-Q1 :

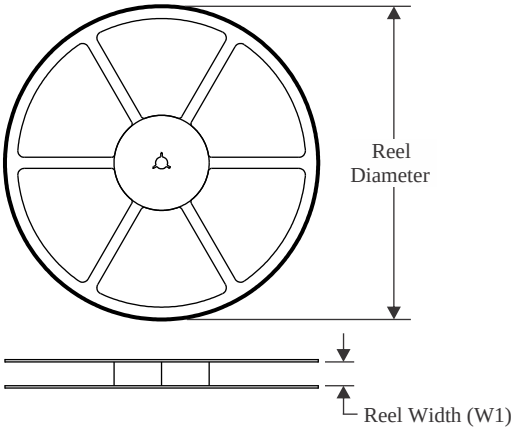
- Catalog : INA148

NOTE: Qualified Version Definitions:

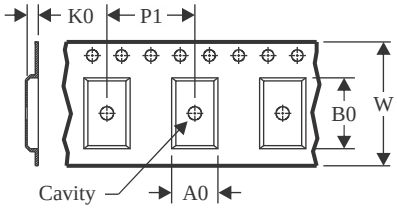
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

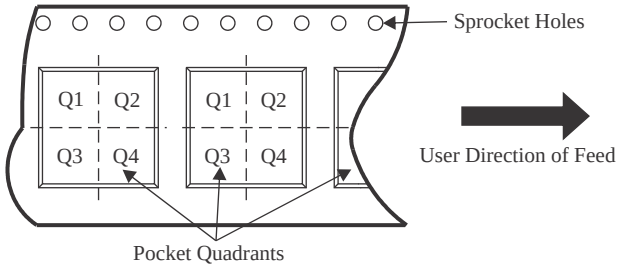


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

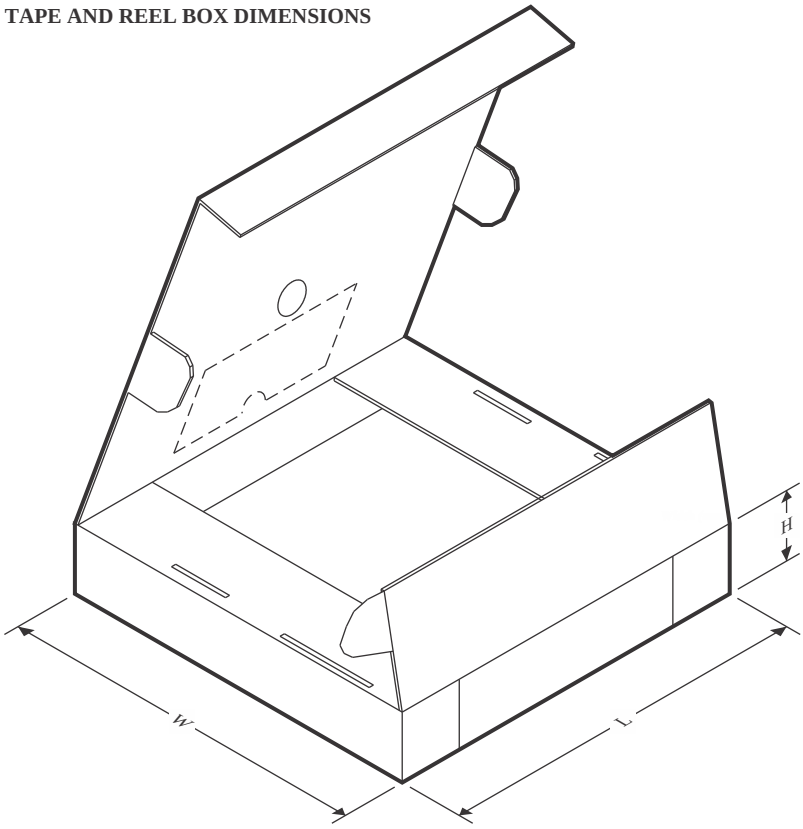
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA148QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA148QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

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