



## INA12x-HT Precision, Low-Power Instrumentation Amplifiers

### 1 Features

- Low Offset Voltage: 25  $\mu$ V Typical
- Low Input Bias Current: 50 nA Typical <sup>(1)</sup>
- High CMR: 95 dB Typical<sup>(1)</sup>
- Inputs Protected to  $\pm 40$  V
- Wide Supply Range:  $\pm 2.25$  V to  $\pm 18$  V
- Low Quiescent Current: 2 mA Typical<sup>(1)</sup>

### 2 Applications

- Bridge Amplifiers
- Thermocouple Amplifiers
- RTD Sensor Amplifiers
- Medical Instrumentation
- Data Acquisition
- Supports Extreme Temperature Applications:
  - Controlled Baseline
  - One Assembly/Test Site
  - One Fabrication Site
  - Available in Extreme Temperature Ranges ( $-55^{\circ}\text{C}$  to  $210^{\circ}\text{C}$ ) <sup>(2)</sup>
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

### 3 Description

The INA128-HT and INA129-HT are low-power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-operational-amplifier design and small size make them ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain. A single external resistor sets any gain from 1 to 10000. The INA128-HT provides an industry-standard gain equation; the INA129-HT gain equation is compatible with the AD620.

The INA128-HT and INA129-HT are laser trimmed for very low offset voltage (25  $\mu$ V Typ) and high common-mode rejection (93 dB at  $G \geq 100$ ). These devices operate with power supplies as low as  $\pm 2.25$  V, and quiescent current of 2 mA, typically. Internal input protection can withstand up to  $\pm 40$  V without damage.

Texas Instruments' high-temperature products use highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

The INA129-HT is available in 8-pin ceramic DIP and 8-pin ceramic surface-mount packages, specified for the  $-55^{\circ}\text{C}$  to  $210^{\circ}\text{C}$  temperature range. The INA128-HT is available in an 8-pin SOIC-8 surface-mount package, specified for the  $-55^{\circ}\text{C}$  to  $175^{\circ}\text{C}$  temperature range.

#### Device Information<sup>(1)</sup>

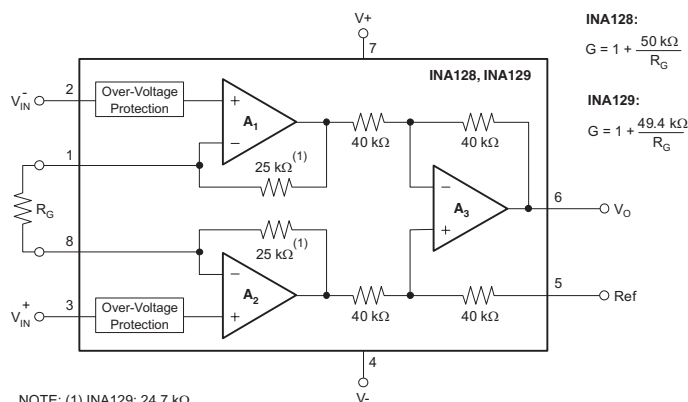
PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA128-HT	SOIC (8)	4.90 mm $\times$ 3.91 mm
INA129-HT	CFP (8)	6.90 mm $\times$ 5.65 mm
	CDIP SB (8)	11.81 mm $\times$ 7.49 mm

(1) Typical values for  $210^{\circ}\text{C}$  application.

(2) Custom temperature ranges available.

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



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## 5 Revision History

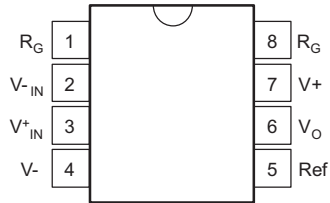
### Changes from Revision E (July 2013) to Revision F

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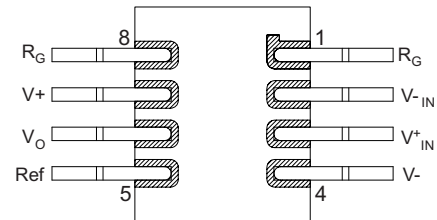
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**
- Deleted *Ordering Information* table; for all available packages, see the package option addendum ..... **3**

## 6 Pin Configuration and Functions

**D, HKJ, or JDJ Package  
8-Pin SOIC, CFP, or CDIP SB  
Top View**



**HKQ Package  
8-Pin CFP  
Top View**



HKQ as formed or HKJ mounted dead bug

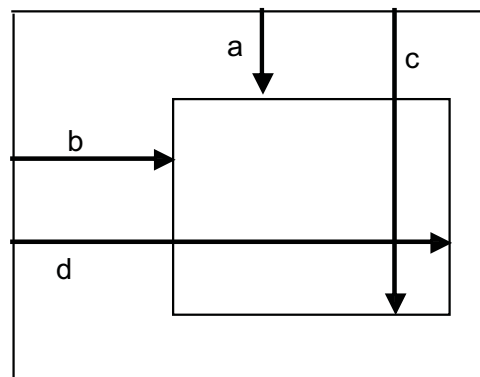
## Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Ref	5	I	Output voltage reference
RG	1, 8	O	Gain resistor connection
V+	7	Power	Positive power supply voltage from 2.25 V to 18 V
V–	4	Power	Negative power supply voltage from –2.25 V to –18 V
V+IN	3	I	Non-inverting input voltage
V–IN	2	I	Inverting input voltage
VO	6	O	Output voltage

## Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils	Silicon with backgrind	GND	Al-Si-Cu (0.5%)

## Origin



# INA128-HT, INA129-HT

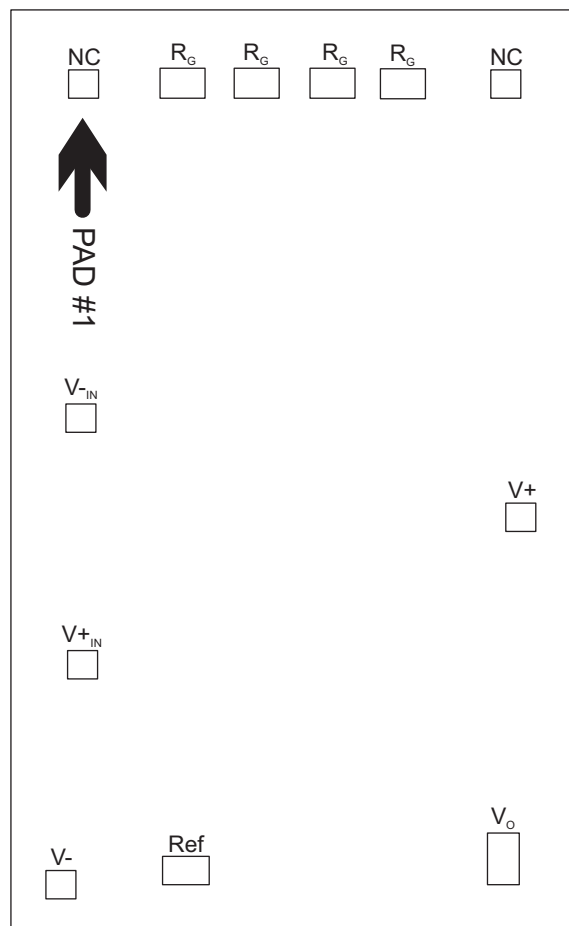
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## Bond Pad Coordinates in Mils

DESCRIPTION	PAD NUMBER	a	b	c	d
NC	1	–57.4	–31.1	–53.3	–27
V <sub>IN</sub> <sup>–</sup>	2	–9.85	–31.4	–5.75	–27.3
V <sub>IN</sub> <sup>+</sup>	3	25.05	–31.4	29.15	–27.3
V <sub>–</sub>	4	56.2	–34.3	60.3	–30.2
Ref	5	53.75	–17.6	57.85	–11
V <sub>O</sub>	6	50.35	27.8	56.95	31.9
V <sub>+</sub>	7	7.75	30.2	11.85	34.3
NC	8	–57.4	28.4	–53.3	32.5
R <sub>G</sub> <sup>(1)</sup>	9	–57.4	13.4	–53.3	20
R <sub>G</sub> <sup>(1)</sup>	10	–57.5	2.7	–53.4	9.3
R <sub>G</sub> <sup>(1)</sup>	11	–57.5	–7.9	–53.4	–1.3
R <sub>G</sub> <sup>(1)</sup>	12	–57.4	–18.6	–53.3	–12

- (1) Pads 9 and 10 must both be bonded to a common point and correspond to package pin 8. Pads 11 and 12 must both be bonded to a common point and correspond to package pin 1.



## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply		±18	V
	Analog input		±40	
Current	Output short-circuit (to ground)	Continuous		
Operating temperature	HKJ, HKQ, KGD and JD packages	–55	210	°C
	D package	–55	175	
Storage temperature, T <sub>stg</sub>	HKJ, HKQ, KGD and JD packages	–55	210	°C
	D package	–55	175	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
A. INA218-HT (D, HKJ, or JDJ Package)			
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±50	
B. INA129-HT (HKQ Package)			
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V power supply	±2.25	±15	±18	V
Input common-mode voltage range for V <sub>O</sub> = 0	V – 2 V		V + –2 V	
T <sub>A</sub> operating temperature INA128-HT	–55		175	°C
T <sub>A</sub> operating temperature INA129-HT	–55		210	°C

### 7.4 Thermal Information: INA128-HT

THERMAL METRIC <sup>(1)</sup>		INA128-HT	UNIT
		D [SOIC]	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	110	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	57	
R <sub>θJB</sub>	Junction-to-board thermal resistance	54	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	11	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	53	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

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**7.5 Electrical Characteristics: INA128-HT**

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = −55°C to +125°C			T <sub>A</sub> = 175°C <sup>(1)</sup>			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
OFFSET VOLTAGE, RTI								
Initial	T <sub>A</sub> = 25°C		±25 ±100/G	±125 ±1000/G				μV
vs temperature	T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		±0.2 ±5/G	±1 ±20/G			±3.5 ±80/G	μV/°C
vs power supply	V <sub>S</sub> = ±2.25 V to ±18 V			±2 ±200/G			±5 ±500/G	μV/V
Long-term stability			±1 ±3/G			±1 ±3/G		μV/mo
Impedance, differential			10 <sup>10</sup>    2			10 <sup>10</sup>    2		Ω    pF
Common mode			10 <sup>11</sup>   9			10 <sup>11</sup>   9		Ω    pF
Common mode voltage range <sup>(2)</sup>	V <sub>O</sub> = 0 V	(V+) − 2	(V+) − 1.4		(V+) − 2	(V+) − 1.4		V
		(V−) + 2	(V−) + 1.7		(V−) + 2	(V−) + 1.7		V
Safe input voltage				±40			±40	V
Common-mode rejection	V <sub>CM</sub> = ±13 V, ΔR <sub>S</sub> = 1 kΩ							dB
	G = 1	58	86		58	75		
	G = 10	78	106		78	85		
	G = 100	99	125		99	110		
	G = 1000	113	130		113	120		
CURRENT								
Bias current			±2	±10			±45	nA
vs temperature			±30			±550		pA/°C
Offset Current			±1	±10			±45	nA
vs temperature			±30			±550		pA/°C
NOISE								
Noise voltage, RTI	G = 1000, R <sub>S</sub> = 0 Ω							
f = 10 Hz			10			10		nV/√Hz
f = 100 Hz			8			8		nV/√Hz
f = 1 kHz			8			8		nV/√Hz
f <sub>B</sub> = 0.1 Hz to 10 Hz			0.2			0.8		μV <sub>PP</sub>
Noise current								
f = 10 Hz			0.9					pA/√Hz
f = 1 kHz			0.3					pA/√Hz
f <sub>B</sub> = 0.1 Hz to 10 Hz			30					pA <sub>PP</sub>

- (1) Minimum and maximum parameters are characterized for operation at  $T_A = 175^{\circ}\text{C}$ , but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
- (2) Input common-mode range varies with output voltage — see typical curves.

## Electrical Characteristics: INA128-HT (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = −55°C to +125°C			T <sub>A</sub> = 175°C <sup>(1)</sup>			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
GAIN									
Gain equation			1 + (50 kΩ/R <sub>G</sub> )			1 + (50 kΩ/R <sub>G</sub> )			V/V
Range of gain			1		10000	1		10000	V/V
Gain error	G = 1		±0.01		±0.1	±0.1%		±0.5%	
	G = 10		±0.02		±0.5	±0.5%		±1%	
	G = 100		±0.05		±0.7	±0.7%		±1.5%	
	G = 1000		±0.5		±2.5	±2%		±4%	
Gain vs temperature <sup>(3)</sup>		G = 1	±1		±10	±75			ppm/°C
50-kΩ resistance <sup>(3)(4)</sup>			±25		±100	±75			ppm/°C
Nonlinearity	V <sub>O</sub> = ±13.6 V, G = 1		±0.0001		±0.001			±0.008	% of FSR
	G = 10		±0.0003		±0.002			±0.01	
	G = 100		±0.0005		±0.002			±0.01	
	G = 1000		±0.001		See <sup>(5)</sup>		±0.6	See <sup>(5)</sup>	
OUTPUT									
Voltage	Positive	R <sub>L</sub> = 10 kΩ	(V+) − 1.4	(V+) − 0.9		(V+) − 1.4	(V+) − 0.9		V
	Negative	R <sub>L</sub> = 10 kΩ	(V−) + 1.4	(V−) + 0.8		(V−) + 1.4	(V−) + 0.8		
Load capacitance stability				1000			1000		pF
Short-circuit current				+6/−15			+6/−15		mA
FREQUENCY RESPONSE									
Bandwidth, −3 dB	G = 1			1300			1100		kHz
	G = 10			700			700		
	G = 100			200			190		
	G = 1000			20			17.5		
Slew rate		V <sub>O</sub> = ±10 V, G = 10		4			4		V/μs
Settling time, 0.01%	G = 1			7			7		μs
	G = 10			7			7		
	G = 100			9			9		
	G = 1000			80			80		
Overload recovery		50% overdrive		4			4		μs
POWER SUPPLY									
Voltage range			±2.25	±15	±18	±2.25	±15	±18	V
Current, total		V <sub>IN</sub> = 0 V		±0.7	±1			±1	mA
TEMPERATURE RANGE									
Specification			−55		+125			175	°C
Operating			−55		+125			175	°C

(3) Specified by wafer test.

(4) Temperature coefficient of the 50-k $\Omega$  term in the gain equation.

(5) Nonlinearity measurements in  $G = 1000$  are dominated by noise. Typical nonlinearity is  $\pm 0.001\%$ .

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**7.6 Electrical Characteristics: INA129-HT**

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = -55°C to +125°C			T <sub>A</sub> = 210°C <sup>(1)</sup>			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
OFFSET VOLTAGE, RTI								
Initial	T <sub>A</sub> = 25°C		±25 ±100/G	±125 ±1000/G				μV
vs temperature	T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		±0.2 ±5/G	±1 ±20/G		±1 ±850/G		μV/°C
vs power supply	V <sub>S</sub> = ±2.25 V to ±18 V		±0.2 ±20/G	±2 ±200/G		±20 ±1000/G		μV/V
Long-term stability			±1 ±3/G			±1 ±3/G		μV/mo
Impedance, differential			10 <sup>10</sup>    2			10 <sup>10</sup>    2		Ω    pF
Common mode			10 <sup>11</sup>   9			10 <sup>11</sup>   9		Ω    pF
Common mode voltage range <sup>(2)</sup>	V <sub>O</sub> = 0 V	(V+) - 2	(V+) - 1.4		(V+) - 2	(V+) - 1.4		V
		(V-) + 2	(V-) + 1.7		(V-) + 2	(V-) + 1.7		V
Safe input voltage				±40			±40	V
Common-mode rejection	V <sub>CM</sub> = ±13 V, ΔR <sub>S</sub> = 1 kΩ							dB
	G = 1	58	86			53		
	G = 10	78	106			69		
	G = 100	99	125			89		
	G = 1000	113	130			95		
CURRENT								
Bias current			±2	±10		±50		nA
vs temperature			±30			±600		pA/°C
Offset Current			±1	±10		±50		nA
vs temperature			±30			±600		pA/°C
NOISE								
Noise voltage, RTI	G = 1000, R <sub>S</sub> = 0 Ω							
f = 10 Hz			10			25		nV/√Hz
f = 100 Hz			8			20		nV/√Hz
f = 1 kHz			8			20		nV/√Hz
f <sub>B</sub> = 0.1 Hz to 10 Hz			0.2			2		μV <sub>PP</sub>
Noise current								
f = 10 Hz			0.9					pA/√Hz
f = 1 kHz			0.3					pA/√Hz
f <sub>B</sub> = 0.1 Hz to 10 Hz			30					pA <sub>PP</sub>

(1) Minimum and maximum parameters are characterized for operation at  $T_A = 210^{\circ}\text{C}$ , but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(2) Input common-mode range varies with output voltage — see typical curves.



## Electrical Characteristics: INA129-HT (continued)

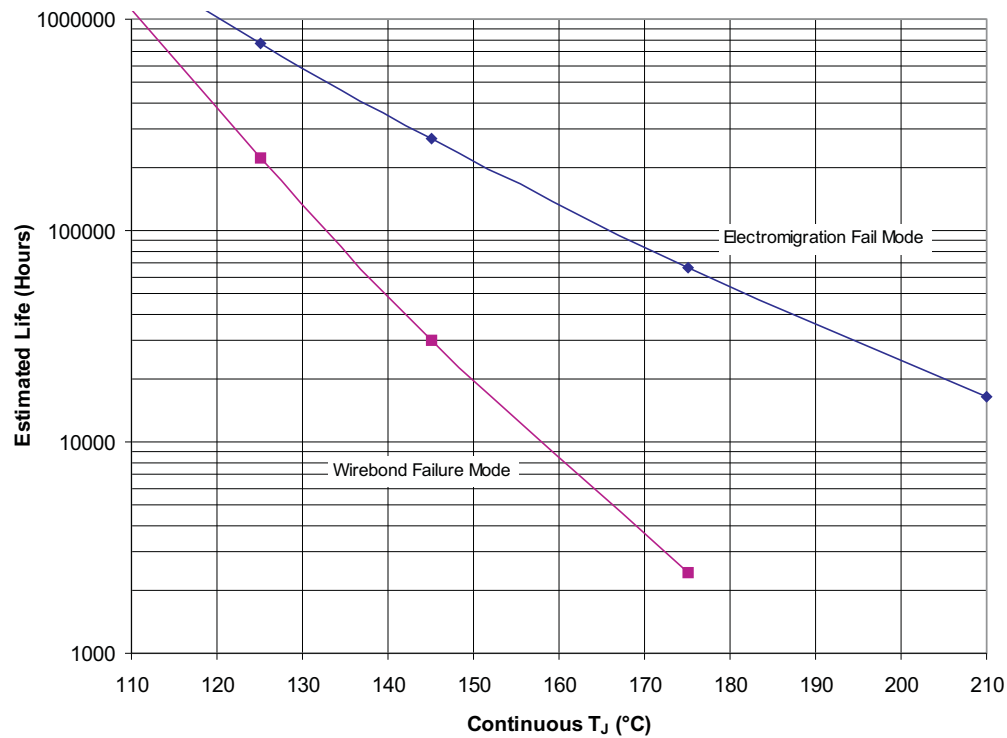
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = –55°C to +125°C			T <sub>A</sub> = 210°C <sup>(1)</sup>			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
GAIN									
Gain equation			1 + (49.4 kΩ/R <sub>G</sub> )			1 + (49.4 kΩ/R <sub>G</sub> )			V/V
Range of gain			1		10000	1		10000	V/V
Gain error	G = 1		±0.01%		±0.1%	±1.1%			
	G = 10		±0.02%		±0.5%	±2.6%			
	G = 100		±0.05%		±0.7%	±13.5%			
	G = 1000		±0.5%		±2.5%	±65.5%			
Gain vs temperature <sup>(3)</sup>	G = 1		±1		±10	±100			ppm/°C
49.4-kΩ resistance <sup>(3)(4)</sup>			±25		±100	±100			ppm/°C
Nonlinearity	V <sub>O</sub> = ±13.6 V, G = 1		±0.0001		±0.001	±0.1			% of FSR
	G = 10		±0.0003		±0.002	±0.2			
	G = 100		±0.0005		±0.002	±0.7			
	G = 1000		±0.001		See <sup>(5)</sup>	±2.4		See <sup>(5)</sup>	
OUTPUT									
Voltage	Positive	R <sub>L</sub> = 10kΩ	(V+) – 1.4	(V+) – 0.9		(V+) – 1.4	(V+) – 0.9		V
	Negative	R <sub>L</sub> = 10kΩ	(V–) + 1.4	(V–) + 0.8		(V–) + 1.4	(V–) + 0.8		
Load capacitance stability					1000			1000	pF
Short-circuit current					+6/–15			+12/–5	mA
FREQUENCY RESPONSE									
Bandwidth, –3 dB	G = 1				1300			850	kHz
	G = 10				700			400	
	G = 100				200			50	
	G = 1000				20			7.5	
Slew rate		V <sub>O</sub> = ±10 V, G = 10			4			4	V/μs
Settling time, 0.01%	G = 1				7			10	μs
	G = 10				7			10	
	G = 100				9			30	
	G = 1000				80			150	
Overload recovery		50% overdrive			4			4	μs
POWER SUPPLY									
Voltage range			±2.25	±15	±18	±2.25	±15	±18	V
Current, total		V <sub>IN</sub> = 0 V		±0.7	±1		±2		mA
TEMPERATURE RANGE									
Specification			–55		+125			210	°C
Operating			–55		+125			210	°C

(3) Specified by wafer test.

(4) Temperature coefficient of the 49.4-kΩ term in the gain equation.

(5) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.



- (1) See the data sheet for absolute maximum and minimum recommended operating conditions.
- (2) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.
- (3) Wirebond lifetime is only applicable for D package.

**Figure 1. INA128HD, INA129SKGD1, and INA129SKGD2 Operating Life Derating Chart**

## 7.7 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

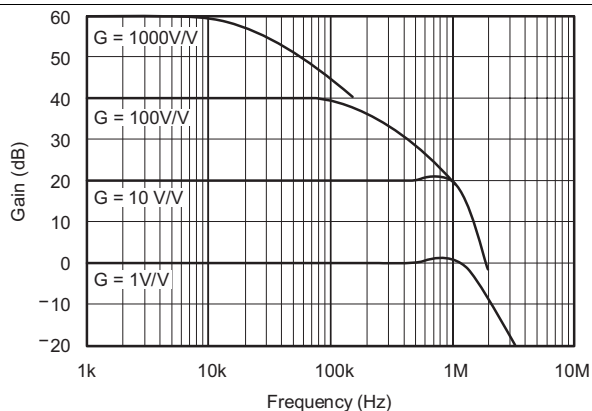


Figure 2. Gain vs Frequency

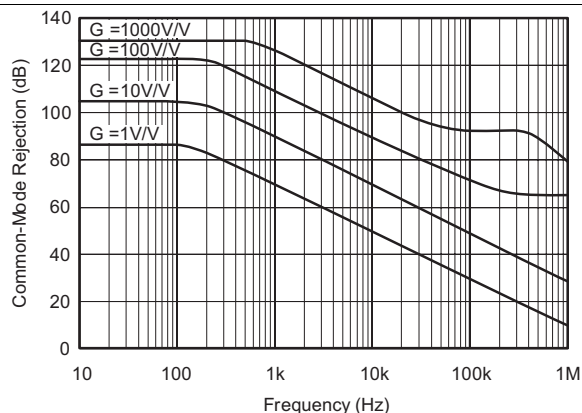


Figure 3. Common-Mode Rejection vs Frequency

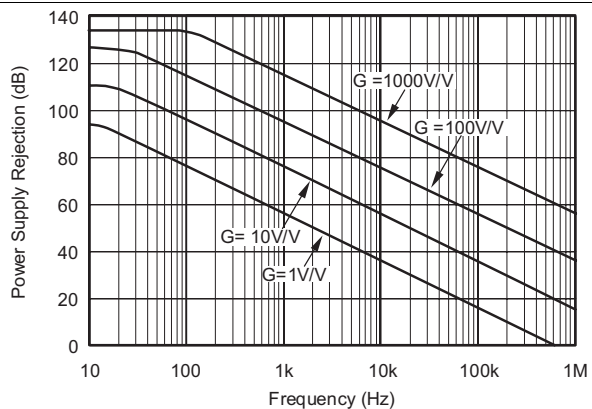


Figure 4. Positive Power-Supply Rejection vs Frequency

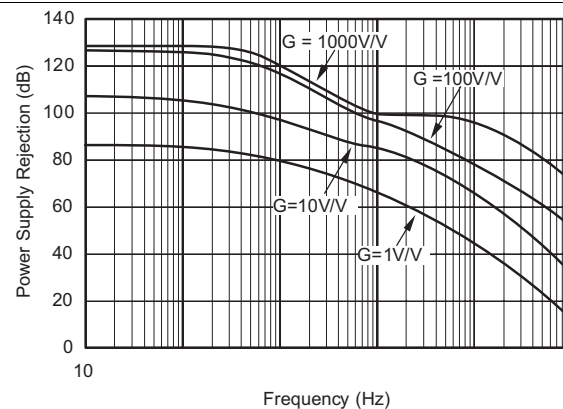


Figure 5. Negative Power-Supply Rejection vs Frequency

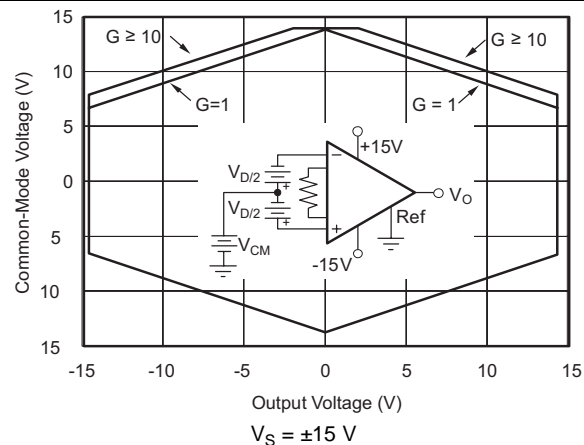


Figure 6. Input Common-Mode Range vs Output Voltage

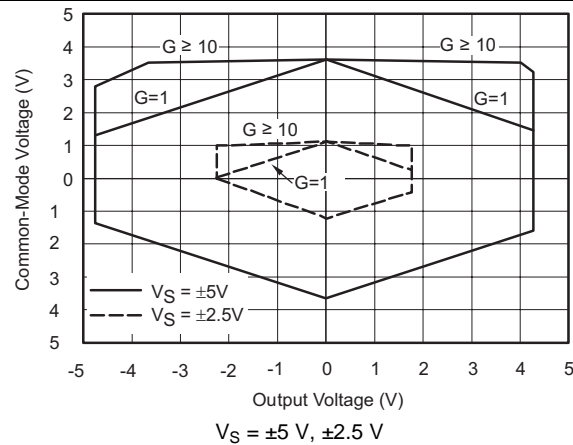
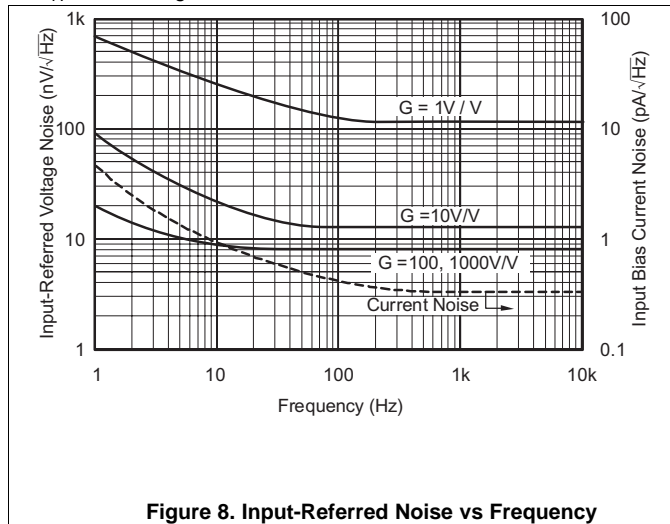


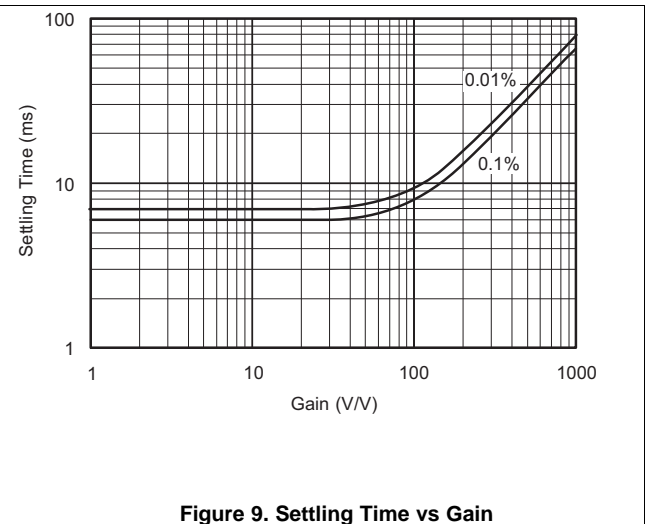
Figure 7. Input Common-Mode Range vs Output Voltage

## Typical Characteristics (continued)

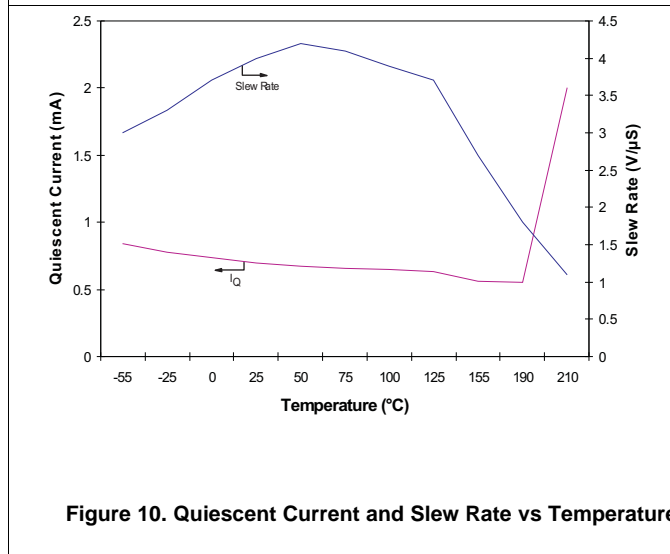
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.



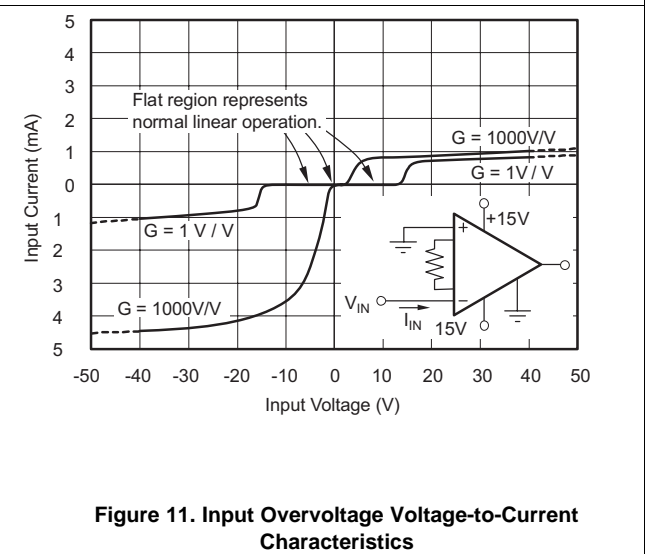
**Figure 8. Input-Referred Noise vs Frequency**



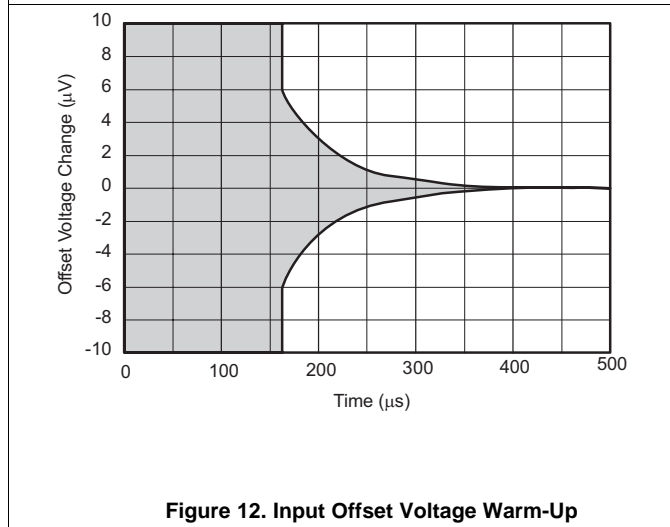
**Figure 9. Settling Time vs Gain**



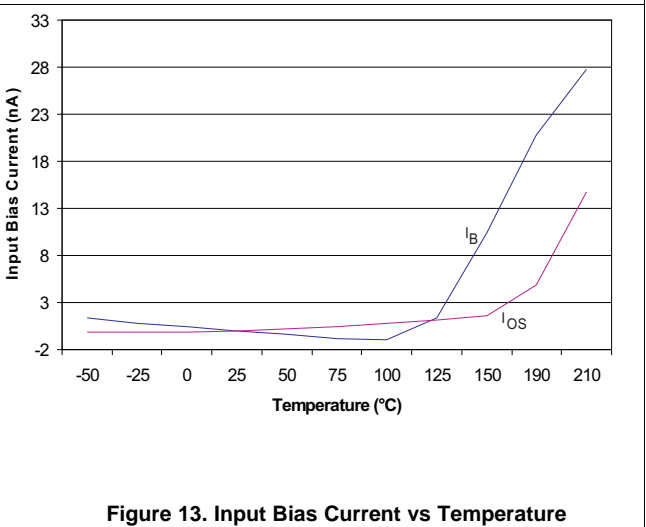
**Figure 10. Quiescent Current and Slew Rate vs Temperature**



**Figure 11. Input Overvoltage Voltage-to-Current Characteristics**



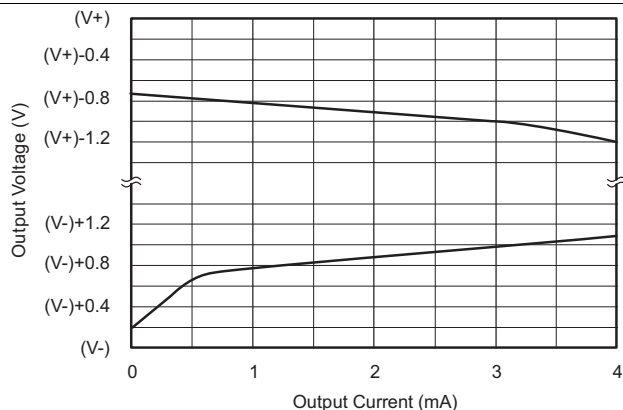
**Figure 12. Input Offset Voltage Warm-Up**



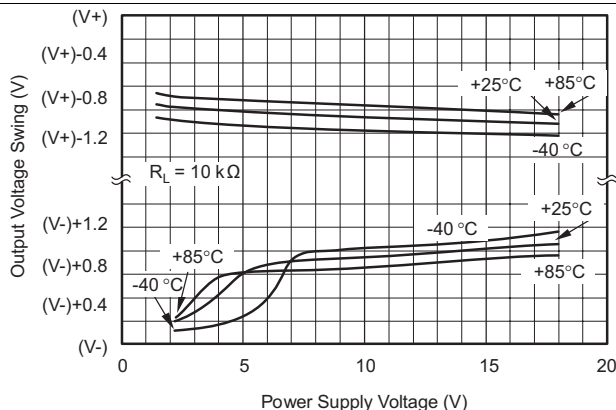
**Figure 13. Input Bias Current vs Temperature**

## Typical Characteristics (continued)

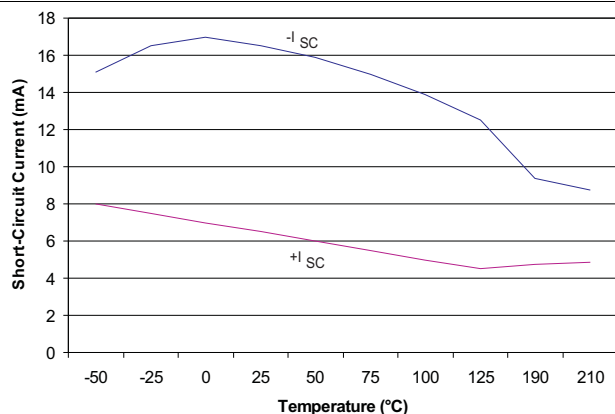
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.



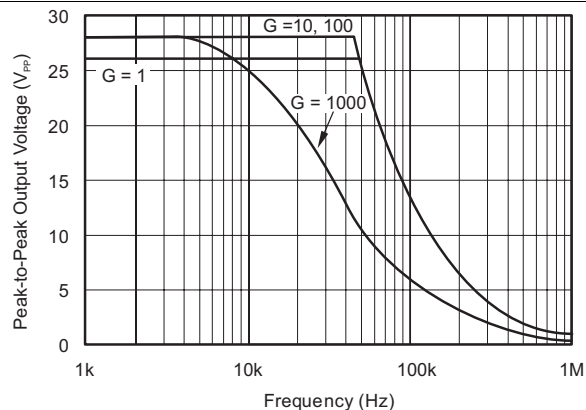
**Figure 14. Output Voltage Swing vs Output Current**



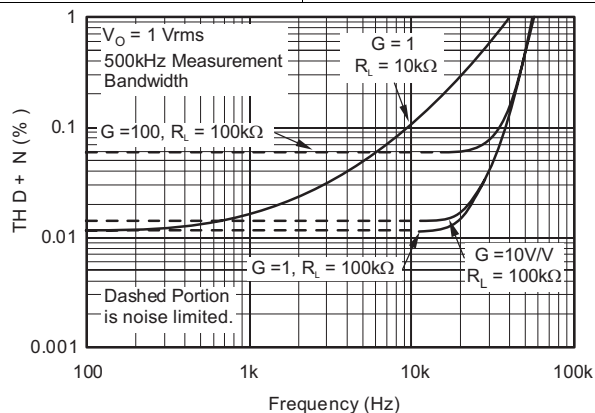
**Figure 15. Output Voltage Swing vs Power Supply Voltage**



**Figure 16. Short-Circuit Output Current vs Temperature**



**Figure 17. Maximum Output Voltage vs Frequency**



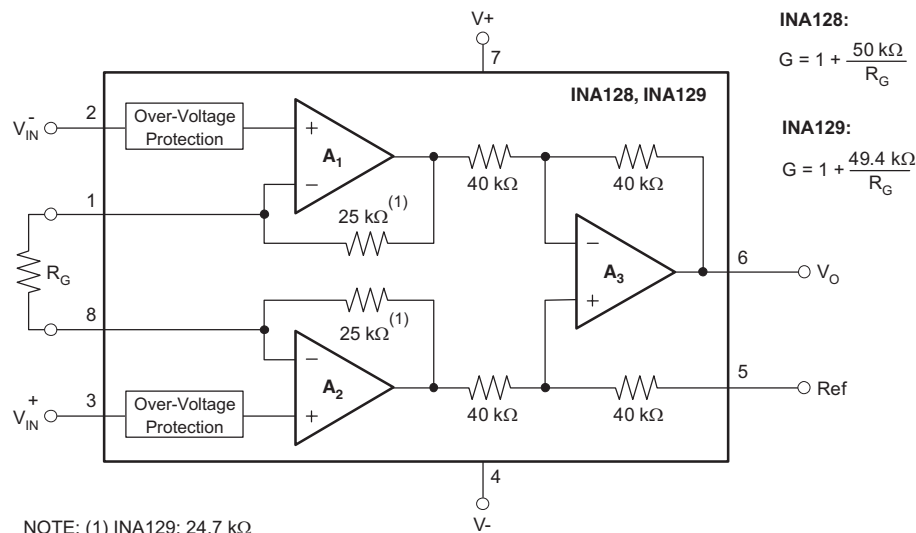
**Figure 18. Total Harmonic Distortion + Noise vs Frequency**

## 8 Detailed Description

### 8.1 Overview

The INA12x instrumentation amplifier is a type of differential amplifier that has been outfitted with input protection circuit and input buffer amplifiers, which eliminate the need for input impedance matching and make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics of the INA12x include a very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. The INA12x is used where great accuracy and stability of the circuit both short and long term are required.

### 8.2 Functional Block Diagram



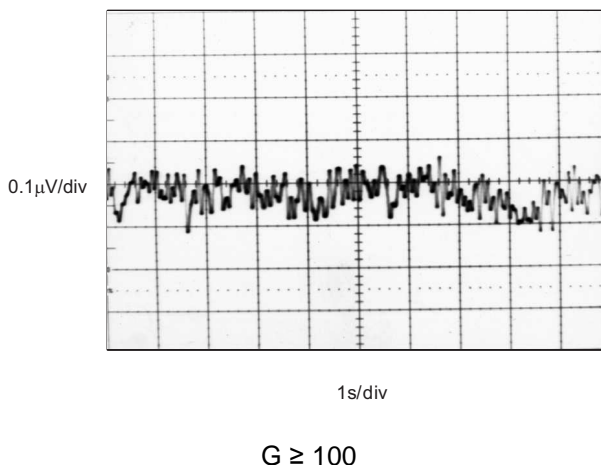
### 8.3 Feature Description

The INA128-HT and INA129-HT are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-operational-amplifier design and small size make the amplifiers ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA128-HT and INA129-HT are laser trimmed for very low offset voltage (25 μV typical) and high common-mode rejection (93 dB at  $G \geq 100$ ). These devices operate with power supplies as low as ±2.25 V, and quiescent current of 2 mA, typically. The internal input protection can withstand up to ±40 V without damage.

## 8.4 Device Functional Modes

### 8.4.1 Noise Performance

The INA128-HT and INA129-HT provide very low noise in most applications. Low-frequency noise is approximately 2  $\mu\text{VPP}$  measured from 0.1 Hz to 10 Hz ( $G \geq 100$ ). This provides dramatically improved noise when compared to state-of-the-art, chopper-stabilized amplifiers.



**Figure 19. 0.1-Hz to 10-Hz Input-Referred Voltage Noise**

### 8.4.2 Input Common-Mode Range

The linear input voltage ranges of the input circuitry of the INA128-HT and INA129-HT are from approximately 1.4 V below the positive supply voltage to 1.7 V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A1 and A2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see [Figure 6](#) and [Figure 7](#)).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A3 will be near 0 V even though both inputs are overloaded.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

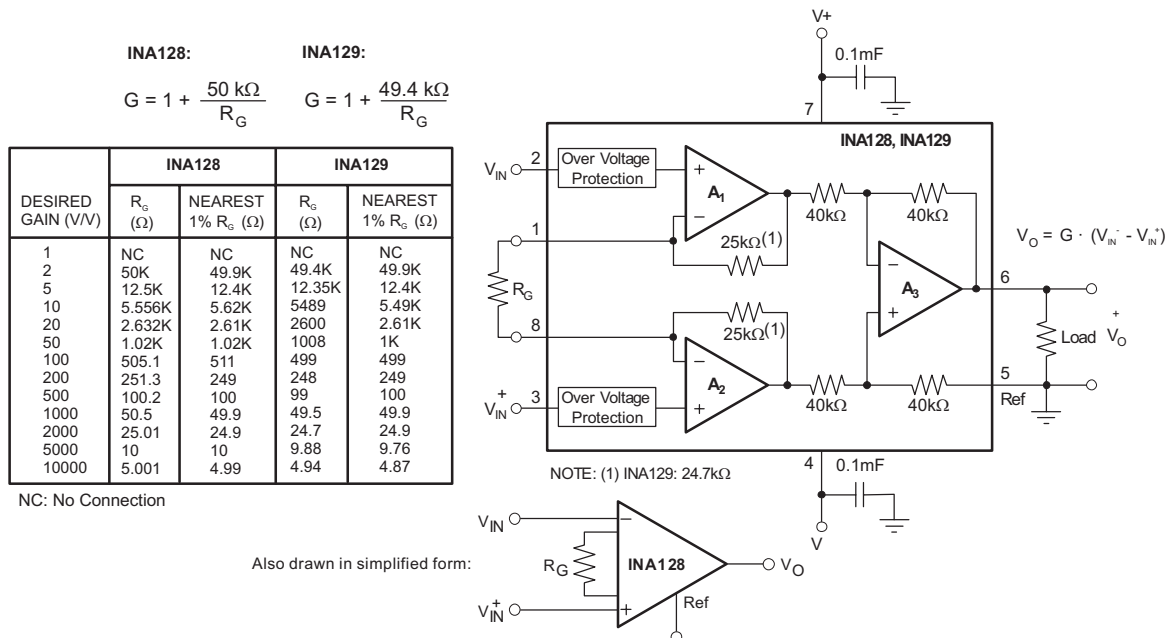
### 9.1 Application Information

The INA12x measures small differential voltage with high common-mode voltage developed between the non-inverting and inverting input. The high-input voltage protection circuit in conjunction with high input impedance make the INA12x suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

### 9.2 Typical Application

Figure 20 shows the basic connections required for operation of the INA128-HT and INA129-HT. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) pin that is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8  $\Omega$  in series with the Ref pin will cause a typical device to degrade.



**Figure 20. Basic Connections**

#### 9.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor  $R_G$ . The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground, as Figure 20 shows. When the input signal increases, the output voltage at the OUT pin increases, too.



## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Setting the Gain

Gain is set by connecting a single external resistor,  $R_G$ , between pins 1 and 8.

INA128-HT:

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

INA129-HT:

$$G = 1 + \frac{49.4 \text{ k}\Omega}{R_G} \quad (2)$$

Commonly used gains and resistor values are shown in [Figure 20](#).

The 50-k $\Omega$  term in [Equation 1](#) (49.4-k $\Omega$  in [Equation 2](#)) comes from the sum of the two internal feedback resistors of A1 and A2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA128-HT and INA129-HT.

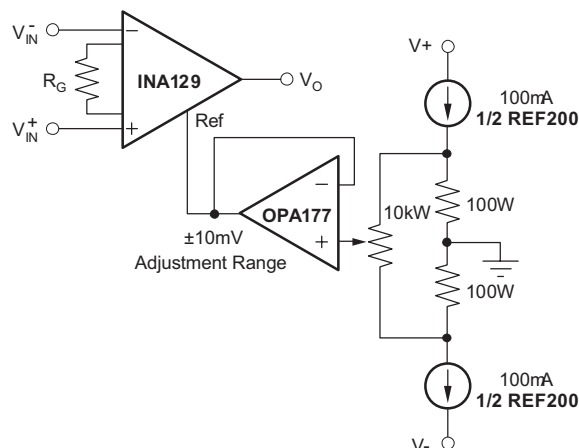
The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain. The  $R_G$  contribution to gain accuracy and drift can be directly inferred from [Equation 2](#). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

#### 9.2.2.2 Dynamic Performance

[Figure 2](#) shows that, despite its low quiescent current, the INA128-HT and INA129-HT achieve wide bandwidth, even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

#### 9.2.2.3 Offset Trimming

The INA128-HT and INA129-HT are laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. [Figure 21](#) shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The operational amplifier buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.



(1) [OPA177](#) and [REF200](#) are not tested or characterized at 210°C.

**Figure 21. Optional Trimming of Output Offset Voltage**

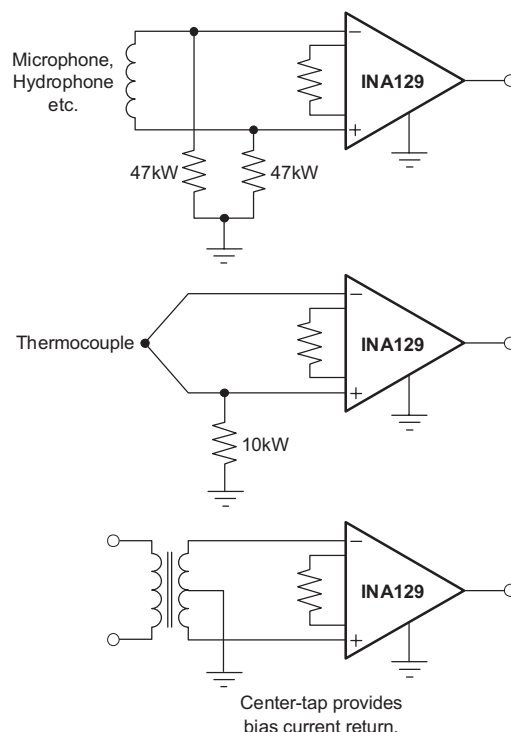
## Typical Application (continued)

### 9.2.2.4 Input Bias Current Return Path

The input impedances of the INA128-HT and INA129-HT are extremely high (approximately  $10^{10} \Omega$ ). However, a path must be provided for the input bias current of both inputs. This input bias current is approximately  $\pm 50 \text{ nA}$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 22 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

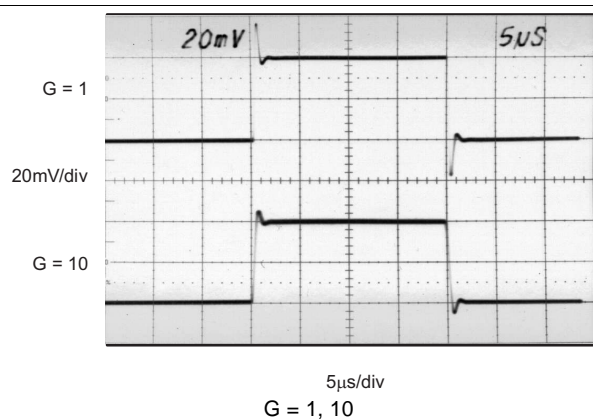
If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 22). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.



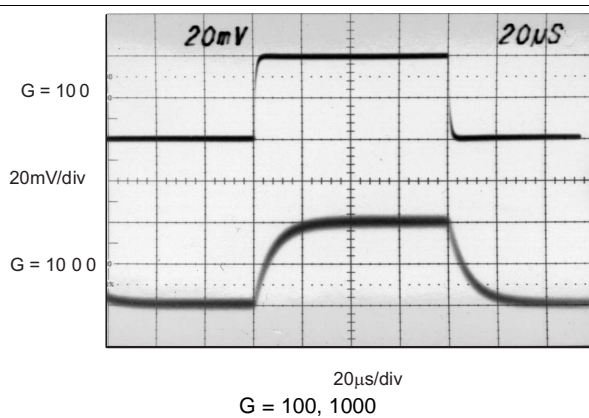
**Figure 22. Providing an Input Common-Mode Current Path**

## Typical Application (continued)

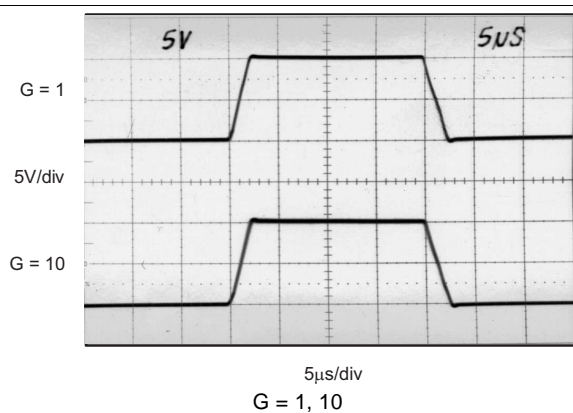
### 9.2.3 Application Curves



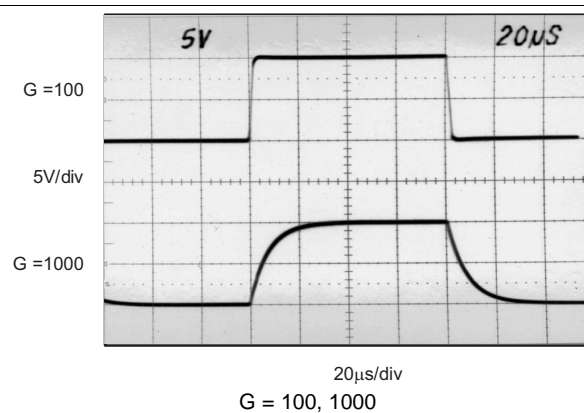
**Figure 23. Small Signal**



**Figure 24. Small Signal**



**Figure 25. Large Signal**



**Figure 26. Large Signal**

## 10 Power Supply Recommendations

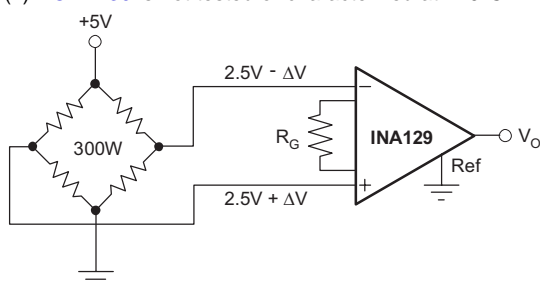
The minimum power supply voltage for INA12x is  $\pm 2.25$  V and the maximum power supply voltage is  $\pm 18$  V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance,  $\pm 15$  V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

### 10.1 Low Voltage Operation

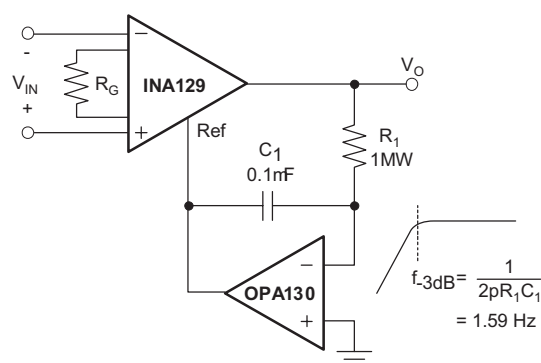
The INA128-HT and INA129-HT can be operated on power supplies as low as  $\pm 2.25$  V. Performance remains excellent with power supplies ranging from  $\pm 2.25$  V to  $\pm 18$  V. Most parameters vary only slightly throughout this supply voltage range.

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Figure 6 and Figure 7 show the range of linear operation for  $\pm 15$  V,  $\pm 5$  V, and  $\pm 2.5$  V supplies.

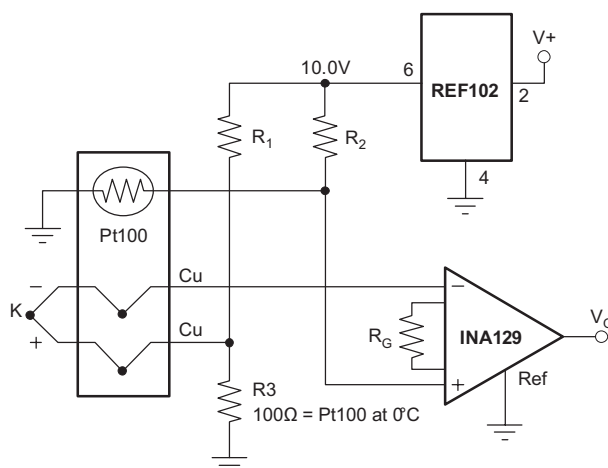
- (1) OPA130 is not tested or characterized at 210°C.



**Figure 27. Bridge Amplifier**



**Figure 28. AC-Coupled Instrumentation Amplifier**

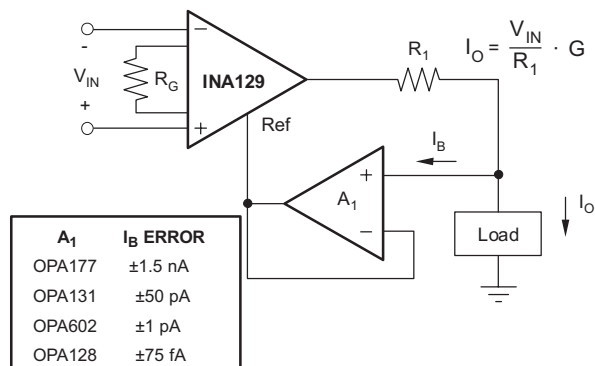


ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (mV/°C)	R <sub>1</sub> , R <sub>2</sub>
E	+Chromel -Constantan	58.5	66.5kW
J	+Iron -Constantan	50.2	76.8kW
K	+Chromel -Alumel	39.4	97.6kW
T	+Copper -Constantan	38	102kW

- (1) REF102 is not tested or characterized at 210°C.

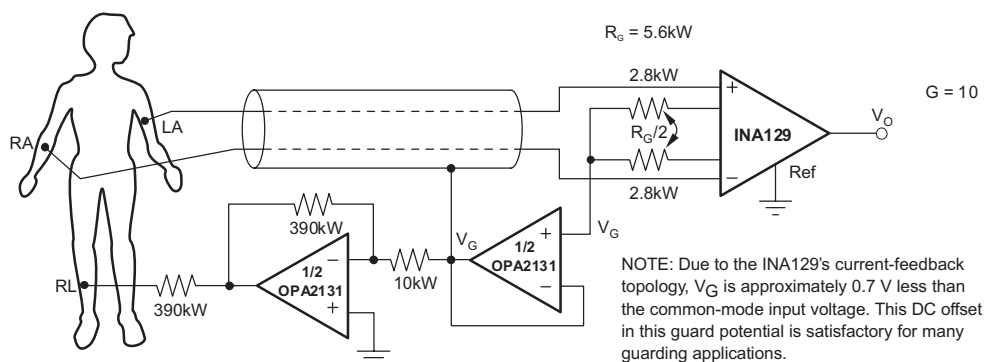
**Figure 29. Thermocouple Amplifier With RTD Cold-Junction Compensation**

## Low Voltage Operation (continued)



- (1) OPA177, OPA131, OPA602, and OPA128 are not tested or characterized at 210°C.

Figure 30. Differential Voltage-to-Current Converter



- (1) OPA2131 is not tested or characterized at 210°C.

Figure 31. ECG Amplifier With Right-Leg Drive

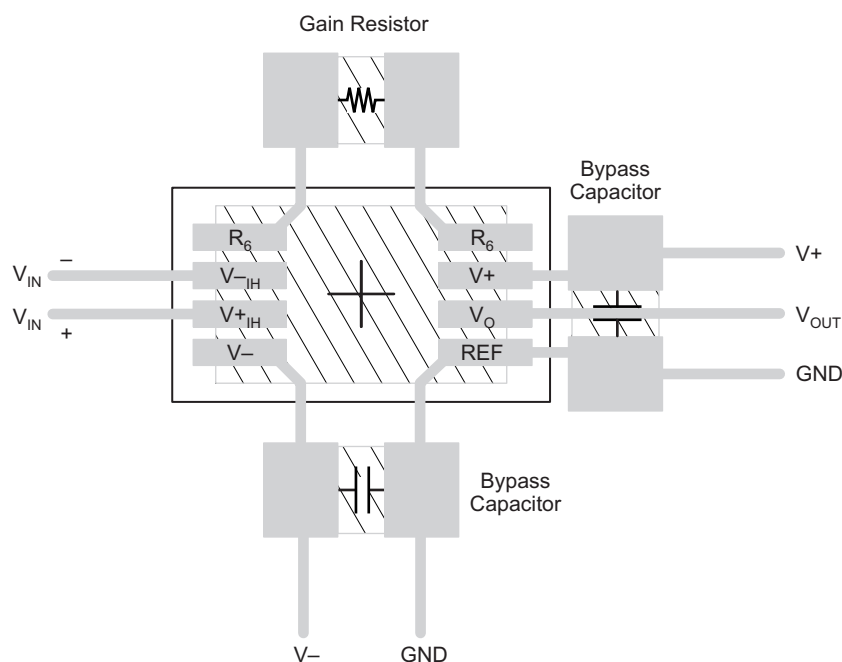
## 11 Layout

### 11.1 Layout Guidelines

Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$ . If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x device.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the part.

### 11.2 Layout Example



**Figure 32. Recommended Layout**

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

**Table 1. Design Kits and Evaluation Modules**

NAME	PART NUMBER	TYPE
<a href="#">DIP Adapter Evaluation Module</a>	DIP-ADAPTER-EVM	Evaluation Modules and Boards
<a href="#">Universal Instrumentation Amplifier Evaluation Module</a>	INAEVM	Evaluation Modules and Boards

**Table 2. Development Tools**

NAME	PART NUMBER	TYPE
<a href="#">Calculate Input Common-Mode Range of Instrumentation Amplifiers</a>	INA-CMV-CALC	Calculation Tools
<a href="#">SPICE-Based Analog Simulation Program</a>	TINA-TI	Circuit Design and Simulation

### 12.2 Related Links

[Table 3](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA128-HT	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
INA129-HT	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Trademarks

All trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">INA128HD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 175	128HD
INA128HD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 175	128HD
<a href="#">INA129SHKJ</a>	Active	Production	CFP (HKJ)   8	25   TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	INA129S HKJ
INA129SHKJ.A	Active	Production	CFP (HKJ)   8	25   TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	INA129S HKJ
<a href="#">INA129SHKQ</a>	Active	Production	CFP (HKQ)   8	25   TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	INA129S HKQ
INA129SHKQ.A	Active	Production	CFP (HKQ)   8	25   TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	INA129S HKQ
<a href="#">INA129SJD</a>	Active	Production	CDIP SB (JDJ)   8	37   TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	INA129SJD
INA129SJD.A	Active	Production	CDIP SB (JDJ)   8	37   TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	INA129SJD
INA129SKGD1	Active	Production	XCEPT (KGD)   0	80   NOT REQUIRED	Yes	Call TI	N/A for Pkg Type	-55 to 210	
INA129SKGD1.A	Active	Production	XCEPT (KGD)   0	80   NOT REQUIRED	Yes	Call TI	N/A for Pkg Type	-55 to 210	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF INA128-HT, INA129-HT :**

- Catalog : [INA128](#), [INA129](#)
- Enhanced Product : [INA129-EP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TUBE

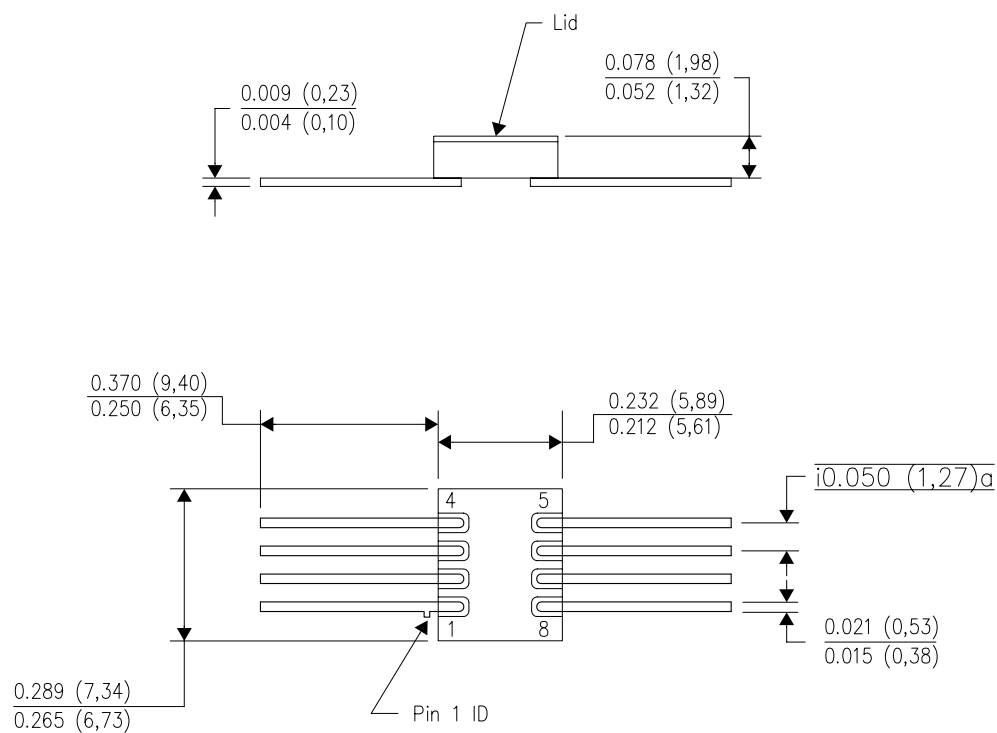


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA128HD	D	SOIC	8	75	506.6	8	3940	4.32
INA128HD.A	D	SOIC	8	75	506.6	8	3940	4.32
INA129SHKJ	HKJ	CFP	8	25	506.98	26.16	6220	NA
INA129SHKJ.A	HKJ	CFP	8	25	506.98	26.16	6220	NA
INA129SHKQ	HKQ	CFP	8	25	506.98	26.16	6220	NA
INA129SHKQ.A	HKQ	CFP	8	25	506.98	26.16	6220	NA
INA129SJD	JDJ	CDIP SB	8	37	506.98	15.24	12290	NA
INA129SJD.A	JDJ	CDIP SB	8	37	506.98	15.24	12290	NA

HKJ (R-CDFP-F8)

CERAMIC DUAL FLATPACK



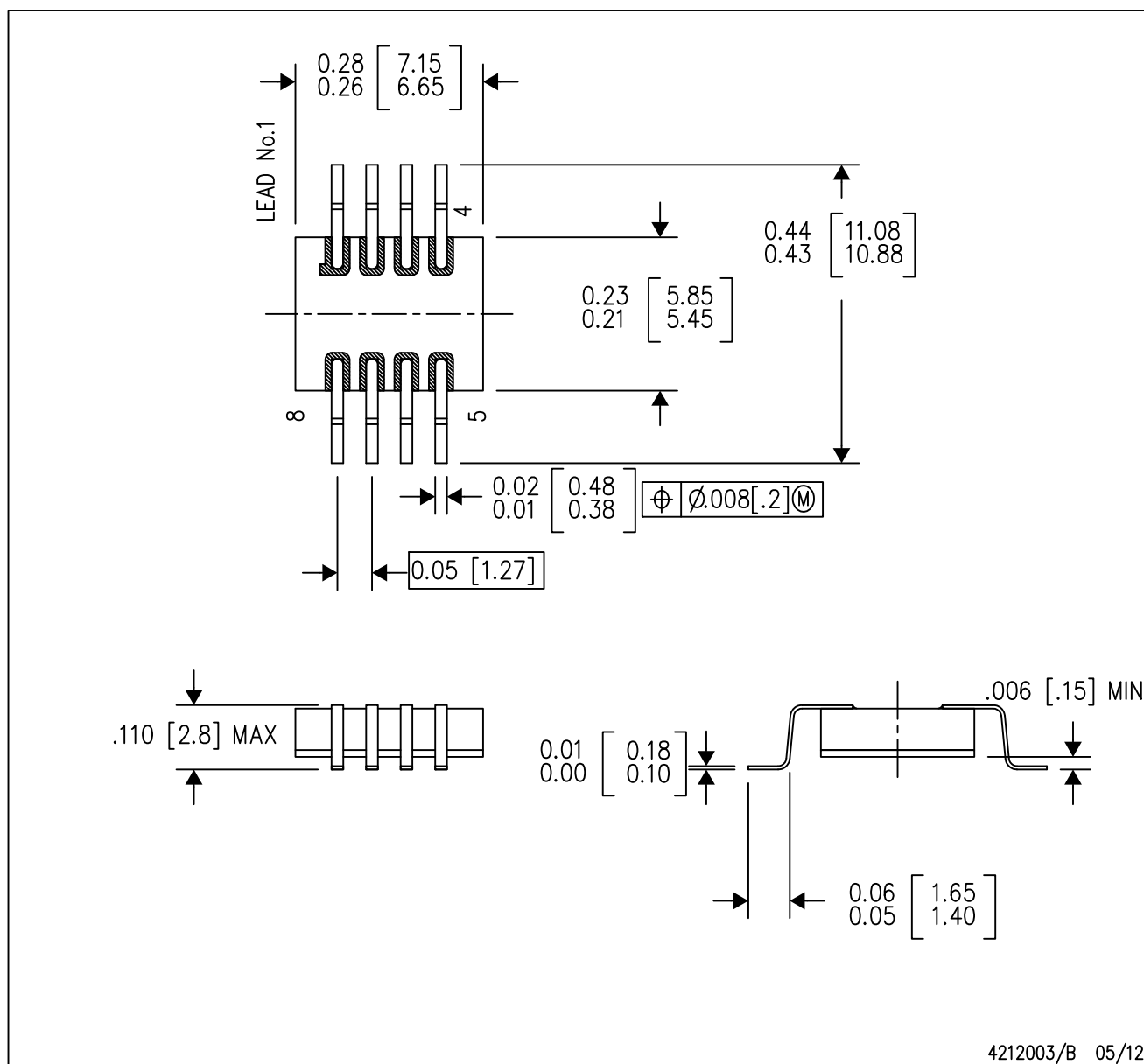
4209892/A 10/08

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals will be gold plated.

# MECHANICAL DATA

HKQ (R-CDFP-G8)

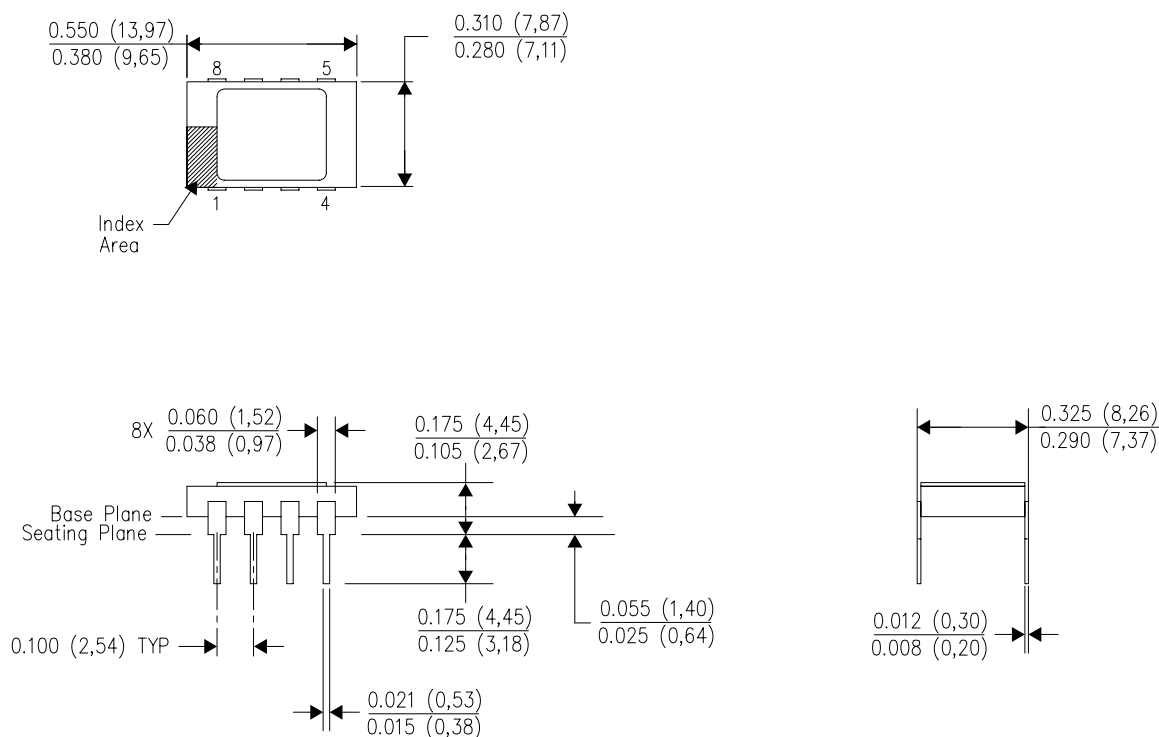
CERAMIC GULL WING



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals will be gold plated.
  - E. Lid is not connected to any lead.

JDJ (R-CDIP-T8)

CERAMIC DUAL IN-LINE PACKAGE



4202646-2/B 07/10

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
  - This package is hermetically sealed with a metal lid.
  - The leads are gold plated and can be solderdipped.
  - Leads not shown for clarity purposes.
  - Lid and heat sink are connected to GND leads.

**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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