INAx126 MicroPower Instrumentation Amplifiers

1 Features

- Low quiescent current: 175µA/channel
- Wide supply range: ±1.35V to ±18V
- Low offset voltage: 250µV maximum
- Low offset drift: 3µV/°C maximum
- Low noise: 35 nV/√Hz
- Low input bias current: 25nA maximum
- Temperature range: –40°C to +85°C
- Multiple package options:
  - Single channel:
    - INA126P/PA 8-pin PDIP (P)
    - INA126U/UA 8-pin SOIC (D)
    - INA126E/EA 8-pin VSSOP (DGK)
  - Dual channels:
    - INA2126P/PA 16-pin PDIP (N)
    - INA2126U/UA 16-pin SOIC (D)
    - INA2126E/EA 16-pin SSOP (DBQ)

2 Applications

- Level transmitter
- Flow transmitter
- Multiparameter patient monitor
- Mixed module (AI, AO, DI, DO)
- AC charging (pile) station
- Infusion pump
- Electrocardiogram (ECG)

3 Description

The INA126 and INA2126 (INAx126) are precision instrumentation amplifiers for accurate, low-noise, differential-signal acquisition. The two-op-amp design provides excellent performance with low quiescent current (175µA/channel). These features combined with a wide operating voltage range of ±1.35V to ±18V make the INAx126 a great choice for portable instrumentation and data acquisition systems.

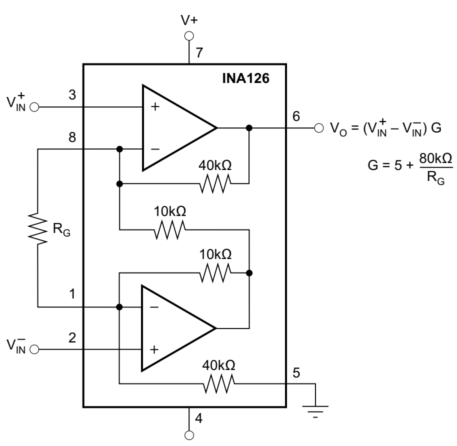
Gain can be set from 5V/V to 10000V/V with a single external resistor. Precision input circuitry provides low offset voltage (250µV, maximum), low offset voltage drift (3µV/°C, maximum), and excellent common-mode rejection.

All versions are specified for the –40°C to +85°C industrial temperature range.

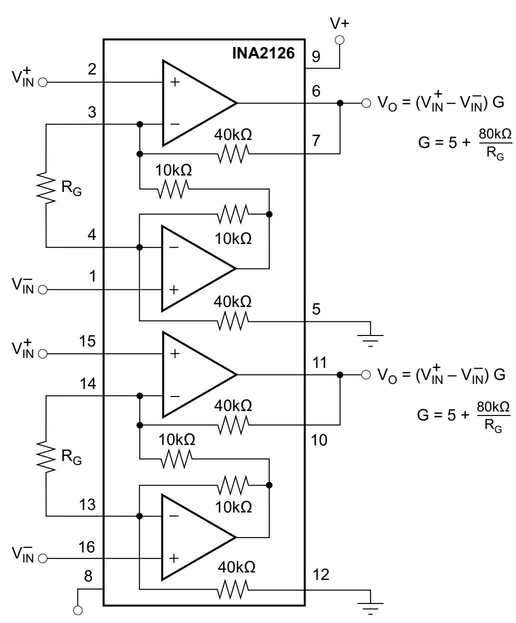
Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
INA126	Single	P (PDIP, 8)
		D (SOIC, 8)
		DGK (VSSOP, 8)
INA2126	Dual	N (PDIP, 16)
		D (SOIC, 16)
		DBQ (SSOP, 16)

(1) For more information, see Section 10.



Simplified Schematic: INA126



Simplified Schematic: INA2126

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4 Pin Configuration and Functions

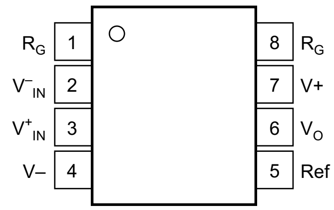


Figure 4-1. INA126: P (8-Pin PDIP), D (8-Pin SOIC), and DGK (8-Pin VSSOP) Packages, Top View

Table 4-1. Pin Functions: INA126

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1, 8	R_G	—	Gain setting pin. For gains greater than 5 place a gain resistor between pin 1 and pin 8.
2	$V-_{IN}$	I	Negative input
3	$V+_{IN}$	I	Positive input
4	V–	—	Negative supply
5	Ref	I	Reference input. This pin must be driven by a low impedance or connected to ground.
6	V_O	O	Output
7	V+	—	Positive supply

(1) I = input, O = output

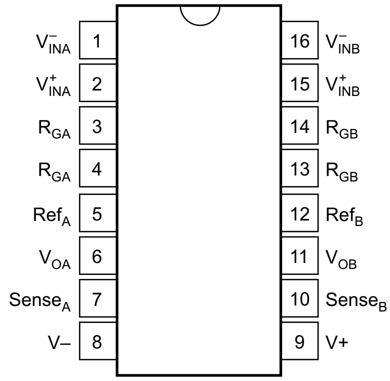


Figure 4-2. INA2126: N (16-Pin PDIP), D (16-Pin SOIC), and DBQ (16-Pin SSOP) Packages, Top View

Table 4-2. Pin Functions: INA2126

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	$V-_{INA}$	I	Negative input for amplifier A
2	$V+_{INA}$	I	Positive input for amplifier A
3, 4	R_{GA}	—	Gain setting pin for amplifier A. For gains greater than 5 place a gain resistor between pin 3 and pin 4.
5	Ref_{A}	I	Reference input for amplifier A. This pin must be driven by a low impedance or connected to ground.
6	V_{OA}	O	Output of amplifier A
7	$Sense_{A}$	I	Feedback for amplifier A. Connect to VOA, amplifier A output.
8	V–	—	Negative supply
9	V+	—	Positive supply
10	$Sense_{B}$	I	Feedback for amplifier B. Connect to VOB, amplifier B output.
11	V_{OB}	O	Output of amplifier B
12	Ref_{B}	I	Reference input for amplifier B. This pin must be driven by a low impedance or connected to ground.
13, 14	R_{GB}	—	Gain setting pin for amplifier B. For gains greater than 5 place a gain resistor between pin 13 and pin 14.
15	$V+_{INB}$	I	Positive input for amplifier B
16	$V-_{INB}$	I	Negative input for amplifier B

(1) I = input, O = output

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 8.1.2.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S	Supply voltage dual supply, V_S = (V+) – (V–)		±18	V
	Supply voltage single supply, V_S = (V+) – (V–)		36	
	Input signal voltage[2]	(V–) – 0.7	(V+) + 0.7	V
	Input signal current[2]		10	mA
	Output short-circuit[3]	Continuous		
T_A	Operating Temperature	–55	125	°C
	Lead temperature (soldering, 10s)		300	°C
T_{stg}	Storage Temperature	–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input signal voltage is limited by internal diodes connected to power supplies. See *Input Protection*.
(3) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	2.7	30	36	V
		Dual-supply	±1.35	±15	±18	
T_A	Specified temperature		–40		85	°C

5.4 Thermal Information: INA126

THERMAL METRIC[(1)]		INA126			UNIT
		PDIP	SOIC	VSSOP	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.2	116.4	167.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.6	62.4	60.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	57.7	88.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.9	10.0	7.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.2	57.1	87.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Thermal Information: INA2126

THERMAL METRIC[(1)]		INA2126			UNIT
		PDIP	SOIC	SSOP	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.3	76.2	115.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	37.8	67.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	33.5	58.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	7.5	19.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.9	33.3	57.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 25kΩ, V_{REF} = 0V, and V_{CM} = V_S / 2, all chips site origins (CSO), unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage (RTI)	INA126P/U/E INA2126P/U/E			±100	±250	μV
		INA126PA/UA/EA INA2126PA/UA/EA			±150	±500	
	Offset voltage drift (RTI)	T_A = –40°C to +85°C	INA126P/U/E INA2126P/U/E		±0.5	±3	μV/°C
			INA126PA/UA/EA INA2126PA/UA/EA		±0.5	±5	
PSRR	Power-supply rejection ratio (RTI)	V_S = ±1.35V to ±18V	INA126P/U/E INA2126P/U/E		±5	±15	uV/V
			INA126PA/UA/EA INA2126PA/UA/EA		±5	±50	
	Input impedance	CSO: SHE			1 || 4		GΩ || pF
		CSO: TID			17.5 || 1		
	Safe input voltage	R_S = 0Ω		(V–) – 0.5		(V+) + 0.5	V
		R_S = 1kΩ		(V–) – 10		(V+) + 10	
V_{CM}	Common-mode voltage[(1)]			–11.25	±11.5	11.25	V
	Channel seperation (dual)	G = 5, dc			130		dB
CMRR	Common-mode rejection ratio	R_S = 0Ω, V_{CM} = ±11.25V	INA126P INA2126P	83	94		dB
			INA126U/E INA2126U/E	80	94		
			INA126PA/UA/EA INA2126PA/UA/EA	74	83		
INPUT BIAS CURRENT							
I_B	Input bias current	INA126P/U/E INA2126P/U/E			±10	±25	nA
		INA126PA/UA/EA INA2126PA/UA/EA			±10	±50	
	Input bias current drift	T_A = –40°C to +85°C			±30		pA/°C
I_{OS}	Input offset current	INA126P/U/E INA2126P/U/E			±0.5	±2	nA
		INA126PA/UA/EA INA2126PA/UA/EA			±0.5	±5	nA
	Input offset current drift	T_A = –40°C to +85°C			±10		pA/°C
GAIN							
	Gain equation				5 + (80 kΩ / R_G)		V/V
G	Gain			5		10000	V/V
GE	Gain error	G = 5 , V_O = ±14V	INA126P/U/E INA2126P/U/E		±0.02	±0.1	%
			INA126PA/UA/EA INA2126PA/UA/EA		±0.02	±0.18	
		G = 100, V_O = ±12V	INA126P/U/E INA2126P/U/E		±0.2	±0.5	
			INA126PA/UA/EA INA2126PA/UA/EA		±0.2	±1	
	Gain drift[(2)]	T_A = –40°C to +85°C	G = 5		±2	±10	ppm/°C
			G = 100		±25	±100	
	Gain nonlinearity	G = 100, V_O = ±14V			±0.002	±0.012	%

5.6 Electrical Characteristics (continued)

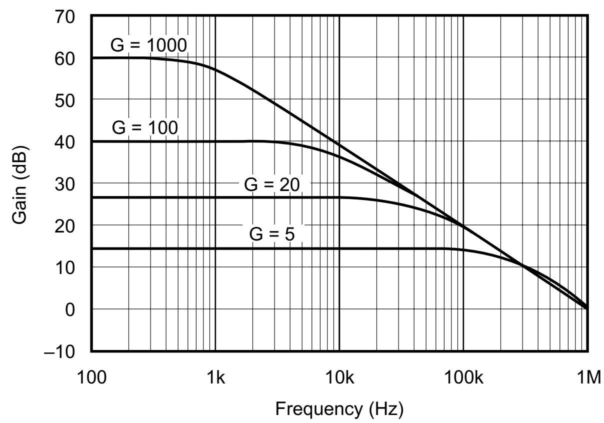
at T_A = 25°C, V_S = ±15V, R_L = 25kΩ, V_{REF} = 0V, and V_{CM} = V_S / 2, all chips site origins (CSO), unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE							
e_N	Voltage noise	f = 1kHz	CSO: SHE		35		$nV/\sqrt{Hz}$
			CSO: TID		24		
		f = 100Hz	CSO: SHE		35		
			CSO: TID		24		
		f_B = 10Hz	CSO: SHE		45		
			CSO: TID		24		
		f_B = 0.1Hz to 10Hz	CSO: SHE		0.7		μV_{PP}
			CSO: TID		0.5		
I_n	Current noise	f = 1 kHz			160		$fA/\sqrt{Hz}$
		f_B = 0.1Hz to 10Hz			7.3		pA_{PP}
OUTPUT							
	Positive output voltage swing			(V+) – 0.9	(V+) – 0.75		V
	Negative output voltage swing			(V–) + 0.95	(V–) + 0.8		V
I_{SC}	Short-circuit current	Continuous to V_S / 2			±5		mA
C_L	Load capacitance	Stable operation			1000		pF
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	G = 5	CSO: SHE		200		kHz
			CSO: TID		250		
		G = 100	CSO: SHE		9		
			CSO: TID		10		
		G = 500	CSO: SHE		1.8		
			CSO: TID		2		
SR	Slew rate	G = 5, V_O = ±10V			0.4		V/µs
t_S	Settling time	To 0.01%, V_{STEP} = 10V	G = 5		30		µs
			G = 100		160		
			G = 500		1500		
	Overload recovery	50% input overload			4		µs
POWER SUPPLY							
I_Q	Quiescent current (per channel)	I_O = 0mA			±175	±200	µA

(1) Input voltage range of the instrumentation amplifier input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves.
(2) The values specified for G > 5 do not include the effects of the external gain-setting resistor, R_G.

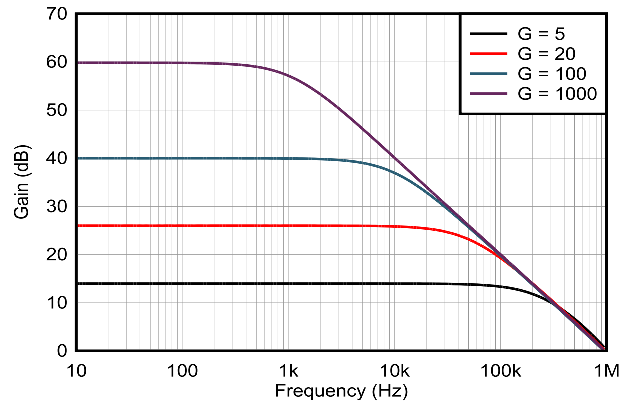
5.7 Typical Characteristics

at T_A = 25°C, V_S = ±15V, all chips site origins (CSO), unless otherwise noted



CSO: SHE

Figure 5-1. Gain vs Frequency



CSO: TID

Figure 5-2. Gain vs Frequency

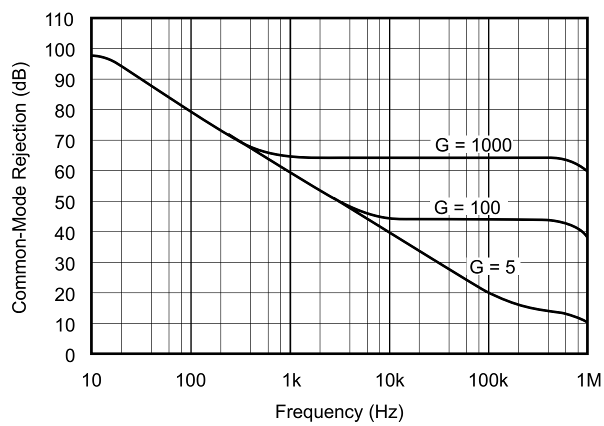


Figure 5-3. Common-Mode Rejection vs Frequency

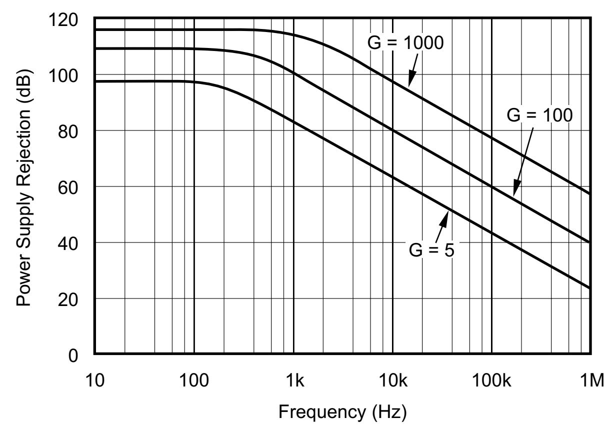


Figure 5-4. Positive Power Supply Rejection vs Frequency

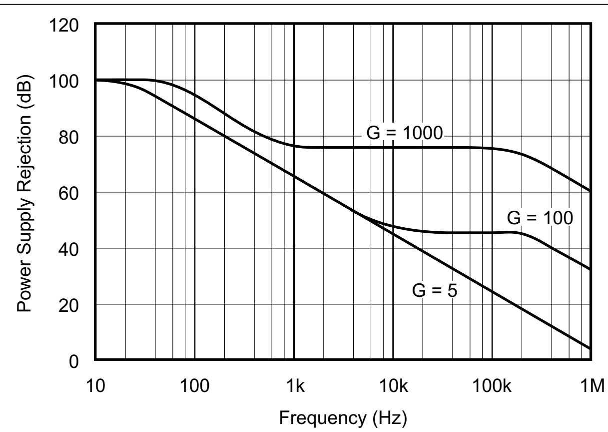
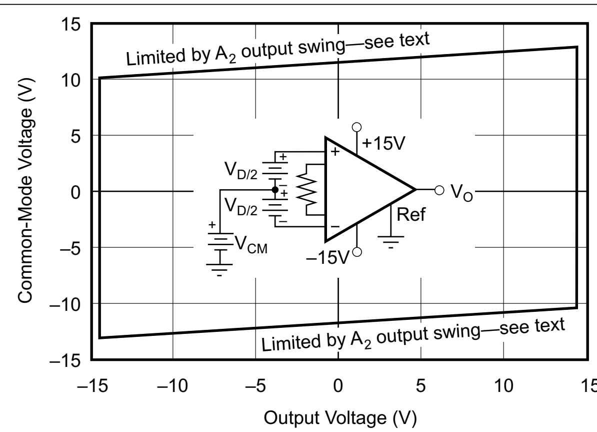


Figure 5-5. Negative Power Supply Rejection vs Frequency

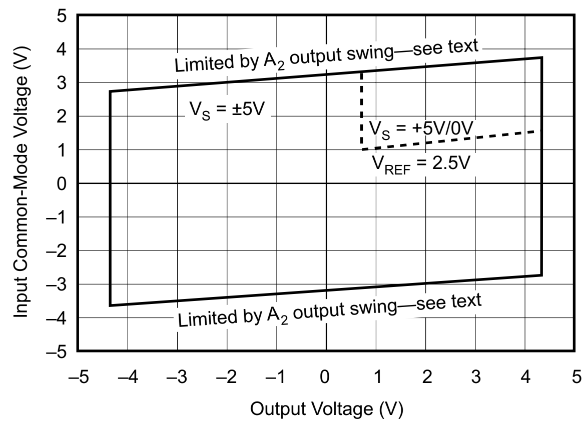


V_S = ±15V

Figure 5-6. Input Common-Mode Voltage Range vs Output Voltage

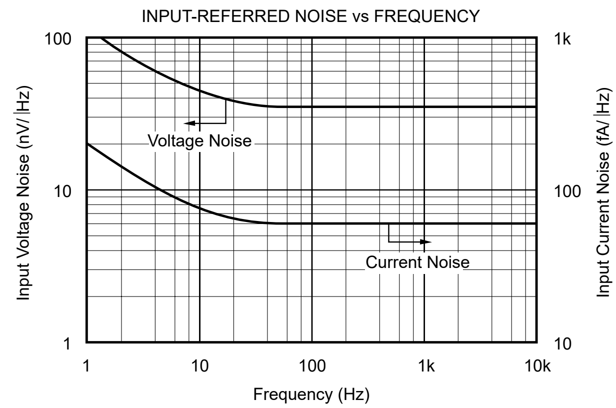
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, all chips site origins (CSO), unless otherwise noted



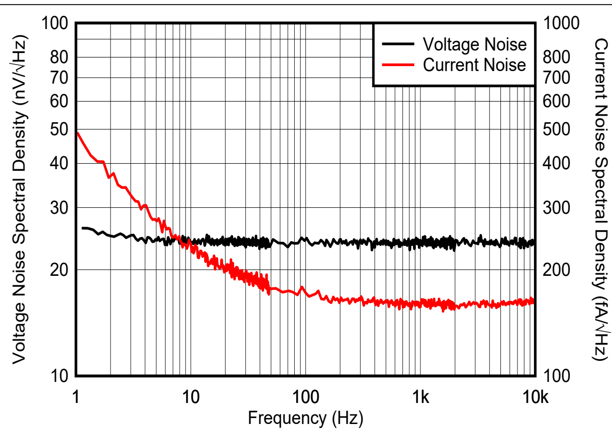
V_S = ±5V

Figure 5-7. Input Common-Mode Voltage Range vs Output Voltage



CSO: SHE

Figure 5-8. Input-Referred Noise vs Frequency



CSO: TID

Figure 5-9. Input-Referred Noise vs Frequency

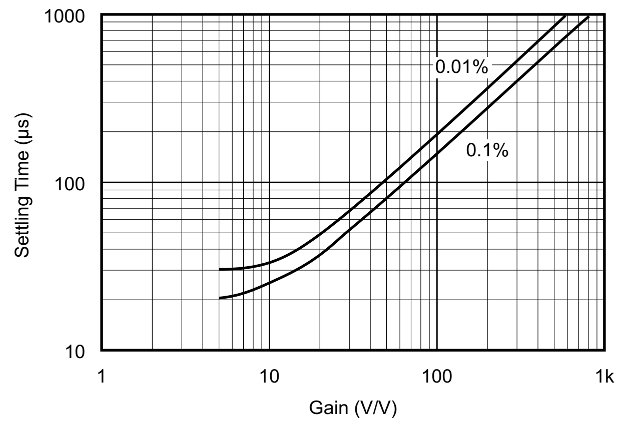
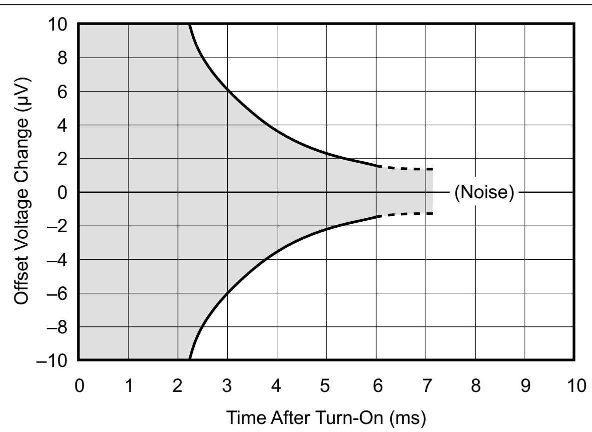
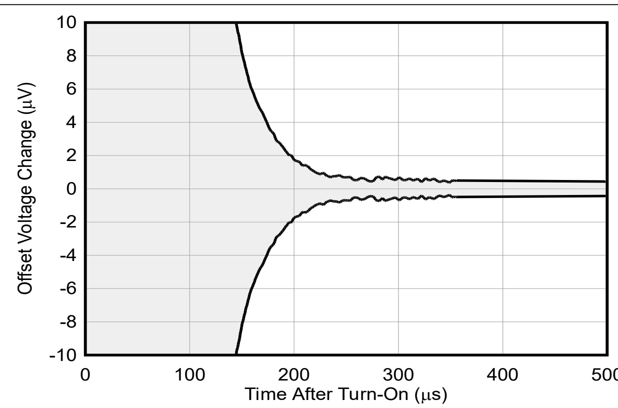


Figure 5-10. Settling Time vs Gain



CSO: SHE

Figure 5-11. Input-Referred Offset Voltage Warmup



CSO: TID

Figure 5-12. Input-Referred Offset Voltage Warmup

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, all chips site origins (CSO), unless otherwise noted

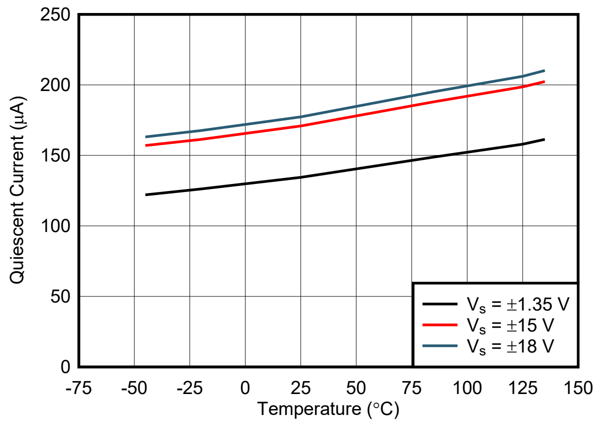


Figure 5-13. Quiescent Current vs Temperature

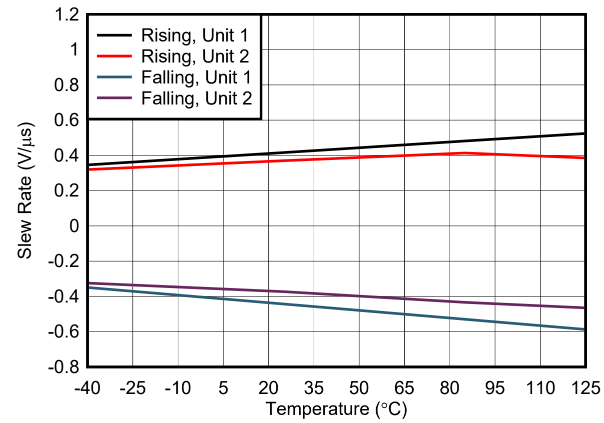
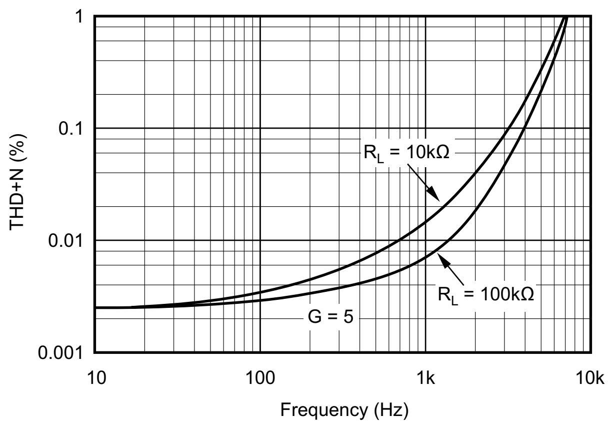
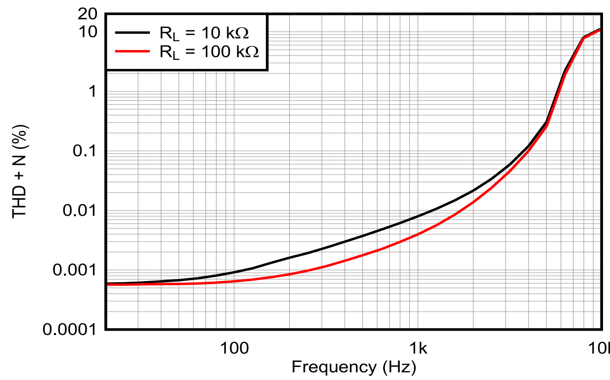


Figure 5-14. Slew Rate vs Temperature



CSO: SHE

Figure 5-15. Total Harmonic Distortion + Noise vs Frequency



CSO: TID

Figure 5-16. Total Harmonic Distortion + Noise vs Frequency

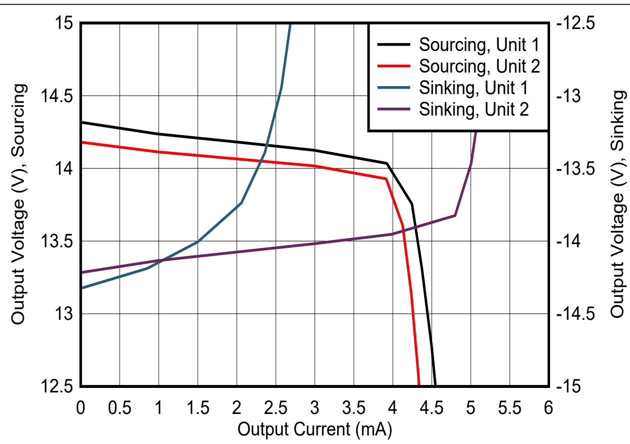
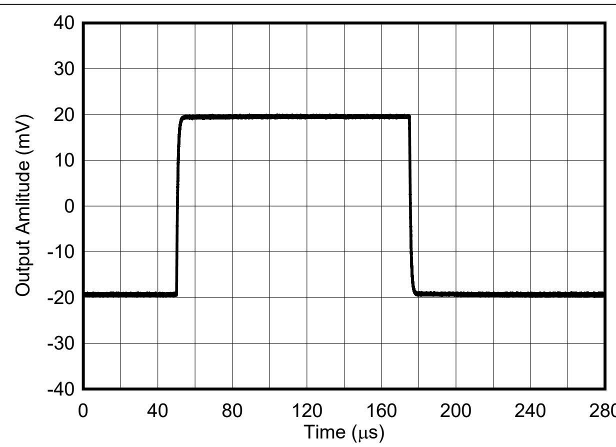


Figure 5-17. Output Voltage Swing vs Output Current



G = 5

Figure 5-18. Small-Signal Response

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, all chips site origins (CSO), unless otherwise noted

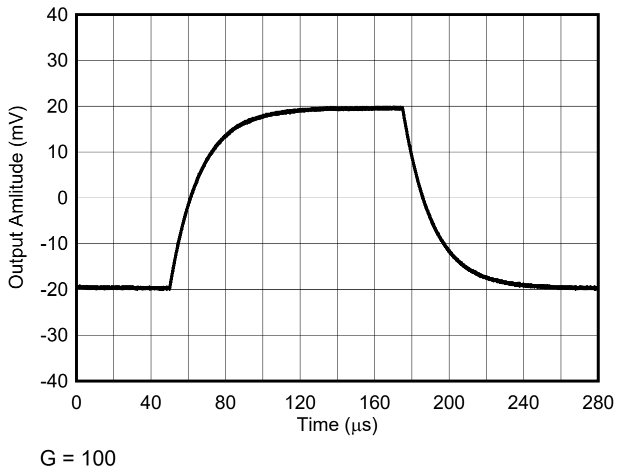


Figure 5-19. Small-Signal Response

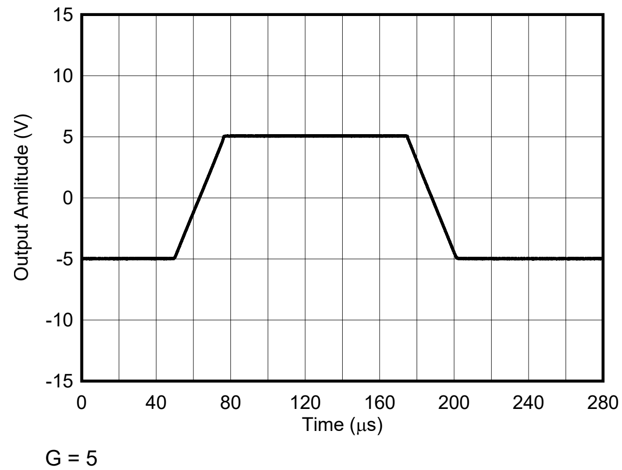


Figure 5-20. Large-Signal Response

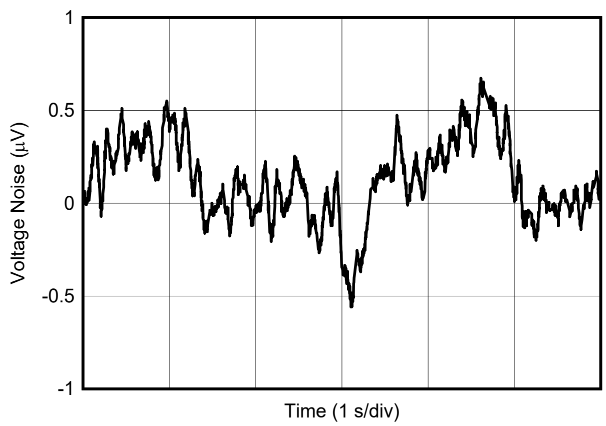


Figure 5-21. 0.1Hz to 10Hz Voltage Noise

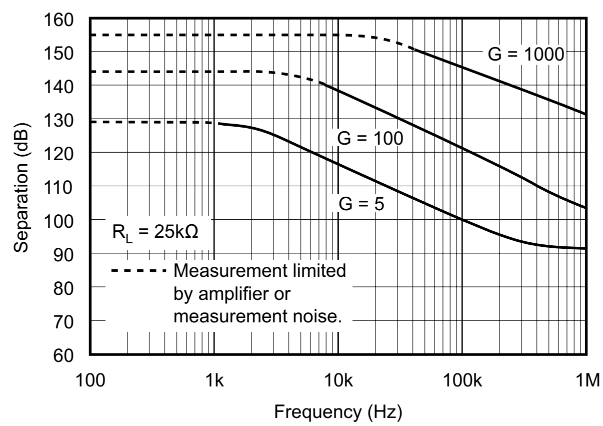


Figure 5-22. Channel Separation vs Frequency, RTI (Dual Version)

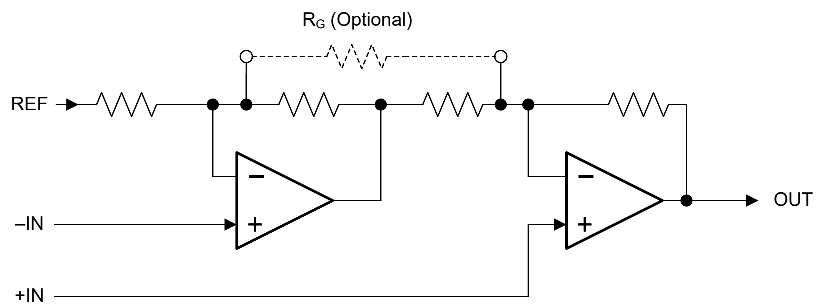
6 Detailed Description

6.1 Overview

The INAx126 use only two, rather than three, operational amplifiers, providing savings in power consumption. In addition, the input resistance is high and balanced, thus permitting the signal source to have an unbalanced output impedance.

A minimum circuit gain of 5 permits an adequate dc common-mode input range, as well as sufficient bandwidth for most applications.

6.2 Functional Block Diagram



6.3 Feature Description

The INAx126 are low-power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile two-operational-amplifier design and small size make the amplifiers an excellent choice for a wide range of applications. The two-op-amp topology reduces power consumption. A single external resistor sets any gain from 5 to 10,000. These devices operate with power supplies as low as ±1.35V, and a quiescent current of 200μA maximum.

6.4 Device Functional Modes

6.4.1 Single-Supply Operation

The INAx126 can be used on single power supplies from 2.7V to 36V. Use the output REF pin to level shift the internal output voltage into a linear operating condition. Ideally, connect the REF pin to a potential that is midsupply to avoid saturating the output of the amplifiers. See *Section 7.1* for information on how to adequately drive the reference pin.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The INAx126 measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high input impedance make the INAx126 an excellent choice for a wide range of applications. The INAx126 can adjust the functionality of the output signals by setting the reference pin, giving additional flexibility that is practical for multiple configurations.

7.2 Typical Application

Figure 7-1 shows the basic connections required for operation of the INA126. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins as shown.

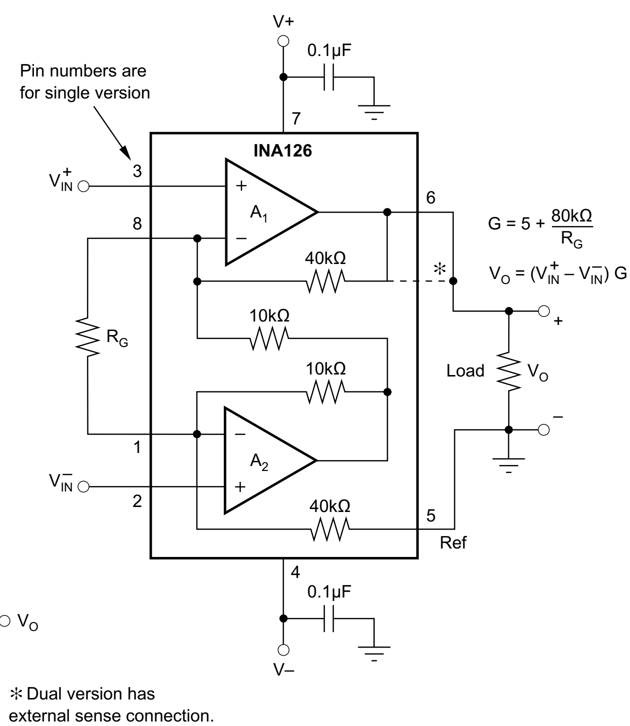
The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of 8Ω in series with the Ref pin causes a typical device to degrade to approximately 80dB CMR.

Figure 7-4 depicts a desired differential signal from a sensor at 1kHz and 5mV$_{PP}$ superimposed on top of a 1V$_{PP}$, 60Hz common-mode signal (the 1kHz signal can not be resolved in this scope trace). The FFT trace in Figure 7-5 shows the two signals. Figure 7-6 shows the clearly recovered differential signal at the output of the INA126 operating at a gain of 250. The FFT of Figure 7-7 shows the 60Hz common-mode is no longer visible.

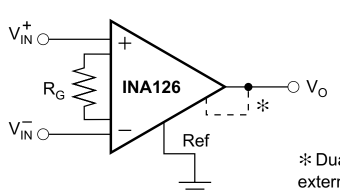
The dual version INA2126 has feedback-sense connections, Sense$_A$ and Sense$_B$, that must be connected to the respective output pins for proper operation. The sense connection can sense the output voltage directly at the load for best accuracy.

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G VALUE
5	NC	NC
10	16k	15.8k
20	5333	5360
50	1779	1780
100	842	845
200	410	412
500	162	162
1000	80.4	80.6
2000	40.1	40.2
5000	16.0	15.8
10000	8.0	7.87

NC: No Connection.



Also drawn in simplified form:



✻ Dual version has external sense connection.

Figure 7-1. Basic Connections

7.2.1 Design Requirements

For the traces shown in Figure 7-2 and Figure 7-3:

- Common-mode rejection of at least 80dB
- Gain of 250

7.2.2 Detailed Design Procedure

7.2.2.1 Setting the Gain

Gain is set by connecting an external resistor, R_G:

$$g = 5 + 80k\Omega / R_G \tag{1}$$

Commonly used gains and R_G resistor values are shown in Figure 7-1.

The 80kΩ term in Equation 1 comes from the internal metal-film resistors, which are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The R_G contribution to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error in gains of approximately 100 or greater.

7.2.2.2 Offset Trimming

The INAx126 family features low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 7-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref pin is added to the output signal. An operational amplifier buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

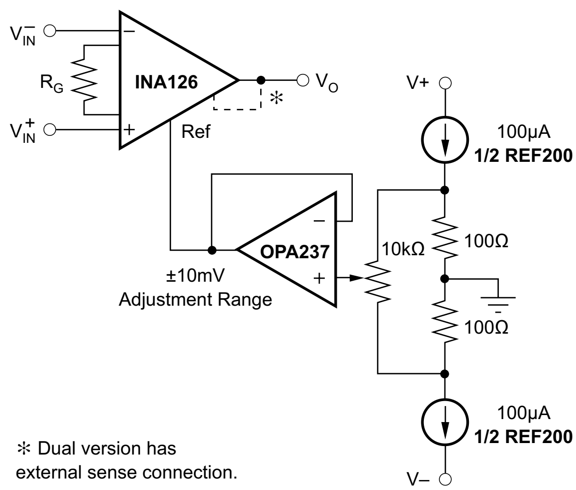


Figure 7-2. Optional Trimming of Output Offset Voltage

7.2.2.3 Input Bias Current Return

The input impedance of the INAx126 is extremely high at approximately 10^9 Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is typically –10nA (current flows out of the input pins). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 7-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range, and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 7-3). With higher source impedance, using two equal resistors provides a balanced input with the advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

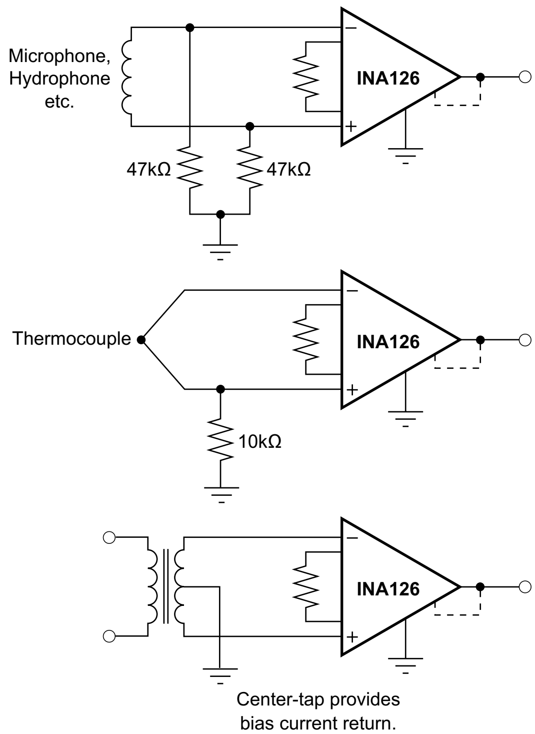


Figure 7-3. Providing an Input Common-Mode Current Path

7.2.2.4 Input Common-Mode Range

The input common-mode range of the INAx126 is shown in *Section 5.7*. The common-mode range is limited on the negative side by the output voltage swing of A_2, an internal circuit node that cannot be measured on an external pin. The output voltage of A_2 can be expressed as shown in Equation 2:

$$V_{O2} = 1.25V^-_{IN} - (V^+_{IN} - V^-_{IN})\,(10k\Omega/R_G) \tag{2}$$

where

- Voltages referred to Ref, pin 5

The internal op amp A_2 is identical to A_1, with an output swing typically limited to 0.7V from the supply rails. When the input common-mode range is exceeded (A_2 output is saturated), A_1 can still be in linear operation and respond to changes in the noninverting input voltage. The output voltage, however, is invalid.

7.2.2.5 Input Protection

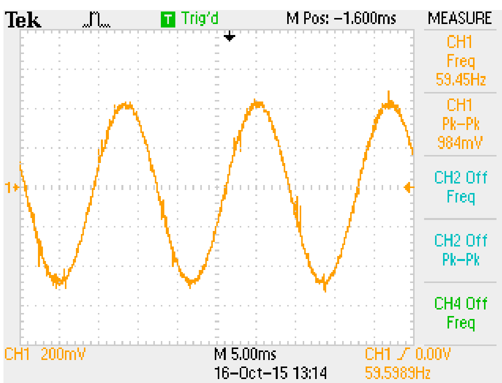
The inputs are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent the signal from exceeding the power supplies by more than approximately 0.7 V. If the signal-source voltage can exceed the power supplies, the source current should be limited to less than 10mA. This limiting can generally be done with a series resistor. Some signal sources are inherently current-limited, and do not require limiting resistors.

7.2.2.6 Channel Crosstalk—Dual Version

The two channels of the INA2126 are completely independent, including all bias circuitry. At dc and low frequency, there is virtually no signal coupling between channels. Crosstalk increases with frequency and depends on circuit gain, source impedance, and signal characteristics.

As source impedance increases, careful circuit layout can help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Carefully balance the stray capacitance of each input to ground, and run the differential inputs of each channel parallel to each other, or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal that is rejected by the IA input.

7.2.3 Application Curves



Differential signal is too small to be seen

Figure 7-4. Common-mode Signal at INA126 Input

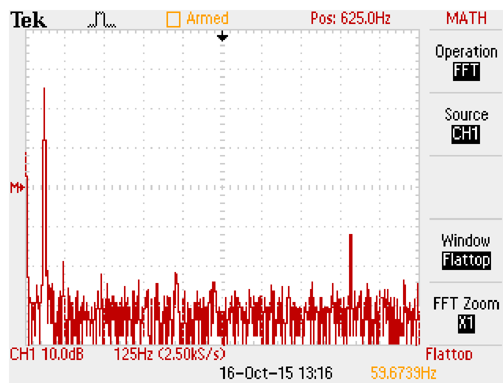


Figure 7-5. FFT of Signal in Previous Figure Shows Both the 60Hz Common-mode Along With 5kHz Differential Signal

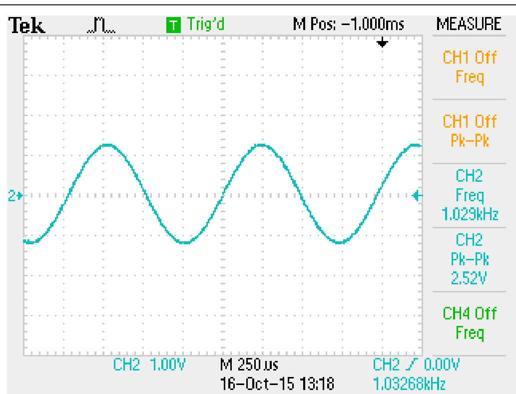


Figure 7-6. Recovered Differential Signal at the Output of the INA126 With a Gain of 250

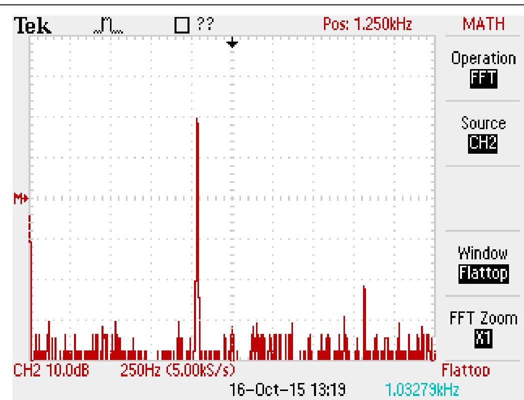


Figure 7-7. FFT of the INA126 Output Shows that the 60Hz Common-mode Signal is Rejected

7.3 Power Supply Recommendations

7.3.1 Low-Voltage Operation

The INAx126 can be operated on power supplies as low as ±1.35V. Performance remains excellent with power supplies ranging from ±1.35 V to ±18V. Most parameters vary only slightly throughout this supply voltage range (see *Section 5.7*). Operation at low supply voltage requires careful attention to make sure that the common-mode voltage remains within the linear range (see Figure 5-6 and Figure 5-7).

The INAx126 operates from a single power supply with careful attention to input common-mode range, output voltage swing of both op amps, and the voltage applied to the Ref pin. Figure 7-8 shows a bridge amplifier circuit operated from a single 5V power supply. The bridge provides an input common-mode voltage near 2.5V, with a relatively small differential voltage.

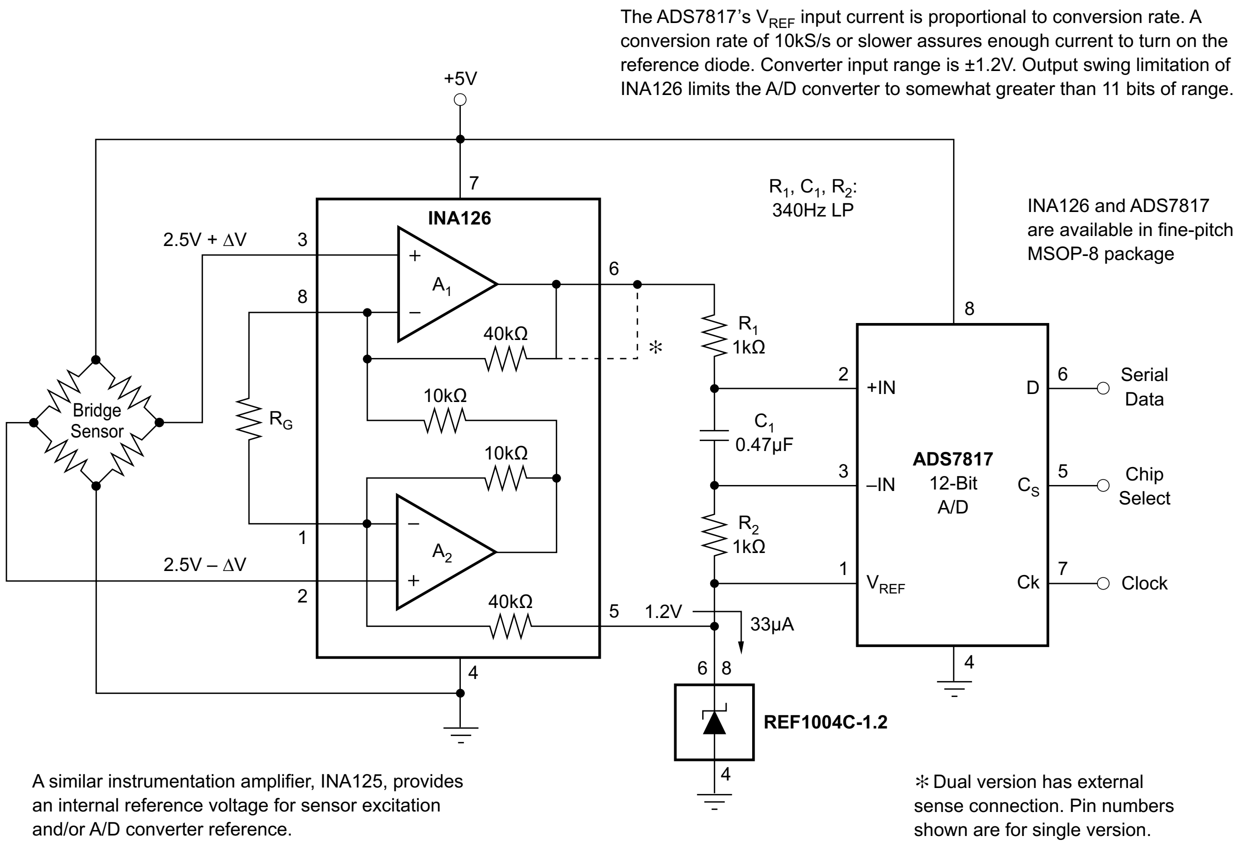


Figure 7-8. Bridge Signal Acquisition, Single 5V Supply

7.4 Layout

7.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible.
  - Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *PCB Design Guidelines For Reduced EMI* application note.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 7-9, keep R_G close to the pins to minimize parasitic capacitance.
- Keep the traces as short as possible

7.4.2 Layout Example

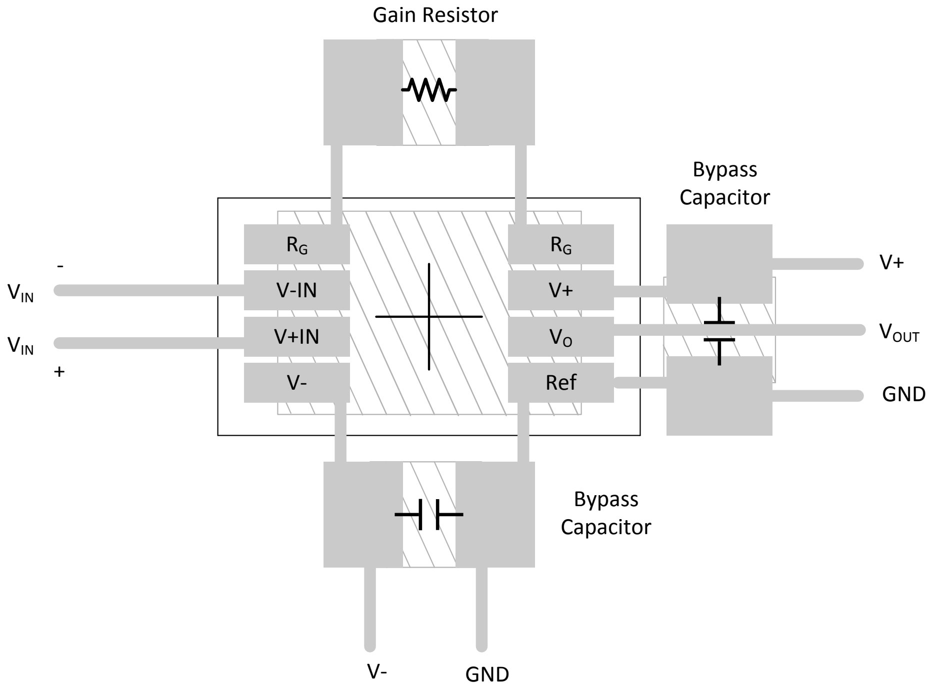


Figure 7-9. INA126 Layout Example

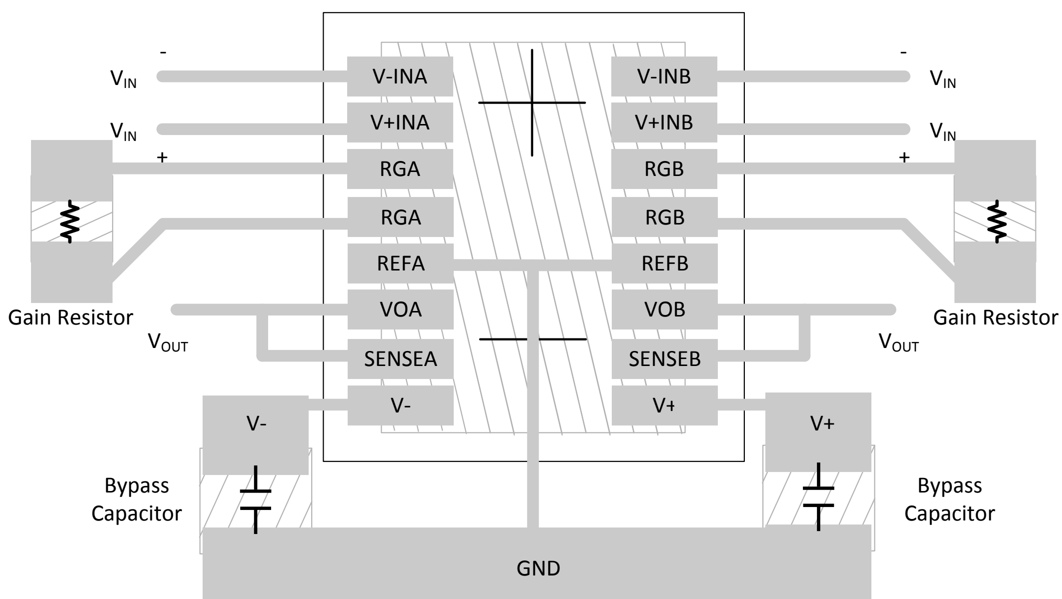


Figure 7-10. INA2126 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

8.1.2 Device Nomenclature

PART NUMBER	DEFINITION
INAx126E/250, INAx126E/2K5, INAx126EA/250, INAx126U, INAx126U/2K5, INAx126UA, INAx126UA/2K5	The die is manufactured in CSO: SHE or CSO: TID.
INA126P, INA126PA, INA126-W	The die is only manufactured in CSO: SHE.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *PCB Design Guidelines For Reduced EMI* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2021) to Revision D (December 2025) **Page**

- Added description of device flow information in the *Specifications*........ 5
- Added *all chips site origins (CSO)* condition to the typical test conditions in the *Electrical Characteristics* 7
- Added different fabrication process specifications for Input Impedance in the *Electrical Characteristics* 7
- Added different fabrication process specifications for Voltage Noise in the *Electrical Characteristics* 7
- Added different fabrication process specifications for Bandwidth, –3dB in the *Electrical Characteristics* 7
- Added *all chips site origins (CSO)* condition to the typical test conditions in the *Typical Characteristics* 9
- Added CSO: SHE flow information to *Gain vs Frequency*, *Input-Referred Offset Voltage Warmup*, and *Total Harmonic Distortion + Noise Frequency* curves in the *Typical Characteristics* 9
- Added *Input-Referred Noise vs Frequency* curve for CSO: SHE flow in the *Typical Characteristics* 9
- Added CSO: TID flow information to *Input-Referred Noise vs Frequency* curve in the *Typical Characteristics* 9
- Added *Gain vs Frequency*, *Input-Referred Offset Voltage Warmup*, and *Total Harmonic Distortion + Noise Frequency* curves for CSO: TID flow in the *Typical Characteristics* 9
- Added part number flow information table to the *Device Nomenclature* 21

Changes from Revision B (December 2015) to Revision C (December 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added dual supply specification to *Absolute Maximum Ratings* 5
- Deleted redundant operating temperature and input common mode voltage specifications in *Recommended Operating Conditions* 5
- Added dual supply and specified temperature specifications in *Recommended Operating Conditions* 5
- Added proper signs for PSRR and input bias current specifications in *Electrical Characteristics* 7
- Deleted V_O = 0 V test condition of common-mode voltage specification in *Electrical Characteristics* 7
- Changed common-mode voltage specification from ±11.25 V minimum, to –11.25 V minimum and 11.25 V maximum, in *Electrical Characteristics* 7
- Changed minimum CMRR specification for INA126U/E, INA2126E from 83 dB to 80 dB in *Electrical Characteristics* 7
- Added typical input bias current specification of ±10 nA for INA126PA/UA/EA and INA2126PA/UA/EA in *Electrical Characteristics* 7
- Changed current noise specifications in *Electrical Characteristics* from 60 fA/√Hz to 160 fA/√Hz for f = 1 kHz, and from 2 pApp to 7.3 pApp for f = 0.1 Hz to 10 Hz........ 7
- Changed test condition for short-circuit current specification in *Electrical Characteristics* from "Short circuit to ground" to "Continuous to V_S / 2" for clarity........ 7
- Changed short-circuit current specification in *Electrical Characteristics* from +10/-5 mA to ±5 mA...................7
- Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics* 7
- Changed Figures 6-7, 6-10, 6-13, 6-14, 6-15, 6-16, 6-17 9
- Added Figure 6-11........9

Changes from Revision A (August 2005) to Revision B (December 2015) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section................... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.