

INA116

Ultra Low Input Bias Current INSTRUMENTATION AMPLIFIER

FEATURES

- LOW INPUT BIAS CURRENT: 3fA typ
- BUFFERED GUARD DRIVE PINS
- LOW OFFSET VOLTAGE: 2mV max
- HIGH COMMON-MODE REJECTION: 84dB (G = 10)
- LOW QUIESCENT CURRENT: 1mA
- INPUT OVER-VOLTAGE PROTECTION: $\pm 40V$

APPLICATIONS

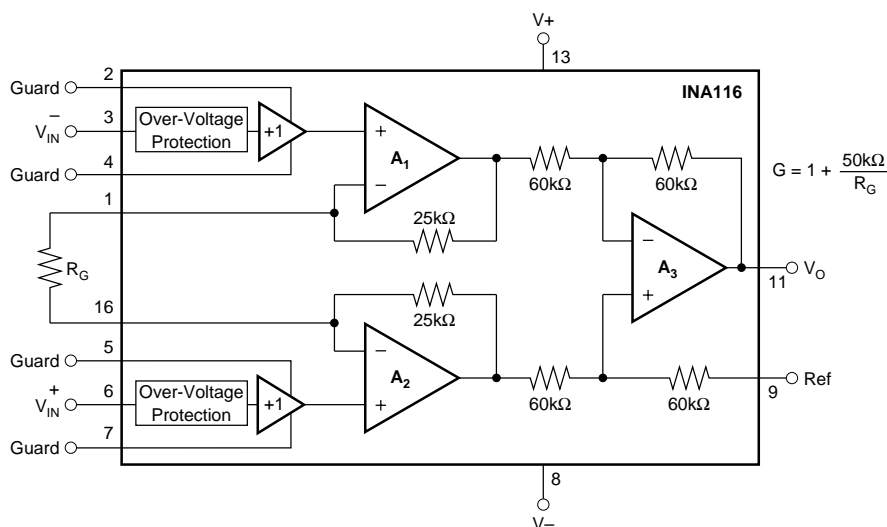
- LABORATORY INSTRUMENTATION
- pH MEASUREMENT
- ION-SPECIFIC PROBES
- LEAKAGE CURRENT MEASUREMENT

DESCRIPTION

The INA116 is a complete monolithic FET-input instrumentation amplifier with extremely low input bias current. *Difet*[®] inputs and special guarding techniques yield input bias currents of 3fA at 25°C, and only 25fA at 85°C. Its 3-op amp topology allows gains to be set from 1 to 1000 by connecting a single external resistor.

Guard pins adjacent to both input connections can be used to drive circuit board and input cable guards to maintain extremely low input bias current.

The INA116 is available in 16-pin plastic DIP and SOL-16 surface-mount packages, specified for the -40°C to +85°C temperature range.



Difet[®], Burr-Brown Corporation

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SPECIFICATIONS

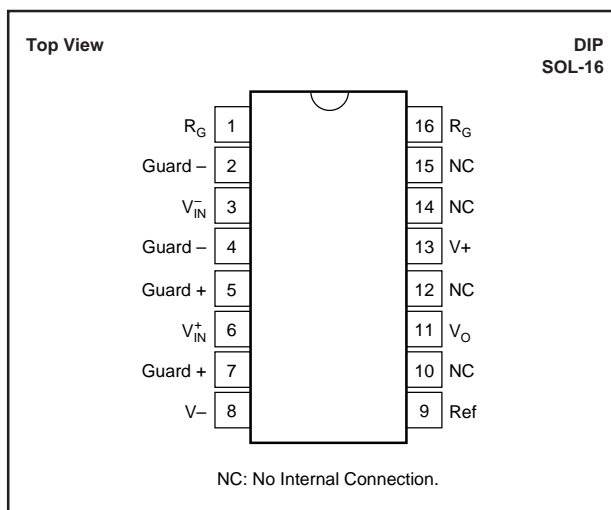
AT $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	INA116P, U			INA116PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX} $V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$		$\pm 0.5 \pm 0.5/\text{G}$	$\pm 2 \pm 2/\text{G}$		*	$\pm 5 \pm 5/\text{G}$	mV
Initial			See Typical Curve			*		
vs Temperature			$\pm 10 \pm 15/\text{G}$	$\pm 50 \pm 100/\text{G}$		*	$\pm 100 \pm 200/\text{G}$	$\mu\text{V}/^\circ\text{V}$
vs Power Supply			$\pm 1 \pm 5/\text{G}$			*		$\mu\text{V}/\text{mV}$
Long-Term Stability			± 3	± 25		*	± 100	fA
Bias Current			See Typical Curve			*		
vs Temperature			± 1	± 25		*	± 100	fA
Offset Current			See Typical Curve			*		
vs Temperature			$>10^{15}/0.2$			*		Ω/pF
Impedance, Differential			$>10^{15}/7$			*		Ω/pF
Common-Mode	$V_{\text{CM}} = \pm 11\text{V}$, $\Delta R_S = 1\text{k}\Omega$ $G = 1$ $G = 10$ $G = 100$ $V_{\text{CM}} = \pm 5\text{V}$, $G = 1000$	(V+)-4	(V+)-2		*	*		V
Common-Mode Voltage Range		(V-)+4	(V-)+2.4		*	*		V
Safe Input Voltage		± 40			*	*		V
Common-Mode Rejection						*		
		80	89		73	*		dB
		84	92		78	*		dB
		86	94		80	*		dB
		86	94		80	*		dB
						*		
						*		
NOISE								
Voltage Noise, RTI	$G = 1000$, $R_S = 0\Omega$		28			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			2			*		$\mu\text{Vp-p}$
$f_B = 0.1\text{Hz}$ to 10Hz						*		
Current Noise	$f = 1\text{kHz}$		0.1			*		$\text{fA}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$						*		
						*		
GAIN								
Gain Equation	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $G = 1$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$	1	$1+(50\text{k}\Omega/R_G)$	1000	*	*	*	V/V
Range of Gain			± 0.01	± 0.05		*	0.1	V/V
Gain Error			± 0.25	± 0.4		*	± 0.5	%
			± 0.35	± 0.5		*	± 0.7	%
			± 1.25			*		%
Gain vs Temperature ⁽¹⁾			± 5	± 10		*	± 20	$\text{ppm}/^\circ\text{C}$
50k Ω Resistance ⁽¹⁾⁽²⁾			± 25	± 100		*	± 100	$\text{ppm}/^\circ\text{C}$
Nonlinearity			± 0.0005	± 0.005		*	± 0.01	% of FSR
			± 0.001	± 0.005		*	± 0.01	% of FSR
			± 0.001	± 0.005		*	± 0.01	% of FSR
GUARD OUTPUTS								
Offset Voltage			± 15	± 50		*	*	mV
Output Impedance			650			*		Ω
Current Drive			$\pm 2/-0.05$			*		mA
OUTPUT								
Voltage Positive	$R_L = 10\text{k}\Omega$ $R_L = 10\text{k}\Omega$	(V+) -1	(V+) -0.7		*	*		V
Negative		(V-) +0.35	(V-) +0.2		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			$\pm 5/-12$			*		mA
						*		
FREQUENCY RESPONSE								
Bandwidth, -3dB	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $G = 10$ to 200 10V Step, $G = 1$ $G = 10$ $G = 100$ $G = 1000$		800			*		kHz
			500			*		kHz
			70			*		kHz
			7			*		kHz
Slew Rate			0.8			*		V/ μs
Settling Time, 0.01%			22			*		μs
			25			*		μs
			145			*		μs
			400			*		μs
Output Overload Recovery			20			*		μs
POWER SUPPLY								
Voltage Range	$V_{\text{IN}} = 0\text{V}$	± 4.5	± 15	± 18	*	*	*	V
Current			± 1	± 1.4		*	*	mA
TEMPERATURE RANGE								
Specification		-40		85	*		*	$^\circ\text{C}$
Operating		-40		125	*		*	$^\circ\text{C}$
θ_{JA}			80			*		$^\circ\text{C}/\text{W}$

* Specification same as INA116P

NOTE: (1) Guaranteed by wafer test. (2) Temperature coefficient of the "50k Ω " term in the gain equation.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

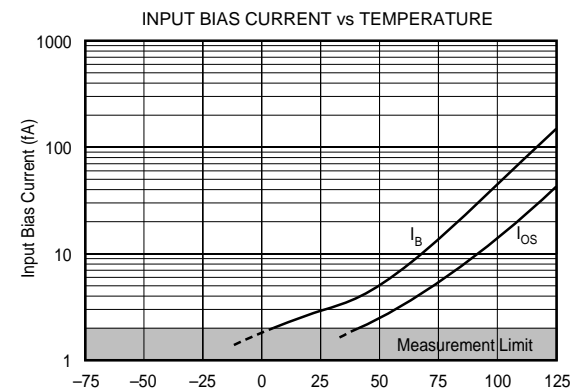
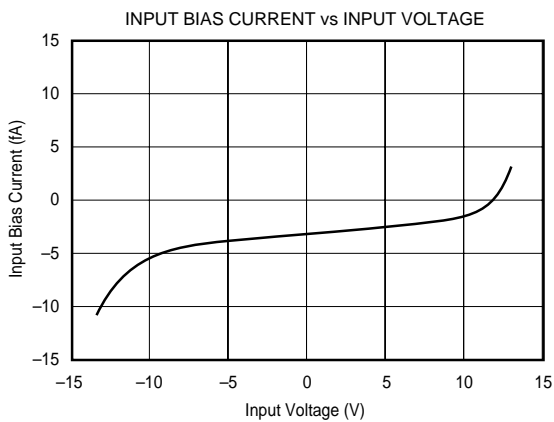
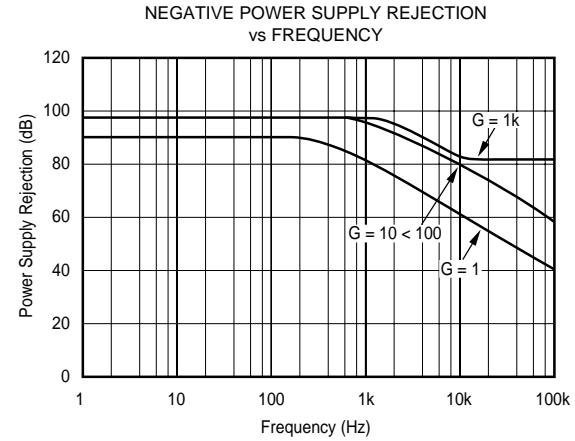
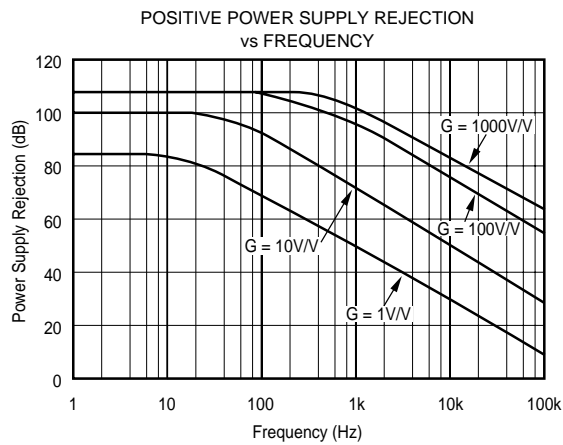
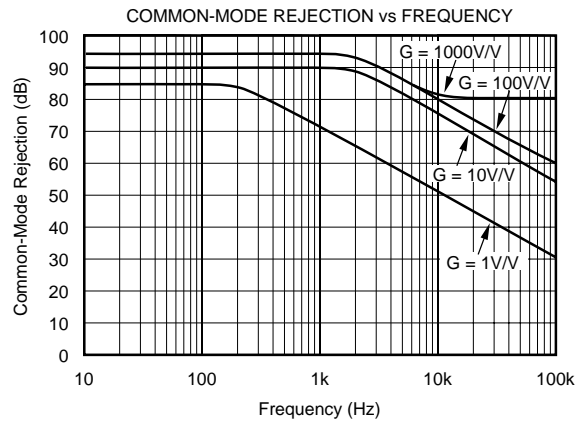
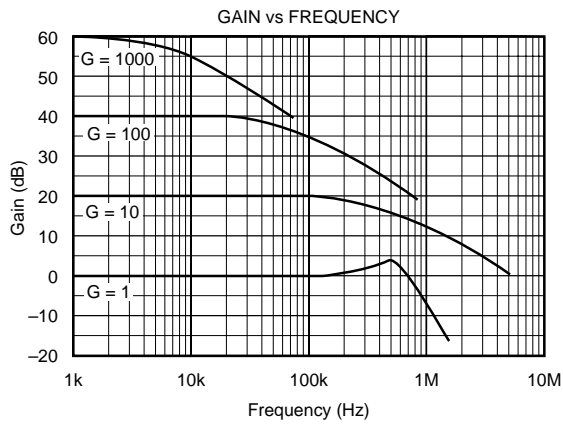
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
INA116PA	16-Pin Plastic DIP	180
INA116P	16-Pin Plastic DIP	180
INA116UA	SOL-16 Surface-Mount	211
INA116U	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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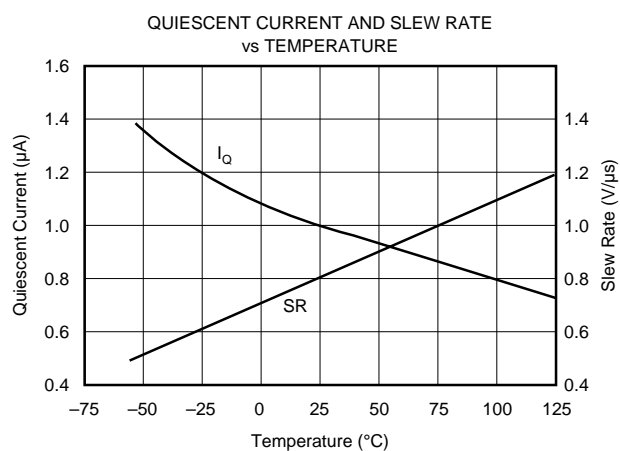
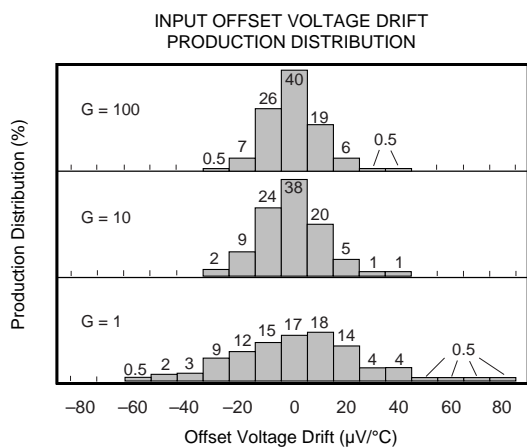
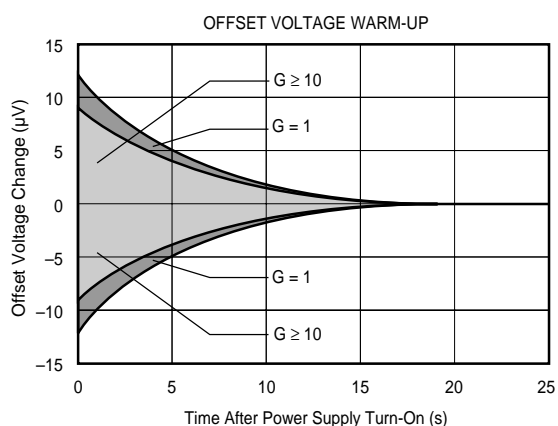
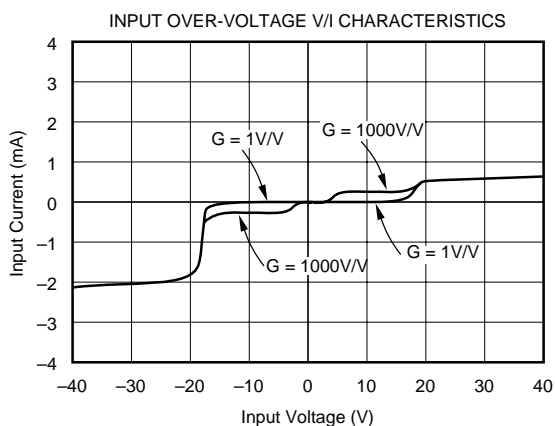
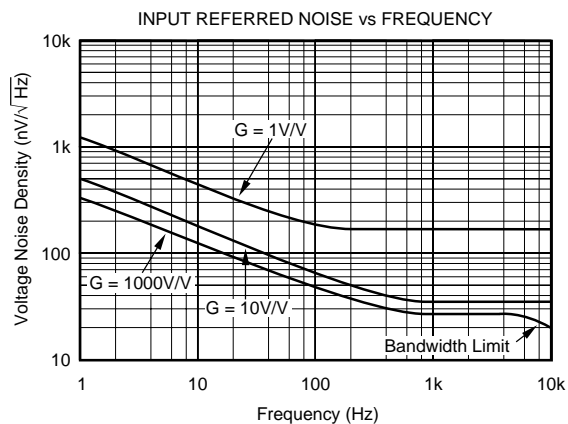
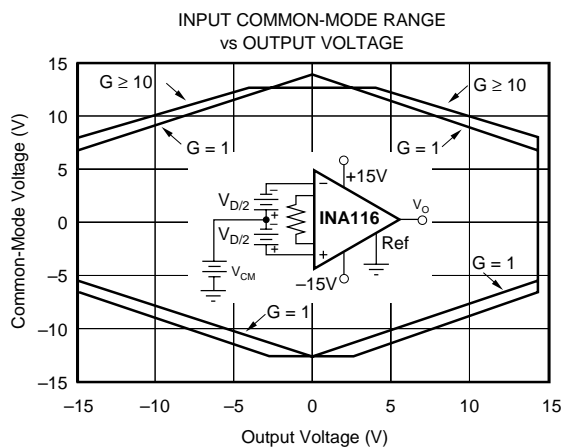
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$, unless otherwise noted.



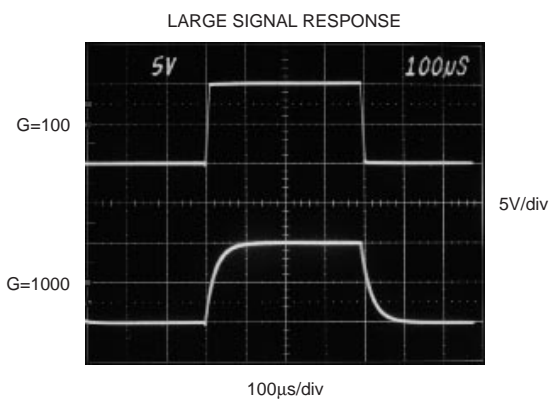
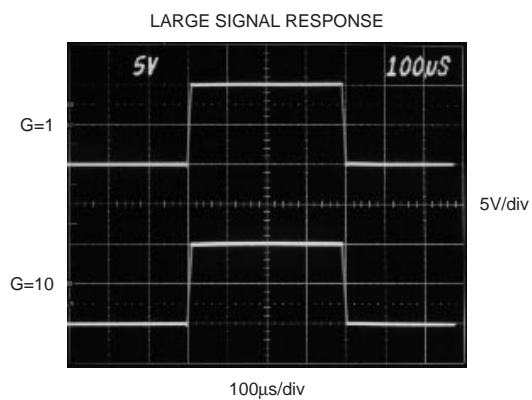
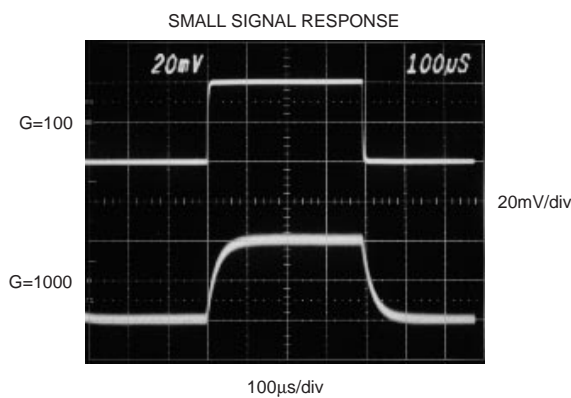
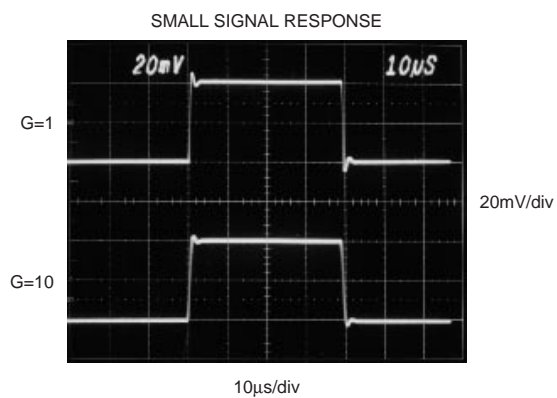
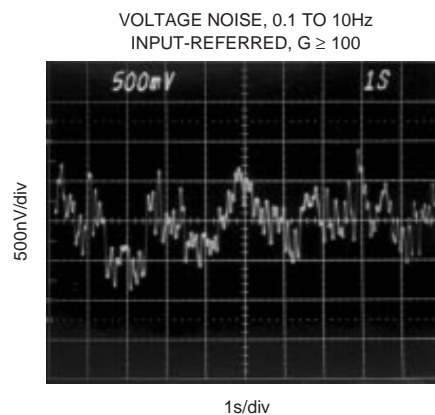
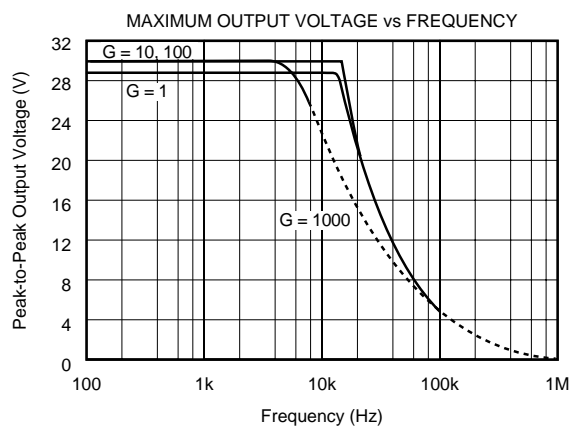
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the connections required for basic operation of the INA116. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the supply pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low impedance connection to assure good common-mode rejection. A resistance of 30Ω in series with this connection will cause a typical device to degrade to approximately 72dB CMR at $G = 1$.

SETTING THE GAIN

Gain of the INA116 is set by connecting a single external resistor, R_G , as shown. The gain is—

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The $50k\Omega$ term in equation 1 is the sum of the two feedback resistors of A_1 and A_2 . These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA116.

The stability and temperature drift of R_G also affect gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain make wiring resistance important. Sockets add to the wiring resistance that will contribute additional gain error in gains of approximately 100 or greater.

OFFSET TRIMMING

The INA116 is laser trimmed for low offset voltage and offset voltage drift; most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. A voltage applied to the Ref terminal is summed at the output. Op amp A_1 provides a low source impedance for the Ref terminal, assuring good common-mode rejection.

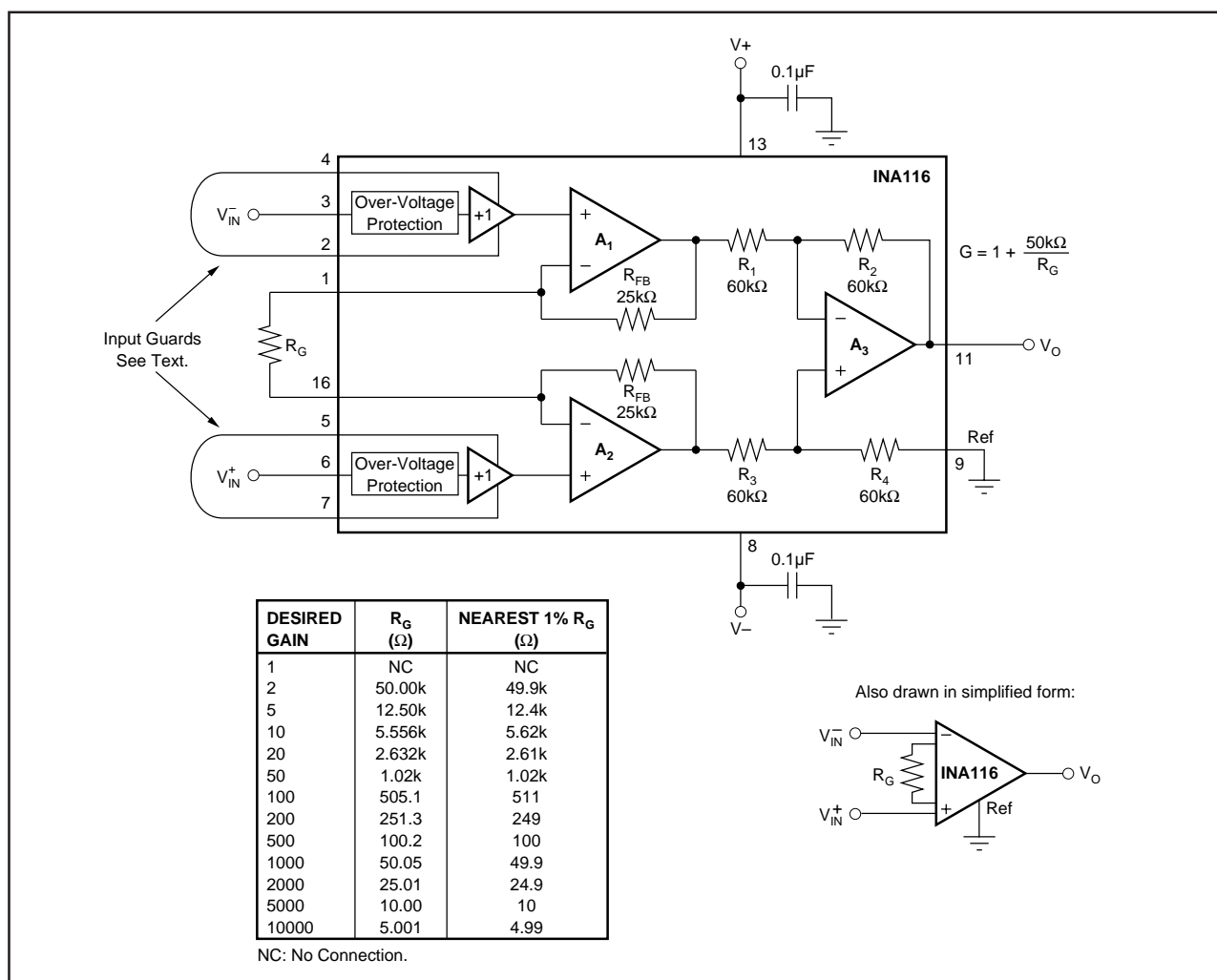


FIGURE 1. Basic Connections.

INPUT CONNECTIONS

Some applications must make high impedance input connections to external sensors or input connectors. To assure low leakage, the input should be guarded all the way to the signal source—see Figure 5. Coaxial cable can be used with the shield driven by the guard. A separate connection is required to provide a ground reference at the signal source. Triaxial cable may reduce noise pickup and provides the ground reference at the source. Drive the inner shield at guard

potential and ground the outer shield. Two separate guarded lines are required if both the inverting and non-inverting inputs are brought to the source.

The guard drive output current is limited to approximately $+2\text{mA}/-50\mu\text{A}$. For slow input signals the internal guard output can directly drive a cable shield. With fast input signals, however, the guard may not provide sufficient output current to rapidly charge the cable capacitance. An op amp buffer may be required as shown in Figure 6.

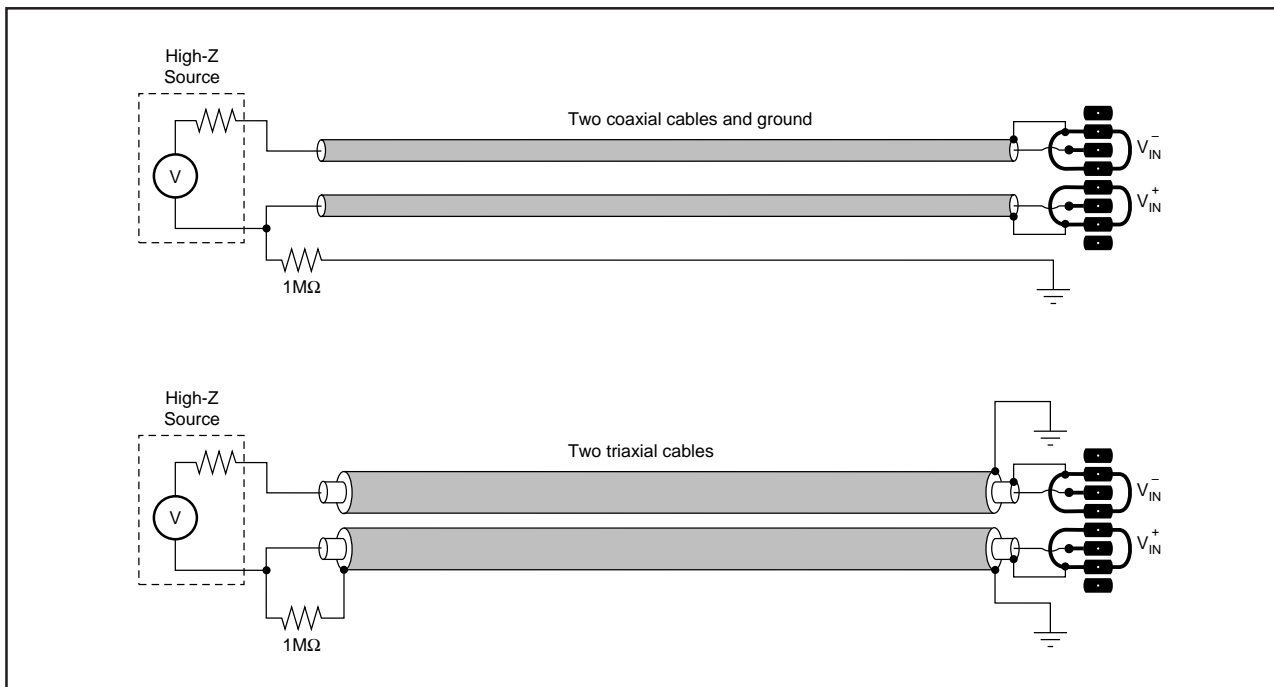


FIGURE 5. Input Cable Guarding Circuits.

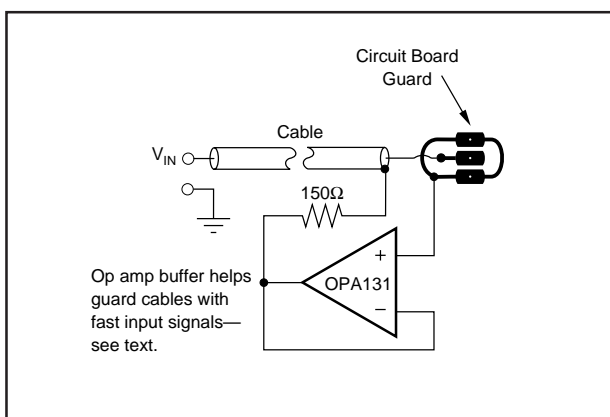


FIGURE 6. Buffered Guard Drive.

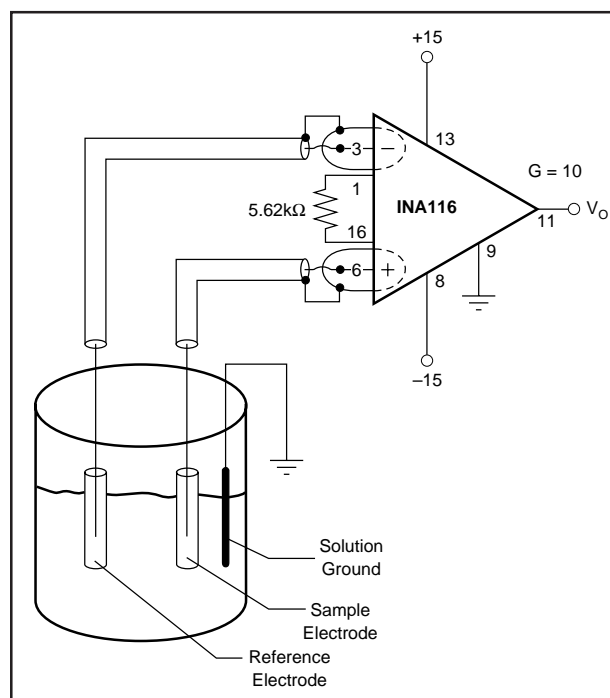


FIGURE 7. pH or Ion Measurement System.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA116PA	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA116PA
INA116UA	NRND	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-	INA116UA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA116PA	N	PDIP	16	25	506	13.97	11230	4.32
INA116UA	DW	SOIC	16	40	507	12.83	5080	6.6
INA116UAG4	DW	SOIC	16	40	507	12.83	5080	6.6

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