

# INA106 Precision Gain = 10 Differential Amplifier

## 1 Features

- Gain of 10 difference amplifier configuration
- High common-mode rejection (CMRR): 86dB (minimum)
- Low gain error: 0.025% (maximum)
- Low gain drift: 4ppm/°C (typical)
- Low nonlinearity: 0.001% (maximum)
- Bandwidth: 0.5MHz (typical)
- Low offset voltage: 200μV (maximum)
- Low offset voltage drift: 0.2μV/°C (typical)

## 2 Applications

- [Battery cell formation & test equipment](#)
- [Sensor tag & data logger](#)
- [Servo drive position feedback](#)
- [Level transmitter](#)
- [String inverter](#)

## 3 Description

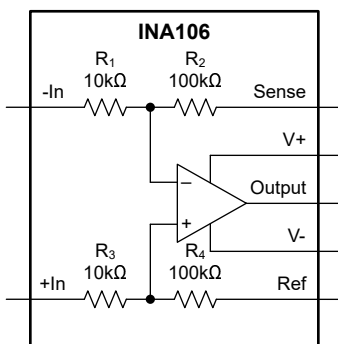
The INA106 is a monolithic gain = 10 differential amplifier consisting of a precision operational amplifier (op amp) and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent tracking of resistors (TCR) maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA106 provides this precision circuit function without using an expensive resistor network. The INA106 is available in 8-pin plastic DIP and SOIC surface-mount packages.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
INA106	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm

- (1) For all available packages, see [Section 10](#).  
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.



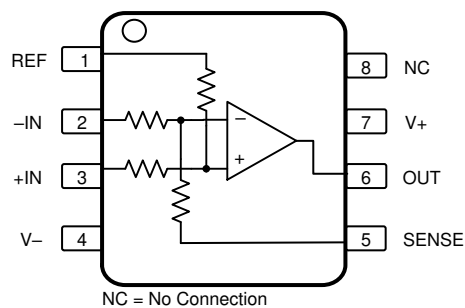
**Precision Gain = 10 Differential Amplifier**



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## 4 Pin Configuration and Functions



**Table 4-1. Pin Functions**

NAME	NO.	TYPE	DESCRIPTION
+IN	3	Input	Positive (noninverting) input 10kΩ resistor to noninverting terminal of op amp
-IN	2	Input	Negative (inverting) input 10kΩ resistor to inverting terminal of op amp
OUT	6	Output	Output
REF	1	Input	Reference input 100kΩ resistor to noninverting terminal of op amp
V+	7	–	Positive (highest) power supply
V-	4	–	Negative (lowest) power supply
SENSE	5	Input	Sense input 100kΩ resistor to inverting terminal of op amp
NC	8	–	No internal connection (can be left floating)

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	36	V
Signal input pins	Single Supply, +In, –In, Sense, and REF	0	$V_S$	V
Output short-circuit <sup>(2)</sup>		Continuous		
Temperature	Operating, $T_A$	–40	85	°C
	Junction, $T_J$		150	
	Storage, $T_{stg}$	–65	125	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to  $V_S / 2$ .

### 5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single supply	10		36	V
	Dual supply	±5		±18	
Specified temperature		0		70	°C

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA106		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.9	74.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.9	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	38.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	4.8	18.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	55.7	37.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ , and  $G = 10$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V <sub>OS</sub>	Offset voltage	RTI <sup>(1) (2)</sup>			50	200	μV
	Offset voltage drift	T <sub>A</sub> = −40°C to +85°C, RTI <sup>(1) (2)</sup>			0.2		μV/°C
PSRR	Power-supply rejection ratio	RTI <sup>(1) (2)</sup> , V <sub>S</sub> = ±6V to ±18V			1	10	μV/V
	Long-term stability				10		μV/mo
ZIN-DM	Differential impedance <sup>(3)</sup>				10		kΩ
ZIN-CM	Common-mode impedance <sup>(3)</sup>				110		kΩ
V <sub>CM</sub>	Operating common-mode input voltage <sup>(4)</sup>			−11		11	V
V <sub>DM</sub>	Operating differential-mode input voltage <sup>(4)</sup>			−1		1	V
CMRR	Common-mode rejection ratio <sup>(5)</sup>	T <sub>A</sub> = −40°C to +125°C		86	100		dB
NOISE VOLTAGE							
e <sub>N</sub>	Voltage noise	RTI <sup>(1) (6)</sup>	f <sub>O</sub> = 10kHz		30		nV/√Hz
			f <sub>B</sub> = 0.01Hz to 10Hz		1.5		μV <sub>PP</sub>
GAIN							
G	Initial gain				10		V/V
GE	Gain error				±0.01	±0.025	%
	Gain drift				−4		ppm/°C
	Gain nonlinearity				0.0002	0.001	% of FSR
OUTPUT							
	Output voltage	I <sub>O</sub> = −5mA, 20mA		10	12		V
	Load capacitance stability				1000		pF
I <sub>sc</sub>	Sourcing	Continuous to V <sub>S</sub> / 2			40 to 70		mA
	Sinking				10 to 70		mA
Z <sub>O</sub>	Output Impedance				0.01		Ω

## 5.4 Electrical Characteristics (continued)

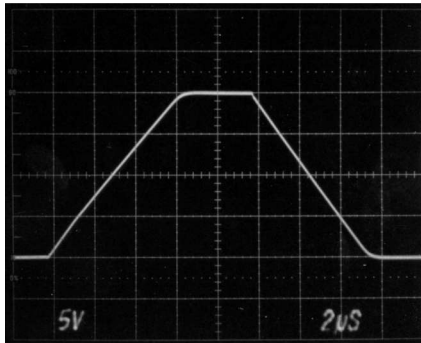
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ , and  $G = 10$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
BW	Bandwidth, −3dB			0.5			MHz
FPBW	Full Power Bandwidth, −3dB	V <sub>O</sub> = 20Vpp		300	400		kHz
SR	Slew rate			2	3		V/μs
t <sub>s</sub>	Settling time	0.1%, V <sub>STEP</sub> = 10V		5			μs
		0.01%, V <sub>STEP</sub> = 10V		10			μs
		0.01%, V <sub>CM-STEP</sub> = 10V, V <sub>DIFF</sub> = 0V		5			μs
POWER SUPPLY							
I <sub>Q</sub>	Quiescent current	V <sub>O</sub> = 0V		±1.5		±2	mA

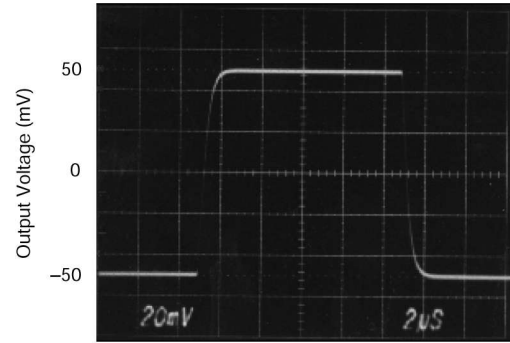
- (1) Referred to input in difference configuration.
- (2) Includes effects of amplifier's input bias and offset currents.
- (3) 25k $\Omega$  resistors are ratio matched but have  $\pm 20\%$  absolute value.
- (4) Maximum input voltage without protection is 10V more than either  $\pm 15\text{V}$  supply ( $\pm 25\text{V}$ ). Limit  $I_{\text{IN}}$  to 1mA.
- (5) With zero source impedance.
- (6) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

## 5.5 Typical Characteristics

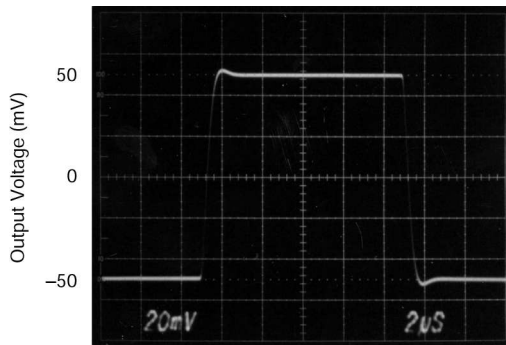
at  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$  (unless otherwise noted)



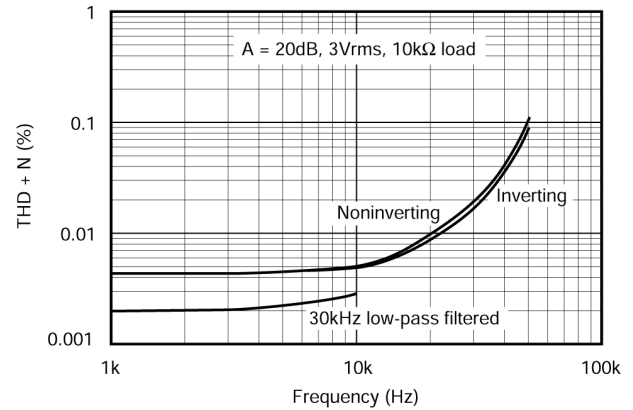
2μs/div  
**Figure 5-1. Step Response**



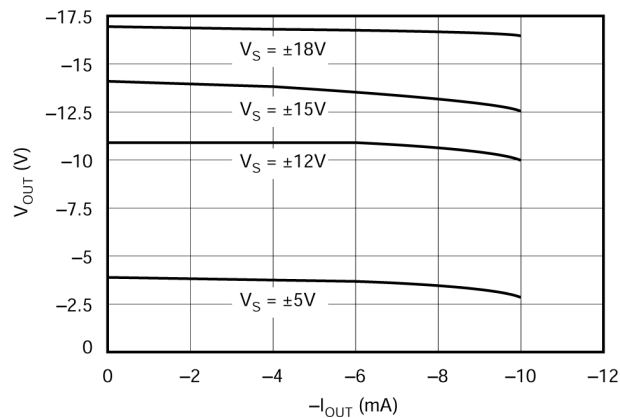
2μs/div  
**Figure 5-2. Small-Signal Response (No Load)**



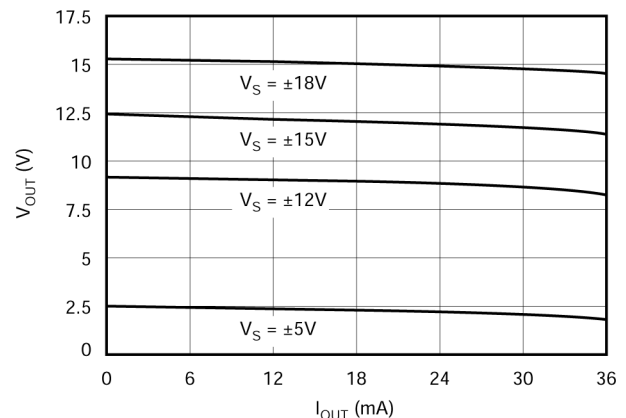
2μs/div  
**Figure 5-3. Small-Signal Response ( $R_{LOAD} = \infty$ ,  $C_{LOAD} = 100\text{pF}$ )**



**Figure 5-4. Total Harmonic Distortion and Noise vs Frequency**



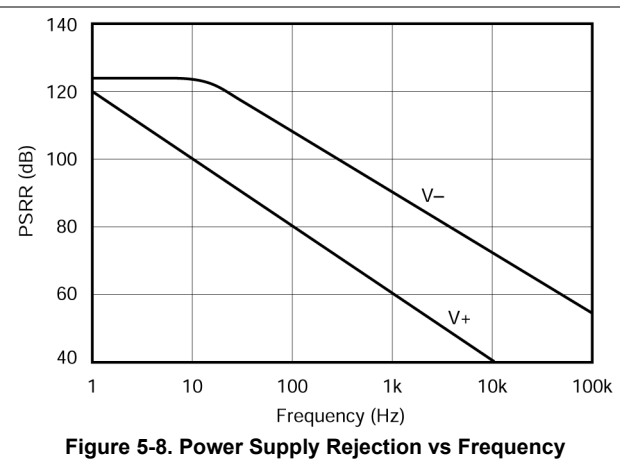
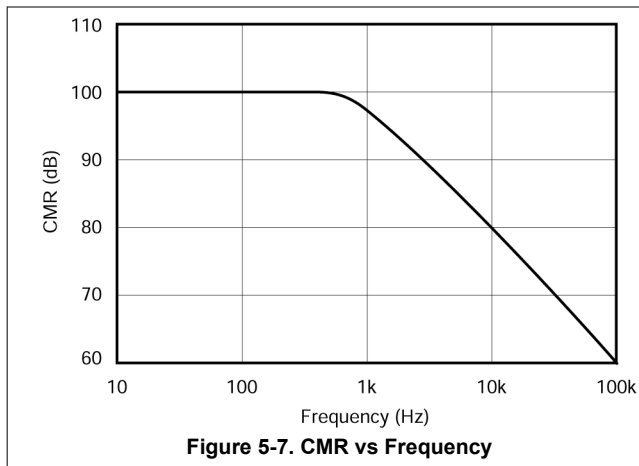
**Figure 5-5. Maximum  $V_{OUT}$  vs  $I_{OUT}$  (Negative Swing)**



**Figure 5-6. Maximum  $V_{OUT}$  vs  $I_{OUT}$  (Positive Swing)**

## 5.5 Typical Characteristics (continued)

at  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$  (unless otherwise noted)





## 6 Detailed Description

### 6.1 Overview

The INA106 consists of a high-precision operational amplifier and four trimmed, on-chip resistors. The device can be configured to make a wide variety of amplifier configurations, including difference, noninverting, and inverting configurations. The integrated, matched resistors provide an advantage over discrete implementation.

Much of the DC performance of op amp circuits depends on the accuracy of the surrounding resistors. The resistors on the INA106 are laid out to be tightly matched. The resistors of each part are matched on-chip and tested for matching accuracy. As a result, the INA106 provides high accuracy for specifications such as gain drift, common-mode rejection ratio, and gain error.

### 6.2 Functional Block Diagram

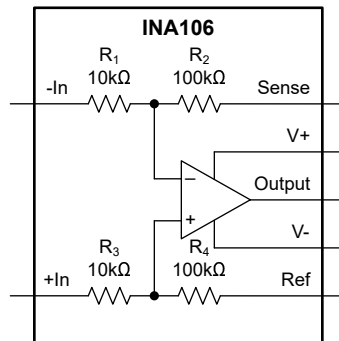


Figure 6-1. Functional Block Diagram

### 6.3 Feature Description

#### 6.3.1 Gain Error and Drift

Gain error in the INA106 is limited by the mismatch of the integrated precision resistors. Gain drift is limited by the slight mismatch of the temperature coefficient of integrated resistors. The integrated resistors are precision-matched with low temperature coefficient resistors to improve overall gain drift compared to the discrete implementation of differences amplifiers build when using external resistors.

### 6.4 Device Functional Modes

The INA106 has one functional mode. The device is specified on a power supply of  $\pm 15\text{V}$  and can operate on a power supply from  $\pm 5\text{V}$  to  $\pm 18\text{V}$  with derated performance. See [Typical Characteristics](#).

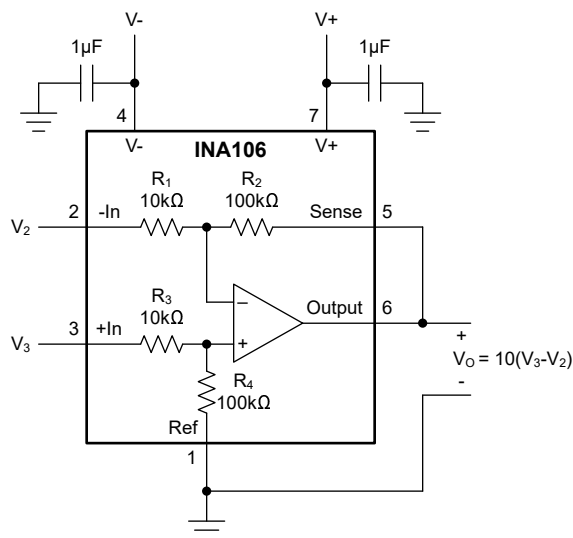
## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

Figure 7-1 shows the basic connections required for operation of the INA106. Place power supply bypass capacitors close to the device pins as shown.

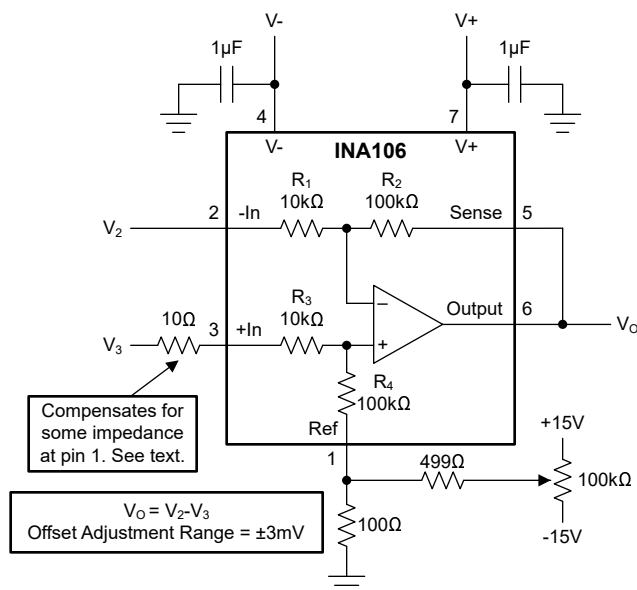


**Figure 7-1. Basic Power Supply and Signal Connections**

The differential input signal is connected to pins 2 and 3 as shown. The source impedance connected to the inputs must be equal for good common-mode rejection. A 5Ω mismatch in source impedance degrades the common-mode rejection of a typical device to approximately 86dB. If the source has a known source impedance mismatch, an additional resistor in series with one input can be used to preserve good common-mode rejection.

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal is summed with the output signal. To maintain good common-mode rejection, keep the source impedance of a signal applied to the Ref terminal less than 10Ω.

Figure 7-2 shows a voltage applied to pin 1 to trim the offset voltage of the INA106. The known 100Ω source impedance of the trim circuit is compensated by the 10Ω resistor in series with pin 3 to maintain good CMR.

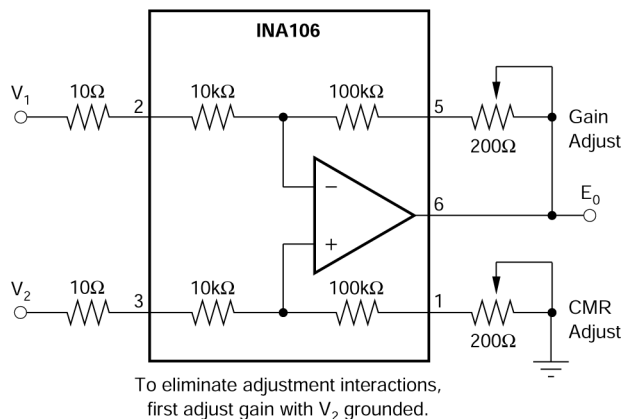


**Figure 7-2. Offset Adjustment**

Referring to [Figure 7-1](#), the CMR depends upon the match of the internal  $R_4/R_3$  ratio to the  $R_1/R_2$  ratio. A CMR of 106dB requires resistor matching of 0.005%. To maintain high CMR over temperature, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

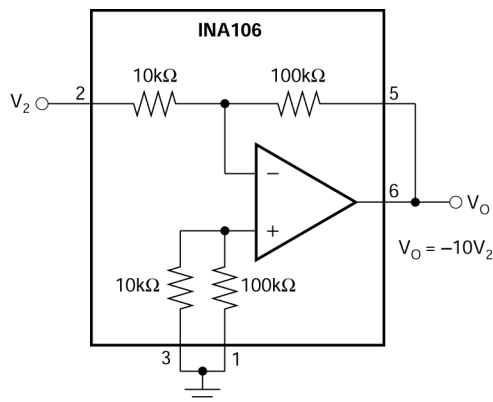
## 7.2 Typical Application

The INA106 can be used in a variety of applications. [Figure 7-3](#) shows one example.



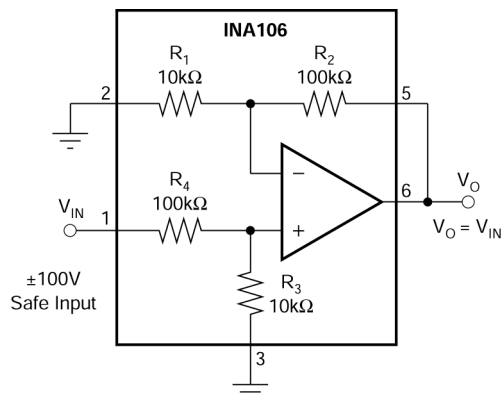
**Figure 7-3. Difference Amplifier With Gain and CMR Adjust**

## 7.3 Additional Applications



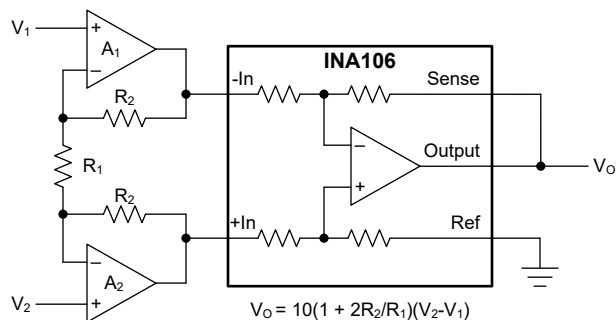
Gain Error = 0.01% maximum  
Nonlinearity = 0.001% maximum  
Gain Drift = 2.ppm/°C

**Figure 7-4. Precision  $G = -10$  Inverting Amplifier**

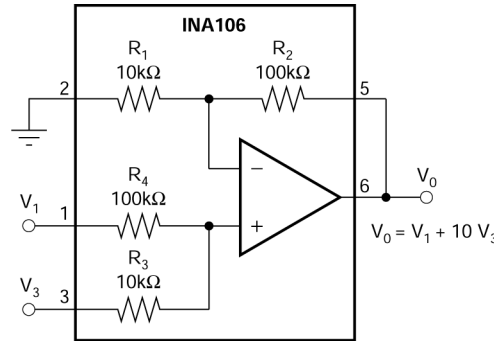


This circuit follows an 11/1 divider with a gain of 11 for an overall gain of unity. With an 11/1 divider, the input signal can exceed 100V without damage.

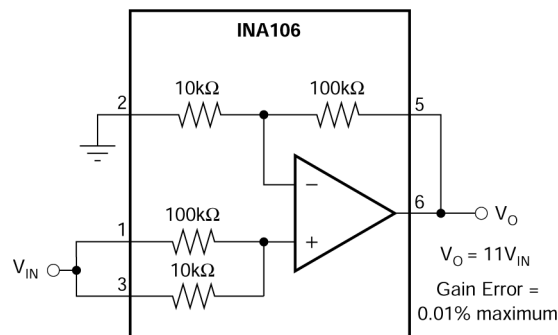
**Figure 7-5. Voltage Follower With Input Protection**



**Figure 7-6. Precision Instrumentation Amplifier**



**Figure 7-7. Precision Summing Amplifier**



**Figure 7-8. Precision G = 11 Buffer**

## 7.4 Power Supply Recommendations

The nominal performance of the INA106 is specified with a supply voltage of  $\pm 15\text{V}$ . The device operates using power supplies from  $\pm 5\text{V}$  to  $\pm 18\text{V}$  with varying performance. Parameters varying across the operating voltage and reference voltage range can be referenced in the [Typical Characteristics](#).

TI highly recommends to add low-ESR ceramic bypass capacitors ( $C_{\text{BYP}}$ ) between each supply pin and ground. Only one  $C_{\text{BYP}}$  is sufficient for single supply operation. Place the  $C_{\text{BYP}}$  as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Route the power supply trace through  $C_{\text{BYP}}$  before reaching the device power supply terminals. For more information, see [Layout Guidelines](#).

## 7.5 Layout

### 7.5.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR,  $0.1\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- To reduce parasitic coupling, route the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is preferred over crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

## 7.5.2 Layout Examples

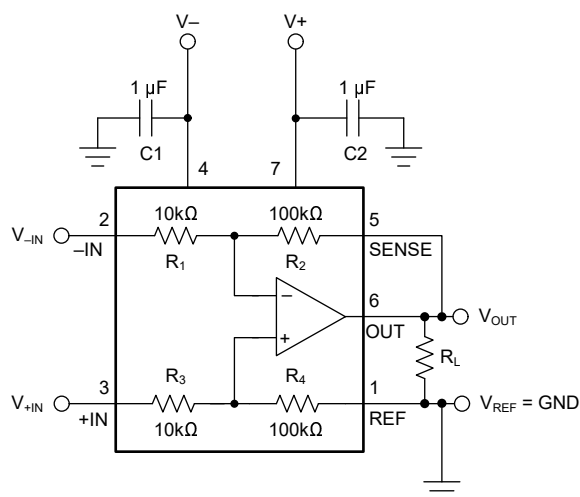


Figure 7-9. Example Schematic

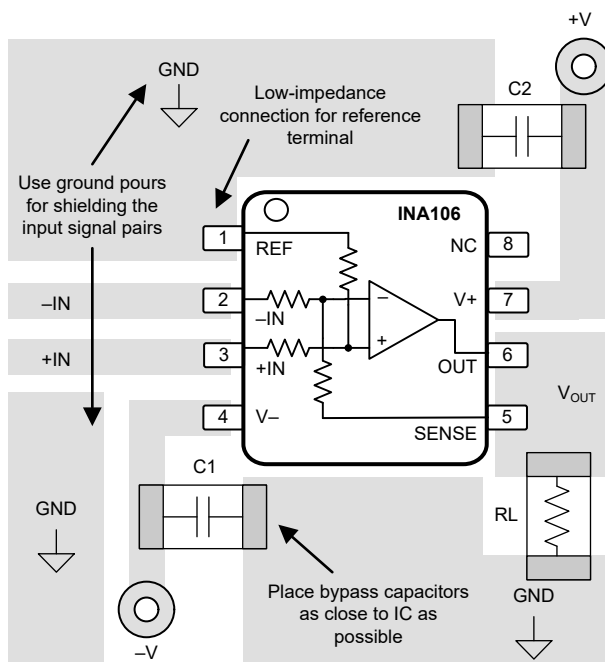


Figure 7-10. Associated PCB Layout for SOIC and PDIP Packages

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Device Support

#### 8.1.1 Development Support

For development support on this product, see the following:

##### 8.1.1.1 PSpice® for TI

**PSpice® for TI** is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

##### 8.1.1.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

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### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

**TI E2E™ support forums** are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.

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### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

### TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2003) to Revision B (March 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added the Pin Configuration and Functions, Specifications, Recommended Operating Conditions, Thermal Information, Detailed Description, Overview, Functional Block Diagram, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Layout Guidelines, Layout Example, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections .....	1
• Changed <i>Precision Gain = 10 Differential Amplifier</i> graphic.....	1
• Added Junction temperature rating in <i>Absolute Maximum</i> table.....	4
• Added more test conditions to the <i>Electrical Characteristics</i> table.....	5
• Changed parameter name in <i>Electrical Characteristics</i> from: <i>Offset voltage vs Temperature</i> to <i>Offset voltage drift</i> .....	5
• Changed parameter name in <i>Electrical Characteristics</i> from: <i>Offset voltage vs Supply</i> to <i>Power-supply rejection ratio</i> .....	5
• Changed parameter name in <i>Electrical Characteristics</i> from: <i>Offset Voltage vs Time</i> to <i>Long-term stability</i> ....	5
• Updated Voltage noise specification in <i>Electrical Characteristics</i> from 1 $\mu$ V <sub>PP</sub> to 1.5 $\mu$ V <sub>PP</sub> .....	5
• Changed output current parameter in <i>Electrical Characteristics</i> from <i>Current Limit</i> to <i>Short-circuit current</i> for sinking and sourcing scenario.....	5
• Updated Full Power Bandwidth in <i>Electrical Characteristics</i> to show bandwidth accounting for the closed loop gain.....	5
• Moved the power supply voltage and temperature ranges from the <i>Electrical Characteristics</i> table to the <i>Absolute Maximum Ratings</i> table.....	5
• Changed the Applications section.....	10
• Changed <a href="#">Figure 7-1</a> .....	10
• Changed <a href="#">Figure 7-2</a> .....	10
• Changed <a href="#">Figure 7-6</a> .....	12

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">INA106KP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA106KP
INA106KP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA106KP
<a href="#">INA106U</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-	INA 106U
<a href="#">INA106U/2K5</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	INA 106U
INA106U/2K5.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 106U

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA106U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA106U/2K5	SOIC	D	8	2500	353.0	353.0	32.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA106KP	P	PDIP	8	50	506	13.97	11230	4.32
INA106KP	P	PDIP	8	50	506	13.97	11230	4.32
INA106KP.A	P	PDIP	8	50	506	13.97	11230	4.32
INA106KP.A	P	PDIP	8	50	506	13.97	11230	4.32

**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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