ESDS452-Q1 Automotive 5.5V Bi-Directional TVS Diode in SOT-23

1 Features

- IEC 61000-4-5 surge protection:
  - 18A (8/20µs)
- IEC 61000-4-2 ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- ISO 10605 (330pF, 330Ω) ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- 5.5V working voltage
- Ultra low leakage current:
  - 1nA (typical)
- I/O capacitance:
  - 3pF (typical)
- Bidirectional polarity to support positive and negative voltage swings
- 2-channel device provides complete ESD/surge protection with single component
- Small, leaded SOT-23 allows low cost automatic optical inspection (AOI)
- AEC-Q101 qualified

2 Applications

- Automotive in-vehicle networks:
  - Hybrid, electric, and powertrain systems
  - HEV/EV battery-management system (BMS)
  - Energy storage systems

3 Description

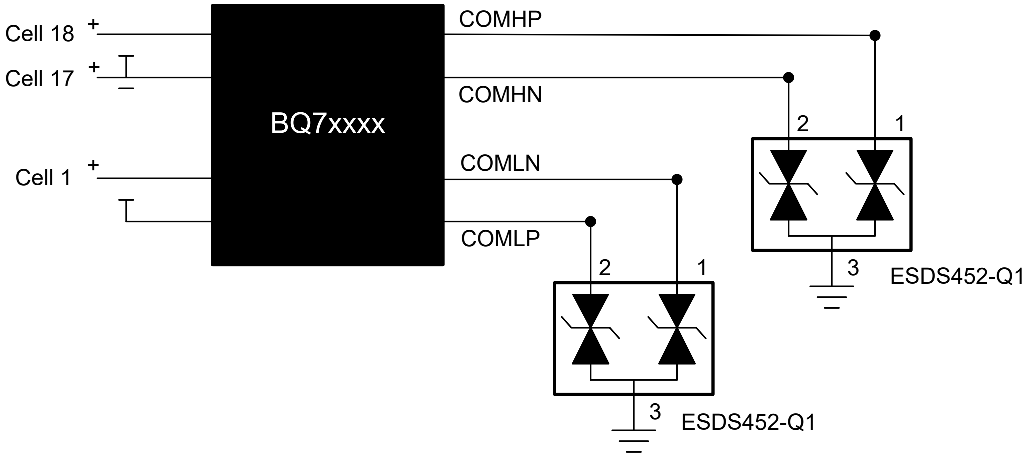
The ESDS452-Q1 is a bidirectional ESD and TVS diode. The ESDS452-Q1 is rated to dissipate ESD strikes beyond the maximum level specified in the IEC 61000-4-2 international standard (±30kV contact, ±30kV air-gap). The device can clamp 8/20µs surges with peak pulse currents up to 18A in accordance with the IEC 61000-4-5 standard. Additionally, the low clamping voltage of the diodes in both the positive and negative directions can help prevent downstream circuitry from being exposed to large voltages and currents during ESD or surge events. This protection is key as automotive systems require a high level of robustness and reliability when controlling safety devices.

The ESDS452-Q1 is available in a small leaded SOT-23 (DBZ) package.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
ESDS452-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm

(1) For more information, see Section 9.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Typical Application for BMS

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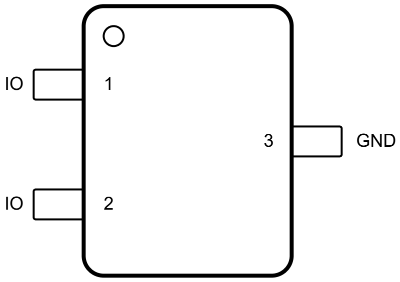
4 Pin Configuration and Functions



Not to scale

Figure 4-1. ESDS452-Q1 DBZ Package, 3-Pin SOT-23 (Top View)

Table 4-1. Pin Functions for ESDS452-Q1

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	Surge and ESD protected IO
GND	3	GND	Ground. Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		MIN	MAX	UNIT
P_{PPM}	IEC 61000-4-5 surge (t_p = 8/20 µs) peak pulse power at 25 °C		172	W
I_{PPM}	IEC 61000-4-5 surge (t_p = 8/20 µs) peak pulse current at 25 °C		18	A
T_A	Operating free-air temperature	–55	150	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings - AEC Specifications

Parameter		Test Conditions	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001(1)	±2500	V
		Charged device model (CDM), per AEC Q101-005(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

5.4 ESD Ratings - ISO Specifications

Parameter		Test Conditions		VALUE	UNIT
$V_{(ESD)}$	ISO 10605 Electrostatic Discharge	C = 150 pF; R = 330 Ω	Contact Discharge, all pins	±30000	V
			Air-gap Discharge, all pins	±30000	
		C = 330 pF; R = 330 Ω	Contact Discharge, all pins	±30000	
			Air-gap Discharge, all pins	±30000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	–5.5		5.5	V
T_A	Operating Free Air Temperature	–55		150	°C

5.6 Thermal Information

THERMAL METRIC[1]		ESDS452-Q1	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	309.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	162.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	149.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	41.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	147.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.7 Electrical Characteristics

At T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 50nA	-5.5		5.5	V
I_{LEAK}	Leakage current at V_{RWM}	VIO = ±5.5 V, I/O to GND and GND to I/O		1	50	nA
V_{BR}	Breakdown voltage, I/O to GND (1)	I_{IO} = ±1mA	7	8	9	V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20µs (2)	I_{PP} = ±1A, I/O to GND		7.5	10	V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20µs (2)	I_{PP} = ±15A, I/O to GND		11.5	14	V
V_{CLAMP}	TLP clamping voltage, t_p = 100ns (3)	I_{PP} = ±16A, I/O to GND		9.6		V
R_{DYN}	Dynamic resistance (4)	I/O to GND		0.29		Ω
		GND to I/O		0.29		
C_{LINE}	Line capacitance, IO to GND	V_{IO} = 0 V, f = 1MHz		3	5	pF

(1) V_{BR} is defined as the voltage when ±1mA is applied in the positive or negative direction respectively.
(2) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5
(3) Non-repetitive square wave current pulse, Transmission Line Pulse (TLP); ANSI / ESD STM5.5.1-2008
(4) 8/20µs (IEC 61000-4-5) dynamic resistance

5.8 Typical Characteristics

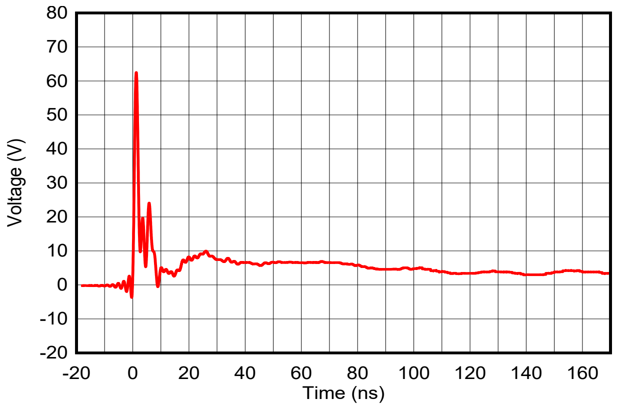


Figure 5-1. +8kV IEC 61000-4-2 Clamping Voltage Waveform

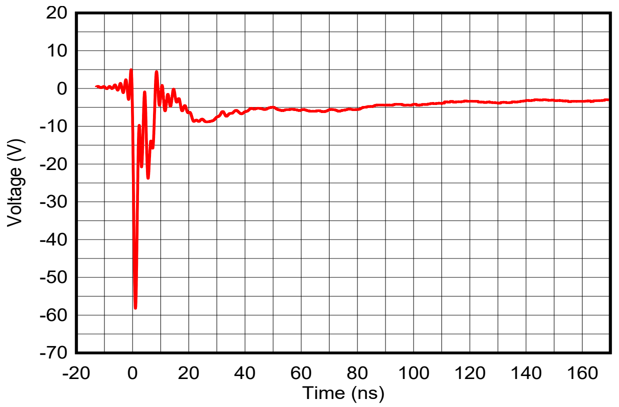


Figure 5-2. -8kV IEC 61000-4-2 Clamping Voltage Waveform

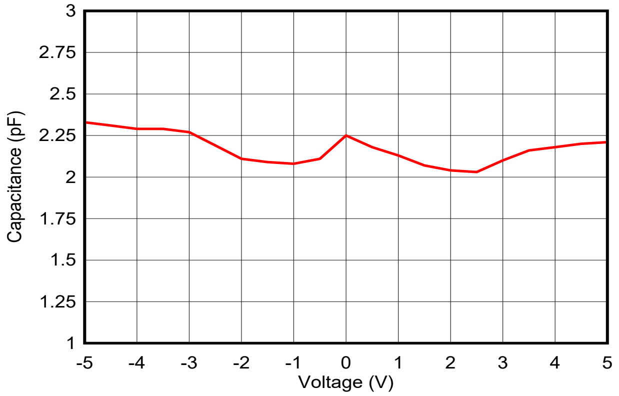


Figure 5-3. Capacitance vs. Bias Voltage

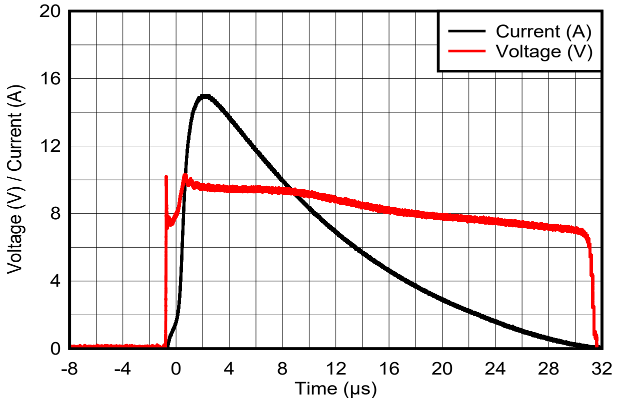


Figure 5-4. 8/20µs Surge Response

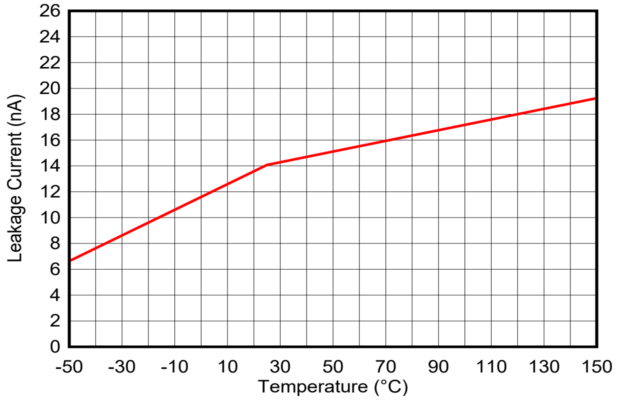


Figure 5-5. Leakage Current vs. Temperature

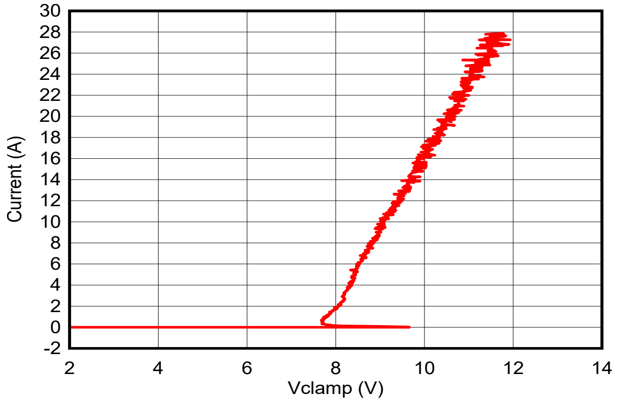


Figure 5-6. Positive TLP Curve

5.8 Typical Characteristics (continued)

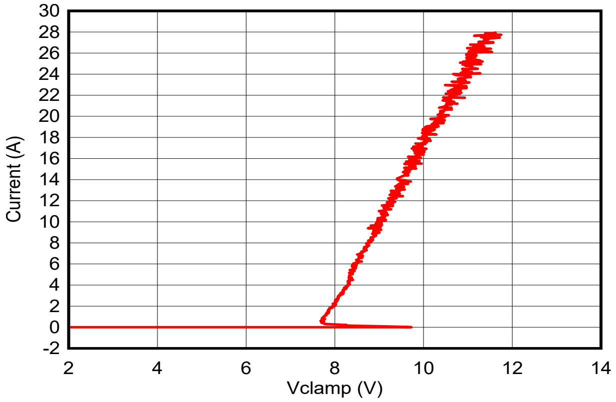


Figure 5-7. Negative TLP Curve

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESDS452-Q1 is a diode type TVS that provides a path to ground for dissipating transient voltage spikes (such as ESD or surge) on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Packaging and Layout Guide*
- Texas Instruments,*TI's IEC 61000-4-x Testing application note*
- Texas Instruments,*ESD Layout Guide user's guide*
- Texas Instruments,*ESD Protection Diodes EVM user's guide*
- Texas Instruments,*Generic ESD Evaluation Module user's guide*
- Texas Instruments,*Reading and Understanding an ESD Protection Data Sheet user's guide*

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

DATE	REVISION	NOTES
April 2024	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESDS452DBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	3BM8
ESDS452DBZRQ1.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	3BM8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

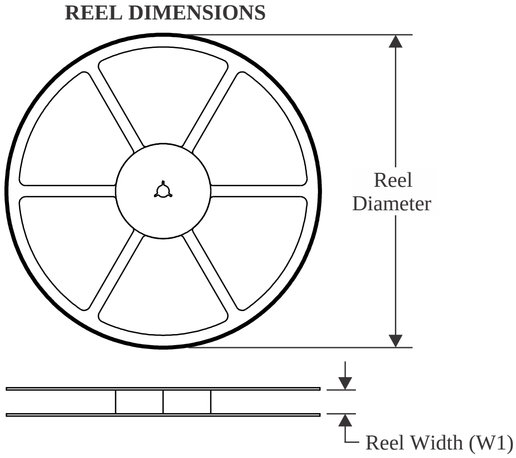
OTHER QUALIFIED VERSIONS OF ESDS452-Q1 :

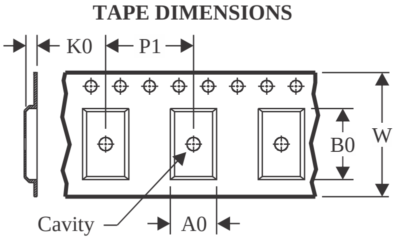
- Catalog : ESDS452

NOTE: Qualified Version Definitions:

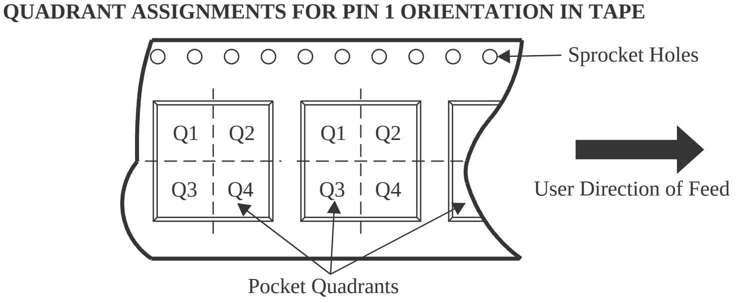
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





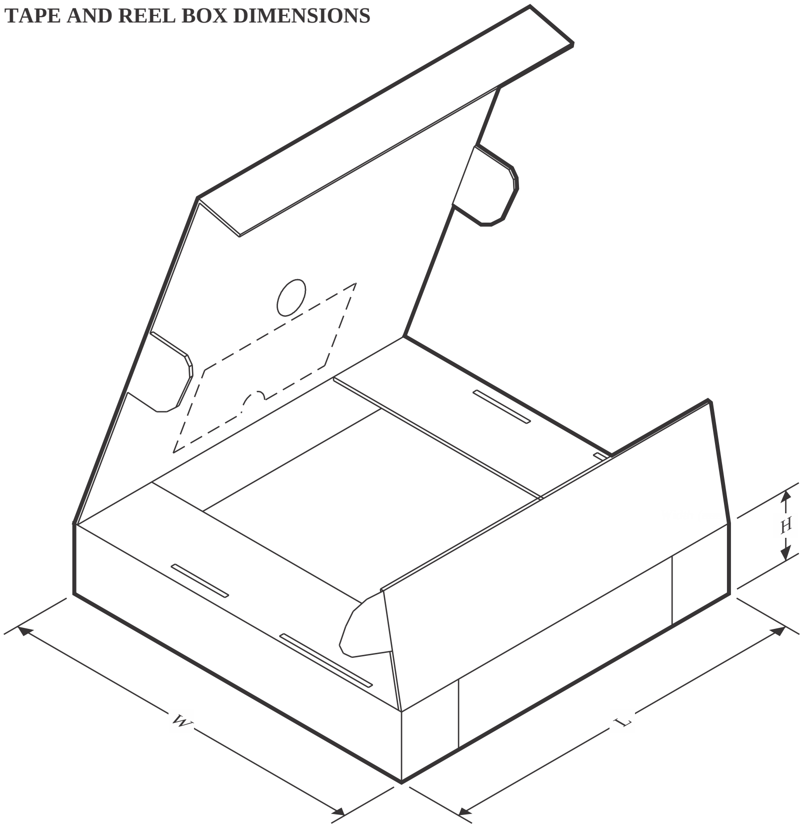
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESDS452DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

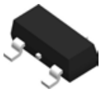
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESDS452DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

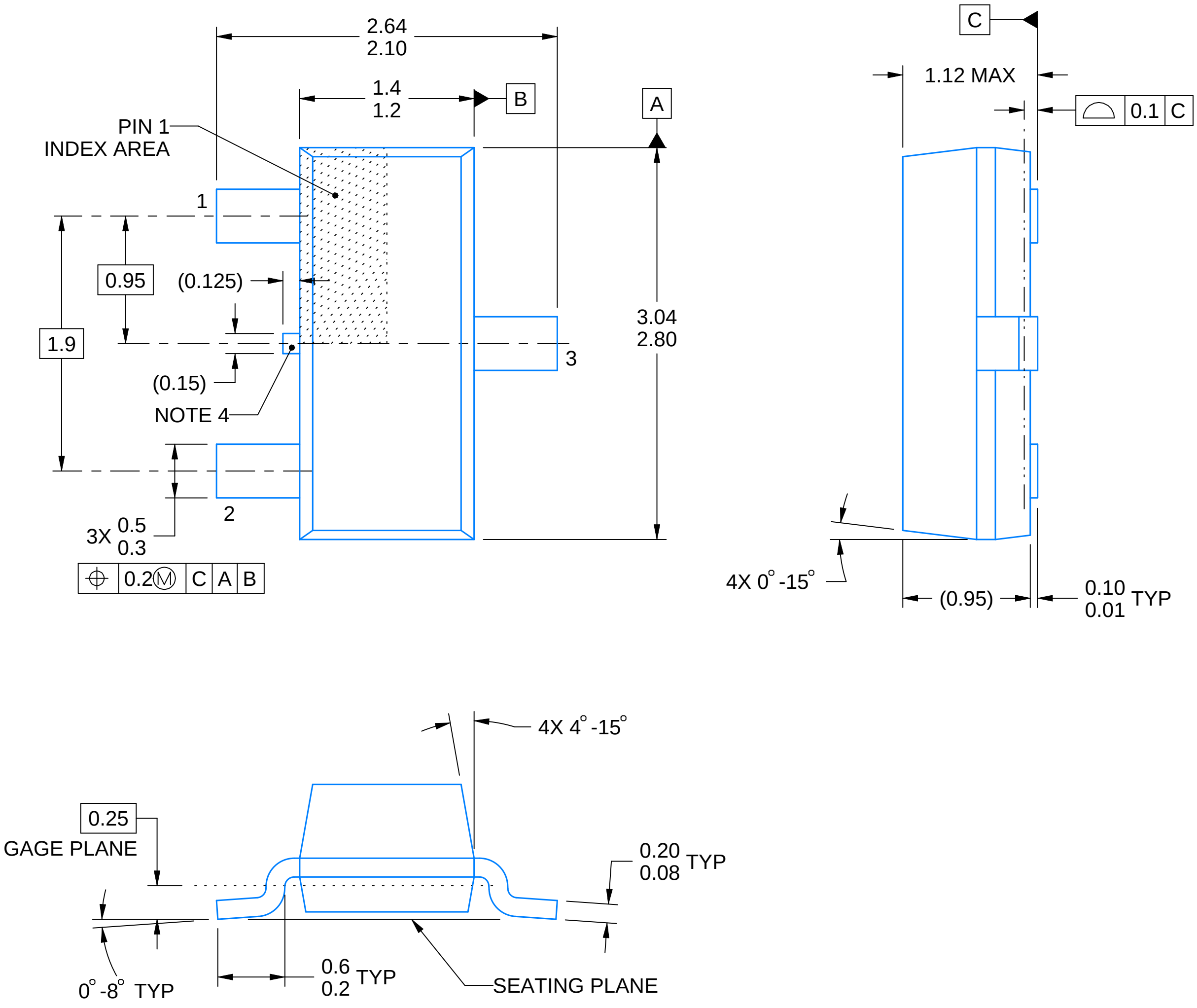
PACKAGE OUTLINE



DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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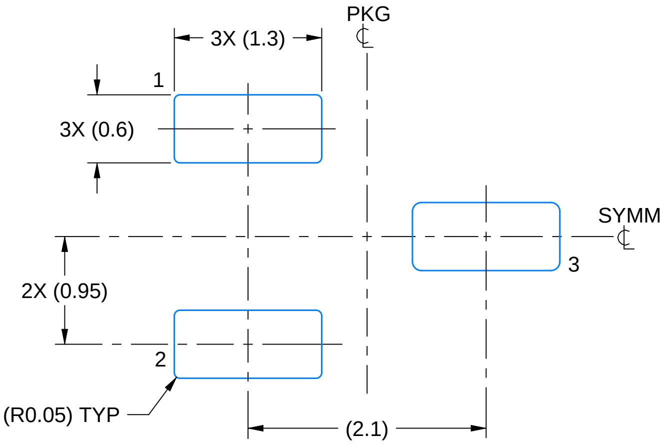
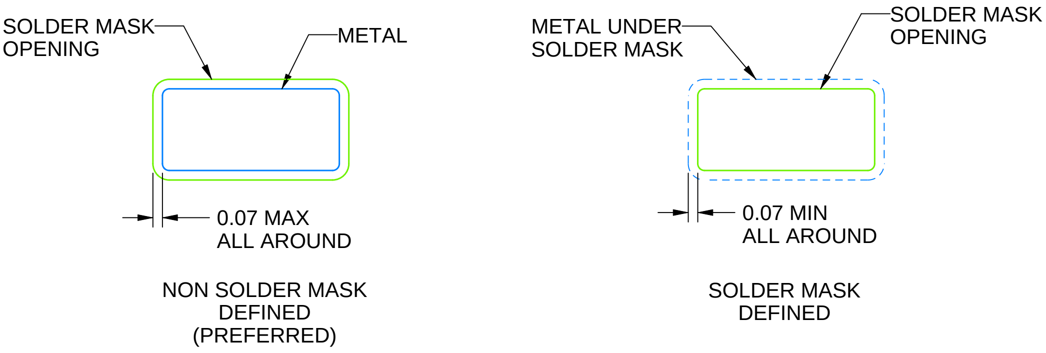
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



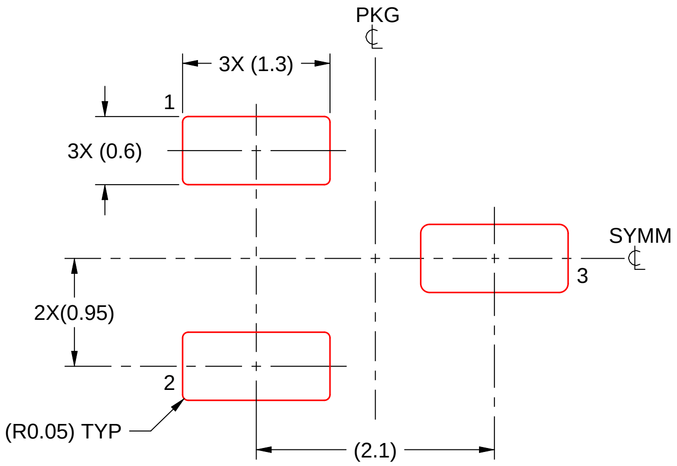
LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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