ESD8x2 2-Channel, 36V ESD Protection Diode

1 Features

- Working voltage 36V
- Low leakage current 50nA (maximum)
- IEC 61000-4-2 ESD protection:
  - ±25kV contact and ±25kV air (ESD852)
  - ±18kV contact and ±18kV air (ESD862)
- Robust surge protection:
  - IEC 61000-4-5 (8/20µs): 4.3A (ESD852)
  - IEC 61000-4-5 (8/20µs): 3.1A (ESD862)
- Bidirectional ESD protection
- I/O capacitance = 2.8pF typical (ESD852)
- I/O capacitance = 2.6pF typical (ESD862)
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- Factory automation
- Communication equipments
- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- Industrial communications:
  - CAN / CAN-FD

3 Description

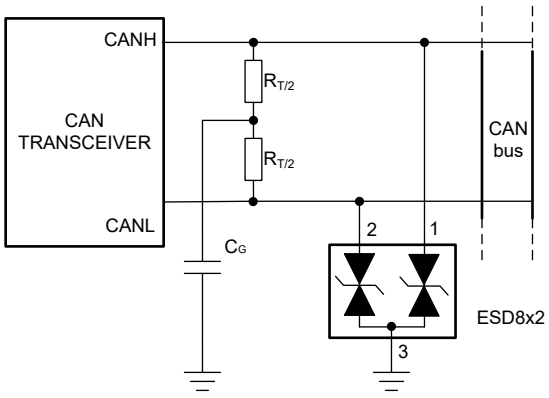
The ESD8x2 devices are bidirectional ESD protection diodes for USB power delivery (USB-PD) and industrial interfaces. The devices are rated to dissipate ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 standard (±25kV contact and airgap, or ±18kV contact and airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The I_{PP} = 4.3A (8/20µs surge waveform) capability of the ESD852 makes it an excellent choice for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 2.8pF or 2.6pF line capacitance of the ESD8x2 are an excellent choice for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

Package Information

PART NUMBER	CHANNEL	PACKAGE(1)
ESD852	2 Channels	DBZ (SOT-23, 3) DCK (SOT-SC70, 3)
ESD862		

(1) For more information, see Section 9.



ESD8x2 Typical Application

Table of Contents

4 Pin Configuration and Functions

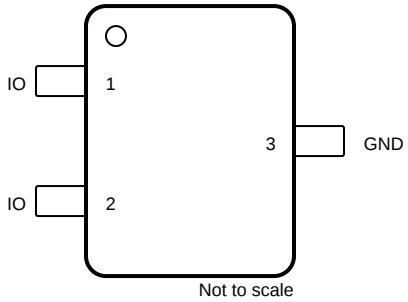


Figure 4-1. DBZ or DCK Package, SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		DEVICE	MIN	MAX	UNIT
Ppp	IEC 61000-4-5 Power (t_p – 8/20µs) at 25°C	ESD852		233	W
	IEC 61000-4-5 Power (t_p – 8/20µs) at 25°C	ESD862		175	W
I_{pp}	IEC 61000-4-5 current (t_p – 8/20µs) at 25°C	ESD852		4.3	A
	IEC 61000-4-5 current (t_p – 8/20µs) at 25°C	ESD862		3.1	A
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	°C
T_{stg}	Storage temperature		-65	155	°C

(1) Operation outside the *Section 5.1* may cause permanent device damage. *Section 5.1* do not imply functional operation of the device at these or any other conditions beyond those listed under *Section 5.4*. If used outside the *Section 5.4* but within the *Section 5.1*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	± 1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD852	±25000	V
			ESD862	±18000	V
		IEC 61000-4-2 Air Discharge, all pins	ESD852	±25000	V
			ESD862	±18000	V

5.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-36		36	V
T_A	Operating free-air temperature	-55		150	°C

5.5 Thermal Information

THERMAL METRIC[1]		ESD852		ESD862		UNIT
		DBZ (SOT-23)	DCK (SC-70)	DBZ (SOT-23)	DCK (SC-70)	
		3 PINS	3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	293.4	258.1	313.5	265.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.9	134.8	162.8	142.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.0	75.1	151.8	82.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.9	31.1	43.5	38.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	132.0	74.3	150.8	81.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			–36		36	V
V_{BRF}	Forward breakdown voltage[1] [2]	I_{IO} = 10mA, IO to GND		37.8	40	44.2	V
V_{BRR}	Reverse breakdown voltage [1] [2]	I_{IO} = -10mA, IO to GND		-44.2	-40	-37.8	V
V_{CLAMP}	Clamping voltage[3]	I_{PP} = 1A, t_p = 8/20 µs, IO to GND	ESD852		43	50	V
		I_{PP} = 4. A, t_p = 8/20µs, from IO to GND			61	66	V
		I_{PP} = 1A, t_p = 8/20µs, from IO to GND	ESD862		47		V
		I_{PP} = 3.1A, t_p = 8/20µs, from IO to GND			61		V
V_{CLAMP}	Clamping voltage[4]	I_{PP} = 16A, TLP, IO to GND or GND to IO	ESD852		63		V
			ESD862		64		V
I_{LEAK}	Leakage current	V_{IO} = ±36V, IO to GND			5	50	nA
R_{DYN}	Dynamic resistance[4]	IO to GND and GND to IO	ESD852		0.49		Ω
			ESD862		0.49		Ω
C_L	Line capacitance[1]	V_{IO} = 0V, f = 1MHz, V_{pp} = 30mV	ESD852		2.8	3.5	pF
			ESD862		2.6	2.9	pF

(1) Measured from IO to GND on each channel.
(2) V_{BRF} and V_{BRR} are defined as the voltage when ± 10mA is applied in the positive or negative direction respectively.
(3) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.
(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

5.7 Typical Characteristics – ESD852

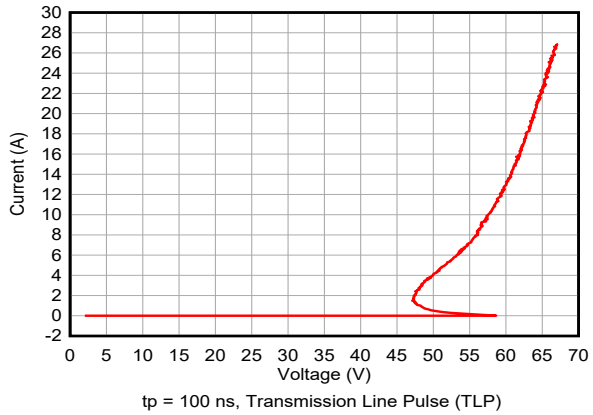


Figure 5-1. Positive TLP Curve

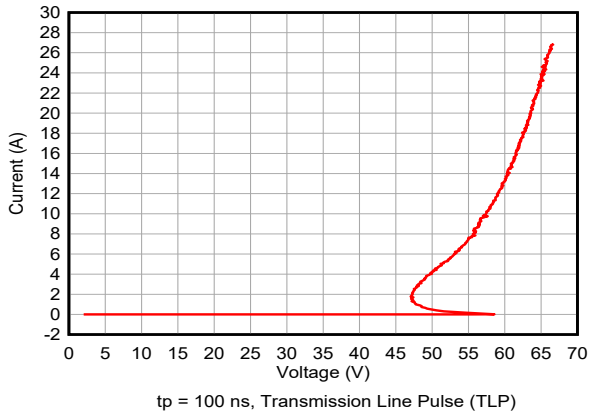


Figure 5-2. Negative TLP Curve

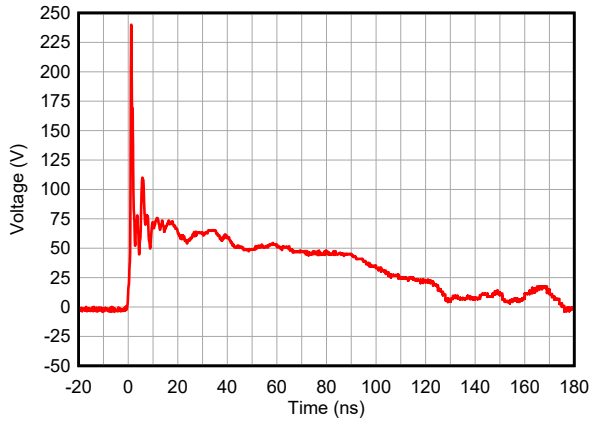


Figure 5-3. +8kV Clamped IEC Waveform

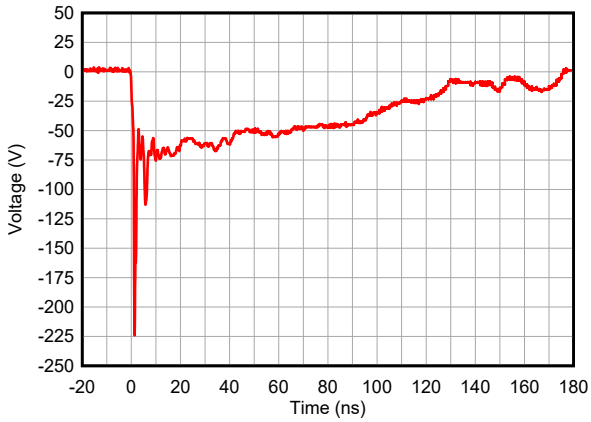


Figure 5-4. −8kV Clamped IEC Waveform

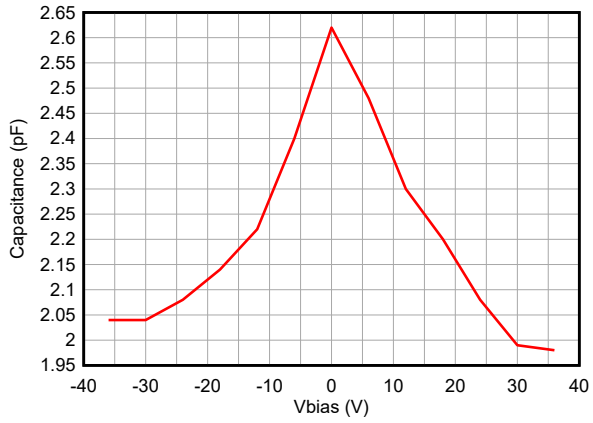


Figure 5-5. Capacitance vs. Bias Voltage

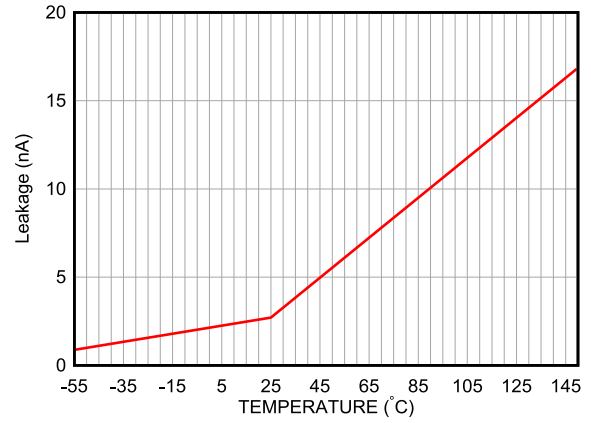


Figure 5-6. Leakage vs. Temperature

5.8 Typical Characteristics – ESD862

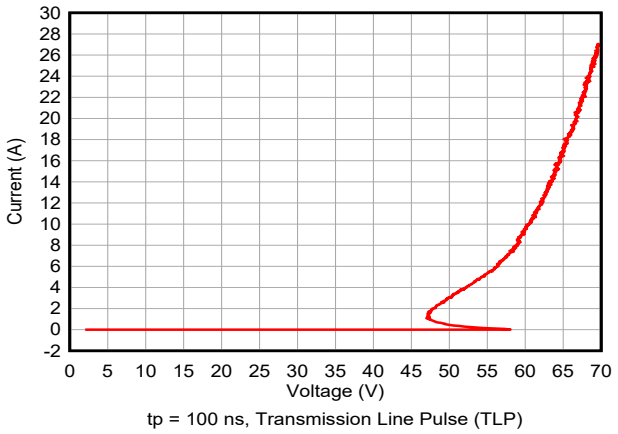


Figure 5-7. Positive TLP Curve

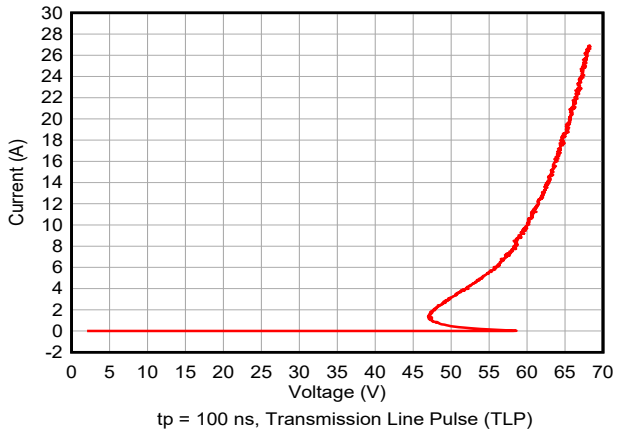


Figure 5-8. Negative TLP Curve

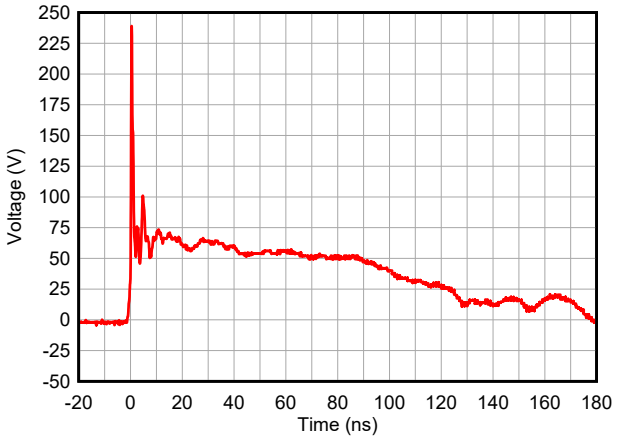


Figure 5-9. +8kV Clamped IEC Waveform

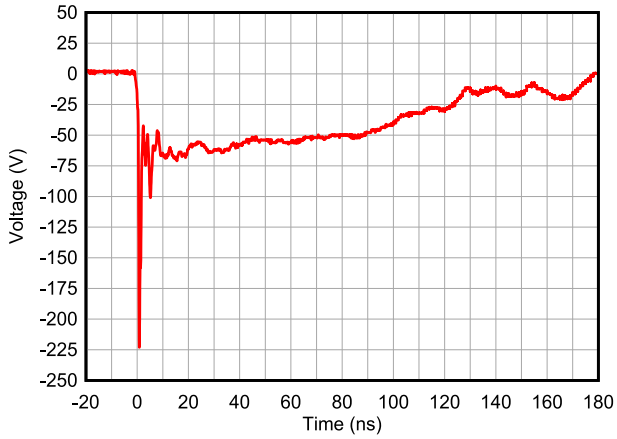


Figure 5-10. -8kV Clamped IEC Waveform

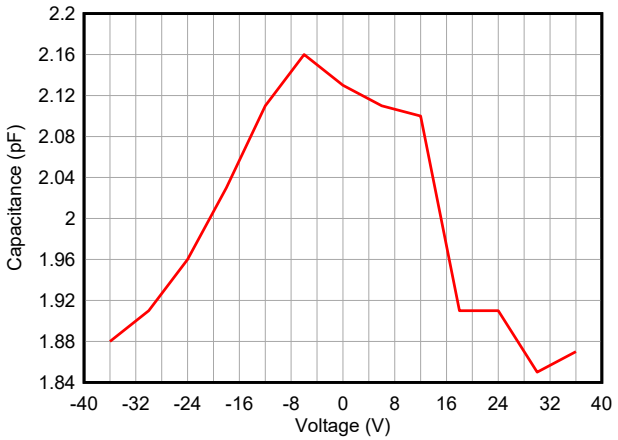


Figure 5-11. Capacitance vs. Bias Voltage

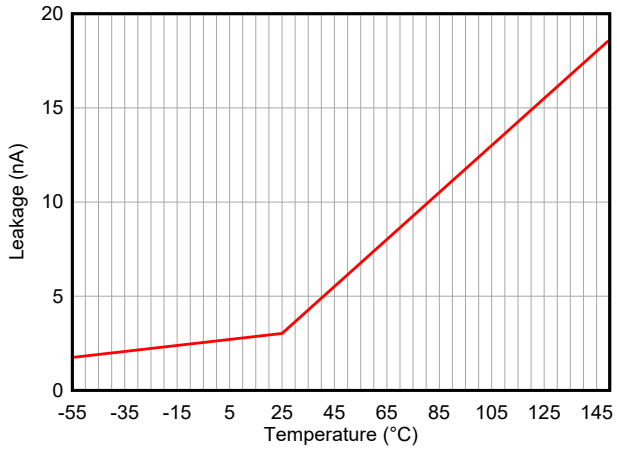


Figure 5-12. Leakage vs. Temperature

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD8x2 devices are ESD diodes which provide a path to ground for dissipating transient voltage spikes, such as ESD or surge on signal lines and power lines. Connect the devices in parallel to the down stream circuitry they are protecting. As the current from the transient passes through the ESD device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered ESD device holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD and Surge Protection for USB Interfaces* application note
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2023) to Revision A (June 2025)	Page
• Added DCK package	1

DATE	REVISION	NOTES
November 2023	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD852DBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z38
ESD852DBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z38
ESD862DBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z78
ESD862DBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z78

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

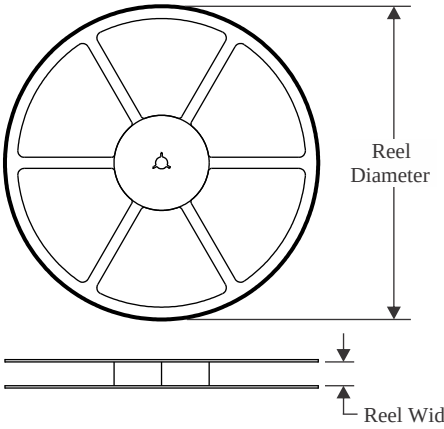
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

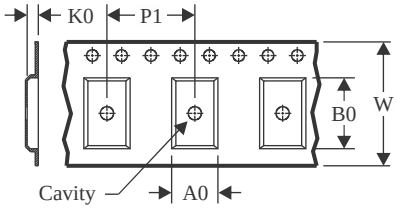
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

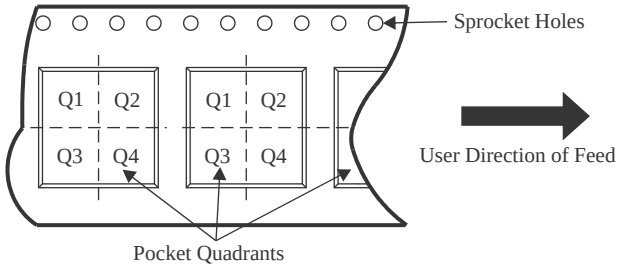


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

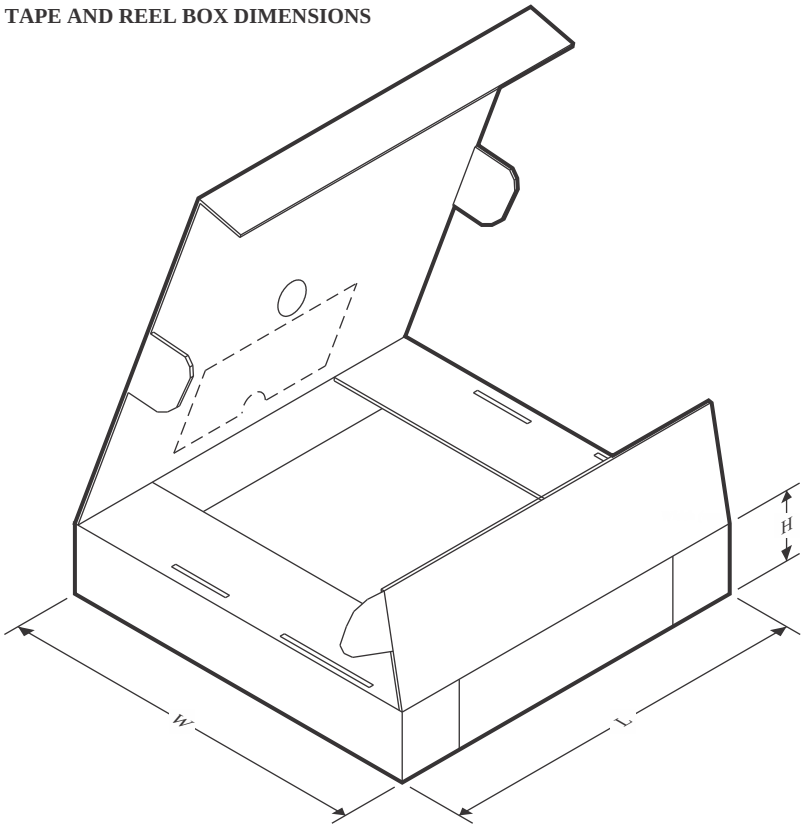
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD852DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD862DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

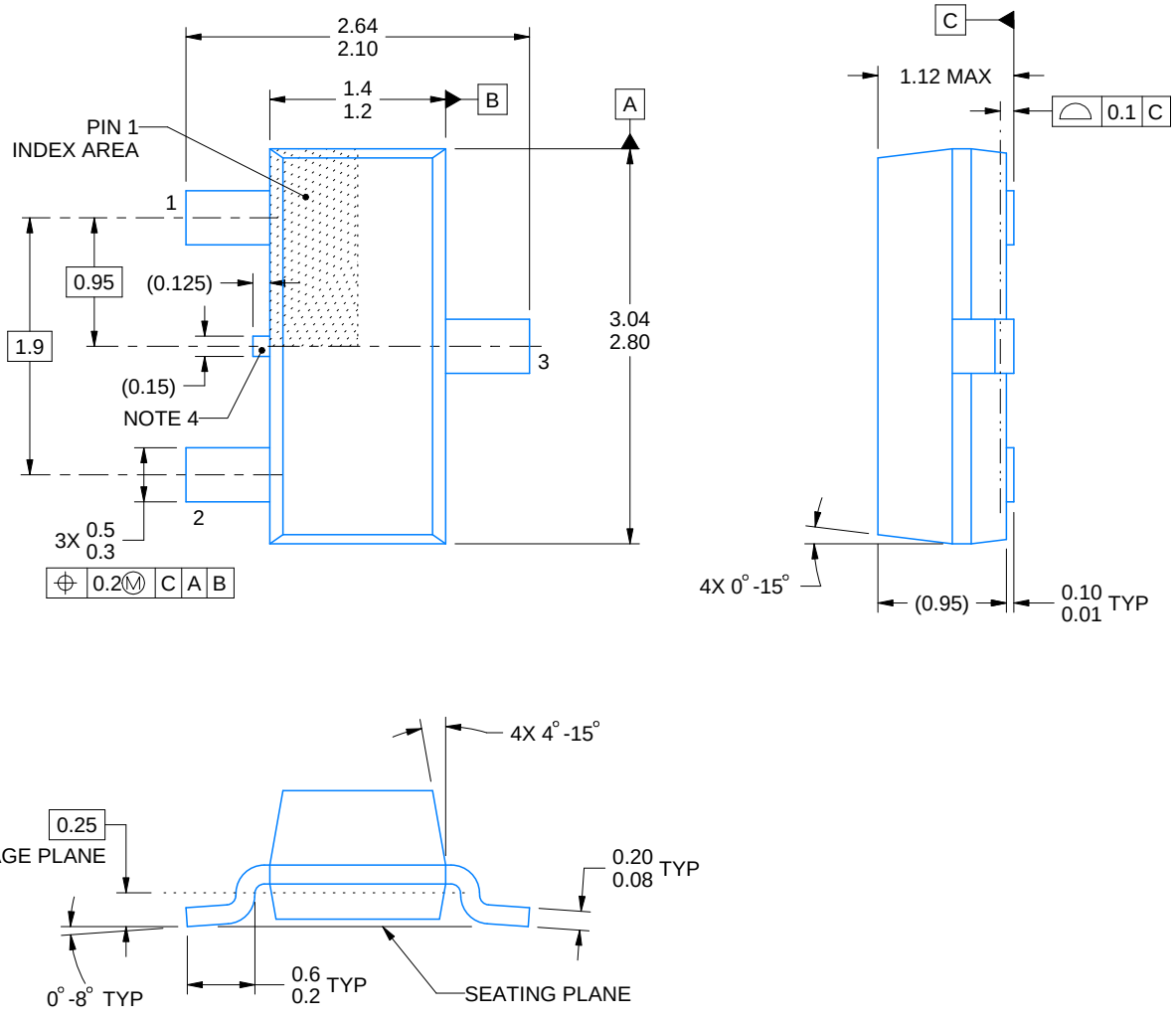
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD852DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD862DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

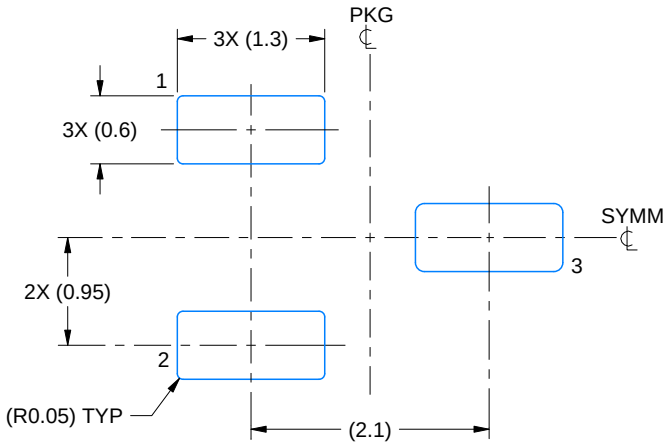
SMALL OUTLINE TRANSISTOR



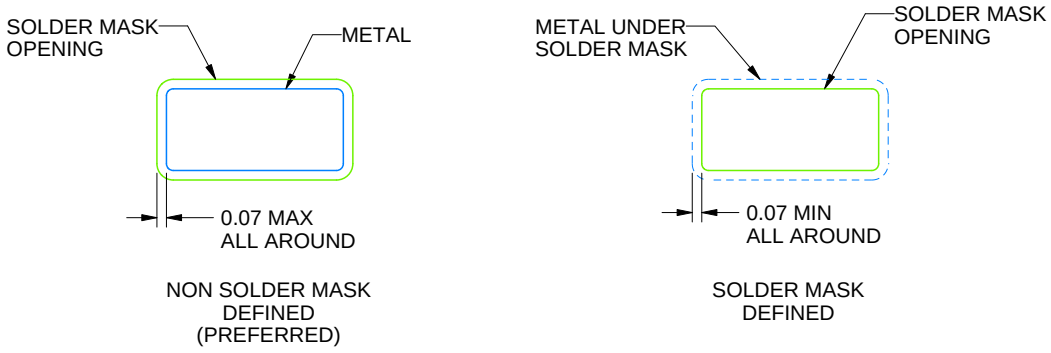
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

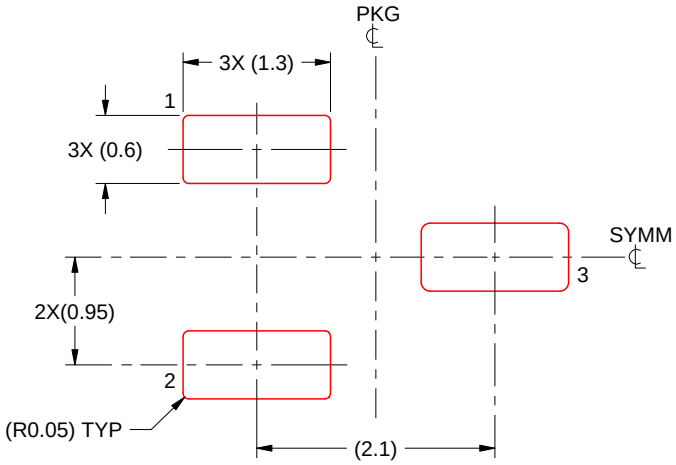


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265