ESD851-Q1 36V Automotive Bidirectional ESD Protection Diode in SOD-323

1 Features

- ISO 10605 (330pF, 330Ω) ESD protection:
  - ±27kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-5 surge protection:
  - 6.5A (8/20µs)
  - Clamping voltage: 71V at 6.5A (8/20µs)
- IO Capacitance: 4.3pF (typical)
- Ultra low leakage current: 10nA (maximum)
- ESD clamping voltage: 56V at 16A TLP
- Industrial temperature range: -55°C to +150°C
- AEC-Q101 qualified
- Industry standard SOD-323 leaded package (2.65mm × 1.3mm)

2 Applications

- I/O Protection
- Body Electronics & Lighting
- Hybrid, Electric, & Powertrain Systems

3 Description

The ESD851-Q1 is a bidirectional ESD protection diode designed for clamping harmful transients such as ESD and surge. The ESD851-Q1 is rated to dissipate ESD strikes up to ±30kV (contact and air gap discharge), which exceeds the maximum level specified in the IEC 61000-4-2 international standard (Level 4). For surges, the device can clamp 8/20µs surges with peak currents up to 6.5A in accordance with the IEC 61000-4-5 standard.

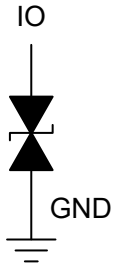
This device also features a 4.3pF (typical) IO capacitance enabling it to protect data lines. The low dynamic resistance and low clamping voltage provides system level protection against transient events.

The ESD851-Q1 is offered in the industry standard, leaded SOD-323 package to enable easy solderability.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD851-Q1	DYF (SOD-323, 2)	2.65mm × 1.3mm

(1) For more information, see Section 8.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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4 Pin Configuration and Functions

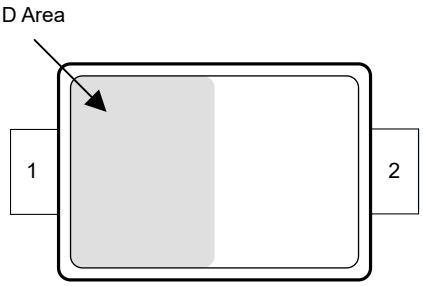

Figure 4-1. DYF Package, 2-Pin SOD-323 (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	IO	I/O	Protected Channel. If used as IO, connect pin 2 to ground
2	IO	I/O	Protected Channel. If used as IO, connect pin 1 to ground

(1) I = input, O = output. GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

Parameter		MIN	MAX	UNIT
P_{PP} (2) (3)	IEC 61000-4-5 (t_p 8/20µs) Peak Pulse Power at 25°C		400	W
I_{PP}	IEC 61000-4-5 (t_p 8/20µs) Peak Pulse Current at 25°C		6.5	A
T_A	Ambient Operating Temperature	-55	150	°C
T_{stg}	Storage Temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25℃

5.2 ESD Ratings - AEC Specifications

Parameter		Test Conditions	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001(1)	±2500	V
		Charged device model (CDM), per AEC Q101-005(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 ESD Ratings - ISO Specifications

Parameter			Test Conditions	VALUE	UNIT
$V_{(ESD)}$	ISO 10605 Electrostatic Discharge	Contact discharge, all pins	C = 150 pF; R = 330 Ω	±30000	V
			C = 330 pF; R = 330 Ω	±27000	
		Air-gap discharge, all pins	C = 150 pF; R = 330 Ω	±30000	
			C = 330 pF; R = 330 Ω	±30000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input pin voltage	-36		36	V
T_A	Operating Free Air Temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC (1)		ESD851-Q1 DYF (SOD-323) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	686.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	267.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	560.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	91.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	546.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.7 Electrical Characteristics

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <10 nA, across operating temperature range			36	V
V_{BR}	Breakdown voltage	I_{IO} = 10 mA, I/O to GND or GND to I/O	37.8			V
I_{LEAK}	Reverse leakage current	V_{IO} = 36 V, IO to GND or GND to IO		5	10	nA
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 1 A, IO to GND or GND to IO			47	V
		I_{PP} = 5 A, IO to GND or GND to IO			64	V
		I_{PP} = 6.5 A, IO to GND or GND to IO			71	V
	TLP clamping voltage, t_p = 100 ns	I_{PP} = 16 A, IO to GND or GND to IO		56		V
R_{DYN}	Dynamic resistance(3)	IO to GND		0.6		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0 V; f = 1 MHz, IO to GND		4.3	6	pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.8 Typical Characteristics

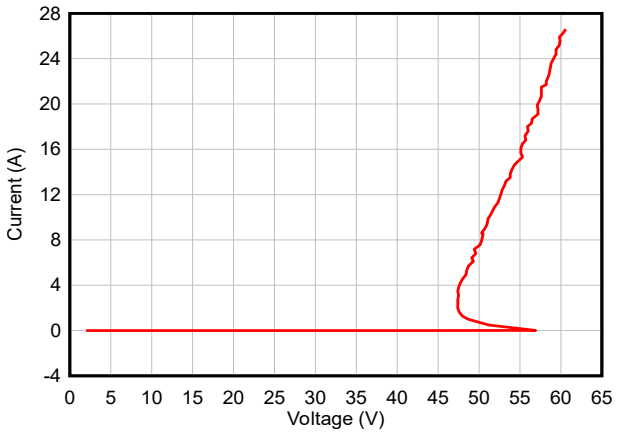

Figure 5-1. Positive TLP Curve

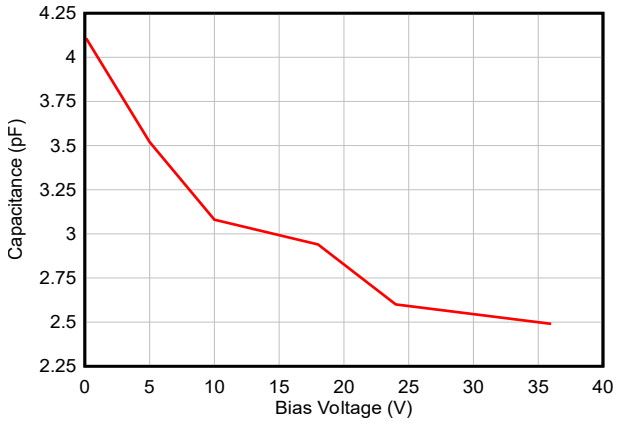

Figure 5-2. Capacitance vs Bias Voltage

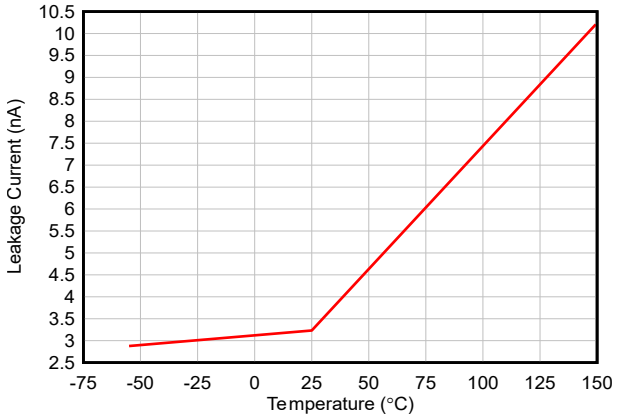

Figure 5-3. Leakage Current vs Temperature

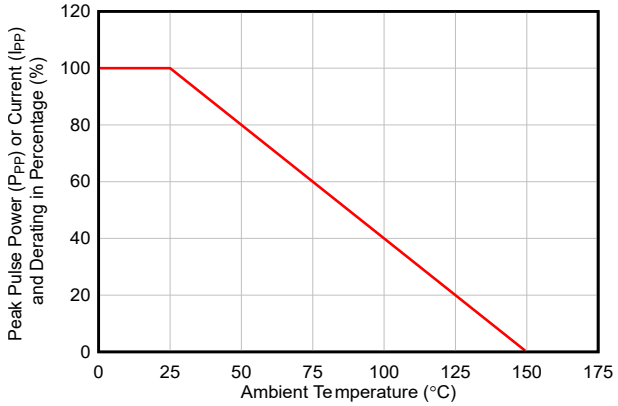

Figure 5-4. Peak Pulse Power Derating Curve

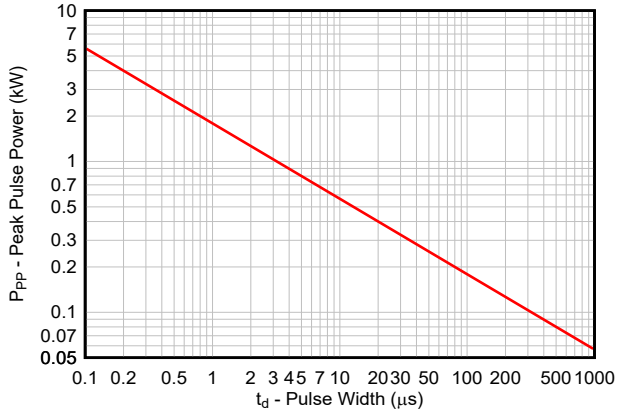

Figure 5-5. Pulse Power Rating Curve

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.4 Trademarks

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6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

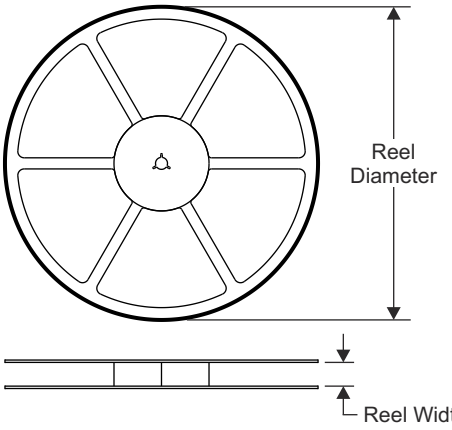
DATE	REVISION	NOTES
December 2024	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

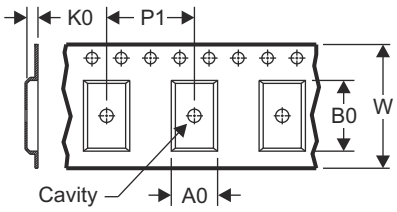
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Tape and Reel Information

REEL DIMENSIONS

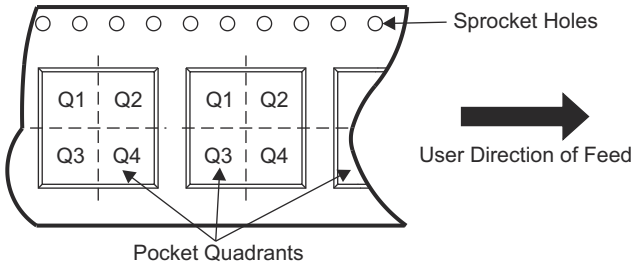


TAPE DIMENSIONS



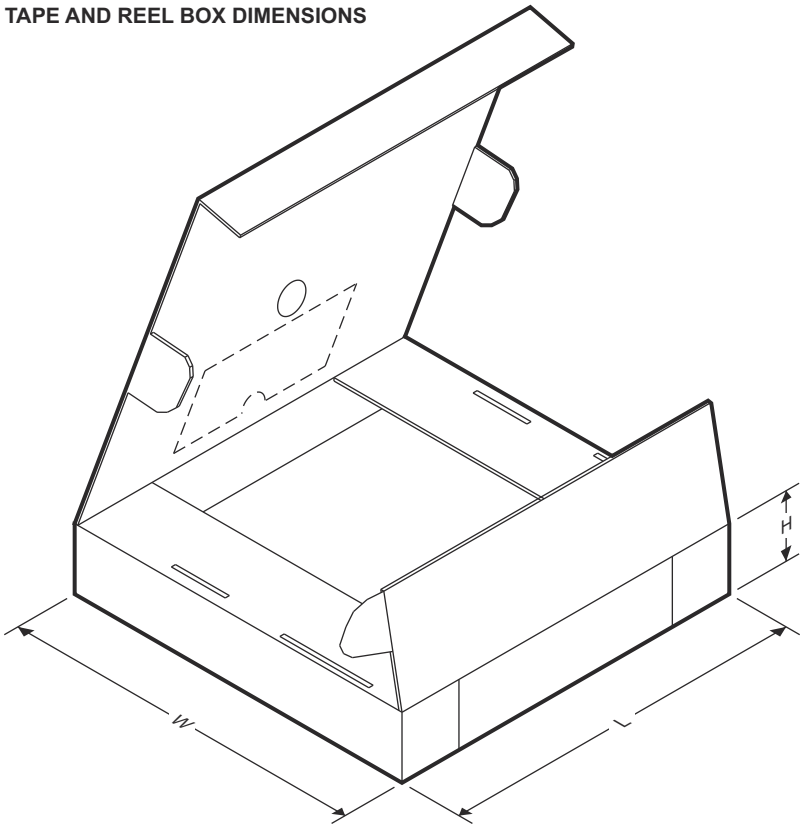
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD851	LARGE T&R	DYF	2	3000	178.000	9.500	1.480	3.300	1.250	4.000	8.000	Q1

TAPE AND REEL BOX DIMENSIONS



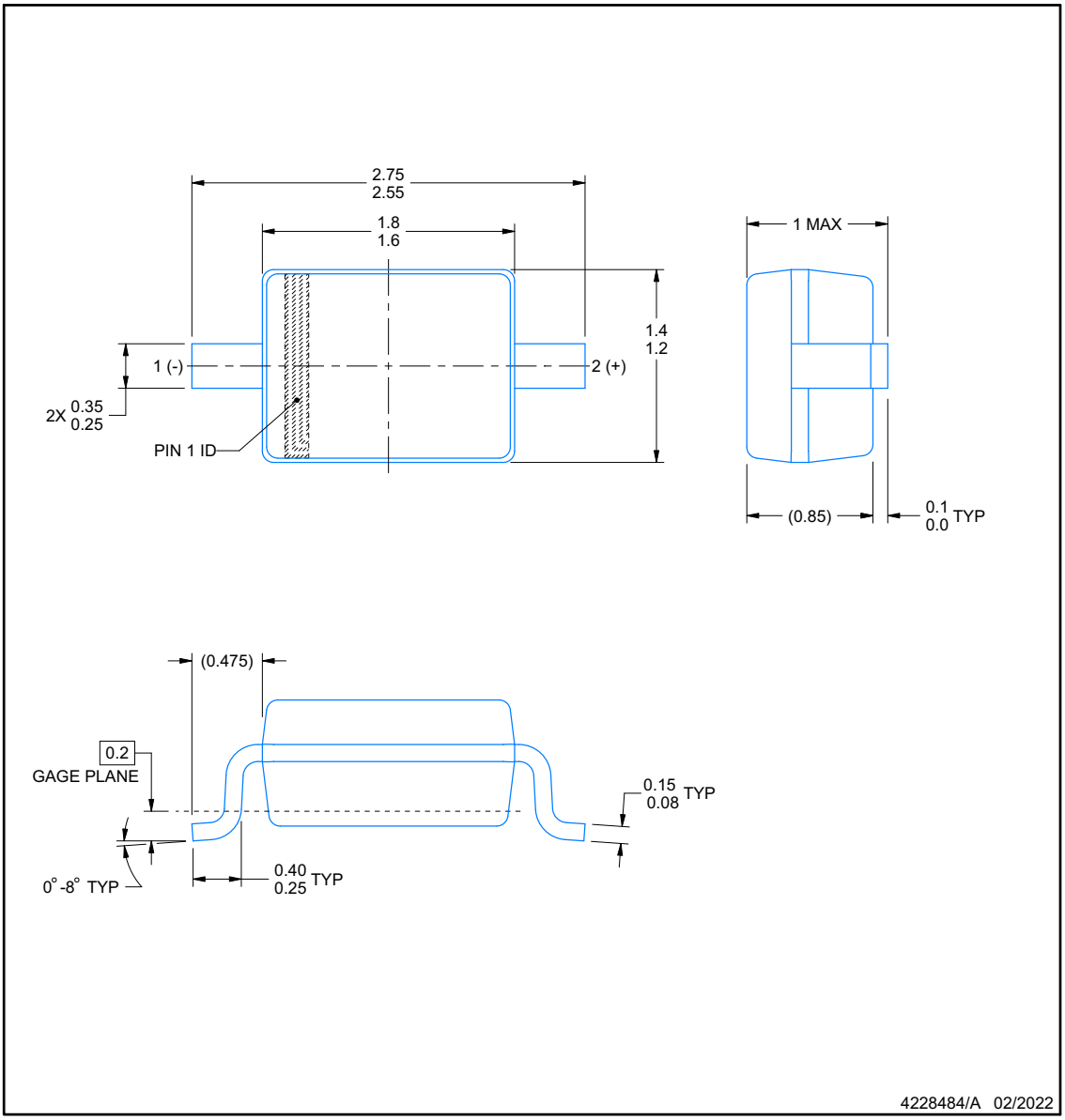
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD851	LARGE T&R	DYF	2	3000	210.000	200.000	42.000

8.2 Mechanical Data

PACKAGE OUTLINE

DYF0002A — **SOT(SOD-323) - 1 mm max height**

SMALL OUTLINE TRANSISTOR



NOTES:

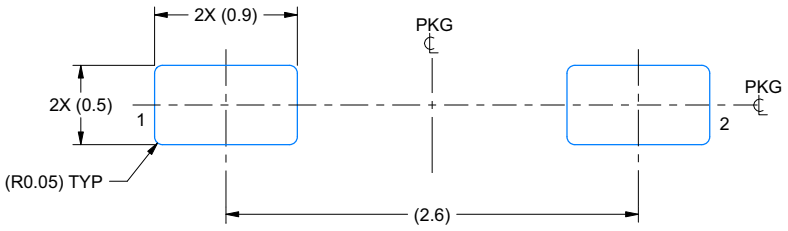
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

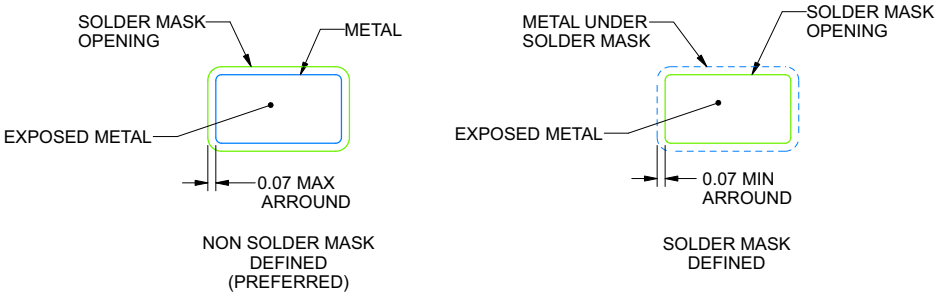
DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4228484/A 02/2022

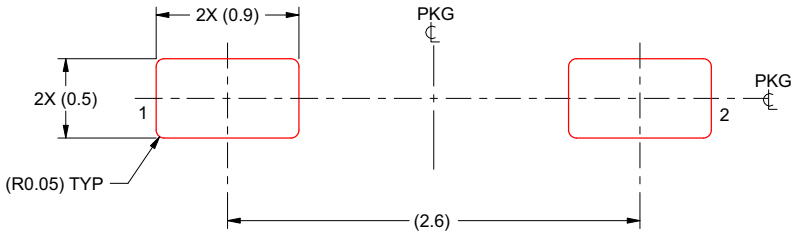
NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYF0002A — **SOT(SOD-323) - 1 mm max height**

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4228484/A 02/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD851DYFRQ1	Active	Production	SOT (DYF) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3H8F
ESD851DYFRQ1.B	Active	Production	SOT (DYF) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3H8F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ESD851-Q1 :

- Catalog : ESD851

NOTE: Qualified Version Definitions:

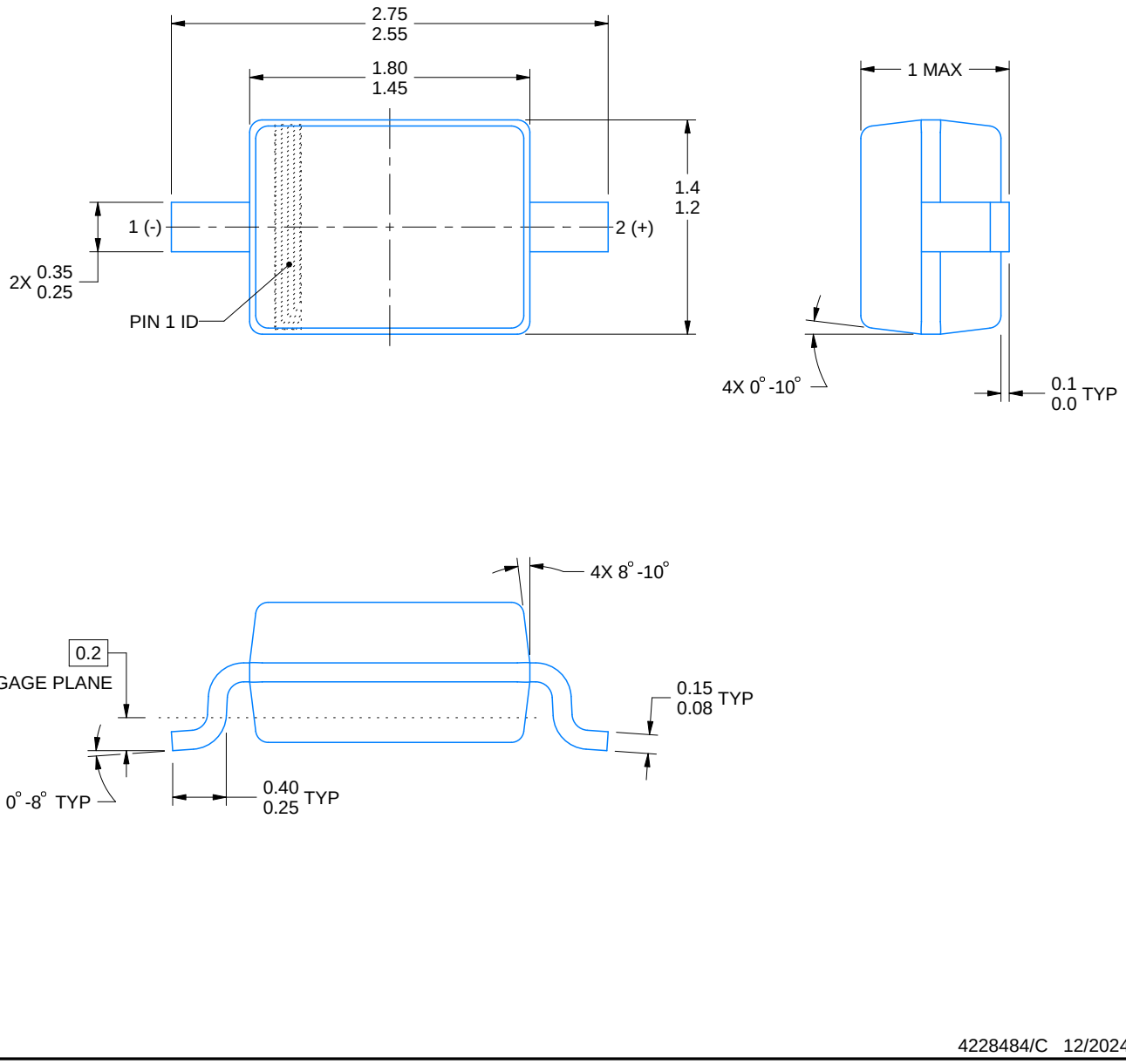
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



4228484/C 12/2024

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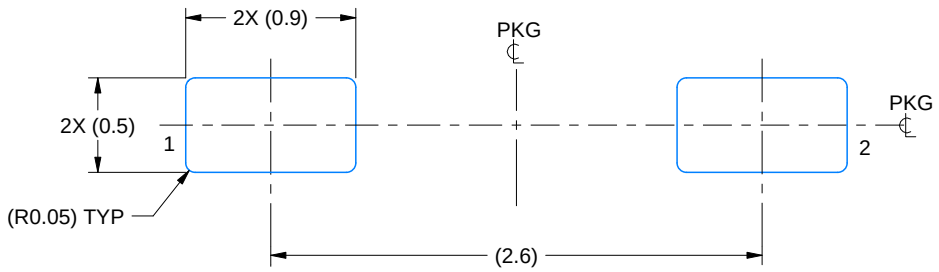

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
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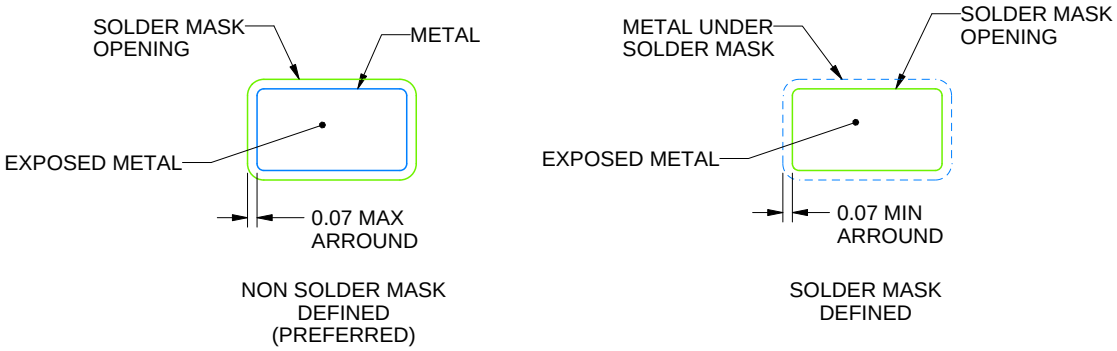

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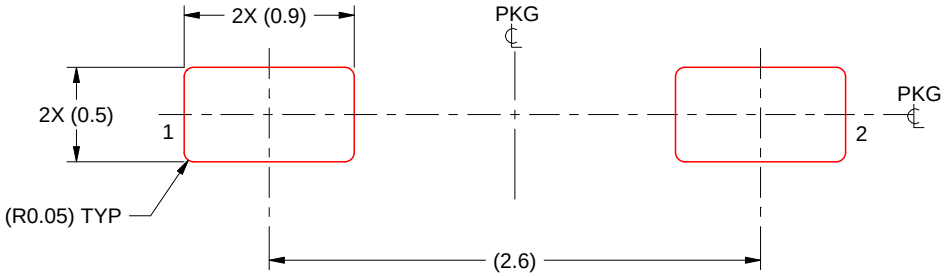

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4228484/C 12/2024

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