







ESD752, ESD762

SLVSGX0B - MAY 2022 - REVISED NOVEMBER 2022

ESD752 and ESD762 24-V, 2-Channel, ESD Protection With 5.7 A of 8/20 μs Surge Protection in a SOT-23 and SOT-323 / SC-70 Package

1 Features

- Robust surge protection:
 - IEC 61000-4-5 (8/20 µs): 5.7 A or 2.5 A
- IEC 61000-4-2 level 4 ESD protection:
 - ±30-kV or ±20-kV contact discharge
 - ±30-kV or ±20-kV air-gap discharge
- 24 V working voltage
- · Bidirectional ESD protection
- 2-channel device provides complete ESD and surge protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 3 pF or 1.7 pF (typical)
- · SOT-23 (DBZ) small, standard, common footprint
- SOT-323 / SC-70 (DCK) very small, standard, space saving, common footprint
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- USB power delivery (USB-PD):
 - VBUS protection
 - IO protection (withstand short to VBUS)
- Industrial control networks:
 - Smart distribution system (SDS)
 - DeviceNet IEC 62026-3
 - CANopen CiA 301/302-2 and EN 50325-4
 - 4/20 mA circuits
 - PLC surge protection
 - ADC surge protection

3 Description

The ESD752 and ESD762 are bidirectional ESD protection diodes for USB power delivery (USB-PD) and industrial interfaces. The ESD752 and ESD762 are rated to dissipate contact ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 level 4 standard (±30-kV or ±20-kV contact and ±30-kV or ±20-kV airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

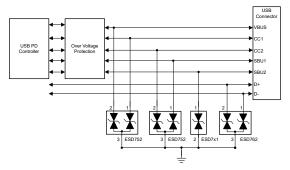
These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The $I_{PP}=5.7$ A (8/20 μ s surge waveform) capability of the ESD752 makes it suitable for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 3 pF or 1.7 pF line capacitance of the ESD752 and ESD762 are suitable for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

The ESD752 and ESD762 are offered in two leaded packages for easy flow through routing.

Package Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESD752	DCK (SOT-323 / SC-70, 3)	2.00 mm × 1.25 mm
	DBZ (SOT-23, 3)	2.92 mm × 1.30 mm
ESD762	DBZ (SOT-23, 3)	2.92 mm × 1.30 mm

 For all available packages, see the orderable addendum at the end of the data sheet.



USB Power Delivery Application

USB Power Delivery Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2022) to Revision B (November 2022)	Page
Added ESD762 Specifications to the data sheet	1
Added the Application Curves section	
Changes from Revision * (May 2022) to Revision A (August 2022)	Page
Changed the status of the data sheet from: Advanced Information to: Production Data	1



5 Pin Configuration and Functions

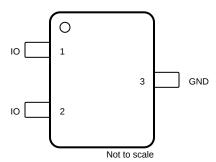


Figure 5-1. DCK and DBZ Package, 3-Pin SOT-323 / SC-70 and SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION	
NAME	NO.	1166	DESCRIPTION	
Ю	1, 2	I/O	ESD protected IO	
GND	3	G	Connect to ground.	

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	PARAMETER	DEVICE	MIN	MAX	UNIT
Desir	IEC 61000-4-5 Power (t _p – 8/20 μs) at 25°C	ESD752		210	W
Ppp	IEC 61000-4-5 Power (t _p – 8/20 μs) at 25°C	ESD762		90	W
	IEC 61000-4-5 current (t _p – 8/20 μs) at 25°C	ESD752		5.7	Α
I _{pp}	IEC 61000-4-5 current (t _p – 8/20 μs) at 25°C	ESD762		2.5	Α
T _A	Operating free-air temperature		-55	150	°C
TJ	Junction temperature		-55	150	°C
T _{stg}	Storage temperature		-65	155	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION		UNIT
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2500	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JS-002 (2)	± 1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufactuuring with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufactuuring with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	DEVICE	VALUE	UNIT
		IEC 61000-4-2 Contact Discharge, all pins	ESD752	±30000	V
V	Electrostatic discharge	TEC 61000-4-2 Contact Discharge, all pins	ESD762	±20000	V
V _(ESD)		IEC 61000-4-2 Air Discharge, all pins	ESD752	±30000	V
		TEC 01000-4-2 All Discharge, all plins	ESD762	±20000	V

6.4 Recommended Operating Conditions

PARAMETER		MIN	NOM MAX	UNIT
V _{IN}	Input voltage	-24	24	V
T _A	Operating free-air temperature	-55	150	°C

6.5 Thermal Information

THERMAL METRIC(1)			ESD752	ESD762	
		DBZ (SOT-23)	DCK (SOT-323 / SC-70)	DBZ (SOT-23)	UNIT
		3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.5	283.0	325.3	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	147.1	164.1	178.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	131.1	105.1	165.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.0	67.1	52.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	130.2	104.4	164.4	°C/W

Product Folder Links: ESD752 ESD762

6.5 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾			ESD752	ESD762	
		DBZ (SOT-23)	DCK (SOT-323 / SC-70)	DBZ (SOT-23)	UNIT
		3 PINS	3 PINS	3 PINS	
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over $T_A = 25^{\circ}C$ (unless otherwise noted)⁽¹⁾

	PARAMETER	TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			-24		24	V
V _{BRF}	Forward breakdown voltage ⁽²⁾	I _{IO} = 10 mA, IO to GND		25.5		35.5	V
V _{BRR}	Reverse breakdown voltage ⁽²⁾	I _{IO} = -10 mA, IO to GND		-35.5		-25.5	V
V	Clamping voltage ⁽³⁾	I_{PP} = 5.7 A, t_p = 8/20 µs, IO to GND	ESD752		37		V
V _{CLAMP}	Clamping voltage(4)	I_{PP} = 2.5 A, t_p = 8/20 μ s, from IO to GND	ESD762		36		V
V	Clamping voltage ⁽⁴⁾	I _{PP} = 16 A, TLP, IO to GND or GND to IO	ESD752		35		V
V _{CLAMP}	V _{CLAMP} Clamping voltage(**)	IPP - 10 A, TEP, 10 to GND of GND to 10	ESD762		38		V
V	Holding voltage after snapback ⁽⁵⁾	TLD	ESD752		30		V
V _{Hold}	Holding voltage after Shapback	ILP	ESD762		30		V
I _{LEAK}	Leakage current	V _{IO} = ±24 V, IO to GND		-50	5	50	nA
В	Dynamic resistance ⁽⁴⁾	IO to GND and GND to IO	ESD752		0.35		Ω
R _{DYN}	Dynamic resistance(**)	IO to GND and GND to IO	ESD762		0.57		Ω
C Line conscitones(6)	Line capacitance ⁽⁶⁾	V 0 V 5 4 MH= V 00 mV	ESD752		3	5	pF
CL	при сараспансе с	$V_{IO} = 0 \text{ V, f} = 1 \text{ MHz, } V_{pp} = 30 \text{ mV}$	ESD762		1.7	2.8	pF

⁽¹⁾ Measurements made on each IO channel.

(6) Measured from IO to GND on each channel.

⁽²⁾ V_{BRF} and V_{BRR} are defined as the voltage when +/- 10 mA is applied in the positive or negative direction respectively, before the device latches into the snapback state.

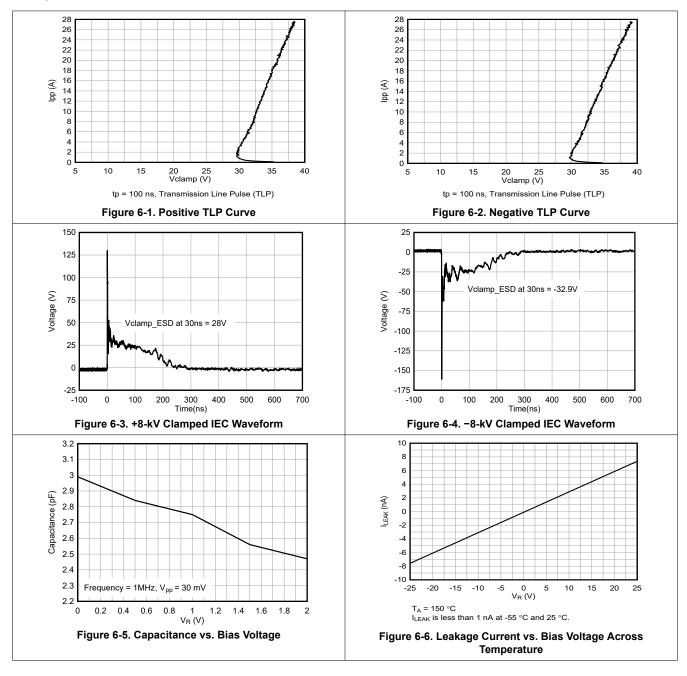
⁽³⁾ Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

⁽⁴⁾ Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

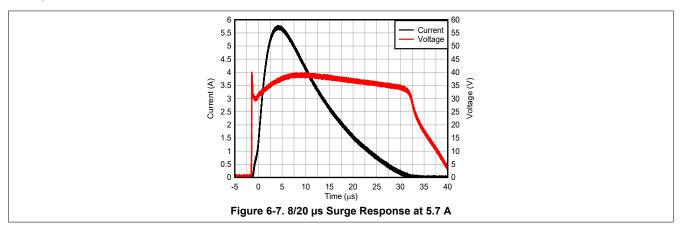
⁽⁵⁾ V_{HOLD} is defined as the lowest voltage on the TLP plot once the trigger threshold is reached and the device snapbacks and begins clamping the voltage.



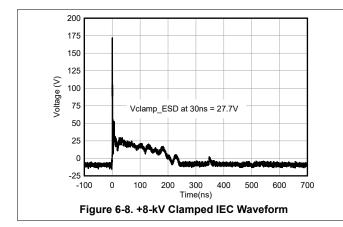
6.7 Typical Characteristics – ESD752

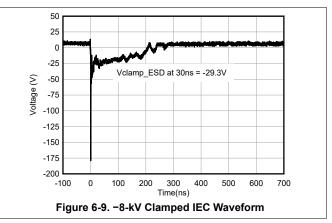


6.7 Typical Characteristics - ESD752 (continued)



6.8 Typical Characteristics - ESD762





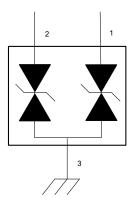
7 Detailed Description

7.1 Overview

The ESD752 and ESD762 are dual-channel ESD TVS diodes in SOT-23 and SOT-323 (SC-70) leaded packages which are convenient for automatic optical inspection. This product offers IEC 61000-4-2 ±30-kV or ±20-kV air-gap, ±30-kV or ±20-kV contact ESD protection respectively, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support.

A typical application of this product is the ESD protection for USB-PD slower speed signals (CC1, CC2, SBU1, SBU2, D+, and D-). The I_{PP} = 5.7 A (8/20 μ s surge waveform) capability of the ESD752 makes it suitable for protecting VBUS. The ESD752 device is also a good fit for protecting industrial IOs requiring 5.7 A or less of surge current protection. The 3 pF or 1.7 pF line capacitance of these ESD protection diodes are suitable for USB-PD slower speed signals and industrial IO applications.

7.2 Functional Block Diagram



7.3 Feature Description

The ESD752 and ESD762 are bidirectional TVS diodes with a high ESD protection level. This device protects the circuit from ESD strikes up to ±30-kV or ±20-kV contact and ±30-kV or ±20-kV air-gap respectively as specified in the IEC 61000-4-2 standard. The ESD752 and ESD762 can also handle up to 5.7 A or 2.5 A of surge current (IEC 61000-4-5 8/20 µs) respectively. The I/O capacitance of 3 pF or 1.7 pF (typical) are suitable for USB power delivery slower speed signals and industrial applications. These clamping devices have a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits.

For example, the ESD752 clamping voltage is only 37 V when the device is taking 5.7 A transient current. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows these diodes to conserve power when working below the V_{RWM} . The temperature range of -55° C to $+150^{\circ}$ C makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 and SOT-323 (SC-70) packages are good for applications requiring automatic optical inspection (AOI).

7.3.1 Temperature Range

These devices are qualified to operate from -55°C to +150°C.

7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 5.7 A and 2.5 A (8/20 µs waveform) for the ESD752 and ESD762 respectively. An ESD-surge clamp diverts this current to ground.

7.3.3 IO Capacitance

The capacitance between the I/O pins is 3 pF and 1.7 pF for the ESD752 and ESD762 respectively. These capacitances are suitable for USB power delivery slower speed signals and industrial applications.

7.3.4 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.35 Ω for the ESD752 device, and 0.57 Ω for the ESD762 device, which prevents system damage during ESD events.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of \pm 25.5 V. This protects sensitive equipment is protected from surges above the reverse standoff voltage of \pm 24 V.

7.3.6 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 50 nA (maximum) with a bias of ± 24 V.

7.3.7 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 37 V (I_{PP} = 5.7 A for 8/20 µs surge waveform), 35 V (I_{PP} = 16 A for TLP), 36 V (I_{PP} = 2.5 A for 8/20 µs surge waveform), and 38 V (I_{PP} = 16 A for TLP) for the ESD752 and ESD762, respectively.

7.3.8 Industry Standard Leaded Packages

These devices feature industry standard SOT-23 (DBZ) and SC-70 (DCK) leaded packages for automatic optical inspection (AOI).

7.4 Device Functional Modes

The ESD752 and ESD762 are dual channel passive clamp devices that have low leakage during normal operation when the voltage between IO and GND is below V_{RWM} , and activate when the voltage between IO and GND goes above V_{BR} . During IEC 61000-4-2 ESD events, transient voltages as high as ± 30 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD} , the device reverts back to the low leakage passive state.

8 Application and Implementation

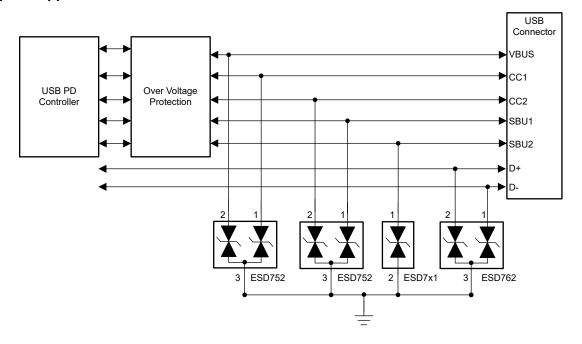
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD752 and ESD762 are dual channel TVS diodes which are used to provide a path to ground for dissipating ESD events on USB-PD or industrial IO signal lines. As the current from the ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

8.2 Typical Application



USB Power Delivery Application

Figure 8-1. USB Power Delivery Typical Application

8.2.1 Design Requirements

For this design example, the ESD752 and ESD762 are used to provide ESD protection on a USB-PD connector. Table 8-1 lists the known design parameters for this application.

Table 8-1. Design Parameters for the USB Power Delivery Typical Application

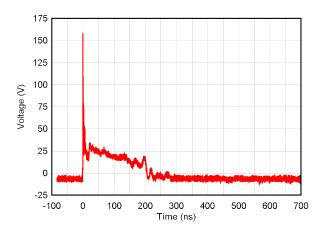
Design Parameter	Value		
Diode configuration	Bidirectional		
VBUS Voltage	+ 20 V		
V _{IO} signal range	+ 3.3 V		
V _{RWM}	± 24 V		
Short to VBUS event on V _{IO}	± 20 V		
Data rate	Up to 480 Mbps		

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8.2.2 Detailed Design Procedure

The ESD752 and ESD762 has a V_{RWM} of ± 24 V to prevent the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic protects both positive and negative polarity. The low 1.7 pF capacitance of the ESD762 device enables data rates up to 480 Mbps, which allows the designer to meet the requirements for the D+ and D- signals. The ESD752 has an I_{PP} = 5.7 A (8/20 μ s) surge current capability making it suitable for protecting the VBUS power rail.

8.2.3 Application Curves



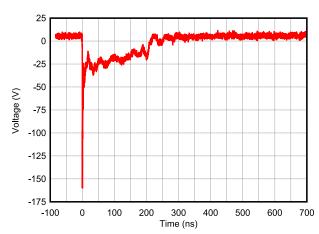


Figure 8-2. +8-kV Clamped IEC Waveform

Figure 8-3. −8-kV Clamped IEC Waveform

9 Power Supply Recommendations

These are passive TVS diode-based ESD protection devices; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.



10 Layout

10.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

This is a typical example of a dual channel IO routing.

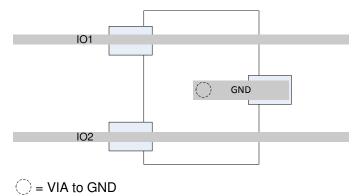


Figure 10-1. Routing with DBZ and DCK Package

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, ESD Layout Guide user's guide
- Texas Instruments, ESD and Surge Protection for USB Interfaces application note
- Texas Instruments, ESD Protection Diodes EVM user's guide
- Texas Instruments, Generic ESD Evaluation Module user's guide
- · Texas Instruments, Reading and Understanding an ESD Protection data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
ESD752DBZR	Active	Production	SOT-23 (DBZ) 3	3000 JUMBO T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RP8
ESD752DBZR.B	Active	Production	SOT-23 (DBZ) 3	3000 JUMBO T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RP8
ESD752DCKR	Active	Production	SC70 (DCK) 3	3000 JUMBO T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 150	1MP
ESD752DCKR.B	Active	Production	SC70 (DCK) 3	3000 JUMBO T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 150	1MP
ESD762DBZR	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RK8
ESD762DBZR.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RK8

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD752DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD752DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
ESD762DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3



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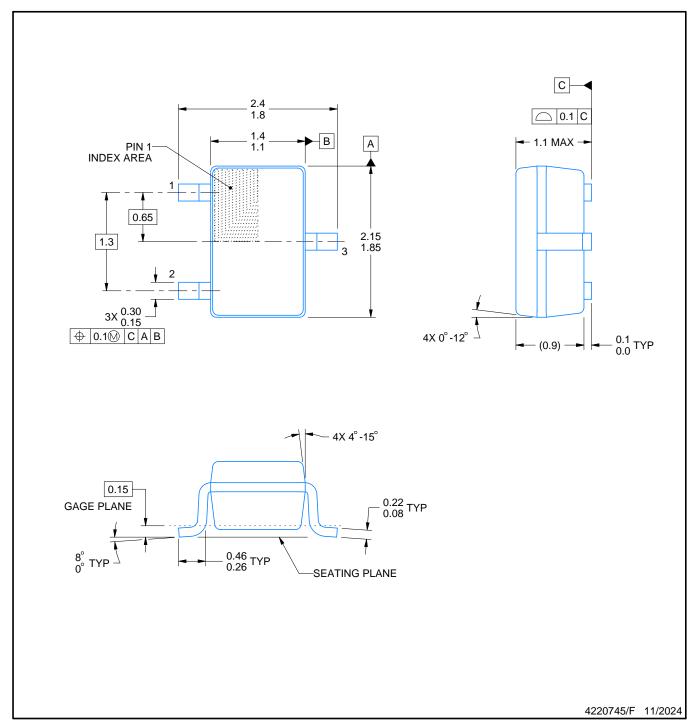


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD752DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD752DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
ESD762DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR SC70



NOTES:

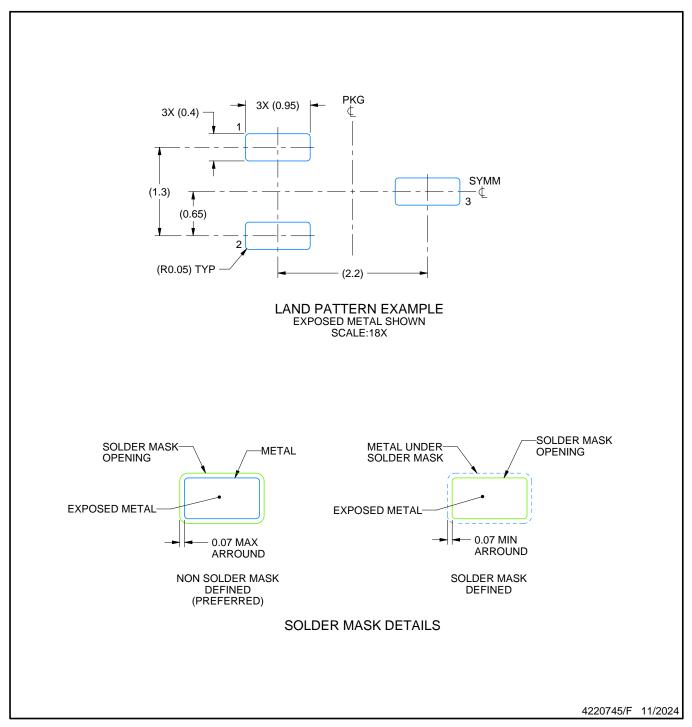
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed
- 0.25mm per side



SMALL OUTLINE TRANSISTOR SC70

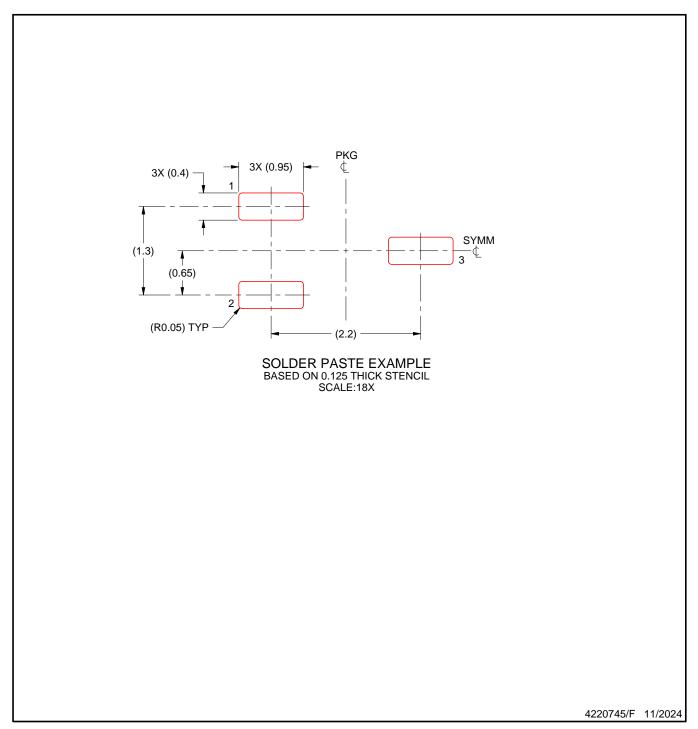


NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR SC70



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE TRANSISTOR



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC registration TO-236, except minimum foot length.

- 4. Support pin may differ or may not be present.
- 5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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