

# ESD652-Q1 Automotive 18V Bi-Directional ESD Protection in SOT-23 for In-Vehicle Networks

## 1 Features

- IEC 61000-4-5 surge protection:
  - 5.5A (8/20 $\mu$ s)
- IEC 61000-4-2 ESD protection:
  - $\pm$ 30kV contact discharge
  - $\pm$ 30kV air gap discharge
- 18V working voltage
- I/O Capacitance:
  - 4pF (typical)
- Bidirectional polarity to support positive and negative voltage swings
- 2 channel device provides complete ESD protection with single component
- Temperature range:  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$
- Small, leaded SOT-23 allows low cost automatic optical inspection (AOI)
- AEC-Q101 qualified

## 2 Applications

- **Automotive in-vehicle networks:**
  - Automotive hybrid and electric powertrain systems
  - Energy storage systems
  - Automotive battery management systems

## 3 Description

The ESD652-Q1 is a bidirectional ESD protection diode for battery management systems and other automotive applications. The ESD652-Q1 is rated to dissipate ESD strikes beyond the maximum level specified in the IEC 61000-4-2 international standard ( $\pm$ 30kV Contact,  $\pm$ 30kV Air-gap). The device can clamp 8/20 $\mu$ s surges with peak pulse currents up to 5.5A in accordance with the IEC 61000-4-5 standard.

This device features a 4pF (typical) IO capacitance enabling high-speed interface protection. The low dynamic resistance and low clamping voltage help protect systems against transient events. This protection is key as automotive systems require a high level of robustness and reliability when they control safety devices.

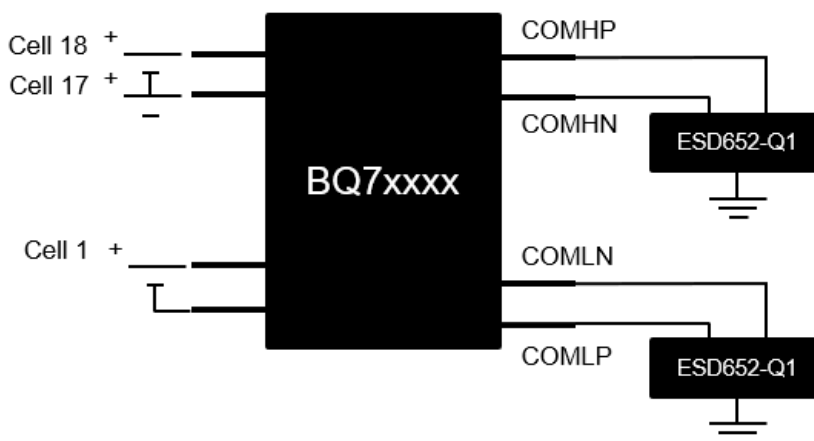
The ESD652-Q1 is available in a small leaded SOT-23 (DBZ) package.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
ESD652-Q1	DBZ (SOT-23, 3)	2.92mm $\times$ 2.37mm

(1) For more information, see [Section 9](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



Typical Application Schematic



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## 4 Pin Configuration and Functions

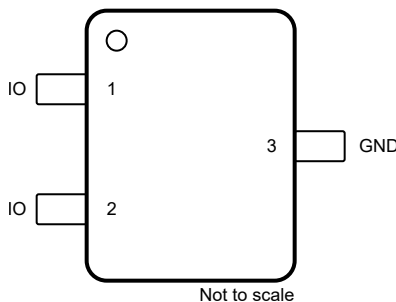


Figure 4-1. ESD652-Q1 DBZ Package, 3-Pin SOT-23 (Top View)

Table 4-1. Pin Functions for ESD652-Q1

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	Surge and ESD protected IO
GND	3	GND	Ground. Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, GND = ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

Parameter		MIN	MAX	UNIT
P <sub>PPM</sub>	IEC 61000-4-5 Surge (t <sub>p</sub> = 8/20 μs) Peak Pulse Power at 25 °C <sup>(2)</sup>		176	W
I <sub>PPM</sub>	IEC 61000-4-5 Surge (t <sub>p</sub> = 8/20 μs) Peak Pulse Current at 25 °C <sup>(2)</sup>		5.5	A
T <sub>A</sub>	Operating free-air temperature	–55	150	°C
T <sub>stg</sub>	Storage temperature	–65	155	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Voltages are with respect to GND unless otherwise noted.

### 5.2 ESD Ratings - AEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q101-001 <sup>(1)</sup>	±2500	V
		Charged device model (CDM), per AEC Q101-005 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

### 5.4 ESD Ratings - ISO Specifications

Parameter		Test Conditions	VALUE	UNIT	
V <sub>(ESD)</sub>	ISO 10605 Electrostatic Discharge	C = 150pF; R = 330Ω	Contact Discharge, all pins	±30000	V
			Air-gap Discharge, all pins	±30000	
		C = 330pF; R = 330Ω	Contact Discharge, all pins	±30000	
			Air-gap Discharge, all pins	±30000	

### 5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage between any 2 pins	–18		18	V
T <sub>A</sub>	Operating Free Air Temperature	–55		150	°C

## 5.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ESD652(Q1)	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	249.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	129.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	24.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	82.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.7 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage	$I_{IO} < 50\text{nA}$	-18		18	V
$I_{LEAK}$	Leakage current at $V_{RWM}$	$V_{IO} = \pm 18\text{V}$ , I/O to GND		1	50	nA
$V_{BR}$	Breakdown voltage, I/O to GND <sup>(1)</sup>	$I_{IO} = \pm 10\text{mA}$	19		25	V
$V_{CLAMP}$	Surge clamping voltage, $t_p = 8/20 \mu\text{s}$ <sup>(2)</sup>	$I_{PP} = \pm 1\text{A}$ , I/O to GND		22	25	V
		$I_{PP} = \pm 5.5\text{A}$ , I/O to GND		25	32	V
$V_{CLAMP}$	TLP clamping voltage, $t_p = 100 \text{ ns}$ <sup>(3)</sup>	$I_{PP} = \pm 16\text{A}$ TLP, I/O to GND		28		V
$R_{DYN}$	Dynamic resistance <sup>(4)</sup>	I/O to GND		0.32		$\Omega$
		GND to I/O		0.32		
$C_{LINE}$	Line capacitance, IO to GND	$V_{IO} = 0\text{V}$ , $f = 1\text{MHz}$		4		pF

(1)  $V_{BR}$  is defined as the voltage obtained at 10mA when sweeping the voltage up, before the device latches into the snapback state

(2) Device stressed with 8/20 $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5

(3) Non-repetitive square wave current pulse, Transmission Line Pulse (TLP); ANSI / ESD STM5.5.1-2008

(4) Extraction of  $R_{DYN}$  using least squares fit of TLP characteristics between  $I = 10\text{A}$  and  $I = 20\text{A}$

### 5.8 Typical Characteristics

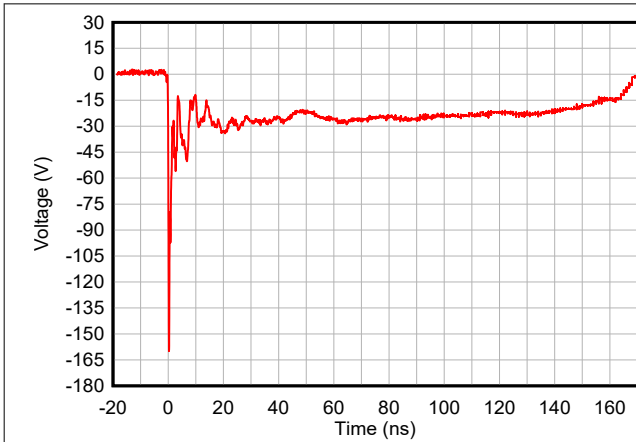


Figure 5-1. -8kV Clamped IEC Waveform

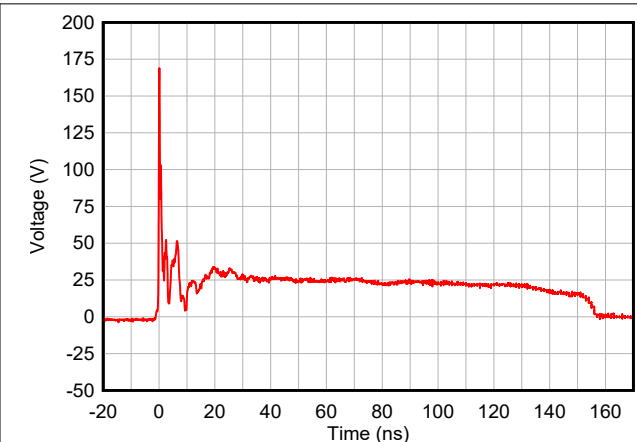


Figure 5-2. +8kV Clamped IEC Waveform

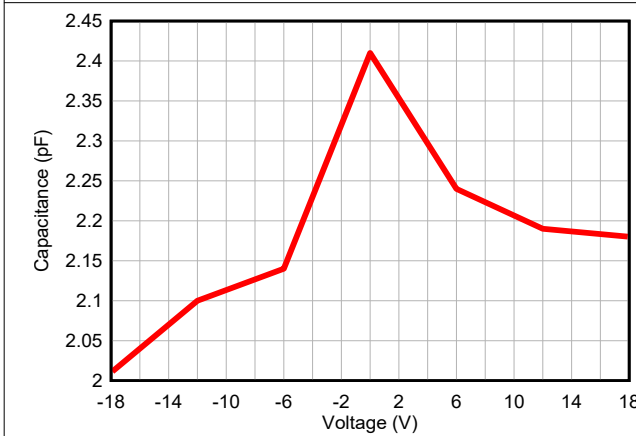


Figure 5-3. Capacitance vs. Bias Voltage

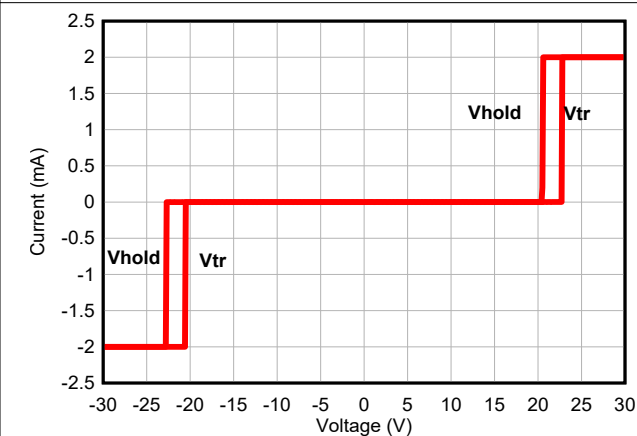


Figure 5-4. DC Voltage Sweep I-V Curve

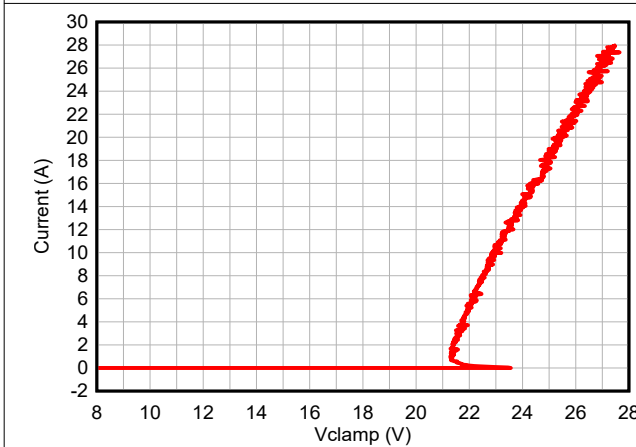


Figure 5-5. Negative TLP Curve

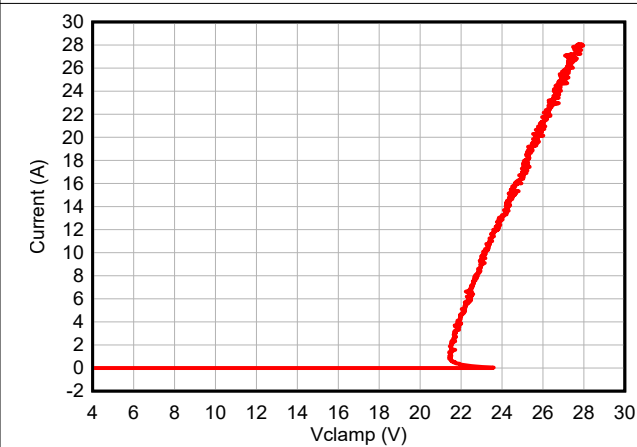
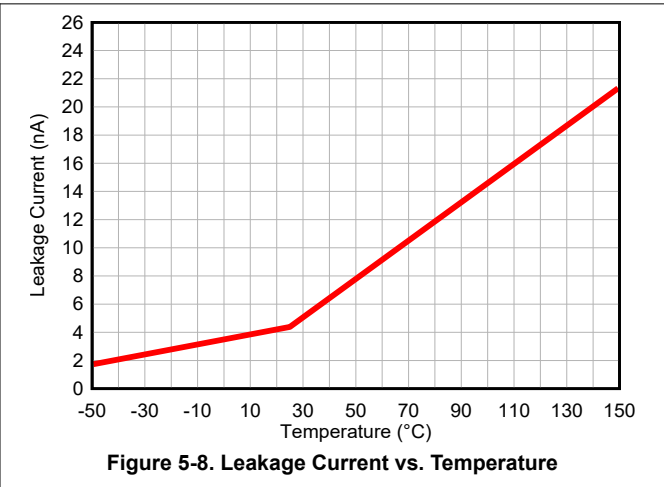
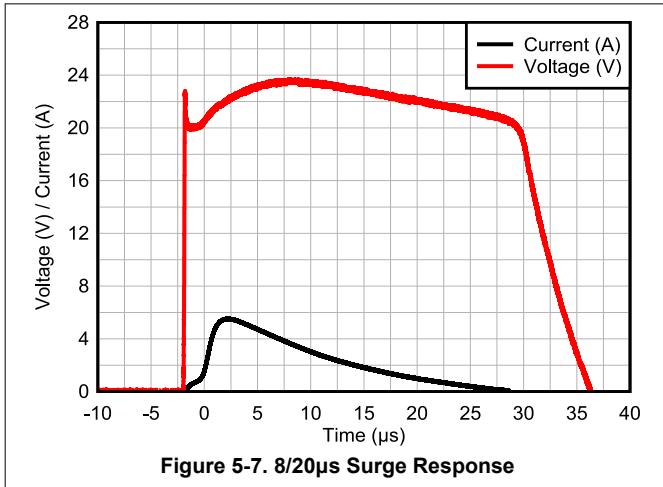


Figure 5-6. Positive TLP Curve

### 5.8 Typical Characteristics (continued)



## 6 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 6.1 Application Information

The ESD652-Q1 is a diode type TVS that provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#) for details.

## 7 Device and Documentation Support

### 7.1 Documentation Support

#### 7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Packaging and Layout Guide](#)
- Texas Instruments, [TI's IEC 61000-4-x Testing application note](#)
- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet user's guide](#)

### 7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 7.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 7.4 Trademarks

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### 7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 7.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 8 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ESD652DBZRQ1</a>	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	37M8
ESD652DBZRQ1.B	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	37M8

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF ESD652-Q1 :**

- Catalog : [ESD652](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

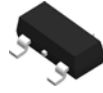
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD652DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD652DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

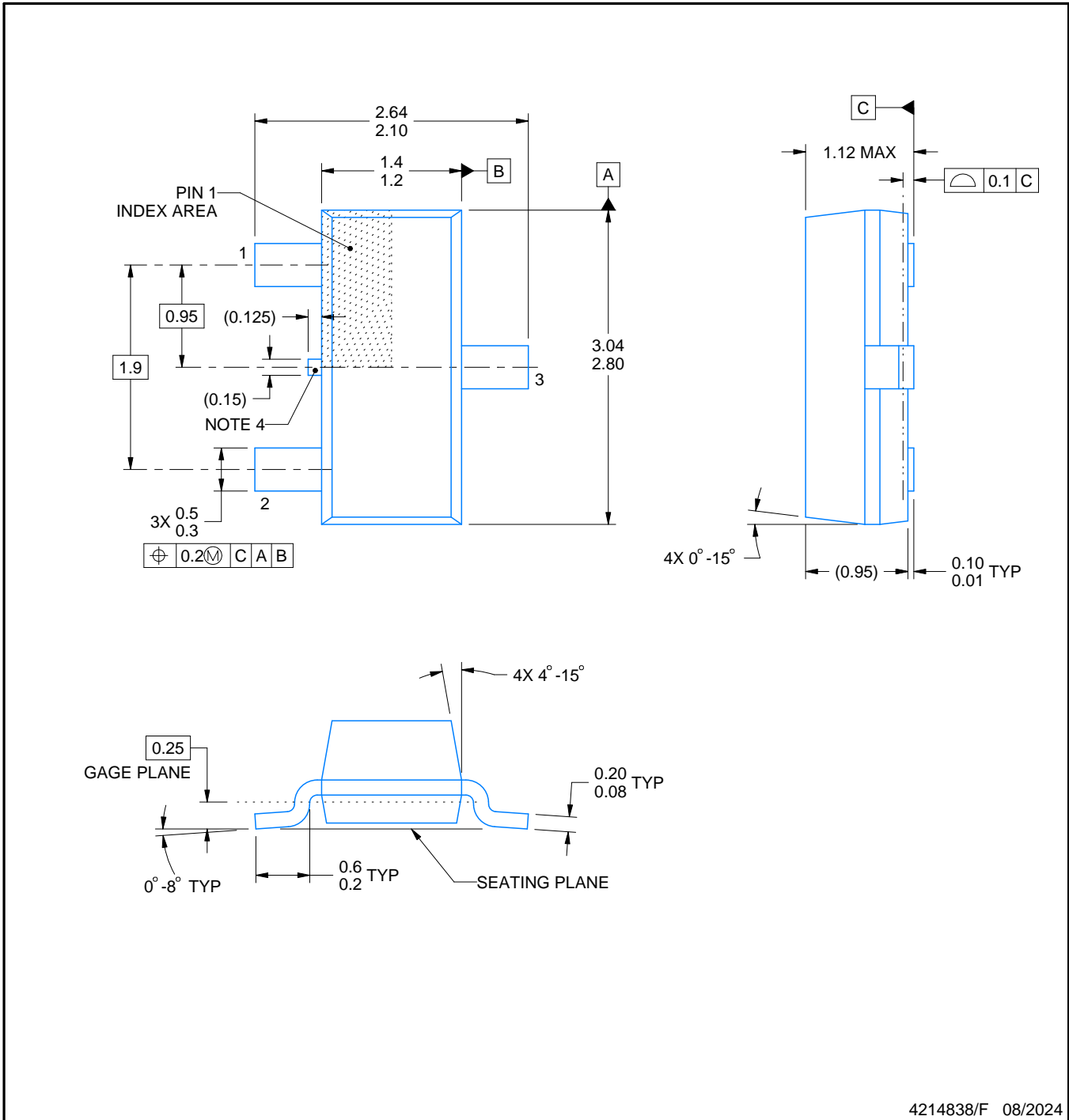
**DBZ0003A**



# PACKAGE OUTLINE

**SOT-23 - 1.12 mm max height**

SMALL OUTLINE TRANSISTOR



4214838/F 08/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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