ESD501-Q1 Automotive Low Capacitance ESD Diode for RF and ADAS Signal Protection

1 Features

- AEC-Q101 Qualified
- IEC 61000-4-2 ESD Protection:
  - ±15kV contact discharge
  - ±15kV air gap discharge
- ISO 10605 (330pF, 330Ω) ESD Protection:
  - ±12kV contact discharge
  - ±12kV air gap discharge
- IEC 61000-4-5 surge protection:
  - 3A (8/20µs)
- I/O capacitance: 0.3pF (typical)
- Ultra low leakage current: 1nA (typical)
- Industry standard 0402 package

2 Applications

- Automotive Antenna ESD Protection
- RF Signal ESD Protection
- Near Field Communications (NFC)
- Automotive SerDes w/Power over Coax
- USB Type-C (short-to-Vbus tolerant)

3 Description

The ESD501-Q1 is a bidirectional ESD protection diode. The ESD501-Q1 is offered in the industry standard 0402 (DFN1006) package, and offers an IEC 61000-4-2 protection level of 15kV. The device can clamp 8/20µs surges with peak pulse currents up to 3A in accordance with the IEC 61000-4-5 standard.

The low capacitance and low leakage current help to ensure protection against transient events in a variety of systems and applications. This protection is key for many applications, such as smaller form factors and faster data speeds, which are becoming more popular over time.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD501-Q1	DPY (DFN1006, 2)	1mm × 0.6mm

(1) For more information, see Section 8.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

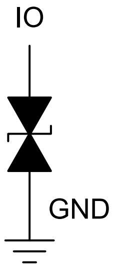

Figure 3-1. Functional Block Diagram

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4 Pin Configuration and Functions

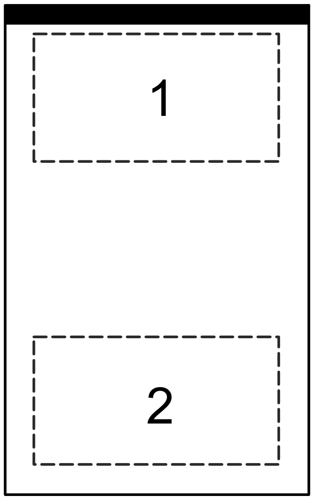

Figure 4-1. DPY Package, 2-Pin DFN1006 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD Protected Channel. If used as ESD I/O, connect pin 2 to ground
IO	2	I/O	ESD Protected Channel. If used as ESD I/O, connect pin 1 to ground

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		MIN	MAX	UNIT
I_{PPM}	IEC 61000-4-5 Surge (t_p = 8/20 µs) Peak Pulse Current at 25 °C (2)		3	A
T_A	Operating free-air temperature	–55	150	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltages are with respect to GND unless otherwise noted.

5.2 ESD Ratings - AEC Specifications

Parameter		Test Conditions	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001(1)	±2500	V
		Charged device model (CDM), per AEC Q101-005(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±15000	V
		IEC 61000-4-2 Air Discharge, all pins	±15000	

5.4 ESD Ratings - ISO Specifications

Parameter		Test Conditions		VALUE	UNIT
$V_{(ESD)}$	ISO 10605 Electrostatic Discharge	C = 150 pF; R = 330 Ω	Contact Discharge, all pins	±15000	V
			Air-gap Discharge, all pins	±15000	
		C = 330 pF; R = 330 Ω	Contact Discharge, all pins	±12000	
			Air-gap Discharge, all pins	±12000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-12		12	V
T_A	Operating Free Air Temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC[1]		ESD501-Q1	UNIT
		DPY (DFN1006)	
		2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	284.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	99.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.7 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	-12		12	V
I_{LEAK}	Leakage current at V_{RWM}	VIO = ±12 V, I/O to GND		1	10	nA
V_{BR}	Breakdown voltage, I/O to GND (1)	I_{IO} = ±1 mA	13.2	15	18	V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 3 A, I/O to GND		23		V
		I_{PP} = 3 A, GND to I/O		23		V
	TLP clamping voltage, t_p = 100 ns (3)	I_{PP} = ±4 A (100 ns TLP), I/O to GND		19.4		V
		I_{PP} = ±16 A (100 ns TLP), I/O to GND		27		V
R_{DYN}	Dynamic resistance (4)	I/O to GND		0.6		Ω
		GND to I/O		0.6		
C_{LINE}	Line capacitance, IO to GND	V_{IO} = 0 V, f = 1 MHz		0.3	0.5	pF

(1) V_{BR} is defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device enters the snapback state
(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5
(3) Non-repetitive square wave current pulse, Transmission Line Pulse (TLP); ANSI / ESD STM5.5.1-2008
(4) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.8 Typical Characteristics

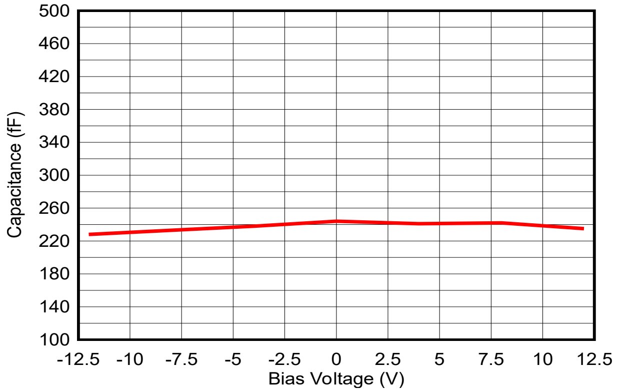

Figure 5-1. Bias Voltage vs. Capacitance

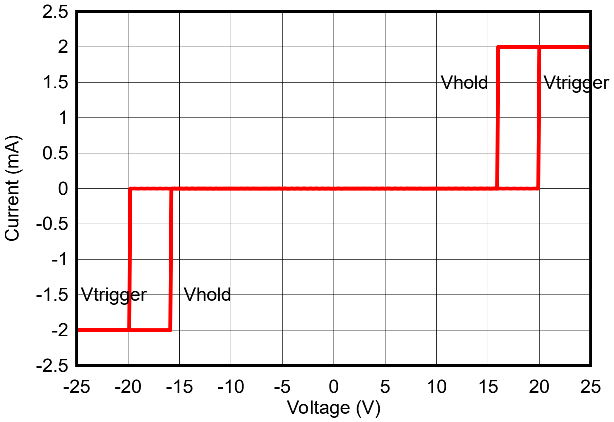

Figure 5-2. DC I-V Curve

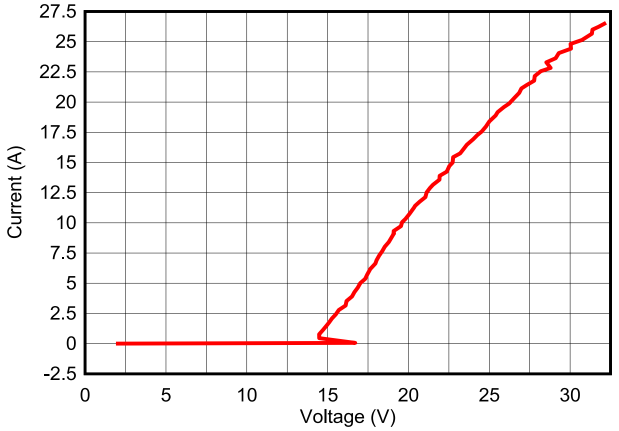

Figure 5-3. Positive TLP Curve

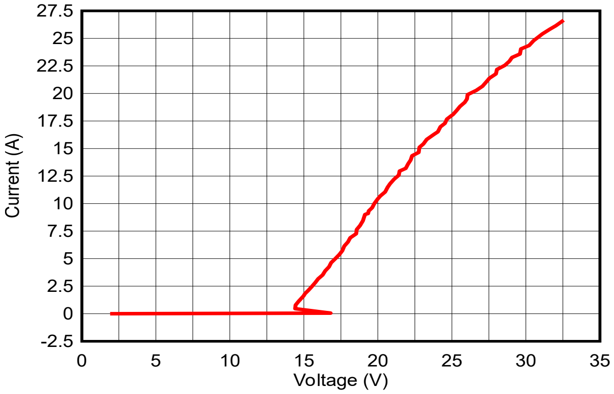

Figure 5-4. Negative TLP Curve

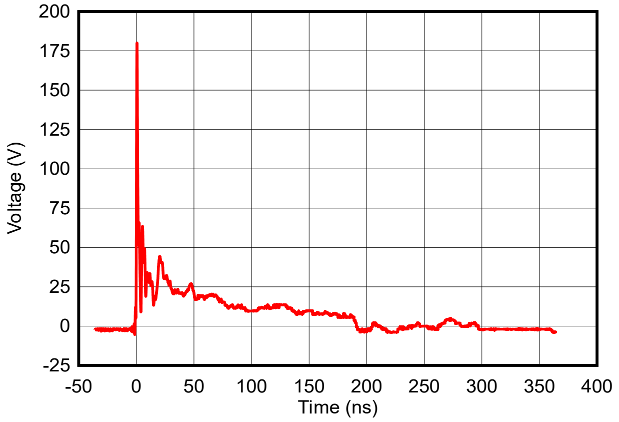

Figure 5-5. +8kV Clamped IEC Waveform

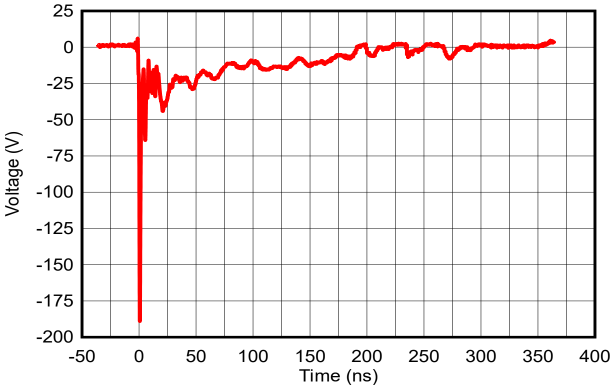

Figure 5-6. -8kV Clamped IEC Waveform

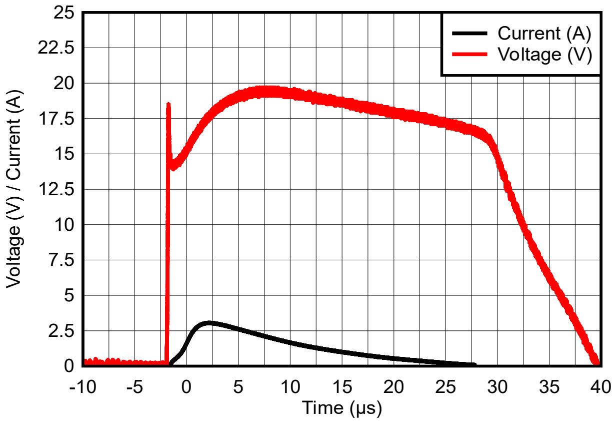

Figure 5-7. 8/20 µs Surge Response

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD501DPYRQ1	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-	Q4
ESD501DPYRQ1.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	-	Call TI	Call TI	See ESD501DPYRQ1	

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ESD501-Q1 :

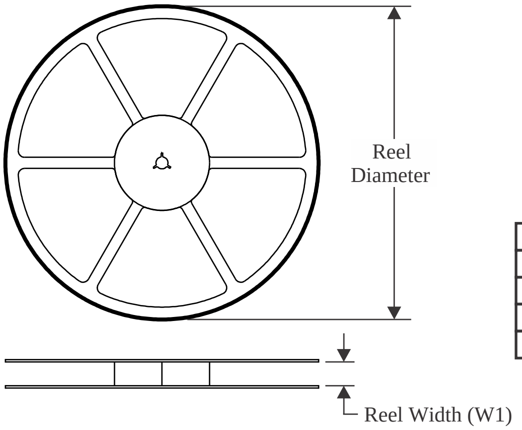
- Catalog : ESD501

NOTE: Qualified Version Definitions:

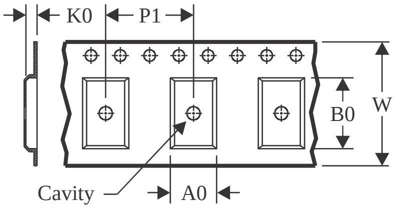
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

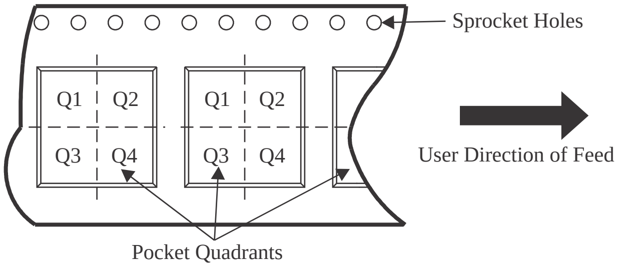


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

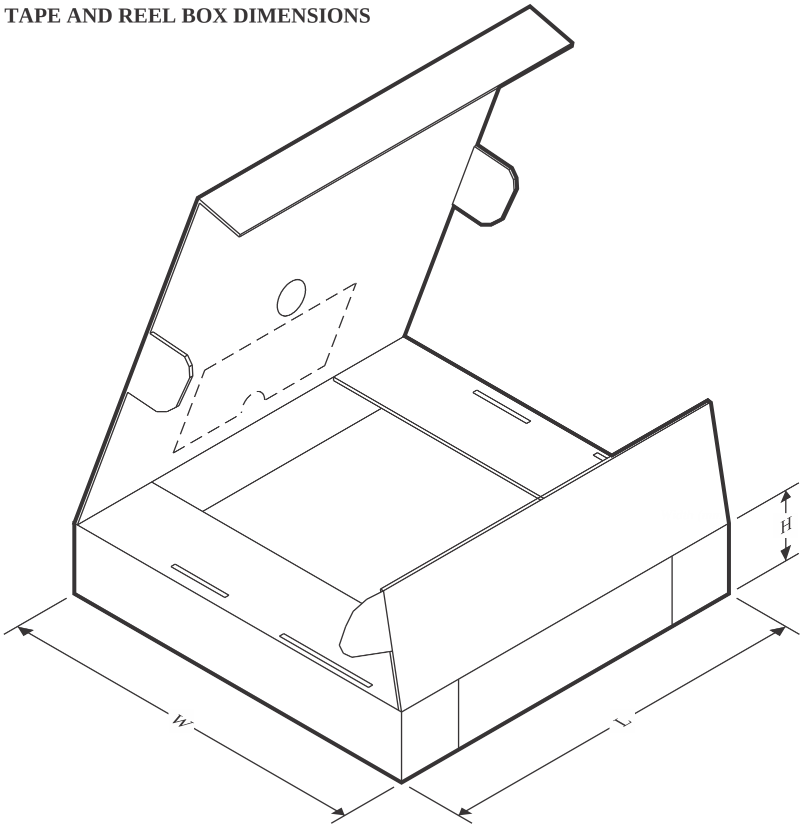
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD501DPYRQ1	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD501DPYRQ1	X1SON	DPY	2	10000	205.0	200.0	33.0

GENERIC PACKAGE VIEW

DPY 2 **X1SON - 0.45 mm max height**

1 x 0.6 mm PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

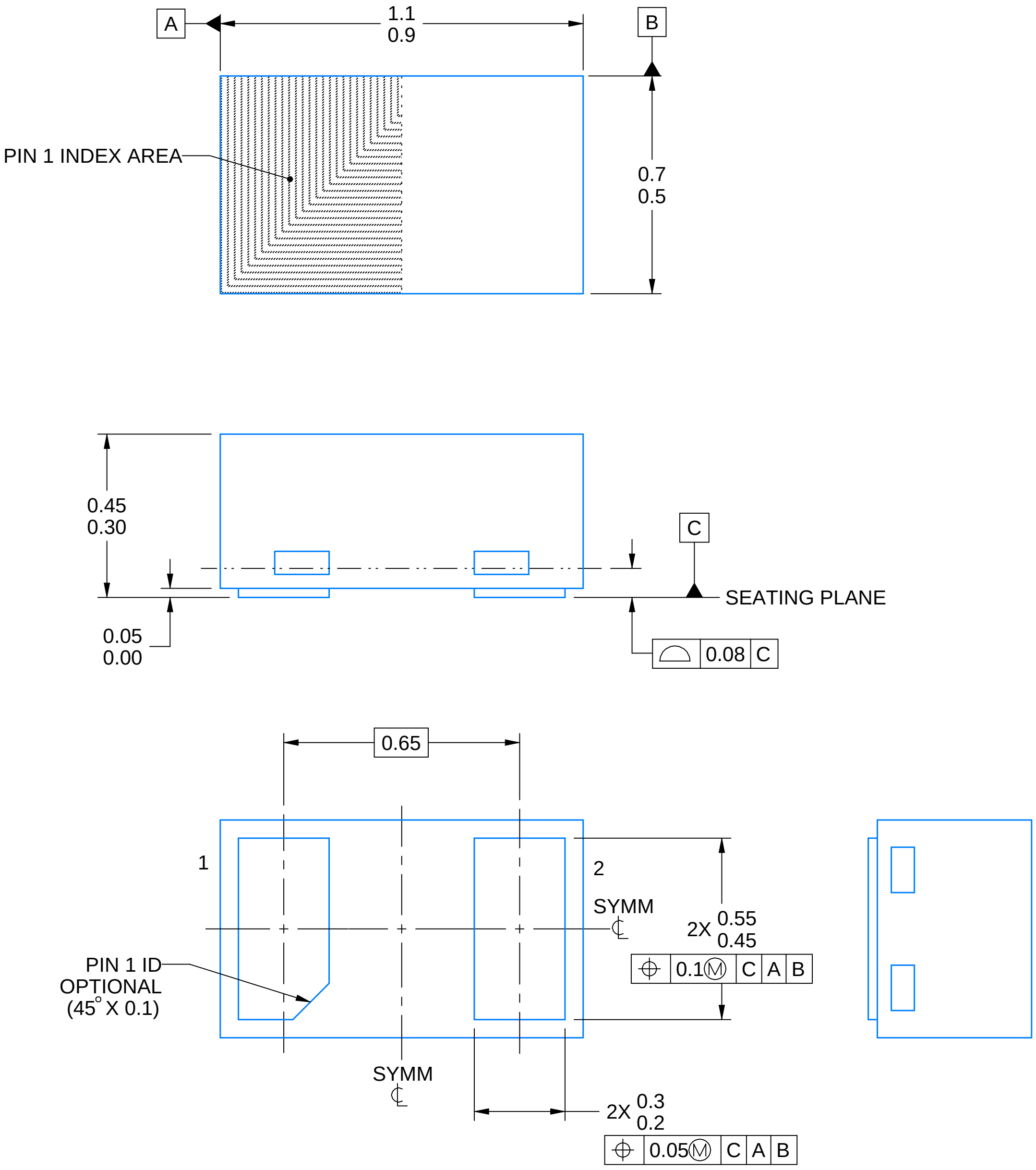
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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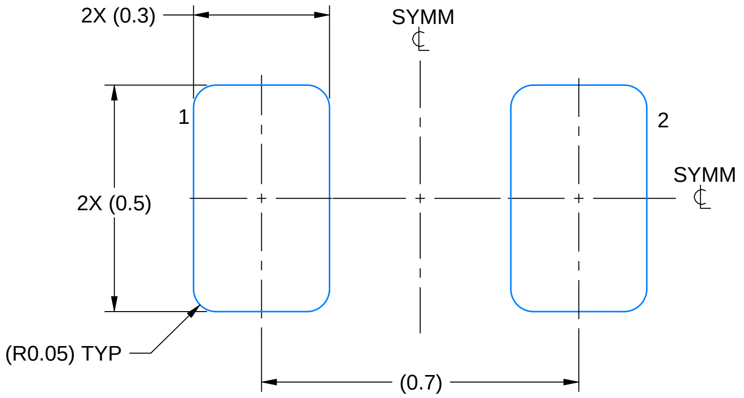
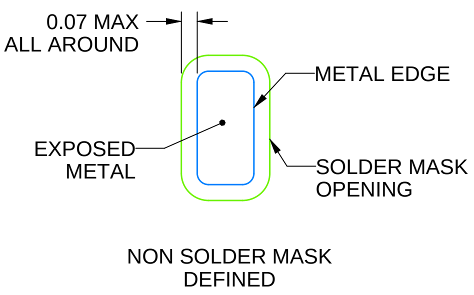
NOTES:

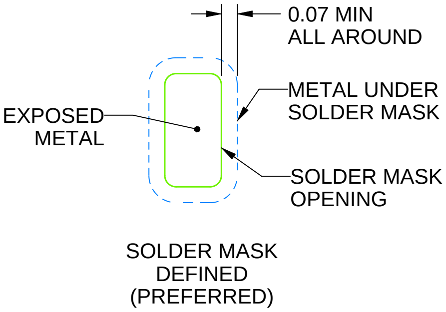
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



NON SOLDER MASK
DEFINED

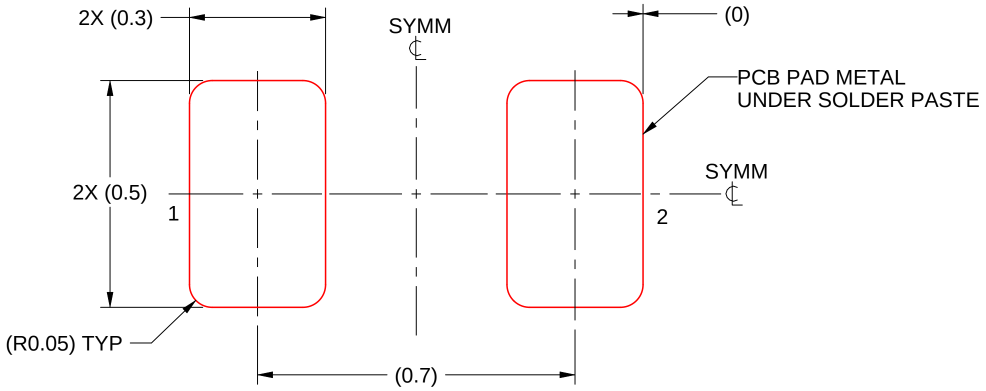


SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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