ESD441 1-Channel ±30 kV Unidirectional ESD Diode in an 0201 Package

1 Features

- IEC 61000-4-2 level 4 ESD protection
  - ±30 kV contact discharge
  - ±30 kV air gap discharge
- IEC 61000-4-5 surge protection
  - 6.2 A (8/20 µs)
- IO capacitance:
  - 1 pF (typical)
- DC breakdown voltage: 7 V (typical)
- Ultra low leakage current: 50 nA (maximum)
- Extremely low ESD clamping voltage
  - 7.6 V at 16 A TLP
  - R_{DYN}: 0.1 Ω (I/O to GND)
- Low insertion loss: 2 GHz (–3 dB bandwidth)
- Supports high speed interfaces up to 4 Gbps
- Industrial temperature range: –55°C to +150°C
- Space-saving industry standard 0201 footprint (0.6 mm × 0.3 mm × 0.3 mm)

2 Applications

- End equipment:
  - Vacuum robots
  - Wearables
  - Smart speakers
  - Portable electronics
  - Small appliances
  - Retail automation and payment
  - Laptops and desktops
  - TV and monitors
  - Docking stations
- Interfaces:
  - USB 2.0
  - HDMI™ 1.4 and 2.0
  - DisplayPort™
  - SIM card
  - GPIO

3 Description

The ESD441 is a unidirectional ESD protection diode for protecting data lines and other I/O ports. The ESD441 is rated to dissipate ESD strikes up to ±30 kV per the IEC 61000-4-2 international standard (greater than Level 4).

This device features a 1 pF (typical) IO capacitance enabling high-speed interfaces protection for protocols such as USB 2.0. The extremely low dynamic resistance (0.1 Ω) and clamping voltage (7.6 V at 16 TLP) is specified for system level protection against transient events.

The 30 kV ESD rating and 6.2 A surge provides robust transient protection in a tiny package for protecting 5.5 V power rails in portable electronics and other space constrained applications such as wearables.

The ESD441 is offered in the industry standard 0201 (DPL) package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD441	DPL (X2SON, 2)	0.6 mm × 0.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Functional Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2023) to Revision A (June 2023)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

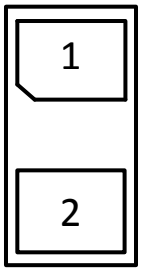

Figure 5-1. DPL Package, 2-Pin X2SON (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected channel
GND	2	GND	Ground. Connect to ground.

(1) I = input, O = output, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Peak Pulse (2) (3)	IEC 61000-4-5 power (t_p - 8/20 µs)		45	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		6	A
T_A	Ambient Operating Temperature	-55	150	°C
T_{stg}	Storage Temperature	-65	155	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25℃

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	Pin 1 to 2	0		5.5	V
T_A	Operating free-air temperature		-55		150	°C

6.5 Thermal Information

THERMAL METRIC (1)		ESD441 DPL (X2SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	519.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	336.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	209.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	136.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	207.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <100 nA, across operating temperature range			5.5	V
I_{LEAK}	Reverse leakage current	V_{IO} = 5.5 V, IO to GND		1	50	nA
V_{BR}	Break-down voltage	I_{IO} = 1 mA, IO to GND	6	7	8	V
V_{FWD}	Forward voltage	I_{IO} = 1 mA, GND to IO		0.8		V
V_{HOLD}	Holding voltage (2)	TLP, IO to GND		6.2		V
V_{CLAMP}	Clamping voltage with TLP (2)	I_{PP} = 1 A, TLP, IO to GND		6.3		V
		I_{PP} = 5 A, TLP, IO to GND		6.5		V
		I_{PP} = 16 A, TLP, IO to GND		7.6		V
		I_{PP} =16 A, TLP, GND to IO		3.8		V
	Clamping voltage with surge strike (4)	I_{PP} = 6 A, t_p = 8/20 µs , IO to GND		7.6		V
R_{DYN}	Dynamic resistance (3)	IO to GND		0.1		Ω
		GND to IO		0.16		
C_L	Line capacitance	V_{IO} = 0 V; f = 1 MHz, V_{pp} = 30 mV, IO to GND		1		pF

(1) Typical parameters are measured at 25℃
(2) Transition line pulse with 100 ns width and 10 ns rise and fall time
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A
(4) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5

6.7 Typical Characteristics

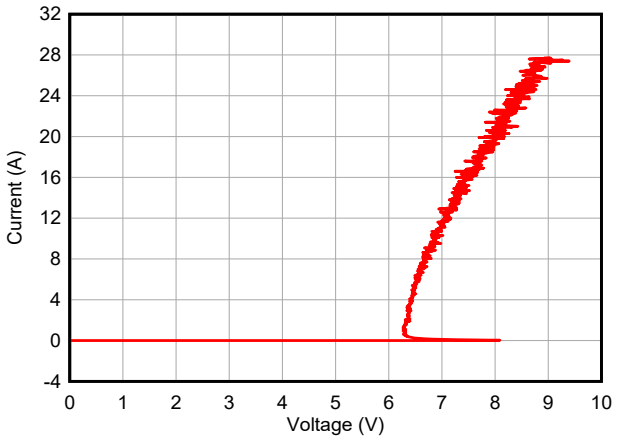

Figure 6-1. Positive TLP Curve

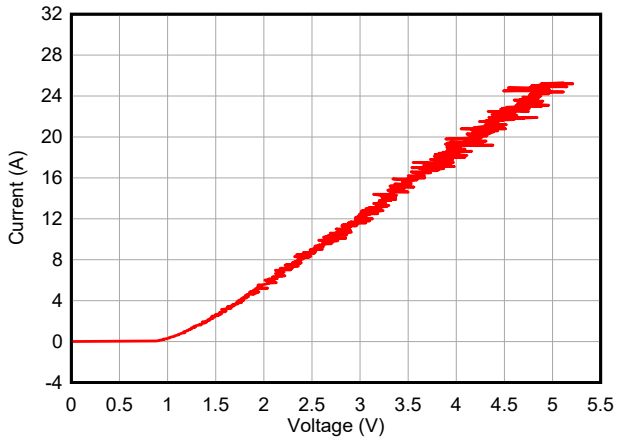

Figure 6-2. Negative TLP Curve

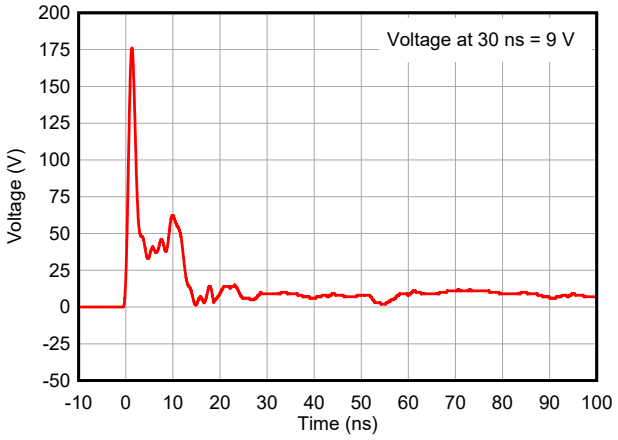

Figure 6-3. +8-kV Clamped IEC Waveform

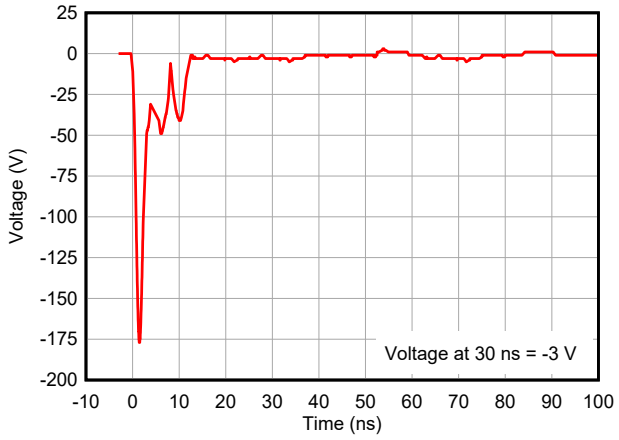

Figure 6-4. -8-kV Clamped IEC Waveform

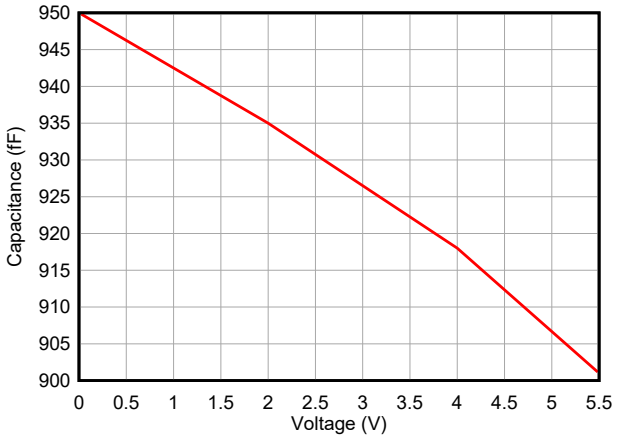

Figure 6-5. Bias Voltage vs. Capacitance

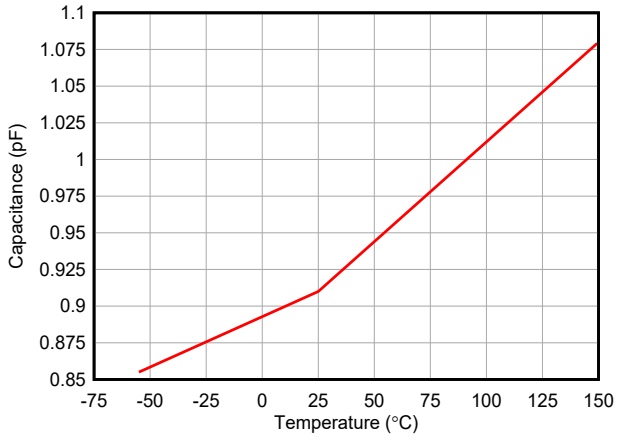

Figure 6-6. Temperature vs. Capacitance

6.7 Typical Characteristics (continued)

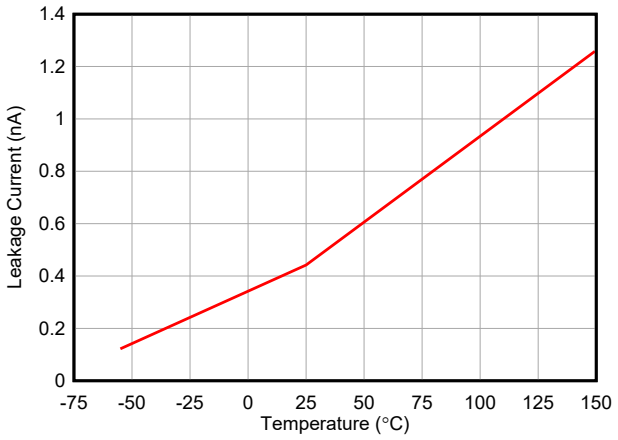

Figure 6-7. Temperature vs. Leakage Current

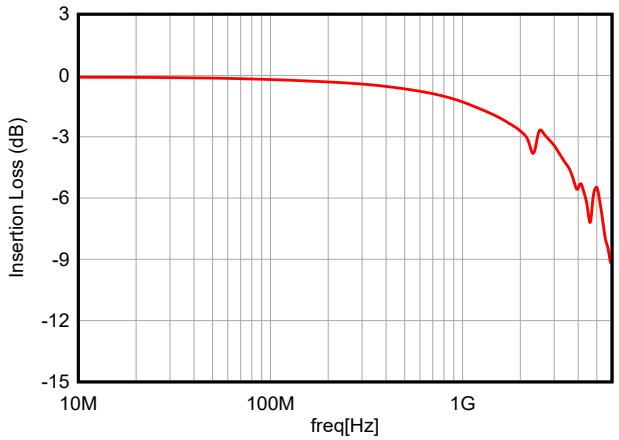

Figure 6-8. Insertion Loss

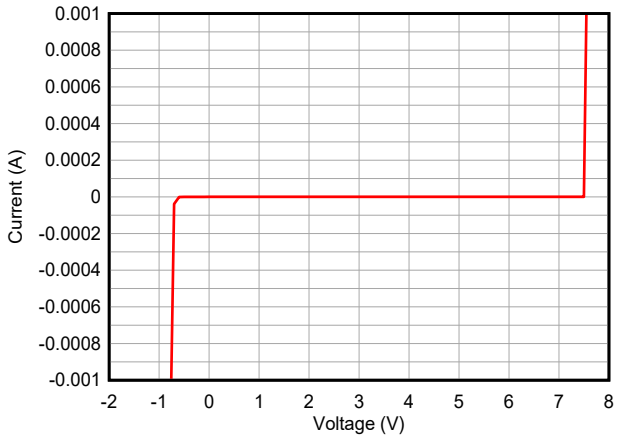

Figure 6-9. DC I-V Curve

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESD441 is a diode type TVS which provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. The device should be connected in parallel to the down stream circuitry it is protecting. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, please refer to the *ESD Packaging and Layout Guide* for details.

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Packaging and Layout Guide*
- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD441DPLR	Active	Production	X2SON (DPL) | 2	15000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E
ESD441DPLR.B	Active	Production	X2SON (DPL) | 2	15000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

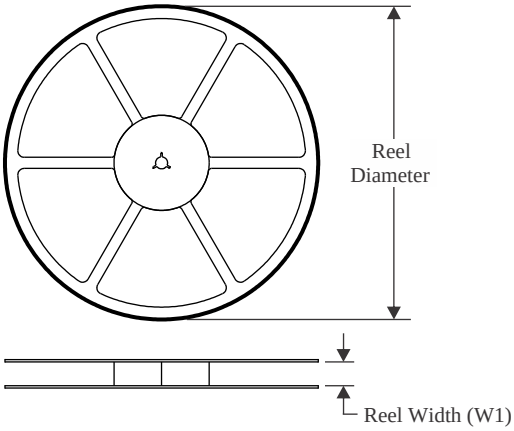
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

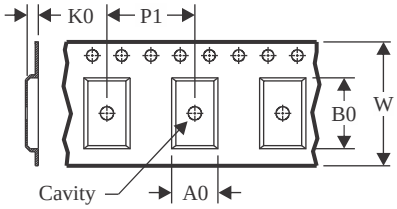
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

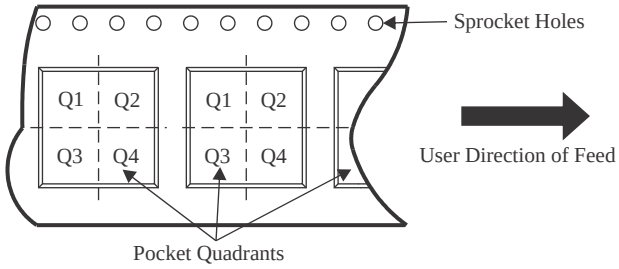


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

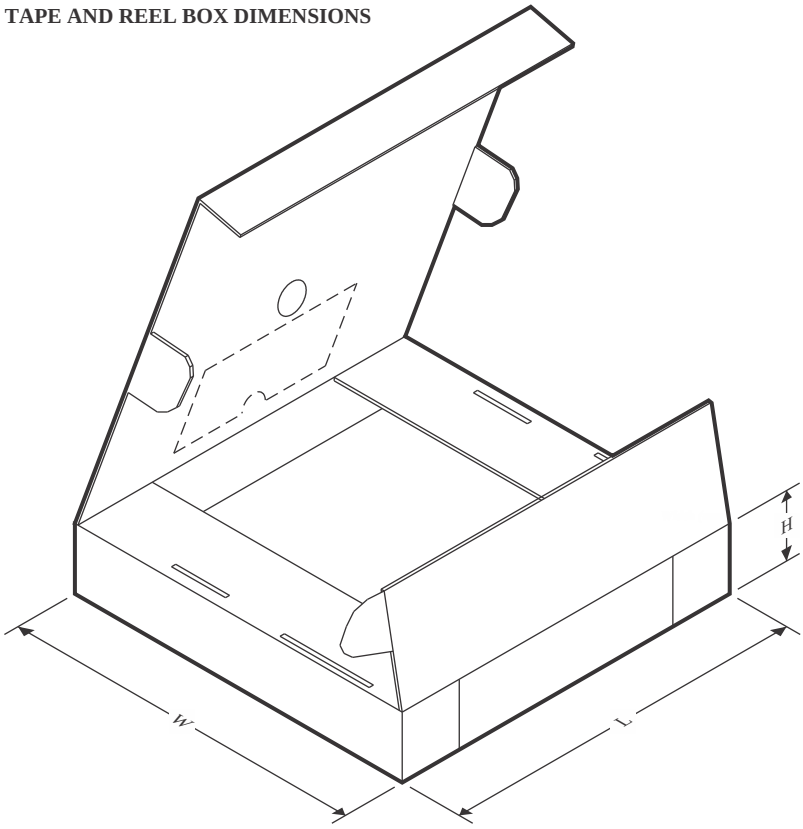
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD441DPLR	X2SON	DPL	2	15000	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1

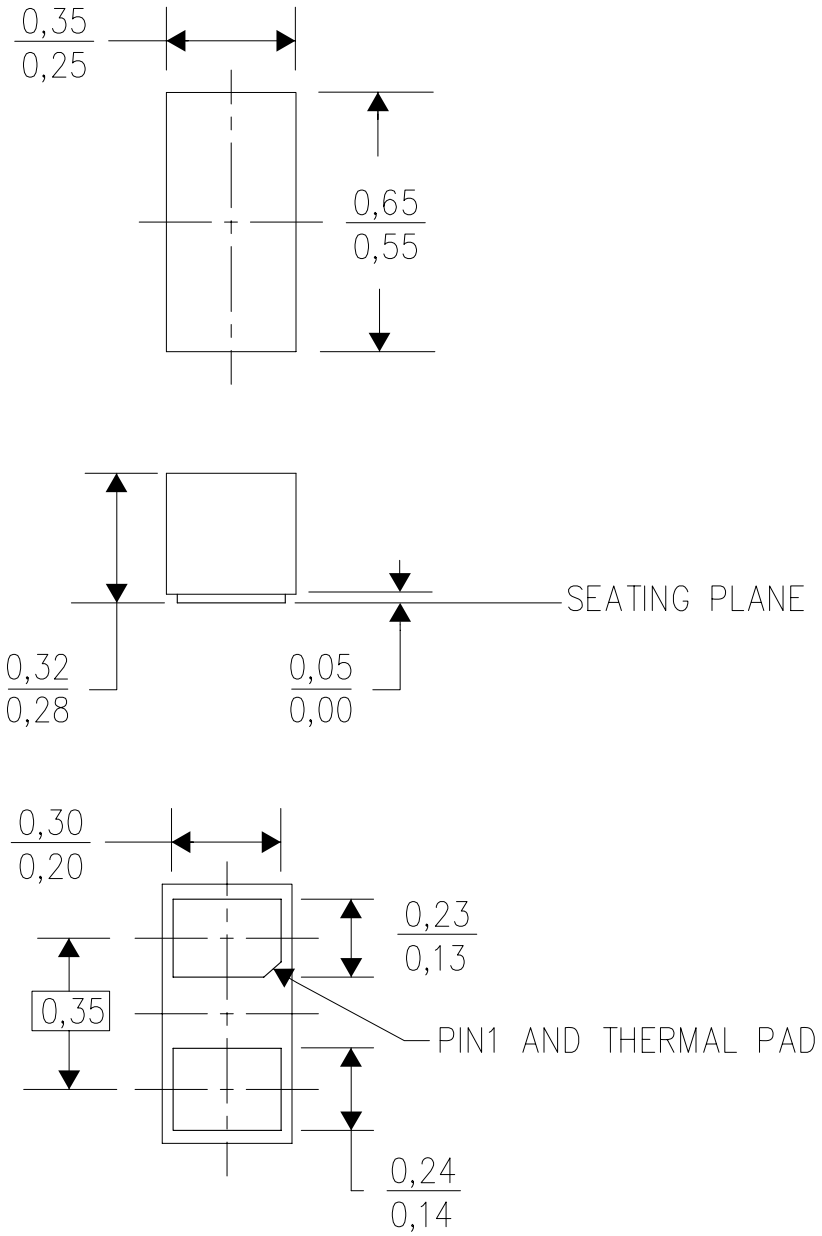
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD441DPLR	X2SON	DPL	2	15000	205.0	200.0	33.0

DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

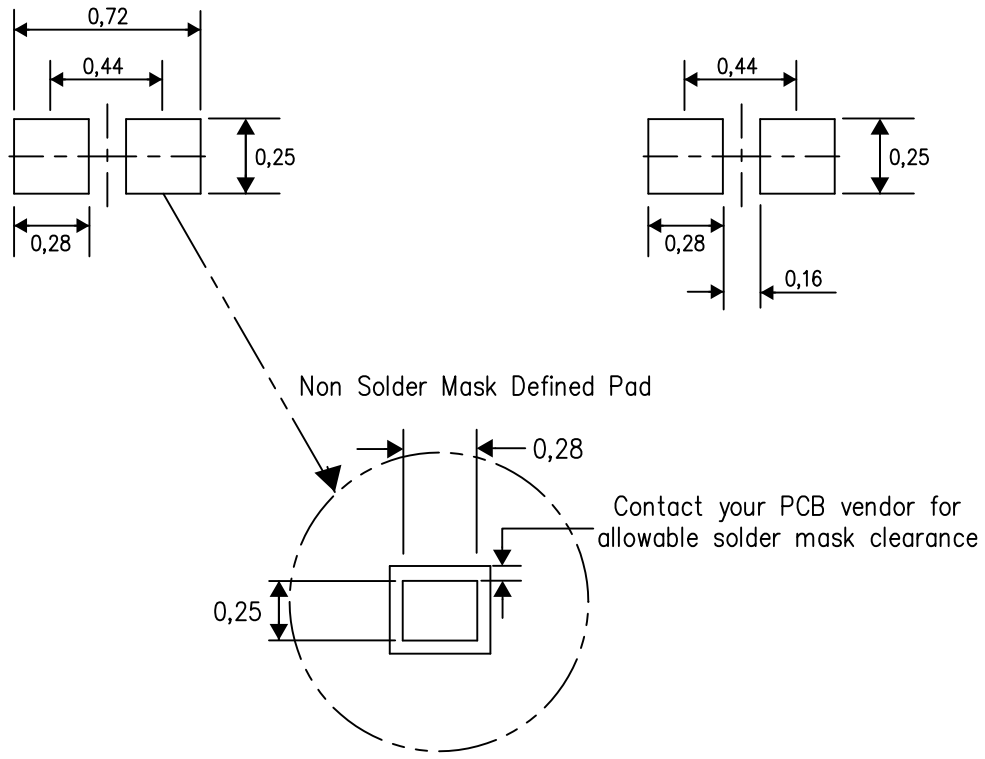


4212149/B 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

DPL (R–PX2SON–N2) SMALL PACKAGE OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)

4217903/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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