

## DS280BR810 Low Power 28 Gbps 8 Channel Linear Repeater

### 1 Features

- Octal-Channel Multi-Protocol Linear Equalizer Supporting up to 28-Gbps Interfaces
- Low Power Consumption: 93 mW and Channel (Typical)
- No Heat Sink Required
- Linear Equalization for Seamless Support of CR4/KR4 Link Training
- Extends Channel Reach by 15 dB+ Beyond Normal ASIC-to-ASIC Capability
- Ultra-Low Latency: 100 ps (Typical)
- Low Additive Random Jitter
- Small 8-mm x 13-mm BGA Package with Integrated RX and TX AC Coupling Capacitors for Easy Flow-Through Routing
- Unique Pinout Allows Routing High-Speed Signals Underneath the Package
- Pin-Compatible Retimer Available
- Single 2.5-V  $\pm 5\%$  Power Supply
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Operating Temperature Range

### 2 Applications

- [Backplane and Mid-Plane Reach Extension](#)
- Front-Port Eye Opener for Optical and Passive Copper (100G-SR4/LR4/CR4)
- QSFP28, SFP28, CFP2, CFP4, CDFP

### 3 Description

The DS280BR810 is an extremely low-power, high-performance eight-channel linear equalizer supporting multi-rate, multi-protocol interfaces up to 28 Gbps. It is used to extend the reach and improve the robustness of high-speed serial links for front-port, backplane, and chip-to-chip applications.

The linear nature of the DS280BR810's equalization preserves the transmit signal characteristics, thereby allowing the host and link partner ASICs to freely negotiate transmit equalizer coefficients (100 G-CR4/KR4). This transparency to the link training protocol facilitates system-level interoperability with minimal effect on the latency. Each channel operates independently, which allows the DS280BR810 to support individual lane Forward Error Correction (FEC) pass-through.

The DS280BR810's small package dimensions, optimized high-speed signal escape, and the pin-compatible retimer portfolio make the DS280BR810 ideal for high-density backplane applications. Simplified equalization control, low power consumption, and ultra-low additive jitter make it suitable for front-port interfaces such as 100 G-SR4/LR4/CR4. The small 8-mm x 13-mm footprint easily fits behind numerous standard front-port connectors like QSFP28, SFP28, CFP2/CFP4, and CDFP without the need for a heat sink.

Integrated AC coupling capacitors (RX and TX) eliminate the need for external capacitors on the PCB. The DS280BR810 has a single power supply and minimal need for external components. These features reduce PCB routing complexity and bill of materials (BOM) cost.

A pin-compatible retimer device is available for longer reach applications.

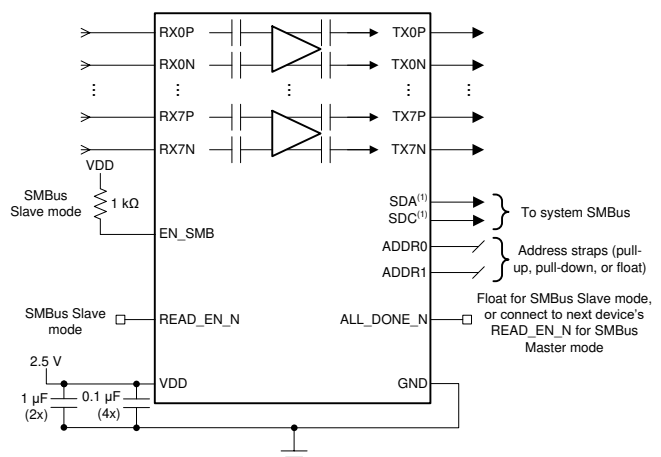
The DS280BR810 can be configured either via the SMBus or through an external EEPROM. Up to 16 devices can share a single EEPROM.

#### Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS280BR810	nFBGA (135)	8.00 mm x 13.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



(1) SMBus signals need to be pulled up elsewhere in the system.



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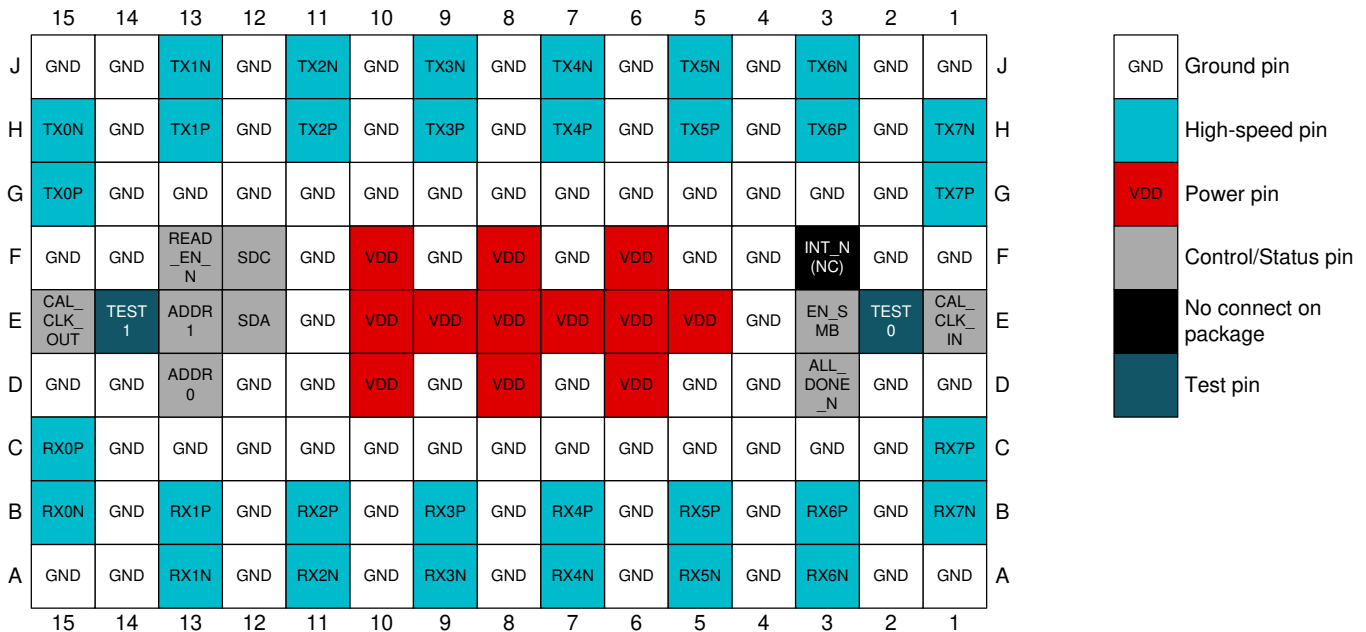
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2017) to Revision C	Page
• Initial Public Release .....	<b>1</b>

## 5 Pin Configuration and Functions

**ZBF Package**  
**135-Pin nfBGA**  
**Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
HIGH SPEED DIFFERENTIAL I/O			
RX0N	B15	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX0P	C15	Input	
RX1N	A13	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX1P	B13	Input	
RX2N	A11	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX2P	B11	Input	
RX3N	A9	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX3P	B9	Input	
RX4N	A7	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX4P	B7	Input	
RX5N	A5	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX5P	B5	Input	
RX6N	A3	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX6P	B3	Input	
RX7N	B1	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX7P	C1	Input	
TX0N	H15	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX0P	G15	Output	

### Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TX1N	J13	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX1P	H13	Output	
TX2N	J11	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX2P	H11	Output	
TX3N	J9	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX3P	H9	Output	
TX4N	J7	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX4P	H7	Output	
TX5N	J5	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX5P	H5	Output	
TX6N	J3	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX6P	H3	Output	
TX7N	H1	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs are AC coupled with 220-nF capacitors assembled on the package substrate.
TX7P	G1	Output	
CALIBRATION CLOCK PINS (FOR SUPPORTING UPGRADE PATH TO PIN-COMPATIBLE RETIMER DEVICE)			
CAL_CLK_IN	E1	Input	25-MHz (±100 PPM) 2.5-V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. <b>A 25-MHz input clock is only required if there is a need to support a future upgrade to the pin-compatible Retimer device.</b> If there is no need to support a future upgrade to a pin-compatible Retimer device, then a 25-MHz clock is not required. this pin can be left floating. This input pin has a weak active pull down and can be left floating if the CAL_CLK feature is not required.
CAL_CLK_O UT	E15	Output	2.5-V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion.
SYSTEM MANAGEMENT BUS (SMBus) PINS			
ADDR0	D13	Input, 4-Level	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 10 kΩ to GND F: Float 1: 1 kΩ to VDD
ADDR1	E13	Input, 4-Level	
ALL_DONE_ N	D3	Output, LVCMOS	Indicates the completion of a valid EEPROM register load operation when in SMBus master mode (EN_SMB = Float): High = External EEPROM load failed or incomplete. Low = External EEPROM load successful and complete. When in SMBus slave mode (EN_SMB = 1), this output will be high-Z until READ_EN_N is driven low, at which point ALL_DONE_N will be driven low. This behavior allows the reset signal connected to READ_EN_N of one device to propagate to the subsequent devices when ALL_DONE_N is connected to READ_EN_N in an SMBus slave mode application.
EN_SMB	E3	Input, 4-Level	4-level 2.5 V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 kΩ to GND - RESERVED R: 10 kΩ to GND - RESERVED F: Float - SMBus master mode 1: 1 kΩ to VDD - SMBus slave mode

### Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
READ_EN_N	F13	Input, LVCMOS	Pin has weak pull-up. This pin is 3.3 V tolerant.  SMBus master mode (EN_SMB = Float): When asserted low, initiates the SMBus master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation.  SMBus slave mode (EN_SMB = 1): When asserted low, this causes the device to be held in reset (SMBus state machine reset and register reset). This pin should be pulled high or left floating for normal operation in SMBus slave mode.
SDA	E12	I/O, 3.3-V LVCMOS, Open Drain	SMBus data input or open drain output. External 2 - $\Omega$ to 5-k $\Omega$ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.
SDC	F12	I/O, 3.3-V LVCMOS, Open Drain	SMBus clock input or open drain clock output. External 2-k $\Omega$ to 5-k $\Omega$ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.
MISCELLANEOUS PINS			
INT_N	F3	No Connect	No connect on package. For applications using multiple repeaters and retimers, this pin should be connected to other devices' INT_N pins. This is only a recommendation for cases where there is a need to support a potential future upgrade to the pin-compatible retimer device, which uses this pin as an interrupt signal to a system controller.
TEST0	E2	Input, LVCMOS	Reserved test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin may be left floating, tied to GND, or connected to a 2.5-V (max) output.
TEST1	E14	Input, LVCMOS	
POWER			
GND	A1, A2, A4, A6, A8, A10, A12, A14, A15, B2, B4, B6, B8, B10, B12, B14, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, D1, D2, D4, D5, D7, D9, D11, D12, D14, D15, E4, E11, F1, F2, F4, F5, F7, F9, F11, F14, F15, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, H2, H4, H6, H8, H10, H12, H14, J1, J2, J4, J6, J8, J10, J12, J14, J15	Power	Ground reference. The GND pins on this device should be connected through a low-impedance path to the board GND plane.
VDD	D6, D8, D10, E5, E6, E7, E8, E9, E10, F6, F8, F10	Power	Power supply, VDD = 2.5 V $\pm$ 5%. Use at least six de-coupling capacitors between the Repeater's VDD plane and GND as close to the Repeater as possible. For example, four 0.1- $\mu$ F capacitors and two 1- $\mu$ F capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a low-resistance path to the board VDD plane. For more information, see <a href="#">Power Supply Recommendations</a> .

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). <sup>(1)</sup>

		MIN	MAX	UNIT
VDD <sub>ABSMAX</sub>	Supply voltage (VDD)	−0.5	2.75	V
VIO <sub>2.5V,ABSMAX</sub>	2.5 V I/O voltage (LVCMOS and CMOS)	−0.5	2.75	V
VIO <sub>3.3V,ABSMAX</sub>	Open drain and 3.3 V-tolerance I/O voltage (SDA, SDC, READ_EN_N)	−0.5	4	V
VIO <sub>HS,ABSMAX</sub>	High-speed I/O voltage (RXnP, RXnN, TXnP, TXnN)	−0.5	2.75	V
TJ <sub>ABSMAX</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	−40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

			MIN	NOM	MAX	UNIT
VDD	Supply voltage, VDD to GND	DC plus AC power should not exceed these limits	2.375	2.5	2.625	V
N <sub>VDD</sub>	Supply noise tolerance <sup>(1)</sup>	Supply noise, DC to <50 Hz, sinusoidal			250	mVpp
		Supply noise, 50 Hz to 10 MHz, sinusoidal			20	mVpp
		Supply noise, >10 MHz, sinusoidal			10	mVpp
T <sub>RampVDD</sub>	VDD supply ramp time	From 0 V to 2.375 V	150			μs
T <sub>J</sub>	Operating junction temperature		−40		110	C
T <sub>A</sub>	Operating ambient temperature		−40		85	C
VDD <sub>SMBUS</sub>	SMBus SDA and SDC Open Drain Termination Voltage	Supply voltage for open drain pull-up resistor			3.6	V
F <sub>SMBus</sub>	SMBus clock (SDC) frequency in SMBus slave mode				400	kHz

- (1) Sinusoidal noise is superimposed to supply voltage with negligible impact to device function or critical performance shown in the Electrical Table.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	CONDITIONS / ASSUMPTIONS	VALUE	UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	44.8	°C/W
	4-layer JEDEC board	26.8	
	10-layer 8-in x 6-in board	25.1	
	20-layer 8-in x 6-in board	25.4	

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>		CONDITIONS / ASSUMPTIONS	VALUE	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		28.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	4-layer JEDEC board	13.1	°C/W
		10-layer 8-in x 6-in board	13.1	
		20-layer 8-in x 6-in board	13.2	
		30-layer 8-in x 6-in board	13.2	
$\Psi_{JB}$	Junction-to-board characterization parameter	4-layer JEDEC board	25.4	°C/W
		10-layer 8-in x 6-in board	22.2	
		20-layer 8-in x 6-in board	21.8	
		30-layer 8-in x 6-in board	21.7	

## 6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER</b>						
$W_{channel}$	Power consumption per active channel	Channel enabled and in linear mode with maximum driver VOD (DRV_SEL_VOD = 3). Static power consumption not included.		82	97 <sup>(1)</sup>	mW
		Channel enabled and in linear mode with minimum driver VOD (DRV_SEL_VOD = 0). Static power consumption not included.		75	89 <sup>(1)</sup>	mW
$W_{channel\_FIR}$	Power consumption per active channel	Channel enabled and in FIR limiting mode with C0 = 31 and maximum driver VOD (DRV_SEL_VOD = 3). Static power consumption not included.		105	123 <sup>(1)</sup>	mW
		Channel enabled and in FIR limiting mode with C0 = 31 and minimum driver VOD (DRV_SEL_VOD = 0). Static power consumption not included.		97	115 <sup>(1)</sup>	mW
$W_{static\_total}$	Idle (static) mode total device power consumption	Channels disabled and powered down (DRV_PD = 1, EQ_PD = 1).		110	132 <sup>(1)</sup>	mW
$I_{total}$	Active mode total device supply current consumption	All channels enabled and in linear mode with maximum driver VOD (DRV_SEL_VOD = 3).		307	347	mA
		All channels enabled and in linear mode with minimum driver VOD (DRV_SEL_VOD = 0).		283	322	mA
$I_{total\_FIR}$	Active mode total device supply current consumption	All channels enabled and in FIR limiting mode with C0 = 31 and maximum driver VOD (DRV_SEL_VOD = 3).		380	426	mA
		All channels enabled and in FIR limiting mode with C0 = 31 and minimum driver VOD (DRV_SEL_VOD = 0).		355	401	mA
$I_{static\_total}$	Idle (static) mode total device supply current consumption	All channels disabled and powered down (DRV_PD = 1, EQ_PD = 1).		44	50	mA

(1) Max values assume VDD = 2.5 V + 5%.



## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS (CAL_CLK_IN, CAL_CLK_OUT, READ_EN_N, ALL_DONE_N, TEST[1:0])						
V <sub>IH</sub>	High level input voltage		1.75	VDD		V
		READ_EN_N pin only	1.75	3.6		V
V <sub>IL</sub>	Low level input voltage		GND	0.7		V
V <sub>OH</sub>	High level output voltage	IOH = 4 mA	2			V
V <sub>OL</sub>	Low level output voltage	IOL = −4 mA		0.4		V
I <sub>IH</sub>	Input high leakage current	Vinput = VDD, TEST[1:0] pins		16		μA
		Vinput = VDD, CAL_CLK_IN pin		66		μA
		Vinput = VDD, READ_EN_N pin <sup>(2)</sup>		1		μA
I <sub>IL</sub>	Input low leakage current	Vinput = 0 V, TEST[1:0] pins	−38			μA
		Vinput = 0 V, CAL_CLK_IN pin <sup>(3)</sup>	−1			μA
		Vinput = 0 V, READ_EN_N pin <sup>(2)</sup>	−55			μA
4-LEVEL LOGIC ELECTRICAL SPECIFICATIONS (APPLIES TO 4-LEVEL INPUT CONTROL PINS ADDR0, ADDR1, and EN_SMB)						
I <sub>IH</sub>	Input high leakage current			105		μA
I <sub>IL</sub>	Input low leakage current		−253			μA
V <sub>TH</sub>	High level (1) input voltage		0.95 × VDD			V
	Float level input voltage		0.67 × VDD			V
	10K to GND input voltage		0.33 × VDD			V
	Low level (0) input voltage		0.1			V
HIGH-SPEED DIFFERENTIAL INPUTS (RXnP, RXnN)						
BST	CTLE high-frequency boost	Measured with maximum CTLE setting and maximum BW setting (EQ_BST1 = 7, EQ_BST2 = 7, EQ_BW = 3). Boost is defined as the gain at 14 GHz relative to 20 MHz.		22.5		dB
		Measured with maximum CTLE setting and maximum BW setting (EQ_BST1 = 7, EQ_BST2 = 7, EQ_BW = 3). Boost is defined as the gain at 12.9 GHz relative to 20 MHz.		23		dB
BST	CTLE high-frequency boost	Measured with minimum CTLE setting and minimum BW setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_BW = 0, EQ_EN_BYPASS = 1). Boost is defined as the gain at 14 Ghz relative to 20 MHz.		0.5		dB
		Measured with minimum CTLE setting and minimum BW setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_BW = 0, EQ_EN_BYPASS = 1). Boost is defined as the gain at 12.9 Ghz relative to 20 MHz.		1		dB

(2) This pin has an internal weak pull-up.

(3) This pin has an internal weak pull-down.



## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BST <sub>delta</sub> CTLE high-frequency gain variation	Measured with maximum CTLE setting (EQ_BST1 = 7, EQ_BST2 = 7). Gain variation is defined as the total change in gain at 14 GHz due to temperature and voltage variation.		< 3		dB
	Measured with maximum CTLE setting (EQ_BST1 = 7, EQ_BST2 = 7). Gain variation is defined as the total change in gain at 12.9 GHz due to temperature and voltage variation.		< 3		dB
BST <sub>delta</sub> CTLE high-frequency gain variation	Measured with minimum CTLE setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_EN_BYPASS = 1). Gain variation is defined as the total change in gain at 14 GHz due to temperature and voltage variation.		< 2		dB
	Measured with minimum CTLE setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_EN_BYPASS = 1). Gain variation is defined as the total change in gain at 12.9 GHz due to temperature and voltage variation.		< 2		dB
RL <sub>SDD11</sub> Input differential return loss	50 MHz to 3.7 GHz		< -12		dB
	3.7 GHz to 10 GHz		< -10		dB
	10 GHz to 14.1 GHz		< -8		dB
	14.1 GHz to 20 GHz		< -6		dB
RL <sub>SDC11</sub> Input differential-to-common-mode return loss	100 MHz to 3.3 GHz		< -35		dB
	3.3 GHz to 12.9 GHz		< -26		dB
	12.9 GHz to 20 GHz		< -22		dB
RL <sub>SCC11</sub> Input common-mode return loss	100 MHz to 10 GHz		< -7		dB
	10 GHz to 20 GHz		< -7		dB
V <sub>SDAT</sub> AC signal detect assert (ON) differential voltage threshold level	Minimum input peak-to-peak amplitude level at device pins required to assert signal detect. 25.78125 Gbps with PRBS7 pattern and 20 dB loss channel.		196		mVpp
V <sub>SDDT</sub> AC signal detect de-assert (OFF) differential voltage threshold level	Maximum input peak-to-peak amplitude level at device pins which causes signal detect to de-assert. 25.78125 Gbps with PRBS7 pattern and 20 dB loss channel.		147		mVpp

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VID <sub>linear</sub>	Input amplitude linear range. The maximum VID for which the repeater remains linear, defined as ≤1 dB compression of Vout/Vin.	Measured with the highest wide-band gain setting (EQ_HIGH_GAIN = 1, DRV_SEL_VOD = 3). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		850		mVpp
		Measured with a mid wide-band gain setting (EQ_HIGH_GAIN = 1, DRV_SEL_VOD = 0). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		900		mVpp
		Measured with a mid wide-band gain setting (EQ_HIGH_GAIN = 0, DRV_SEL_VOD = 3). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		1050		mVpp
		Measured with the lowest wide-band gain setting (EQ_HIGH_GAIN = 0, DRV_SEL_VOD = 0). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		1250		mVpp
HIGH-SPEED DIFFERENTIAL OUTPUTS (TXnP, TXnN)						
PRE <sub>DEM-MAX</sub>	Maximum pre-cursor de-emphasis in FIR limiting mode	Measured with an 16T pattern at 28.125 Gbps using C(0), Reg_0x0B[4:0], set to 0x0C, C(-1), Reg_0x0D[3:0], set to 0xF, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1.		-11		dB
PST <sub>DEM-MAX</sub>	Maximum post-cursor de-emphasis in FIR limiting mode	Measured with an 16T pattern at 28.125 Gbps using C(0), Reg_0x0B[4:0], set to 0x0C, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0xF. TX drv_sel_fir, Reg_0x06[0], set to 0x1.		-11		dB
T <sub>PRE</sub>	Pre-cursor FIR tap delay in FIR limiting mode	Independent of data rate		28		ps
T <sub>PST</sub>	Post-cursor FIR tap delay in FIR limiting mode	Independent of data rate		25		ps
VOD <sub>LIM-MIN</sub>	Minimum differential output amplitude in FIR limiting mode	Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x00, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x0.		185		mVpp
		Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x00, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x3.		360		mVpp

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOD <sub>LIM-MAX</sub>	Maximum differential output amplitude in FIR limiting mode		705		mVpp
	Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x1F, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x0.				
	Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x1F, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x3.		1260		mVpp
VOD <sub>idle</sub>	Differential output amplitude, TX disabled or otherwise muted		< 10		mVpp
G <sub>DC</sub>	Vout/Vin wide-band amplitude gain in linear mode		4.5		dB
	Measured with the highest wide-band gain setting (EQ_HIGH_GAIN = 1, DRV_SEL_VOD = 3) at 20 MHz.				
	Measured with the lowest wide-band gain setting (EQ_HIGH_GAIN = 0, DRV_SEL_VOD = 0) at 20 MHz.		–5		
V <sub>cm-TX-AC</sub>	Common-mode AC output noise		6		mV, RMS
RJ <sub>ADD-RMS</sub>	Additive random jitter		11		fs RMS
RL <sub>SDD22</sub>	Output differential-to-differential return loss	50 MHz to 4.8 GHz	< –12		dB
		4.8 GHz to 10 GHz	< –11		
		10 GHz to 14.1 GHz	< –7		
		14.1 GHz to 20 GHz	< –6		
RL <sub>SCD22</sub>	Output common-mode-to-differential return loss	50 MHz to 6.0 GHz	< –21		dB
		6.0 GHz to 12.9 GHz	< –22		
		12.9 GHz to 14.1 GHz	< –21		
		14.1 GHz to 20 GHz	< –20		
RL <sub>SCC22</sub>	Output common-mode return loss	50 MHz to 3.3 GHz	< –13		dB
		3.3 GHz to 10.3 GHz	< –11		
		10.3 GHz to 20 GHz	< –8		
t <sub>r</sub> , t <sub>f</sub>	Transition time (20%-80%) in FIR limiting mode	Measured at 28.125 Gbps with 16T data pattern using C(0), Reg_0x0B[4:0], set to 0x00, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1.	19.9		ps
		Measured at 28.125 Gbps with 16T data pattern using C(0), Reg_0x0B[4:0], set to 0x1F, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1.	25.8		ps

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OTHER PARAMETERS</b>						
$t_D$	Input-to-output latency (propagation delay) through a channel	Linear mode		100		ps
$t_D$	Input-to-output latency (propagation delay) through a channel	FIR limiting mode, Reg_0x06[0]=1		160		ps
$t_{SK}$	Channel-to-channel interpair skew	Latency difference between channels		<14		ps
$T_{EEPROM}$	EEPROM configuration load time	Time to assert ALL_DONE_N after REAN_EN_N has been asserted. Single device reading its configuration from an EEPROM with common channel configuration. This time scales with the number of devices reading from the same EEPROM. Does not include power-on reset time.			4	ms
		Time to assert ALL_DONE_N after REAN_EN_N has been asserted. Single device reading its configuration from an EEPROM. Non-common channel configuration. This time scales with the number of devices reading from the same EEPROM. Does not include power-on reset time.			7	
$T_{POR}$	Power-on reset assertion time	Internal power-on reset (PoR) stretch between stable power supply and de-assertion of internal PoR. The SMBus address is latched on the completion of the PoR stretch, and SMBus accesses are permitted once PoR completes.			60	ms

## 6.6 Electrical Characteristics -- Serial Management Bus Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	Input high level voltage	SDA and SDC	1.75		3.6	V
$V_{IL}$	Input low level voltage	SDA and SDC	GND		0.8	V
$V_{OL}$	Output low level voltage	SDA and SDC, $I_{OL} = 1.25$ mA	GND		0.4	V
$C_{IN}$	Input pin capacitance	SDA and SDC		15		pF
$I_{IN}$	Input current	SDA or SDC, $V_{INPUT} = V_{IN}, V_{DD},$ GND	-18		18	$\mu$ A

## 6.7 Timing Requirements -- Serial Management Bus Interface

Over operating free-air temperature range (unless otherwise noted).

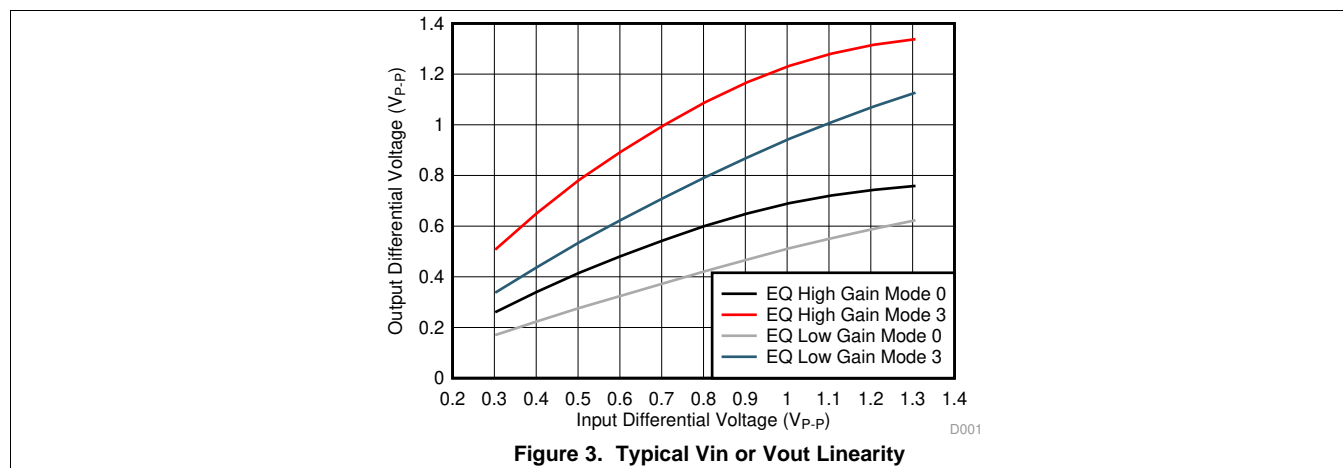
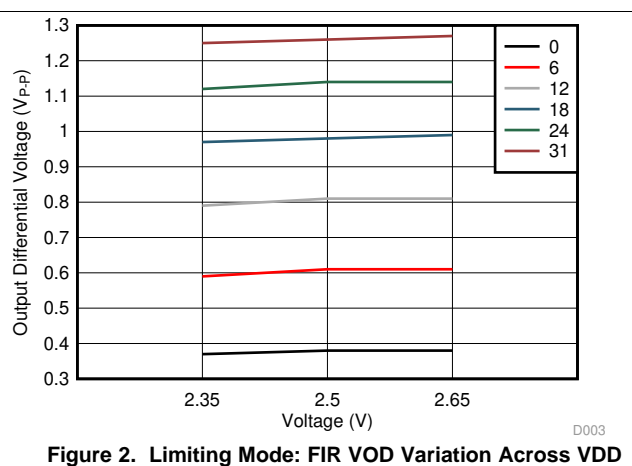
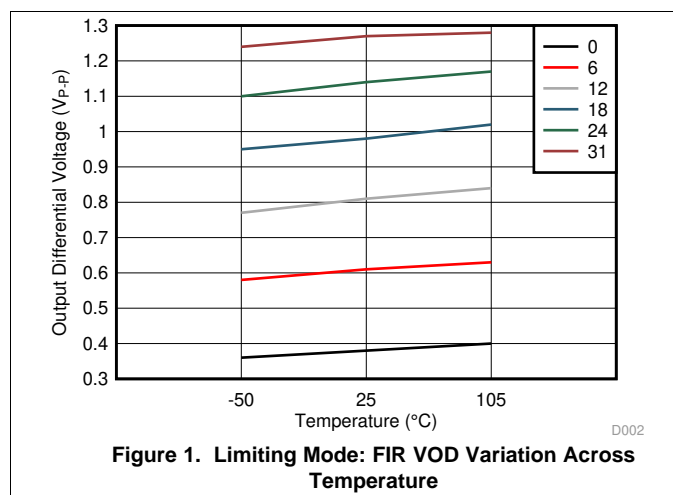
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RECOMMENDED SMBus SWITCHING CHARACTERISTICS (SMBus SLAVE MODE)</b>						
$f_{SDC}$	SDC clock frequency	EN_SMB = 1 k to VDD (Slave Mode)	10	100	400	kHz
$T_{SDA-HD}$	Data hold time			0.75		ns
$T_{SDA-SU}$	Data setup time			100		ns
$T_{SDA-R}$	SDA rise time, read operation	Pull-up resistor = 1 k $\Omega$ , Cb = 50 pF		150		ns
$T_{SDA-F}$	SDA fall time, read operation	Pull-up resistor = 1 k $\Omega$ , Cb = 50 pF		4.5		ns
<b>SMBus SWITCHING CHARACTERISTICS (SMBus MASTER MODE)</b>						
$f_{SDC}$	SDC clock frequency	EN_SMB = Float (Master Mode)	260	303	346	kHz
$T_{SDC-LOW}$	SDC low period		1.66	1.90	2.21	$\mu$ s
$T_{SDC-HIGH}$	SDC high period		1.22	1.40	1.63	$\mu$ s
$T_{HD-START}$	Hold time start operation			0.6		$\mu$ s

## Timing Requirements -- Serial Management Bus Interface (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SU-START}$	Setup time start operation		0.6		$\mu s$
$T_{SDA-HD}$	Data hold time		0.9		$\mu s$
$T_{SDA-SU}$	Data setup time		0.1		$\mu s$
$T_{SU-STOP}$	Stop condition setup time		0.6		$\mu s$
$T_{BUF}$	Bus free time between Stop-Start		1.3		$\mu s$
$T_{SDC-R}$	SDC rise time	Pull-up resistor = 1 k $\Omega$	300		ns
$T_{SDC-F}$	SDFC fall time	Pull-up resistor = 1 k $\Omega$	300		ns

## 6.8 Typical Characteristics



## 7 Detailed Description

### 7.1 Overview

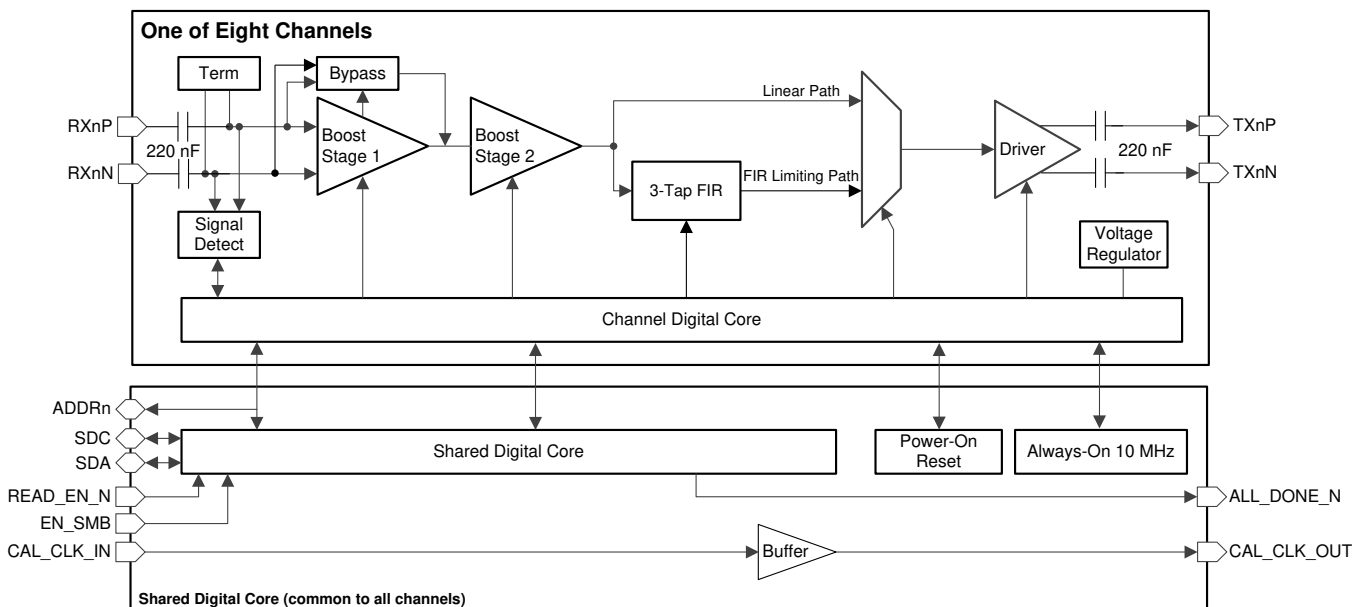
The DS280BR810 is an eight-channel multi-rate linear repeater with integrated signal conditioning. The eight channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE), an optional FIR filter and a linear output driver, which compensate for the presence of a dispersive transmission channel between the source transmitter and the final receiver.

All transmit and receive channels on the DS280BR810 are AC-coupled with physical AC coupling capacitors (220 nF  $\pm 20\%$ ) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.

The DS280BR810 is configurable through a single SMBus port. The DS280BR810 can also act as an SMBus master to configure itself from an EEPROM.

The sections which follow describe the functionality of various circuits and features within the DS280BR810. For more information about how to program or operate these features, consult the DS280BR810 Programming Guide.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Device Data Path Operation

The DS280BR810 data path consists of several key blocks as shown in [Functional Block Diagram](#). These key circuits are:

- AC-coupled Receiver and Transmitter
- Signal Detect
- 2-stage CTLE
- Driver DC Gain Control
- FIR Filter
- Data path Mux

## Feature Description (continued)

### 7.3.2 AC-Coupled Receiver and Transmitter

The differential receiver for each DS280BR810 channel contains an integrated on die 100  $\Omega$  differential termination as well as 220 nF AC coupling capacitors embedded onto the package substrate. The differential transmitter for each DS280BR810 channel also has 220 nF  $\pm 20\%$  AC coupling capacitors embedded on the package substrate.

### 7.3.3 Signal Detect

Each DS280BR810 high speed receiver has a signal detect circuit which monitors the energy level on the inputs. The signal detect circuit will enable the high-speed data path if a signal is detected, or power it off if no signal is detected. By default, this feature is enabled, but can be manually controlled through the SMBus channel registers. This can be useful if it is desired to manually force channels to be disabled. For information on how to manually operate the signal detect circuit refer to the DS280BR810 Programming Guide.

### 7.3.4 2-Stage CTLE

The continuous-time linear equalizer (CTLE) in the DS280BR810 consists of two stages which are configurable through the SMBus channel registers. This CTLE is designed to be highly linear to allow the DS280BR810 to preserve the transmitter's pre-cursor and post cursor signal characteristics. This highly linear behavior enables the DS280BR810 to be used in applications that use protocols such as link training, where it is important to recover and pass through incremental changes in transmit equalization.

Each stage in the CTLE has 3-bit boost control. The first CTLE stage provides a coarse adjustment of the total boost. Larger settings correspond to higher total boost. The first stage can be bypassed entirely to achieve the lowest possible total boost. The second CTLE stage acts as a fine adjustment on the total boost and impacts the shape of the boost curve accordingly. Larger settings correspond to higher total boost. The bandwidth of the CTLE can be adjusted using a 2-bit bandwidth control. Larger settings correspond to higher total bandwidth. For information on how to program the CTLE refer to the DS280BR810 Programming Guide.

In addition to high-frequency boost, the CTLE can apply wide-band amplitude gain. There are two settings (high-gain and low-gain) which work together with the driver DC gain control to affect the total input-to-output wide-band amplitude gain.

### 7.3.5 Driver DC Gain Control

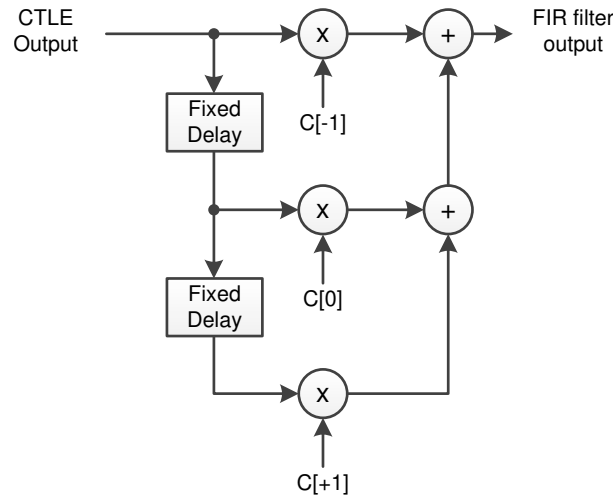
In addition to the high-frequency boost provided by the CTLE, the DS280BR810 is also able to provide additional DC or low-frequency gain. The effective DC gain is controlled by a 3-bit field, allowing for eight levels of DC attenuation or DC gain. For information on how to configure the DC gain refer to the DS280BR810 Programming Guide.

### 7.3.6 FIR Filter (Limiting Mode)

The DS280BR810 has an optional limiting mode with a fixed-delay 3-tap finite impulse response (FIR) filter to provide transmit equalization. This FIR can be configured to apply pre-cursor and post-cursor boost to the high speed signal. The FIR filter also allows for main cursor amplitude control. The tap polarities in the FIR filter are fixed to allow for pre-cursor or post-cursor boost to be applied to the signal.



## Feature Description (continued)



**Figure 4. 3-Tap FIR Filter Block Diagram**

Linear mode is recommended for the majority of applications, especially those which require Link Training. Common protocols such as 100 GbE and 40 GbE CR4/KR4, 50 GbE and 25GbE CR, 10 GbE KR, InfiniBand EDR, and others require Link Training. Linear mode is required for Link Training so that the ASIC transmitter precursor and post-cursor coefficients can propagate through the DS280BR810 in a transparent fashion. For applications which do not utilize Link Training, limiting mode may be used to provide output pre-cursor and post-cursor equalization for the purpose of improving the far-end eye opening. If the downstream receiver SerDes uses a decision feedback equalizer (DFE) to equalize the signal, the linear mode may be preferable to the limiting mode. DFE circuits often perform best when operating on a linear signal.

### 7.3.7 Configurable SMBus Address

The DS280BR810's SMBus slave address is strapped at power up using the ADDR[1:0] pins. The pin state is read on power up, after the internal power-on reset completes. The ADDR[1:0] pins are four-level LVCMOS IOs, which provide for 16 unique SMBus addresses. [Table 1](#) lists the DS280BR810 SMBus slave address options.

**Table 1. SMBus Address Map**

7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	REQUIRED ADDRESS PIN STRAP VALUE	
		ADDR1	ADDR0
0x18	0x30	0	0
0x19	0x32	0	R
0x1A	0x34	0	F
0x1B	0x36	0	1
0x1C	0x38	R	0
0x1D	0x3A	R	R
0x1E	0x3C	R	F
0x1F	0x3E	R	1
0x20	0x40	F	0
0x21	0x42	F	R
0x22	0x44	F	F
0x23	0x46	F	1
0x24	0x48	1	0
0x25	0x4A	1	R
0x26	0x4C	1	F
0x27	0x4E	1	1

## 7.4 Device Functional Modes

### 7.4.1 SMBus Slave Mode Configuration

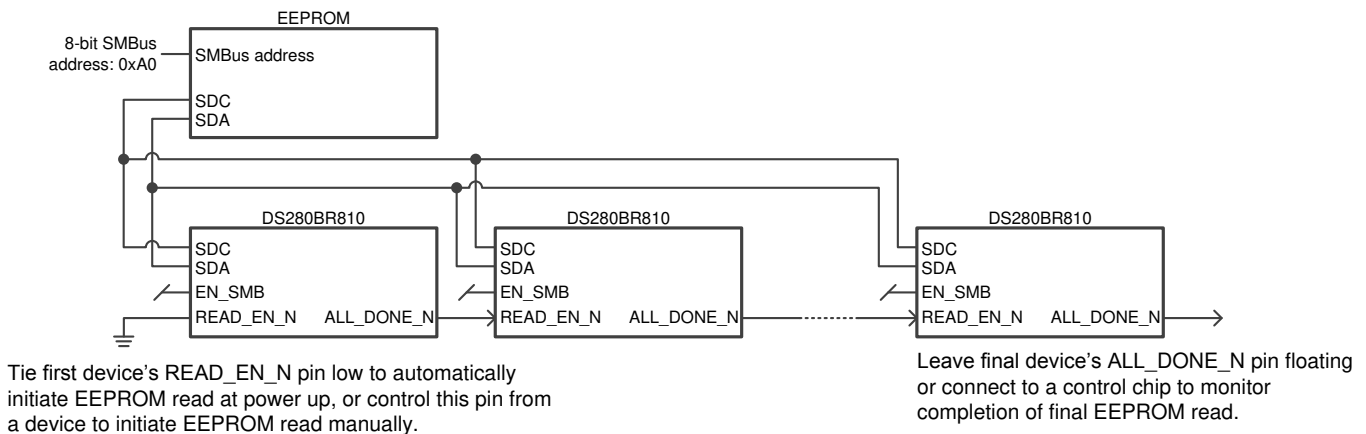
To configure the DS280BR810 for SMBus slave mode connect the EN\_SMB pin to VDD with a 1 kΩ resistor. When the DS280BR810 is configured for SMBus slave mode operation the READ\_EN\_N becomes an active-low reset pin, resetting register values when driven to LOW, or  $V_{IL}$ . Additionally, when the DS280BR810 is configured for SMBus slave mode the ALL\_DONE\_N output pin is high-Z; except for when READ\_EN\_N is driven LOW which causes ALL\_DONE\_N to also be driven LOW. Refer to [Register Maps](#) for additional register information.

### 7.4.2 SMBus Master Mode Configuration (EEPROM Self Load)

To configure the DS280BR810 for SMBus master mode, leave the EN\_SMB pin floating (no connect). If the DS280BR810 is configured for SMBus master mode, it will remain in the SMBus IDLE state until the READ\_EN\_N pin is asserted to LOW. Once the READ\_EN\_N pin is driven LOW, the DS280BR810 becomes an SMBus master and attempts to self-configure by reading device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the DS280BR810 has finished reading from the EEPROM successfully, it will drive the ALL\_DONE\_N pin LOW and then change from an SMBus master to an SMBus slave. Not all bits in the register map can be configured through an EEPROM load. Refer to the Programming Guide for more information.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- Maximum EEPROM size is 8 kb (1024 x 8-bit).
- Set EN\_SMB = FLOAT, configure for SMBus master mode.
- The external EEPROM device address byte must be 0xA0 and capable of 400 kHz operation at 2.5 V or 3.3 V supply.
- Configure the ADDR[1:0] inputs to select the SMBus slave address for the DS280BR810. Once the DS280BR810 completes its EEPROM load the device becomes a slave on the control bus.



**Figure 5. Example Daisy Chain for Multiple Device Single EEPROM Configuration**

When tying multiple DS280BR810 devices to the SDA and SDC bus, use these guidelines to configure the devices for SMBus master mode:

- Use SMBus ADDR[1:0] address bits so that each device can load its configuration from the EEPROM. The example below is for four devices. The first device in the sequence conventionally uses the 8-bit slave write address 0x30, while subsequent devices follow the address order listed below.
  - DS280BR810 instance 1 (U1): ADDR[1:0] = {0, 0} = 0x30
  - DS280BR810 instance 2 (U2): ADDR[1:0] = {0, R} = 0x32
  - DS280BR810 instance 3 (U3): ADDR[1:0] = {0, F} = 0x34
  - DS280BR810 instance 4 (U4): ADDR[1:0] = {0, 1} = 0x36
- Use a pull-up resistor on SDA and SDC; resistor value = 2 kΩ to 5 kΩ is adequate.
- Float (no connect) the EN\_SMB pin (E3) on all DS280BR810 devices to configure them for SMBus master mode. The EN\_SMB pin should not be dynamically changed between the high and float states.

## Device Functional Modes (continued)

- Daisy-chain READ\_EN\_N (pin F13) and ALL\_DONE\_N (pin D3) from one device to the next device in the following sequence so that they do not compete for master control of the EEPROM at the same time.
  1. Tie READ\_EN\_N of the first device in the chain (U1) to GND to trigger EEPROM read immediately after the DS280BR810 power-on reset (PoR) completes. Alternatively, drive the READ\_EN\_N pin from a control device (micro-controller or FPGA) to trigger the EEPROM read at a specific time.
  2. Tie ALL\_DONE\_N of U1 to READ\_EN\_N of U2
  3. Tie ALL\_DONE\_N of U2 to READ\_EN\_N of U3
  4. Tie ALL\_DONE\_N of U3 to READ\_EN\_N of U4
  5. Optional: Tie ALL\_DONE\_N output of U4 to a micro-controller or an LED to show the devices have been loaded successfully.

Once the ALL\_DONE\_N status pin of the last device is flagged to indicate that all devices sharing the SMBus line have been successfully programmed, control of the SMBus line is released by the DS280BR810. The device then reverts back to SMBus slave mode. At this point, an external MCU can perform any additional Read or Write operations to the DS280BR810.

Refer to the Programming Guide for additional information concerning SMBus master mode.

## 7.5 Programming

The DS280BR810 can be programmed in two ways. The DS280BR810 can be configured as an SMBus slave (EN\_SMB = HIGH) or the device can temporarily act as an SMBus master and load its configuration settings from an external EEPROM (EN\_SMB = FLOAT). Refer to [SMBus Slave Mode Configuration](#) and [SMBus Master Mode Configuration \(EEPROM Self Load\)](#) for details.

### 7.5.1 Transfer of Data with the SMBus Interface

The System Management Bus (SMBus) is a two-wire serial interface through which a master can communicate with various system components. Slave devices are identified by a unique device address. The two-wire serial interface consists of SDC and SDA signals. SDC is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The DS280BR810 SMBus, SDC, and SDA signals are open drain and require external pull-up resistors.

#### Start and Stop Conditions:

The master generates Start and Stop conditions at the beginning and end of each transaction:

- Start: High to LOW transition (falling edge) of SDA while SDC is HIGH.
- Stop: Low to HIGH transition (rising edge) of SDA while SDC is HIGH.

The master generates 9 clock pulses for each byte transfer. The 9th clock pulse constitutes the acknowledge (ACK) cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is when the device pulls SDA LOW, while a NACK (no acknowledge) is recorded if the line remains HIGH.

Writing data from a master to a slave consists of three parts:

- The master begins with a start condition followed by the slave device address with the R/W bit cleared.
- The master sends the 8-bit register address that will be written.
- The master sends the data byte to write for the selected register address. The register address pointer will then increment, so the master can send the data byte for the subsequent register without re-addressing the device, if desired. The final data byte to write should be followed by a stop condition.

SMBus read operations consist of four parts:

- The master initiates the read cycle with start condition followed by slave device address with the R/W bit cleared.
- The master sends the 8-bit register address that will be read.
- After acknowledgment from the slave, the master initiates a re-start condition.
- The slave device address is resent followed with R/W bit set.
- After acknowledgment from the slave, the data is read back from the slave to the master. The last ACK is HIGH if there are no more bytes to read.

## 7.6 Register Maps

Many of the registers in the DS280BR810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS280BR810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. This sequence is commonly referred to as Read-Modify-Write. If the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first.

Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.

Register bits can have the following interface constraints:

- R - Read only
- RW - Read/Write
- RWSC - Read/Write, Self-Clearing

### 7.6.1 Register Types: Global, Shared, and Channel

The DS280BR810 has 3 types of registers:

1. Global Registers - These registers can be accessed at any time and are used to select between individual channel registers and shared registers, or to read back the TI ID and version information.
2. Shared Registers - These registers are used for device-level configuration, status read back or control. Set register 0xFF[0] = 0 and configure 0xFF[5:4] to access the shared registers.
3. Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other. Set register 0xFF[0] = 1 and configure register 0xFC to access the desired channel register set.

Refer to the Programming Guide for additional information on register configuration.

### 7.6.2 Global Registers: Channel Selection and ID Information

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS280BR810 global registers are located at address 0xEF - 0xFF.

**Table 2. Global Register Map**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
0xEF		0x0C			General	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	1	R	N	DEVICE_ID_QUAD_CNT[3]	TI device ID (quad count). Contains 0x0C.
	2	1	R	N	DEVICE_ID_QUAD_CNT[2]	
	1	0	R	N	DEVICE_ID_QUAD_CNT[1]	
	0	0	R	N	DEVICE_ID_QUAD_CNT[0]	

## Register Maps (continued)

**Table 2. Global Register Map (continued)**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
<b>0xF0</b>		<b>0x00</b>			<b>Version Revision</b>	
	7	0	R	N	TYPE	TI version ID. Contains 0x00.
	6	0	R	N	VERSION[6]	
	5	0	R	N	VERSION[5]	
	4	0	R	N	VERSION[4]	
	3	0	R	N	VERSION[3]	
	2	0	R	N	VERSION[2]	
	1	0	R	N	VERSION[1]	
	0	0	R	N	VERSION[0]	
<b>0xF1</b>		<b>0x40</b>			<b>Channel Control</b>	
	7	0	R	N	DEVICE_ID[7]	TI device ID. Contains 0x40.
	6	1	R	N	DEVICE_ID[6]	
	5	0	R	N	DEVICE_ID[5]	
	4	0	R	N	DEVICE_ID[4]	
	3	0	R	N	DEVICE_ID[3]	
	2	0	R	N	DEVICE_ID[2]	
	1	0	R	N	DEVICE_ID[1]	
	0	0	R	N	DEVICE_ID[0]	
<b>0xF3</b>		<b>0x00</b>			<b>Channel Control</b>	
	7	0	R	N	CHAN_VERSION[3]	TI digital channel version ID. Contains 0x00.
	6	0	R	N	CHAN_VERSION[2]	
	5	0	R	N	CHAN_VERSION[1]	
	4	0	R	N	CHAN_VERSION[0]	
	3	0	R	N	SHARE_VERSION[3]	TI digital share version ID. Contains 0x00.
	2	0	R	N	SHARE_VERSION[2]	
	1	0	R	N	SHARE_VERSION[1]	
	0	0	R	N	SHARE_VERSION[0]	
<b>0xFC</b>		<b>0x00</b>			<b>General</b>	
	7	0	RW	N	EN_CH7	Select channel 7
	6	0	RW	N	EN_CH6	Select channel 6
	5	0	RW	N	EN_CH5	Select channel 5
	4	0	RW	N	EN_CH4	Select channel 4
	3	0	RW	N	EN_CH3	Select channel 3
	2	0	RW	N	EN_CH2	Select channel 2
	1	0	RW	N	EN_CH1	Select channel 1
	0	0	RW	N	EN_CH0	Select channel 0
<b>0xFD</b>		<b>0x00</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

## Register Maps (continued)

**Table 2. Global Register Map (continued)**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
<b>0xFE</b>		<b>0x03</b>			<b>Vendor ID</b>	
	7	0	R	N	VENDOR_ID[7]	TI vendor ID. Contains 0x03.
	6	0	R	N	VENDOR_ID[6]	
	5	0	R	N	VENDOR_ID[5]	
	4	0	R	N	VENDOR_ID[4]	
	3	0	R	N	VENDOR_ID[3]	
	2	0	R	N	VENDOR_ID[2]	
	1	1	R	N	VENDOR_ID[1]	
	0	1	R	N	VENDOR_ID[0]	
<b>0xFF</b>		<b>0x10</b>			<b>Channel Control</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	EN_SHARE_Q1	Select shared registers for Quad 1 (Channels 4-7).
	4	1	RW	N	EN_SHARE_Q0	Select shared registers for Quad 0 (Channels 0-3).
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	WRITE_ALL_CH	Allows customer to write to all channels as if they are the same, but only allows to read back from the channel specified in 0xFC and 0xFD. Note: EN_CH_SMB must be = 1 or else this function is invalid.
	0	0	RW	N	EN_CH_SMB	1: Enables SMBus access to the channels specified in register 0xFC. 0: The shared registers are selected, see 0xFF[5:4].

## 7.6.3 Shared Registers

**Table 3. Shared Register Map**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
<b>0x00</b>		<b>0x0C</b>			<b>General</b>	
	7	0	R	N	I <sup>2</sup> C_ADDR[3]	I <sup>2</sup> C strap observation. The device 7-bit slave address is 0x18 + I <sup>2</sup> C_ADDR[3:0].
	6	0	R	N	I <sup>2</sup> C_ADDR[2]	
	5	0	R	N	I <sup>2</sup> C_ADDR[1]	
	4	0	R	N	I <sup>2</sup> C_ADDR[0]	
	3	0	R	N	RESERVED	RESERVED
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
<b>0x01</b>		<b>0x00</b>			<b>Version Revision</b>	
	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
<b>0x02</b>		<b>0x00</b>			<b>Channel Control</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x03</b>		<b>0x00</b>			<b>Channel Control</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x04</b>		<b>0x01</b>			<b>General</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RWSC	N	RST_I <sup>2</sup> C_REGS	1: Reset shared registers, bit is self-clearing. 0: Normal operation
	5	0	RWSC	N	RST_I <sup>2</sup> C_MAS	1: Self-clearing reset for I <sup>2</sup> C master. 0: Normal operation
	4	0	RW	N	FRC_EEPRM_RD	1: Override EN_SMB and input chain status to force EEPROM Configuration. 0: Normal operation
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	REGS_CLOCK_EN	RESERVED
	1	0	RW	N	I <sup>2</sup> C_MAS_CLK_EN	RESERVED
	0	1	RW	N	I <sup>2</sup> CSLV_CLK_EN	RESERVED



**Table 3. Shared Register Map (continued)**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
<b>0x05</b>		<b>0x00</b>			<b>General</b>	
	7	0	RW	N	DISAB_EEPRM_CFG	1: Disable Master Mode EEPROM Configuration (If not started, not effective midway or after configuration). 0: Normal operation
	6	0	RW	N	CRC_EN	RESERVED
	5	0	RW	N	ML_TEST_CONTROL	RESERVED
	4	0	R	N	EEPROM_READING_DONE	Sets 1 when EEPROM reading done.
	3	0	R	N	RESERVED	RESERVED
	2	0	R	Y	CAL_CLK_INV_DIS	1: Disable the inversion of CAL_CLK_OUT. 0: Normal operation, CAL_CLK_OUT is inverted with respect to CAL_CLK_IN.
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	TEST0_AS_CAL_CLK	RESERVED
<b>0x06</b>		<b>0x00</b>			<b>General</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x07</b>		<b>0x00</b>			<b>General</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	R	N	CAL_CLK_DET	1: Indicates that CAL_CLK has been detected. 0: Indicates that CAL_CLK has not been detected.
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	MR_CAL_CLK_DET_DIS	1: Disable CAL_CLK detect. 0: Enable CAL_CLK detect.
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	Y	DIS_CAL_CLK_OUT	1: Disable CAL_CLK_OUT, output is high-Z. 0: Enable CAL_CLK_OUT.
<b>0x08</b>		<b>0x00</b>			<b>General</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x09</b>		<b>0x00</b>			<b>General</b>	
	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED

**Table 3. Shared Register Map (continued)**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
<b>0x0A</b>		<b>0x00</b>			<b>General</b>	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
<b>0x0B</b>		<b>0x00</b>				
	7	0	R	N	EECFG_CMPLT	11: Not valid. 10: EEPROM load completed successfully.
	6	0	R	N	EECFG_FAIL	01: EEPROM load failed after 64 attempts. 00: EEPROM load in progress.
	5	0	R	N	EECFG_ATMPT[5]	Indicates number of attempts made to load EEPROM image.
	4	0	R	N	EECFG_ATMPT[4]	
	3	0	R	N	EECFG_ATMPT[3]	
	2	0	R	N	EECFG_ATMPT[2]	
	1	0	R	N	EECFG_ATMPT[1]	
	0	0	R	N	EECFG_ATMPT[0]	
<b>0x0C</b>		<b>0x91</b>				
	7	1	RW	N	I <sup>2</sup> C_FAST	1: EEPROM load uses Fast I <sup>2</sup> C Mode (400 kHz). 0: EEPROM load uses Standard I <sup>2</sup> C Mode (100 kHz).
	6	0	RW	N	I <sup>2</sup> C_SDA_HOLD[2]	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SDC input. Units are 100 ns.
	5	0	RW	N	I <sup>2</sup> C_SDA_HOLD[1]	
	4	1	RW	N	I <sup>2</sup> C_SDA_HOLD[0]	
	3	0	RW	N	I <sup>2</sup> C_FLTR_DEPTH[3]	I <sup>2</sup> C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SDC and SDA inputs that will be rejected. Units are 100 ns.
	2	0	RW	N	I <sup>2</sup> C_FLTR_DEPTH[2]	
	1	0	RW	N	I <sup>2</sup> C_FLTR_DEPTH[1]	
	0	1	RW	N	I <sup>2</sup> C_FLTR_DEPTH[0]	

## 7.6.4 Channel Registers

**Table 4. Channel Register Map**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
<b>0x00</b>		<b>0x00</b>			<b>General</b>	
	7	0	RW	N	CLK_CORE_DISAB	1: Disables 10 M core clock. This is the main clock domain for all the state machines. 0: Normal operation
	6	0	RW	N	CLK_REGS_EN	1: Force enable the clock to the registers. Normally, the register clock is enabled automatically on a needed basis. 0: Normal operation
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	CLK_REF_DISAB	1: Disables the 25 MHz CAL_CLK domain. 0: Normal operation
	3	0	RW	N	RST_CORE	1: Reset the 10 M core clock domain. This is the main clock domain for all the state machines. 0: Normal operation
	2	0	RWSC	N	RST_REGS	1: Reset channel registers to power-up defaults. 0: Normal operation
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RST_CAL_CLK	1: Resets the 25 MHz reference clock domain. 0: Normal operation
<b>0x01</b>		<b>0x00</b>			<b>SIG_DET</b>	
	7	0	R	N	SIGDET	Signal detect status. 1: Signal detected at RX inputs. 0: No signal detected at RX inputs.
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
<b>0x02</b>		<b>0x00</b>				
	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x03</b>		<b>0x80</b>			<b>CTLE_BOOST</b>	
	7	1	RW	Y	EQ_BW[1]	EQ stage one buffer current (strength) control. Impacts EQ bandwidth. 2'b11 yields highest bandwidth, 2'b00 yields lowest bandwidth. Refer to the Programming Guide for more information.
	6	0	RW	Y	EQ_BW[0]	
	5	0	RW	Y	EQ_BST2[2]	EQ boost stage 2 controls. Directly goes to analog. No override bit is needed. Refer to the Programming Guide for more information.
	4	0	RW	Y	EQ_BST2[1]	
	3	0	RW	Y	EQ_BST2[0]	
	2	0	RW	Y	EQ_BST1[2]	EQ boost stage 1 controls. Directly goes to analog. No override bit is needed. Refer to the Programming Guide for more information.
	1	0	RW	Y	EQ_BST1[1]	
	0	0	RW	Y	EQ_BST1[0]	
<b>0x04</b>		<b>0x90</b>				
	7	1	RW	N	RESERVED	RESERVED
	6	0	RW	N	EQ_PD_SD	1: Power down signal detect 0: Normal operation

**Table 4. Channel Register Map (continued)**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	5	0	RW	Y	EQ_HIGH_GAIN	1: Enable EQ high gain 0: Enable EQ low gain
	4	1	RW	Y	EQ_EN_DC_OFF	RESERVED
	3	0	RW	Y	EQ_PD_EQ	1: Power down EQ 0: Enable EQ
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	Y	BG_SEL_IPP100[2]	CTLE bias programming. BG_SEL_IPP100[1:0] is in Reg_0x0F[5:4].
	0	0	RW	Y	EQ_EN_BYPASS	1: Enable EQ bypass 0: Normal operation, signal travels through EQ.
<b>0x05</b>		<b>0x04</b>			<b>SIG_DET_CONFIG</b>	
	7	0	RW	Y	EQ_SD_PRESET	1: Force signal detect result to 1 0: Normal operation This bit should not be set if 0x05[6] is also set.
	6	0	RW	Y	EQ_SD_RESET	1: Force signal detect result to 0 0: Normal operation This bit should not be set if 0x05[7] is also set.
	5	0	RW	Y	EQ_REFA_SEL[1]	Signal detect assert thresholds. Refer to the Programming Guide for more information.
	4	0	RW	Y	EQ_REFA_SEL[0]	
	3	0	RW	Y	EQ_REFD_SEL[1]	Signal detect de-assert thresholds. Refer to the Programming Guide for more information.
	2	1	RW	Y	EQ_REFD_SEL[0]	
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x06</b>		<b>0xC0</b>			<b>GPIO2 Config</b>	
	7	1	RW	Y	DRV_SEL_VOD[1]	Driver VOD adjust (DC gain), applicable to both linear and FIR limiting mode. Refer to the Programming Guide for more information.
	6	1	RW	Y	DRV_SEL_VOD[0]	
	5	0	RW	Y	DRV_EQ_PD_OV	1: Driver and equalizer power down manually with Reg_0x06[3] and Reg_0x04[3], respectively. 0: Driver and equalizer are powered down/up by default when LOS=1/0.
	4	0	RW	Y	DRV_SEL_MUTE_OV	Driver mute override: 1: Use register 0x06[1] for mute control. 0: Normal operation. Mute is automatically controlled by signal detect.
	3	0	RW	Y	DRV_PD	1: Power down the driver. 0: Normal operation, driver power on or off is controlled by signal detect.
	2	0	RW	Y	DRV_PD_CM_LOOP	1: Disable the driver's common mode loop control circuit. 0: Normal operation, common mode loop enabled.
	1	0	RW	Y	DRV_SEL_MUTE	1: Mute driver if override bit is enabled. 0: Normal operation
	0	0	RW	Y	DRV_SEL_FIR	Linear versus Limiting Mode select. Refer to the Programming Guide for more information. 1: Enable Limiting FIR mode. 0: Enable Linear mode (disable limiting FIR).
<b>0x07</b>		<b>0x20</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	1	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x08</b>		<b>0x54</b>				
	7	0	RW	Y	RESERVED	RESERVED

**Table 4. Channel Register Map (continued)**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	6	1	RW	Y	RESERVED	RESERVED
	5	0	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	BG_SEL_IPTAT25	1: Increases the current to the CTLE by 5%. 0: Default
	2	1	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x09</b>		<b>0x00</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x0A</b>		<b>0x30</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	Y	RESERVED	RESERVED
	5	1	RW	Y	SD_REF_HIGH	Signal detect threshold controls: 11: Normal operation 10: Signal detect assert or de-assert thresholds reduced. 01: Signal detect assert or de-assert thresholds reduced. 00: Signal detect assert or de-assert thresholds reduced.
	4	1	RW	Y	SD_GAIN	
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x0B</b>		<b>0x1A</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	Y	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	1	RW	Y	FIR_MAIN[4]	FIR Limiting mode main-cursor control. Refer to the Programming Guide for more information.
	3	1	RW	Y	FIR_MAIN[3]	
	2	0	RW	Y	FIR_MAIN[2]	
	1	1	RW	Y	FIR_MAIN[1]	
	0	0	RW	Y	FIR_MAIN[0]	
<b>0x0C</b>		<b>0x40</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	Y	FIR_PST[3]	FIR Limiting mode post-cursor control. There is no sign bit for the post-cursor. The post-cursor always provides a high-pass filter effect. Refer to the Programming Guide for more information.
	2	0	RW	Y	FIR_PST[2]	
	1	0	RW	Y	FIR_PST[1]	
	0	0	RW	Y	FIR_PST[0]	
<b>0x0D</b>		<b>0x40</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED

**Table 4. Channel Register Map (continued)**

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	3	0	RW	Y	FIR_PRE[3]	FIR Limiting mode pre-cursor control. There is no sign bit for the pre-cursor. The pre-cursor always provides a high-pass filter effect. Refer to the Programming Guide for more information.
	2	0	RW	Y	FIR_PRE[2]	
	1	0	RW	Y	FIR_PRE[1]	
	0	0	RW	Y	FIR_PRE[0]	
<b>0x0E</b>		<b>0x00</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
<b>0x0F</b>		<b>0x00</b>				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	Y	BG_SEL_IPP100[1]	CTLE bias programming. BG_SEL_IPP100[2] is in Reg_0x04[1]. 000: 0% additional current (Default) 001: 5% additional current 010: 10% additional current 011: 15% additional current 100: 20% additional current 101: 25% additional current 110: 30% additional current 111: 35% additional current
	4	0	RW	Y	BG_SEL_IPP100[0]	
	3	0	RW	Y	BG_SEL_IPH200_v1[1]	
	2	0	RW	Y	BG_SEL_IPH200_v1[0]	
	1	0	RW	Y	BG_SEL_IPH200_v0[1]	Program driver bias current: 00: 0% additional current (Default) 01: 12.5% additional current 10: 25% additional current 11: 37.5% additional current
	0	0	RW	Y	BG_SEL_IPH200_v0[0]	

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

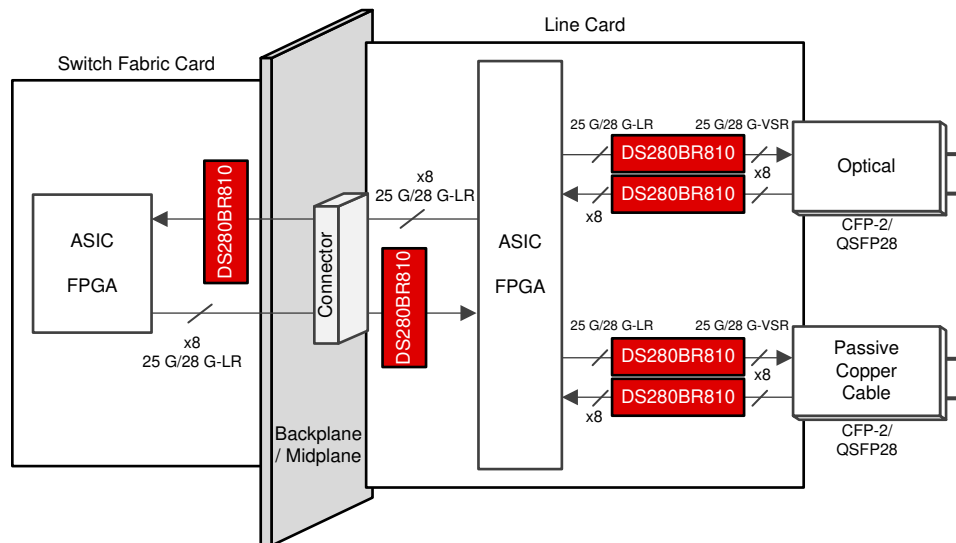
### 8.1 Application Information

The DS280BR810 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

### 8.2 Typical Application

The DS280BR810 is typically used in three main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port eye opening for copper and optical applications



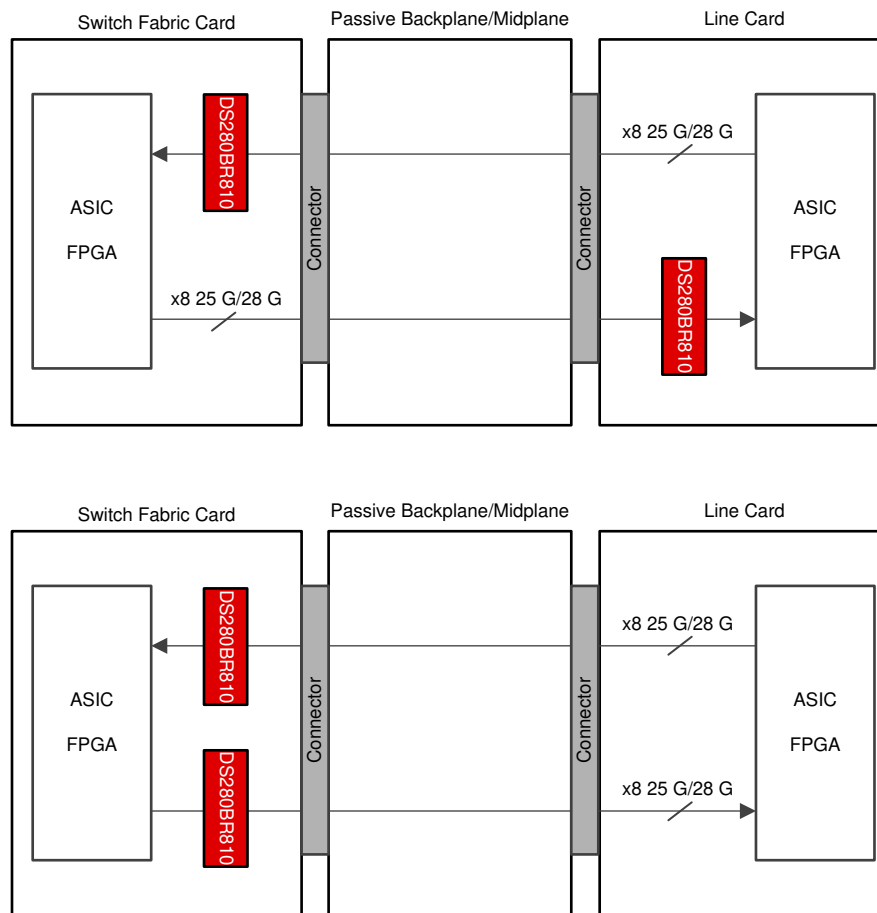
**Figure 6. Typical Application Diagram**

#### 8.2.1 Backplane and Mid-Plane Reach Extension

The DS280BR810 has strong equalization capabilities that allow it to equalize insertion loss and extend the reach of backplane channels by 15-20 dB beyond the normal capabilities of the ASICs operating over the channel. The DS280BR810 is designed to apply gain in a linear fashion. In most cases, the DS280BR810 should be placed with the higher loss channel segment at the input and the lower loss channel segment at the output (as shown in [Figure 7](#)); however, since the DS280BR810 operates in a linear fashion, it can also be used in applications where the lower loss channel segment is at the input and the higher loss channel segment is at the output (as shown in [Figure 7](#)).

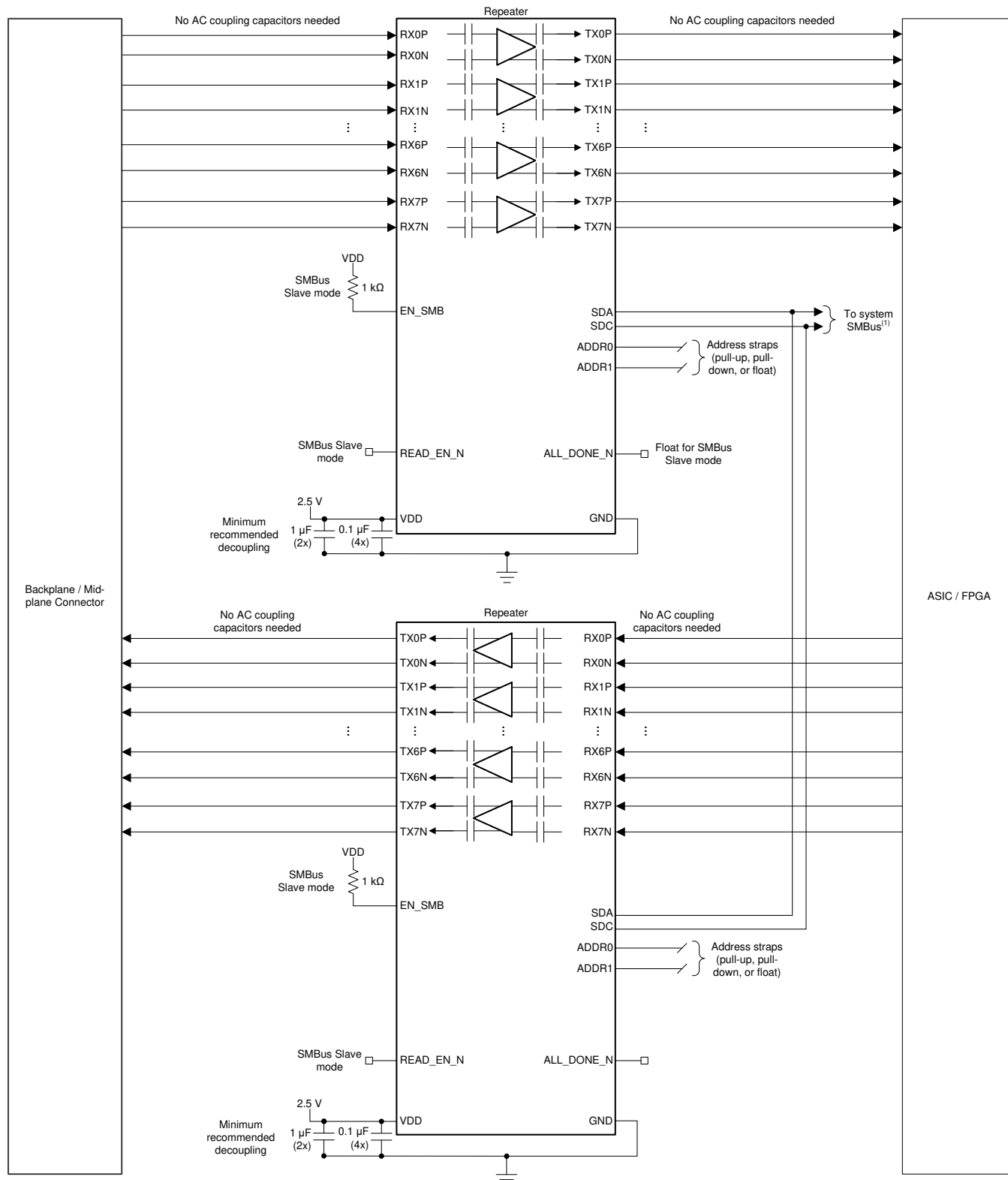


## Typical Application (continued)



**Figure 7. Typical Backplane and Mid-Plane Application Diagram**

## Typical Application (continued)



**Figure 8. Typical Backplane and Mid-Plane Schematic**

## Typical Application (continued)

### 8.2.1.1 Design Requirements

For backplane and mid-plane reach extension application, use the guidelines in the table below.

DESIGN PARAMETER	REQUIREMENT
AC Coupling Capacitors	Not required. 220 nF AC coupling capacitors are included in the device package on both the RX and TX side.
Input Channel Insertion Loss	$\geq 10$ dB at 14 GHz as a rough guideline. For best performance, the input channel insertion loss should be greater than or equal to the equalizer boost setting used in the DS280BR810.
Output Channel Insertion Loss	Depends on downstream ASIC and FPGA SerDes capabilities. Should be $\geq 5$ dB at 14 GHz as a rough guideline.
Total (Input + Output) Channel Insertion Loss	Depends on downstream ASIC and FPGA SerDes capabilities. The DS280BR810 can extend the reach between two ASICs by 15 to 20 dB beyond the ASICs' normal capabilities.
Link Partner TX Launch Amplitude	800 mV <sub>PP</sub> to 1200 mV <sub>PP</sub> differential
Link Partner TX FIR Filter	Depends on the channel loss.

### 8.2.1.2 Detailed Design Procedure

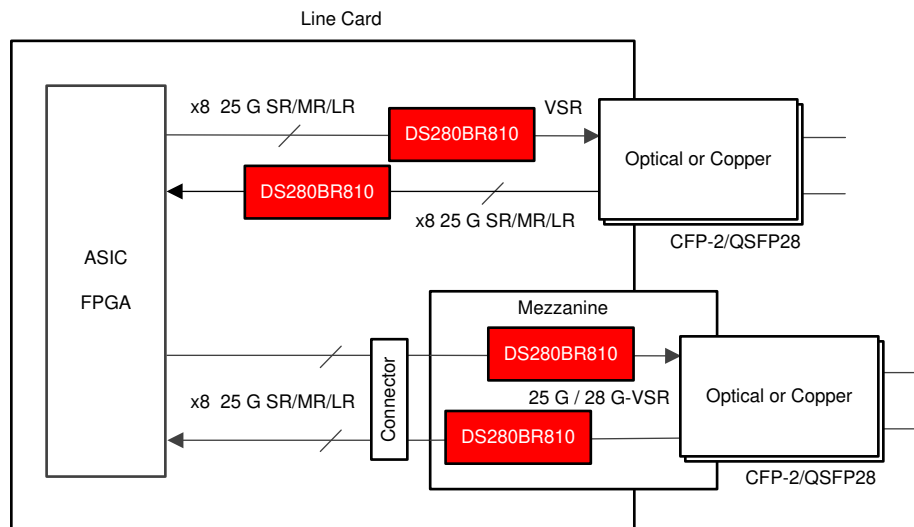
The design procedure for backplane and mid-plane applications is as follows:

1. Determine the total number of channels on the board which require a DS280BR810 for signal conditioning. This will dictate the total number of DS280BR810 devices required for the board. It is generally recommended that channels with similar total insertion loss on the board be grouped together in the same DS280BR810 device. This will simplify the device settings, as similar loss channels generally utilize similar settings.
2. Determine the maximum current draw required for all DS280BR810 devices. This may impact the selection of the regulator for the 2.5 V supply rail. To calculate the maximum current draw, multiply the maximum power supply current by the total number of DS280BR810 devices.
3. Determine the SMBus address scheme needed to uniquely address each DS280BR810 device on the board, depending on the total number of devices identified in step 1. Each DS280BR810 can be strapped with one of 16 unique SMBus addresses. If there are more DS280BR810 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I<sup>2</sup>C expander like the TCA/PCA family of I<sup>2</sup>C/SMBus switches and multiplexers to split the SMBus into multiple busses.
4. Determine if the device will be configured from EEPROM (SMBus master mode) or from the system SMBus (SMBus slave mode).
  - a. If SMBus master mode will be used, provisions should be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
  - b. If SMBus slave mode will be used for all device configurations, an EEPROM is not needed.
5. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to [Power Supply Recommendations](#) for more information.
6. If there is a need to potentially upgrade to a pin-compatible TI Retimer device, then make provisions in the schematic and layout for a 25 MHz ( $\pm 100$  ppm) single-ended CMOS clock. Each DS280BR810 buffers the clock on the CAL\_CLK\_IN pin and presents the buffered clock on the CAL\_CLK\_OUT pin. This allows multiple (up to 20) DS280BR810 calibration clocks to be daisy chained to avoid the need for multiple oscillators on the board. If the oscillator used on the board has a 2.5 V CMOS output, then no AC coupling capacitor or resistor ladder is required at the input to CAL\_CLK\_IN. No AC coupling or resistor ladder is needed between one DS280BR810 CAL\_CLK\_OUT output and the next DS280BR810's CAL\_CLK\_IN input. The final DS280BR810's CAL\_CLK\_OUT output can be left floating. A 25 MHz clock is not required for the DS280BR810, but it is good practice to provision for it in case there is a future plan to upgrade to a pin-compatible TI Retimer device.

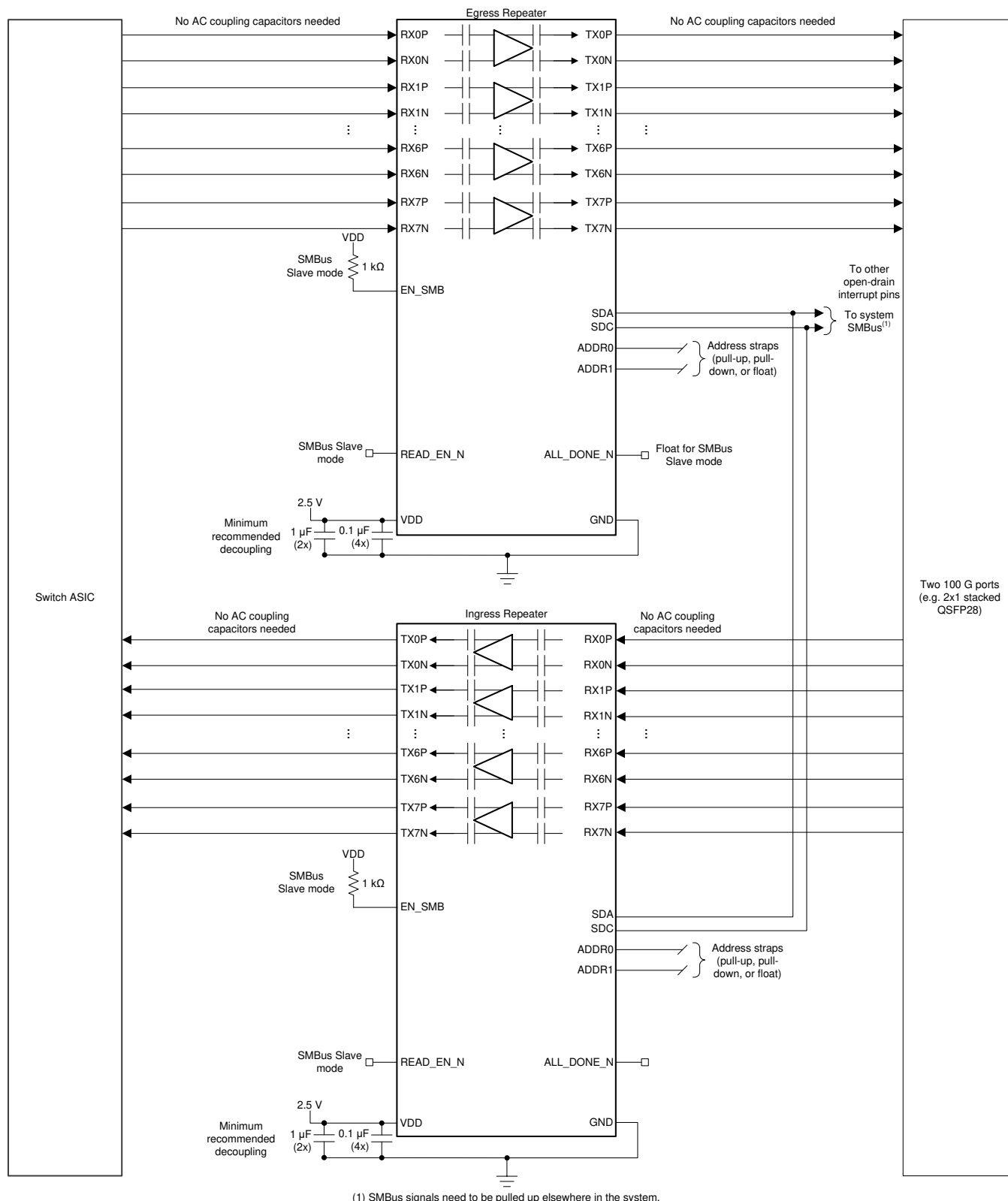
7. If there is a need to potentially upgrade to a pin-compatible TI Retimer device, then connect the INT\_N pin to an FPGA or CPU for interrupt monitoring. Note that multiple INT\_N outputs can be connected together. The common INT\_N net should be pulled high to 2.5 V or 3.3 V. The INT\_N pin on the DS280BR810 does not perform the interrupt functionality that the equivalent pin on the pin-compatible Retimer device does; however, it is good practice to provision for this in case there is a future plan to upgrade to a pin-compatible TI Retimer device.

### 8.2.2 Front-Port Applications

The DS280BR810 has strong equalization capabilities that allow it to equalize insertion loss and extend the reach of front-port channels by 15 dB beyond the normal capabilities of the ASIC while support CAUI-4 and CR4 electrical requirements. The DS280BR810 is designed to apply gain in a linear fashion in order to support longer distances between the switch ASIC and the front-port module. A single DS280BR810 can be used to support all eight *egress* channels or all eight *ingress* channels for two 100 GbE ports. [Figure 9](#) illustrates this configuration.



**Figure 9. Typical Front-Port Application Diagram**


**Figure 10. Typical Front-port Schematic**

### 8.2.2.1 Design Requirements

This section lists some critical areas for high speed printed circuit board design consideration and study.

DESIGN PARAMETER	REQUIREMENT
AC Coupling Capacitors	Not required. 220 nF AC coupling capacitors are included in the device package on both the RX and TX side.
Input Channel Insertion Loss	$\geq 10$ dB at 14 GHz as a <i>rough</i> guideline. For best performance, the input channel insertion loss should be greater than or equal to the equalizer boost setting used in the Repeater.
Output Channel Insertion Loss	For best performance in <i>egress</i> applications, place the Repeater close to the front-port cage. For best performance in <i>ingress</i> applications, place the Repeater with $\geq 5$ dB loss at 14 GHz between the output and the downstream ASIC.
Switch ASIC TX Launch Amplitude	600 mVppd to 1000 mVppd

### 8.2.2.2 Detailed Design Procedure

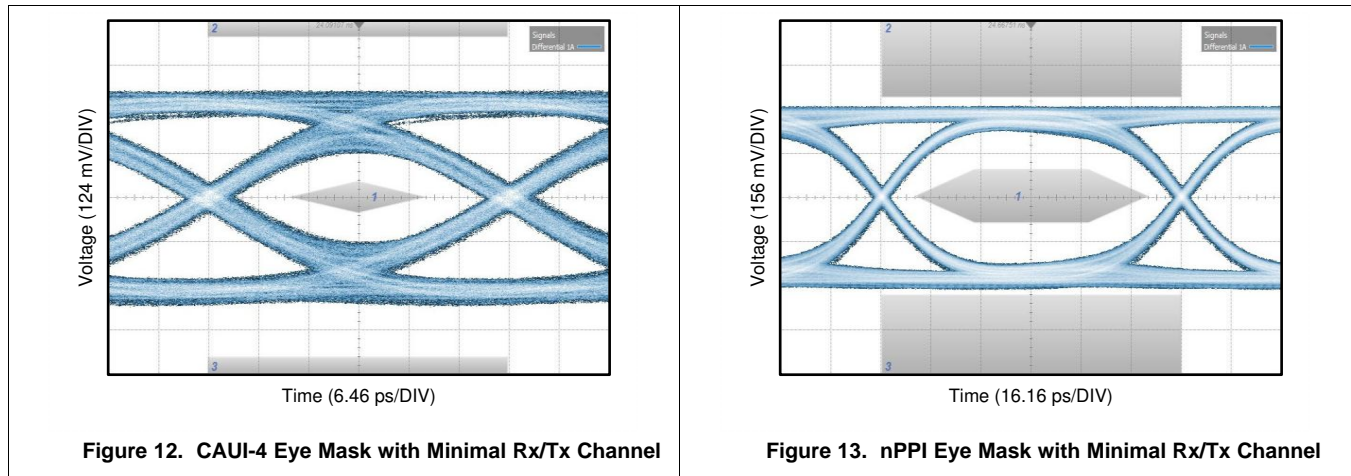
The design procedure for front-port applications is as follows:

1. Determine the total number of channels on the board which require a DS280BR810 for signal conditioning. This will dictate the total number of DS280BR810 devices required for the board. It is generally recommended that channels belonging to the same QSFP port be grouped together in the same DS280BR810 device. This will simplify the device settings, as similar loss channels generally utilize similar settings.
2. Determine the maximum current draw required for all DS280BR810 devices. This may impact the selection of the regulator for the 2.5 V supply rail. To calculate the maximum current draw, multiply the maximum power supply current by the total number of DS280BR810 devices.
3. Determine the SMBus address scheme needed to uniquely address each DS280BR810 device on the board, depending on the total number of devices identified in step 1. Each DS280BR810 can be strapped with one of 16 unique SMBus addresses. If there are more DS280BR810 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I<sup>2</sup>C expander like the TCA/PCA family of I<sup>2</sup>C/SMBus switches and multiplexers to split the SMBus into multiple busses.
4. Determine if the device will be configured from EEPROM (SMBus master mode) or from the system I<sup>2</sup>C bus (SMBus slave mode).
  1. If SMBus master mode will be used, provisions should be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
  2. If SMBus slave mode will be used for all device configurations, an EEPROM is not needed.
5. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to [Power Supply Recommendations](#) for more information.

## 8.2.3 Application Curves



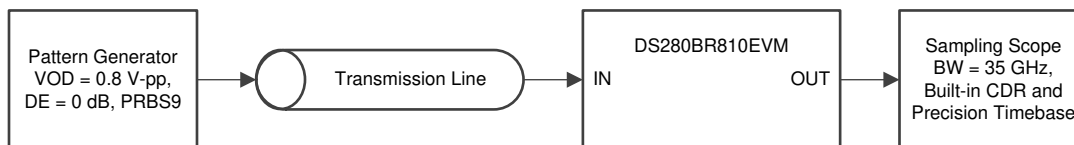
**Figure 11. Minimal Rx/Tx Channel Test Setup**



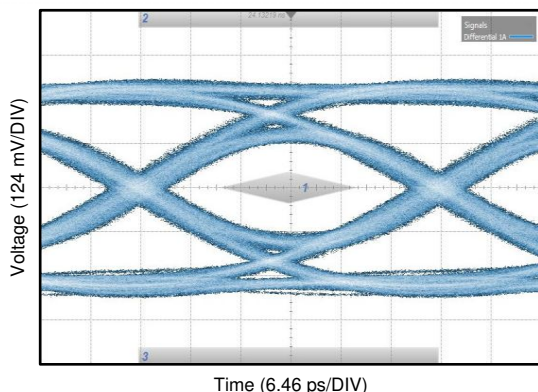
**Table 5. Settings and Measurements for CAUI-4 and nPPI with Minimal Rx/Tx Channel**

	25.78125 Gbps (CAUI-4)	10.3125 Gbps (nPPI)
DS280BR810 Rx Channel Loss	4 dB @ 12.9 GHz	2 dB @ 5.2 GHz
DS280BR810 Tx Channel Loss	4 dB @ 12.9 GHz	2 dB @ 5.2 GHz
EQ BST1	Bypass	Bypass
EQ BST2	2	2
EQ BW	3	3
VOD	2	2
EQ DC Gain Mode	Low	Low
Total Jitter @ 1E-15	10.4 ps <sub>P-P</sub>	10.5 ps <sub>P-P</sub>
Differential Eye Height @ 1E-15	233 mV <sub>P-P</sub>	445 mV <sub>P-P</sub>

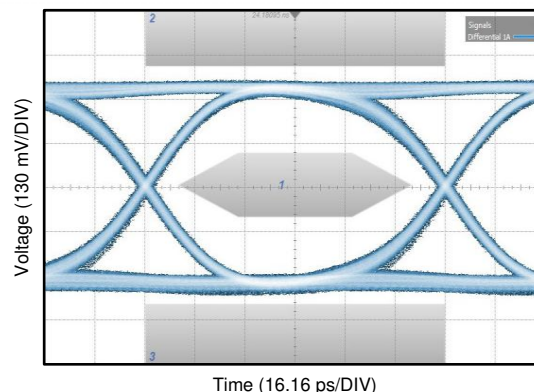




**Figure 14. 5 in Rx and Minimal Tx Channel Test Setup**



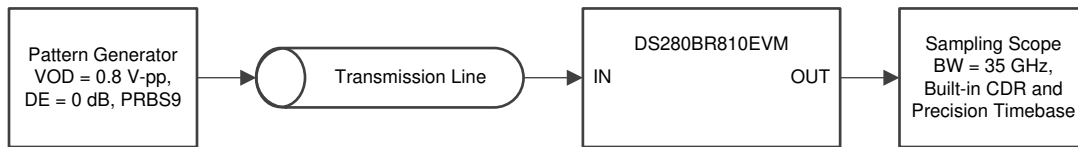
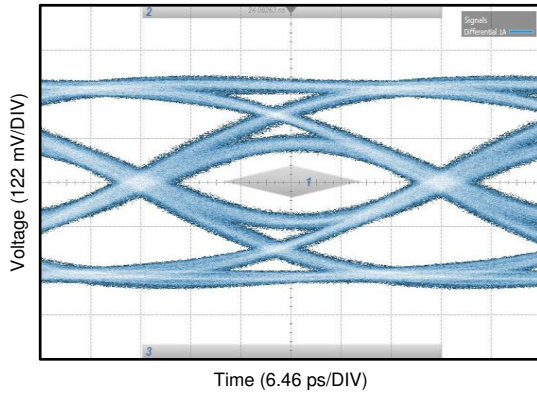
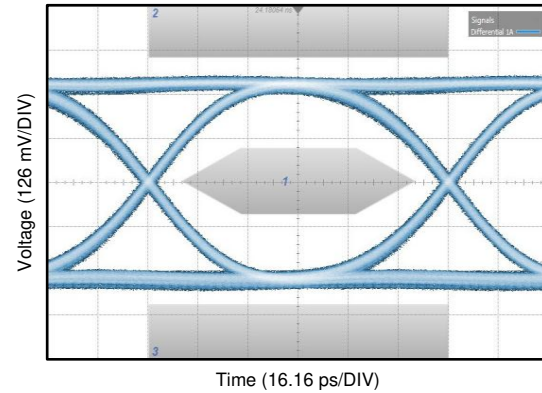
**Figure 15. CAUI-4 Eye Mask with 5 in Rx and Minimal Tx Channel**



**Figure 16. nPPI Eye Mask with 5 in Rx and Minimal Tx Channel**

**Table 6. Settings and Measurements for CAUI-4 and nPPI with 5 in Rx and Minimal Tx Channel**

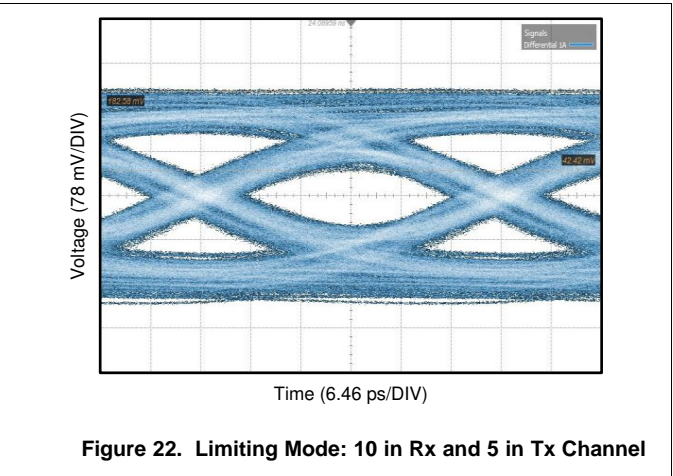
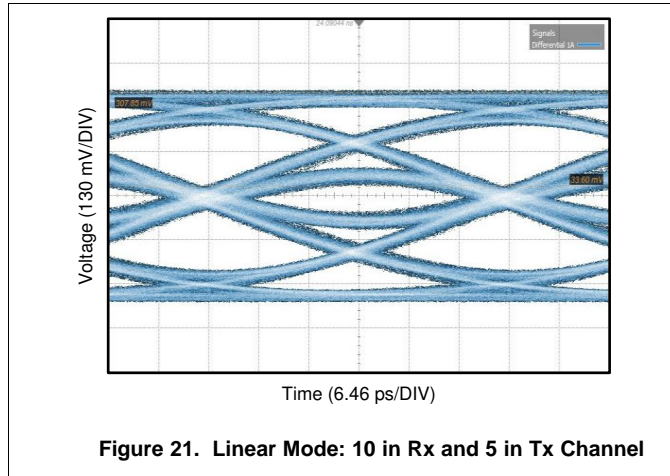
	<b>25.78125 Gbps (CAUI-4)</b>	<b>10.3125 Gbps (nPPI)</b>
Transmission Line 1	5 in 5 mil FR4 + 8 in SMA cable	5 in 5 mil FR4 + 8 in SMA cable
DS280BR810 Rx Channel Loss	14 dB @ 12.9 GHz	6 dB @ 5.2 GHz
DS280BR810 Tx Channel Loss	4 dB @ 12.9 GHz	2 dB @ 5.2 GHz
EQ BST1	2	2
EQ BST2	0	0
EQ BW	3	3
VOD	2	2
EQ DC Gain Mode	Low	Low
Total Jitter @ 1E-15	11.6 ps <sub>P-P</sub>	10.4 ps <sub>P-P</sub>
Differential Eye Height @ 1E-15	236 mV <sub>P-P</sub>	504 mV <sub>P-P</sub>


**Figure 17. 10 in Rx and Minimal Tx Channel Test Setup**

**Figure 18. CAUI-4 Eye Mask with 10 in Rx and Minimal Tx Channel**

**Figure 19. nPPI Eye Mask with 10 in Rx and Minimal Tx Channel**
**Table 7. Settings and Measurements for CAUI-4 and nPPI with 10 in Rx and Minimal Tx Channel**

	25.78125 Gbps (CAUI-4)	10.3125 Gbps (nPPI)
Transmission Line	10 in 5 mil FR4 + 8 in SMA cable	10 in 5 mil FR4 + 8 in SMA cable
DS280BR810 Rx Channel Loss	22 dB @ 12.9 GHz	10 dB @ 5.2 GHz
DS280BR810 Tx Channel Loss	4 dB @ 12.9 GHz	2 dB @ 5.2 GHz
EQ BST1	4	4
EQ BST2	2	2
EQ BW	3	3
VOD	2	2
EQ DC Gain Mode	Low	Low
Total Jitter @ 1E-15	12.4 ps <sub>P-P</sub>	10.4 ps <sub>P-P</sub>
Differential Eye Height @ 1E-15	148 mV <sub>P-P</sub>	504 mV <sub>P-P</sub>



**Figure 20. 10 in Rx and 5 in Tx Channel Test Setup**



**Table 8. Settings and Measurements for 10 in Rx and 5 in Tx Channel**

	<b>LINEAR MODE (25.78125 Gbps)</b>	<b>LIMITING MODE (25.78125 Gbps)</b>
Transmission Line 1	10 in 5 mil FR4 + 8 in SMA cable	10 in 5 mil FR4 + 8 in SMA cable
Transmission Line 2	5 in 5 mil FR4 + 8 in SMA cable	5 in 5 mil FR4 + 8 in SMA cable
DS280BR810 Rx Channel Loss	22 dB @ 12.9 GHz	22 dB @ 12.9 GHz
DS280BR810 Tx Channel Loss	14 dB @ 12.9 GHz	14 dB @ 12.9 GHz
Total Channel Loss	36 dB @ 12.9 GHz	36 dB @ 12.9 GHz
EQ BST1	6	4
EQ BST2	7	2
EQ BW	3	3
VOD	3	3
EQ DC Gain Mode	Low	High
Tx Main-Cursor	N/A	16
Tx Pre-Cursor	N/A	-2
Tx Post-Cursor	N/A	-13
Total Jitter @ 1E-15	15.8 pS <sub>P-P</sub>	18.2 pS <sub>P-P</sub>
Differential Eye Height @ 1E-15	61 mV <sub>P-P</sub>	79 mV <sub>P-P</sub>



Figure 23. FIR Test Setup

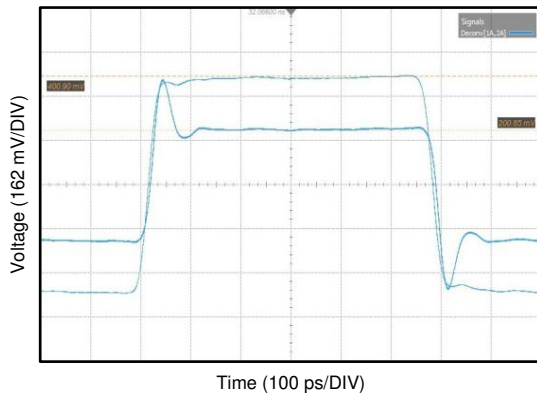


Figure 24. FIR Post-Cursor Example

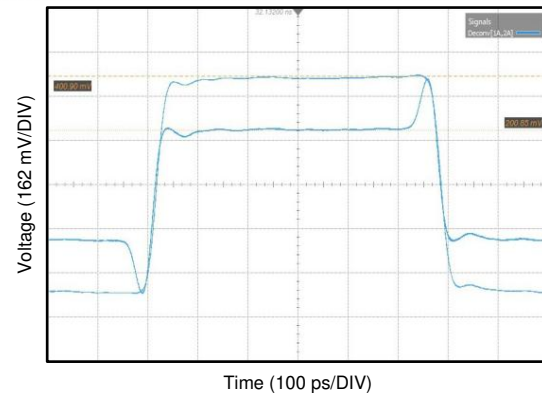


Figure 25. FIR Pre-Cursor Example

Table 9. Example FIR Settings

Figure 24	Figure 25
(Pre, Main, Post) = (0, 12, 0)	(Pre, Main, Post) = (0, 12, 0)
(Pre, Main, Post) = (0, 16, 15)	(Pre, Main, Post) = (11, 12, 0)

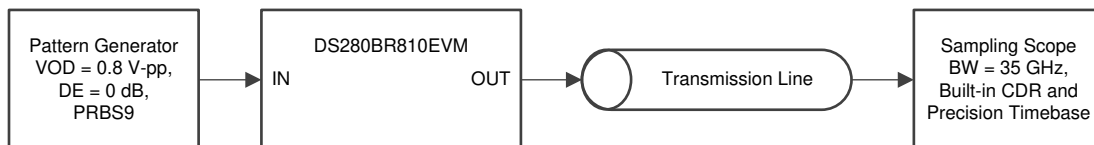


Figure 26. Transmit FIR Test Setup

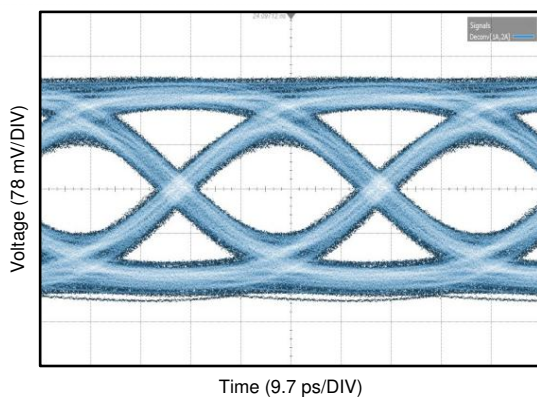


Figure 27. 25.78125 Gbps Limiting Mode with FIR

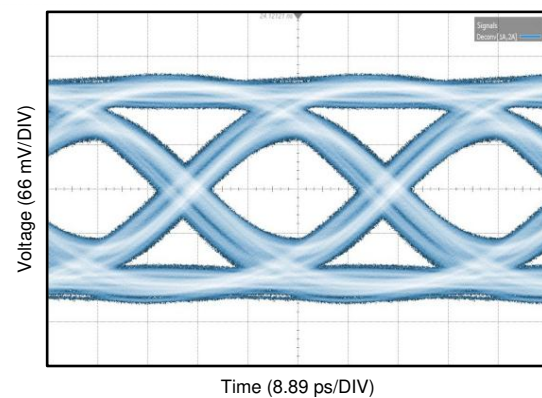


Figure 28. 28.125 Gbps Limiting Mode with FIR

**Table 10. Settings and Measurements for 5 in Tx Channel with Limiting Mode**

	<b>25.78125 Gbps, Limiting Mode</b>	<b>28.125 Gbps, Limiting Mode</b>
Transmission Line	5 in 5 mil FR4 + 8 in SMA cable	5 in 5 mil FR4 + 8 in SMA cable
DS280BR810 Tx Channel Loss	10 dB @ 12.9 GHz	11 dB @ 14 GHz
VOD	3	3
Main-Cursor	16	15
Pre-Cursor	2	2
Post-Cursor	13	14
Total Jitter @ 1E-15	13.8 p <sub>SP,P</sub>	15.3 p <sub>SP,P</sub>
Differential Eye Height @ 1E-15	142 mV <sub>P,P</sub>	138 mV <sub>P,P</sub>

### 8.3 Initialization Set Up

The DS280BR810 does not require any particular start-up or initialization sequence. The device defaults to a medium boost value for each channel. It is recommend that the channels be appropriately configured before data traffic is transmitted to the DS280BR810 to avoid issues with the link partner ASIC's adaption. Example configuration settings can be found in the DS280BR810 Programming Guide.

## 9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the recommended operating conditions outlined in [Specifications](#) in terms of DC voltage, AC noise, and start-up ramp time.
2. The maximum current draw for the DS280BR810 is provided in [Specifications](#). This figure can be used to calculate the maximum current the supply must provide. Typical mission-mode current draw can be inferred from the typical power consumption in [Specifications](#).
3. The DS280BR810 **does not** require any special power supply filtering, such as ferrite beads, provided the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1  $\mu$ F capacitor per power pin, and single 1.0  $\mu$ F and 10  $\mu$ F bulk capacitors.

## 10 Layout

### 10.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VDD pins as possible. Placing them directly underneath the device is one option if the board design permits.
2. High-speed differential signals should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, care should be taken to minimize the via stub, either by transitioning through most or all layers, or by back drilling.
4. GND relief can be used beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.
6. BGA landing pads for a 0.8 mm pitch flip-chip BGA are typically 0.4 mm in diameter (exposed). The actual size of the copper pad will depend on whether solder-mask-defined (SMD) or non-solder-mask-defined solder land pads are used. For more information, refer to TI's Surface Mount Technology (SMT) References website.

### 10.2 Layout Example

The following example layout demonstrates how all signals can be escaped from the BGA array using stripline routing on a generic 28-layer stackup. This example layout assumes the following:

- Trace width: 0.127 mm (5 mil)

## Layout Example (continued)

- Trace edge-to-edge spacing: 0.152 mm (6 mil)
- VIA finished hole size (diameter): 0.203 mm (8 mil)
- VIA drilled hole size: 0.254 mm (10 mil)
- VIA-to-VIA spacing: 1.0 mm (39 mil), to enhance PCB manufacturability
- No VIA-in-pad used

Note that many other escape routing options exist using different trace width and spacing combinations. The optimum trace width and spacing will depend on the PCB material, PCB routing density, and other factors. Microstrip escape routing is also possible and may be preferable in some application scenarios, including front-port applications.

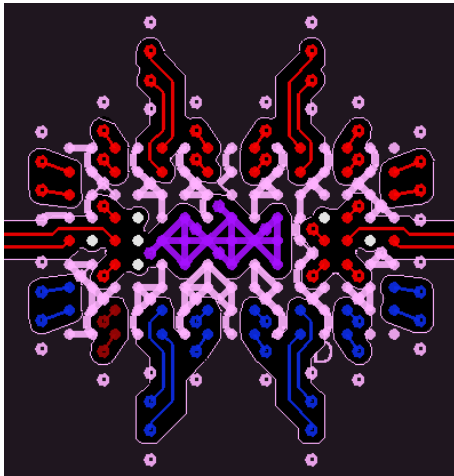


Figure 29. Top Layer

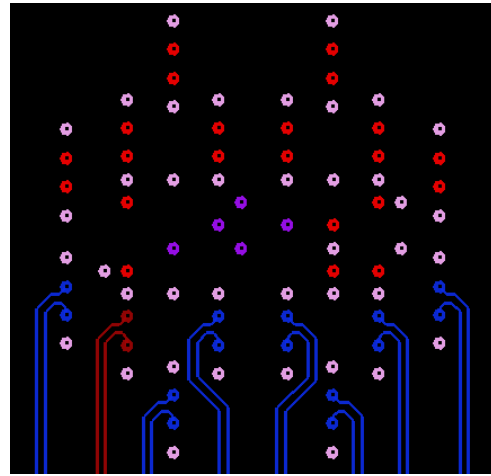


Figure 30. Internal Signal Layer 1

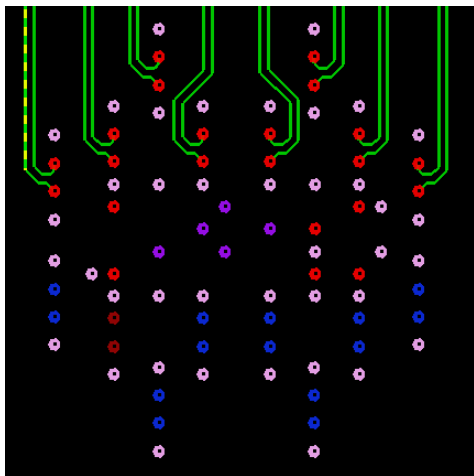


Figure 31. Internal Signal Layer 2

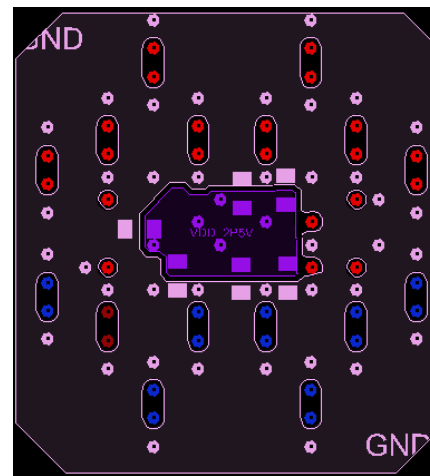


Figure 32. Bottom Layer



## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documents

For related documentation see the following:

- Texas Instruments, [Understanding EEPROM Programming for 25G and 28G Repeaters and Retimers Application Report](#)
- Texas Instruments, [Selection Guide for TI 25G and 28G Retimers and Repeaters Application Report](#)
- Texas Instruments, [DS280BR810EVM User's Guide](#)
- Texas Instruments, [DS280BR810 Programming Guide](#)

#### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

#### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## 12.1 Package Option Addendum

### 12.1.1 Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4)(5)</sup>
DS280BR810ZBFR	ACTIVE	NFBGA	ZBF	135	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8
DS280BR810ZBFT	ACTIVE	NFBGA	ZBF	135	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

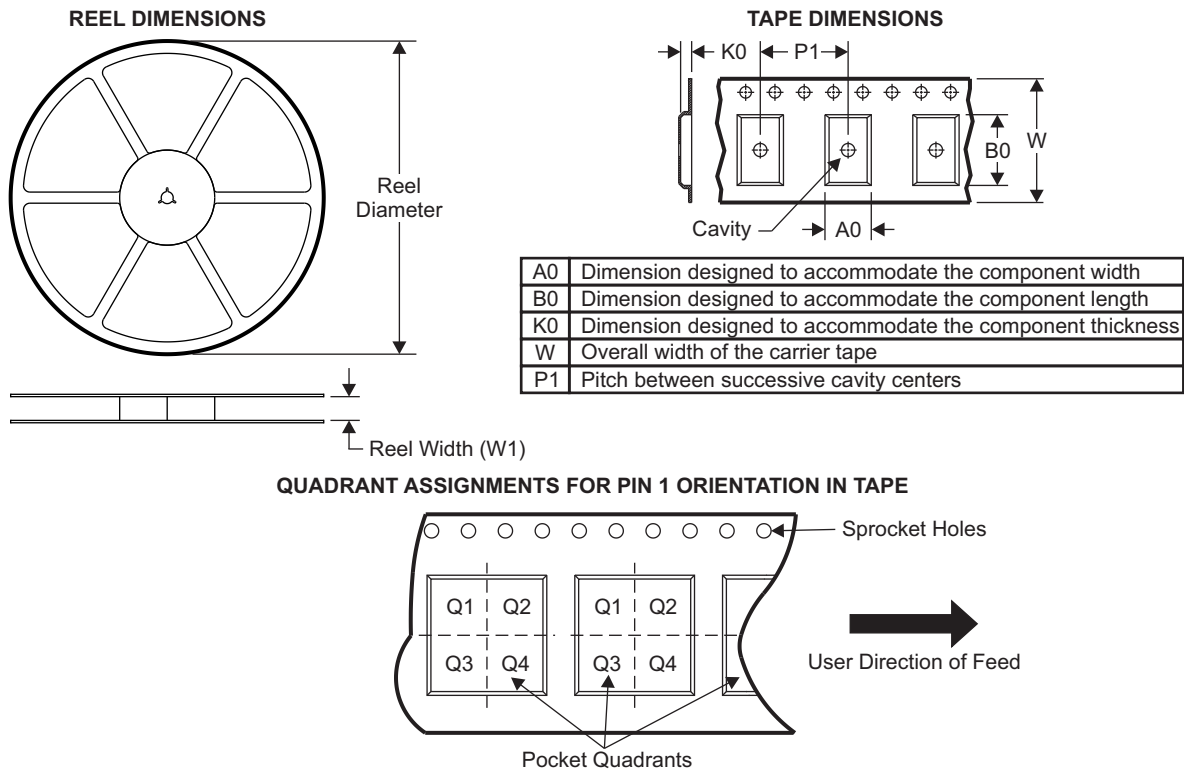
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## DS280BR810

SNLS514C –NOVEMBER 2015–REVISED OCTOBER 2019

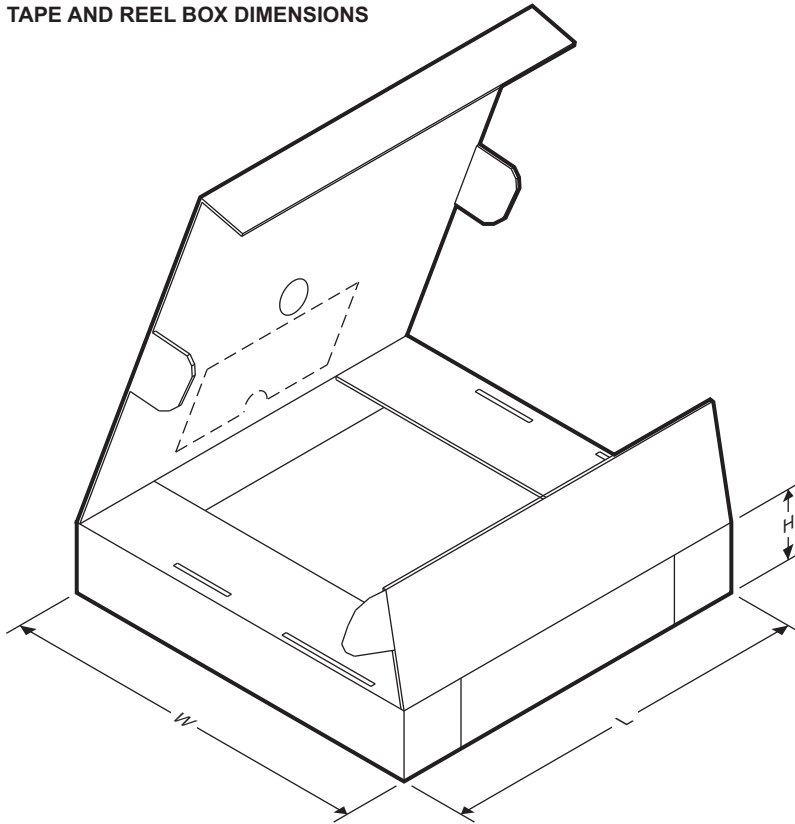
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### 12.1.2 Tape and Reel Information



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS280BR810ZBFR	NFBGA	ZBF	135	1000	330.0	24.4	8.4	13.4	1.9	12.0	24.0	Q2
DS280BR810ZBFT	NFBGA	ZBF	135	250	178.0	24.4	8.4	13.4	1.9	12.0	24.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS280BR810ZBFR	NFBGA	ZBF	135	1000	367.0	367.0	45.0
DS280BR810ZBFT	NFBGA	ZBF	135	250	213.0	191.0	55.0

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DS280BR810ZBFR</a>	Active	Production	NFBGA (ZBF)   135	1000   LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8
DS280BR810ZBFR.A	Active	Production	NFBGA (ZBF)   135	1000   LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8
DS280BR810ZBFR.B	Active	Production	NFBGA (ZBF)   135	1000   LARGE T&R	-	Call TI	Call TI	-40 to 85	
<a href="#">DS280BR810ZBFT</a>	Active	Production	NFBGA (ZBF)   135	250   SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8
DS280BR810ZBFT.A	Active	Production	NFBGA (ZBF)   135	250   SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8
DS280BR810ZBFT.B	Active	Production	NFBGA (ZBF)   135	250   SMALL T&R	-	Call TI	Call TI	-40 to 85	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS280BR810ZBFR	NFBGA	ZBF	135	1000	330.0	24.4	8.4	13.4	1.9	12.0	24.0	Q2
DS280BR810ZBFT	NFBGA	ZBF	135	250	178.0	24.4	8.4	13.4	1.9	12.0	24.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS280BR810ZBFR	NFBGA	ZBF	135	1000	356.0	356.0	45.0
DS280BR810ZBFT	NFBGA	ZBF	135	250	213.0	191.0	55.0

## NFBGA - 1.35 mm max height

[illegible]

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

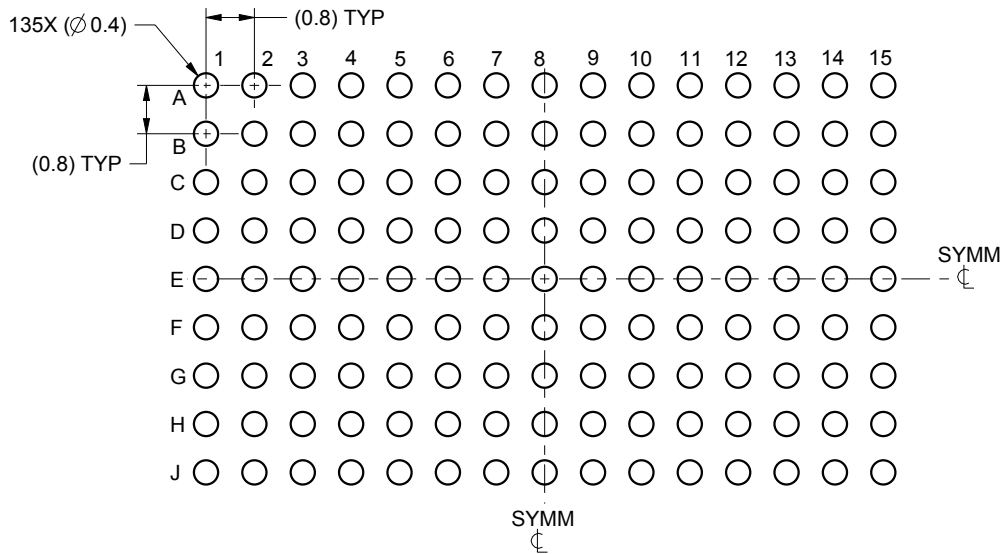


# EXAMPLE BOARD LAYOUT

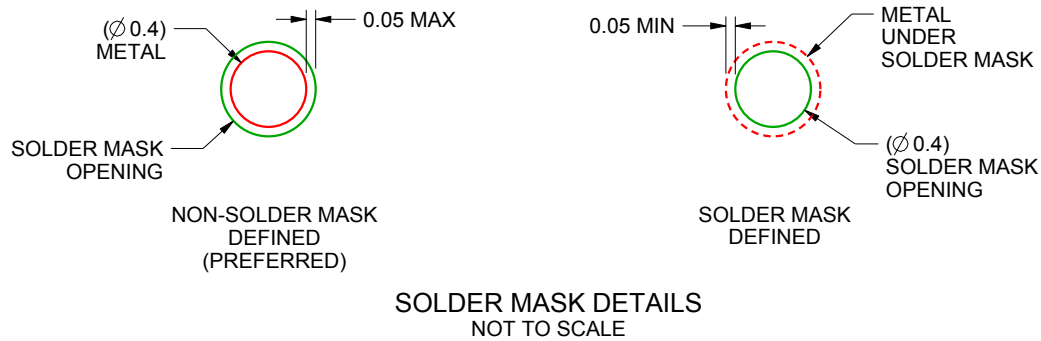
**ZBF0135A**

**NFBGA - 1.35 mm max height**

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:8X



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NOTES: (continued)

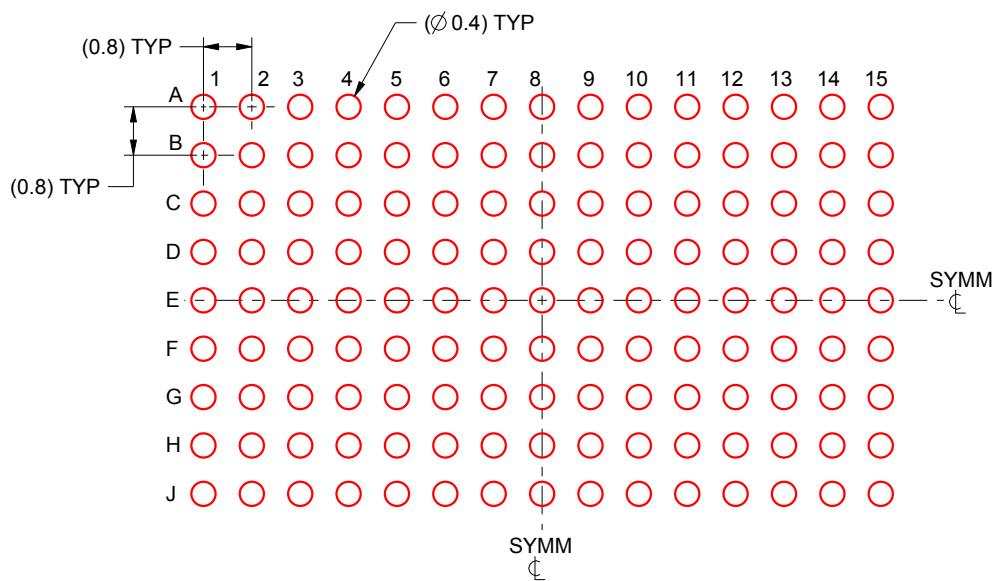
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

## EXAMPLE STENCIL DESIGN

ZBF0135A

NFBGA - 1.35 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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