

# DS25BR440 3.125 Gbps Quad LVDS Buffer with Transmit Pre-Emphasis and Receive Equalization

Check for Samples: DS25BR440

#### **FEATURES**

- DC 3.125 Gbps Low Jitter, Low Skew, Low Power Operation
- Pin Selectable Transmit Pre-Emphasis and Receive Equalization Eliminate Data Dependant Jitter
- Wide Input Common Mode Voltage Range Allows DC-Coupled Interface to LVDS, CML and LVPECL Drivers
- LOS Circuitry Detects Open Inputs Fault
- Integrated 100Ω Input and Output Terminations
- 8 kV ESD on LVDS I/O Pins Protects Adjoining Components
- Small 6 mm x 6 mm WQFN-40 Space Saving Package

#### **APPLICATIONS**

- Clock and Data Buffering and Repeating
- Copper Cable Driving and Equalization
- FR-4 Equalization
- OC-48 / STM-16

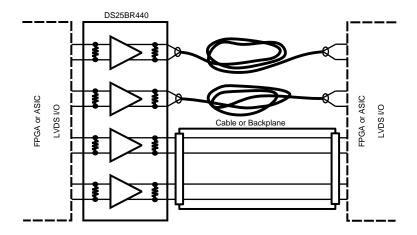
#### DESCRIPTION

The DS25BR440 is a 3.125 Gbps Quad LVDS buffer optimized for high-speed signal routing and repeating over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR440 features two levels of transmit preemphasis (PE) and two levels of receive equalization (EQ). Both of these features compensate for interconnect losses and <u>ultimately maximize noise</u> margin. A loss-of-signal (<u>LOS</u>) circuit monitors each input channel and a unique <u>LOS</u> pin is asserted when no signal is detected at that input.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a  $100\Omega$  resistor to lower device return losses, reduce component count and further minimize board space.

#### **Typical Application**

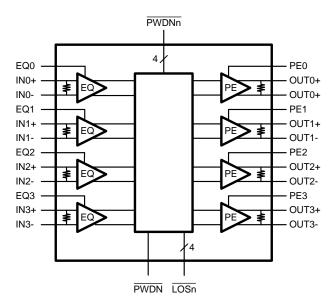


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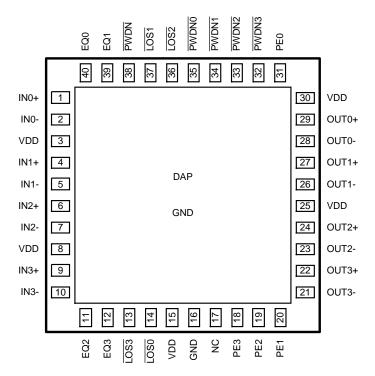
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## **Block Diagram**



# **Connection Diagram**



DS25BR440 Pin Diagram

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#### **PIN DESCRIPTIONS**

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0- , IN1+, IN1-, IN2+, IN2-, IN3+, IN3-	1, 2, 4, 5, 6, 7, 9, 10	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-, OUT2+, OUT2-, OUT3+, OUT3-	29, 28, 27, 26, 24, 23, 22, 21	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
EQ0, EQ1, EQ2, EQ3	40, 39, 11, 12	I, LVCMOS	Receive equalization level select pins.
PE0, PE1, PE2, PE3	31, 20, 19, 18	I, LVCMOS	Transmit pre-emphasis level select pins.
PWDNO, PWDN1, PWDN2, PWDN3	35, 34, 33, 32	I, LVCMOS	Channel output power down pins. When the PWDNn is set to L, the channel output OUTn is in the power down mode. The LOS circuitry on the corresponding input remains enabled.
<u>LOS0</u> , <u>LOS1</u> , <u>LOS2</u> , <u>LOS3</u>	14, 37, 36, 13	O, LVCMOS	Loss Of Signal output pins, $\overline{\text{LOSn}}$ report when an open input fault condition is detected at the input, INn. These are open drain outputs. External pull up resistors are required.
NC	17	NC	NO CONNECT pins. May be left floating.
PWDN	38	I, LVCMOS	Device power down pin. When the PWDN is set to L, the device is in the power down mode. The LOS circuitry is disabled as well.
VDD	3, 8, 15,25, 30	Power	Power supply pins.
GND	16, DAP	Power	Ground pin and a pad (DAP - die attach pad).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



## Absolute Maximum Ratings (1)(2)

Supply Voltage  LVCMOS Input Voltage	-0.3V to +4V -0.3V to (V <sub>CC</sub> + 0.3V)
LVCMOS Input Voltage	
	0.37/ +0.77/ + 0.37/
LVCMOS Output Voltage	$-0.3V$ to $(V_{CC} + 0.3V)$
LVDS Input Voltage	-0.3V to +4V
Differential Input Voltage  VID	1V
LVDS Output Voltage	$-0.3V$ to $(V_{CC} + 0.3V)$
LVDS Differential Output Voltage	0.0V to +1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
RTA0040A Package	2.44W
Derate RTA0040A Package	19.49 mW/°C above +25°C
Package Thermal Resistance	
$\theta_{JA}$	+26.9°C/W
θ <sub>JC</sub>	+3.8°C/W
ESD Susceptibility	
HBM <sup>(3)</sup>	≥8 kV
MM <sup>(4)</sup>	≥250V
CDM <sup>(5)</sup>	≥1250V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

#### **Recommended Operating Conditions**

	Min	Тур	Max	Units
Supply Voltage (V <sub>CC</sub> )	3.0	3.3	3.6	٧
Receiver Differential Input Voltage (V <sub>ID</sub> )	0		1	٧
Operating Free Air Temperature (T <sub>A</sub> )	-40	+25	+85	°C

#### **Electrical Characteristics**

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
LVCMOS DC SPECIFICATIONS							
$V_{IH}$	High Level Input Voltage		2.0		$V_{DD}$	٧	
$V_{IL}$	Low Level Input Voltage		GND		0.8	V	
I <sub>IH</sub>	High Level Input Current	$V_{IN} = 3.6V$ $V_{CC} = 3.6V$		0	±10	μA	

- (1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V<sub>OD</sub> and ΔV<sub>OD</sub>.
- (3) Typical values represent most likely parametric norms for V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

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## **Electrical Characteristics (continued)**

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
I <sub>IL</sub>	Low Level Input Current	V <sub>IN</sub> = GND V <sub>CC</sub> = 3.6V		0	±10	μA
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18 \text{ mA}, V_{CC} = 0 \text{V}$		-0.9	-1.5	V
$V_{OL}$	Low Level Output Voltage	I <sub>OL</sub> = 4 mA		0.26	0.4	V
LVDS IN	PUT DC SPECIFICATIONS					
$V_{ID}$	Input Differential Voltage		0		1	V
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +0.05V \text{ or } V_{CC}-0.05V$		0	+100	mV
$V_{TL}$	Differential Input Low Threshold		-100	0		mV
V <sub>CMR</sub>	Common Mode Voltage Range	V <sub>ID</sub> = 100 mV	0.05		V <sub>CC</sub> - 0.05	V
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = +3.6V or 0V V <sub>CC</sub> = 3.6V or 0V		±1	±10	μΑ
C <sub>IN</sub>	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R <sub>IN</sub>	Input Termination Resistor	Between IN+ and IN-		100		Ω
LVDS O	UTPUT DC SPECIFICATIONS		•			•
V <sub>OD</sub>	Differential Output Voltage		250	350	450	mV
$\Delta V_{OD}$	Change in Magnitude of V <sub>OD</sub> for Complimentary Output States	$R_L = 100\Omega$	-35		35	mV
Vos	Offset Voltage		1.05	1.2	1.375	V
ΔV <sub>OS</sub>	Change in Magnitude of V <sub>OS</sub> for Complimentary Output States	$R_L = 100\Omega$	-35		35	mV
Ios	Output Short Circuit Current (4)	OUT to GND		-35	-55	mA
		OUT to V <sub>CC</sub>		7	55	mA
C <sub>OUT</sub>	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R <sub>OUT</sub>	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
SUPPLY	CURRENT					
I <sub>CC</sub>	Supply Current	PE = OFF, EQ = OFF PWDN = H		162	190	mA
I <sub>CCZ</sub>	Power Down Supply Current	PWDN = L		55	63	mA

<sup>(4)</sup> Output short circuit current (I<sub>OS</sub>) is specified as magnitude only, minus sign indicates direction only.

# AC Electrical Characteristics (1) (2)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Units		
LVDS OUTPUT A	VDS OUTPUT AC SPECIFICATIONS							
t <sub>PLHD</sub>	Differential Propagation Delay Low to High <sup>(3)</sup>	D 4000		390	600	ps		
t <sub>PHLD</sub>	Differential Propagation Delay High to Low (3)	$R_L = 100\Omega$		400	600	ps		
t <sub>SKD1</sub>	Pulse Skew  t <sub>PLHD</sub> - t <sub>PHLD</sub>			10	50	ps		

<sup>(1)</sup> The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

<sup>(2)</sup> Typical values represent most likely parametric norms for V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

<sup>(3)</sup> Specification is guaranteed by characterization and is not tested in production.

<sup>(4)</sup> t<sub>SKD1</sub>, |t<sub>PLHD</sub> - t<sub>PHLD</sub>|, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.



# AC Electrical Characteristics (1) (2) (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conc	litions	Min	Тур	Max	Units
t <sub>SKD2</sub>	Channel to Channel Skew				18	65	ps
t <sub>SKD3</sub>	Part to Part Skew				50	170	ps
t <sub>LHT</sub>	Rise Time (3)				80	160	ps
t <sub>HLT</sub>	Fall Time (3)	VID = 350 mV			80	160	ps
t <sub>ON</sub>	Any PWDN to Output Active Time				8	20	μs
t <sub>OFF</sub>	Any PWDN to Output Inactive Time				5	12	ns
JITTER PERFO	RMANCE WITH EQ = Off, PE = Off (3) (F	igure 5)			•		-
t <sub>RJ1</sub>	Random Jitter (RMS Value)		2.5 Gbps		0.5	1	ps
$t_{RJ2}$	No Test Channels	V <sub>CM</sub> = 1.2V Clock (RZ)	3.125 Gbps		0.5	1	ps
t <sub>DJ1</sub>	Deterministic Jitter (Peak to Peak)	V <sub>ID</sub> = 350 mV	2.5 Gbps		6	22	ps
$t_{\rm DJ2}$	Deterministic Jitter (Peak to Peak)  No Test Channels (8)  Total Jitter (Peak to Peak)  No Test Channels (9)  MANCE WITH EQ = Off, PE = On (3) (Fig Random Jitter (RMS Value)	V <sub>CM</sub> = 1.2V K28.5 (NRZ)	3.125 Gbps		10	29	ps
t <sub>TJ1</sub>	Total Jitter (Peak to Peak)	$V_{CM} = 1.2V$ PRBS-23 (NRZ)	2.5 Gbps		0.04	0.09	UI <sub>P-P</sub>
t <sub>TJ2</sub>		V <sub>CM</sub> = 1.2V PRBS-23 (NRZ)	3.125 Gbps		0.06	0.14	UI <sub>P-P</sub>
JITTER PERFO	RMANCE WITH EQ = Off, PE = On (3) (F	, ,					
t <sub>RJ1B</sub>		V <sub>ID</sub> = 350 mV	2.5 Gbps		0.5	1	ps
t <sub>RJ2B</sub>			3.125 Gbps		0.5	1	ps
t <sub>DJ1B</sub>	Deterministic Jitter (Peak to Peak)	` ,	2.5 Gbps		7	15	ps
t <sub>DJ2B</sub>			3.125 Gbps		4	23	ps
t <sub>TJ1B</sub>	Total Jitter (Peak to Peak)	, ,	2.5 Gbps		0.05	0.10	UI <sub>P-P</sub>
t <sub>TJ2B</sub>	Test Channel B	$V_{CM} = 1.2V$	3.125 Gbps		0.06	0.14	UI <sub>P-P</sub>
JITTER PERFO	RMANCE WITH EQ = On, PE = Off (11) (F	, ,			1		1
t <sub>RJ1D</sub>	Random Jitter (RMS Value)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.5	1	ps
t <sub>RJ2D</sub>	Test Channel D		3.125 Gbps		0.5	1	ps
t <sub>DJ1D</sub>	Deterministic Jitter (Peak to Peak)	V <sub>ID</sub> = 350 mV	2.5 Gbps		14	30	ps
t <sub>DJ2D</sub>	Test Channel D		3.125 Gbps		15	30	ps
t <sub>TJ1D</sub>	Total Jitter (Peak to Peak)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.08	0.15	UI <sub>P-P</sub>
t <sub>TJ2D</sub>	Test Channel D		3.125 Gbps		0.10	0.17	UI <sub>P-P</sub>
JITTER PERFO	RMANCE WITH EQ = On, PE = On (11) (F	Figure 8, Figure 9)		1	1		1
t <sub>RJ1BD</sub>	Random Jitter (RMS Value)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.5	1	ps
t <sub>RJ2BD</sub>	Input Test Channel D Output Test Channel B (12)	V <sub>CM</sub> = 1.2V Clock (RZ)	3.125 Gbps		0.5	1	ps

- (5) t<sub>SKD2</sub>, Channel to Channel Skew, is the difference in propagation delay (t<sub>PLHD</sub> or t<sub>PHLD</sub>) among all output channels in Broadcast mode (any one input to all outputs).
- (6) t<sub>SKD3</sub>, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V<sub>CC</sub> and within 5°C of each other within the operating temperature range.
- (7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
- (8) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
- (9) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.
- (10) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.
- (11) Specification is guaranteed by characterization and is not tested in production.
- (12) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
- (13) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

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# AC Electrical Characteristics (1) (2) (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Cond	Conditions			Max	Units
t <sub>DJ1BD</sub>	Deterministic Jitter (Peak to Peak)	V <sub>ID</sub> = 350 mV	2.5 Gbps		11	23	ps
t <sub>DJ2BD</sub>	Input Test Channel D	V <sub>CM</sub> = 1.2V K28.5 (NRZ)	3.125 Gbps		5	24	ps
t <sub>TJ1BD</sub>	Total Jitter (Peak to Peak)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.08	0.14	UI <sub>P-P</sub>
t <sub>TJ2BD</sub>	Input Test Channel D Output Test Channel B (10)	V <sub>CM</sub> = 1.2V PRBS-23 (NRZ)	3.125 Gbps		0.10	0.20	UI <sub>P-P</sub>



#### DC TEST CIRCUITS

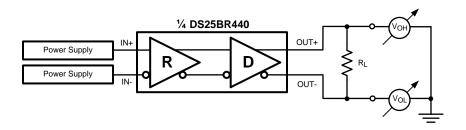


Figure 1. Differential Driver DC Test Circuit

## **AC Test Circuits and Timing Diagrams**

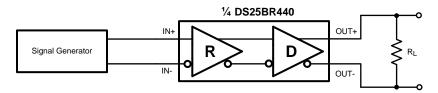


Figure 2. Differential Driver AC Test Circuit

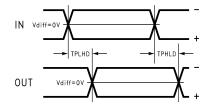


Figure 3. Propagation Delay Timing Diagram

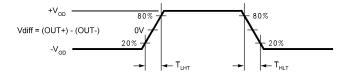


Figure 4. LVDS Output Transition Times

## **Pre-Emphasis and Equalization Test Circuits**

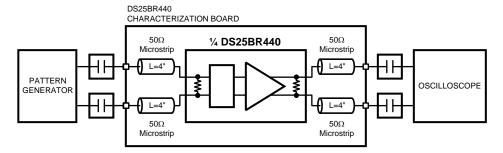


Figure 5. Jitter Performance Test Circuit



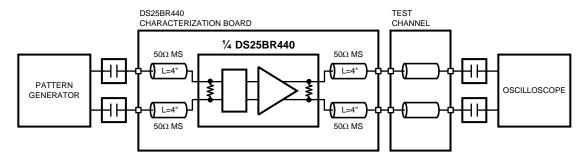


Figure 6. Pre-emphasis Performance Test Circuit

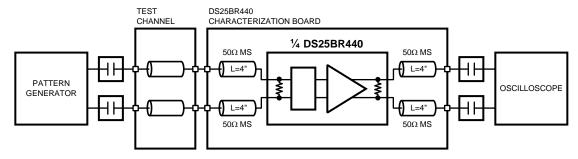


Figure 7. Equalization Performance Test Circuit

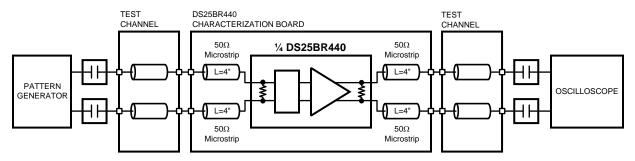


Figure 8. Pre-emphasis and Equalization Performance Test Circuit

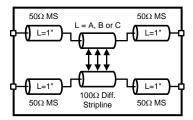


Figure 9. Test Channel Block Diagram

#### **Test Channel Loss Characteristics**

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.



Test Channel	Length						
	(inches)	500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
Α	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
В	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
С	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
Е	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

#### **Functional Description**

The DS25BR440 is a 3.125 Gbps Quad LVDS buffer optimized for high-speed signal routing and repeating over lossy FR-4 printed circuit board backplanes and balanced cables.

The DS25BR440 has a pre-emphasis control pin for each output for switching the transmit pre-emphasis to ON and OFF setting and an equalization control pin for each input for switching the receive equalization to ON and OFF setting. The following are the transmit pre-emphasis and receive equalization truth tables.

Table 1. Transmit Pre-Emphasis Truth Table (1)

OUTPUT OUTn, n = {0, 1, 2, 3}					
CONTROL Pin (PEn) State	Pre-emphasis Level				
0	OFF				
1	ON				

(1) Transmit Pre-emphasis Level Selection for an Output OUTn

Table 2. Receive Equalization Truth Table (1)

INPUT INn, n = {0, 1, 2, 3}				
CONTROL Pin (EQn) State	Equalization Level			
0	OFF			
1	ON			

(1) Receive Equalization Level Selection for an Input INn

#### Input Interfacing

The DS25BR440 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR440 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR440 inputs are internally terminated with a  $100\Omega$  resistor.

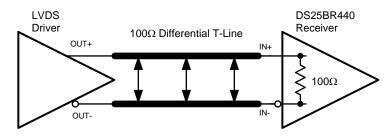


Figure 10. Typical LVDS Driver DC-Coupled Interface to an DS25BR440 Input



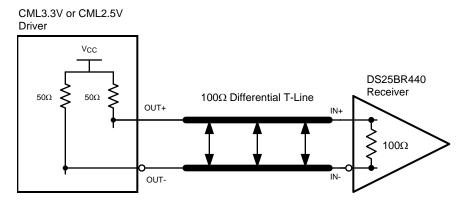


Figure 11. Typical CML Driver DC-Coupled Interface to an DS25BR440 Input

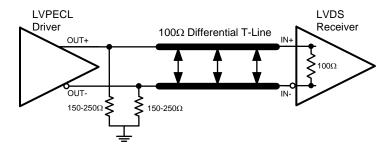


Figure 12. Typical LVPECL Driver DC-Coupled Interface to an DS25BR440 Input

#### **Output Interfacing**

The DS25BR440 outputs signals compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's data sheet prior to implementing the suggested interface implementation.

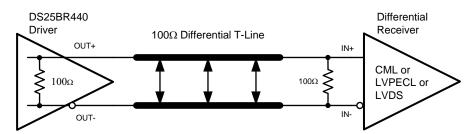


Figure 13. Typical DS25BR440 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver



## **Typical Performance**

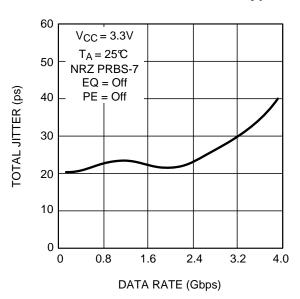


Figure 14. Total Jitter as a Function of Data Rate

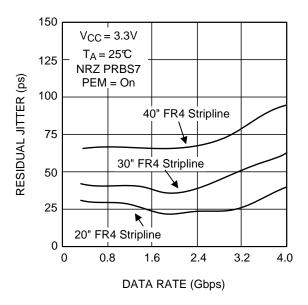


Figure 16. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and PE Level

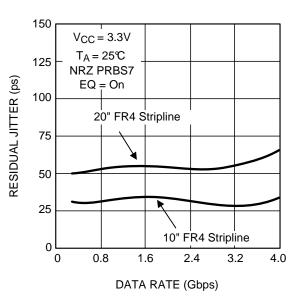


Figure 15. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and EQ Level

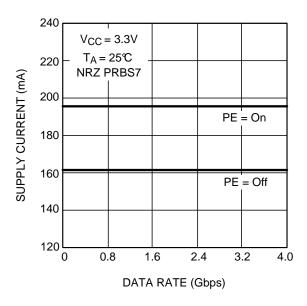


Figure 17. Supply Current as a Function of Data Rate and PE Level





## **REVISION HISTORY**

CI	Changes from Revision A (March 2013) to Revision B					
•	Changed layout of National Data Sheet to TI format	12				

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
		( )			(-)	(4)	(5)		(-)
DS25BR440TSQ/NOPB	Active	Production	WQFN (RTA)   40	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-	2BR440SQ
DS25BR440TSQ/NOPB.A	Active	Production	WQFN (RTA)   40	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2BR440SQ
DS25BR440TSQ/NOPB.B	Active	Production	WQFN (RTA)   40	250   SMALL T&R	-	Call TI	Call TI	-40 to 85	
DS25BR440TSQX/NOPB	Active	Production	WQFN (RTA)   40	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2BR440SQ
DS25BR440TSQX/NOPB.A	Active	Production	WQFN (RTA)   40	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2BR440SQ
DS25BR440TSQX/NOPB.B	Active	Production	WQFN (RTA)   40	2500   LARGE T&R	-	Call TI	Call TI	-40 to 85	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



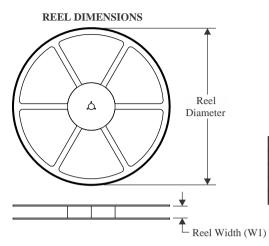
# **PACKAGE OPTION ADDENDUM**

www.ti.com 1-Nov-2025

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 1-Aug-2025

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR440TSQ/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS25BR440TSQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

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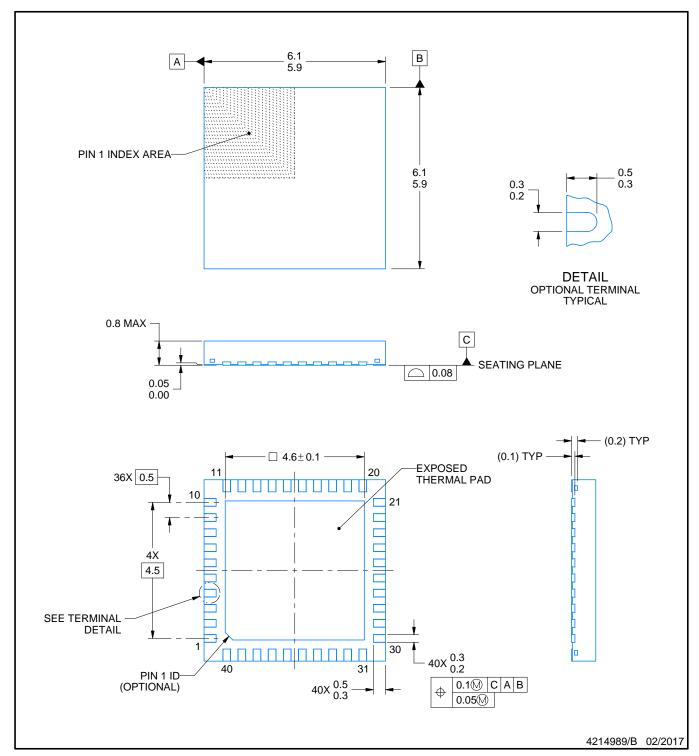


## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR440TSQ/NOPB	WQFN	RTA	40	250	208.0	191.0	35.0
DS25BR440TSQX/NOPB	WQFN	RTA	40	2500	356.0	356.0	36.0



PLASTIC QUAD FLATPACK - NO LEAD

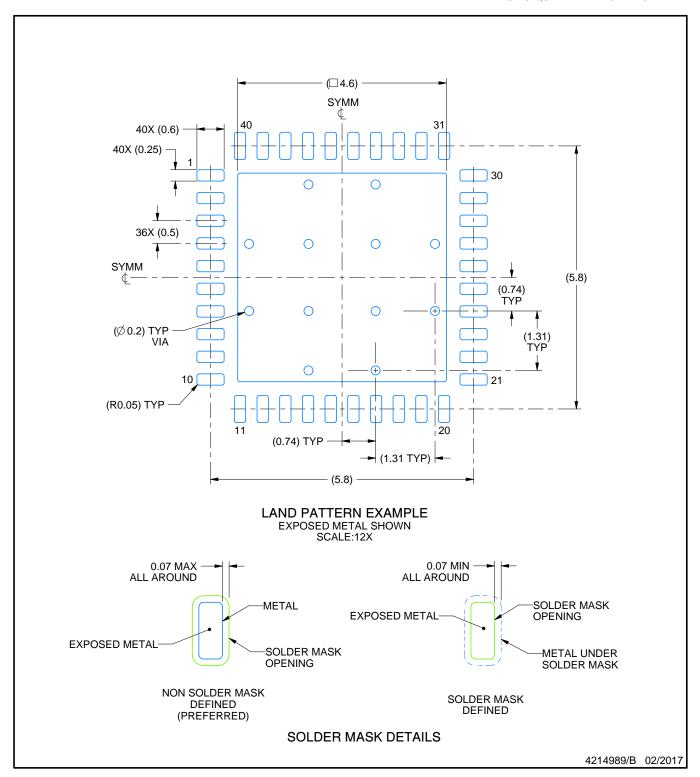


#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

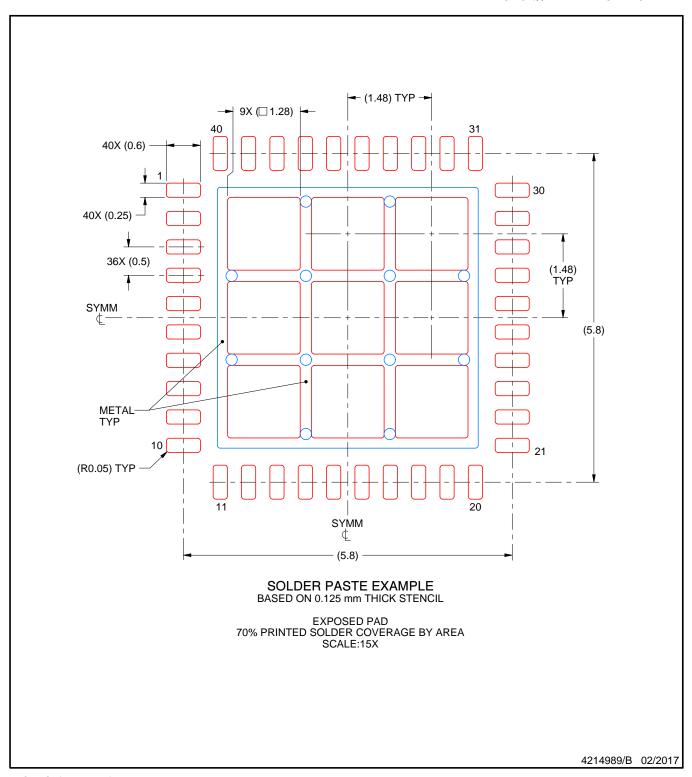


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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