DS160PR1601 16 Gbps 16 Lane Linear Redriver

1 Features

- 16-lane linear redriver supporting PCIe 4.0, and UPI 2.0
- Supports data rates up to 16-Gbps
- P2P with Intel retimer common footprint
- 64 integrated AC coupling capacitors on TX pins inside package saving board space
- CTLE boosts of 16 dB at 8 GHz
- Analog EyeScan to aid redriver tuning, debug and remote monitoring
- Ultra-low latency of 130 ps
- Low additive random jitter of 100 fs for PRBS data
- Excellent RX/TX return loss of −13 dB at 8 GHz
- Single 3.3 V supply
- Low active power of 160 mW/channel
- I^2C/SMBus or EEPROM programming
- Automatic receiver detection for PCIe use cases
- Seamless support for PCIe link training
- Internal voltage regulator provides immunity to supply noise
- High speed production testing for reliable manufacturing
- Support for x4, x8, x16 bus width
- 8.90 mm × 22.80 mm BGA package

2 Applications

- Rack server, Microserver, and tower server
- High performance computing
- Hardware accelerator
- Network attached storage
- Storage area network (SAN) and host bus adapter (HBA) card
- Network interface card (NIC)
- Desktop PC or motherboard

3 Description

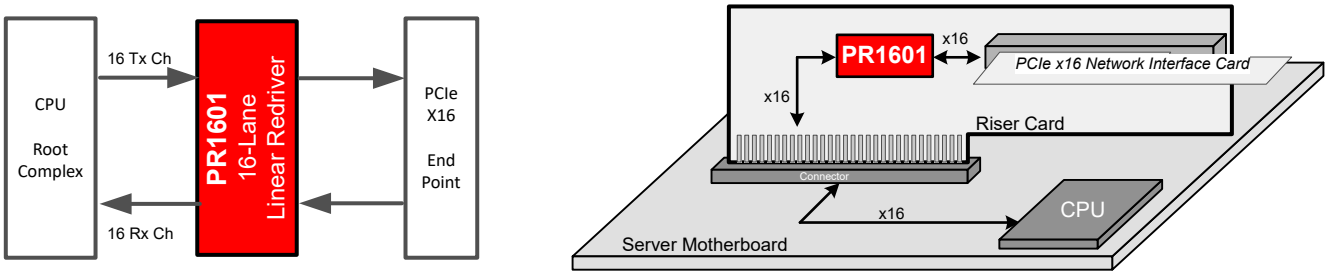
The DS160PR1601 is a 32-channel (16-channel in each direction) x16 (16-lane) low-power high-performance linear repeater or redriver designed to support PCIe 4.0, UPI 2.0 and other interfaces up to 16 Gbps.

The DS160PR1601 receivers deploy continuous time linear equalizers (CTLE) to provide a programmable high-frequency boost. The equalizer can open an input eye that is completely closed due to inter-symbol interference (ISI) induced by an interconnect medium, such as PCB traces. The CTLE receiver is followed by a linear output driver. The linear datapaths of DS160PR1601 preserves transmit preset signal characteristics. The linear redriver becomes part of the passive channel that as a whole get link trained for best transmit and receive equalization settings. This transparency in the link training protocol results in best electrical link and lowest possible latency. Low channel-channel cross-talk, low additive jitter and excellent return loss makes the device almost a passive element in the link, but with its equalization.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS160PR1601	ZDG (nfBGA, 354)	22.89 mm × 8.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

DATE	REVISION	NOTES
February 2023	*	Initial Release

5 Pin Configuration and Functions

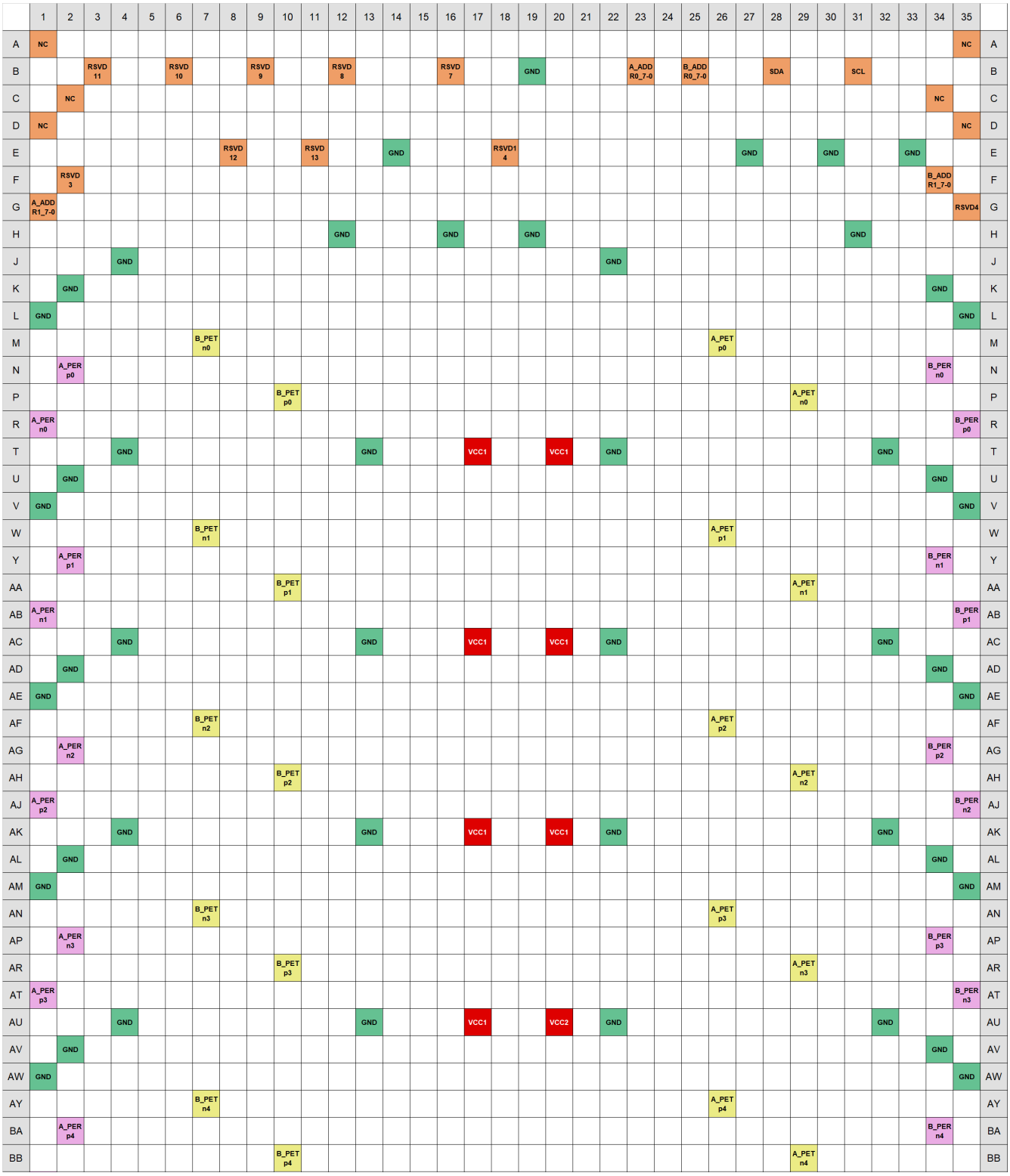


Figure 5-1. ZDG Package, 354-Pin BGA (Top View 1/3)

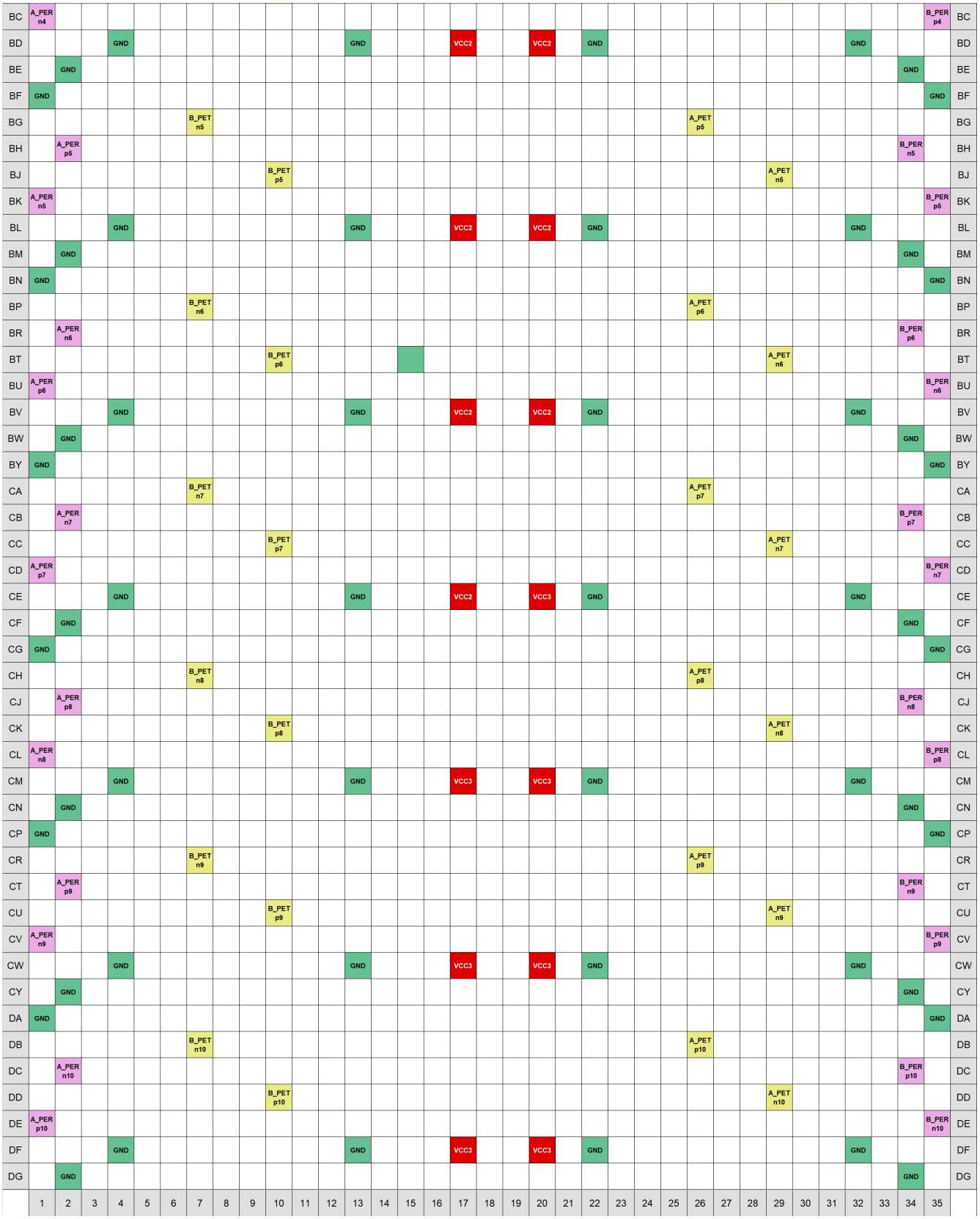


Figure 5-2. ZDG Package, 354-Pin BGA (Top View 2/3)

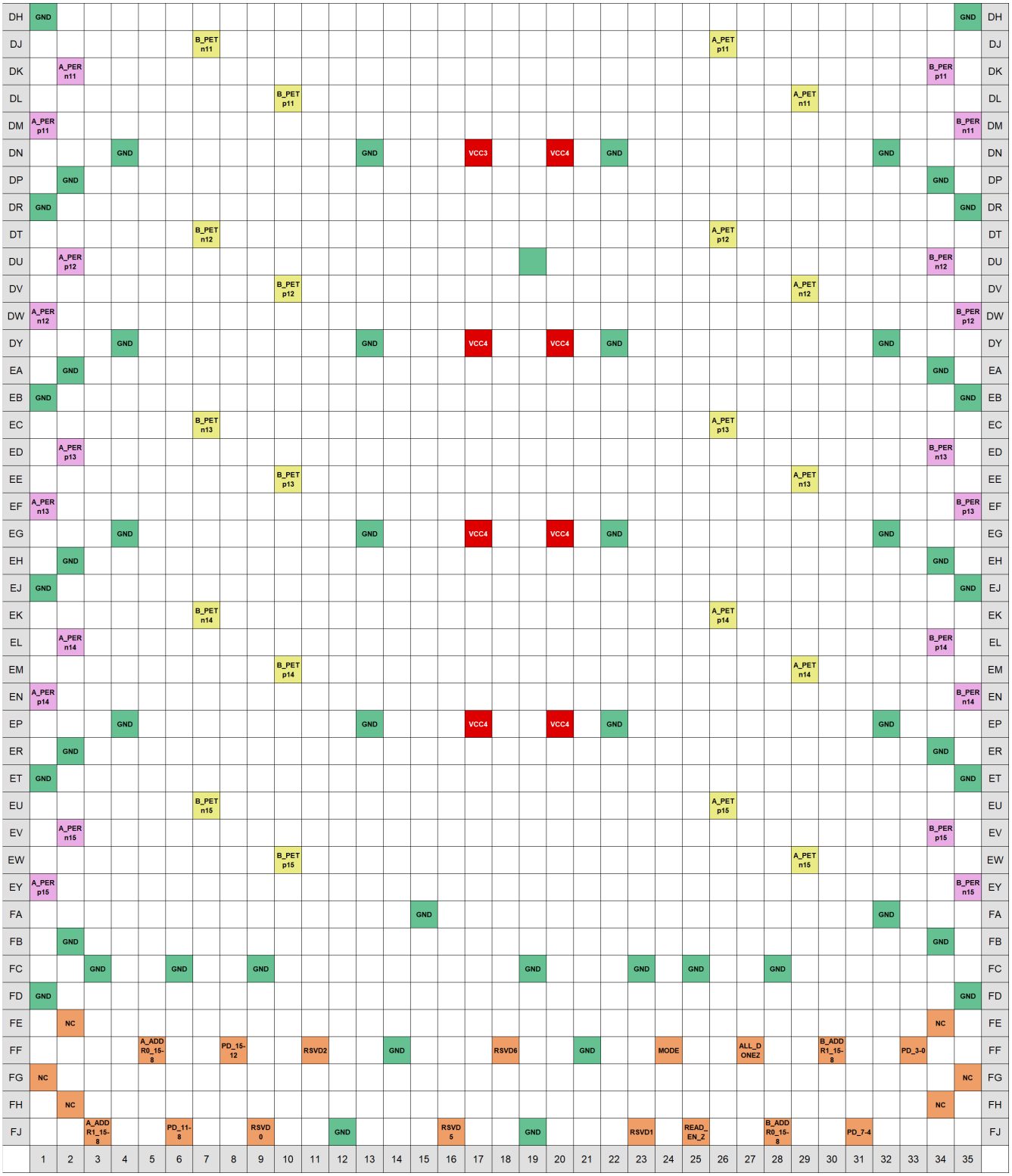


Figure 5-3. ZDG Package 354-Pin BGA Top View 3/3

Legend				
Ground	Power	IOs, RSVD /NC	Differential Input	Differential Output

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	N/C	—	No internal connection.
A35	N/C	—	No internal connection.
B12	RSVD8	—	Reserved for future use. No internal connection.
B16	RSVD7	—	Reserved for future use. No internal connection.
B19	GND	Ground	Ground
B23	A_ADDR0_7-0	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
B25	B_ADDR0_7-0	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
B28	SDA	Input /Output	3.3 V SMBus/I2C data IO pin SDA. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I2C interface standard. The device can alter between SMBus/I2C primary and secondary mode through exercising MODE pin.
B3	RSVD11	—	Reserved for future use. No internal connection.
B31	SCL	Input /Output	3.3 V SMBus/I2C clock IO pin SCL. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I2C interface standard. The device can alter between SMBus/I2C primary and secondary mode through exercising MODE pin.
B6	RSVD10	—	Reserved for future use. No internal connection.
B9	RSVD9	—	Reserved for future use. No internal connection.
C2	N/C	—	No internal connection.
C34	N/C	—	No internal connection.
D1	N/C	—	No internal connection.
D35	N/C	—	No internal connection.
E11	RSVD13	—	Reserved for future use. No internal connection.
E14	GND	Ground	Ground
E18	RSVD14	—	Reserved for future use. No internal connection.
E27	GND	Ground	Ground
E30	GND	Ground	Ground
E33	GND	Ground	Ground
E8	RSVD12	—	Reserved for future use. No internal connection.
F2	RSVD3	—	Reserved for future use. No internal connection.
F34	B_ADDR1_7-0	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
G1	A_ADDR1_7-0	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
G35	RSVD4	—	Reserved for future use. No internal connection.
H12	GND	Ground	Ground
H16	GND	Ground	Ground
H19	GND	Ground	Ground
H31	GND	Ground	Ground
J22	GND	Ground	Ground
J4	GND	Ground	Ground
K2	GND	Ground	Ground
K34	GND	Ground	Ground
L1	GND	Ground	Ground
L35	GND	Ground	Ground
M26	A_PETp0	Diff Output	Differential transmit signal, channel A, lane 0, positive
M7	B_PETn0	Diff Output	Differential transmit signal, channel B, lane 0, negative

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
N2	A_PERp0	Diff Input	Differential receive signal, channel A, lane 0, positive
N34	B_PERn0	Diff Input	Differential receive signal, channel B, lane 0, negative
P10	B_PETp0	Diff Output	Differential transmit signal, channel B, lane 0, positive
P29	A_PETn0	Diff Output	Differential transmit signal, channel A, lane 0, negative
R1	A_PERn0	Diff Input	Differential receive signal, channel A, lane 0, negative
R35	B_PERp0	Diff Input	Differential receive signal, channel B, lane 0, positive
T13	GND	Ground	Ground
T17	VCC1	Power	3.3 V Supply Voltage
T20	VCC1	Power	3.3 V Supply Voltage
T22	GND	Ground	Ground
T32	GND	Ground	Ground
T4	GND	Ground	Ground
U2	GND	Ground	Ground
U34	GND	Ground	Ground
V1	GND	Ground	Ground
V35	GND	Ground	Ground
W26	A_PETp1	Diff Output	Differential transmit signal, channel A, lane 1, positive
W7	B_PETn1	Diff Output	Differential transmit signal, channel B, lane 1, negative
Y2	A_PERp1	Diff Input	Differential receive signal, channel A, lane 1, positive
Y34	B_PERn1	Diff Input	Differential receive signal, channel B, lane 1, negative
AA10	B_PETp1	Diff Output	Differential transmit signal, channel B, lane 1, positive
AA29	A_PETn1	Diff Output	Differential transmit signal, channel B, lane 1, negative
AB1	A_PERn1	Diff Input	Differential receive signal, channel A, lane 1, negative
AB35	B_PERp1	Diff Input	Differential receive signal, channel B, lane 1, positive
AC13	GND	Ground	Ground
AC17	VCC1	Power	3.3 V Supply Voltage
AC20	VCC1	Power	3.3 V Supply Voltage
AC22	GND	Ground	Ground
AC32	GND	Ground	Ground
AC4	GND	Ground	Ground
AD2	GND	Ground	Ground
AD34	GND	Ground	Ground
AE1	GND	Ground	Ground
AE35	GND	Ground	Ground
AF26	A_PETp2	Diff Output	Differential transmit signal, channel A, lane 2, positive
AF7	B_PETn2	Diff Output	Differential transmit signal, channel B, lane 2, negative
AG2	A_PERn2	Diff Input	Differential receive signal, channel A, lane 2, negative
AG34	B_PERp2	Diff Input	Differential receive signal, channel B, lane 2, positive
AH10	B_PETp2	Diff Output	Differential transmit signal, channel B, lane 2, positive
AH29	A_PETn2	Diff Output	Differential transmit signal, channel A, lane 2, negative
AJ1	A_PERp2	Diff Input	Differential receive signal, channel A, lane 2, positive
AJ35	B_PERn2	Diff Input	Differential receive signal, channel B, lane 2, negative
AK13	GND	Ground	Ground
AK17	VCC1	Power	3.3 V Supply Voltage

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
AK20	VCC1	Power	3.3 V Supply Voltage
AK22	GND	Ground	Ground
AK32	GND	Ground	Ground
AK4	GND	Ground	Ground
AL2	GND	Ground	Ground
AL34	GND	Ground	Ground
AM1	GND	Ground	Ground
AM35	GND	Ground	Ground
AN26	A_PETp3	Diff Output	Differential transmit signal, channel A, lane 3, positive
AN7	B_PETn3	Diff Output	Differential transmit signal, channel B, lane 3, negative
AP2	A_PERn3	Diff Input	Differential receive signal, channel A, lane 3, negative
AP34	B_PERp3	Diff Input	Differential receive signal, channel B, lane 3, positive
AR10	B_PETp3	Diff Output	Differential transmit signal, channel B, lane 3, positive
AR29	A_PETn3	Diff Output	Differential transmit signal, channel A, lane 3, negative
AT1	A_PERp3	Diff Input	Differential receive signal, channel A, lane 3, positive
AT35	B_PERn3	Diff Input	Differential receive signal, channel B, lane 3, negative
AU13	GND	Ground	Ground
AU17	VCC1	Power	3.3 V Supply Voltage
AU20	VCC2	Power	3.3 V Supply Voltage
AU22	GND	Ground	Ground
AU32	GND	Ground	Ground
AU4	GND	Ground	Ground
AV2	GND	Ground	Ground
AV34	GND	Ground	Ground
AW1	GND	Ground	Ground
AW35	GND	Ground	Ground
AY26	A_PETp4	Diff Output	Differential transmit signal, channel A, lane 4, positive
AY7	B_PETn4	Diff Output	Differential transmit signal, channel B, lane 4, negative
BA2	A_PERp4	Diff Input	Differential receive signal, channel A, lane 4, positive
BA34	B_PERn4	Diff Input	Differential receive signal, channel B, lane 4, negative
BB10	B_PETp4	Diff Output	Differential transmit signal, channel B, lane 4, positive
BB29	A_PETn4	Diff Output	Differential transmit signal, channel A, lane 4, negative
BC1	A_PERn4	Diff Input	Differential receive signal, channel A, lane 4, negative
BC35	B_PERp4	Diff Input	Differential receive signal, channel B, lane 4, positive
BD13	GND	Ground	Ground
BD17	VCC2	Power	3.3 V Supply Voltage
BD20	VCC2	Power	3.3 V Supply Voltage
BD22	GND	Ground	Ground
BD32	GND	Ground	Ground
BD4	GND	Ground	Ground
BE2	GND	Ground	Ground
BE34	GND	Ground	Ground
BF1	GND	Ground	Ground
BF35	GND	Ground	Ground

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
BG26	A_PETp5	Diff Output	Differential transmit signal, channel A, lane 5, positive
BG7	B_PETn5	Diff Output	Differential transmit signal, channel B, lane 5, negative
BH2	A_PERp5	Diff Input	Differential receive signal, channel A, lane 5, positive
BH34	B_PERn5	Diff Input	Differential receive signal, channel B, lane 5, negative
BJ10	B_PETp5	Diff Output	Differential transmit signal, channel B, lane 5, positive
BJ29	A_PETn5	Diff Output	Differential transmit signal, channel A, lane 5, negative
BK1	A_PERn5	Diff Input	Differential receive signal, channel A, lane 5, negative
BK35	B_PERp5	Diff Input	Differential receive signal, channel B, lane 5, positive
BL13	GND	Ground	Ground
BL17	VCC2	Power	3.3 V Supply Voltage
BL20	VCC2	Power	3.3 V Supply Voltage
BL22	GND	Ground	Ground
BL32	GND	Ground	Ground
BL4	GND	Ground	Ground
BM2	GND	Ground	Ground
BM34	GND	Ground	Ground
BN1	GND	Ground	Ground
BN35	GND	Ground	Ground
BP26	A_PETp6	Diff Output	Differential transmit signal, channel A, lane 6, positive
BP7	B_PETn6	Diff Output	Differential transmit signal, channel B, lane 6, negative
BR2	A_PERn6	Diff Input	Differential receive signal, channel A, lane 6, negative
BR34	B_PERp6	Diff Input	Differential receive signal, channel B, lane 6, positive
BT10	B_PETp6	Diff Output	Differential transmit signal, channel B, lane 6, positive
BT29	A_PETn6	Diff Output	Differential transmit signal, channel A, lane 6, negative
BU1	A_PERp6	Diff Input	Differential receive signal, channel A, lane 6, positive
BU35	B_PERn6	Diff Input	Differential receive signal, channel B, lane 6, negative
BV13	GND	Ground	Ground
BV17	VCC2	Power	3.3 V Supply Voltage
BV20	VCC2	Power	3.3 V Supply Voltage
BV22	GND	Ground	Ground
BV32	GND	Ground	Ground
BV4	GND	Ground	Ground
BW2	GND	Ground	Ground
BW34	GND	Ground	Ground
BY1	GND	Ground	Ground
BY35	GND	Ground	Ground
CA26	A_PETp7	Diff Output	Differential transmit signal, channel A, lane 7, positive
CA7	B_PETn7	Diff Output	Differential transmit signal, channel B, lane 7, negative
CB2	A_PERn7	Diff Input	Differential receive signal, channel A, lane 7, negative
CB34	B_PERp7	Diff Input	Differential receive signal, channel B, lane 7, positive
CC10	B_PETp7	Diff Output	Differential transmit signal, channel B, lane 7, positive
CC29	A_PETn7	Diff Output	Differential transmit signal, channel A, lane 7, negative
CD1	A_PERp7	Diff Input	Differential receive signal, channel A, lane 7, positive
CD35	B_PERn7	Diff Input	Differential receive signal, channel B, lane 7, negative

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
CE13	GND	Ground	Ground
CE17	VCC2	Power	3.3 V Supply Voltage
CE20	VCC3	Power	3.3 V Supply Voltage
CE22	GND	Ground	Ground
CE32	GND	Ground	Ground
CE4	GND	Ground	Ground
CF2	GND	Ground	Ground
CF34	GND	Ground	Ground
CG1	GND	Ground	Ground
CG35	GND	Ground	Ground
CH26	A_PETp8	Diff Output	Differential transmit signal, channel A, lane 8, positive
CH7	B_PETn8	Diff Output	Differential transmit signal, channel B, lane 8, negative
CJ2	A_PERp8	Diff Input	Differential receive signal, channel A, lane 8, positive
CJ34	B_PERn8	Diff Input	Differential receive signal, channel B, lane 8, negative
CK10	B_PETp8	Diff Output	Differential transmit signal, channel B, lane 8, positive
CK29	A_PETn8	Diff Output	Differential transmit signal, channel A, lane 8, negative
CL1	A_PERn8	Diff Input	Differential receive signal, channel A, lane 8, negative
CL35	B_PERp8	Diff Input	Differential receive signal, channel B, lane 8, positive
CM13	GND	Ground	Ground
CM17	VCC3	Power	3.3 V Supply Voltage
CM20	VCC3	Power	3.3 V Supply Voltage
CM22	GND	Ground	Ground
CM32	GND	Ground	Ground
CM4	GND	Ground	Ground
CN2	GND	Ground	Ground
CN34	GND	Ground	Ground
CP1	GND	Ground	Ground
CP35	GND	Ground	Ground
CR26	A_PETp9	Diff Output	Differential transmit signal, channel A, lane 9, positive
CR7	B_PETn9	Diff Output	Differential transmit signal, channel B, lane 9, negative
CT2	A_PERp9	Diff Input	Differential receive signal, channel A, lane 9, positive
CT34	B_PERn9	Diff Input	Differential receive signal, channel B, lane 9, negative
CU10	B_PETp9	Diff Output	Differential transmit signal, channel B, lane 9, positive
CU29	A_PETn9	Diff Output	Differential transmit signal, channel A, lane 9, negative
CV1	A_PERn9	Diff Input	Differential receive signal, channel A, lane 9, negative
CV35	B_PERp9	Diff Input	Differential receive signal, channel B, lane 9, positive
CW13	GND	Ground	Ground
CW17	VCC3	Power	3.3 V Supply Voltage
CW20	VCC3	Power	3.3 V Supply Voltage
CW22	GND	Ground	Ground
CW32	GND	Ground	Ground
CW4	GND	Ground	Ground
CY2	GND	Ground	Ground
CY34	GND	Ground	Ground

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
DA1	GND	Ground	Ground
DA35	GND	Ground	Ground
DB26	A_PETp10	Diff Output	Differential transmit signal, channel A, lane 10, positive
DB7	B_PETn10	Diff Output	Differential transmit signal, channel B, lane 10, negative
DC2	A_PERn10	Diff Input	Differential receive signal, channel A, lane 10, negative
DC34	B_PERp10	Diff Input	Differential receive signal, channel B, lane 10, positive
DD10	B_PETp10	Diff Output	Differential transmit signal, channel B, lane 10, positive
DD29	A_PETn10	Diff Output	Differential transmit signal, channel A, lane 10, negative
DE1	A_PERp10	Diff Input	Differential receive signal, channel A, lane 10, positive
DE35	B_PERn10	Diff Input	Differential receive signal, channel B, lane 10, negative
DF13	GND	Ground	Ground
DF17	VCC3	Power	3.3 V Supply Voltage
DF20	VCC3	Power	3.3 V Supply Voltage
DF22	GND	Ground	Ground
DF32	GND	Ground	Ground
DF4	GND	Ground	Ground
DG2	GND	Ground	Ground
DG34	GND	Ground	Ground
DH1	GND	Ground	Ground
DH35	GND	Ground	Ground
DJ26	A_PETp11	Diff Output	Differential transmit signal, channel A, lane 11, positive
DJ7	B_PETn11	Diff Output	Differential transmit signal, channel B, lane 11, negative
DK2	A_PERn11	Diff Input	Differential receive signal, channel A, lane 11, negative
DK34	B_PERp11	Diff Input	Differential receive signal, channel B, lane 11, positive
DL10	B_PETp11	Diff Output	Differential transmit signal, channel B, lane 11, positive
DL29	A_PETn11	Diff Output	Differential transmit signal, channel A, lane 11, negative
DM1	A_PERp11	Diff Input	Differential receive signal, channel A, lane 11, positive
DM35	B_PERn11	Diff Input	Differential receive signal, channel B, lane 11, negative
DN13	GND	Ground	Ground
DN17	VCC3	Power	3.3 V Supply Voltage
DN20	VCC4	Power	3.3 V Supply Voltage
DN22	GND	Ground	Ground
DN32	GND	Ground	Ground
DN4	GND	Ground	Ground
DP2	GND	Ground	Ground
DP34	GND	Ground	Ground
DR1	GND	Ground	Ground
DR35	GND	Ground	Ground
DT26	A_PETp12	Diff Output	Differential transmit signal, channel A, lane 12, positive
DT7	B_PETn12	Diff Output	Differential transmit signal, channel B, lane 12, negative
DU2	A_PERp12	Diff Input	Differential receive signal, channel A, lane 12, positive
DU34	B_PERn12	Diff Input	Differential receive signal, channel B, lane 12, negative
DV10	B_PETp12	Diff Output	Differential transmit signal, channel B, lane 12, positive
DV29	A_PETn12	Diff Output	Differential transmit signal, channel A, lane 12, negative

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
DW1	A_PERn12	Diff Input	Differential receive signal, channel A, lane 12, negative
DW35	B_PERp12	Diff Input	Differential receive signal, channel B, lane 12, positive
DY13	GND	Ground	Ground
DY17	VCC4	Power	3.3 V Supply Voltage
DY20	VCC4	Power	3.3 V Supply Voltage
DY22	GND	Ground	Ground
DY32	GND	Ground	Ground
DY4	GND	Ground	Ground
EA2	GND	Ground	Ground
EA34	GND	Ground	Ground
EB1	GND	Ground	Ground
EB35	GND	Ground	Ground
EC26	A_PETp13	Diff Output	Differential transmit signal, channel A, lane 13, positive
EC7	B_PETn13	Diff Output	Differential transmit signal, channel B, lane 13, negative
ED2	A_PERp13	Diff Input	Differential receive signal, channel A, lane 13, positive
ED34	B_PERn13	Diff Input	Differential receive signal, channel B, lane 13, negative
EE10	B_PETp13	Diff Output	Differential transmit signal, channel B, lane 13, positive
EE29	A_PETn13	Diff Output	Differential transmit signal, channel A, lane 13, negative
EF1	A_PERn13	Diff Input	Differential receive signal, channel A, lane 13, negative
EF35	B_PERp13	Diff Input	Differential receive signal, channel B, lane 13, positive
EG13	GND	Ground	Ground
EG17	VCC4	Power	3.3 V Supply Voltage
EG20	VCC4	Power	3.3 V Supply Voltage
EG22	GND	Ground	Ground
EG32	GND	Ground	Ground
EG4	GND	Ground	Ground
EH2	GND	Ground	Ground
EH34	GND	Ground	Ground
EJ1	GND	Ground	Ground
EJ35	GND	Ground	Ground
EK26	A_PETp14	Diff Output	Differential transmit signal, channel A, lane 14, positive
EK7	B_PETn14	Diff Output	Differential transmit signal, channel B, lane 14, negative
EL2	A_PERn14	Diff Input	Differential receive signal, channel A, lane 14, negative
EL34	B_PERp14	Diff Input	Differential receive signal, channel B, lane 14, positive
EM10	B_PETp14	Diff Output	Differential transmit signal, channel B, lane 14, positive
EM29	A_PETn14	Diff Output	Differential transmit signal, channel A, lane 14, negative
EN1	A_PERp14	Diff Input	Differential receive signal, channel A, lane 14, positive
EN35	B_PERn14	Diff Input	Differential receive signal, channel B, lane 14, negative
EP13	GND	Ground	Ground
EP17	VCC4	Power	3.3 V Supply Voltage
EP20	VCC4	Power	3.3 V Supply Voltage
EP22	GND	Ground	Ground
EP32	GND	Ground	Ground
EP4	GND	Ground	Ground

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
ER2	GND	Ground	Ground
ER34	GND	Ground	Ground
ET1	GND	Ground	Ground
ET35	GND	Ground	Ground
EU26	A_PETp15	Diff Output	Differential transmit signal, channel A, lane 15, positive
EU7	B_PETn15	Diff Output	Differential transmit signal, channel B, lane 15, negative
EV2	A_PERn15	Diff Input	Differential receive signal, channel A, lane 15, positive
EV34	B_PERp15	Diff Input	Differential receive signal, channel B, lane 15, positive
EW10	B_PETp15	Diff Output	Differential transmit signal, channel B, lane 15, negative
EW29	A_PETn15	Diff Output	Differential transmit signal, channel A, lane 15, negative
EY1	A_PERp15	Diff Input	Differential receive signal, channel A, lane 15, positive
EY35	B_PERn15	Diff Input	Differential receive signal, channel B, lane 15, negative
FA15	GND	Ground	Ground
FA32	GND	Ground	Ground
FB2	GND	Ground	Ground
FB34	GND	Ground	Ground
FC19	GND	Ground	Ground
FC23	GND	Ground	Ground
FC25	GND	Ground	Ground
FC28	GND	Ground	Ground
FC3	GND	Ground	Ground
FC6	GND	Ground	Ground
FC9	GND	Ground	Ground
FD1	GND	Ground	Ground
FD35	GND	Ground	Ground
FE2	N/C	—	No internal connection.
FE34	N/C	—	No internal connection.
FF11	RSVD2	—	Reserved for future use. No internal connection.
FF14	GND	Ground	Ground
FF18	RSVD6	—	Reserved for future use. No internal connection.
FF21	GND	Ground	Ground
FF24	MODE	Input	5-level input strap pin. Sets device control configuration modes. The pin can be exercised at device power up or in normal operation mode. L1: SMBus/I2C Primary Mode - device control configuration is read from external EEPROM. When the device has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I2C secondary operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I2C primary wants to access the device registers it must support arbitration. To set the pin for L1 pull-down with 2.062 kΩ±10% resistor. L2: SMBus/I2C Secondary Mode – device control configuration is done by an external controller with SMBus/I2C primary. To set the pin for L1 pull-down with 18.75 kΩ±10% resistor. L0, L3 and L4: RESERVED – TI internal test modes.

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
FF27	ALL_DONE#	Output	EEPROM loading is done. Active low 3.3 V open drain output pin. The pin can be left unconnected. In *SMBus/I2C Primary Mode*: Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7 kΩ required for operation. • High: External EEPROM load failed or incomplete • Low: External EEPROM load successful and complete In *SMBus/I2C secondary*: The pin is High-Z.
FF30	B_ADDR1_15-8	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
FF33	PD_3-0	Input	3.3 V LVCMOS input. Implements device power-down /reset according to Table 7-1.
FF5	A_ADDR0_15-8	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
FF8	PD_15-12	Input	3.3 V LVCMOS input. Implements device power-down /reset according to Table 7-1.
FG1	N/C	—	No internal connection.
FG35	N/C	—	No internal connection.
FH2	N/C	—	No internal connection.
FH34	N/C	—	No internal connection.
FJ12	GND	Ground	Ground
FJ16	RSVD5	—	Reserved for future use. No internal connection.
FJ19	GND	Ground	Ground
FJ23	RSVD1	Input	TI internal use. Leave unconnected.
FJ25	READ_EN_#	Input	Initiate EEPROM load. Active low 3.3 V LVCMOS input.. In *SMBus/I2C Primary Mode*: After device power up, when the pin is low, it initiates the EEPROM read function. Once EEPROM read is complete (indicated by ALL_DONE# asserted low), this pin can be held low for normal device operation. During the EEPROM load process the device's signal path is disabled. In *SMBus/I2C Secondary*: In these modes the pin is not used. The pin can be left floating. The pin has internal 1-MΩ weak pulldown resistor.
FJ28	B_ADDR0_15-8	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
FJ3	A_ADDR1_15-8	Input	5-level input strap pins as defined in Table 7-2. Sets SMBus/I2C secondary address according to Table 7-1 and Table 7-3.
FJ31	PD_7-4	Input	3.3 V LVCMOS input. Implements device power-down /reset according to Table 7-1.
FJ6	PD_11-8	Input	3.3 V LVCMOS input. Implements device power-down /reset according to Table 7-1.
FJ9	RSVD0	Input	TI internal use. Leave unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply Voltage (VCC)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3 V LVCMOS and Open Drain I/O voltage	–0.5	4.0	V
$VIO_{5LVL,ABSMAX}$	5-level Input I/O voltage	–0.5	2.75	V
$VIO_{HS\text{-}RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS\text{-}TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD and Latchup Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
$V_{(Signal+)}$	Positive signal pin latch-up	Signal pin test, per JESD78F class II, immunity level A (all signal pins)	+100	mA
$V_{(Signal-)}$	Negative signal pin latch-up	Signal pin test, per JESD78F class II, immunity level A (all signal pins except RX pins)	-100	
		Signal pin test, per JESD78F class II, immunity level B, annex A flow 1F (RX pins are connected through 75nF - 265 nF capacitors)(3)	-100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Per annex A flow 1F, negative pulse immunity on RX pins is –50 mA without series capacitors.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance	DC to <50 Hz, sinusoidal[1]			250	mVpp
		50 Hz to 500 kHz, sinusoidal[1]			100	mVpp
		500 kHz to 2.5 MHz, sinusoidal[1]			33	mVpp
		Supply noise, >2.5 MHz, sinusoidal[1]			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T_J	Operating junction temperature		–40		120	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PD1/0, and READ_EN_N	200			µs
VCC_{SMBUS}	SMBus/I²C SDA and SCL Open Drain Termination Voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency in secondary mode		10		400	kHz

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate		1		16	Gbps

6.4 Thermal Information

THERMAL METRIC(1)		DSPR16 NJX, 64 Pins	UNIT
$R_{\theta JA\text{-}High\ K}$	Junction-to-ambient thermal resistance	17.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
P_{ACT}	Device active power	32-channels (16-lanes), EQ = 0-3		4.7	6.0	W
P_{ACT}	Device active power	32-channels (16-lanes), EQ = 4-19		5.8	7.0	W
P_{RXDET}	Device power consumption while waiting for far end receiver terminations	All channels enabled but no far end receiver detected		660		mW
P_{STBY}	Device power consumption in standby power mode	All channels disabled		92		mW
Control IO						
V_{OH}	High level output voltage	$R_{pull\text{-}up}$ = 4.7 kΩ (SDA, SCL, ALL_DONE_N pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = –4 mA (SDA, SCL, ALL_DONE_N pins)			0.4	V
I_{IH}	Input high leakage current	V_{Input} = VCC, (SCL, SDA, PD, READ_EN_N pins)			40	µA
I_{IL}	Input low leakage current	V_{Input} = 0 V, (SCL, SDA, PD, READ_EN_N pins)	-40			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6 V, VCC = 0 V, (SCL, SDA, PD, READ_EN_N pins)			800	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SDA, SCL, PD, READ_EN_Npins		1.2		pF
5 Level IOs (MODE, A/B_ADDR pins)						
I_{IH_5L}	Input high leakage current, 4 level IOs	VIN = 2.5 V			40	µA
I_{IL_5L}	Input low leakage current for all 4 level IOs except MODE.	VIN = GND	-40			µA
$I_{IL\_5L,MODE}$	Input low leakage current for MODE pin	VIN = GND	-800			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	RX DC Common Mode Voltage	Device is in active or standby state		1.4		V

6.5 DC Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{RX-DC}	Rx DC Single-Ended Impedance			50		Ω
$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance during Reset or power-down	Inputs are at $V_{RX-DC-CM}$ voltage	15			kΩ
Transmitter						
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	Impedance of Tx during active signaling, VID,diff = 1Vpp		100		Ω
$V_{TX-DC-CM}$	Tx DC common mode Voltage			1.0		V
$I_{TX-SHORT}$	Tx Short Circuit Current	Total current the Tx can supply when shorted to GND		70		mA

6.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	50 MHz to 1.25 GHz		-20		dB
		1.25 GHz to 2.5 GHz		-19		dB
		2.5 GHz to 4.0 GHz		-16		dB
		4.0 GHz to 8.0 GHz		-12		dB
RL_{RX-CM}	Input common-mode return loss	50 MHz to 2.5 GHz		-15		dB
		2.5 GHz to 8.0 GHz		-15		dB
XT_{RX}	Receive-side pair-to-pair isolation	Pair-to-pair isolation (SDD21) between two adjacent receiver pairs from 10 MHz to 8 GHz.		-50		dB
Transmitter						
$V_{TX-AC-CM-PP}$	Tx AC Peak-to-Peak Common Mode Voltage	Measured with lowest EQ, flat_gain = 101			50	mVpp
$V_{TX-RCV-DETECT}$	Amount of Voltage change allowed during Receiver Detection	Measured while Tx is sensing whether a low-impedance Receiver is present. No load is connected to the driver output	0		600	mV
$RL_{TX-DIFF}$	Output differential return loss	50 MHz to 1.25 GHz		-19		dB
		1.25 GHz to 2.5 GHz		-17		dB
		2.5 GHz to 4.0 GHz		-12		dB
		4.0 GHz to 8.0 GHz		-10		dB
RL_{TX-CM}	Output Common-mode return loss	50 MHz to 2.5 GHz		-14		dB
		2.5 GHz to 8.0 GHz		-12		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent transmitter pairs from 10 MHz to 8 GHz.		-50		dB
$C_{AC,TX}$	AC coupling capacitors on transmit pins			220		nF
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either Low-to-High or High-to-Low transition.		130	170	ps
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	Between any two lanes within a single transmitter.			24	ps

6.6 High Speed Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{RJ-DATA}$	Additive Random Jitter with data	Jitter through redriver minus the calibration trace. 16 Gbps PRBS15. 800 mVpp-diff input swing.		100		fs
$T_{RJ-INTRINSIC}$	Intrinsic additive Random Jitter with clock	Jitter through redriver minus the calibration trace. 8 Ghz CK. 800 mVpp-diff input swing.		100		fs
$JITTER_{TOTAL-DATA}$	Additive Total Jitter with data	Jitter through redriver minus the calibration trace. 16 Gbps PRBS15. 800 mVpp-diff input swing.		2.0		ps
$JITTER_{TOTAL-INTRINSIC}$	Intrinsic additive Total Jitter with clock	Jitter through redriver minus the calibration trace. 8 Ghz CK. 800 mVpp-diff input swing.		1.3		ps
$EQ\text{-}MIN_{8G}$	EQ boost at min setting (EQ INDEX = 0)	AC gain at 8 GHz relative to gain at 100 MHz.		1.7		dB
$EQ\text{-}MAX_{8G}$	EQ boost at max setting (EQ INDEX = 19)	AC gain at 8 GHz relative to gain at 100 MHz.		16		dB
$FLAT\text{-}GAIN_{VAR}$	Flat gain variation across PVT measured at DC	Flat_gain = 000, 001, 011, 101 or 111, at minimum EQ setting. Max-Min for a single channel.	-1.0		1.0	dB
$EQ\text{-}GAIN_{VAR,8G}$	EQ boost variation across PVT	At 8 Ghz. Flat_gain = 101, maximum EQ setting. Max-Min for a single channel.	-1.5		1.5	dB
LINEARITY-DC	Output DC Linearity	Flat_gain = 101. 128T pattern at 2.5 Gbps.		1800		mVpp
LINEARITY-AC	Output AC Linearity	Flat_gain = 101. 1T pattern at 16 Gbps.		1000		mVpp

6.7 SMBUS/I2C Timing Charateristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Secondary Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU-STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD-DAT}	Data hold time		0			µs
T_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		120		ns
t_f	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		2		ns
t_{SU-STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid acknowledge time				0.9	µs
C_b	Capacitive load for each bus line				400	pF

6.7 SMBUS/I2C Timing Charateristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Primary Mode						
f_{SCL-M}	SCL clock frequency	MODE = L1 (Primary Mode)		303		kHz
t_{LOW-M}	SCL low period			1.90		µs
T_{HIGH-M}	SCL high period			1.40		µs
$t_{SU-STA-M}$	Set-up time for a repeated START condition			2		µs
$t_{HD-STA-M}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated			1.5		µs
$T_{SU-DAT-M}$	Data setup time			1.4		µs
$t_{HD-DAT-M}$	Data hold time			0.5		µs
t_{R-M}	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		120		ns
T_{F-M}	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		2		ns
$t_{SU-STO-M}$	Stop condition setup time			1.5		µs
EEPROM Timing						
T_{EEPROM}	EEPROM configuration load time	Time to assert ALL_DONE_N after READ_EN_N has been asserted.		30		ms
T_{POR}	Time to first SMBus access	Power supply stable after initial ramp. Includes initial power-on reset time.		50		ms

6.8 Typical Characteristics

Figure 6-1 shows typical EQ gain curves versus frequency for different EQ settings for the DS160PR1601. Figure 6-2 shows typical differential return loss for Rx and Tx pins.

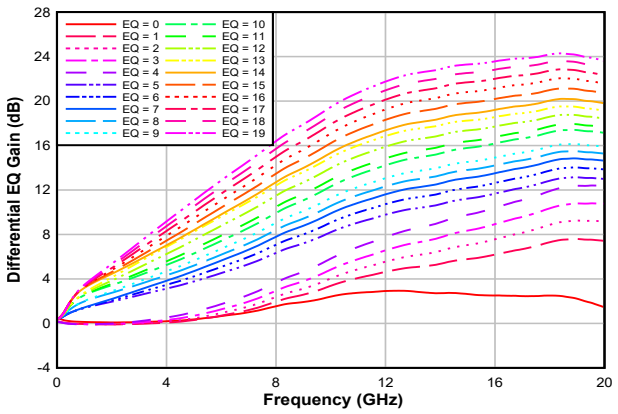


Figure 6-1. Typical EQ Boost vs Frequency

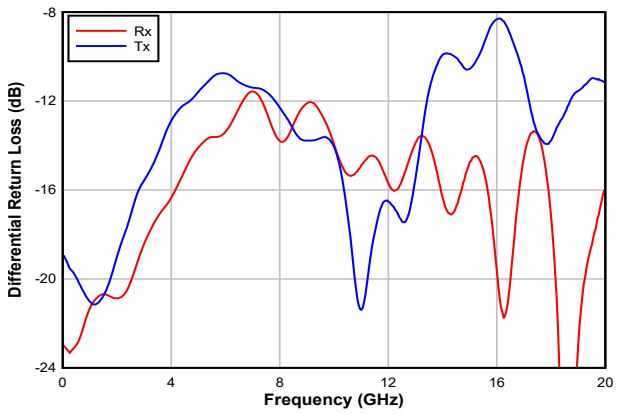


Figure 6-2. Typical Differential Return Loss

6.9 Typical Jitter Characteristics

Figure 6-3 and Figure 6-4 show eye diagrams through calibration traces, and through the DS160PR1601 respectively. Note: DS160PR1601 adds little to no random or deterministic jitter.

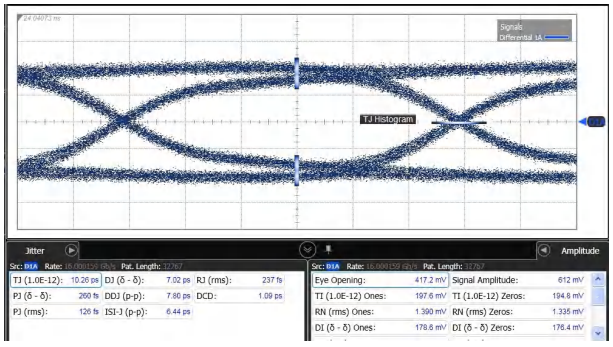


Figure 6-3. Through Baseline Calibration Trace Setup (10.26 ps Total Jitter Including Source)

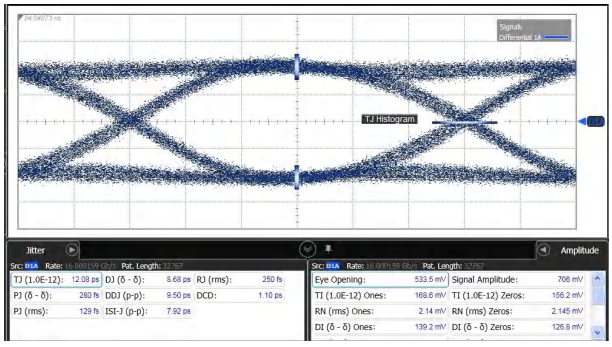


Figure 6-4. Through the DS160PR1601 with DUT EQ = 0 (12.08ps Total Jitter – Very Little Added Jitter Due to Redriver)

7 Detailed Description

7.1 Overview

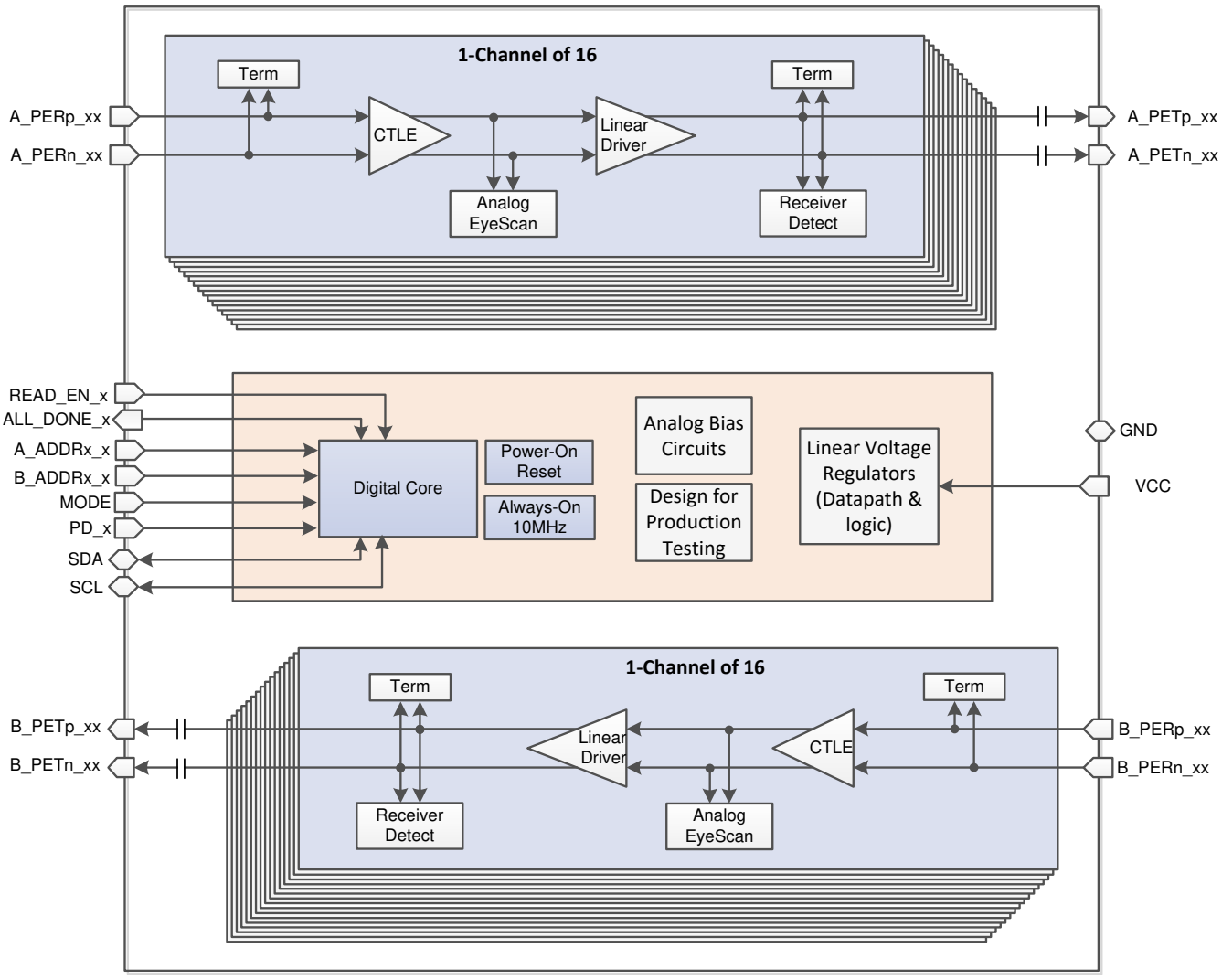
The DS160PR1601 is a 16-lane multi-rate linear repeater with integrated signal conditioning. The device's signal channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

The DS160PR1601 can be configured two different ways:

SMBus/I^{2}C Primary mode – device control configuration is read from external EEPROM. When the DS160PR1601 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I^{2}C secondary operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I^{2}C primary wants to access DS160PR1601 registers it must support arbitration. The mode is prefferred when software implementation is not desired.

SMBus/I^{2}C Secondary mode – provides most flexibility. Requires a SMBus/I^{2}C primary device to configure DS160PR1601 though writing to its secondary address.

7.2 Functional Block Diagram



7.3 Control and Configuration Interface

7.3.1 Pin Configurations for Lanes

The DS160PR1601 has 16 data lanes with 16-Tx channels and 16-Rx channels. The data channels are grouped for I2C configurations and PCIe state machine grouping as shown in Figure 7-1 using xADDRx and PDx pins. Table 7-1 defines the channel grouping.

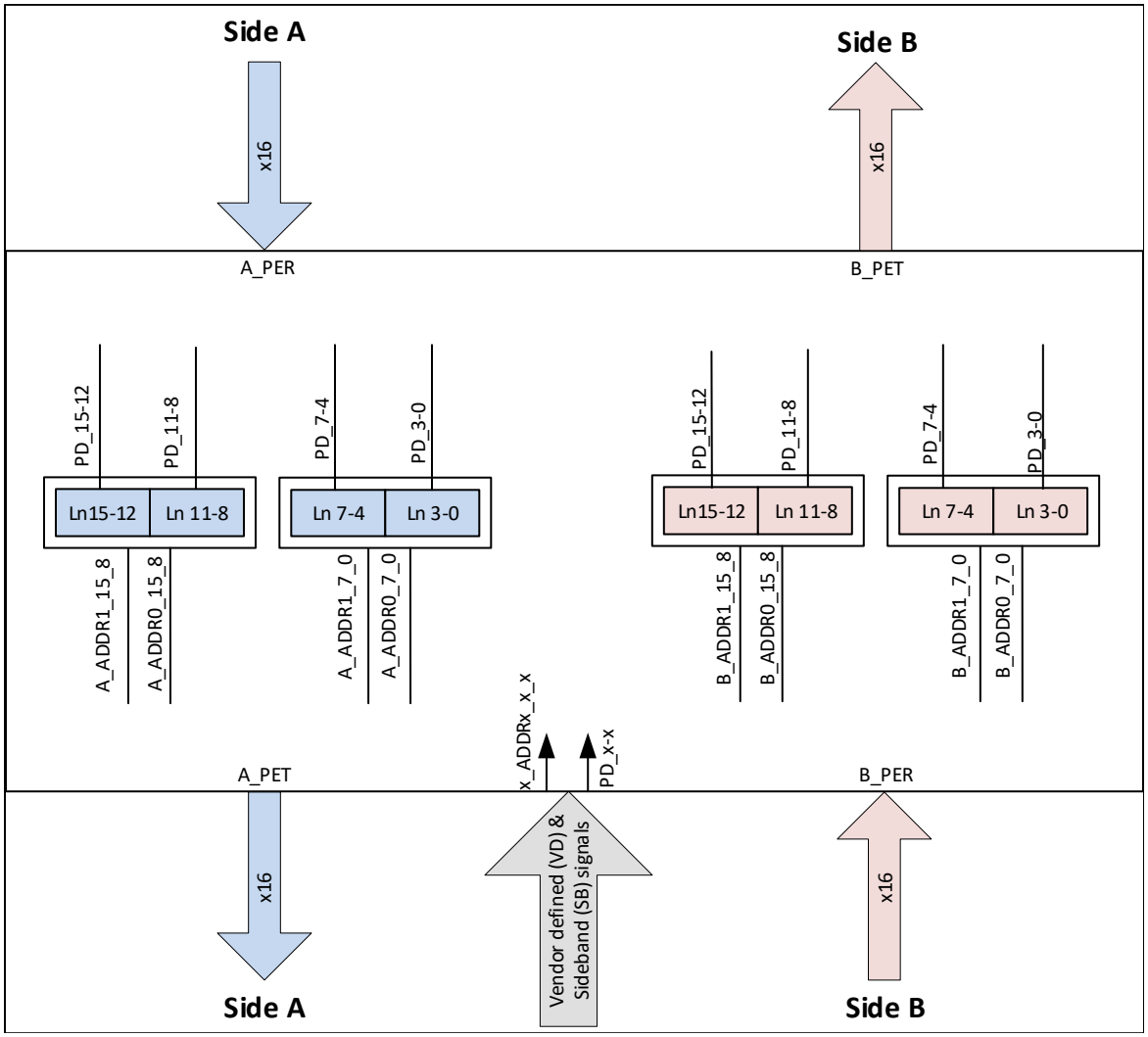


Figure 7-1. Pin Configurations for Lanes

Table 7-1. Definition of PDx and xADDRx pins

Pin Name	Description
PD_15-12 PD_11-8 PD_7-4 PD_3-0	Active in all device control modes. The pin has internal 1-MΩ weak pulldown resistor. The pin triggers PCIe RX detect state machine when toggled. • High: power down • Low: power up normal operation. Each PD pin sets control for a bank of 8 lanes (4 from Side A and 4 from Side B) to provide flexibility for x4 and x8 bifurcation: • PD_15-12: Lanes 15-12, both Side A and B • PD_11-8: Lanes 11-8, both Side A and B • PD_7-4: Lanes 7-4, both Side A and B • PD_3-0: Lanes 3-0, both Side A and B PCIe hot plug insertion implementation varies from system to system. One way to implement will be to use CEM interface PRSNT# signal. For PCIe x16 application all four PD signals can be shorted together and connect to CEM interface PRSNT# signal.
A_ADDR1_15-8 A_ADDR0_15-8 A_ADDR1_7-0 A_ADDR0_7-0 B_ADDR1_15-8 B_ADDR0_15-8 B_ADDR1_7-0 B_ADDR0_7-0	5-level input pins as implemented by pull-down resistor on the pin according to Table 7-2. These pins are sampled at device power-up only. Sets SMBus / I2C secondary address according to Table 7-3. Each set of ADDR1 and ADDR0 pins defines the addresses for bank of 8 lanes: • A_ADDR1_15-8, A_ADDR0_15-8: Lanes 15-8 of Side A • A_ADDR1_7-0, A_ADDR0_7-0: Lanes 7-0 of Side A • B_ADDR1_15-8, B_ADDR0_15-8: Lanes 15-8 of Side B • B_ADDR1_7-0, B_ADDR0_7-0: Lanes 7-0 of Side B Figure 7-1 shows how I2C secondary addresses are accessed for specific lanes.

7.3.1.1 Five-Level Control Inputs

The has 5-level inputs pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The pins are sampled at power-up only.

Table 7-2. 5-level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L4	F (Float)

7.3.2 SMBUS/I^{2}C Register Control Interface

If MODE = L2 (SMBus / I^{2}C secondary control mode), the DS160PR1601 is configured through a standard I^{2}C or SMBus interface that may operate up to 400 kHz. The device also can be configured through loading settings from EEPROM. The SMBus / I^{2}C primary / secondary address of the DS160PR1601 is determined by the pin strap settings on the xADDRx pins. Note addresses to access differental channels are different. To illustrate A_ADDR1_15_8 and A_ADDR0_15_8 sets the primary / secondary address for bank of lanes 15-12 and 11-8 of Side A, while A_ADDR1_7_0 and A_ADDR0_7_0 sets for bank of lanes 7-4 and 3-0 of Side A. B side address is also set similarly. Table 7-3 show SMBus / I^{2}C primary / secondary addresses.

Table 7-3. SMBus / I²C Primary / Secondary Address

x_ADDR1_x	x_ADDR0_x	7-bit address Upper (for Side A) / Lower (for Side B) 4 Lanes of each Bank	7-bit address Lower (for Side A) / Upper (for Side B) 4 Lanes of each Bank
L0	L0	0x19	0x18
L0	L1	0x1B	0x1A
L0	L2	0x1D	0x1C
L0	L3	0x1F	0x1E
L0	L4	Reserved	Reserved
L1	L0	0x21	0x20
L1	L1	0x23	0x22
L1	L2	0x25	0x24
L1	L3	0x27	0x26
L1	L4	Reserved	Reserved
L2	L0	0x29	0x28
L2	L1	0x2B	0x2A
L2	L2	0x2D	0x2C
L2	L3	0x2F	0x2E
L2	L4	Reserved	Reserved
L3	L0	0x31	0x30
L3	L1	0x33	0x32
L3	L2	0x35	0x34
L3	L3	0x37	0x36
L3	L4	Reserved	Reserved

In SMBus/I²C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 50 pF.

Refer to the *DS160PR1601 Programming Guide* for detail register sets and control configuration procedures.

7.3.3 SMBus/I²C Primary Mode Configuration (EEPROM Self Load)

The DS160PR1601 can also be configured by reading from EEPROM. To enter into this mode MODE pin must be set to L1. The EEPROM load operation only happens once after device's initial power-up. If the DS160PR1601 is configured for SMBus primary mode, it will remain in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. After the READ_EN_N pin is driven LOW, the DS160PR1601 becomes an SMBus primary and attempts to self-configure by reading device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the DS160PR1601 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C secondary operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I²C primary wants to access DS160PR1601 registers it must support arbitration.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2 kb (256 × 8-bit) is recommended.
- Set MODE = L1, configure for SMBus primary mode
- The external EEPROM device address byte must be 0xA0 and capable of 400 kHz operation at 3.3 V supply
- In SMBus/I²C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Refer to the *DS160PR1601 Programming Guide* for detail register sets and control configuration procedures.

7.4 Feature Description

7.4.1 Linear Equalization

The DS160PR1601 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The device has 20 available equalization boost settings that can be set though SMBus/I^{2}C registers. Table 7-4 shows the device EQ settings.

Refer to the *DS160PR1601 Programming Guide* for detail register sets and control configuration procedures.

Table 7-4. Equalization Control Settings

EQ INDEX	TYPICAL EQ BOOST (dB) at 8 GHz
0	2.0
1	3.5
2	5.0
3	7.0
4	8.0
5	9.0
6	9.8
7	10.2
8	10.8
9	11.2
10	11.8
11	12.2
12	12.8
13	13.2
14	13.8
15	14.2
16	14.8
17	15.2
18	15.6
19	16.0

7.4.2 Flat-Gain

The overall datapath Flat-Gain (DC and AC) of the DS160PR1601 can be programmed through SMBus/I^{2}C registers. Table 7-5 shows five available flat gain settings to configure the DS160PR1601 datapaths.

Table 7-5. Flat Gain Settings

Flat_gain	SETTING
000	-6 dB
001	-4 dB
011	-2 dB
101	0 dB (default and recommended)
111	+2dB

The default recommendation for most systems will be 0 dB.

The Flat-Gain and equalization of the DS160PR1601 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

Refer to the *DS160PR1601 Programming Guide* for detail register sets and control configuration procedures.

7.4.3 Analog EyeScan

The DS160PR1601 implements Analog EyeScan feature that enables monitoring of the internal eye for each data channel after the receiver CTLE stage. It provides a measure of vertical eye opening estimation using signal statistics. The Analog EyeScan feature is useful for redriver tuning to choose CTLE and Flat-Gain settings to optimize an electrical link between a transmitter and a receiver. This is also useful for hardware engineers for initial system bring-up and at field system diagnostics. The EyeScan feature can be invoked by I^2C or SMBus interface.

7.4.4 Receiver Detect State Machine

The DS160PR1601 deploys an RX detect state machine that governs the RX detection cycle as defined in the PCI express specifications. At power up, after a manually triggered event through PDx pins, or writing to the relevant I^2C/SMBus register, the redriver determines whether or not a valid PCI express termination is present at the far end of the link. The Rx Detect Registers provide additional flexibility for system designers to appropriately set the device in desired mode through SMBus/I^2C control interface.

7.4.5 Integrated Capacitors

The DS160PR1601 has intergrated AC coupling caps for all TX pins (64 count). The capacitors are 220 nF each with 2.5 V voltage rating and 20% tolerance.

7.5 Device Functional Modes

7.5.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled through SMBus/I^2C registers. In this mode PDx pins are driven low in a system (for example by PCIE connector "PRSNT" or inverted "PERST" signal). In this mode, the DS160PR1601 redrives and equalizes PCIe RX or TX signals to provide better signal integrity.

7.5.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled through I^2C registers. This mode is recommended for non-PCIe use cases. In this mode the device is working as a buffer to provide linear equalization to improve signal integrity.

7.5.3 Standby Mode

The device is in standby mode invoked by PDx pins. In this mode, the device is in standby mode conserving power.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS160PR1601 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The DS160PR1601 is a 16-lane protocol agnostic PCI Express linear redriver. Its protocol agnostic nature allows it to be used in PCI Express x4, x8, and x16 applications. Figure 8-1 shows how single DS160PR1601 can be used in four x4, two x8 or single x16 links.

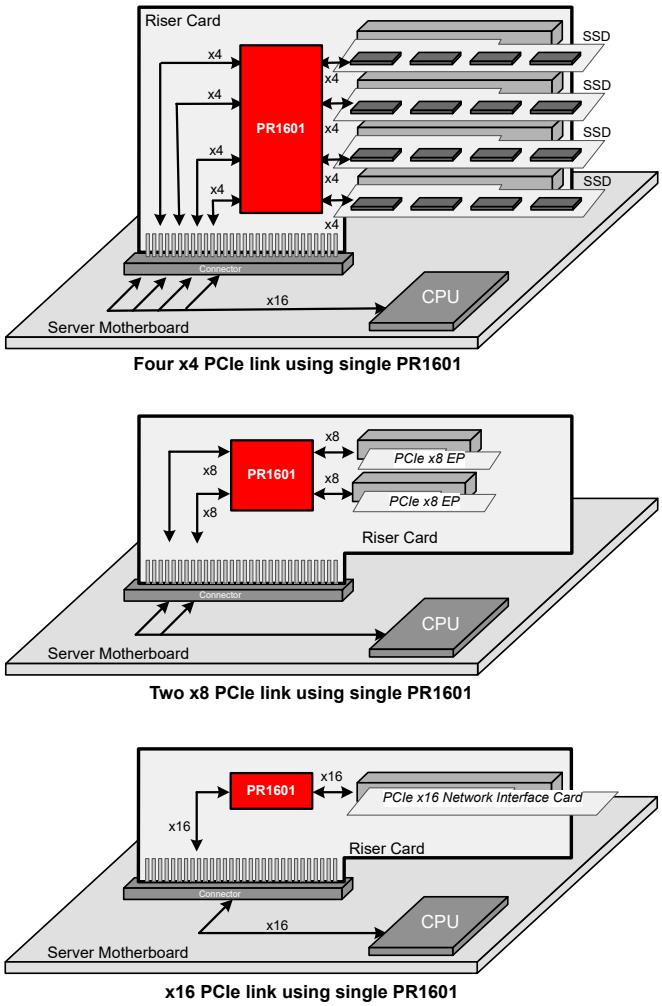


Figure 8-1. PCI Express x4, x8, and x16 Implementation Using DS160PR1601

8.2.1 PCIe x16 Lane Configuration

The DS160PR1601 can be used in server or motherboard applications to boost transmit and receive signals to increase the reach of the host or root complex processor to PCI Express slots or connectors. The section outlines detailed procedure and design requirement for a typical PCIe x16 lane confuration. However, the design recommendations can also be used in x4 or x8 lane configuration.

8.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-end segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

In PCIe Gen 3.0 and 4.0 applications, the specification requires Rx-Tx (of root-complex and endpoint) link training to establish and optimize signal conditioning settings. In link training, the Rx partner requests a series of FIR – preshoot and deemphasis coefficients (10 Presets) from the Tx partner. The Rx partner includes 7-levels of CTLE followed by a single tap DFE. The link training would pre-condition the signal, with an equalized link between the root-complex and endpoint resulting an optimized link. Note that there is no link training in PCIe Gen 1.0 (2.5 Gbps) or PCIe Gen 2.0 (5.0 Gbps) applications.

The DS160PR1601 is designed with linear datapth to pass the Tx Preset signaling (by root complex and end point) onto the Rx (of root complex and end point) for a PCIe link to train and optimize for the Rx equalization settings. The linear redriver helps extend the PCB trace reach distance by boosting the attenuated signals with its own equalization, which allows the Rx to recover signals more easily. The device must be placed in between the Tx and Rx (of root complex and end point) such a way that signal swing of both upstream and downstream signals stays within the linearity range of the device. Adjustments to the DS160PR1601 EQ setting should be performed based on the channel loss to optimize the eye opening in the Rx partner. The available EQ gain settings are provided in Table 7-4. For most PCIe systems the default Flat gain setting of 0 dB (flat_gain = 101) would be sufficient.

The DS160PR1601 can be optimized for a given system utlizing its two configuration modes – SMBus/I^2C Primary mode and SMBus/I^2C Secondary mode. In SMBus/I^2C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Figure 8-2 shows a simplified schematic for x16 lane configuration in SMBus/I2C Primary mode.

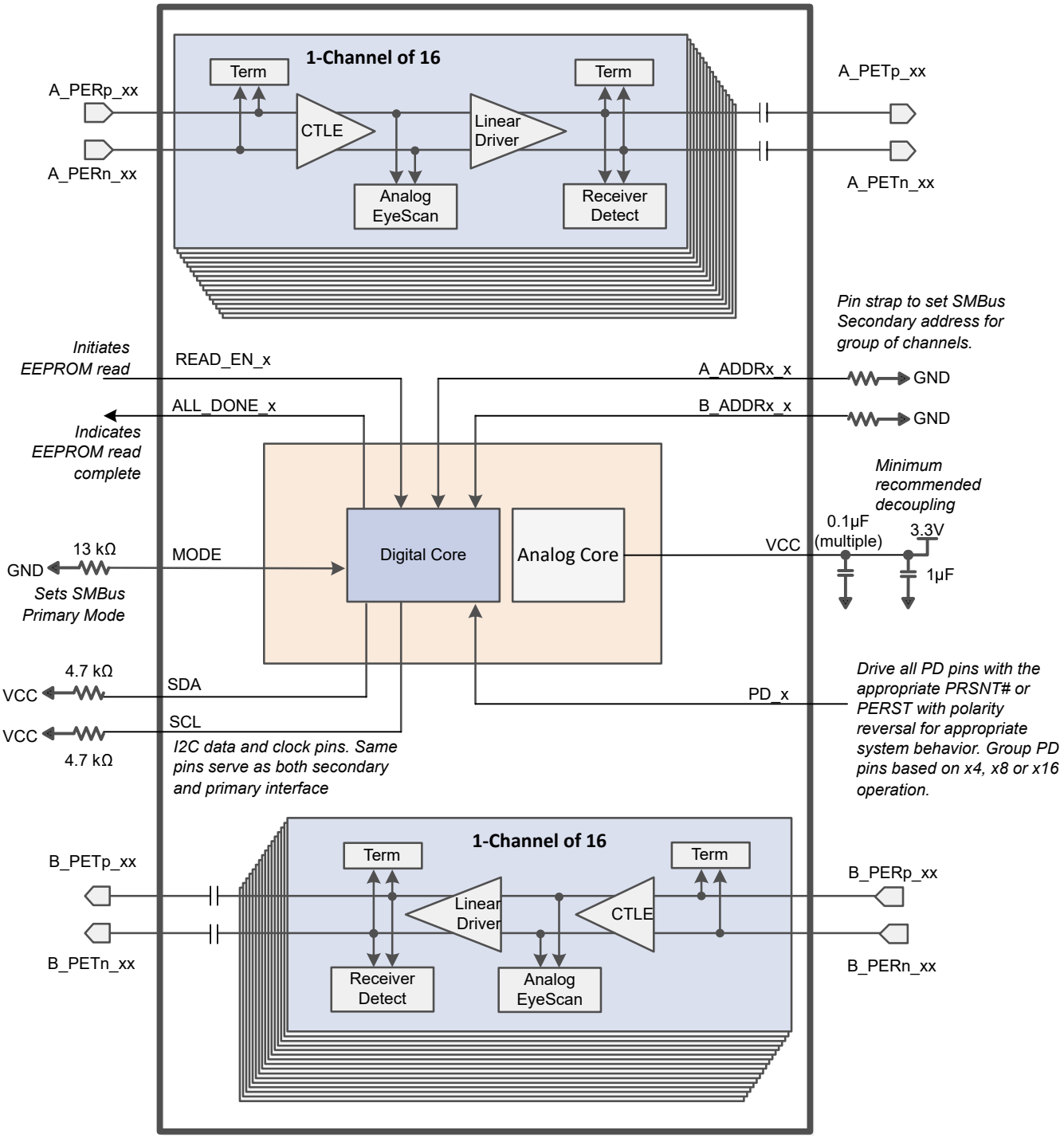


Figure 8-2. Simplified Schematic for PCIe x16 Lane Configuration in SMBus/I2C Primary Mode

8.2.1.3 Application Curves

The DS160PR1601 is a linear redriver that can be used to extend channel reach of a PCIe link. Normally, PCIe-compliant Tx and Rx are equipped with signal-conditioning functions and can handle channel losses of up to 28 dB at 16 Gbps (8 GHz) PCIe 4.0. With the DS160PR1601, the total channel loss between a PCIe root complex and an end point can be extended up to 42 dB (16 dB additional) at 8 GHz.

To demonstrate the reach extension capability of the DS160PR1601, two comparative setups are constructed. In first setup as shown in Figure 8-3 there is no redriver in the PCIe 5.0 link. Figure 8-4 shows eye diagram at the end of the link using SigTest. In second setup as shown in Figure 8-5, the DS160PR1601 is inserted in the middle to extend link reach. Figure 8-6 shows SigTest eye diagram.

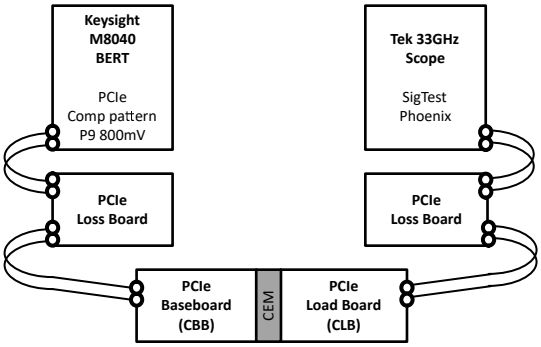


Figure 8-3. PCIe 4.0 Link Baseline Setup Without Redriver – Link Elements

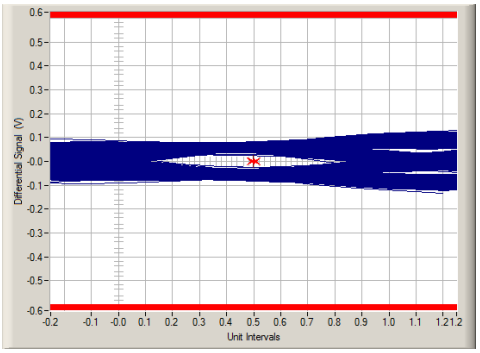


Figure 8-4. PCIe 4.0 link Baseline Setup Without Redriver – Eye Diagram Using SigTest

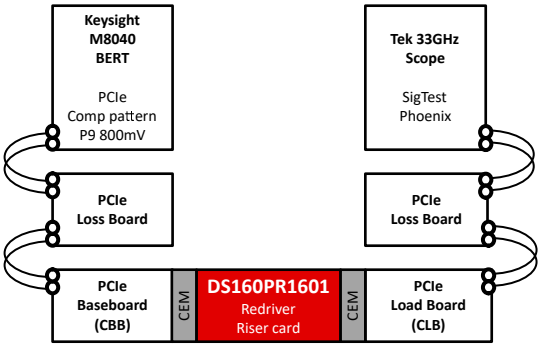


Figure 8-5. PCIe 4.0 Link Setup with the DS160PR1601 – the Link Elements

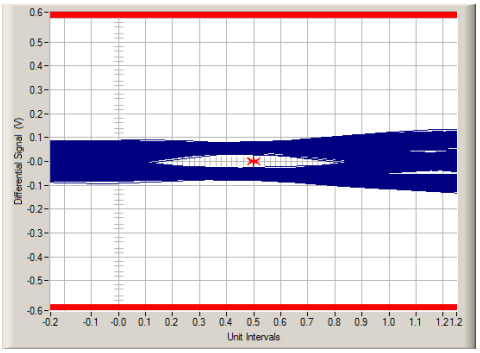


Figure 8-6. PCIe 4.0 Link Setup with the DS160PR1601 – Eye Diagram Using SigTest

Table 8-1 summarizes the PCIe 4.0 links without and with the DS160PR1601. The illustration shows that redriver is capable of ≅16 dB (additional) reach extension at PCIe 4.0 speed with EQ = 15 and flat_gain = 101. Note: actual reach extension depends on various signal integrity factors. It is recommended to run signal intergrity simulations with all the components in the link to get any guidance.

Table 8-1. PCIe 4.0 Reach Extension Using the DS160PR1601

Setup	Pre Channel Loss	Post Channel Loss	Total Loss	Eye at BER 1E-12	SigTest Pass?
Baseline – no DUT	—	—	≅27 dB	29 ps, 48 mV	Pass
With DUT (DS160PR1601)	≅25 dB	≅18 dB	≅43 dB	30 ps, 55 mV	Pass

8.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The DS160PR1601 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of adequate numbers of 0.1 µF capacitors near device VCC pins, several 1.0 µF and 10.0 bulk capacitors on VCC power plane. The local decoupling (0.1 µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the DS160PR1601 ground pad. For more specific guidance, refer to *DS320PR1601RSC-EVM User's Guide*.

8.4 Layout

8.4.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most/all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

8.4.2 Layout Example

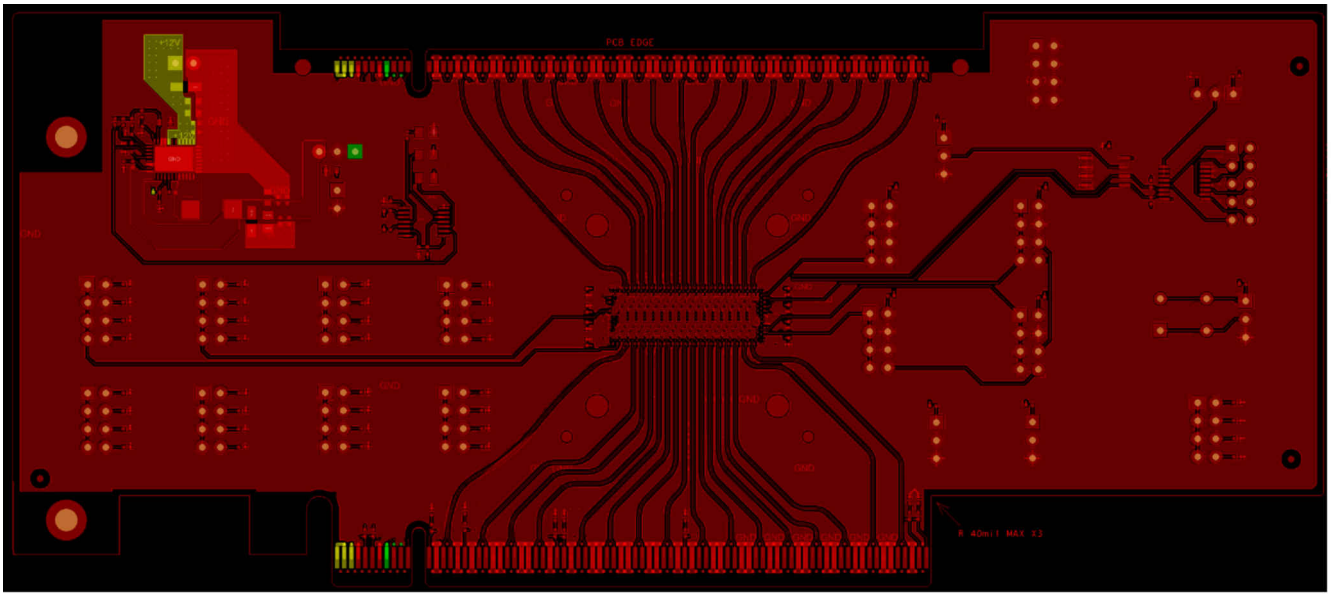


Figure 8-7. Top Layer View of TI PCIe Riser Card Using DS160PR1601 with CEM Connectors

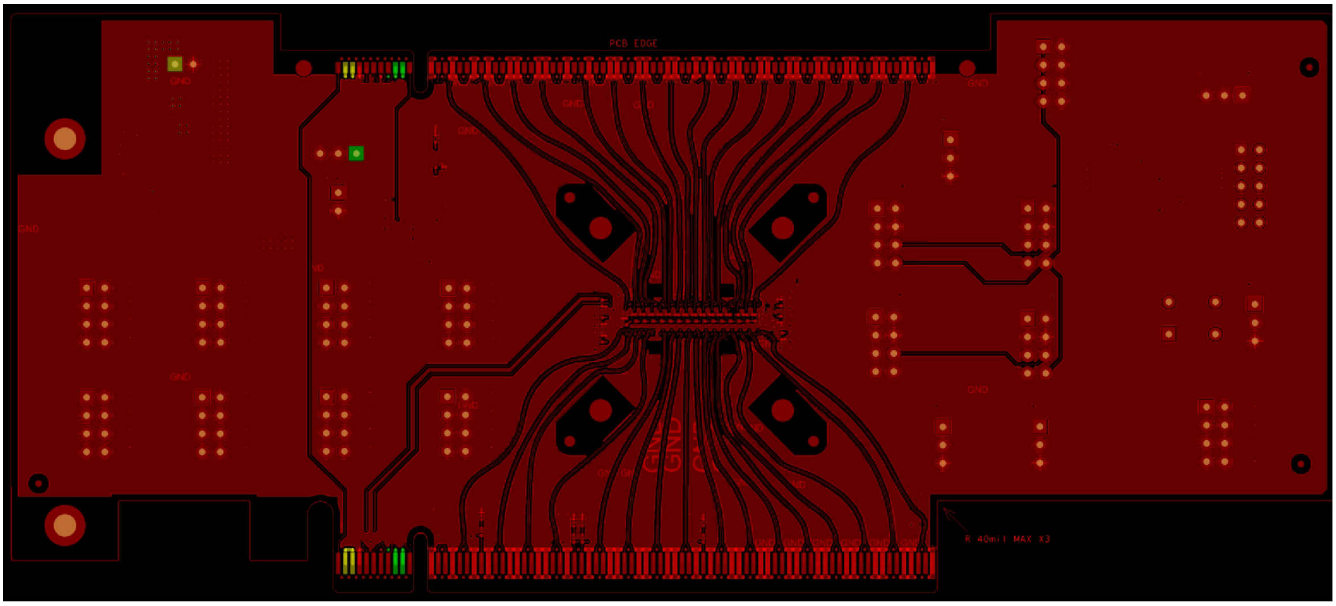


Figure 8-8. Bottom Layer View of TI PCIe Riser Card Using DS160PR1601 with CEM Connectors

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DS320PR1601RSC-EVM User's Guide*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS160PR1601ZDGR	Active	Production	NFBGA (ZDG) | 354	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	PR16X
DS160PR1601ZDGR.B	Active	Production	NFBGA (ZDG) | 354	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DS160PR1601ZDGT	Active	Production	NFBGA (ZDG) | 354	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	PR16X
DS160PR1601ZDGT.B	Active	Production	NFBGA (ZDG) | 354	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

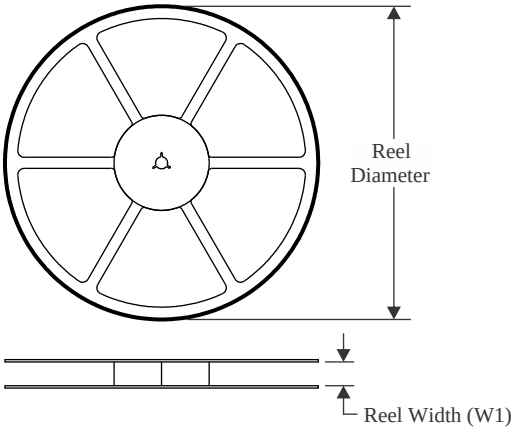
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

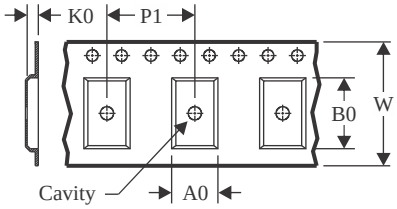
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

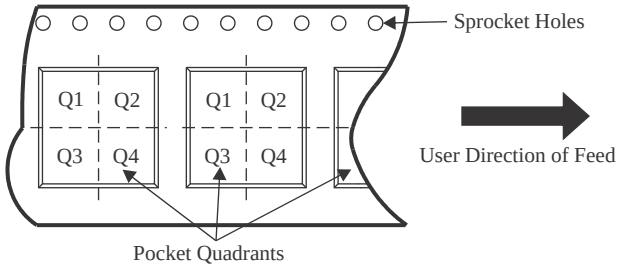


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

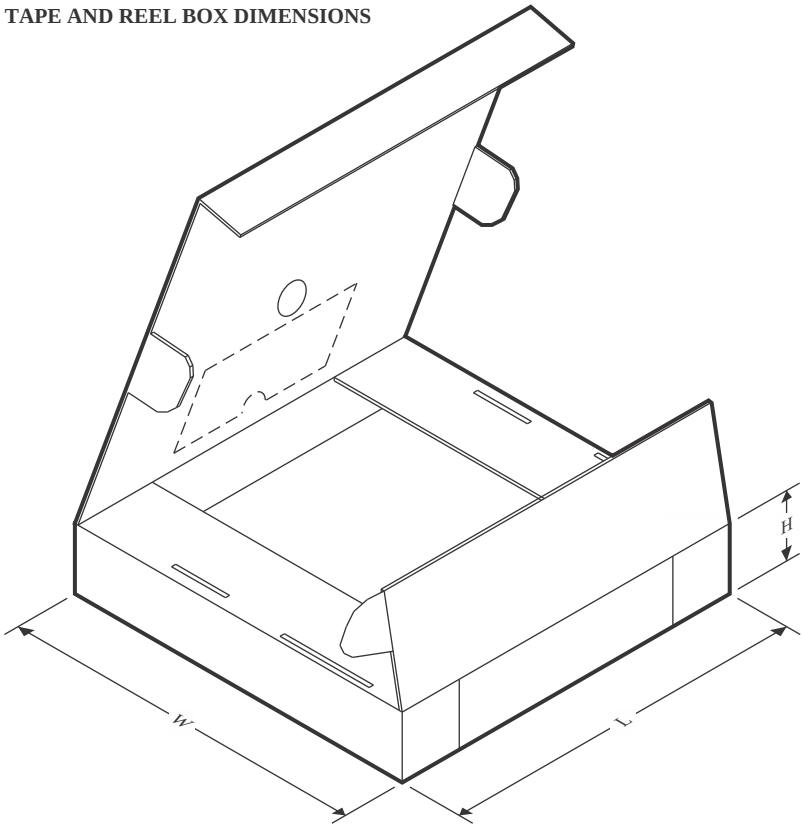
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS160PR1601ZDGR	NFBGA	ZDG	354	1000	330.0	44.4	9.5	23.4	2.0	16.0	44.0	Q1
DS160PR1601ZDGT	NFBGA	ZDG	354	250	330.0	44.4	9.5	23.4	2.0	16.0	44.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

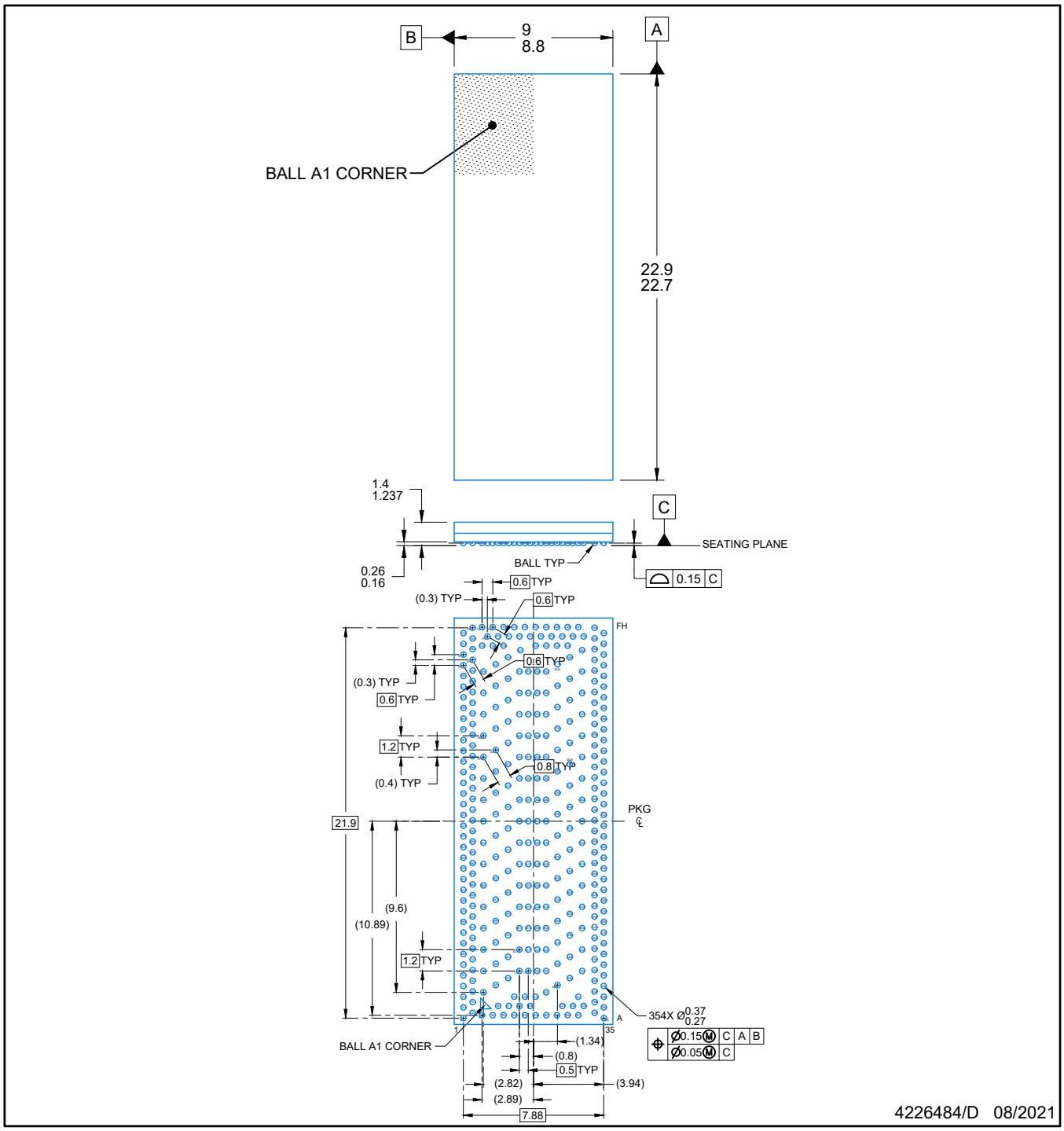
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS160PR1601ZDGR	NFBGA	ZDG	354	1000	336.6	336.6	53.2
DS160PR1601ZDGT	NFBGA	ZDG	354	250	336.6	336.6	53.2

PACKAGE OUTLINE

ZDG0354A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

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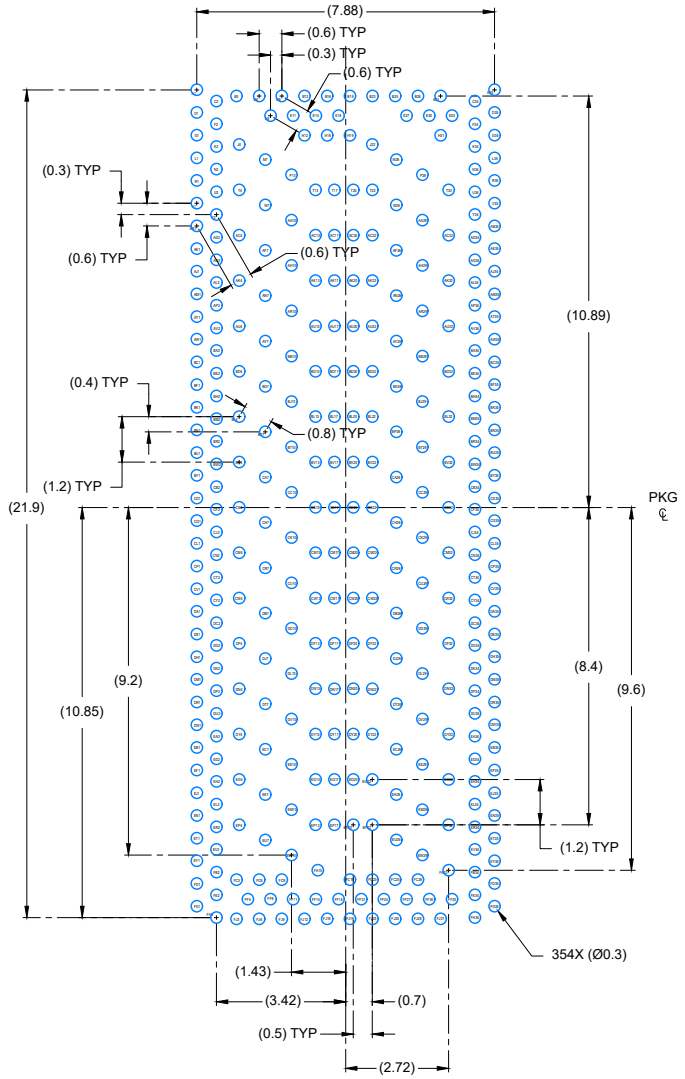
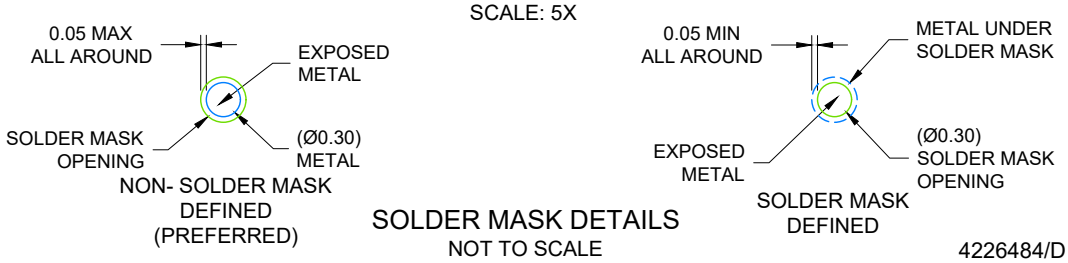
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 5X



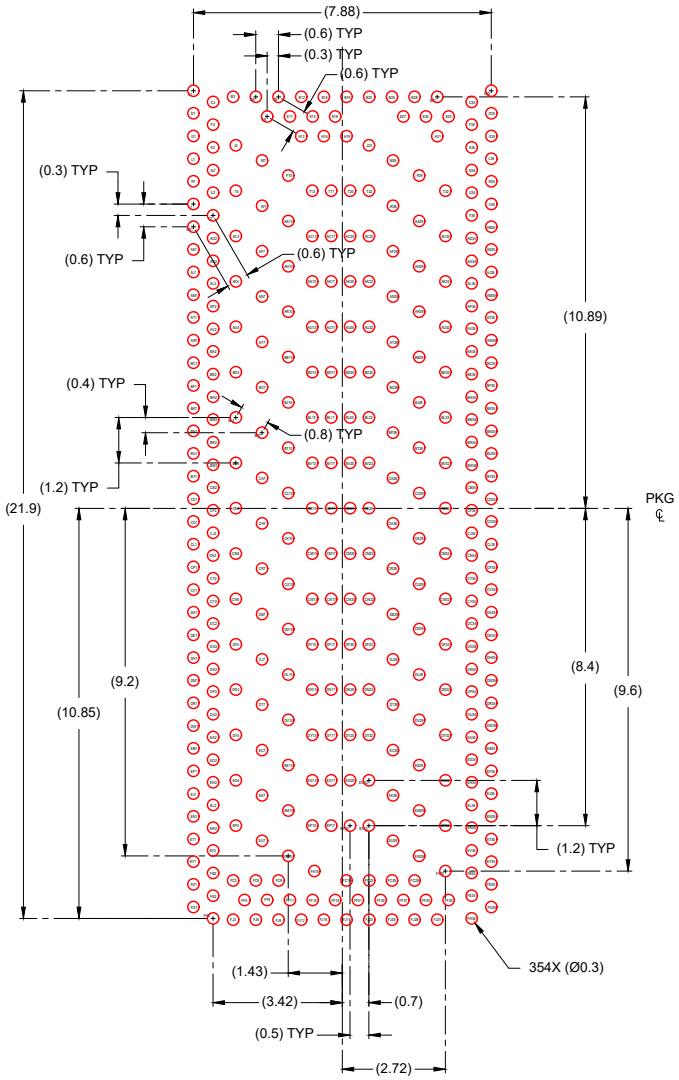
SOLDER MASK DETAILS

NOT TO SCALE

4226484/D 08/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL
SCALE: 5X

4226484/D 08/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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