DRV8952 Four-channel Half-Bridge Driver with Current Sense Outputs

1 Features

- Four-channel half-bridge driver
  - **Independent control** of each half-bridge
- **4.5V to 55V** operating supply voltage range
- Low $R_{DS(ON)}$: **50mΩ** for each FET (24 V, 25 °C)
- High current capacity:
  - DDW package: Up to **5A per output**
  - PWP package: Up to **4A per output**
- Can drive various types of loads -
  - Up to four solenoids or valves
  - One stepper motor
  - Two brushed-DC motors
  - One or two thermoelectric coolers (TEC)
  - One 3-phase brushless-DC motor
  - One 3-phase permanent magnet synchronous motor (PMSM)
- Integrated current sense and regulation
  - Current sensing across high-side MOSFETs
  - **IPROPI** outputs for each half-bridge (DDW)
  - **5 %** sense accuracy at maximum current
  - Optional external sense resistor
- Pin-to-pin compatible with:
  - DRV8955PWP: 48V, 4-ch half-bridge driver
  - DRV8962DDW: 65V, 4-ch half-bridge driver
- Separate logic supply voltage (**VCC**) (DDW)
- Programmable output rise/fall time (DDW)
- Programmable fault recovery method (DDW)
- Supports 1.8V, 3.3V, 5.0V logic inputs
- Low-current sleep mode (3µA)
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Factory Automation, Stepper Drives and Robotics
- Medical Imaging, Diagnostics and Equipment
- Stage Lighting
- PLCs
- TEC Drivers
- BLDC Motor Modules
- Brushed-DC and Stepper Motor drivers

3 Description

The DRV8952 is a wide-voltage, high-power, four-channel half-bridge driver for a wide variety of industrial applications. The device supports up to 55V supply voltage, and integrated MOSFETs with close to 50mΩ on-resistance allow up to 5A current on each output with the DDW package; and up to 4A current per output with the PWP package.

The device can be used for driving up to four solenoids or valves, one stepper motor, two brushed-DC motors, one BLDC or PMSM motor and up to two thermoelectric coolers (Peltier elements). The output stage of the device consists of N-channel power MOSFETs configured as four independent half-bridges, charge pump regulator, current sensing and regulation circuits, current sense outputs and protection circuitry.

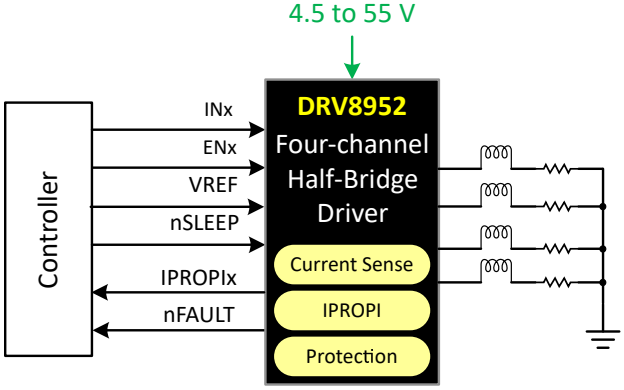
Integrated current sensing across the high-side MOSFETs allows the device to regulate the current when the load is connected from output to ground. A current regulation limit can be set with an adjustable external voltage reference (VREF). With the DDW package, the device provides four proportional current output pins, one for each half-bridge high-side FET. Optional external sense resistors can be connected from the PGND pins to the system ground.

A low-power sleep mode is provided to achieve ultra-low quiescent current. Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output over current (OCP), and device overtemperature (OTSD).

Device Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE (NOM)[(2)]
DRV8952DDWR	HTSSOP (44)	14mm x 8.1mm
DRV8952PWPR	HTSSOP (28)	9.7mm x 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



DRV8952 Simplified Schematic

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4 Pin Configuration and Functions

The DRV8952 is available in thermally-enhanced, 44-Pin HTSSOP (DDW) and 28-Pin HTSSOP (PWP) packages.

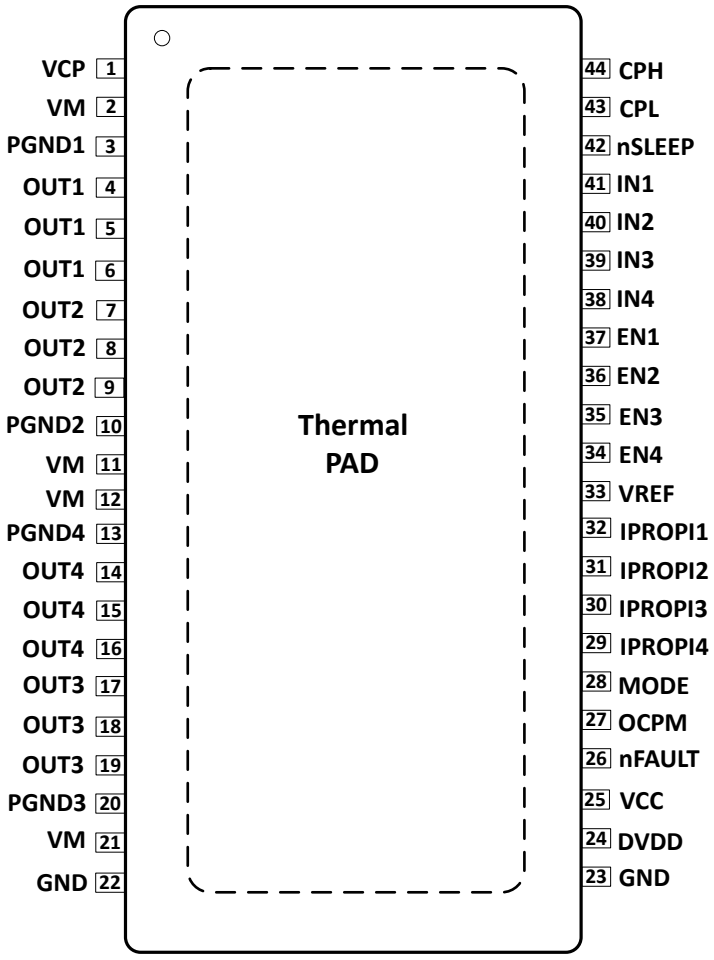


Figure 4-1. DDW Package, Top View

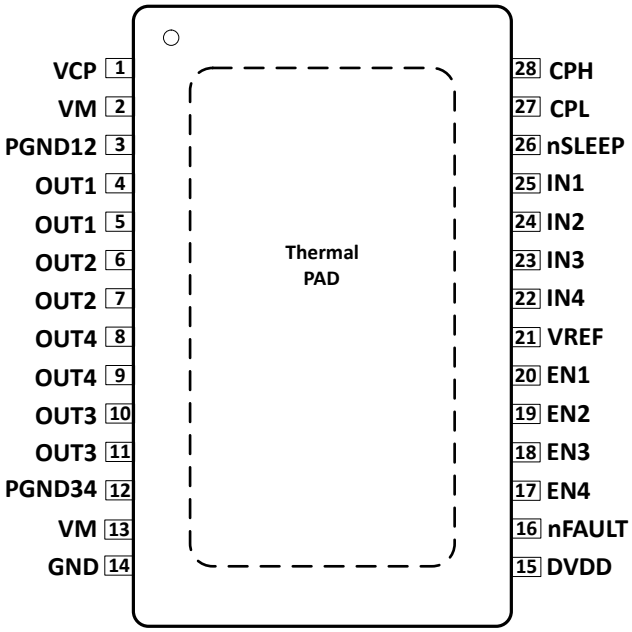


Figure 4-2. PWP Package (28-Pin HTSSOP), Top View

PIN			TYPE	DESCRIPTION
NAME	DDW	PWP		
VCP	1	1	Power	Charge pump output. Connect a X7R, 1-µF, 16-V ceramic capacitor from VCP to VM.
VM	2, 11, 12, 21	2, 13	Power	Power supply. Connect to motor supply voltage and bypass to PGND pins with 0.01-µF ceramic capacitors plus a bulk capacitor rated for VM.
IPROPI1	32	-	Output	Current sense output for half-bridge 1.
IPROPI2	31	-	Output	Current sense output for half-bridge 2.
IPROPI3	30	-	Output	Current sense output for half-bridge 3.
IPROPI4	29	-	Output	Current sense output for half-bridge 4.
EN1	37	20	Input	Enable input of half-bridge 1.
EN2	36	19	Input	Enable input of half-bridge 2.
EN3	35	18	Input	Enable input of half-bridge 3.
EN4	34	17	Input	Enable input of half-bridge 4.
IN1	41	25	Input	PWM input for half-bridge 1.
IN2	40	24	Input	PWM input for half-bridge 2.
IN3	39	23	Input	PWM input for half-bridge 3.
IN4	38	22	Input	PWM input for half-bridge 4.
CPH	44	28	Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM rated ceramic capacitor from CPH to CPL.
CPL	43	27		
PGND12	-	3	Power	Common power ground for half-bridges 1 and 2. Connect to system ground.
PGND34	-	12	Power	Common power ground for half-bridges 3 and 4. Connect to system ground.
PGND1	3	-	Power	Power ground for half-bridge 1. Connect to system ground.
PGND2	10	-	Power	Power ground for half-bridge 2. Connect to system ground.

PIN			TYPE	DESCRIPTION
NAME	DDW	PWP		
PGND3	20	-	Power	Power ground for half-bridge 3. Connect to system ground.
PGND4	13	-	Power	Power ground for half-bridge 4. Connect to system ground.
OUT1	4, 5, 6	4, 5	Output	Connect to load terminal.
OUT2	7, 8, 9	6, 7	Output	Connect to load terminal.
OUT3	17, 18, 19	10, 11	Output	Connect to load terminal.
OUT4	14, 15, 16	8, 9	Output	Connect to load terminal.
GND	22, 23	14	Power	Device ground. Connect to system ground.
DVDD	24	15	Power	Internal LDO output. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VREF	33	21	Input	Voltage reference input for setting current regulation threshold. DVDD can be used to provide VREF through a resistor divider.
VCC	25	-	Power	Supply voltage for internal logic blocks. When separate logic supply voltage is not available, tie the VCC pin to the DVDD pin.
nFAULT	26	16	Open Drain	Fault indication output. Pulled logic low with fault condition. Open drain output requires an external pullup resistor.
MODE	28	-	Input	This pin programs the output rise/fall time.
OCPM	27	-	Input	Determines the fault recovery method. Depending on the OCPM voltage, fault recovery can be either latch-off or auto-retry type.
nSLEEP	42	26	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. A narrow nSLEEP reset pulse clears latched faults.
PAD	-	-	-	Thermal pad. Connect to system ground.

5 Specifications

Over operating free-air temperature range (unless otherwise noted). ((1)) ((2))

5.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	60	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 5.75	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
External logic supply (VCC)	-0.3	5.75	V
Reference input pin voltage (VREF)	-0.3	5.75	V
IPROPI pin voltage (IPROPI)	-0.3	DVDD + 0.3	V
Control pin voltage	–0.3	5.75	V
PGNDx to GND voltage	-0.5	0.5	V
PGNDx to GND voltage, < 1 µs	-2.5	2.5	V
Open drain output current (nFAULT)	0	10	mA
Continuous OUTx pin voltage	–1	V_{VM} + 1	V
Transient 100 ns OUTx pin voltage	–3	V_{VM} + 3	V
Peak drive current	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2]	Corner pins	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	55	V
V_I	Logic level input voltage	0	5.5	V
V_{VCC}	VCC pin voltage	3.05	5.5	V
V_{REF}	Reference voltage (VREF)	0.05	3.3	V
f_{PWM}	Applied PWM signal	0	200	kHz
I_{DDW}	Current per output, DDW Package	0	5	A
I_{PWP}	Current per output, PWP Package	0	4	A
T_A	Operating ambient temperature	–40	125	°C

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_J	Operating junction temperature	–40	150	°C

5.4 Thermal Information

THERMAL METRIC		DDW	PWP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.5	24.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.8	13.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.9	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.8	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	0.9	°C/W

5.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No load, VCC = External 5V		4	7	mA
		nSLEEP = 1, No load, VCC = DVDD		6	9	
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		3	8	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.85	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.85	1.3	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 55 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.35	4.45		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 55 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, EN1, EN2, EN3, EN4, MODE, OCPM, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis (all pins except nSLEEP)			100		mV
V_{HYS_nSLEEP}	nSLEEP logic hysteresis			300		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = DVDD			50	µA
t_1	ENx high to OUTx high delay	INx = 1			2	µs
t_2	ENx low to OUTx low delay	INx = 1			2	µs
t_3	ENx high to OUTx low delay	INx = 0			2	µs

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_4	ENx low to OUTx high delay	INx = 0			2	µs
t_5	INx high to OUTx high delay			600		ns
t_6	INx low to OUTx low delay			600		ns
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.35	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -5 A		54	63	mΩ
		T_J = 125 °C, I_O = -5 A		80	94	mΩ
		T_J = 150 °C, I_O = -5 A		90	105	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 5 A		58	66	mΩ
		T_J = 125 °C, I_O = 5 A		85	98	mΩ
		T_J = 150 °C, I_O = 5 A		94	107	mΩ
t_{RF}	Output rise/fall time	I_O = 5 A, MODE = 0 for DDW package, or for PWP package, between 10% and 90%		140		ns
		I_O = 5 A, MODE = 1 for DDW package, between 10% and 90%		70		ns
t_D	Output dead time	VM = 24V, I_O = 5 A		300		ns
CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A_{IPROPI}	Current mirror gain			212		µA/A
K_V	Transimpedance Gain	VREF = 3.3 V, PWP Package	0.625	0.66	0.695	V/A
A_{ERR}	Current mirror scaling error	10% to 20% rated current	-7		9	%
		20% to 40% rated current	-4		6	
		40% to 100% rated current	-3.5		5	
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			20	nA
t_{OFF}	PWM off-time			16		µs
t_{DEG}	Current regulation deglitch time			0.5		µs
t_{BLK}	Current Regulation Blanking time			1.5		µs
t_{DELAY}	Current sense delay time			2		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling	4.1	4.23	4.35	V
		VM rising	4.2	4.35	4.47	
VCC_{UVLO}	VCC UVLO lockout	VCC falling	2.7	2.8	2.9	V
		VCC rising	2.75	2.92	3.05	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		110		mV
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	7.6			A
t_{OCP}	Overcurrent detection delay			2.2		µs
t_{RETRY}	Overcurrent retry time			4.1		ms
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

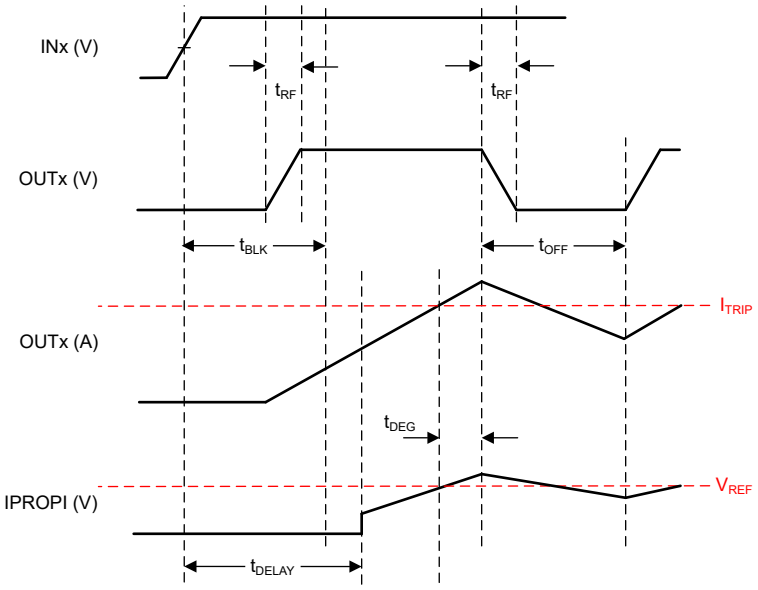


Figure 5-1. IPROPI Timing Diagram

5.6 Typical Characteristics

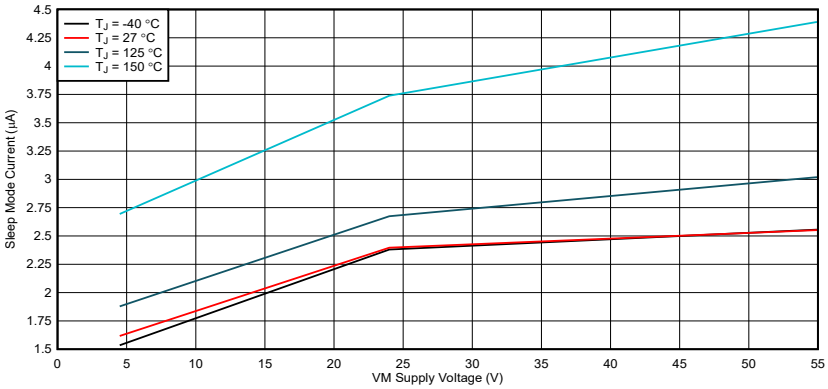


Figure 5-2. Sleep mode supply current

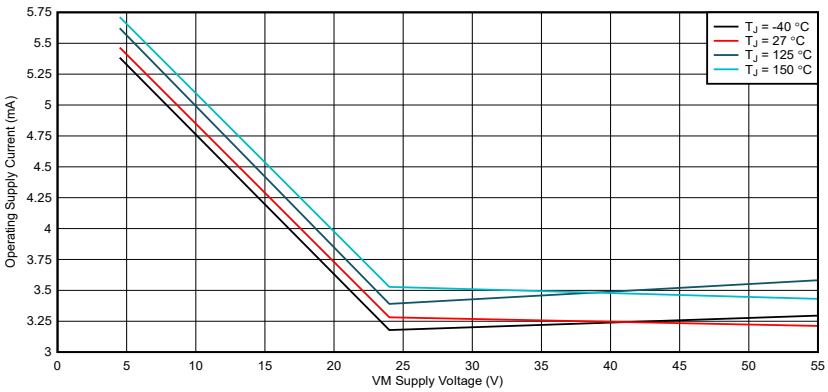


Figure 5-3. Operating supply current, VCC = External 5 V

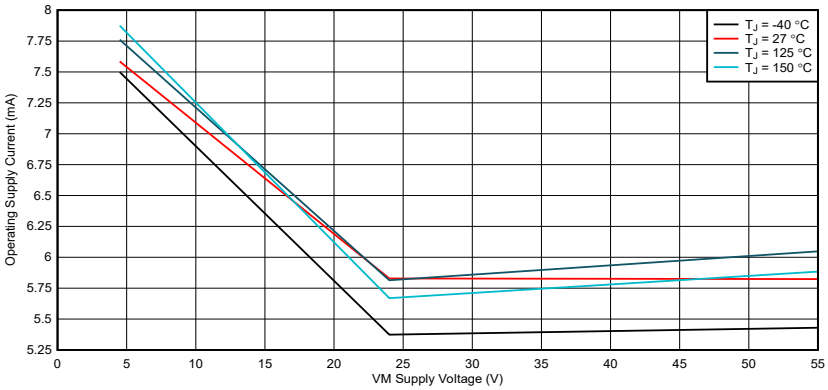


Figure 5-4. Operating supply current, VCC = DVDD

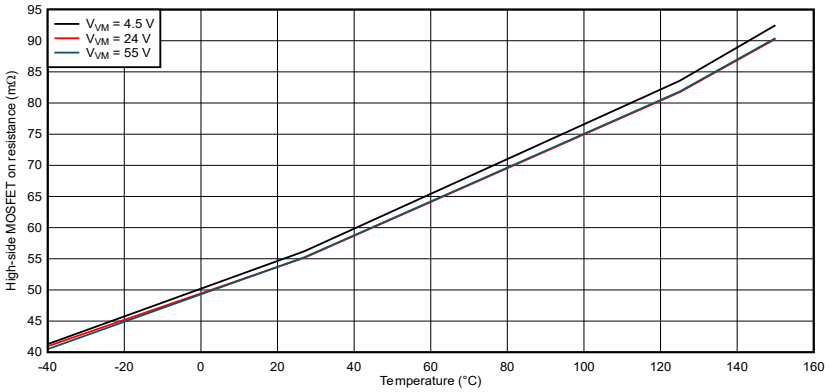


Figure 5-5. High-side FET on resistance

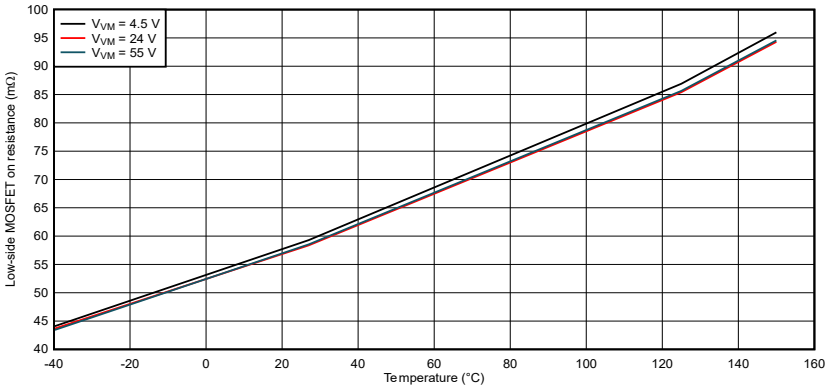


Figure 5-6. Low-side FET on resistance

6 Detailed Description

6.1 Overview

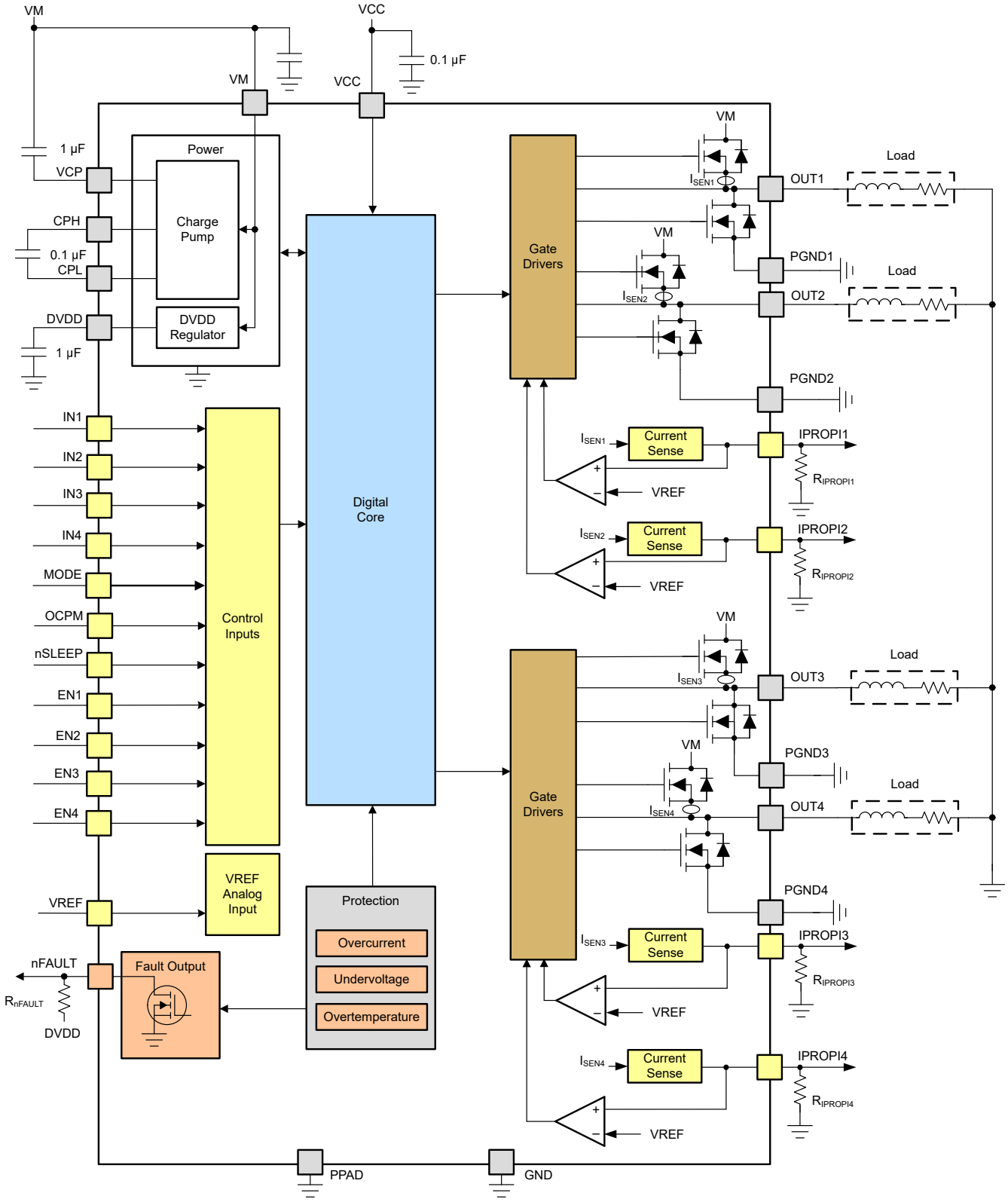
The DRV8952 is a four-channel half-bridge driver that operates from 4.5 V to 55 V and supports a wide range of load currents for various types of loads. The device integrates four half-bridge output power stages. The device integrates a charge pump regulator to support efficient high-side N-channel MOSFETs and 100% duty cycle operation. The DRV8952 can operate from a single power supply input (VM). Alternatively, the VCC pin can be connected to a second power supply to provide power to the internal logic blocks when using the DDW package. The nSLEEP pin provides an ultra-low power mode to minimize current draw during system inactivity.

The device is available in two packages - a 44-pin HTSSOP (DDW) package; and another 28-pin HTSSOP (PWP) package. The DDW package provides up to 5-A current per output, whereas the PWP package can deliver up to 4-A current per output. The DRV8952 DDW package is pin-to-pin compatible with the DRV8962, and the DRV8952 PWP package is pin-to-pin compatible with the DRV8955. The actual current that can be delivered depends on the ambient temperature, supply voltage, and PCB thermal design.

The DRV8952 DDW package provides current sense outputs. The IPROPI pins source a small current that is proportional to the current in the high-side MOSFETs. The current from the IPROPI pins can be converted to a proportional voltage using an external resistor (R_{IPROPI}). The integrated current sensing allows the DRV8952 to limit the output current with a fixed off-time PWM chopping scheme and provide load information to the external controller to detect changes in load. The sense accuracy of the IPROPI output is -3.5%/+5% for 40% to 100% of rated current. External power sense resistors can also be connected if higher accuracy sensing is required. The current regulation level can be configured during operation through the VREF pin to limit the load current according to the system demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), over current protection (OCP), and over temperature shutdown (OTSD). Fault conditions are indicated on the nFAULT pin.

6.2 Functional Block Diagram



6.3 Feature Description

The following table shows the recommended values of the external components for the DRV8952.

Table 6-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND1	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM2}	VM	PGND3	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM3}	VM	PGND1	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 1-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.1-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 1-µF, 6.3-V or 10-V rated ceramic capacitor
C_{VCC}	VCC	GND	X7R, 0.1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{nFAULT}	DVDD or VCC	nFAULT	10-kΩ resistor
R_{REF1}	VREF	DVDD	Resistors to set current regulation threshold.
R_{REF2}	VREF	GND	
$R_{IPROPIx}$	IPROPIx	GND	For details, see Section 6.5.1

6.4 Independent Half-bridge Operation

- The DRV8952 can drive four half-bridge loads simultaneously.
- For the DDW package, the MODE pin configures the typical output rise and fall times to 70 ns or 140 ns.
- Rise and fall times are 140 ns for the PWP package.
- The ENx pins enable or disable (Hi-Z) the outputs.
- The INx pins control the state (high or low) of the outputs
  - The INx pins can accept static or pulse-width modulated (PWM) signals.
  - The INx and ENx inputs can be powered before VM is applied.
- The truth table does not take into account the internal current regulation feature.
- The device automatically handles the dead time generation when switching between the high-side and low-side MOSFET of a half-bridge.

Table 6-2. Independent Half-Bridge Operation Truth Table

nSLEEP	INx	ENx	OUTx	DESCRIPTION
0	X	X	Hi-Z	Sleep mode, all half-bridges disabled (Hi-Z)
1	X	0	Hi-Z	Individual outputs disabled (Hi-Z)
1	0	1	L	OUTx Low-side ON
1	1	1	H	OUTx High-side ON

The inputs can also be used for PWM control of, for example, the speed of a DC motor. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to the ENx pin; to use slow decay, the PWM signal is applied to the INx pin. The following table is an example of driving a DC motor using OUT1 and OUT2 as an H-bridge:

Table 6-3. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
1	1	PWM	1	Forward PWM, slow decay
PWM	1	1	1	Reverse PWM, slow decay
1	PWM	0	PWM	Forward PWM, fast decay
0	PWM	1	PWM	Reverse PWM, fast decay

6.5 Current Sensing and Regulation

The DRV8952 integrates current sensing across the high-side MOSFETs, current regulation, and current sense feedback. These features allow the device to sense the load current when the load is connected between output nodes and ground, without connecting an external sense resistor or sense circuitry; reducing system size, cost, and complexity. The current sense proportional outputs (IPROPI) of the DDW package allow the device to give detailed feedback to the controller about the load current.

6.5.1 Current Sensing and Feedback

The DRV8952 in DDW package supports four IPROPI outputs, one for each half-bridge. The IPROPI outputs represent the current of each high-side MOSFET, as shown below -

$$I_{PROPI} = I_{HS} \times A_{IPROPI} \quad (1)$$

Where I_{HS} is the current flowing through the high-side MOSFET and A_{IPROPI} is the current mirror gain.

Each IPROPI pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin. This allows the current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. The device implements an internal clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events. The IPROPI voltage should be less than the maximum recommended value of VREF, which is 3.3V.

The corresponding IPROPI voltage to the output current can be calculated as shown below -

$$V_{IPROPI}\ (V) = I_{PROPI}\ (A) \times R_{IPROPI}\ (\Omega) \quad (2)$$

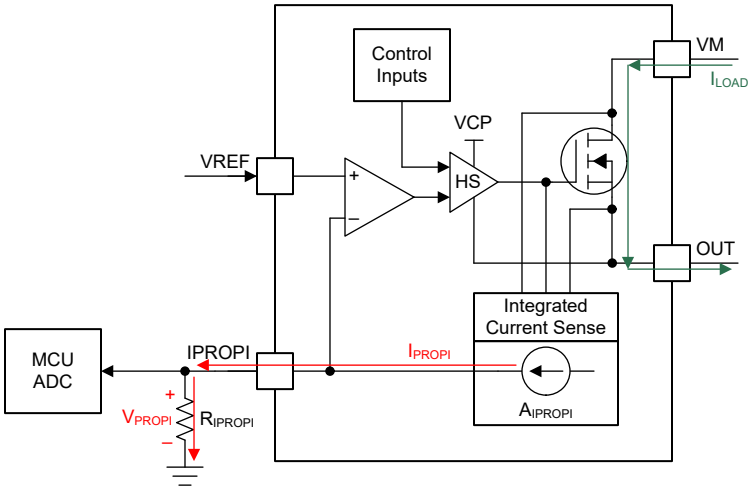


Figure 6-1. Integrated Current Sensing

The A_{ERR} parameter in the Electrical Characteristics table is the error associated with the A_{IPROPI} gain. It indicates the combined effect of offset error added to the I_{OUT} current and gain error.

6.5.2 Current Sensing with External Resistor

The IPROPI output accuracy is -3.5% to +5% for 40% to 100% of rated current. If more accurate current sensing is desired, or for the PWP package, external sense resistors can also be used between the PGND pins and the system ground to sense the load currents, as shown below.

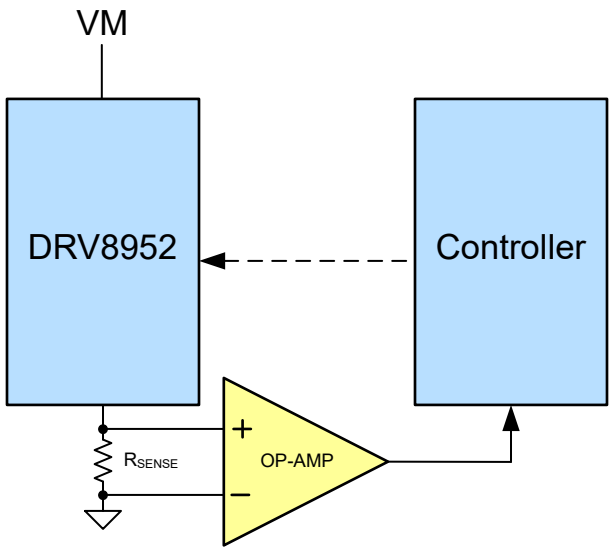


Figure 6-2. Current Sensing with External Resistor

The voltage drop across the external sense resistor should not exceed 300 mV.

Place the sense resistors as close as possible to the corresponding IC pins. Use a symmetrical sense resistor layout to ensure good matching. Low-inductance sense resistors should be used to prevent voltage spikes and ringing. For optimal performance, the sense resistor should be a surface-mount resistor rated for high enough power.

6.5.3 Current Regulation

For the DRV8952 in DDW package, the current chopping threshold (I_{TRIP}) is set through a combination of the VREF voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

$$I_{TRIP}\ (A) \times A_{IPROPI}\ (\mu A/A) = V_{VREF}\ (V) / R_{IPROPI}\ (\Omega) \quad (3)$$

For example, to set I_{TRIP} at 5 A with V_{VREF} at 3.3 V, R_{IPROPI} has to be -

$R_{IPROPI} = V_{VREF} / (I_{TRIP} \times A_{IPROPI}) = 3.3 / (5 \times 212 \times 10^{-6}) = 3.09\ k\Omega$

The internal current regulation can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND (if current feedback is not required). If current feedback is required and current regulation is not required, set V_{VREF} and R_{IPROPI} such that V_{IPROPI} never reaches the V_{VREF} threshold.

For the DRV8952 in PWP package, the current chopping threshold (I_{TRIP}) is set by the VREF voltage (V_{VREF}) as shown below -

$$I_{TRIP}\ (A) = V_{VREF}\ (V) / K_V\ (V/A) \quad (4)$$

The DRV8952 can simultaneously drive up to four resistive or inductive loads. When an output load is connected to ground, the load current can be regulated to the I_{TRIP} level. The PWM off-time (t_{OFF}) is fixed at 16 µs. The fixed off-time mode allows for a simple current chopping scheme without involvement from the external controller. Fixed off-time mode will support 100% duty cycle current regulation.

Another way of controlling the load current is the cycle-by-cycle control mode, where PWM pulse width of the INx input pins have to be controlled. This allows for additional control of the current chopping scheme by the external controller.

Few scenarios of driving high-side and low-side loads are described below -

- **Resistive loads connected to ground:**

The regulated current will not exceed I_{TRIP}. If I_{TRIP} is higher than the (VM / R_{LOAD}), the load current is regulated at VM / R_{LOAD} level while INx = 1 (shown in Figure 6-3).

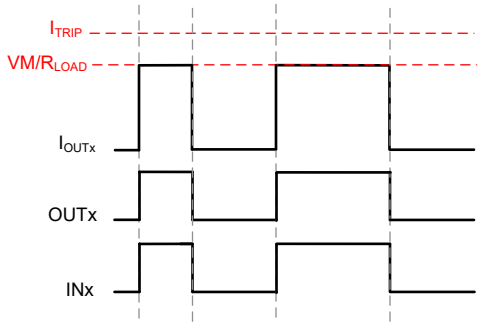


Figure 6-3. Resistive Load Connected to ground, Cycle-by-cycle control

- **Inductive loads connected to ground:**

It should be ensured that the current decays enough every cycle to prevent runaway and triggering overcurrent protection.

- For the scenario shown in Figure 6-4, with INx = 1, the low-side MOSFET is turned on for t_{OFF} duration after I_{OUT} exceeds I_{TRIP}. After t_{OFF}, the high side MOSFET is again turned on till I_{OUT} exceeds I_{TRIP} again.

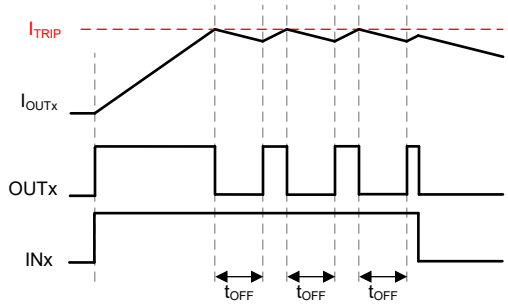


Figure 6-4. Inductive Load Connected to ground, fixed off-time current chopping

If, after the t_{OFF} time has elapsed the current is still higher than the I_{TRIP} level, the device enforces another t_{OFF} time period of the same duration. The OFF time extension will continue till sensed current is less than I_{TRIP} at the end of t_{OFF} time.

- Loads can also be controlled using the cycle-by-cycle method. When INx = 1, the current through the load builds up; and when INx = 0, the current through the load decays. By properly choosing the duty cycle of the INx pulse, current can be regulated to a target value. Various such scenarios are shown in Figure 6-5 and Figure 6-6.

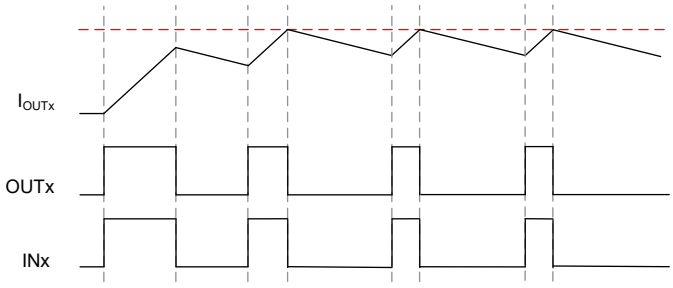


Figure 6-5. Inductive Load Connected to ground, Cycle-by-cycle control

The next scenario requires INx pin duty cycle adjustment (T has to be less than T_{OFF}) to ensure that the current does not run away.

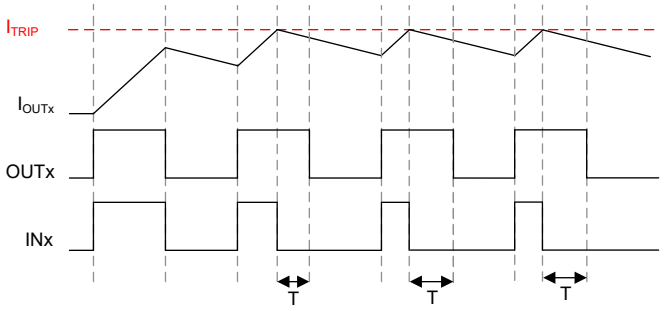


Figure 6-6. Inductive Load Connected to ground, Cycle-by-cycle control

- **Loads connected to VM:**

Such loads can be controlled by controlling the INx pin pulse width: INx = 0 builds up the current, and INx = 1 decays the current, as shown in Figure 6-7 and Figure 6-8.

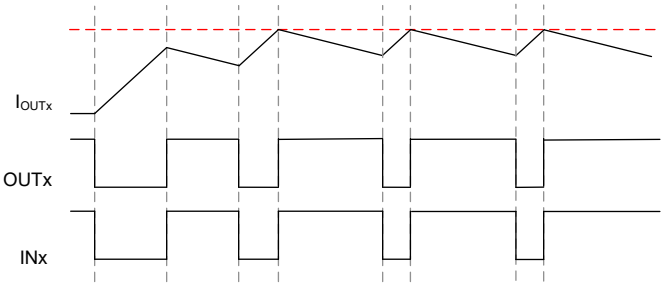


Figure 6-7. Inductive Load Connected to VM, Cycle-by-cycle control

This scenario requires INx pin duty cycle adjustment to ensure that the current does not run away.

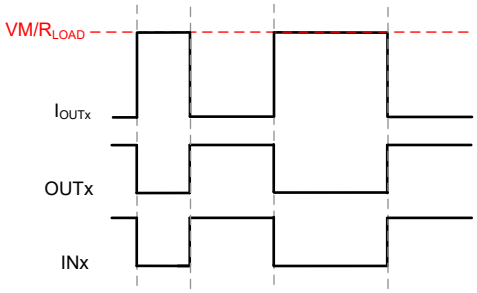


Figure 6-8. Resistive Load Connected to ground, Cycle-by-cycle control

6.6 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

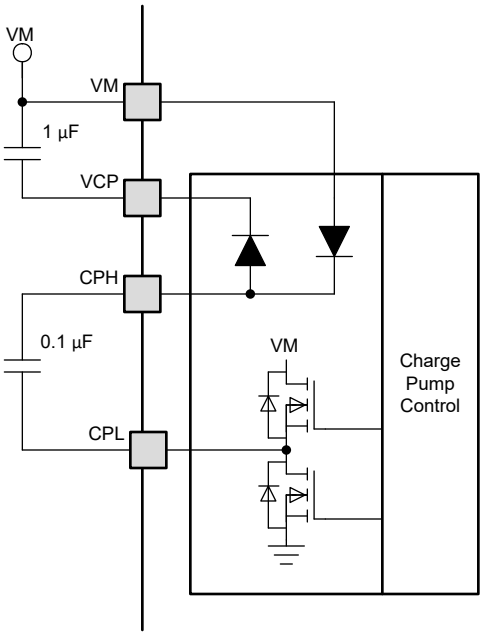


Figure 6-9. Charge Pump Block Diagram

6.7 Linear Voltage Regulator

A linear voltage regulator is integrated in the device. When the VCC pin is connected to DVDD, the DVDD regulator provides power to the low-side gate driver and all the internal circuits. For proper operation, bypass the DVDD pin to GND using a 1 µF ceramic capacitor. The DVDD output is nominally 5-V.

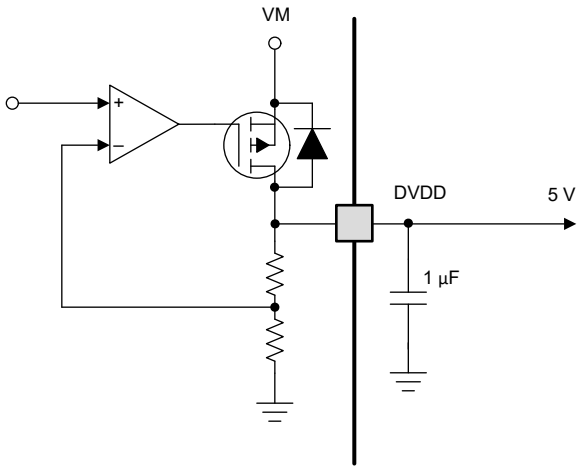


Figure 6-10. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

6.8 VCC Voltage Supply

For the DRV8952 in DDW package, an external voltage can be applied to the VCC pin to power the internal logic circuitry. The voltage on the VCC pin should be between 3.05 V and 5.5 V and should be well regulated. When an external supply is not available, VCC must be connected to the DVDD pin of the device.

When powered by the VCC, the internal logic blocks do not consume power from the VM supply rail - thereby reducing the power loss in the DRV8952. This is beneficial in high voltage applications, and when ambient temperature is high. Bypass the VCC pin to ground using a 0.1 µF ceramic capacitor.

6.9 Logic Level Pin Diagram

The pin diagram below shows the input structure for INx, ENx, MODE, OCPM and nSLEEP pins.

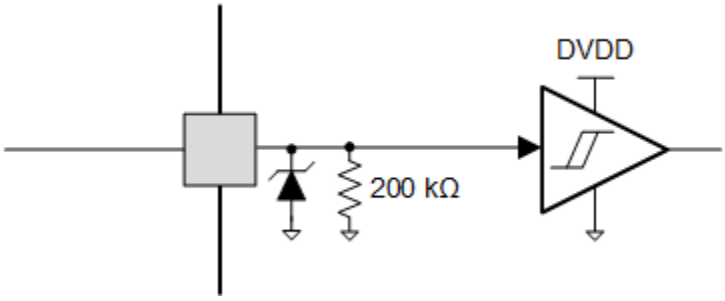


Figure 6-11. Logic-Level Input Pin Diagram

6.10 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

6.10.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO threshold voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump is disabled

Normal operation resumes (driver operation and nFAULT released) when the VM voltage recovers above the UVLO rising threshold voltage.

If the VM voltage falls below the internal digital reset voltage (3.9 V maximum), then the internal logic circuits are disabled and the pull-down on nFAULT is also disabled. So, when VM drops below about 3.9 V, nFAULT is pulled high again.

6.10.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump remains active

Normal operation resumes (driver operation and nFAULT released) when the VCP undervoltage condition is removed.

6.10.3 Logic Supply Power on Reset (POR)

If at any time the voltage on the VCC pin falls below the VCC_{UVLO} threshold:

- All the outputs are disabled (High-Z)

- Charge pump is disabled

VCC UVLO is not reported on the nFAULT pin. Normal motor-driver operation resumes when the VCC undervoltage condition is removed.

6.10.4 Overcurrent Protection (OCP)

Analog current-limit circuit on each MOSFET limits the current through that MOSFET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, an overcurrent fault is detected.

- Only the half-bridge experiencing the overcurrent will be disabled
- nFAULT is driven low
- Charge pump remains active

Overcurrent conditions on both high and low side MOSFETs; meaning a short to ground or short to supply will result in an overcurrent fault detection.

Once the overcurrent condition is removed, the recovery mechanism depends on the OCPM pin setting for the DDW package. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically (driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

The PWP package will only support latch-off type recovery - normal operation will resume after applying an nSLEEP reset pulse or a power cycling.

6.10.5 Thermal Shutdown (OTSD)

Thermal shutdown is detected if the die temperature exceeds the thermal shutdown limit (T_{OTSD}). When thermal shutdown is detected -

- All MOSFETs in the Half-bridges are disabled
- nFAULT is driven low
- Charge pump is disabled

Once the thermal shutdown condition is removed, the recovery mechanism depends on the OCPM pin setting for the DDW package. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

For the PWP package, normal operation after thermal shutdown fault resumes automatically after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

6.10.6 nFAULT Output

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

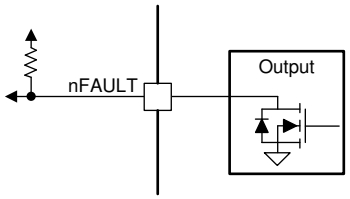


Figure 6-12. nFAULT Pin

6.10.7 Fault Condition Summary

Table 6-4. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	nFAULT	Disabled	Disabled	Reset	VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	nFAULT	Disabled	Operating	Operating	VCP > V_{CPUV}
Logic Supply POR	VCC < VCC_{UVLO}	-	Disabled	Disabled	Reset	VCC > VCC_{UVLO}
Overcurrent (OCP)	I_{OUT} > I_{OCP} , OCPM = 0 (DDW Package)	nFAULT	Disabled	Operating	Operating	Latched: nSLEEP reset pulse
	I_{OUT} > I_{OCP} , OCPM = 1 (DDW Package)	nFAULT	Disabled	Operating	Operating	Automatic retry: t_{RETRY}
	I_{OUT} > I_{OCP} , PWP Package	nFAULT	Disabled	Operating	Operating	Latched: nSLEEP reset pulse
Thermal Shutdown (OTSD)	T_J > T_{TSD}, OCPM = 0 (DDW Package)	nFAULT	Disabled	Disabled	Operating	Latched: nSLEEP reset pulse
	T_J > T_{TSD}, OCPM = 1 (DDW Package)	nFAULT	Disabled	Disabled	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}
	T_J > T_{TSD}, PWP Package	nFAULT	Disabled	Disabled	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

6.11 Device Functional Modes

6.11.1 Sleep Mode (nSLEEP = 0)

When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs, the DVDD regulator, SPI and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

6.11.2 Operating Mode

This mode is enabled when -

- nSLEEP is high
- VM > UVLO

The t_{WAKE} time must elapse before the device is ready for inputs.

6.11.3 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20 µs and smaller than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram below. This reset pulse does not affect the status of the charge pump or other functional blocks.

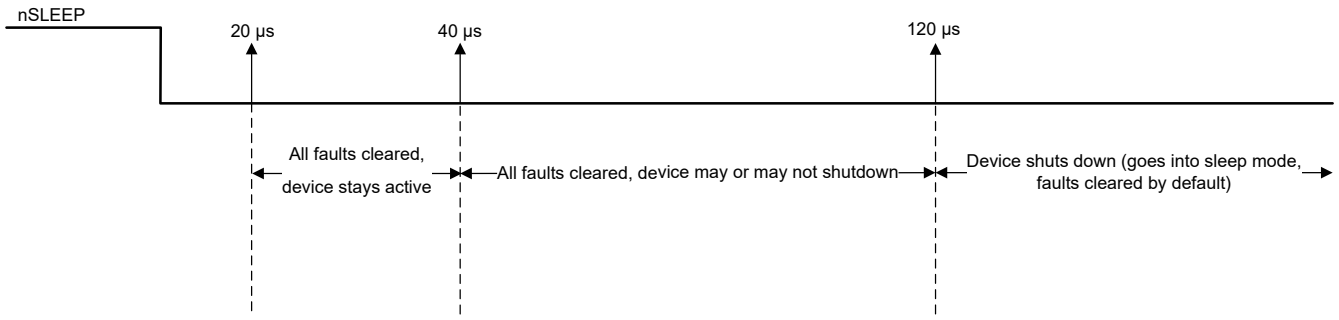


Figure 6-13. nSLEEP Reset Pulse

6.11.4 Functional Modes Summary

lists a summary of the functional modes.

Table 6-5. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 55 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled
Operating	4.5 V < VM < 55 V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The DRV8952 can be used to drive the following types of loads -

- Up to four solenoid loads
- One stepper motor
- Two brushed-DC motors
- One 3-phase sinewave Brushless-DC motor
- One 3-phase Permanent magnet synchronous motor (PMSM)
- One or two thermoelectric coolers (TEC)

7.1.1 Driving Solenoid Loads

The DRV8952 can drive four solenoid loads at the same time. For loads connected to ground, the IPROPI pins output the load current information (for DDW package); and the load current can be regulated to an I_{TRIP} level determined by the voltage on the VREF pin.

The DRV8952 supports independent IN and EN pins for each of the four half-bridges. All the four half-bridges also have separate PGND pins.

7.1.1.1 Solenoid Driver Typical Application

Figure 7-1 shows a schematic of the DRV8952 driving four loads connected to ground.

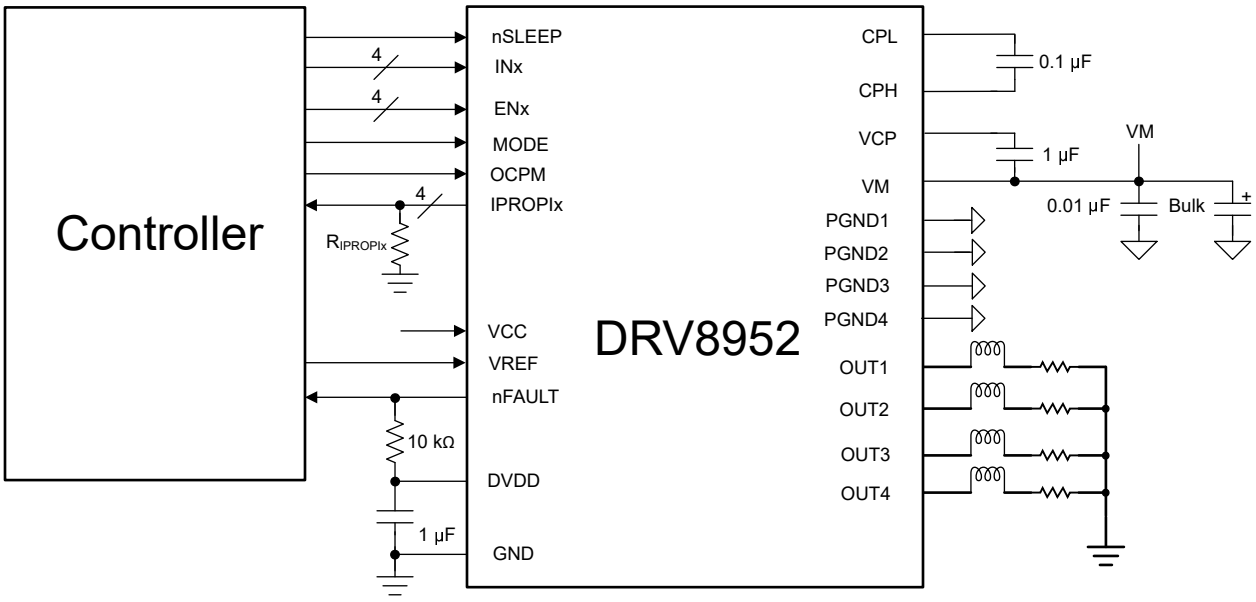


Figure 7-1. Driving Solenoids with DRV8952

7.1.1.2 Thermal Calculations

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation for the device is composed of three main components. These are the power MOSFET $R_{DS(ON)}$ (conduction) losses, the power MOSFET switching losses and the quiescent supply current dissipation. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

7.1.1.2.1 Power Loss Calculations

The total power dissipation in each half-bridge can be calculated as -

$$P_{HB} = P_{HS} + P_{LS} = [R_{DS(ON)} \times I_L{}^2] + [((2 \times V_D \times t_D) + (VM \times t_{RF})) \times I_L \times f_{PWM}]$$

Where,

- $R_{DS(ON)}$ = ON resistance of each FET
  - For DRV8952, it is typically 56 mΩ average at 25 °C
- f_{PWM} = PWM switching frequency
- VM = Supply voltage to the driver
- I_L = Load current
- D = PWM duty cycle (between 0 and 1)
- t_{RF} = Output voltage rise/ fall time
  - For DRV8952, the rise/fall time is either 70 ns or 140 ns for DDW package; and 140 ns for PWP package.
- V_D = FET body diode forward bias voltage
  - For DRV8952, it is 1 V
- t_D = dead time
  - For DRV8952, it is 300 ns

So, total power dissipation in the DRV8952 is -

$$P_{TOT} = n \times P_{HB} + P_Q$$

Where n is the number of half-bridges switching at the same time, and P_Q is the quiescent power loss.

For this example, let us assume -

- All four half-bridges are switching
- VM = 24 V
- I_L = 3 A
- Ambient temperature (T_A) = 25 °C
- t_{RF} = 140 ns
- Input PWM frequency = 20 kHz

When the VCC pin is connected to an external power supply, the quiescent current is 4 mA, and therefore P_Q will be (24 V x 4 mA) = 96 mW.

$$P_{HB} = [56\ m\Omega \times 3^2] + [((2 \times 1\ V \times 300\ ns) + (24\ V \times 140\ ns)) \times 3\ A \times 20\ KHz] = 0.742\ W$$

$$P_{TOT} = (4 \times 0.742) + 0.096 = 3.062\ W$$

7.1.1.2.2 Junction Temperature Estimation

The estimated junction temperature will be: $T_J = T_A + (P_{TOT} \times \theta_{JA})$

The junction-to-ambient thermal resistance θ_{JA} is 22.5 °C/W for the DDW package and 24.5 °C/W for the PWP package on a JEDEC standard PCB.

Therfore, the first estimate of the junction temperature for the DDW package is -

$$T_J = T_A + (P_{TOT} \times \theta_{JA}) = 25 + (3.062 \times 22.5) = 93.9°C$$

The first estimate of the junction temperature for the PWP package is -

$$T_J = T_A + (P_{TOT} \times \theta_{JA}) = 25 + (3.062 \times 24.5) = 100\ °C$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in the Typical Operating Characteristics section.

7.1.1.3 Application Performance Plots

Traces from top to bottom: OUT1, OUT2, OUT3, OUT4, IPROPI1

Figure 7-2. Driving four loads simultaneously

Traces from top to bottom: OUT1, IOUT1, IN1, IPROPI1

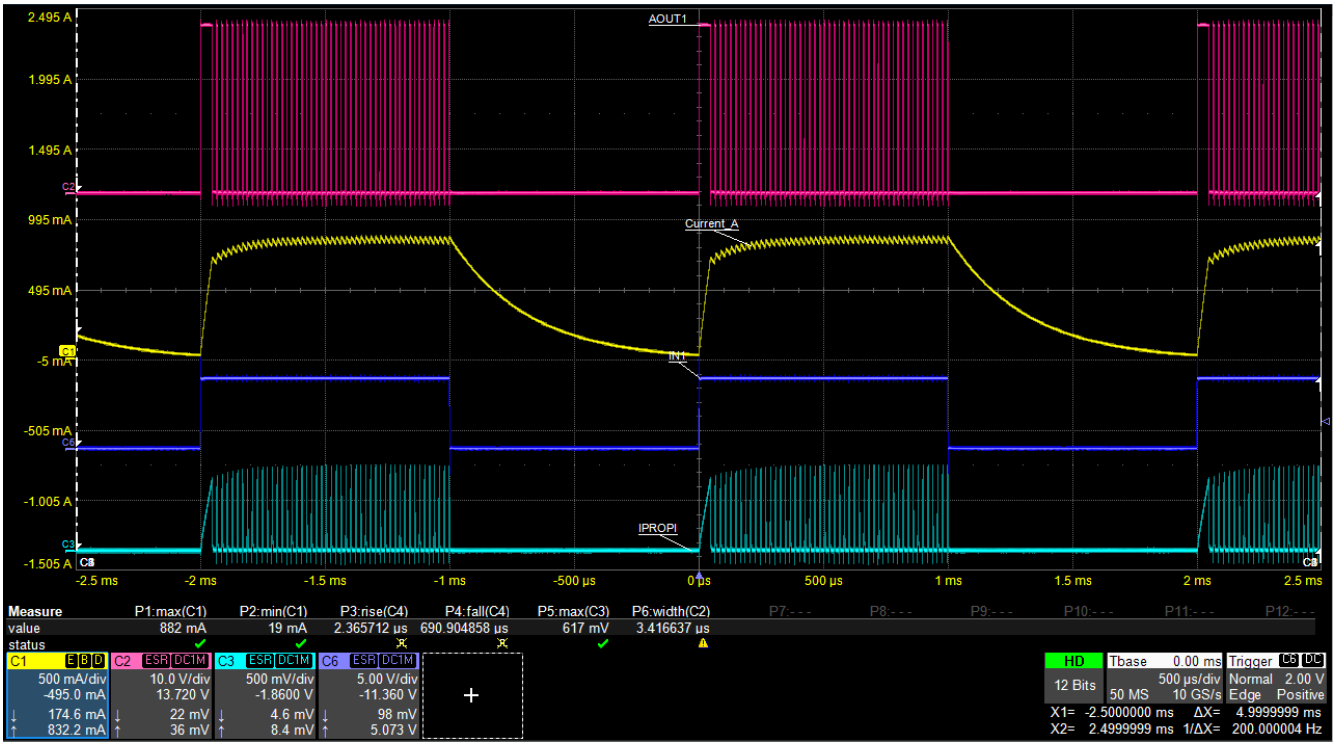


Figure 7-3. Current regulation with IPROPI Output

7.1.2 Driving Stepper Motors

The DRV8952 can drive one stepper motor using the PWM input interface.

7.1.2.1 Stepper Driver Typical Application

The following schematic shows the DRV8952 driving a stepper motor.

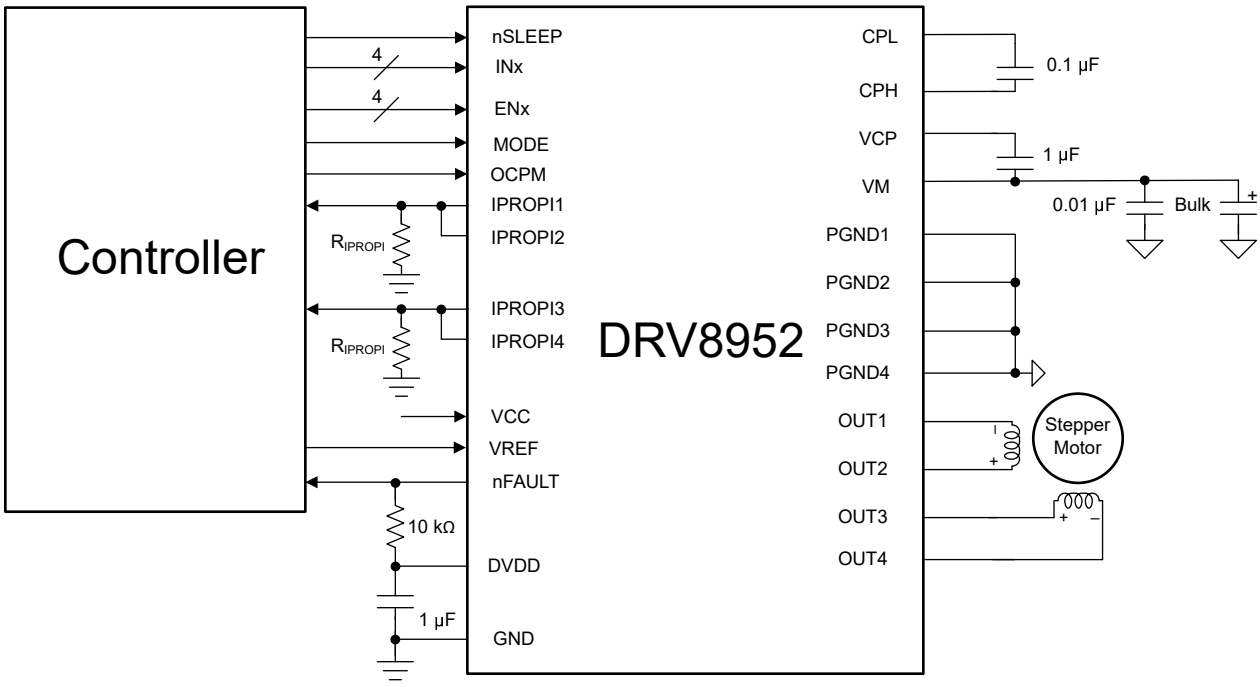


Figure 7-4. Driving Stepper Motor with DRV8952

The full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the VREF voltage and the resistor connected from IPROPI pin to ground (for the DDW package) or on the K_V parameter (for the PWP package). The maximum allowable voltage on the VREF pins is 3.3 V. DVDD can be used to provide VREF through a resistor divider.

Note

The I_{FS} current must also follow Equation 5 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{5}$$

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}), determine the frequency of the input waveform as follows -

$$f_{step}\ (steps/s) = \frac{v\ (rpm) \times 360\ (°/rot)}{\theta_{step}\ (°/step) \times n_m\ (steps/microstep) \times 60\ (s/min)} \tag{6}$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

The frequency f_{step} gives the frequency of input change on the DRV8952. 1/ f_{step} = t_{STEP} on the diagram below. Equation 7 shows an example calculation for a 120 rpm target speed and 1/2 step.

$$f_{step}\,(\text{steps/s}) = \frac{120\ \text{rpm} \times 360^\circ/\text{rot}}{1.8^\circ/\text{step} \times 1/2\ \text{steps/microstep} \times 60\ \text{s/min}} = 800\,\text{Hz} \quad (7)$$

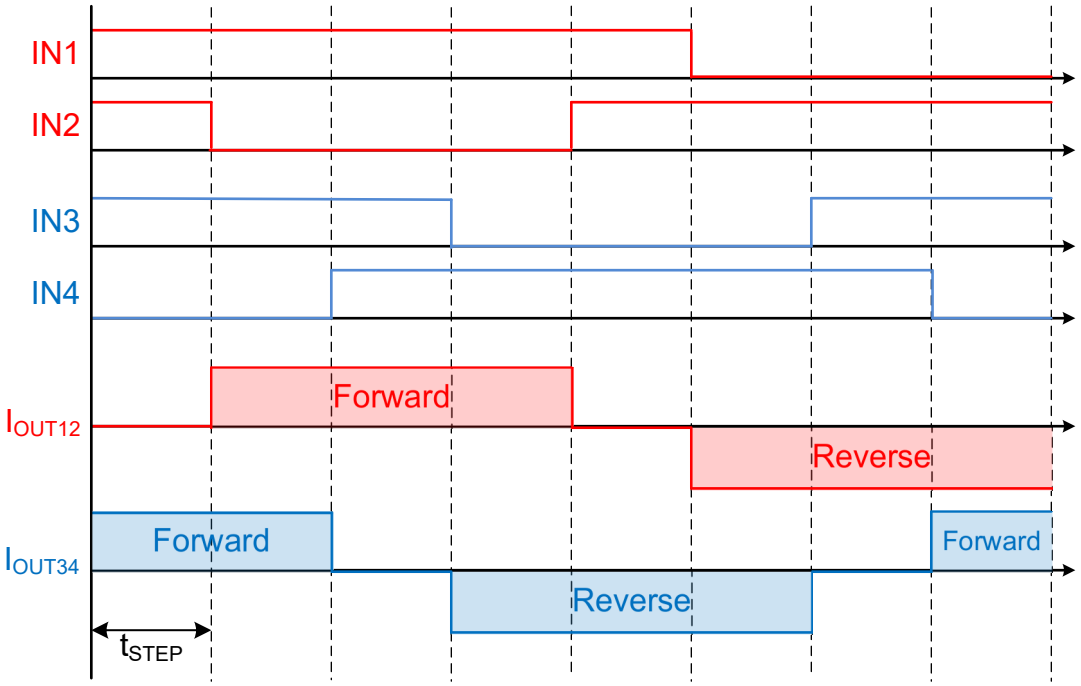


Figure 7-5. Example 1/2 Stepping Operation

For the DDW package, connect the IPROPI outputs corresponding to the same H-bridge together. IPROPI1 and IPROPI2, when connected together, reprsent the current of coil A of the stepper (connected between OUT1 and OUT2) during drive and slow-decay (high-side recirculation) modes. Similarly, IPROPI3 and IPROPI4, connected together, will reprsent coil B current. When two IPROPI pins are connected together, the effective current mirror gain will be 424 µA/A typical. The resistor from the combined IPROPI pin to ground should be selected accordingly.

7.1.2.2 Power Loss Calculations

The following calculations assume a use case where the supply voltage is 24 V, full-scale current is 5 A, rise/fall time is 140 ns and input PWM frequency is 30-kHz.

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 8.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \quad (8)$$

The conduction loss for the typical application shown in Section 7.1.2.1 is calculated in Equation 9.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (5\text{-A} / \sqrt{2})^2 \times (0.112\text{-}\Omega) = 2.8\text{-W} \quad (9)$$

The power loss due to the PWM switching frequency depends on the output voltage rise/fall time (t_{RF}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in Equation 10 and Equation 11.

$$P_{SW\_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (10)$$

$$P_{SW\_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (11)$$

After substituting the values of various parameters, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (140\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W} \quad (12)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (100\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W} \quad (13)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.178\text{-W} + 0.178\text{-W}) = 0.712\text{-W} \quad (14)$$

Note

The output rise/fall time (t_{RF}) is expected to change based on the supply-voltage, temperature and device to device variation.

When the VCC pin is connected to an external voltage, the quiescent current is typically 4 mA. The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (15)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 4\text{-mA} = 0.096\text{-W} \quad (16)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variations.

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in Equation 17.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 2.8\text{-W} + 0.712\text{-W} + 0.096\text{-W} = 3.608\text{-W} \quad (17)$$

7.1.2.3 Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 22.5 °C/W for the DDW package and 24.5 °C/W for the PWP package.

Assuming 25°C ambient temperature, the junction temperature for the DDW package is calculated as shown below -

$$T_J = 25°C + (3.608\text{-W} \times 22.5\ °C/W) = 106.2\ °C \quad (18)$$

The junction temperature for the PWP package is calculated as shown below -

$$T_J = 25°C + (3.608\text{-W} \times 24.5\ °C/W) = 113.4\ °C \quad (19)$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in the Typical Operating Characteristics section.

7.1.3 Driving Brushed-DC Motors

The DRV8952 can be used to drive one or two brushed-DC motors.

7.1.3.1 Brushed-DC Driver Typical Application

The schematic below shows the DRV8952 driving two brushed-DC motors.

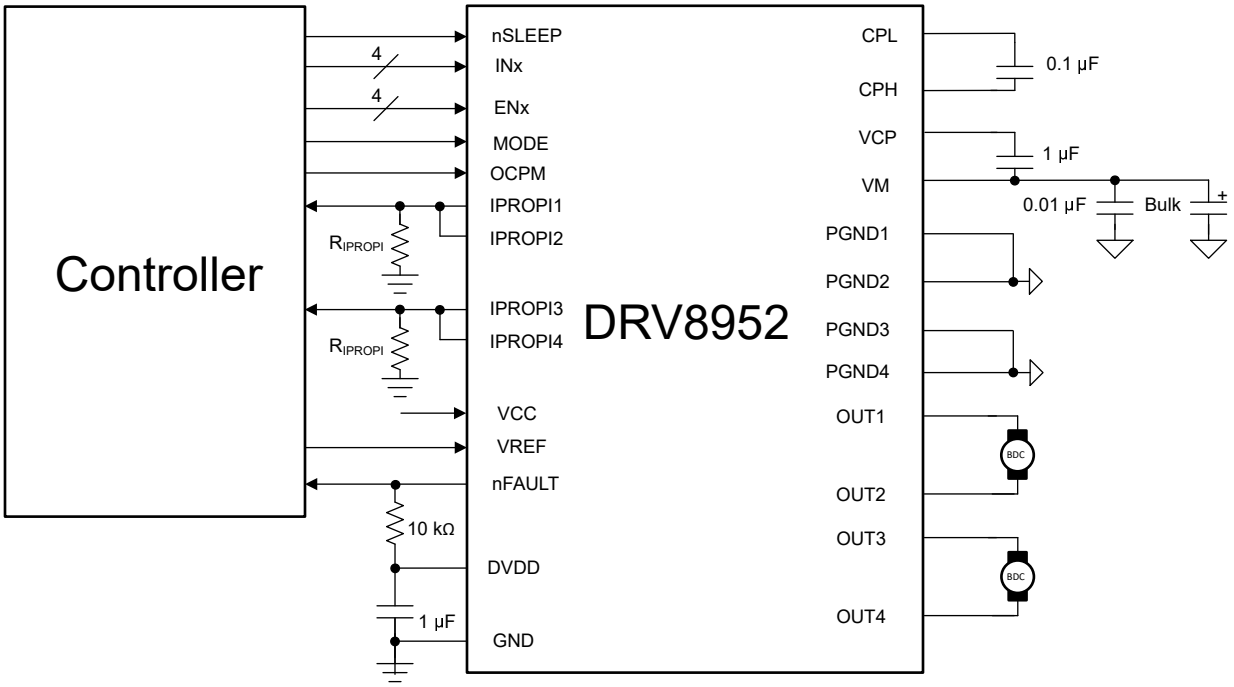


Figure 7-6. Driving two Brushed-DC Motors with DRV8952

The following truth table describes how to control brushed-DC motors -

Table 7-1. Brushed-DC Motor Truth Table

Function	EN1	EN2	IN1	IN2	OUT1	OUT2
Forward	1	1	1	PWM	H	H/L
Reverse	1	1	PWM	1	H/L	H
Brake	1	1	1	1	H	H
Brake*	1	1	0	0	L	L
Coast*	0	X	X	X	Z	X
Coast*	X	0	X	X	X	Z

Note

* IPROPI pins of the DDW package can not output proportional current in these conditions.

7.1.3.2 Power Loss Calculation

For a H-bridge with high-side recirculation, power dissipation for each FET can be approximated as follows:

- $P_{HS1} = R_{DS(ON)} \times I_L^{\ 2}$
- $P_{LS1} = 0$

- $P_{HS2} = [R_{DS(ON)} \times I_L{}^2 \times (1-D)] + [2 \times V_D \times I_L \times t_D \times f_{PWM}]$
- $P_{LS2} = [R_{DS(ON)} \times I_L{}^2 \times D] + [VM \times I_L \times t_{RF} \times f_{PWM}]$

For estimating power dissipation for load current flow in the reverse direction, identical equations apply, with only swapping of HS1 with HS2 and LS1 with LS2.

Substituting the following values in the equations above -

- VM = 24 V
- I_L = 4 A
- $R_{DS(ON)}$ = 56 mΩ
- D = 0.5
- V_D = 1 V
- t_D = 300 ns
- t_{RF} = 140 ns
- f_{PWM} = 20 kHz

The losses in each FET can be calculated as follows -

$P_{HS1} = 56\ m\Omega \times 4^2 = 0.896\ W$

$P_{LS1} = 0$

$P_{HS2} = [56\ m\Omega \times 4^2 \times (1-0.5)] + [2 \times 1\ V \times 4\ A \times 300\ ns \times 20\ KHz] = 0.496\ W$

$P_{LS2} = [\ 56\ m\Omega \times 4^2 \times 0.5] + [24 \times 4\ A \times 140\ ns \times 20\ kHz] = 0.717\ W$

Quiescent Current Loss $P_Q = 24\ V \times 4\ mA = 0.096\ W$

$P_{TOT} = 2 \times (P_{HS1} + P_{LS1} + P_{HS2} + P_{LS2}) + P_Q = 2 \times (0.896 + 0 + 0.496 + 0.717) + 0.096 = 4.314\ W$

7.1.3.3 Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 22.5 °C/W for the DDW package and 24.5 °C/W for the PWP package.

Assuming 25°C ambient temperature, the junction temperature for the DDW package is calculated as shown below -

$$T_J = 25°C + (4.314\text{-W} \times 22.5\ °C/W) = 122.1\ °C \quad (20)$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature.

7.1.3.4 Driving Single Brushed-DC Motor

The outputs of DRV8952 can be connected in parallel to increase the drive current. Figure 7-7 shows the schematic of DRV8952 driving a single brushed-DC motor.

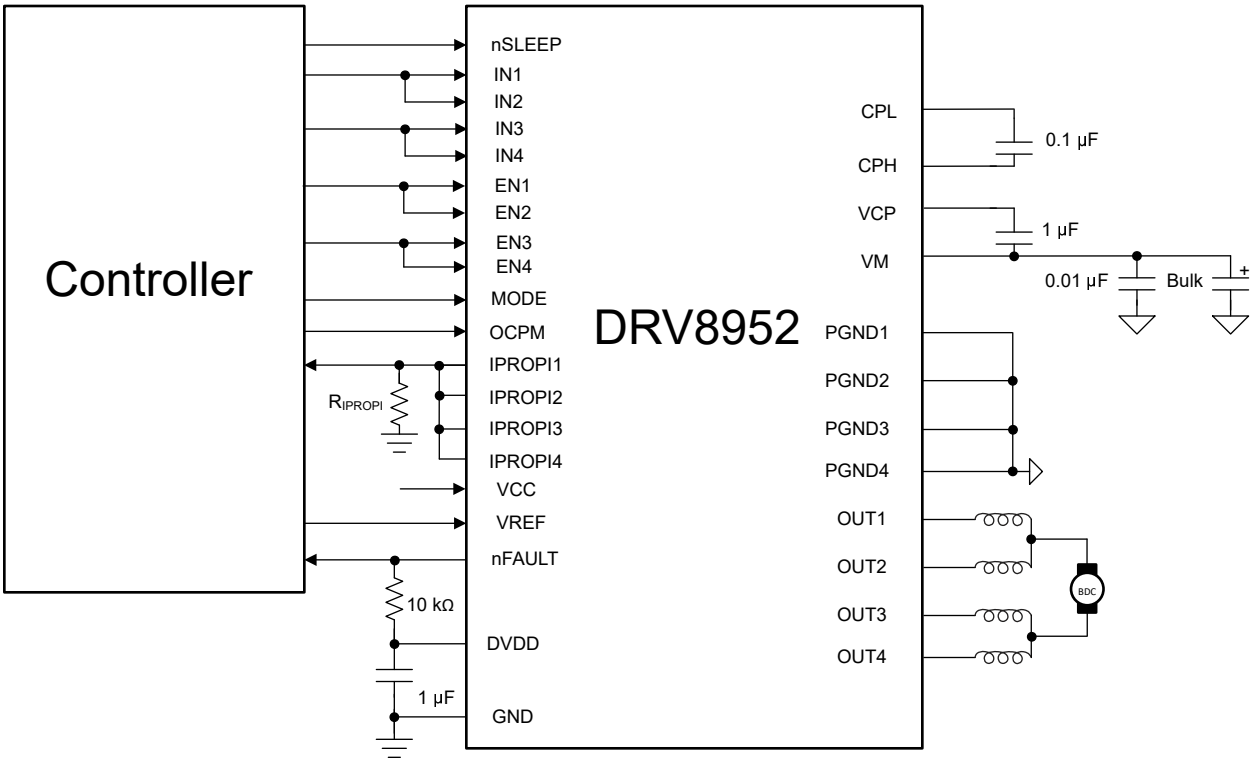


Figure 7-7. Driving Single Brushed-DC motor with DRV8952

In this mode, a minimum of 30 nH to 100 nH inductance or a ferrite bead is required after the output pins before connecting the two channels together. This will help to prevent any shoot through between two paralleled channels during switching transient due to mismatch of paralleled channels (for example, asymmetric PCB layout, etc).

7.1.4 Driving Thermoelectric Coolers (TEC)

Thermoelectric coolers (TEC) work according to the Peltier effect. When a voltage is applied across the TEC, a DC current flows through the junction of the semiconductors, causing a temperature difference. Heat is transferred from one side of the TEC to the other. This creates a “hot” and a “cold” side of the TEC element. If the DC current is reversed, the hot and cold sides reverse as well.

A common way of modulating the current through the TEC is to use PWM driving and make the average current change by varying the ON and OFF duty cycles. To allow both heating and cooling from a single supply, a H-bridge topology is required. The DRV8952 can drive two H-bridges to drive two TECs bi-directionally with up to 5-A current. Pair of half-bridges can also be paralleled together to drive a single TEC with up to 10-A current.

The DRV8952 in DDW package also features current sense output (IPROPI) with 5% accuracy to eliminate the need for two external shunt resistors in a closed-loop control topology, saving bill-of-materials cost and space. Figure 7-8 shows the schematic of two TECs connected to a DRV8952 driver.

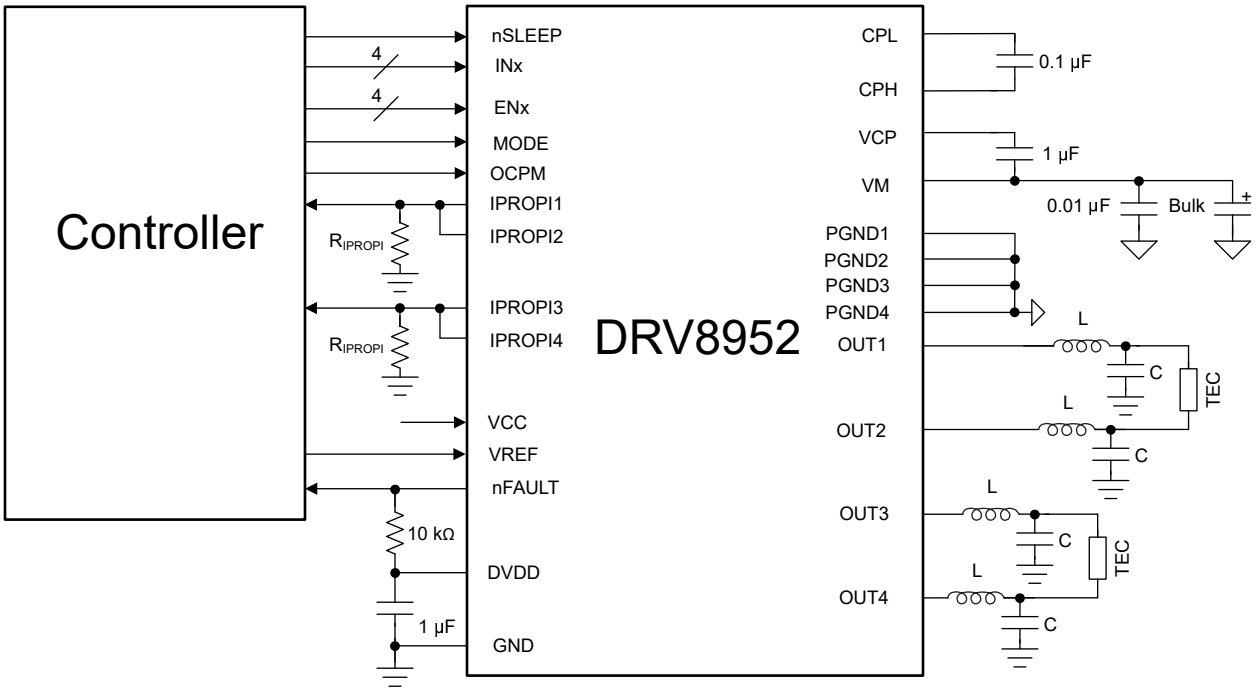


Figure 7-8. Driving two TECs

Figure 7-9 shows the schematic to drive one TEC with higher current.

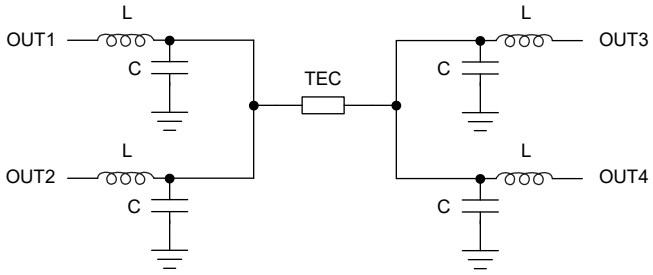


Figure 7-9. Driving one TEC with higher current

The LC filters connected to the output nodes convert the PWM output from the DRV8952 into a low-ripple DC voltage across the TEC. The filters are required to minimize the ripple current, because fast transients (e.g., square wave power) can shorten the life of the TEC. The maximum ripple current is recommended to be less than 10% of maximum current. The maximum temperature differential across the TEC, which decreases as ripple current increases, is calculated with the following equation:

$$\Delta T = \Delta T_{MAX} / (1 + N^2) \quad (21)$$

Where ΔT is actual temperature differential, ΔT_{MAX} is maximum possible temperature differential specified in the TEC datasheet, N is the ratio between ripple and maximum current. N should not be greater than 0.1.

The choice of the input PWM frequency is a trade-off between switching loss and use of smaller inductors and capacitors. High PWM frequency also means that the voltage across the TEC can be tightly controlled, and the LC components can potentially be cheaper.

The transfer function of a second order low-pass filter is shown in Equation 21:

$$H(j\omega) = 1 / (1 - (\omega / \omega_0)^2 + j\omega / Q\omega_0) \quad (22)$$

Where,

ω_0 = 1 / √(LC), resonant frequency of the filter

Q = quality factor

ω = DRV8952 input PWM frequency

The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the PWM frequency. With this assumption, Equation 21 may be simplified to -

H in dB = -40 log (f_S/f_0)

Where f_0 = 1/ 2π√(LC) and f_S is the input PWM switching frequency.

- If L = 10 µH and C = 22 µF, the resonant frequency is 10.7 kHz.
- This resonant frequency corresponds to 39 dB of attenuation at 100 kHz switching frequency.
- For VM = 24 V, 39 dB attenuation means that the amount of ripple voltage across the TEC element will be approximately 270 mV.
- For a TEC element with a resistance of 1.5 Ω, the ripple current through the TEC will therefore be 180 mA.
- At the 5-A maximum output current of the DRV8952, 180 mA corresponds to 3.6% ripple current.
- This will cause about 0.13 % reduction of the maximum temperature differential of the TEC element, as per Equation 21.

Adjust the LC values according to the supply voltage and DC current through the TEC element. The DRV8952 supports up to 200 kHz input PWM frequency. The power loss in the device at any given ambient temperature must be carefully considered before selecting the input PWM frequency.

Closing the loop on current is important in some TEC based heating and cooling systems. The DRV8952 in DDW package can achieve this without the need for external current shunt resistors. Internal current mirrors are used to monitor the currents in each half-bridge and this information is available on IPROPI pins. A microcontroller can monitor and adjust the PWM duty based on the IPROPI pin voltage. When driving two TECs, connect the IPROPI pins of the corresponding half-bridges together to measure the H-bridge current. For example, for the schematic shown in Figure 7-8, IPROPI1 and IPROPI2 are tied together, and IPROPI3 and IPROPI4 are also together. When driving only one TEC as shown in Figure 7-9, tie all the IPROPI pins together.

Additionally, the DRV8952 can regulate the current internally by providing an external voltage reference (VREF) to the device to adjust the current regulation trip point. The current loop would then be closed within the H-bridge itself.

7.1.5 Driving Brushless DC Motors

The DRV8952 can also be used to drive a three-phase brushless DC (BLDC) motor. The DRV8952 supports independent control of three phases required to drive the BLDC motor. One of the four half-bridges of the DRV8952 can be disabled while driving a BLDC motor, by connecting the corresponding EN pin to ground. Figure 7-10 shows a schematic of the DRV8952 driving a BLDC motor.

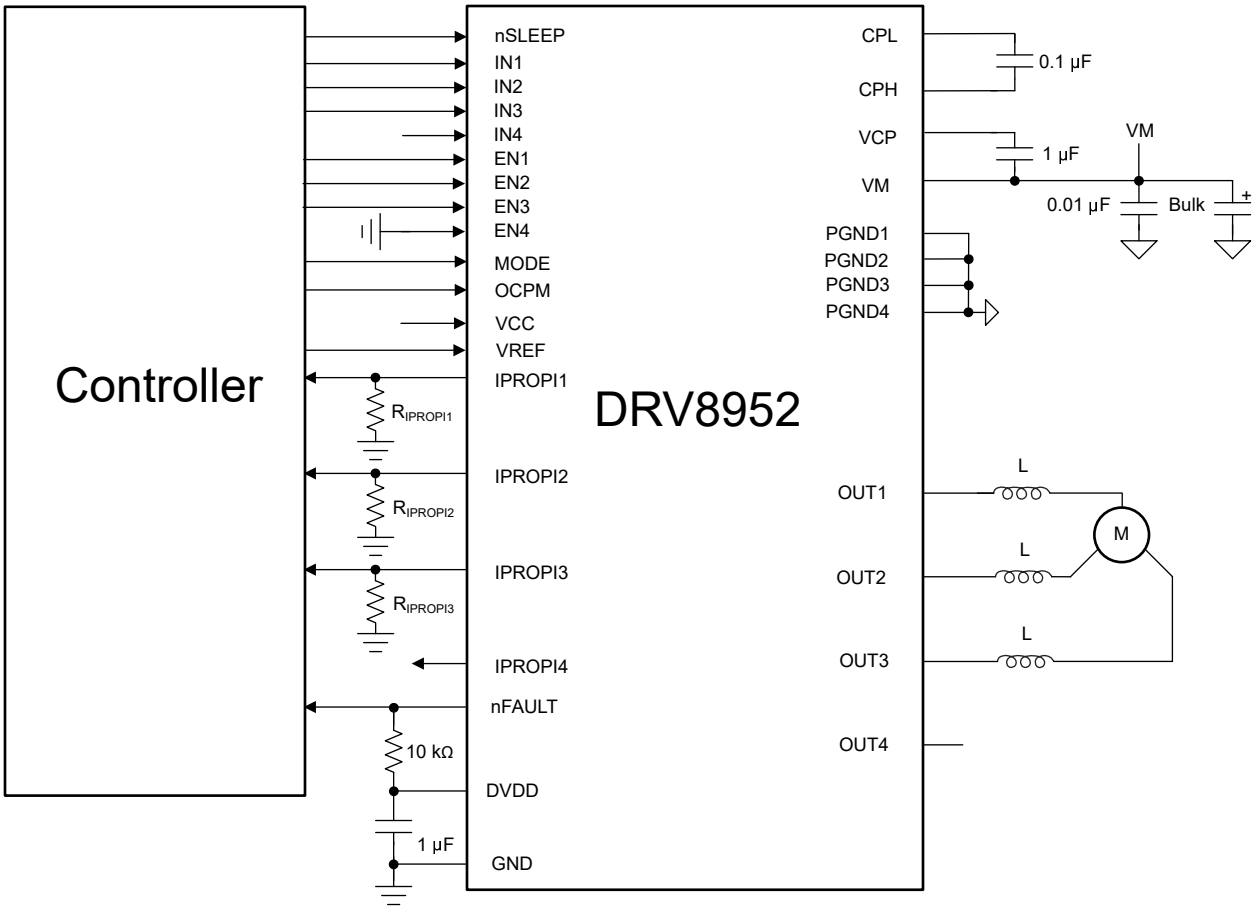


Figure 7-10. Driving BLDC Motor with DRV8952

The three half-bridges required to drive a BLDC motor can be controlled by six inputs - EN1, EN2, EN3 and IN1, IN2, IN3.

- When EN1 is low, OUT1 becomes high-impedance, allowing current to flow through the internal body diodes of the high-side and low-side FETs.
- When EN1 is high and IN1 is low, OUT1 is driven low with its low-side FET enabled.
- When EN1 is high and IN1 is high, OUT1 is driven high with its high-side FET enabled.
- Likewise is true for OUT2 and OUT3.
- EN4 can be grounded to permanently disable OUT4.

A minimum of 30 nH to 100 nH inductance or a ferrite bead has to be connected after the output pins. This will help to prevent any shoot through due to mismatch between channels (for example, process variation, unsymmetrical PCB layout, etc).

The IPROPI pins of the DDW package output a current proportional to the current flowing through the high-side FET of each half-bridge. The IPROPI output accuracy at maximum rated current is 5%.

$I_{IPROPI} = I_{HS} \times A_{IPROPI}$

Each IPROPI pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC).

$V_{IPROPI} = IPROPI \times R_{IPROPI}$

If higher accuracy of current sensing is required or for the PWP package, external sense resistors can be placed between the PGND pins and system ground. The voltage drop across the external sense resistor should not exceed 300 mV.

7.2 Power Supply Recommendations

The DRV8952 is designed to operate from an input voltage supply (VM) range from 4.5 V to 55 V. A 0.01-µF ceramic capacitor rated for VM must be placed close to the VM pins of DRV8952. In addition, a bulk capacitor must be included on VM.

7.2.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and system
- The acceptable voltage ripple

The inductance between the power supply and system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps with a change in voltage. When adequate bulk capacitance is used, the voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

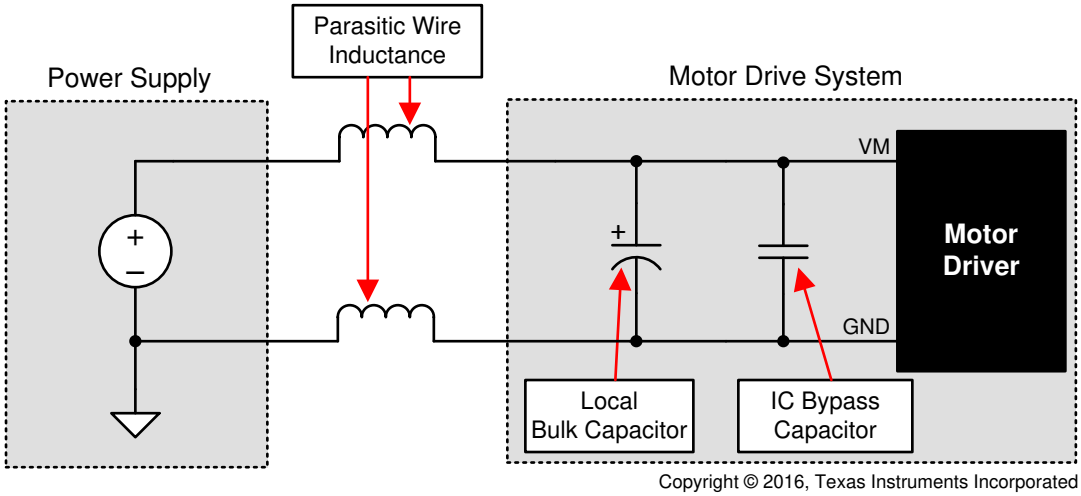


Figure 7-11. Example Setup of System With External Power Supply

7.2.2 Power Supplies

The DRV8952 needs only a single supply voltage connected to the VM pins.

- The VM pin provides the power supply to the half-Bridges.
- An internal voltage regulator provides a 5V supply (DVDD) for the digital and low-voltage analog circuitry. The DVDD pin is not recommended to be used as a voltage source for external circuitry.

- For the DDW package, an external low-voltage supply can be connected to the VCC pin to power the internal circuitry. A 0.1-µF decoupling capacitor should be placed close to the VCC pin to provide a constant voltage during transient.
- Additionally, the high-side gate drive requires a higher voltage supply, which is generated by built-in charge pump requiring external capacitors.

7.3 Layout

7.3.1 Layout Guidelines

- The VM pins should be bypassed to PGND pins using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VM. The capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device PGND pins.
- The VM pins should be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.
- A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.
- Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- For the DDW package, bypass the VCC pin to ground with a low-ESR ceramic capacitor. A value of 0.1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD must be connected to system ground.
  - It is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer.
  - In order to minimize the impedance and inductance, the traces from ground pins should be as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Multiple vias are suggested to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD will also help spreading the heat and reduce the thermal resistance.

7.3.2 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper on both top and bottom layer is recommended for improved thermal performance and better EMI margin (due to lower PCB trace inductance).

7.3.3 Thermal Considerations

Thermal pad of the package is attached at bottom of the device to improve the thermal capability. The thermal pad has to be soldered with a very good coverage on PCB to deliver the power specified in the data sheet. Refer to the Section 7.3.1 section for more details.

8 Package Thermal Considerations

8.1 DDW Package

The thermal pad of the package has to be soldered with a very good coverage on PCB to deliver the power specified in the data sheet. Refer to the Section 7.3.1 section for more details.

8.1.1 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria:

HTSSOP (DDW package)

- 2-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the thermal pad (13 x 5 thermal via array, 1.1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: HTSSOP package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Bottom layer: ground plane thermally connected through vias under the thermal pad for the driver. Bottom layer copper area varies with top copper area.
- 4-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the thermal pad (13 x 5 thermal via array, 1.1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: HTSSOP package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Mid layer 1: GND plane thermally connected to thermal pad through vias. The area of the ground plane varies with top copper area.
  - Mid layer 2: power plane, no thermal connection. The area of the power plane varies with top copper area.
  - Bottom layer: signal layer thermally connected through via stitching from the TOP and internal GND plane. Bottom layer thermal pad is the same size as the top layer copper area.

Figure 8-1 shows an example of the simulated board for the DDW package. Table 8-1 shows the dimensions of the board that were varied for each simulation.

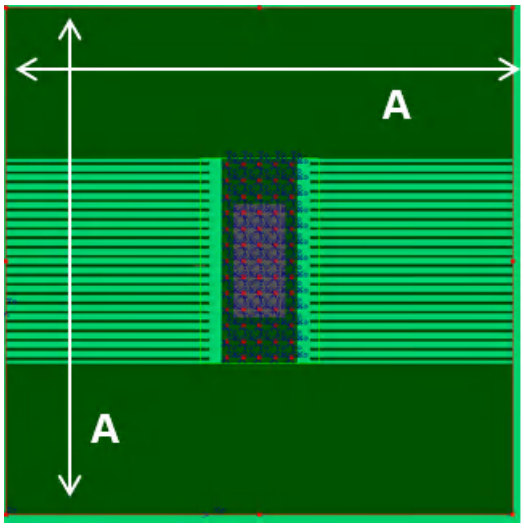


Figure 8-1. DDW PCB model top layer

Table 8-1. Dimension A for DDW package

Cu area (cm^2)	Dimension A (mm)
2	19.79
4	26.07
8	34.63
16	46.54
32	63.25

8.1.1.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the driver operates with a constant RMS current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

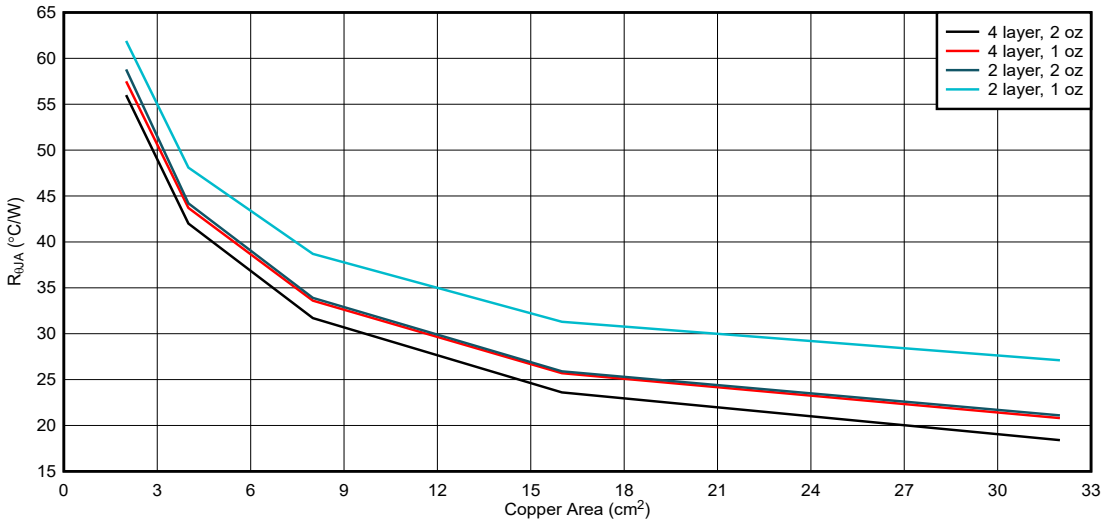


Figure 8-2. DDW Package, PCB junction-to-ambient thermal resistance vs copper area

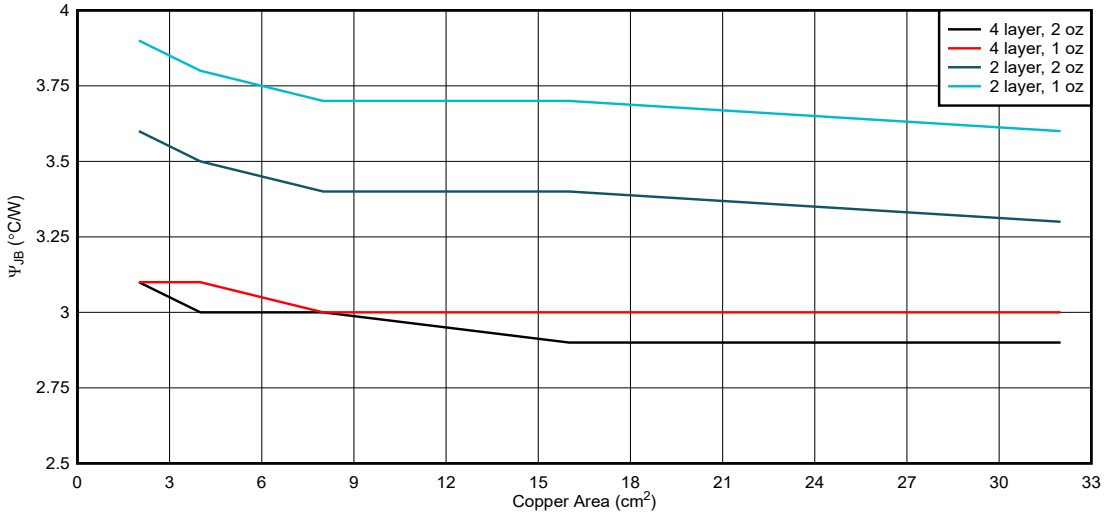


Figure 8-3. DDW Package, junction-to-board characterization parameter vs copper area

8.1.1.2 Transient Thermal Performance

The driver may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include -

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1-oz and 2-oz copper layouts for the DDW package. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

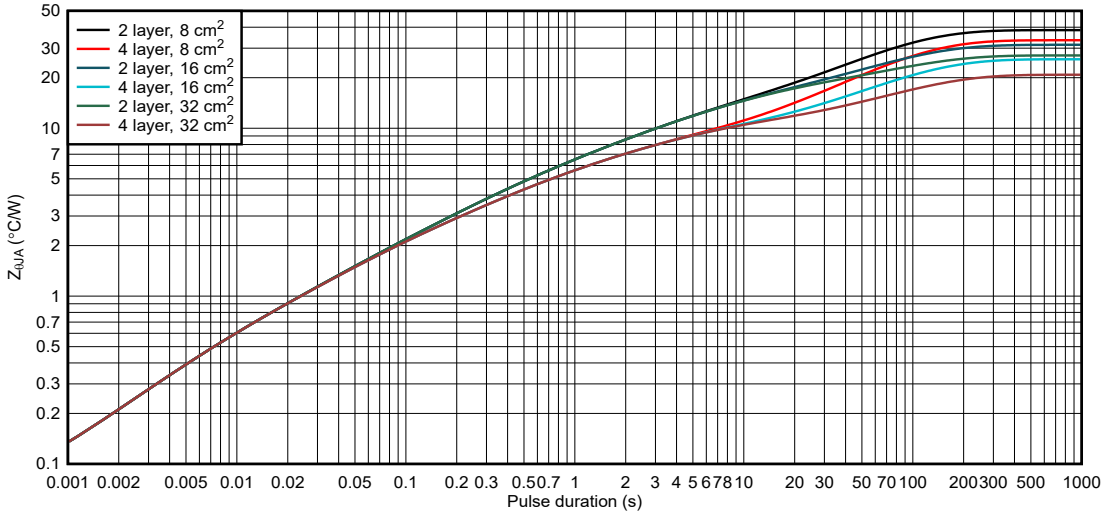


Figure 8-4. DDW package junction-to-ambient thermal impedance for 1-oz copper layouts

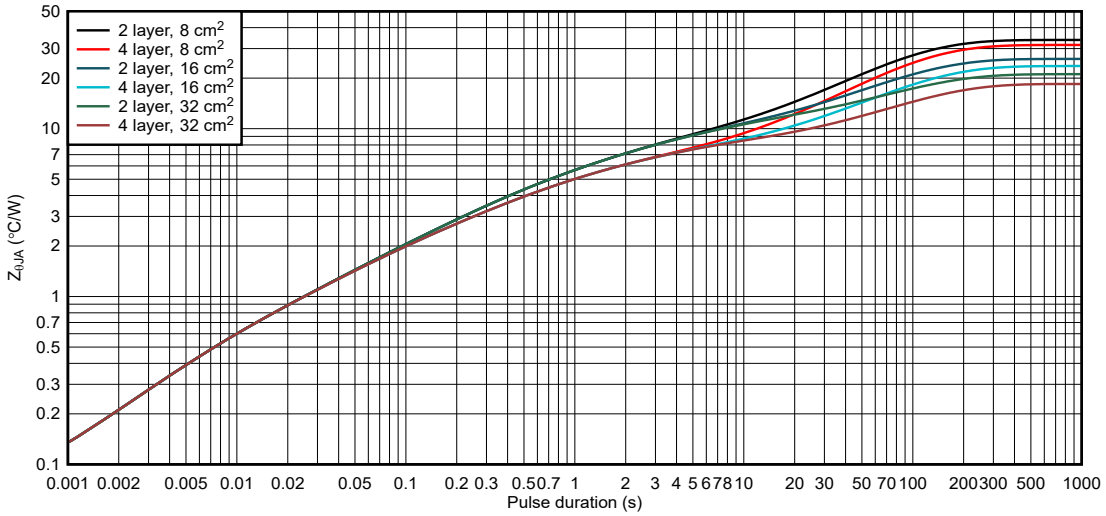


Figure 8-5. DDW package junction-to-ambient thermal impedance for 2-oz copper layouts

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Related Documentation

- Texas Instruments, *How to Drive Unipolar Stepper Motors with DRV8xxx* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Motor Drives Layout Guide* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *What Motor Drivers should be considered for driving TEC*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

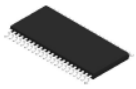
Changes from Revision * (March 2023) to Revision A (January 2025)	Page
• Added PWP packaged to data sheet.	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

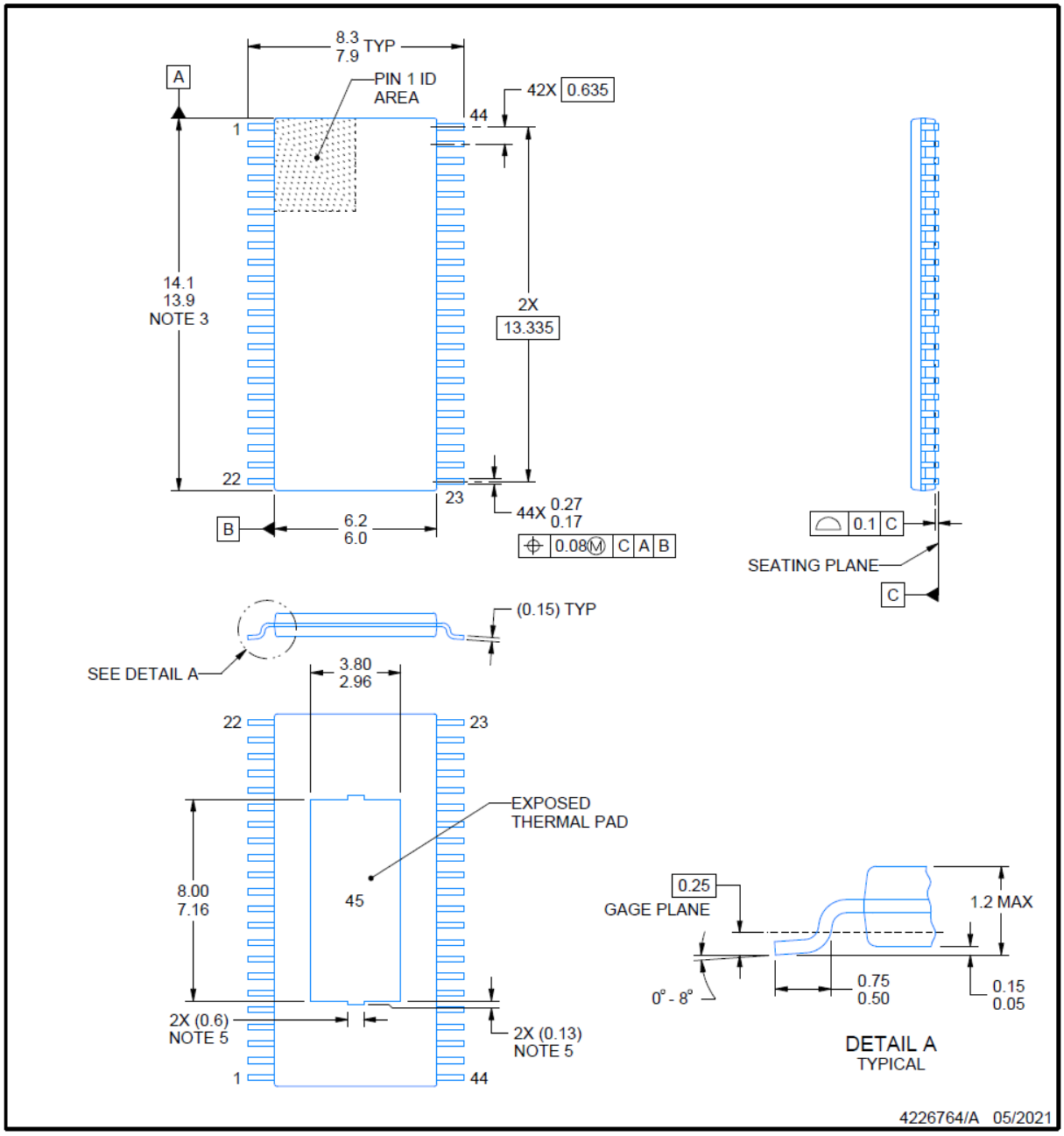
PACKAGE OUTLINE

DDW0044E



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

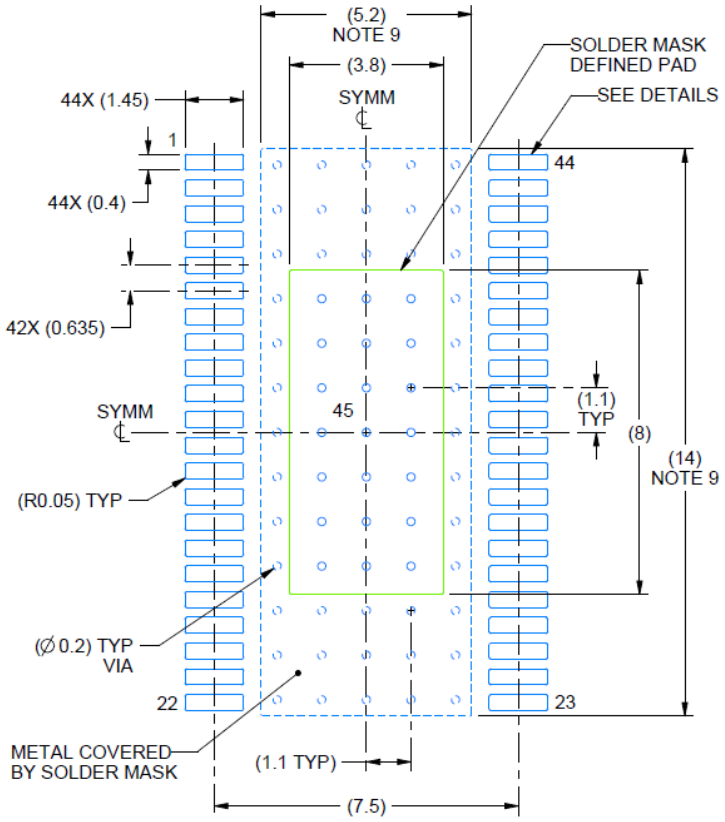
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

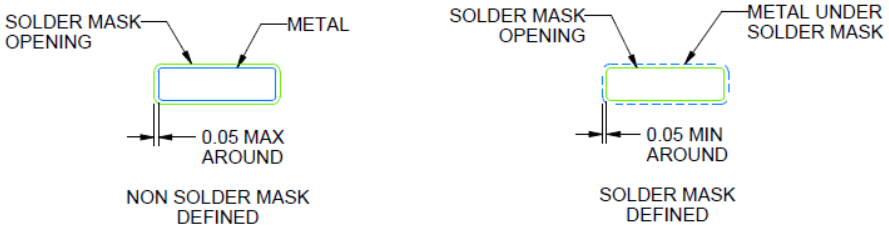
DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4226764/A 05/2021

NOTES: (continued)

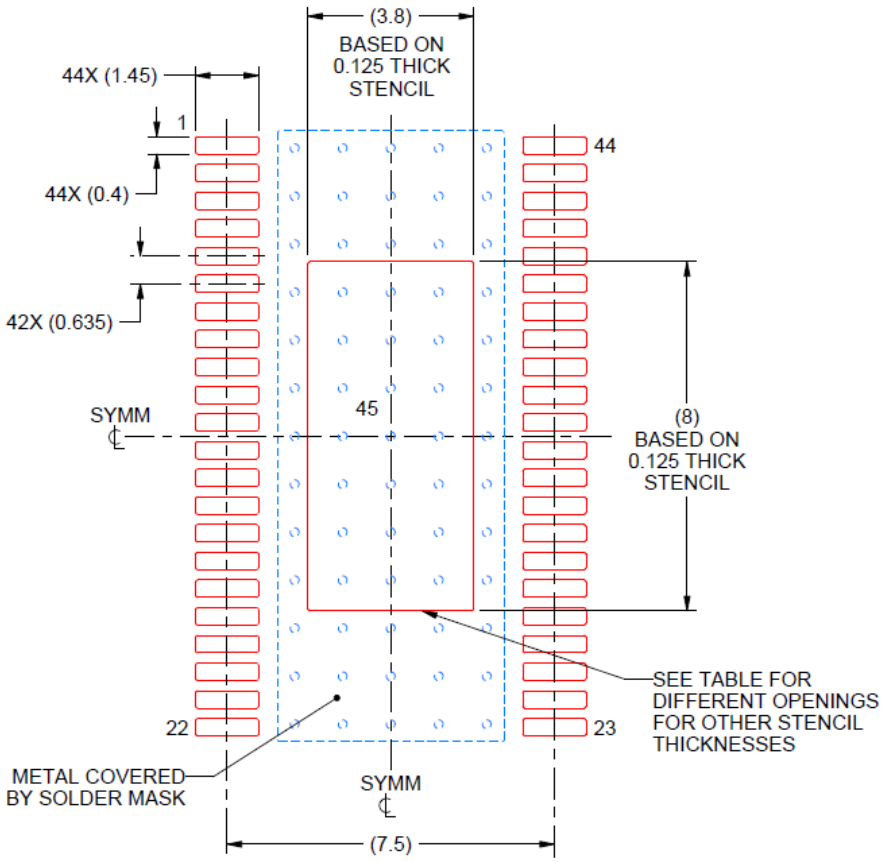
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

4226764/A 05/2021

NOTES: (continued)

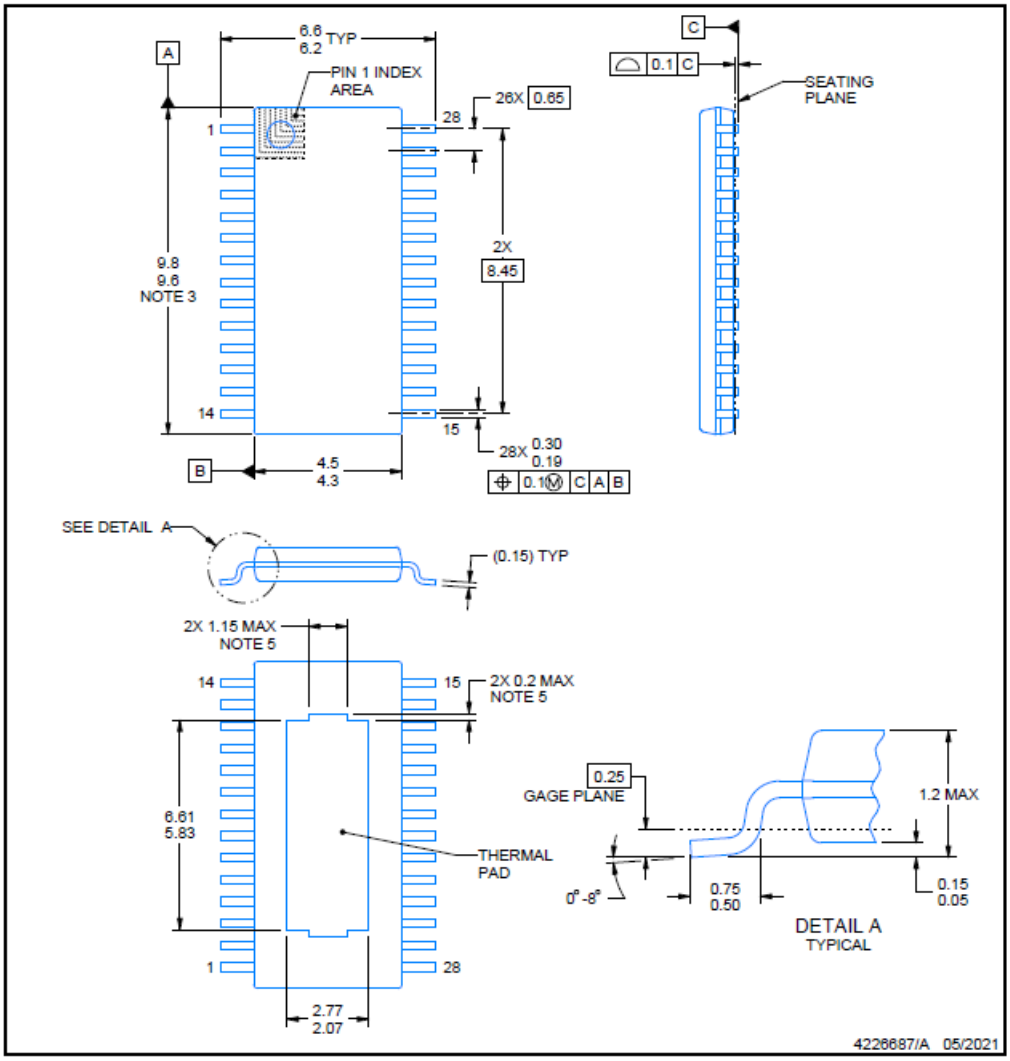
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PWP0028T

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

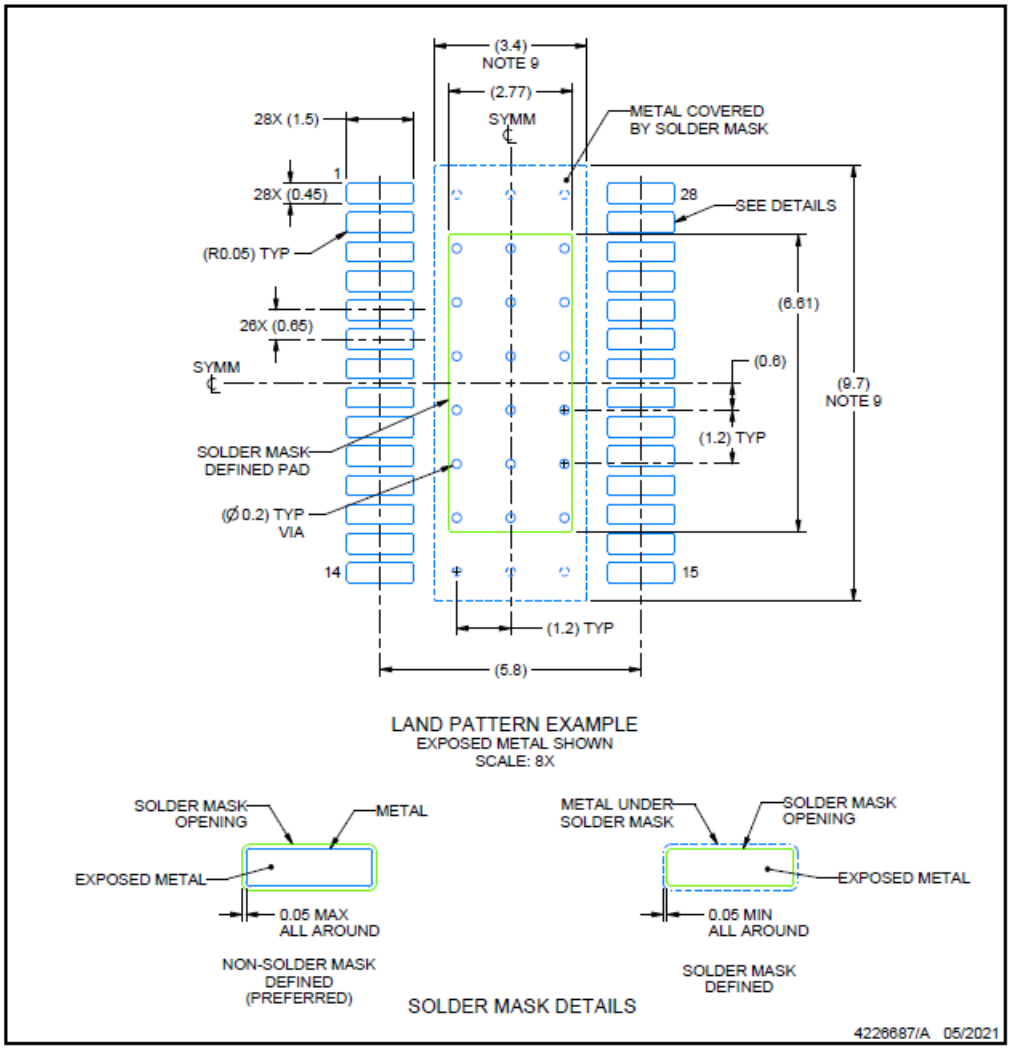
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028T — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



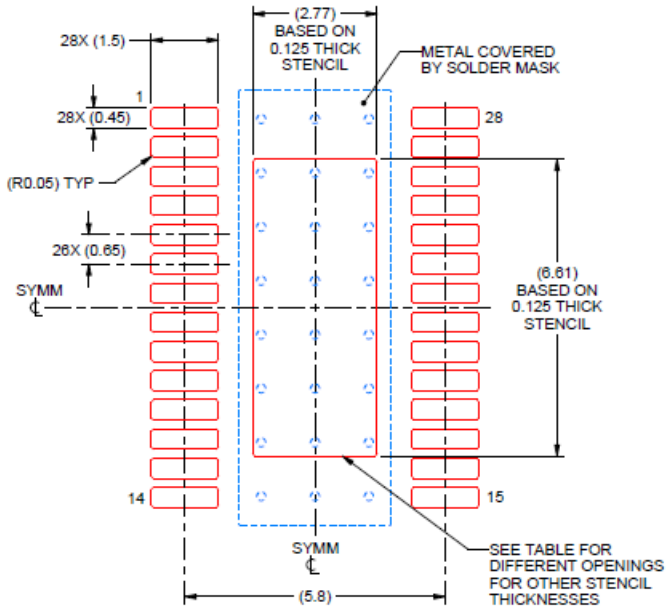
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028T — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

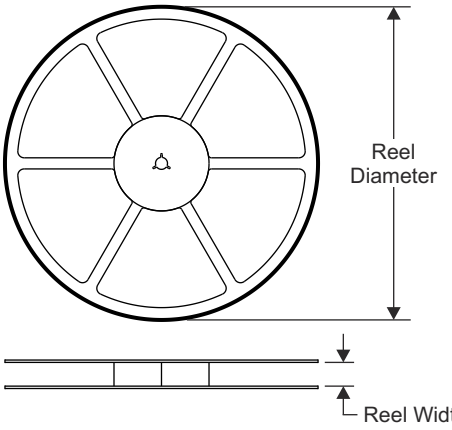
4226687/A 05/2021

NOTES: (continued)

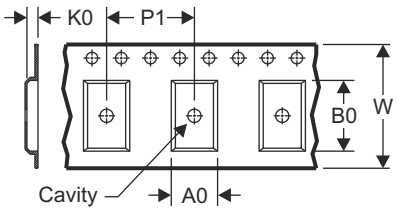
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

11.1 Tape and Reel Information

REEL DIMENSIONS

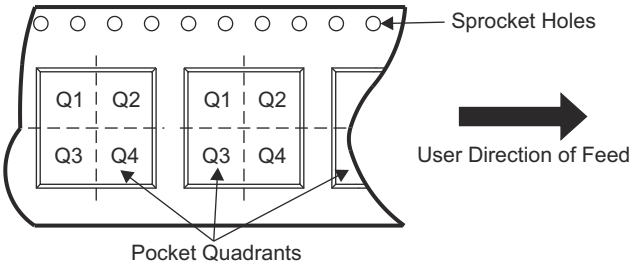


TAPE DIMENSIONS



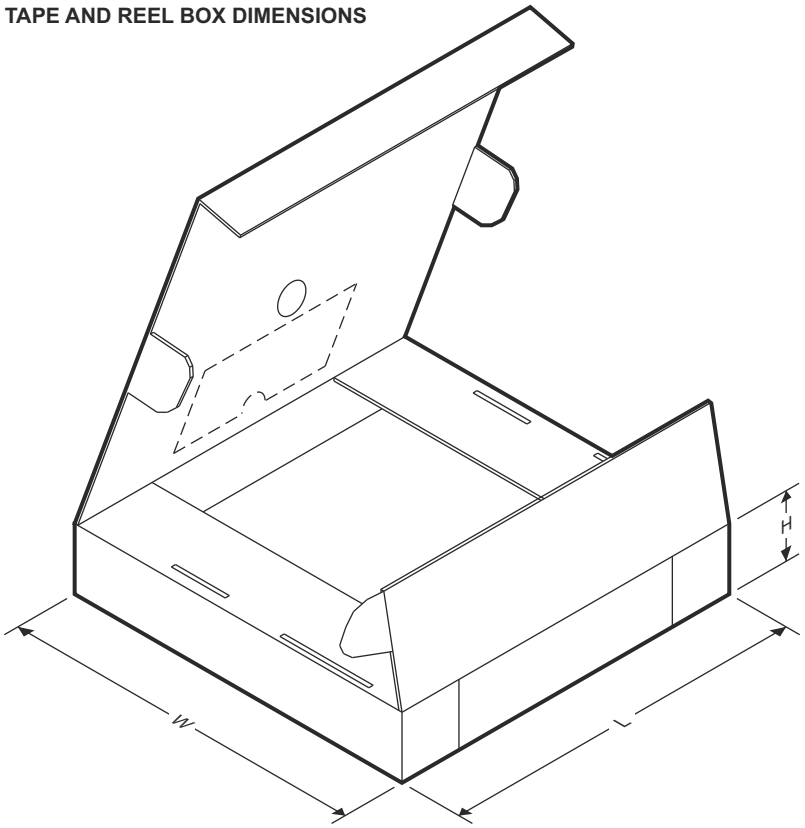
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8952PWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.75	10.1	1.8	12	16	Q1
DRV8952DDWR	HTSSOP	DDW	44	2500	330.0	24.4	8.9	14.7	1.4	12	24	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8952PWPR	HTSSOP	PWP	28	2500	356.0	356.0	35.0
DRV8952DDWR	HTSSOP	DDW	44	2500	367.0	367.0	45.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8952DDWR	Active	Production	HTSSOP (DDW) | 44	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8952
DRV8952DDWR.A	Active	Production	HTSSOP (DDW) | 44	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8952
DRV8952PWPR	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8952
DRV8952PWPR.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8952

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

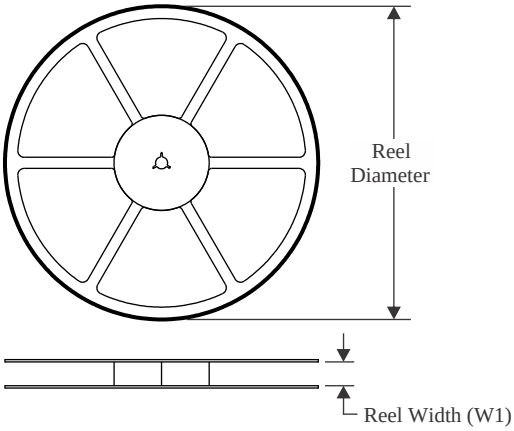
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

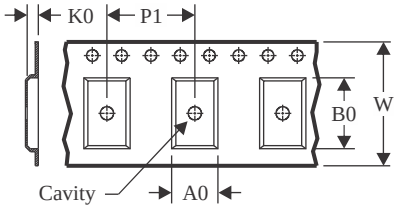
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

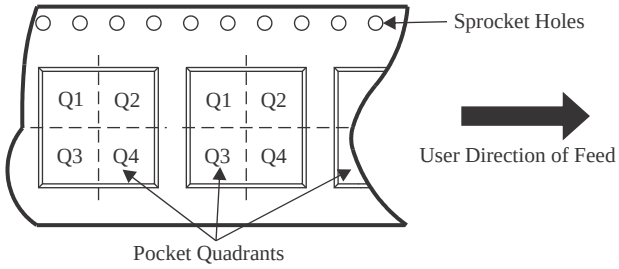


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

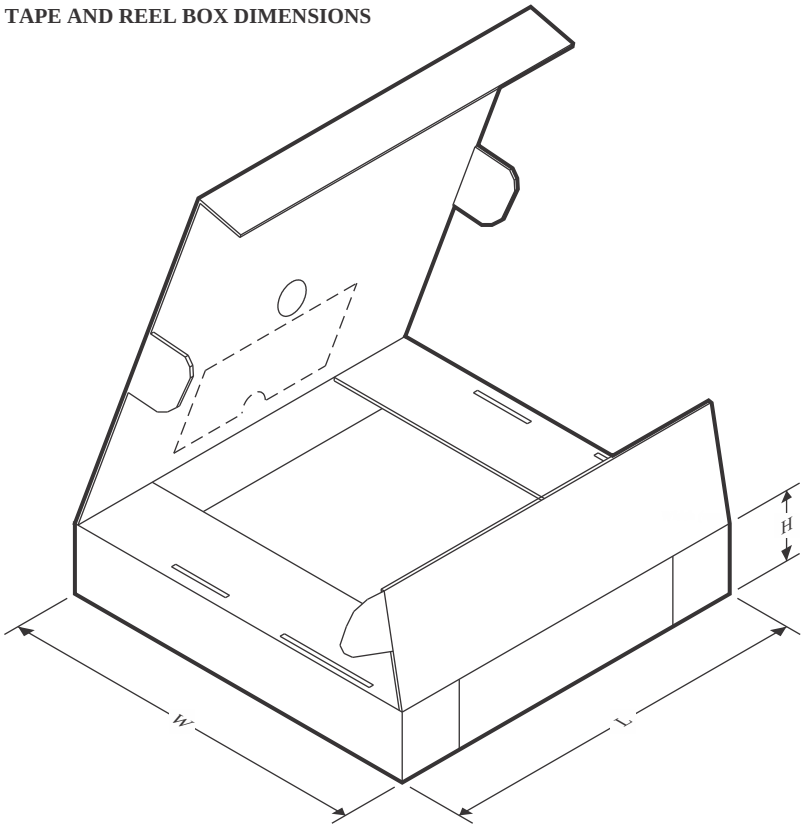
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8952DDWR	HTSSOP	DDW	44	2500	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
DRV8952PWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8952DDWR	HTSSOP	DDW	44	2500	356.0	356.0	45.0
DRV8952PWPR	HTSSOP	PWP	28	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

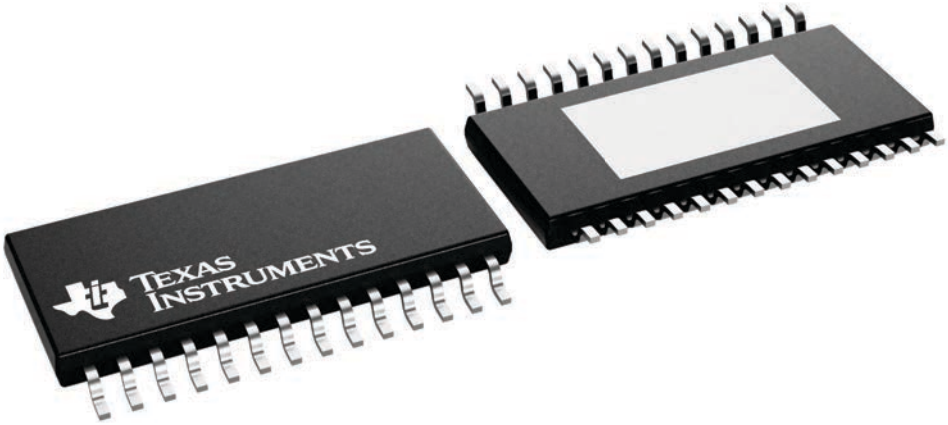
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

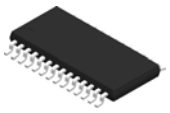
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

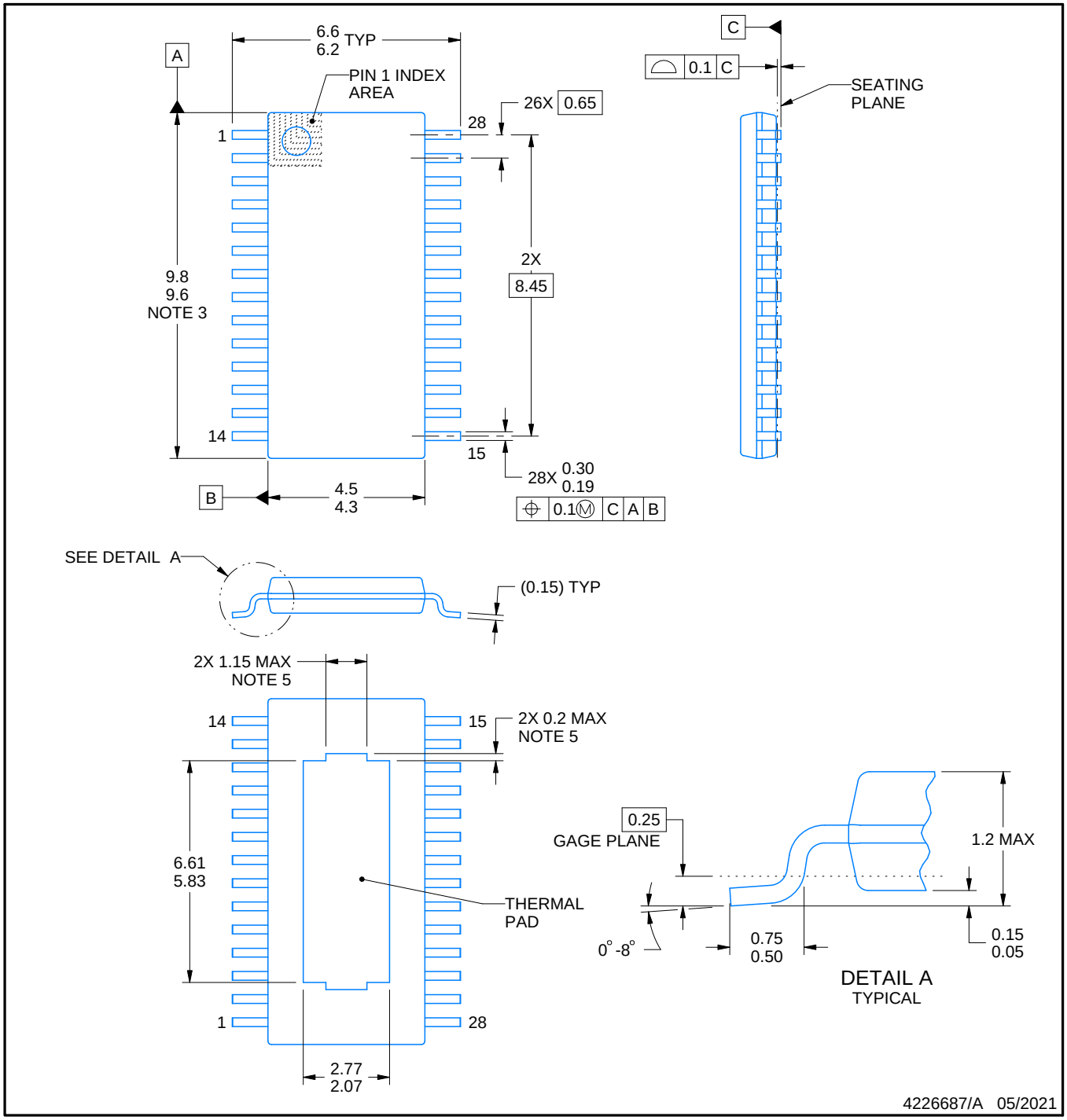
PACKAGE OUTLINE

PWP0028T



PowerPAD™ TSSOP - 1.2 mm max height

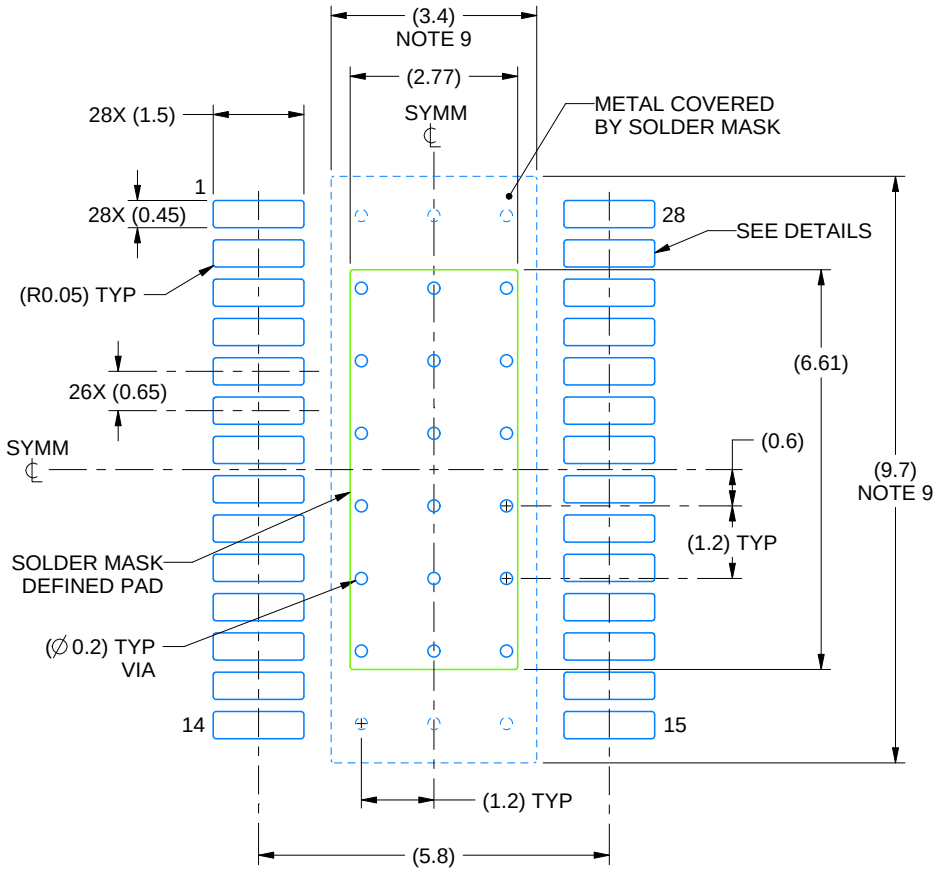
SMALL OUTLINE PACKAGE



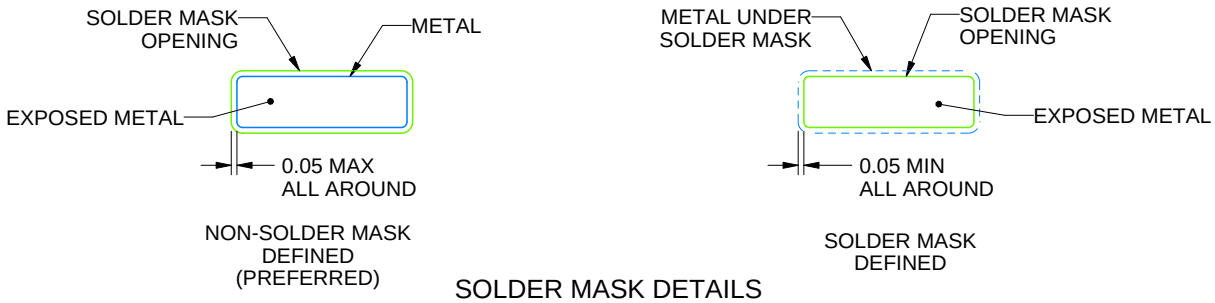
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

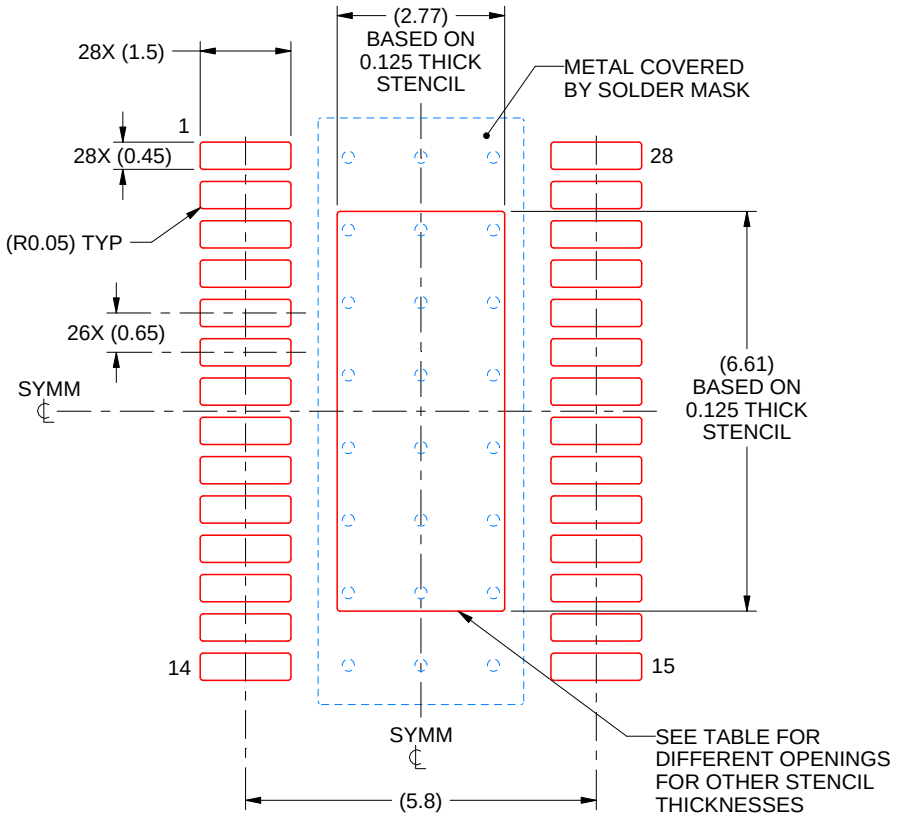


SOLDER MASK DETAILS

4226687/A 05/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

4226687/A 05/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

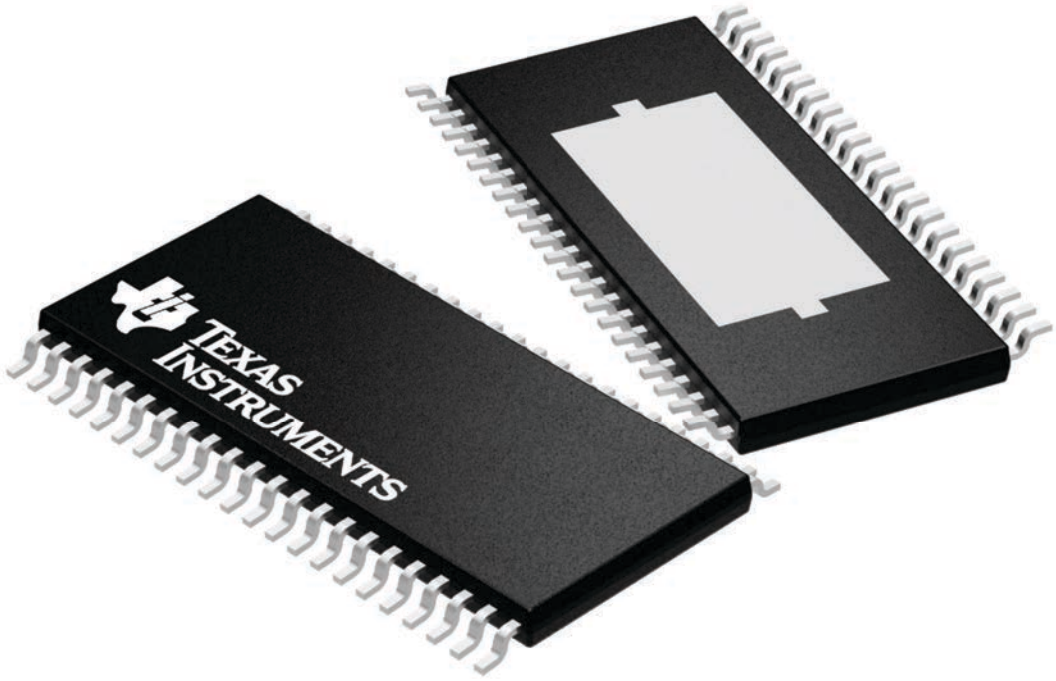
DDW 44

PowerPAD TSSOP - 1.2 mm max height

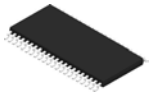
6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224876/A

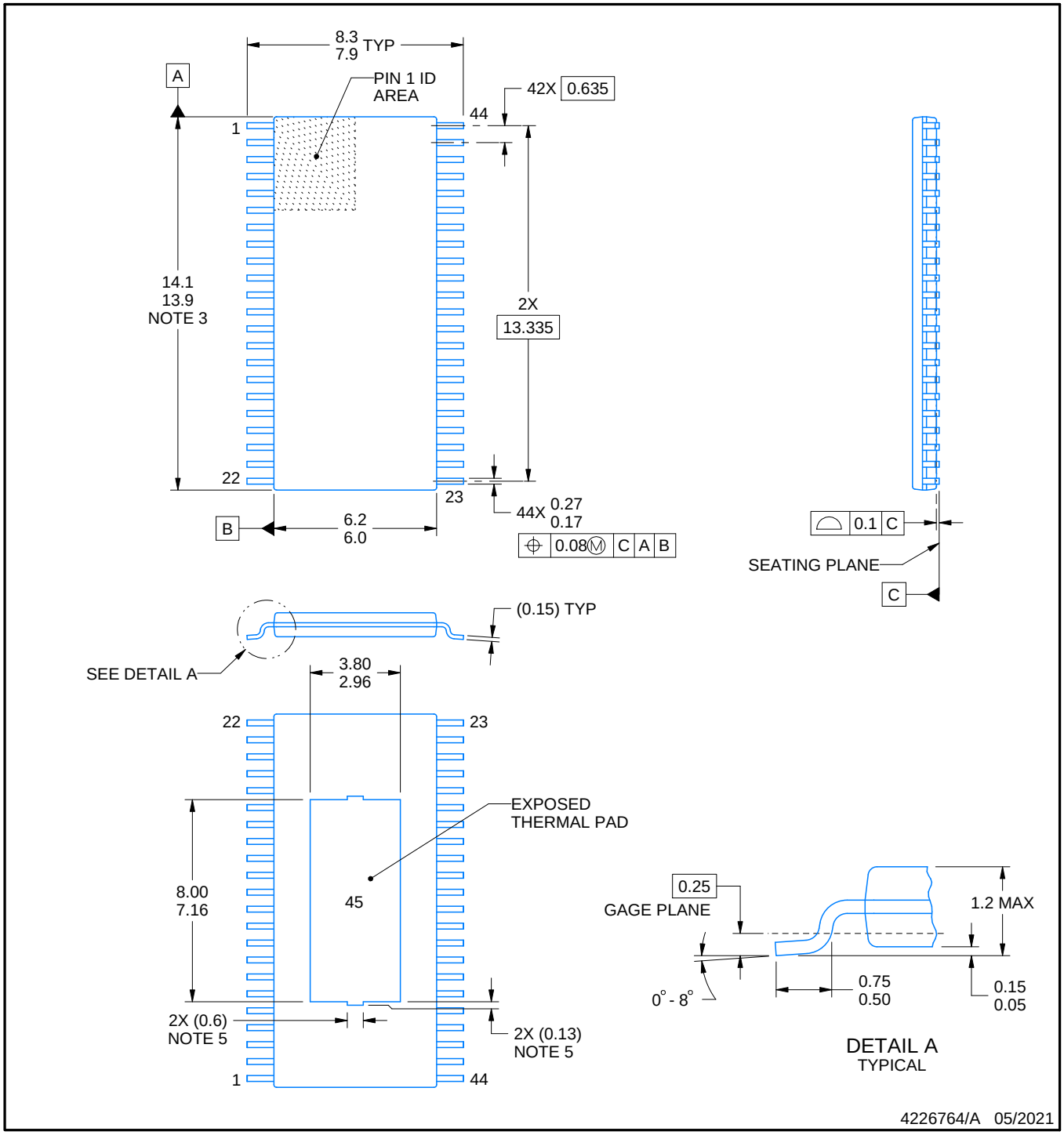


PACKAGE OUTLINE

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

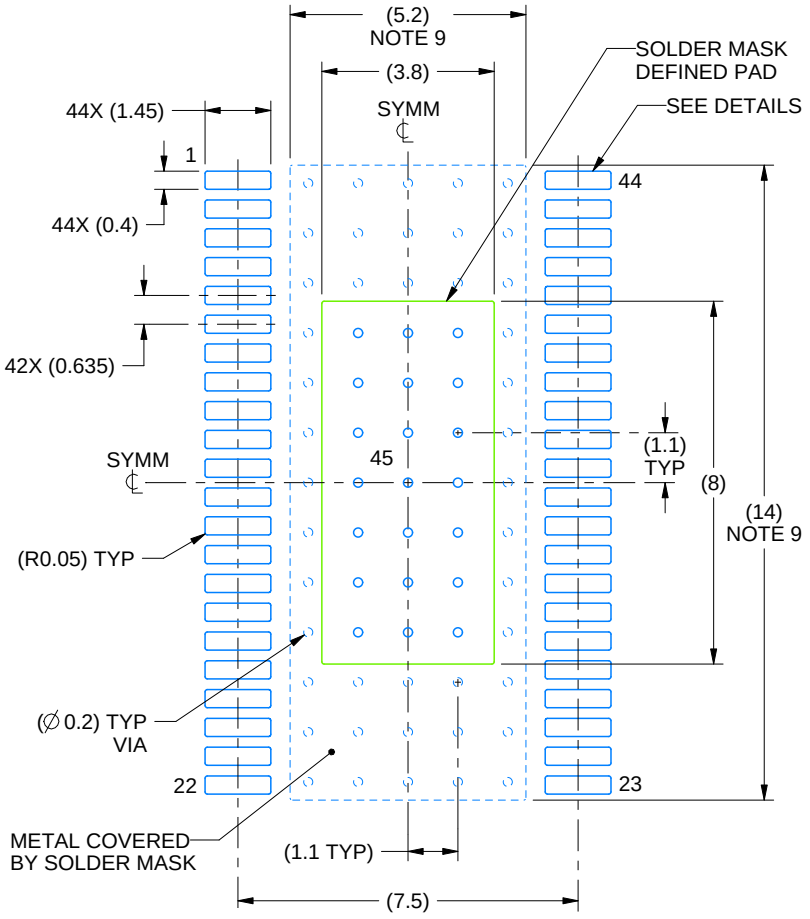
PLASTIC SMALL OUTLINE



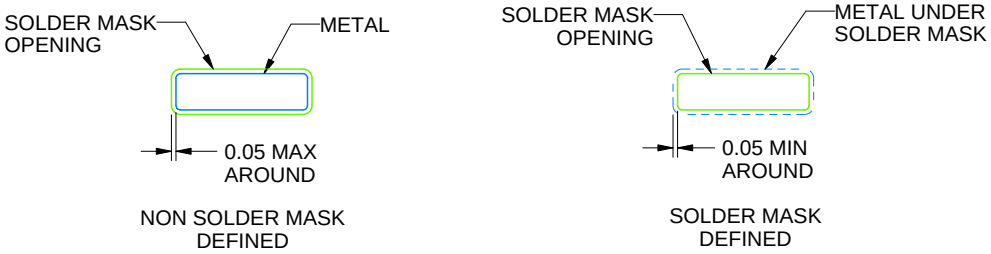
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

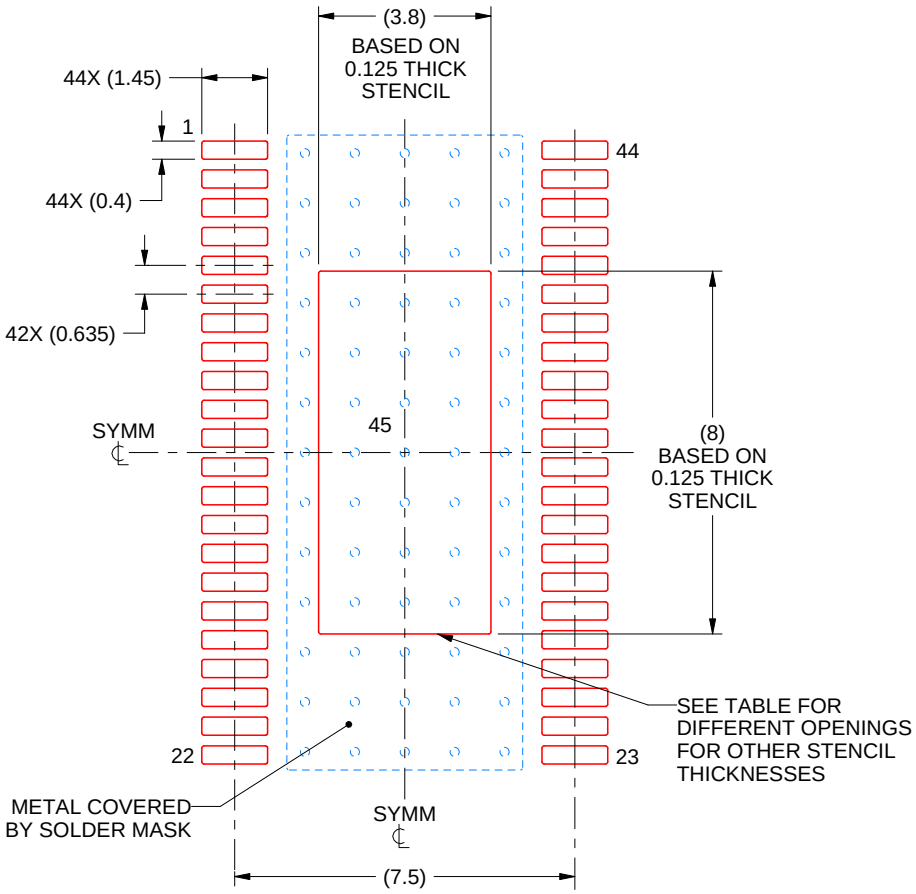


SOLDER MASK DETAILS
NOT TO SCALE

4226764/A 05/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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