







SLVSAB7E - MAY 2010 - REVISED MARCH 2023

DRV8840

DRV8840 DC Motor Driver IC

1 Features

- Single H-Bridge Current-Control Motor Driver
- 8.2-V to 45-V Operating Supply Voltage Range
- Five Bit Current Control Allows up to 32 Current Levels
- Low MOSFET $R_{DS(on)}$ Typical 0.4 Ω (HS + LS)
- 5-A Maximum Drive Current at 24 V, T_A = 25°C
- Built-In 3.3-V Reference Output
- Parallel Digital Control Interface
- Thermal Enhanced Surface Mount Package
- Protection Features:
 - Overcurrent Protection (OCP)
 - Thermal Shutdown (TSD)
 - VM Undervoltage Lockout (UVLO)
 - Fault Condition Indication Pin (nFAULT)

2 Applications

- **Printers**
- Scanners
- Office Automation Machines
- **Gaming Machines**
- **Factory Automation**
- Robotics

3 Description

The DRV8840 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has one H-bridge driver, and is intended to drive one DC motor. The output driver block for each consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings. The DRV8840 can supply up to 5-A peak or 3.5-A output current (with proper heatsinking at 24 V and 25°C).

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable to allow braking or coasting of the motor when disabled.

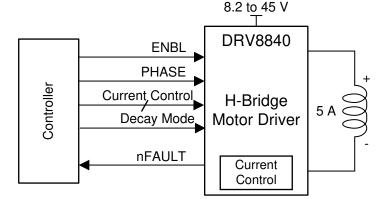
Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

The DRV8840 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)	
DRV8840	HTSSOP (28)	9.70 mm × 4.40 mm	

For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Schematic



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4 Revision History NOTE: Page numbers for previous revisions may diff		Domo
Changes from Revision D (December 2015) to Re		Page
Typo corrections		1
Changes from Revision C (August 2013) to Revis	sion D (December 2015)	Page
Added Pin Configuration and Functions section, E Functional Modes, Application and Implementatio section, Device and Documentation Support secti section	on section, Power Supply Recommendations se ion, and Mechanical, Packaging, and Orderable	ection, <i>Layout</i> e <i>Information</i> 1
 Updated Features bullets 		1

Added MIN value for ISENSEx row from -0.3 V to -0.8 V5



5 Pin Configuration and Functions

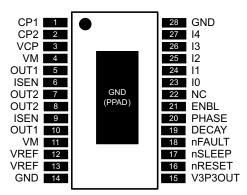


Figure 5-1. PWP Package 28-Pin HTSSOP Top View

Table 5-1. Pin Functions

P	IN	I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS	
NAME NO.		1/0(1/	DESCRIPTION	OR CONNECTIONS	
POWER AND	GROUND	1		,	
GND	14, 28	_	Device ground		
VM	4, 11	_	Bridge A power supply	Connect to motor supply (8.2 - 45 V). Both pins must be connected to same supply.	
V3P3OUT	15	0	3.3-V regulator output	Bypass to GND with a 0.47-µF, 6.3-V ceramic capacitor. Can be used to supply VREF.	
CP1	1	Ю	Charge pump flying capacitor	Connect a 0.01-µF 50-V capacitor between	
CP2	2	Ю	Charge pump flying capacitor	CP1 and CP2.	
VCP	3	Ю	High-side gate drive voltage	Connect a 0.1-μF 16-V ceramic capacitor and a 1-MΩ resistor to VM.	
CONTROL					
PHASE	20	I	Bridge phase (direction)	Logic high sets OUT1 high, OUT2 low. Internal pulldown.	
ENBL	21	I	Bridge enable	Logic high to enable H-bridge. Internal pulldown.	
10	23	I			
l1	24	ı			
12	25	ı	Current set inputs	Sets winding current as a percentage of full- scale. Internal pulldown.	
13	26	I		μ	
14	27	I			
DECAY	19	I	Decay (brake) mode	Low = brake (slow decay), high = coast (fast decay). Internal pulldown and pullup.	
nRESET	16	I	Reset input	Active-low reset input initializes the logic and disables the H-bridge outputs. Internal pulldown.	
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to ente low-power sleep mode. Internal pulldown.	
VREF	12,13	I	Current set reference input	Reference voltage for winding current set. Both pins must be connected together on the PCB.	



Table 5-1. Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS	
NAME	NAME NO.		DESCRIPTION	OR CONNECTIONS	
STATUS					
nFAULT 18 OD			Fault	Logic low when in fault condition (overtemperature, overcurrent)	
OUTPUT					
ISEN	6, 9	Ю	Bridge ground / Isense	Connect to current sense resistor. Both pins must be connected together on the PCB.	
OUT1	5, 10	0	Bridge output 1	Connect to motor winding. Both pins must be connected together on the PCB.	
OUT2	7, 8	0	Bridge output 2	Connect to motor winding. Both pins must be connected together on the PCB.	

⁽¹⁾ Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VMx	Power supply voltage	-0.3	47	V
	Digital pin voltage	-0.5	7	V
VREF	Input voltage	-0.3	4	V
	ISENSEx pin voltage ⁽³⁾	-0.8	0.8	V
	Peak motor drive output current, t < 1 μS	Internall	Internally limited	
	Continuous motor drive output current ⁽⁴⁾	0	5	А
	Continuous total power dissipation	See Se	ction 6.4	
TJ	Operating virtual junction temperature	-40	150	°C
T _A	Operating ambient temperature	-40	85	°C
T _{stg}	Storage temperature	-60	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 6.3 is not implied. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

- (2) All voltage values are with respect to network ground pin.
- Transients of ±1 V for less than 25 ns are acceptable.
- (4) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	V

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _M	Motor power supply voltage ⁽¹⁾	8.2	45	V
V _{REF}	VREF input voltage ⁽²⁾	1	3.5	V
I _{V3P3}	V3P3OUT load current	0	1	mA
f _{PWM}	Externally applied PWM frequency	0	100	kHz

- (1) All V_M pins must be connected to the same supply voltage.
- (2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.

6.4 Thermal Information

		DRV8840	
	THERMAL METRIC ⁽¹⁾	PWP (HTSSOP)	UNIT
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.2	°C/W
ΨЈВ	Junction-to-board characterization parameter	5.5	°C/W



		DRV8840	
	THERMAL METRIC ⁽¹⁾	PWP (HTSSOP)	UNIT
		28 PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	1.4	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

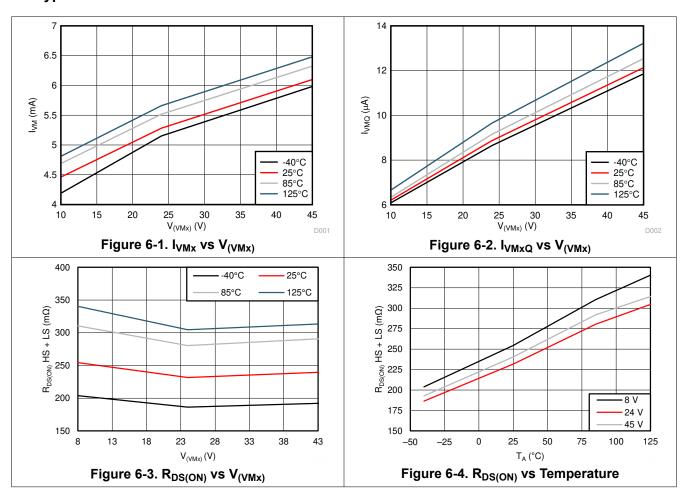
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER	SUPPLIES					
I _{VM}	VM operating supply current	V _M = 24 V, f _{PWM} < 50 kHz		5	8	mA
I _{VMQ}	VM sleep mode supply current	V _M = 24 V		10	20	μA
V _{UVLO}	VM undervoltage lockout voltage	V _M rising		7.8	8.2	V
	T REGULATOR					
V _{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.2	3.3	3.4	V
	EVEL INPUTS					
V _{IL}	Input low voltage			0.6	0.7	V
V _{IH}	Input high voltage		2.2		5.25	V
V _{HYS}	Input hysteresis		0.3	0.45	0.6	V
I _{IL}	Input low current	VIN = 0	-20		20	μA
I _{IH}	Input high current	VIN = 3.3 V		33	100	μA
R _{PD}	Internal pulldown resistance			100		kΩ
nFAULT	OUTPUT (OPEN-DRAIN OUTPUT)					
V _{OL}	Output low voltage	I _O = 5 mA			0.5	V
I _{OH}	Output high leakage current	V _O = 3.3 V			1	μA
DECAY I	NPUT					
V _{IL}	Input low threshold voltage	For slow decay (brake) mode	0		0.8	V
V _{IH}	Input high threshold voltage	For fast decay (coast) mode	2			V
I _{IN}	Input current				±40	μA
R _{PU}	Internal pullup resistance			130		kΩ
R _{PD}	Internal pulldown resistance			80		kΩ
	 GE FETS					
	HS FET on resistance	V _M = 24 V, I _O = 1 A, T _J = 25°C		0.1		
R _{DS(ON)}		V _M = 24 V, I _O = 1 A, T _J = 85°C		0.13	0.16	Ω
	LS FET on resistance	V _M = 24 V, I _O = 1 A, T _J = 25°C		0.1		
R _{DS(ON)}		V _M = 24 V, I _O = 1 A, T _J = 85°C		0.13	0.16	Ω
I _{OFF}	Off-state leakage current		-40		40	μΑ
	DRIVER					F** *
	Internal current control PWM					
f _{PWM}	frequency			50		kHz
t _{BLANK}	Current sense blanking time			3.75		μs
t _R	Rise time		30		200	ns
t _F	Fall time		30		200	ns
PROTEC	CTION CIRCUITS					
I _{OCP}	Overcurrent protection trip level		6			Α
t _{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRE	NT CONTROL	,				
I _{REF}	VREF input current	VREF = 3.3 V	-3		3	μA
V _{TRIP}	ISENSE trip voltage	VREF = 3.3 V, 100% current setting	635	660	685	mV
	Current trip accuracy	VREF = 3.3 V, 5% current setting	-25%		25%	
	(relative to programmed value)	VREF = 3.3 V, 10% - 34% current setting	-15%		15%	
ΔI_{TRIP}		VREF = 3.3 V, 38% - 67% current setting	-10%		10%	
		VREF = 3.3 V, 71% - 100% current setting	-5%		5%	



over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
A _{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

6.6 Typical Characteristics





7 Detailed Description

7.1 Overview

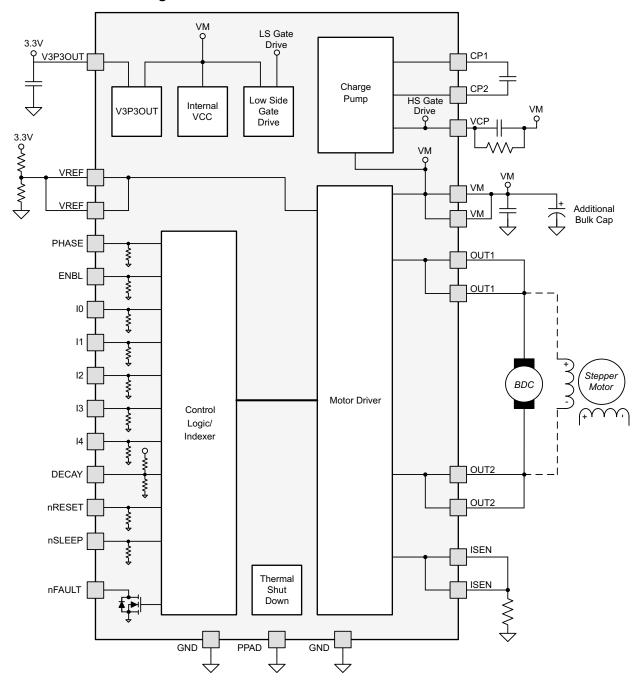
The DRV8840 is an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device integrates a single NMOS H-bridge, charge pump, current sense, current regulation, and device protection circuitry. The DRV8828 can be powered from a single voltage supply from 8.2 V to 45 V, and is capable of providing a continuous output current up to 5 A.

A simple PHASE/ENBL interface allows for easy interfacing to an external controller. A 5 bit current control scheme allows for up to 32 discrete current levels. The current regulation method is adjustable between slow and fast decay.

Integrated protection circuits allows the device to monitor and protect against overcurrent, undervoltage, and overtemperature faults which are all reported through a fault indication pin (nFAULT). A low power sleep mode is integrated which allows the system to lower power consumption when not driving the motor.



7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Driver

The DRV8840 device contains one H-bridge motor driver with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 7-1.

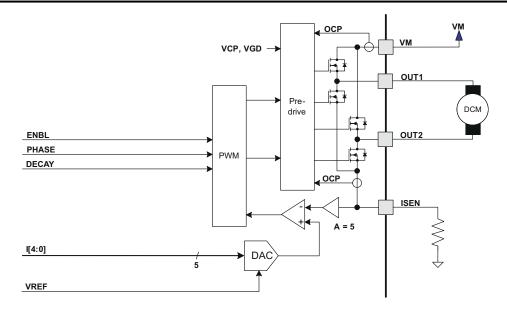


Figure 7-1. Motor Control Circuitry

There are multiple VM, ISEN, OUT, and VREF pins. All like-named pins must be connected together on the PCB.

7.3.2 Bridge Control

The PHASE input pin controls the direction of current flow through the H-bridge, and hence the direction of rotation of a DC motor. The ENBL input pin enables the H-bridge outputs when active high, and can also be used for PWM speed control of the motor. Note that the state of the DECAY pin selects the behavior of the bridge when ENBL = 0, allowing the selection of slow decay (brake) or fast decay (coast). Table 7-1 shows the logic.

	Table 7-1. 11-bridge Logic						
DECAY	ENBL	PHASE	OUT1	OUT2			
0	0	Х	L	L			
1	0	Х	Z	Z			
Х	1	1	Н	L			
Х	1	0	L	Н			

Table 7-1. H-Bridge Logic

The control inputs have internal pulldown resistors of approximately 100 k Ω .

7.3.3 Current Regulation

The maximum current through the motor winding is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For DC motors, current regulation is used to limit the start-up and stall current of the motor. Speed control is typically performed by providing an external PWM signal to the ENBLx input pins.

If the current regulation feature is not needed, it can be disabled by connecting the ISENSE pins directly to ground and the VREF pins to V3P3.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the ISEN pin, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the VREF pin, and is scaled by a 5-bit DAC that allows current settings of zero to 100% in an approximately sinusoidal sequence.

The full-scale (100%) chopping current is calculated in Equation 1.



$$I_{CHOP} = \frac{V_{REFX}}{5 \times R_{ISENSE}}$$
 (1)

Example:

If a 0.25- Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current will be 2.5 V / $(5 \times 0.25 \Omega)$ = 2 A.

Five input pins (I0 - I4) are used to scale the current in the bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The I0 - I4 pins have internal pulldown resistors of approximately 100 k Ω . The function of the pins is shown in Table 7-2.

Table 7-2. Pin Functions

I[40] RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)	Table 7-2. Pin Functions								
0x01h 5% 0x02h 10% 0x03h 15% 0x04h 20% 0x05h 24% 0x06h 29% 0x07h 34% 0x08h 38% 0x09h 43% 0x0Ah 47% 0x0Bh 51% 0x0Ch 56% 0x0Dh 60% 0x0Eh 63% 0x0Fh 67% 0x10h 71% 0x11h 74% 0x12h 77% 0x13h 80% 0x14h 83% 0x15h 86% 0x17h 90% 0x18h 92% 0x19h 94% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	I[40]	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)							
0x02h 10% 0x03h 15% 0x04h 20% 0x05h 24% 0x06h 29% 0x07h 34% 0x08h 38% 0x09h 43% 0x0Ah 47% 0x0Bh 51% 0x0Ch 56% 0x0Dh 60% 0x0Eh 63% 0x0Fh 67% 0x10h 71% 0x11h 74% 0x12h 77% 0x13h 80% 0x14h 83% 0x16h 88% 0x17h 90% 0x18h 92% 0x19h 94% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x00h	0%							
0x03h 15% 0x04h 20% 0x05h 24% 0x06h 29% 0x07h 34% 0x08h 38% 0x09h 43% 0x0Ah 47% 0x0Bh 51% 0x0Ch 56% 0x0Dh 60% 0x0Eh 63% 0x0Fh 67% 0x10h 71% 0x11h 74% 0x12h 77% 0x13h 80% 0x14h 83% 0x15h 86% 0x17h 90% 0x18h 92% 0x19h 94% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x01h	5%							
0x04h 20% 0x05h 24% 0x06h 29% 0x07h 34% 0x08h 38% 0x09h 43% 0x0Ah 47% 0x0Bh 51% 0x0Ch 56% 0x0Dh 60% 0x0Eh 63% 0x0Fh 67% 0x10h 71% 0x11h 74% 0x12h 77% 0x13h 80% 0x14h 83% 0x15h 86% 0x17h 90% 0x18h 92% 0x19h 94% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x02h	10%							
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0x07h 34% 0x08h 38% 0x09h 43% 0x0Ah 47% 0x0Bh 51% 0x0Ch 56% 0x0Dh 60% 0x0Eh 63% 0x0Fh 67% 0x10h 71% 0x11h 74% 0x12h 77% 0x13h 80% 0x14h 83% 0x15h 86% 0x16h 88% 0x17h 90% 0x18h 92% 0x1Ah 96% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x05h	24%							
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0x15h 86% 0x16h 88% 0x17h 90% 0x18h 92% 0x19h 94% 0x1Ah 96% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x13h	80%							
0x16h 88% 0x17h 90% 0x18h 92% 0x19h 94% 0x1Ah 96% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x14h	83%							
0x17h 90% 0x18h 92% 0x19h 94% 0x1Ah 96% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x15h	86%							
0x18h 92% 0x19h 94% 0x1Ah 96% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x16h	88%							
0x19h 94% 0x1Ah 96% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x17h	90%							
0x1Ah 96% 0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x18h	92%							
0x1Bh 97% 0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x19h	94%							
0x1Ch 98% 0x1Dh 99% 0x1Eh 100%	0x1Ah	96%							
0x1Dh 99% 0x1Eh 100%	0x1Bh	97%							
0x1Eh 100%	0x1Ch	98%							
	0x1Dh	99%							
0x1Fh 100%	0x1Eh	100%							
	0x1Fh	100%							

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7.3.4 Decay Mode and Braking

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-2 as case 1. The current flow direction shown indicates the state when the xENBL pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 7-2 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7-2 as case 3.

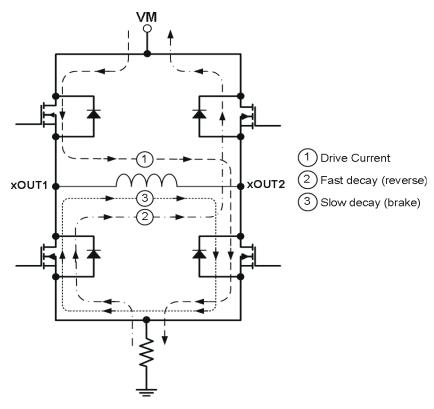


Figure 7-2. Decay Mode

The DRV8840 device supports fast decay and slow decay mode. Slow or fast decay mode is selected by the state of the DECAY pin - logic low selects slow decay, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 k Ω and an internal pulldown resistor of approximately 80 k Ω . This sets the mixed decay mode if the pin is left open or undriven.

DECAY mode also affects the operation of the bridge when it is disabled (by taking the ENBL pin inactive). This applies if the ENABLE input is being used for PWM speed control of the motor, or if it is simply being used to start and stop motor rotation.

If the DECAY pin is high (fast decay), when the bridge is disabled fast decay mode will be entered until the current through the bridge reaches zero. Once the current is at zero, the bridge is disabled to prevent the motor from reversing direction. This allows the motor to coast to a stop.

If the DECAY pin is low (slow decay), both low-side FETs will be turned on when ENBL is made inactive. This essentially shorts out the back EMF of the motor, causing the motor to brake, and stop quickly. The low-side FETs will stay in the ON state even after the current reaches zero.



7.3.5 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at $3.75 \,\mu s$. Note that the blanking time also sets the minimum on time of the PWM.

7.3.6 Protection Circuits

The DRV8840 device is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.6.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

7.3.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

7.3.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when $V_{\rm M}$ rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge driver. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. Note that nRESET and nSLEEP have internal pulldown resistors of approximately 100 k Ω . These signals need to be driven to logic high for device operation.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8840 device is used in brushed motor or stepper motor control. The onboard current regulation allows for limiting the motor current through simple pin configurations.

8.2 Typical Application

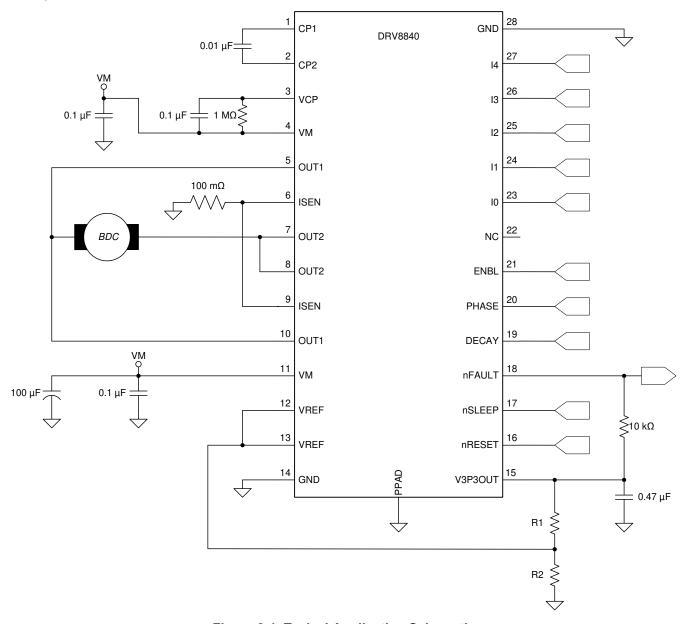


Figure 8-1. Typical Application Schematic



8.2.1 Design Requirements

Table 8-1 shows the design parameters for this application.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	VM	24 V
Motor Winding Resistance	RM	3.9 V
Motor Winding Inductance	LM	2.9 mH
Target Chopping Current	ITRIP	1.5 A
Sense Resistor	RSENSE	100 mΩ
VREF Voltage	VREF	0.75 V

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

The maximum current (I_{TRIP}) is set by the Ix pins, the VREF analog voltage, and the sense resistor value (R_{SENSE}). When starting a brushed DC motor, a large inrush current may occur because there is no back-EMF and high detent torque. Current regulation will act to limit this inrush current and prevent high current on start-up.

$$I_{TRIP} / (5 \times R_{SENSE})$$
 (2)

Example: If the desired chopping current is 1.5 A:

- Set RSENSE = 100 mΩ
- VREF would have to be 0.75 V
- Create a resistor divider network from V3P3OUT (3.3 V) to set VREF = 0.75 V
- Set R2 = 10 kΩ and set R1 = 3 kΩ

8.2.2.2 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- · Low inductance
- · Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $Irms^2 \times R$. For example, if the RMS motor current is 1.5 A and a 200-m Ω sense resistor is used, the resistor will dissipate 1.5 A² × 0.2 Ω = 0.3 W. The power quickly increases with greater current levels.

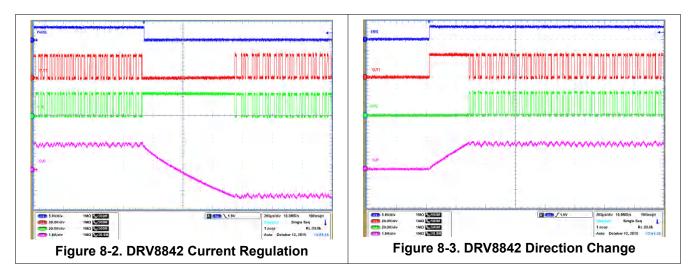
Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

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8.2.3 Application Curves





9 Power Supply Recommendations

The DRV8840 is designed to operate from an input voltage supply (VM) range from 8.2 V to 45 V. The device has an absolute maximum rating of 47 V. A 0.1-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8840 as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be greater than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

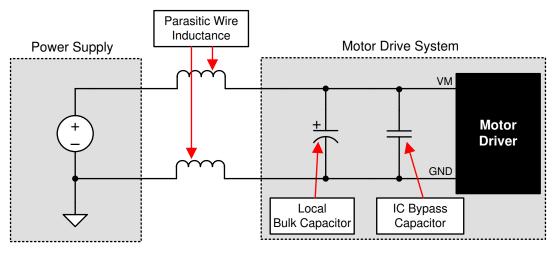


Figure 9-1. Setup of Motor Drive System With External Power Supply

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10 Layout

10.1 Layout Guidelines

Each VM terminal must be bypassed to GND using a low-ESR ceramic bypass capacitors with recommended values of $0.1~\mu F$ rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.1 μ F rated for VM . Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.47 μ F rated for 16 V. Place this component as close to the pins as possible. In addition, place a 1 M Ω between VM and VCP.

Bypass V3P3OUT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

The current sense resistor should be placed as close as possible to the device pins to minimize trace inductance between the pin and resistor.

10.2 Layout Example

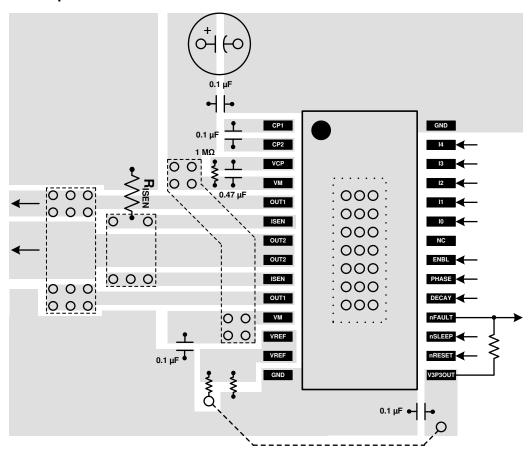


Figure 10-1. Example Layout

10.3 Thermal Considerations

The DRV8840 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.



Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Average power dissipation in the DRV8840 when running a DC motor can be roughly estimated by: Equation 3.

$$P = 2 \times R_{DS(ON)} \times (I_{OUT})^2$$
(3)

where

- · P is the power dissipation of one H-bridge
- R_{DS(ON)} is the resistance of each FET
- I_{OUT} is the RMS output current being applied to each winding.

 I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multilayer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and the TI application brief, *PowerPAD™ Made Easy* (SLMA004), available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- PowerPAD™ Thermally Enhanced Package, SLMA002
- PowerPAD™ Made Easy, SLMA004

11.2 Community Resources

11.3 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14-Jul-2025 www.ti.com

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
DRV8840PWP	Obsolete	Production	HTSSOP (PWP) 28	-	-	Call TI	Call TI	-40 to 85	DRV8840
DRV8840PWPR	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8840
DRV8840PWPR.A	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8840
DRV8840PWPR.B	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8840
DRV8840PWPRG4	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8840
DRV8840PWPRG4.A	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8840
DRV8840PWPRG4.B	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8840

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

	Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	DRV8840PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
L	DRV8840PWPRG4	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8840PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
DRV8840PWPRG4	HTSSOP	PWP	28	2000	350.0	350.0	43.0

4.4 x 9.7, 0.65 mm pitch

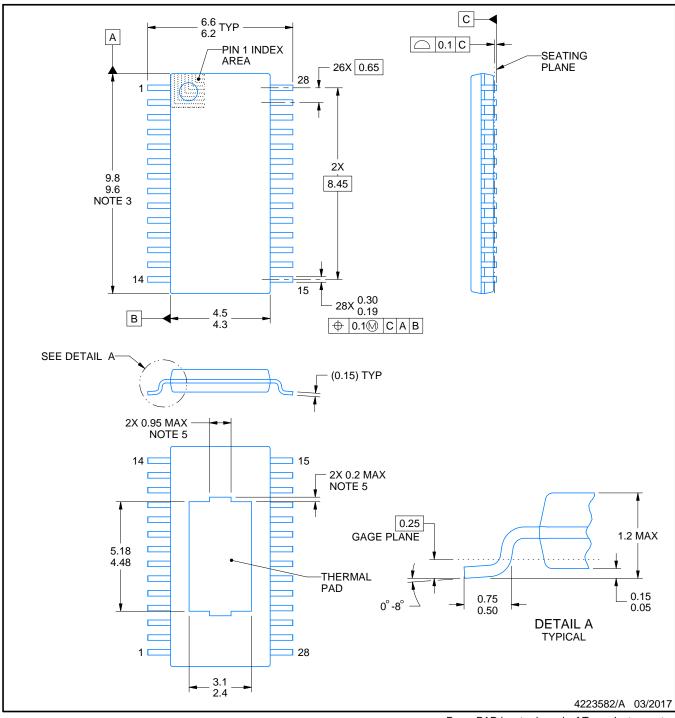
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



PowerPAD[™] TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

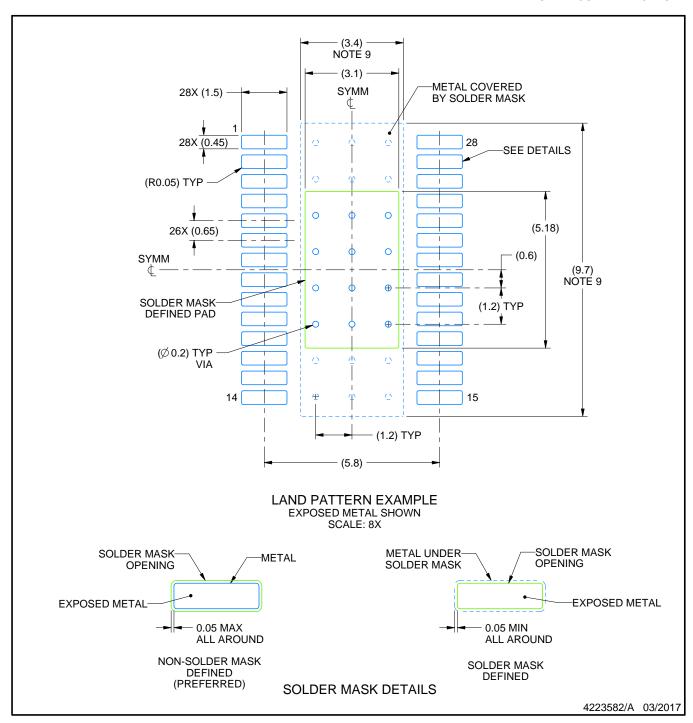
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.
- 5. Features may differ or may not be present.



SMALL OUTLINE PACKAGE

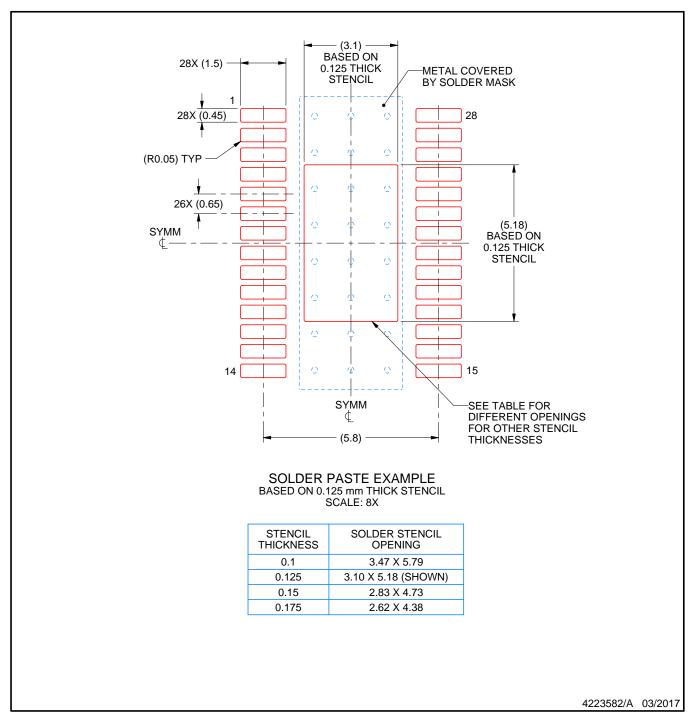


NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



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