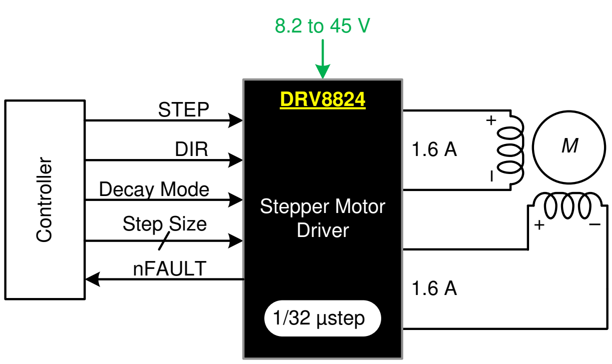
DRV8824 Stepper Motor Controller IC

1 Features

- PWM Microstepping Stepper Motor Driver
  - Built-In Microstepping Indexer
  - Up to 1/32 Microstepping
- Multiple Decay Modes:
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- 8.2-V to 45-V Operating Supply Voltage Range
- 1.6-A Maximum Drive Current at 24 V and T_A = 25°C
- Simple STEP/DIR Interface
- Low-Current Sleep Mode
- Built-In 3.3-V Reference Output
- Small Package and Footprint
- Protection Features:
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VMx Undervoltage Lockout (UVLO)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Automatic Teller Machines
- Money Handling Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics



Simplified Schematic

3 Description

The DRV8824 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers and a microstepping indexer, and is intended to drive a bipolar stepper motor. The output driver block consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings. The DRV8824 is capable of driving up to 1.6 A of current from each output (with proper heatsinking, at 24 V and 25°C).

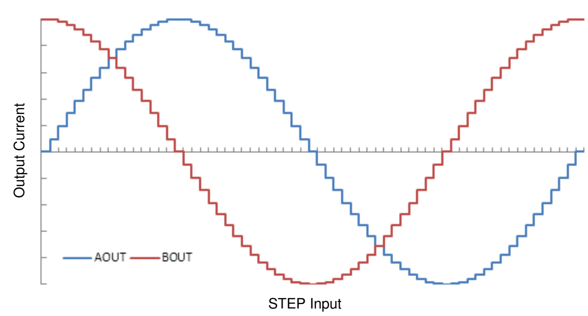
A simple STEP/DIR interface allows easy interfacing to controller circuits. Mode pins allow for configuration of the motor in full-step up to 1/32-step modes. Decay mode is configurable so that slow decay, fast decay, or mixed decay can be used. A low-power sleep mode is provided which shuts down internal circuitry to achieve very-low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

Internal shutdown functions are provided for overcurrent, short circuit, undervoltage lockout, and over temperature. Fault conditions are indicated through the nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8824	HTSSOP (28)	9.70 mm × 6.40 mm
	VQFN (28)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Microstepping Current Waveform

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (July 2014) to Revision K (January 2022) **Page**

- Updated RHD pinout 3
- Added additional external component to connect to the VCP pin 3
- Updated the *Handling Ratings* table to and *ESD Ratings* table and moved T_{stg} to the *Absolute Maximum Ratings* table.....5
- Corrected device part number 19
- Added *Section 10.1* 24

Changes from Revision I (June 2014) to Revision J (July 2014) **Page**

- Updated images on the front page 1
- Update the continuous motor drive output current value in *Absolute Maximum Ratings* 5
- Updated typical t_{DEG} time 6
- Updated text and equations in *Section 8.2.2* 19
- Updated *Section 9.1* and image.....21
- *Layout Example* image updated. 22

Changes from Revision H (December 2013) to Revision I (June 2014) **Page**

- Updated data sheet to new TI standard: added sections and rearranged material 1
- Updated pin description for AVREF and BVREF 3
- Added power supply ramp rate to *Absolute Maximum Ratings* 5
- Added minimum voltage for V_{IL} and removed typical.....6
- Updated parameter descriptions in *Timing Requirements* and t_{WAKE} minimum and maximum 7

Changes from Revision G (August 2013) to Revision H (December 2013) **Page**

- Changed in Electrical Characteristics table, section DECAY INPUT third row.....6

5 Pin Configuration and Functions

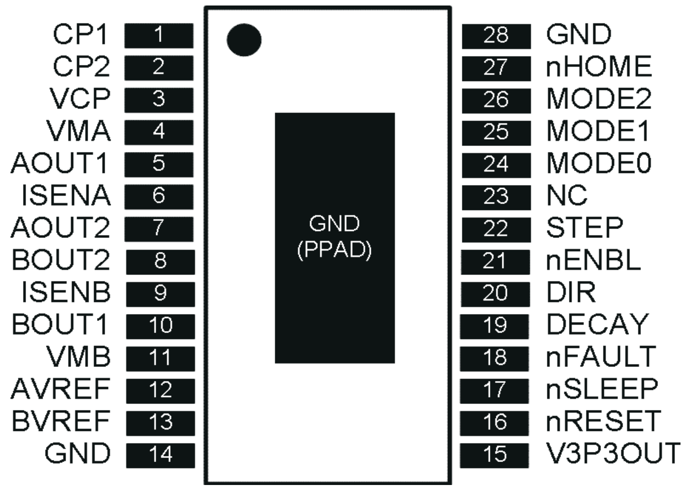


Figure 5-1. PWP Package 28-Pin HTSSOP Top View

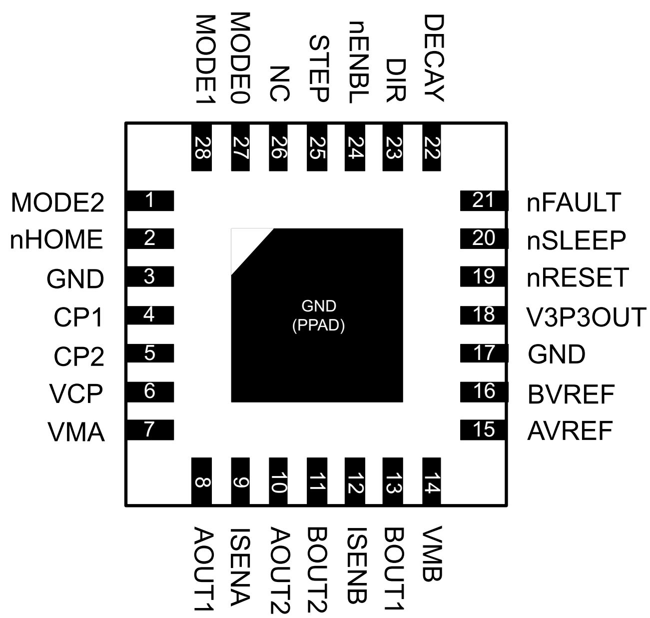


Figure 5-2. RHD Package 28-Pin VQFN Top View

Table 5-1. Pin Functions

PIN			I/O[(1)]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	PWP	RHD			
POWER AND GROUND					
GND	14, 28	3, 17	—	Device ground	
VMA	4	7	—	Bridge A power supply	Connect to motor supply (8.2 to 45 V). Both pins must be connected to same supply, bypassed with a 0.1-µF capacitor to GND, and connected to appropriate bulk capacitance.
VMB	11	14	—	Bridge B power supply	
V3P3OUT	15	18	O	3.3-V regulator output	Bypass to GND with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	4	IO	Charge pump flying capacitor	Connect a 0.01-µF 50-V capacitor between CP1 and CP2.
CP2	2	5	IO	Charge pump flying capacitor	

Table 5-1. Pin Functions (continued)

PIN			I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	PWP	RHD			
VCP	3	6	IO	High-side gate drive voltage	Connect a 0.1-μF 16-V ceramic capacitor. A 1-MΩ resistor can be connected to VM to accelerate discharge of the VCP capacitor.
CONTROL					
nENBL	21	24	I	Enable input	Logic high to disable device outputs and indexer operation, logic low to enable. Internal pulldown.
nSLEEP	17	20	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
STEP	22	25	I	Step input	Rising edge causes the indexer to move one step. Internal pulldown.
DIR	20	23	I	Direction input	Level sets the direction of stepping. Internal pulldown.
MODE0	24	27	I	Microstep mode 0	MODE0 through MODE2 set the step mode: full, 1/2, 1/4, 1/8/ 1/16, or 1/32 step. Internal pulldown.
MODE1	25	28	I	Microstep mode 1	
MODE2	26	1	I	Microstep mode 2	
DECAY	19	22	I	Decay mode	Low = slow decay, Open = mixed decay, High = fast decay. Internal pulldown and pullup.
nRESET	16	19	I	Reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs. Internal pulldown.
AVREF	12	15	I	Bridge A current set reference input	Reference voltage for winding current set. Normally AVREF and BVREF are connected to the same voltage. Can be connected to V3P3OUT.
BVREF	13	16	I	Bridge B current set reference input	
NC	23	26	—	No connect	Leave this pin unconnected.
STATUS					
nHOME	27	2	OD	Home position	Logic low when at home state of step table
nFAULT	18	21	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT					
ISENA	6	9	IO	Bridge A ground / Isense	Connect to current sense resistor for bridge A.
ISENB	9	12	IO	Bridge B ground / Isense	Connect to current sense resistor for bridge B.
AOUT1	5	8	O	Bridge A output 1	Connect to bipolar stepper motor winding A. Positive current is AOUT1 → AOUT2
AOUT2	7	10	O	Bridge A output 2	
BOUT1	10	13	O	Bridge B output 1	Connect to bipolar stepper motor winding B. Positive current is BOUT1 → BOUT2
BOUT2	8	11	O	Bridge B output 2	

(1) Directions: I = input, O = output, OD = open-drain output, IO = input/output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
$V_{(VMx)}$	Power supply voltage	–0.3	47	V
$V_{(VMx)}$	Power supply ramp rate		1	V/µs
	Digital pin voltage	–0.5	7	V
$V_{(xVREF)}$	Input voltage	–0.3	4	V
	ISENSEx pin voltage(4)	–0.8	0.8	V
	Peak motor drive output current, t <1 µs	Internally limited		A
	Continuous motor drive output current(3)		1.6	A
	Continuous total power dissipation	See Section 6.4		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.
(3) Power dissipation and thermal limits must be observed.
(4) Transients of ±1 V for less than 25 ns are acceptable.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{(VMx)}$	Motor power supply voltage range(1)	8.2		45	V
$V_{(xVREF)}$	VREF input voltage(2)	1		3.5	V
I_{V3P3}	V3P3OUT load current			1	mA

(1) All V_M pins must be connected to the same supply voltage.
(2) Operational at VREF between 0 and 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8824 PWP (HTSSOP) 28 PINS	DRV8824 RHD (VQFN) 28 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	38.9	35.8	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	23.3	25.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	21.2	8.2	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.8	0.3	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	20.9	8.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range of –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMx}	VMx operating supply current	$V_{(VMx)}$ = 24 V, f_{PWM} < 50 kHz		5	8	mA
I_{VMxQ}	VMx sleep mode supply current	$V_{(VMx)}$ = 24 V		10	20	μA
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	I_{OUT} = 0 to 1 mA, $V_{(VMx)}$ = 24 V, T_J = 25°C	3.18	3.30	3.42	V
		I_{OUT} = 0 to 1 mA	3.10	3.30	3.50	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage		0		0.7	V
V_{IH}	Input high voltage		2		5.25	V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	$V_{(VIN)}$ = 0	–20		20	μA
I_{IH}	Input high current	$V_{(VIN)}$ = 3.3 V			100	μA
R_{PD}	Internal pulldown resistance	nENBL, nRESET, DIR, STEP, MODEx		100		kΩ
		nSLEEP		1		MΩ
nHOME, nFAULT OUTPUTS (OPEN-DRAIN OUTPUTS)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	μA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay mode			0.8	V
V_{IH}	Input high threshold voltage	For fast decay mode	2			V
I_{IN}	Input current		–100		100	μA
R_{PU}	Internal pullup resistance			130		kΩ
R_{PD}	Internal pulldown resistance			80		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	$V_{(VMx)}$ = 24 V, I_O = 1 A, T_J = 25°C		0.63		Ω
		$V_{(VMx)}$ = 24 V, I_O = 1 A, T_J = 85°C		0.76	0.90	
$R_{DS(ON)}$	LS FET on resistance	$V_{(VMx)}$ = 24 V, I_O = 1 A, T_J = 25°C		0.65		Ω
		$V_{(VMx)}$ = 24 V, I_O = 1 A, T_J = 85°C		0.78	0.90	
I_{OFF}	Off-state leakage current		–20		20	μA
MOTOR DRIVER						
f_{PWM}	Internal PWM frequency			50		kHz
t_{BLANK}	Current sense blanking time			3.75		μs
t_R	Rise time	$V_{(VMx)}$ = 24 V	100		360	ns
t_F	Fall time	$V_{(VMx)}$ = 24 V	80		250	ns
t_{DEAD}	Dead time			400		ns
PROTECTION CIRCUITS						
V_{UVLO}	VMx undervoltage lockout voltage	$V_{(VMx)}$ rising		7.8	8.2	V
I_{OCP}	Overcurrent protection trip level		1.8		5	A
t_{DEG}	Overcurrent deglitch time			3		μs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	xVREF input current	$V_{(xVREF)}$ = 3.3 V	–3		3	μA
V_{TRIP}	xISENSE trip voltage	$V_{(xVREF)}$ = 3.3 V, 100% current setting	635	660	685	mV

over operating free-air temperature range of –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{TRIP}	Current trip accuracy (relative to programmed value)	$V_{(xVREF)}$ = 3.3 V , 5% current setting	–25%		25%	
		$V_{(xVREF)}$ = 3.3 V , 10% to 34% current setting	–15%		15%	
		$V_{(xVREF)}$ = 3.3 V, 38% to 67% current setting	–10%		10%	
		$V_{(xVREF)}$ = 3.3 V, 71% to 100% current setting	–5%		5%	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

6.6 Timing Requirements

			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		175	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	2.8		μs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	2.8		μs
4	$t_{SU(STEP)}$	Setup time, command before STEP rising	200		ns
5	$t_{H(STEP)}$	Hold time, command after STEP rising	200		ns
6	t_{ENBL}	Enable time, nENBL active to STEP	200		ns
7	t_{WAKE}	Wakeup time, nSLEEP inactive high to STEP input accepted		1	ms

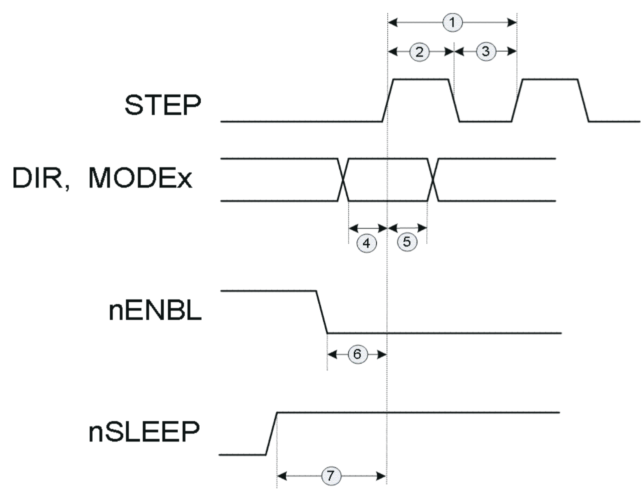


Figure 6-1. Timing Diagram

6.7 Typical Characteristics

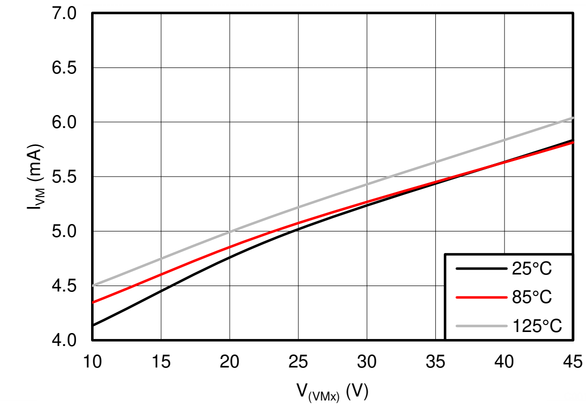


Figure 6-2. I_{VMx} vs $V_{(VMx)}$

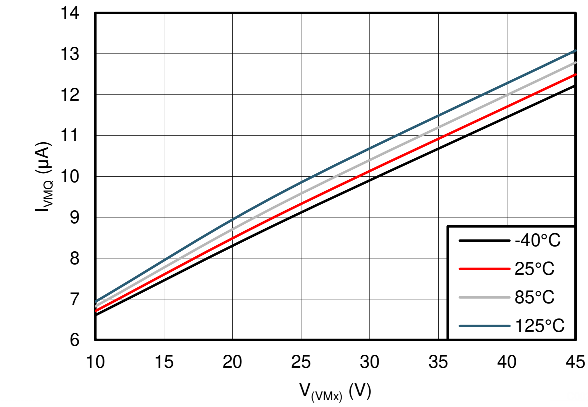


Figure 6-3. I_{VMxQ} vs $V_{(VMx)}$

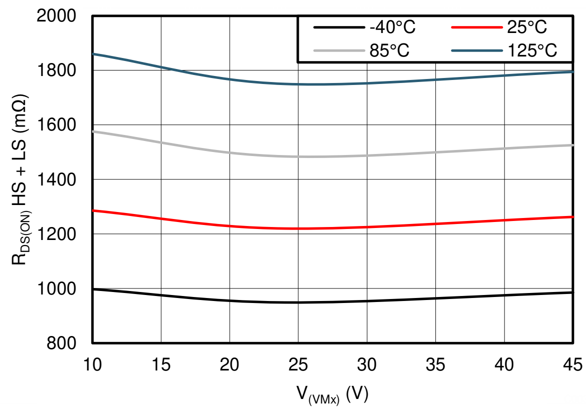


Figure 6-4. $R_{DS(ON)}$ vs $V_{(VMx)}$

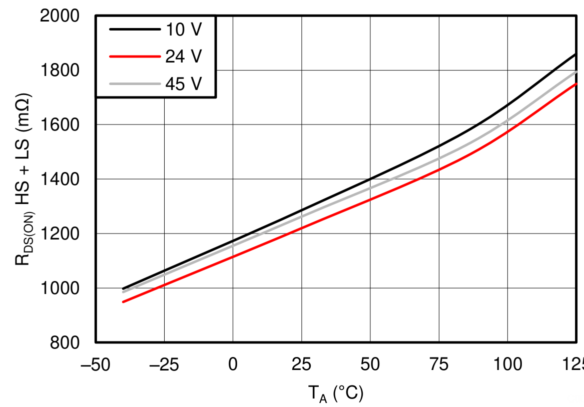


Figure 6-5. $R_{DS(ON)}$ vs Temperature

7 Detailed Description

7.1 Overview

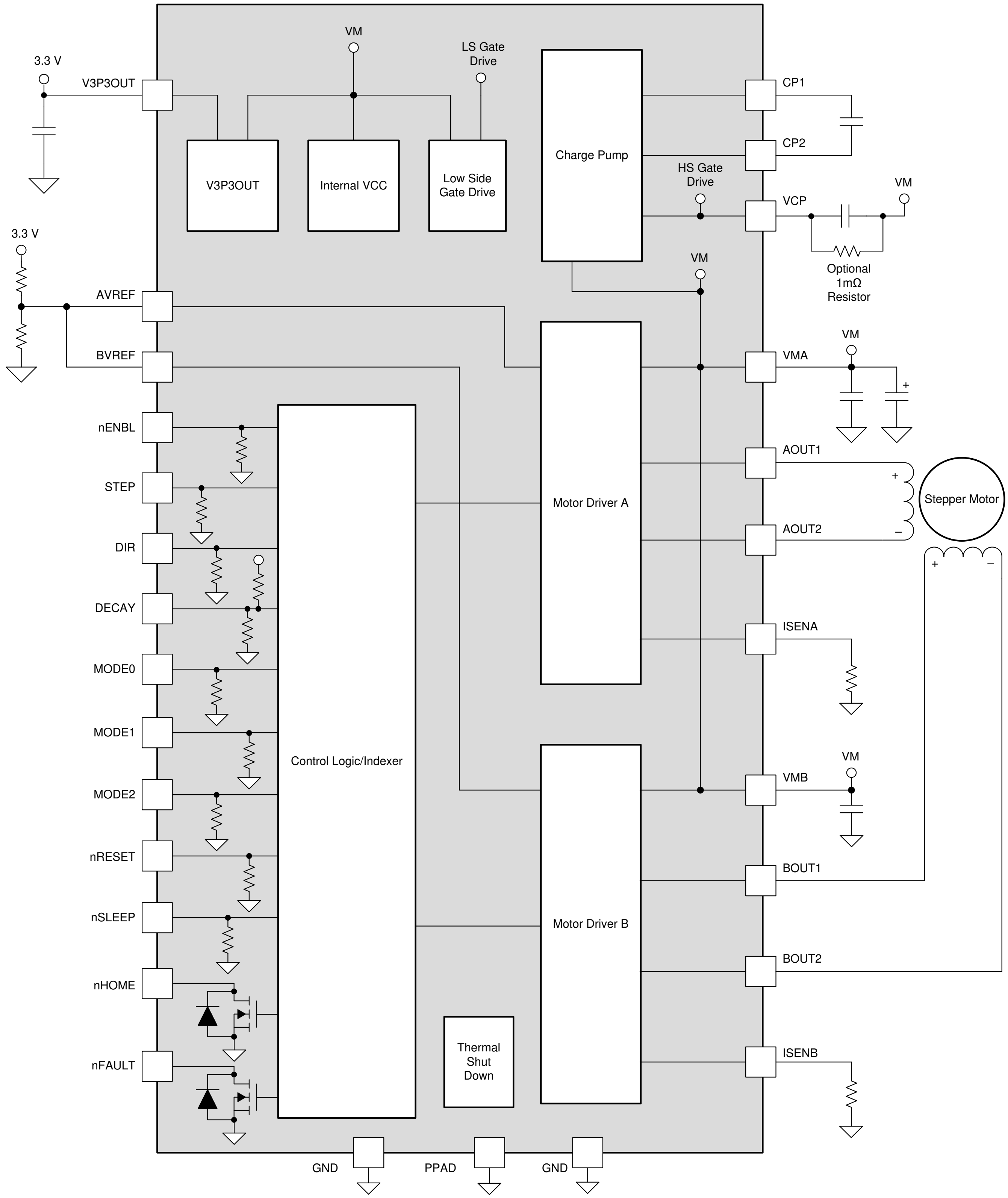
The DRV8824 is an integrated motor driver solution for bipolar stepper motors. The device integrates two NMOS H-bridges, current sense, regulation circuitry, and a microstepping indexer. The DRV8824 can be powered with a supply voltage between 8.2 to 45 V and is capable of providing an output current up to 1.6 A full-scale.

A simple STEP/DIR interface allows for easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level.

The current regulation is highly configurable, with three decay modes of operation. Fast, slow, and mixed decay can be selected depending on the application requirements.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8824 contains two H-bridge motor drivers with current-control PWM circuitry. Figure 7-1 shows a block diagram of the motor control circuitry.

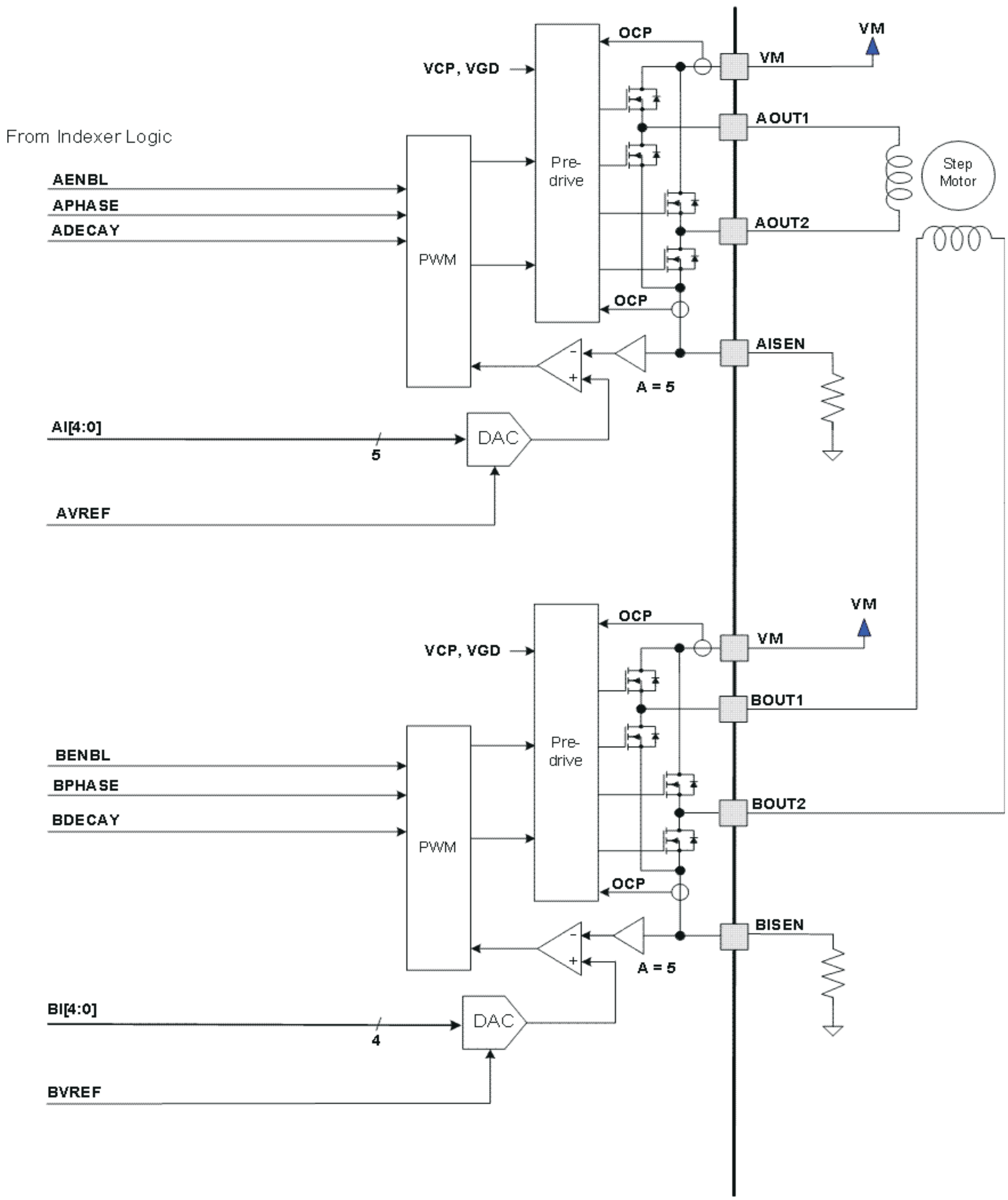


Figure 7-1. Motor Control Circuitry

Note that there are multiple VMx motor power supply pins. All VMx pins must be connected together to the motor supply voltage.

7.3.2 Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. After the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

In stepping motors, current regulation is used to vary the current in the two windings in a semi-sinusoidal fashion to provide smooth motion.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{(xREF)}}{5 \times R_{ISENSE}} \tag{1}$$

Example:

If a 0.5-Ω sense resistor is used and the xVREF pin is 3.3 V, the full-scale (100%) chopping current will be 3.3 V / (5 × 0.5 Ω) = 1.32 A.

The reference voltage is scaled by an internal DAC that allows fractional stepping of a bipolar stepper motor, as described in *Section 7.3.5*.

7.3.3 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. Figure 7-2 shows this as case 1. The current flow direction shown indicates positive current flow.

After the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, after the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches 0, the bridge is disabled to prevent any reverse current flow. Figure 7-2 shows fast decay mode as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. Figure 7-2 shows this as case 3.

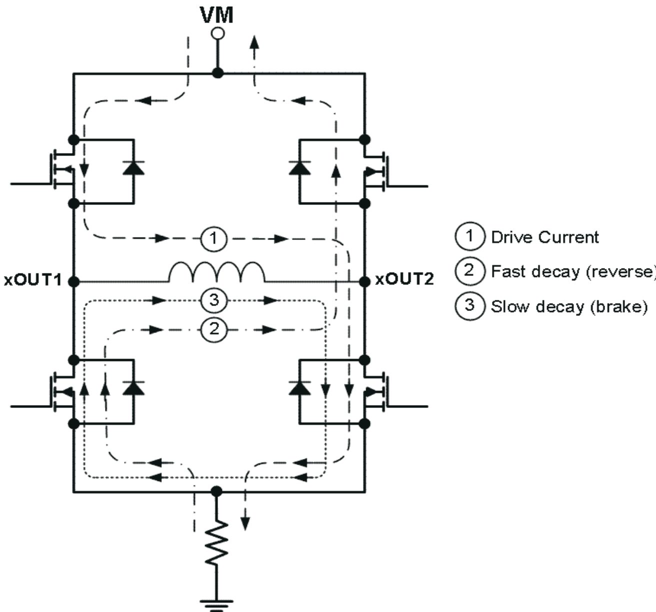


Figure 7-2. Decay Mode

The DRV8824 supports fast decay, slow decay, and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin – logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period. This occurs only if the current through the winding is decreasing (per Table 7-2); if the current is increasing, then slow decay is used.

7.3.4 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

7.3.5 Microstepping Indexer

Built-in indexer logic in the DRV8824 allows a number of different stepping configurations. The MODE0 through MODE2 pins are used to configure the stepping format, as shown in Table 7-1.

Table 7-1. Stepping Format

MODE2	MODE1	MODE0	STEP MODE
0	0	0	Full step (2-phase excitation) with 71% current
0	0	1	1/2 step (1-2 phase excitation)
0	1	0	1/4 step (W1-2 phase excitation)
0	1	1	8 microsteps/step
1	0	0	16 microsteps/step
1	0	1	32 microsteps/step
1	1	0	32 microsteps/step
1	1	1	32 microsteps/step

Table 7-2 shows the relative current and step directions for different settings of MODEx. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high;

if the DIR pin is low, the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that if the step mode is changed while stepping, the indexer advances to the next valid state for the new MODEx setting at the rising edge of STEP.

The home state is 45°. This state is entered at power-up or application of nRESET. This is shown in Table 7-2 by the shaded cells. The logic inputs DIR, STEP, nRESET, and MODEx have an internal pulldown resistors of 100 kΩ

Table 7-2. Relative Current and Step Directions

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
1	1	1	1	1		100%	0%	0
2						100%	5%	3
3	2					100%	10%	6
4						99%	15%	8
5	3	2				98%	20%	11
6						97%	24%	14
7	4					96%	29%	17
8						94%	34%	20
9	5	3	2			92%	38%	23
10						90%	43%	25
11	6					88%	47%	28
12						86%	51%	31
13	7	4				83%	56%	34
14						80%	60%	37
15	8					77%	63%	39
16						74%	67%	42
17	9	5	3	2	1	71%	71%	45
18						67%	74%	48
19	10					63%	77%	51
20						60%	80%	53
21	11	6				56%	83%	56
22						51%	86%	59
23	12					47%	88%	62
24						43%	90%	65
25	13	7	4			38%	92%	68
26						34%	94%	70
27	14					29%	96%	73
28						24%	97%	76
29	15	8				20%	98%	79
30						15%	99%	82
31	16					10%	100%	84
32						5%	100%	87
33	17	9	5	3		0%	100%	90
34						–5%	100%	93
35	18					–10%	100%	96
36						–15%	99%	98
37	19	10				–20%	98%	101

Table 7-2. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
38						–24%	97%	104
39	20					–29%	96%	107
40						–34%	94%	110
41	21	11	6			–38%	92%	113
42						–43%	90%	115
43	22					–47%	88%	118
44						–51%	86%	121
45	23	12				–56%	83%	124
46						–60%	80%	127
47	24					–63%	77%	129
48						–67%	74%	132
49	25	13	7	4	2	–71%	71%	135
50						–74%	67%	138
51	26					–77%	63%	141
52						–80%	60%	143
53	27	14				–83%	56%	146
54						–86%	51%	149
55	28					–88%	47%	152
56						–90%	43%	155
57	29	15	8			–92%	38%	158
58						–94%	34%	160
59	30					–96%	29%	163
60						–97%	24%	166
61	31	16				–98%	20%	169
62						–99%	15%	172
63	32					–100%	10%	174
64						–100%	5%	177
65	33	17	9	5		–100%	0%	180
66						–100%	–5%	183
67	34					–100%	–10%	186
68						–99%	–15%	188
69	35	18				–98%	–20%	191
70						–97%	–24%	194
71	36					–96%	–29%	197
72						–94%	–34%	200
73	37	19	10			–92%	–38%	203
74						–90%	–43%	205
75	38					–88%	–47%	208
76						–86%	–51%	211
77	39	20				–83%	–56%	214
78						–80%	–60%	217
79	40					–77%	–63%	219
80						–74%	–67%	222
81	41	21	11	6	3	–71%	–71%	225
82						–67%	–74%	228

Table 7-2. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
83	42					–63%	–77%	231
84						–60%	–80%	233
85	43	22				–56%	–83%	236
86						–51%	–86%	239
87	44					–47%	–88%	242
88						–43%	–90%	245
89	45	23	12			–38%	–92%	248
90						–34%	–94%	250
91	46					–29%	–96%	253
92						–24%	–97%	256
93	47	24				–20%	–98%	259
94						–15%	–99%	262
95	48					–10%	–100%	264
96						–5%	–100%	267
97	49	25	13	7		0%	–100%	270
98						5%	–100%	273
99	50					10%	–100%	276
100						15%	–99%	278
101	51	26				20%	–98%	281
102						24%	–97%	284
103	52					29%	–96%	287
104						34%	–94%	290
105	53	27	14			38%	–92%	293
106						43%	–90%	295
107	54					47%	–88%	298
108						51%	–86%	301
109	55	28				56%	–83%	304
110						60%	–80%	307
111	56					63%	–77%	309
112						67%	–74%	312
113	57	29	15	8	4	71%	–71%	315
114						74%	–67%	318
115	58					77%	–63%	321
116						80%	–60%	323
117	59	30				83%	–56%	326
118						86%	–51%	329
119	60					88%	–47%	332
120						90%	–43%	335
121	61	31	16			92%	–38%	338
122						94%	–34%	340
123	62					96%	–29%	343
124						97%	–24%	346
125	63	32				98%	–20%	349
126						99%	–15%	352
127	64					100%	–10%	354

Table 7-2. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
128						100%	–5%	357

7.3.6 nRESET, nENBL and nSLEEP Operation

The nRESET pin, when driven active low, resets internal logic, and resets the step table to the home position. It also disables the H-bridge drivers. The STEP input is ignored while nRESET is active.

The nENBL pin is used to control the output drivers and enable or disable operation of the indexer. When nENBL is low, the output H-bridges are enabled, and rising edges on the STEP pin are recognized. When nENBL is high, the H-bridges are disabled, the outputs are in a high-impedance state, and the STEP input is ignored.

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state, all inputs are ignored until nSLEEP returns high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before applying a STEP input, to allow the internal circuitry to stabilize.

The nRESET and nENBL pins have internal pulldown resistors of 100 kΩ. The nSLEEP pin has an internal pulldown resistor of 1 MΩ.

7.3.7 Protection Circuits

The DRV8824 is protected against undervoltage, overcurrent, and overtemperature events.

7.3.7.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device remains disabled until either nRESET pin is applied, nSLEEP is toggled low and high, or VMx is removed and re-applied.

Overcurrent conditions on both high and low side devices, that is, a short to ground, supply, or across the motor winding, all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or xVREF voltage.

7.3.7.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. After the die temperature has fallen to a safe level, operation automatically resumes.

7.3.7.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VMx pins falls below the UVLO threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation resumes when $V_{(VMx)}$ rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 STEP/DIR Interface

The STEP/DIR interface provides a simple method for advancing through the indexer table. For each rising edge on the STEP pin, the indexer travels to the next state in the table. The direction it moves in the table is determined by the input to the DIR pin. The signals applied to the STEP and DIR pins should not violate the timing diagram specified in Figure 6-1.

7.4.2 Microstepping

The microstepping indexer allows for a variety of stepping configurations. The state of the indexer is determined by the configuration of the three MODE pins (refer to Table 7-1 for configuration options). The DRV8824 supports full step up to 1/32 microstepping.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8824 is used in bipolar stepper control. The microstepping motor driver provides additional precision and a smooth rotation from the stepper motor. The following design is a common application of the DRV8824.

8.2 Typical Application

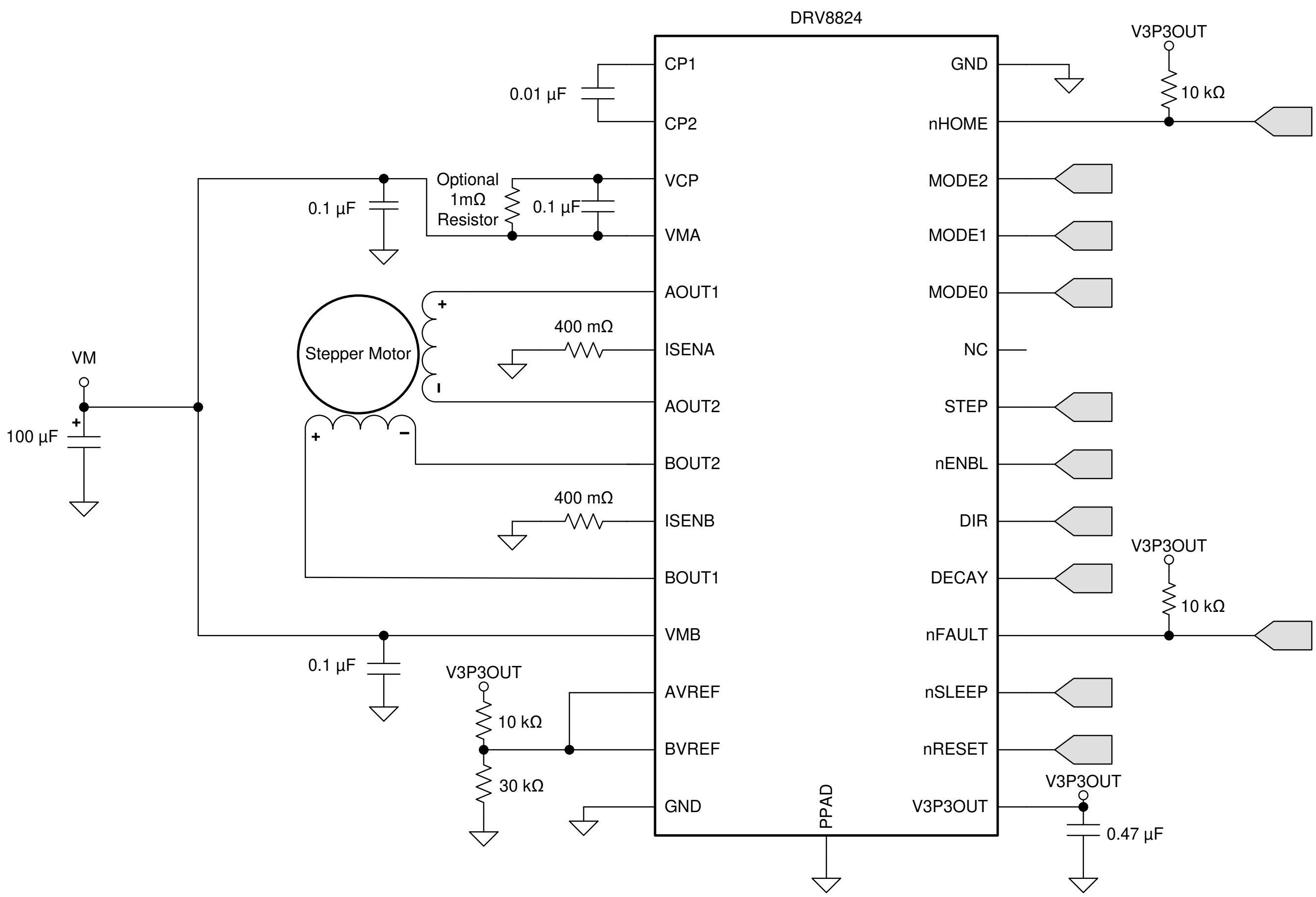


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

Table 8-1 gives design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VMx	24 V
Motor winding resistance	R_L	1.0 Ω/phase
Motor winding inductance	L_L	3.5 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	8 microsteps per step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	1.25 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8824 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor startup speed is too high, the motor will not spin. Make sure that the motor can support the target speed or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\,(\mu steps / second) = \frac{v\left(\frac{rotations}{minute}\right) \times 360\left(\frac{°}{rotation}\right) \times n_m\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times \theta_{step}\left(\frac{°}{step}\right)} \tag{2}$$

$$f_{step}\,(\mu steps / second) = \frac{120\left(\frac{rotations}{minute}\right) \times 360\left(\frac{°}{rotation}\right) \times 8\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times 1.8\left(\frac{°}{step}\right)} \tag{3}$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

For the DRV8824, the microstepping level is set by the MODE pins and can be any of the settings in Table 7-1. Higher microstepping will mean a smoother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

8.2.2.2 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the xVREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8824 is set for 5 V/V.

$$I_{FS}\,(A) = \frac{xVREF\,(V)}{A_v \times R_{SENSE}\,(\Omega)} = \frac{xVREF\,(V)}{5 \times R_{SENSE}\,(\Omega)} \tag{4}$$

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.4 Ω, xVREF should be 2.5 V.

8.2.2.3 Decay Modes

The DRV8824 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8824 will place the winding in one of the three decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time, t_{BLANK}, defines the minimum drive time for the current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

8.2.3 Application Curves

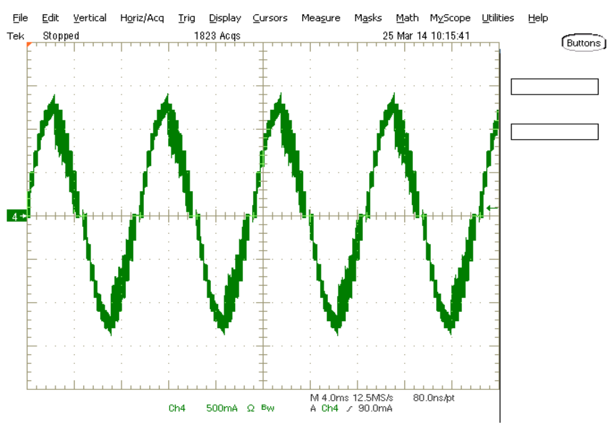


Figure 8-2. Microstepping Waveform, Phase A, Mixed Decay

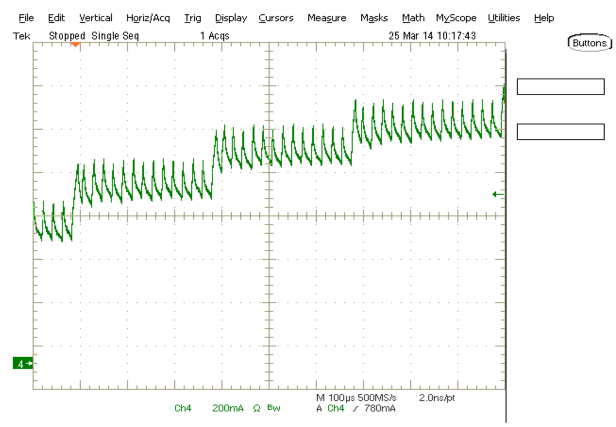


Figure 8-3. Microstepping Waveform, Slow Decay on Increasing Steps

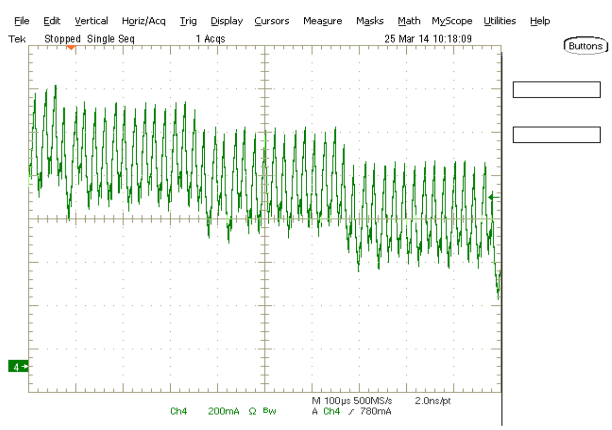


Figure 8-4. Microstepping Waveform, Mixed Decay on Decreasing Steps

Power Supply Recommendations

The DRV8824 is designed to operate from an input voltage supply ($V_{(VMx)}$) range between 8.2 and 45 V. Two 0.01-µF ceramic capacitors rated for VMx must be placed as close as possible to the VMA and VMB pins respectively (one on each pin). In addition to the local decoupling caps, additional bulk capacitance is required and must be sized accordingly to the application requirements.

9.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. It depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. The designer must size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

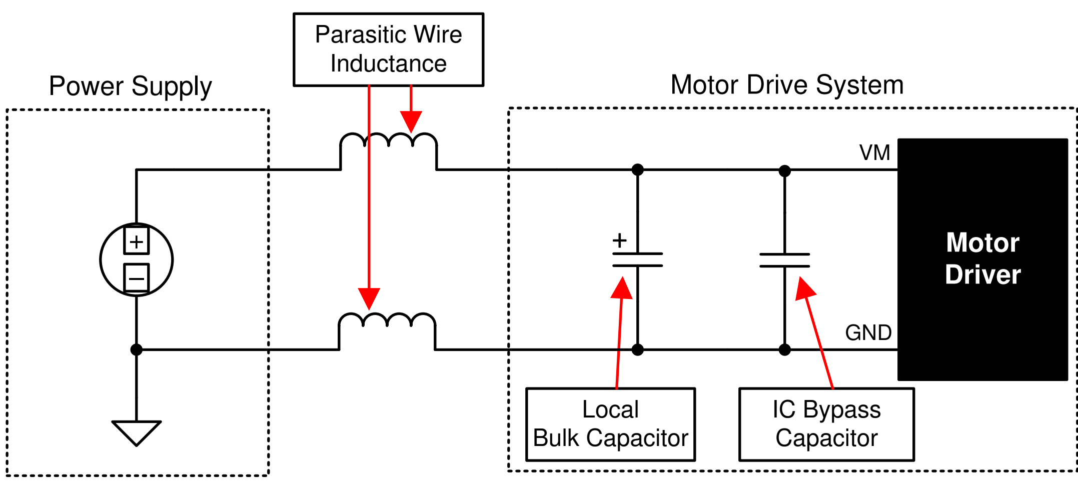


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

9.2 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8824. It is okay for digital input signals to be present before VMx is applied. After VMx is applied to the DRV8824, it begins operation based on the status of the control pins.

9 Layout

9.1 Layout Guidelines

The VMA and VMB pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VMx. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

The VMA and VMB pins must be bypassed to ground using a bulk capacitor. This component may be an electrolytic. If VMA and VMB are connected to the same board net, a single bulk capacitor is sufficient.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.01 µF rated for VMA and VMB. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VMA and VCP pins. TI recommends a value of 0.1 µF rated for 16 V. Place this component as close to the pins as possible. Also, an optional 1-MΩ resistor may be placed between VCP and VMA to accelerate discharge of the VCP capacitor.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

9.2 Layout Example

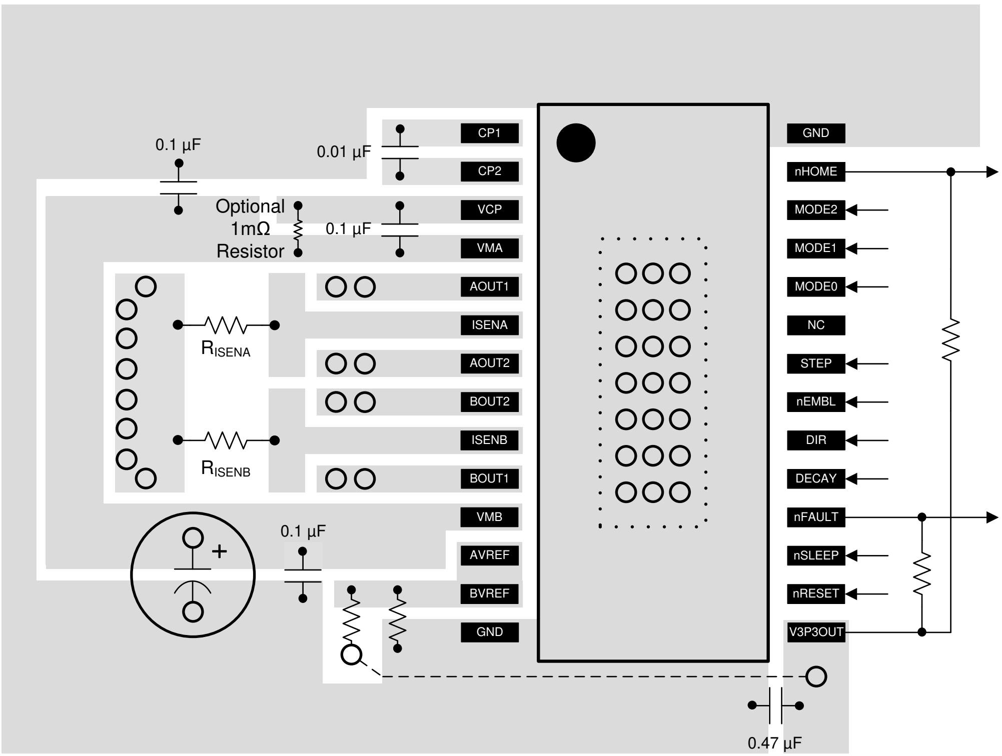


Figure 9-1. Layout Recommendation

9.3 Thermal Considerations

The DRV8824 has TSD, as described in *Section 7.3.7.2*. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

9.4 Power Dissipation

Power dissipation in the DRV8824 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 5.

$$P_{TOT} = 4 \times R_{DS(ON)} \times \left(I_{OUT(RMS)}\right)^2 \quad (5)$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of each FET
- $I_{OUT(RMS)}$ is the RMS output current being applied to each winding

$I_{OUT(RMS)}$ is equal to the approximately 0.7× the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

9.5 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, *PowerPAD™ Thermally Enhanced Package* and TI application brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. It can be seen that the heatsink effectiveness increases rapidly to about 20 cm^2, then levels off somewhat for larger areas.

10 Device and Documentation Support

10.1 Community Resources

10.2 Trademarks

PowerPAD™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8824PWP	Obsolete	Production	HTSSOP (PWP) | 28	-	-	Call TI	Call TI	-40 to 85	DRV8824
DRV8824PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8824
DRV8824PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8824
DRV8824PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8824
DRV8824RHDR	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8824
DRV8824RHDR.A	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8824
DRV8824RHDR.B	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8824
DRV8824RHDT	Obsolete	Production	VQFN (RHD) | 28	-	-	Call TI	Call TI	-40 to 85	DRV8824

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV8824 :

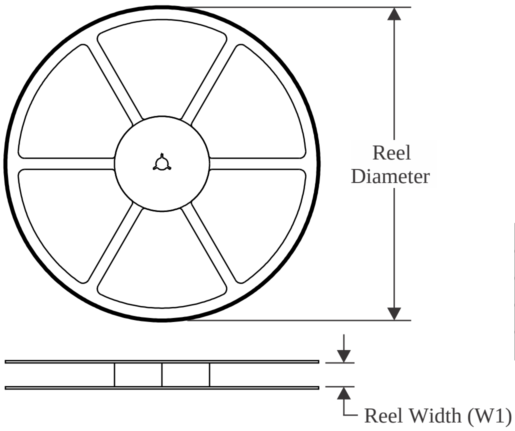
- Automotive : DRV8824-Q1

NOTE: Qualified Version Definitions:

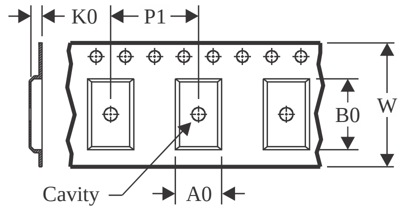
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

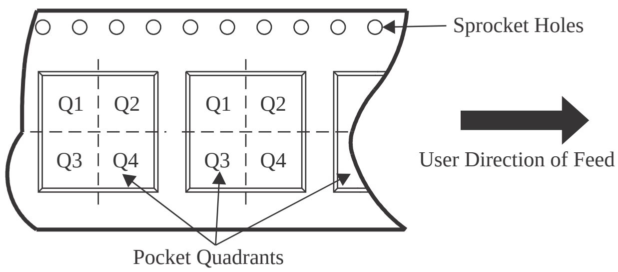


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

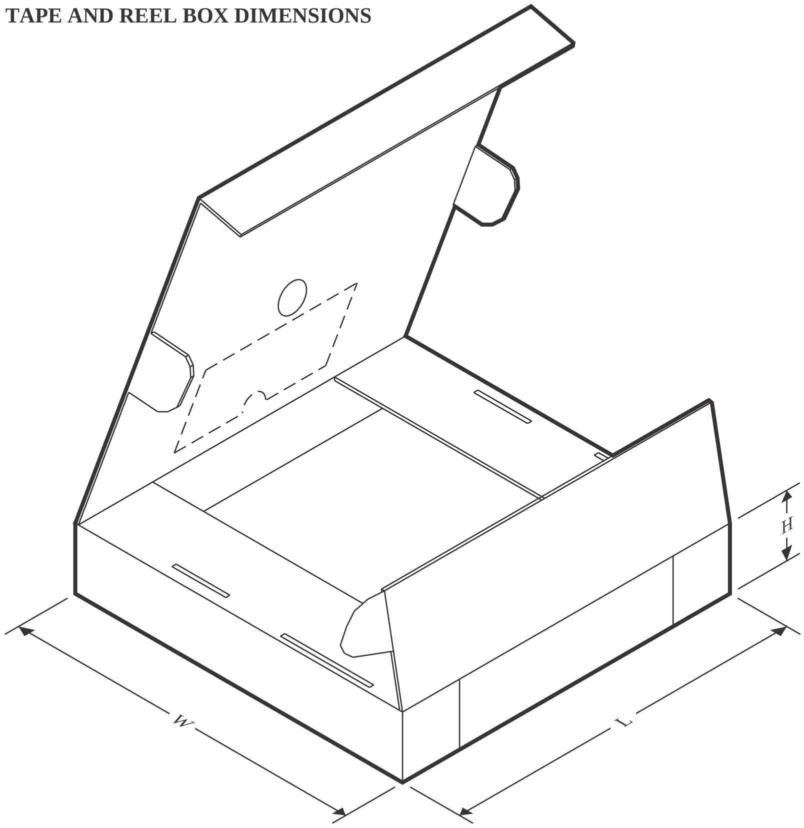
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8824PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8824RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

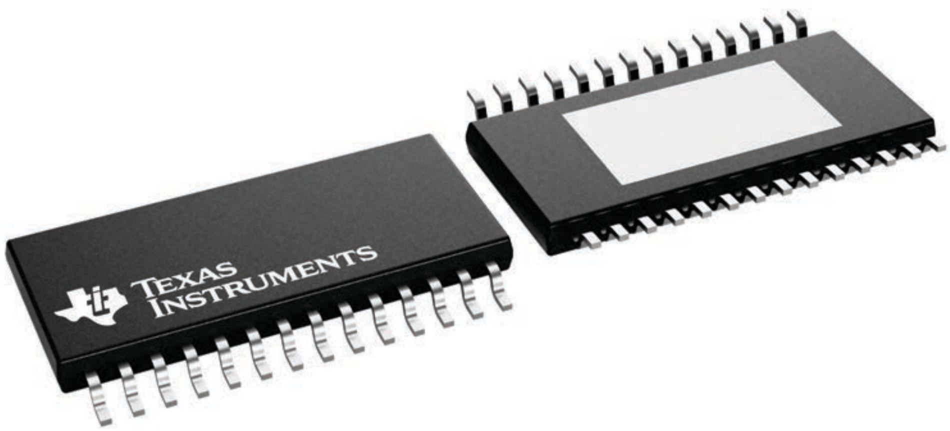
TAPE AND REEL BOX DIMENSIONS

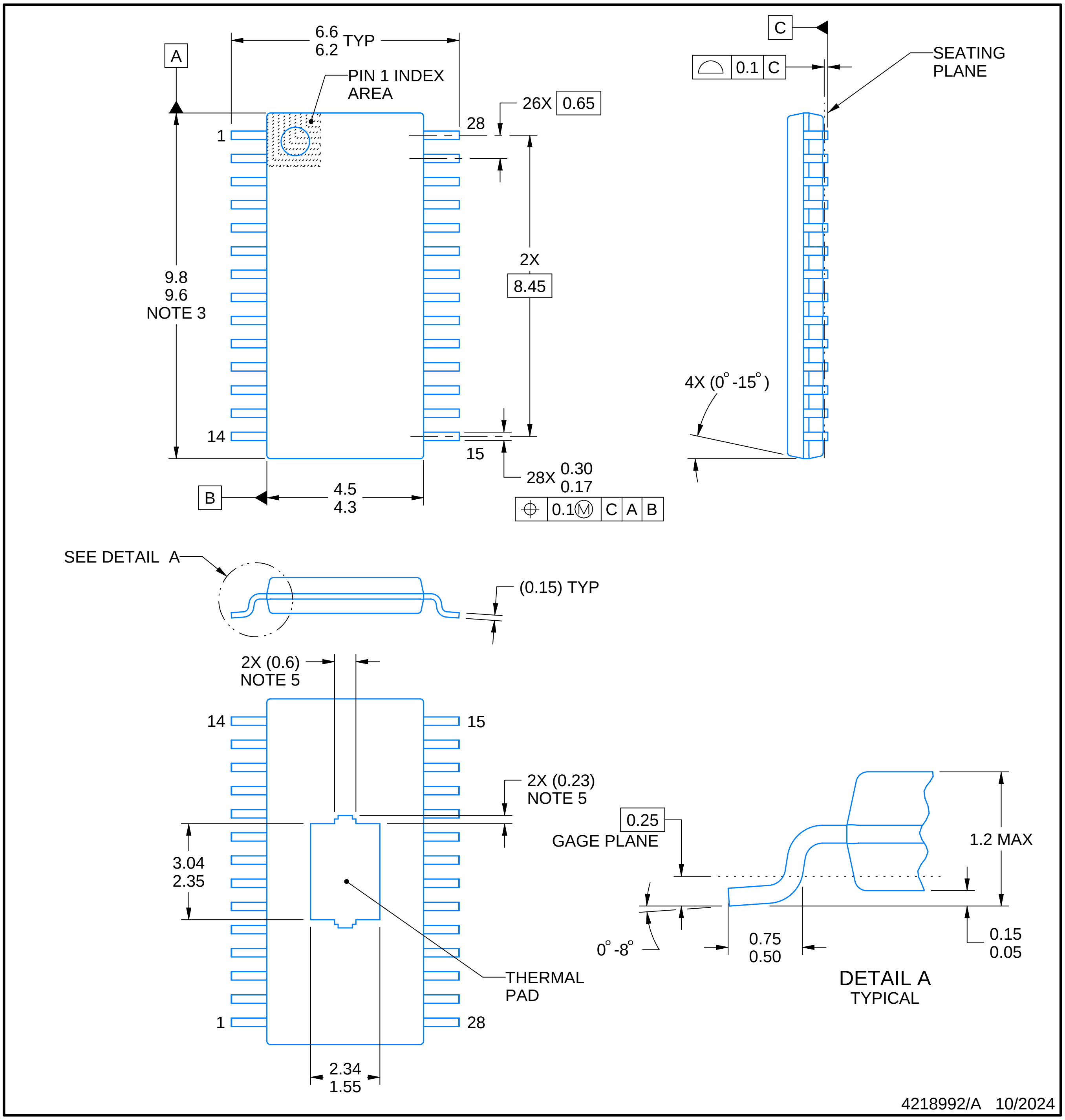


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8824PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
DRV8824RHDR	VQFN	RHD	28	3000	346.0	346.0	33.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

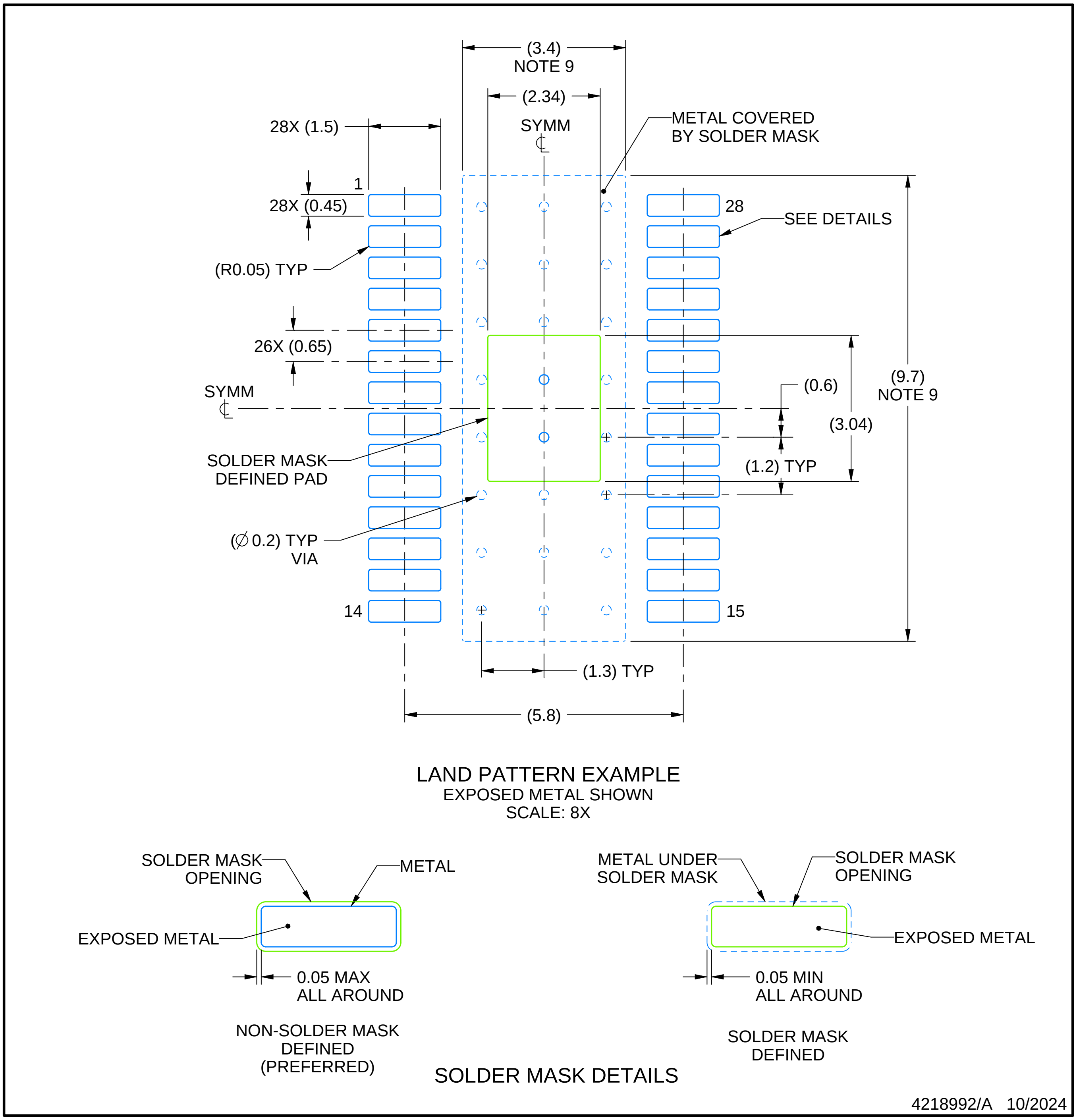




PowerPAD is a trademark of Texas Instruments.

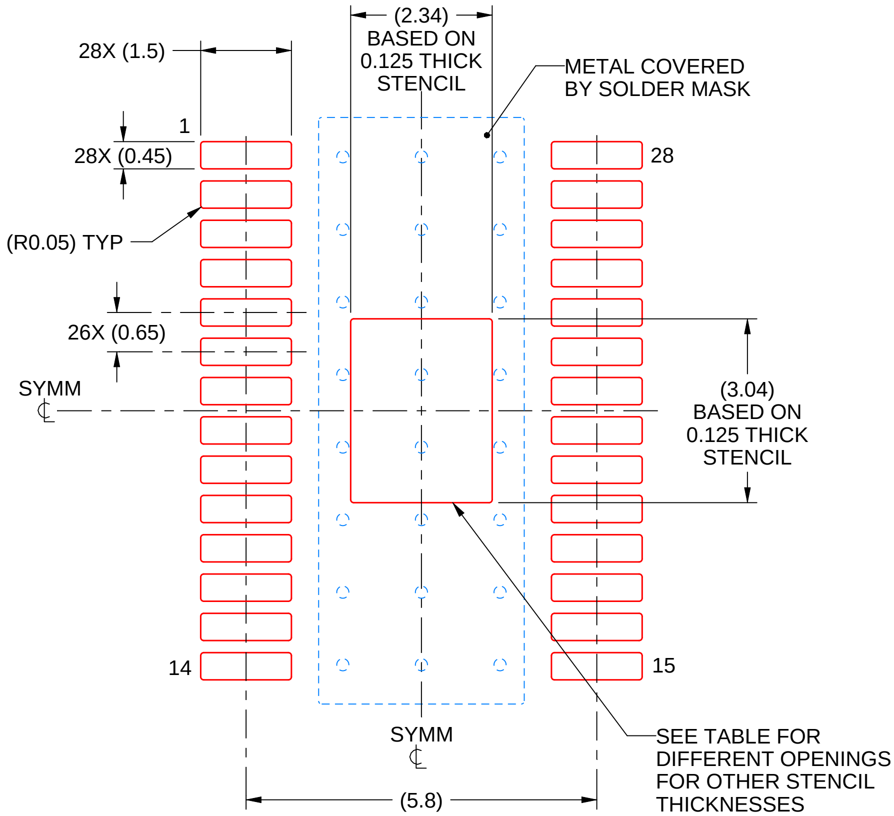
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

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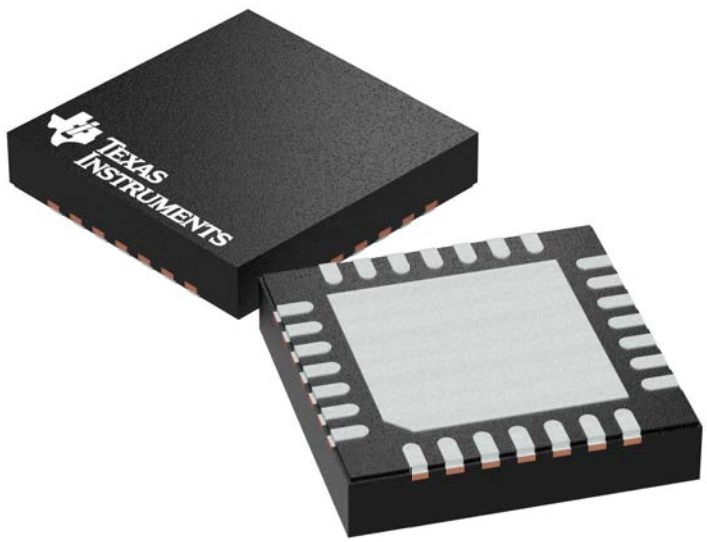
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

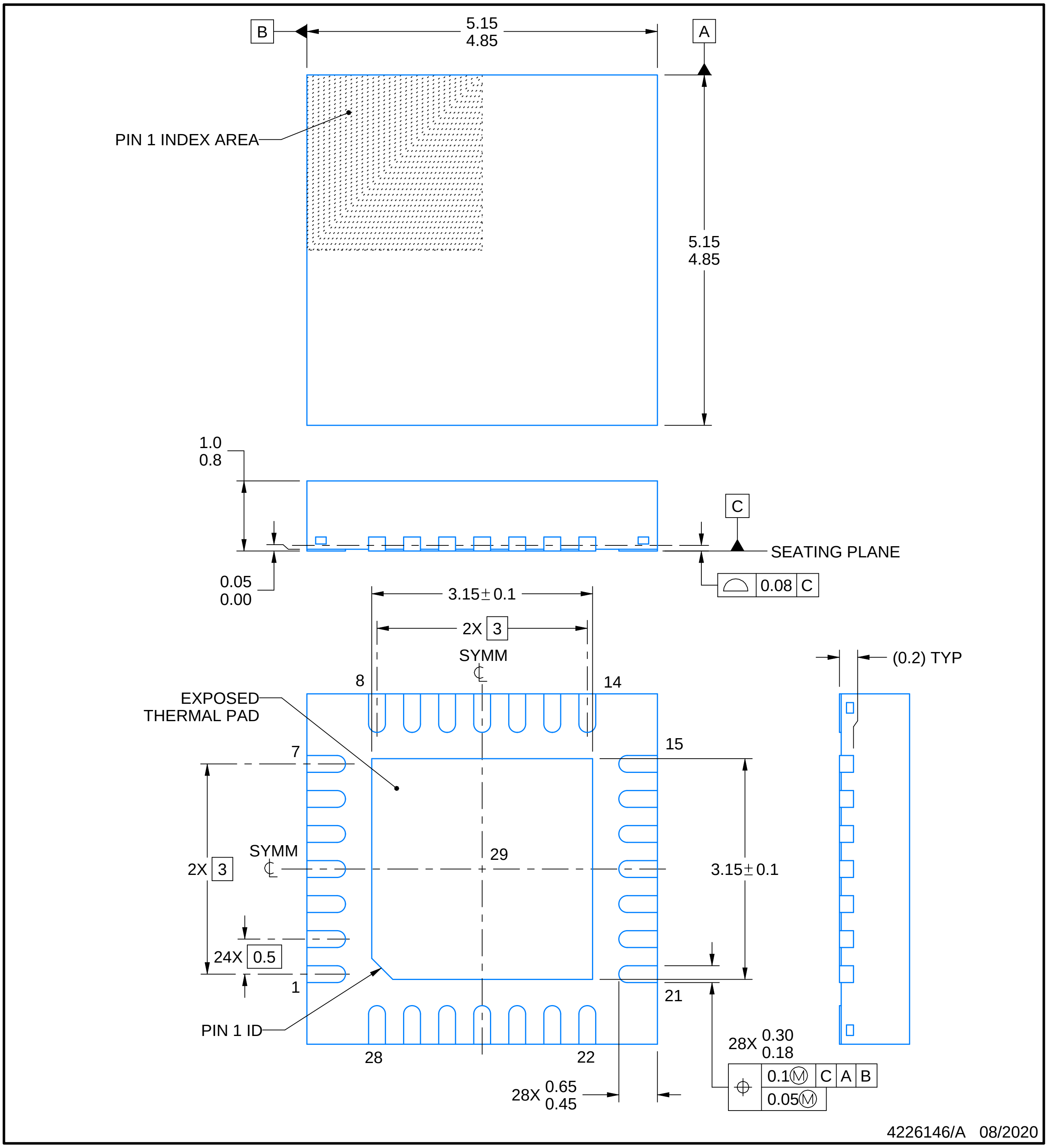
GENERIC PACKAGE VIEW

RHD 28 — VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch — PLASTIC QUAD FLATPACK - NO LEAD

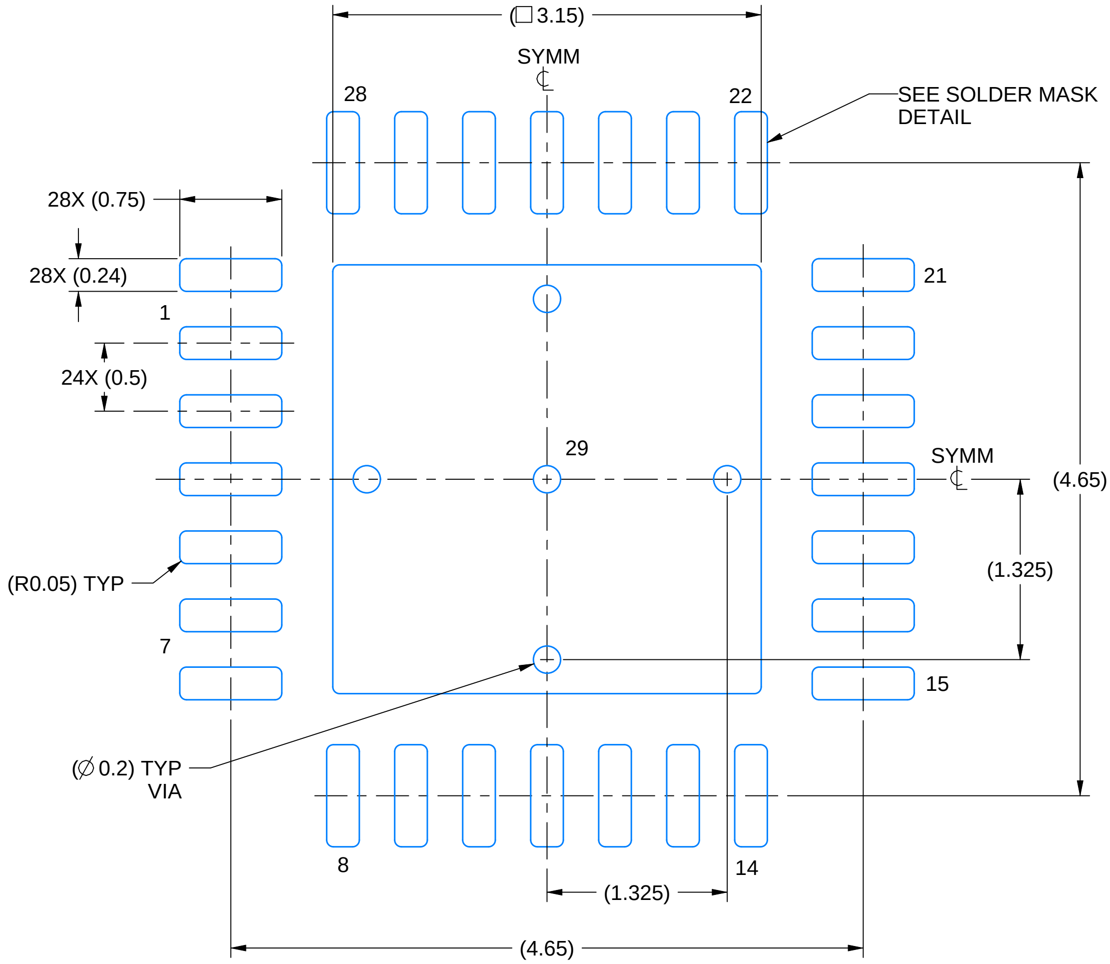


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

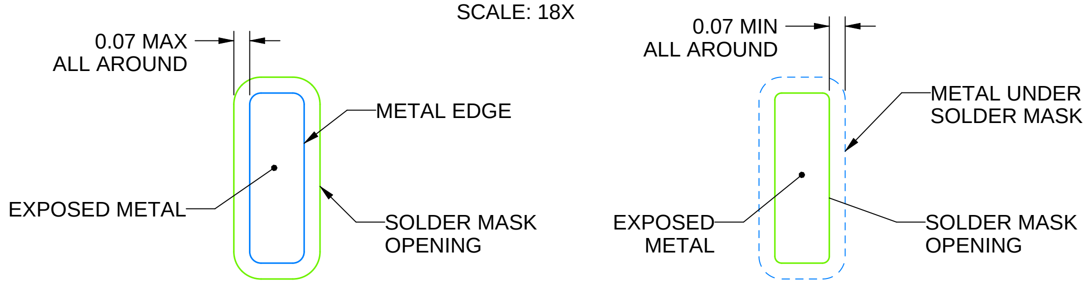


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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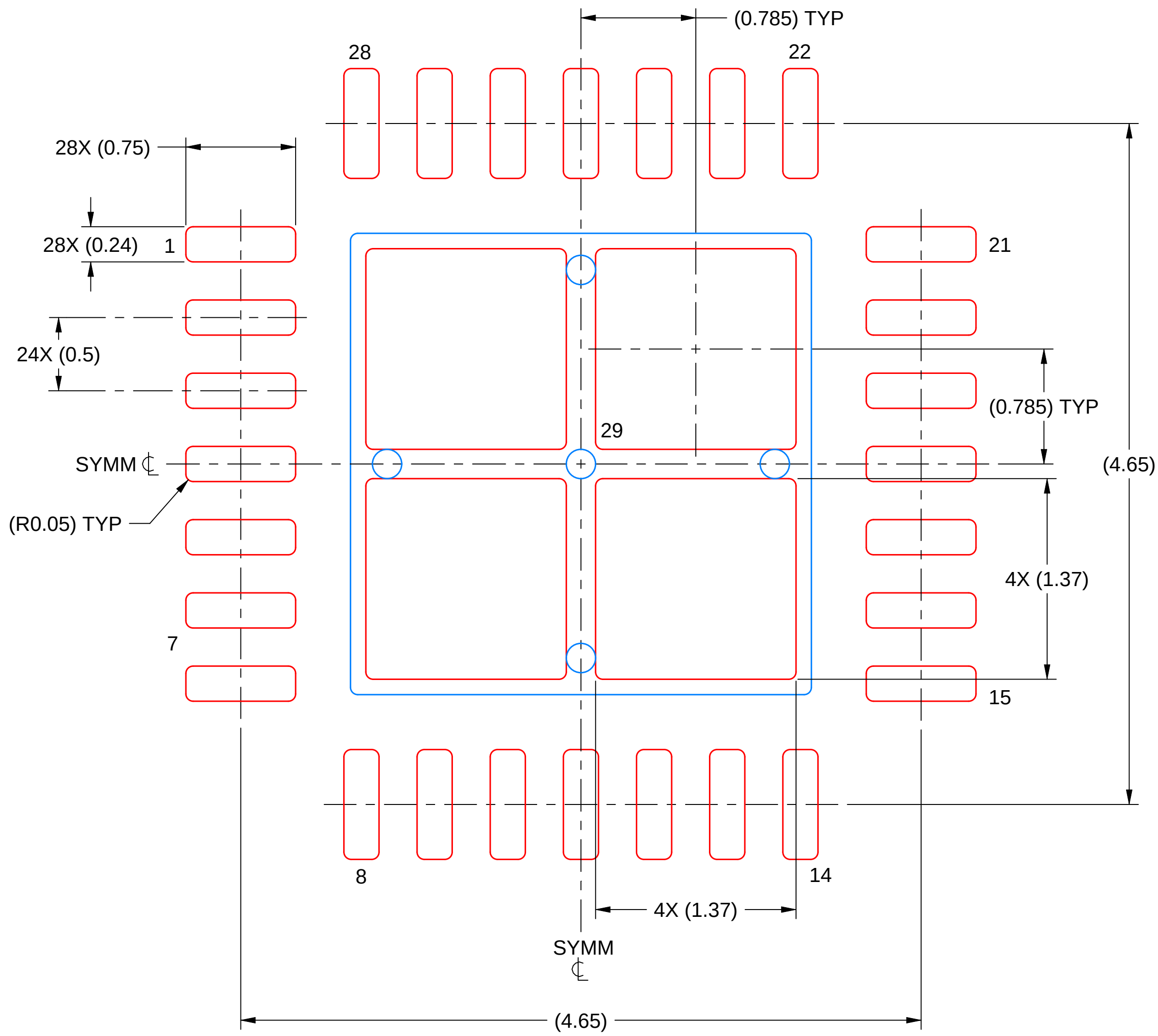
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265