DRV8801-Q1 DMOS Full-Bridge Motor Drivers

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With The Following Results:
  - Device Temperature Grade 1: T_A = –40°C to 125°C
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4
- Low $R_{DS(on)}$ Outputs (0.83-Ω HS + LS Typical)
- Low-Power Sleep Mode
- 100% PWM Duty Cycle Supported
- 8–38 V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package
- Configurable Overcurrent Limit
- **Protection Features**
  - VBB Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Short-to-supply Protection
  - Short-to-ground Protection
  - Overtemperature Warning (OTW)
  - Overtemperature Shutdown (OTS)
  - Overcurrent and Overtemperature Fault Conditions Indicated on Pins (nFAULT)

2 Applications

- Automotive Body Systems
- Door Locks
- HVAC Actuators
- Piezo Alarm

3 Description

The DRV8801-Q1 provides a versatile power driver solution with a full H-bridge driver. The device can drive a brushed DC motor or one winding of a stepper motor, as well as other devices like solenoids. A simple PHASE/ENABLE interface allows easy interfacing to controller circuits

The output stages use N-channel power MOSFETs configured as ½-H-bridges. The DRV8801-Q1 is capable of peak output currents up to ±2.8 A and operating voltages up to 38 V. An internal charge pump generates needed gate drive voltages.

A low-power sleep mode is provided which shuts down internal circuitry to achieve very low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

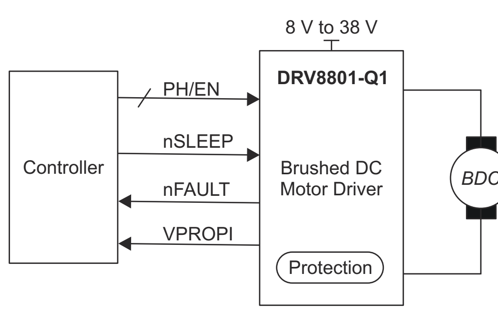
Internal protection functions are provided: undervoltage lockout, overcurrent protection, short-to-supply protection, short-to-ground protection, overtemperature warning, and overtemperature shutdown. Overcurrent (including short-to-ground and short-to-supply) and overtemperature fault conditions are indicated via an nFAULT pin.

The DRV8801-Q1 is packaged in a 16-pin QFN package with exposed thermal pad, providing enhanced thermal dissipation.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
DRV8801-Q1	QFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2016) to Revision D (March 2021) — **Page**

- Improved description for pins CP1,CP2,nFAULT, nSLEEP, VBB and VCP in *Pin Functions* table....4
- Added entries for VCP and CP2 pins in *Absolute Maximum Ratings* table....5
- Change SLEEP to nSLEEP in PWM Control Timing Figure....8
- Provide additional information on SENSE pin behavior....13
- Added equation for VPROPI to help when connecting pin's output to ADC in *Feature Description*....14
- Added die temperature estimation equation utilizing junction to ambient thermal impedance in Application and Implementation section....17
- Added information on using motor driver's pulse width modulating modes in *Application and Implementation* section....18
- Added information on connecting multiple DRV8801-Q1 together to support higher current in *Application and Implementation* section....19

Changes from Revision B (January 2016) to Revision C (June 2016) — **Page**

- Changed one of the MODE1 pins to MODE2 in the *Functional Block Diagram* section....11
- Added the *Receiving Notification of Documentation Updates* section....25

Changes from Revision A (January 2014) to Revision B (October 2014) — **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....5
- Added t_{pd} to the *Overcurrent Control Timing* image....13

Changes from Revision * (February 2011) to Revision A (January 2014) — **Page**

- Deleted part number DRV8800-Q1 from page header....1
- Added AEC-Q100 qualifications to Features list....1
- Added an Applications section to the front page....1
- Deleted part number DRV8800-Q1 from Description section....1
- Deleted Ordering Information table....1
- Deleted DRV8800-Q1 pinout diagram....4

- Deleted Terminal Name column for DRV8800-Q1 from Terminal Functions table..4
- Deleted DRV8800-Q1 pin descriptions for pins 5 and 9 from Terminal Functions table....................................4
- Added a Thermal Information table.. 5
- Removed DRV8800-Q1 part number from column heading of Thermal Information table................................5
- Changed parameter name and test condition for Electrical Characteristics, VTRP row....................................7
- Added two notes to end of Electrical Characteristics table...7
- Changed "Overcurrent protection period" parameter to "Overcurrent retry time"..8
- Deleted DRV8800-Q1 from text of Device Operation section... 11
- Deleted DRV8800-Q1 Functional Block Diagram... 11
- Updated the *Overcurrent Control Timing* image.. 13
- Updated the *Overcurrent Control Timing* image.. 14
- Changed *active low* to *low* in Diagnostic Output section.. 15
- Deleted VREG section; deleted "(DRV8801-Q1 Only)" from VPROPI section title.. 15
- Changed a value in row 5 of the Control Logic Table... 15
- Added a row to Control Logic Table...15
- Deleted DRV8800-Q1 from the text of the Low-Power Mode sedtion... 15
- Deleted DRV8800-Q1 Typical Application Diagram...16
- Corrected part number in DRV8801-Q1 application diagram.. 16

5 Pin Configuration and Functions

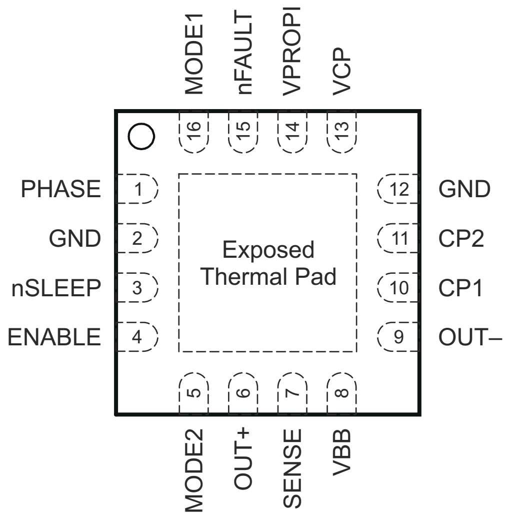


Figure 5-1. RTY Package 16-Pin QFN With Exposed Thermal Pad Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CP1	10	PWR	Charge pump switching node. Connect a X7R, 0.1-μF, VBB-rated ceramic capacitor from CP1 to CP2.
CP2	11	PWR	
ENABLE	4	I	Enable logic input
GND	2, 12	PWR	Ground
MODE 1	16	I	Mode logic input
MODE 2	5	I	Mode 2 logic input
nFAULT	15	O	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	3	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
OUT+	6	O	DMOS full-bridge output positive
OUT–	9	O	DMOS full-bridge output negative
PHASE	1	I	Phase logic input for direction control
SENSE	7	IO	Sense power return
VBB	8	PWR	Driver supply voltage. Bypass to GND with 0.1-μF ceramic capacitors plus a bulk capacitor rated for VBB.
VCP	13	O	Charge pump reservoir capacitor pin. Connect a X7R, 0.1-μF, 16-V ceramic capacitor to VBB.
VPROPI	14	O	Winding current proportional voltage output
Thermal Pad	PAD	PWR	Exposed pad for thermal dissipation; connect to GND pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
V_{BB}	Load supply voltage[(2)]	–0.3	40	V
VCP and CP2	Charge pump voltage	–0.3	VBB+17	V
I_{OUT}	Output current	0	2.8	A
V_{Sense}	Sense voltage	–500	500	mV
V_{BB_OUT}	VBB to OUTx		36	V
V_{OUT_SEN}	OUTx to SENSE		36	V
V_{DD}	PHASE, ENABLE, MODE1, MODE2, nSLEEP, nFAULT[(2)]	–0.3	7	V
P_D	Continuous total power dissipation	See *Section 6.4*		
T_A	Operating free-air temperature	–40	125	°C
T_J	Maximum junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{BB}	Power supply voltage	8	38	V
V_{DD}	Logic voltage	0	5.5	V
f_{PWM}	Applied PWM signal (PHASE and ENABLE)	0	100	kHz
T_A	Ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		DRV8801-Q1 RTY (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.5	°C/W

THERMAL METRIC[(1)]		DRV8801-Q1 RTY (QFN) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VBB)							
VBB	VBB operating voltage			8		38	V
I_{VBB}	VBB operating supply current	f_{PWM} < 50 kHz			6		mA
		Charge pump on, outputs disabled			3.2		
I_{VBBQ}	VBB sleep-mode supply current	nSLEEP = 0, T_J = 25°C				10	µA
CONTROL INPUTS (PHASE, ENABLE, MODE1, MODE2, nSLEEP)							
V_{IL}	Input logic low voltage	PHASE, ENABLE, MODE1, MODE2				0.8	V
V_{IH}	Input logic high voltage			2			
V_{IHYS}	Input hysteresis			100	500	800	mV
I_{IL}	Input logic low current	PHASE, MODE1, MODE2	V_{IN} = 0.8 V	–20	< –2	20	µA
I_{IH}	Input logic high current		V_{IN} = 2.0 V		< 1	20	
I_{IL}	Input logic low current	ENABLE	V_{IN} = 0.8 V		16	40	µA
I_{IH}	Input logic high current		V_{IN} = 2.0 V		40	100	
V_{IL}	Input logic low voltage	nSLEEP				0.8	V
V_{IH}	Input logic high voltage			2.7			V
I_{IL}	Input logic low current		V_{IN} = 0.8 V		<1	10	µA
I_{IH}	Input logic high current		V_{IN} = 2.7 V		27	50	
CONTROL OUTPUTS (nFAULT)							
V_{OL}	Output logic low voltage	I_O = 1 mA				0.4	V
VBBNFR	VBB nFAULT release	8 V < VBB < 40 V			12	13.8	V
DMOS DRIVERS (OUT+, OUT-, SENSE, VPROPI)							
$R_{DS(on)}$	Output ON resistance	Source driver, I_{OUT} = –2.8 A, T_J = 25°C			0.48		Ω
		Source driver, I_{OUT} = –2.8 A, T_J = 125°C			0.74	0.85	
		Sink driver, I_{OUT} = 2.8 A, T_J = 25°C			0.35		
		Sink driver, I_{OUT} = 2.8 A, T_J = 125°C			0.52	0.7	
V_{TRIP}	SENSE trip voltage	R_{SENSE} between SENSE and GND			500		mV
V_f	Body diode forward voltage	Source diode, I_f = –2.8 A				1.4	V
		Sink diode, I_f = 2.8 A				1.4	
A_{VDA}	Differential AMP gain	SENSE = 0.1 V to 0.4 V			5		V/V
PROTECTION CIRCUITRY							
VUV	UVLO threshold	VBB increasing			6.5	7.5	V
I_{OCP}	Overcurrent protection trip level	VBB = 8.0 approximately 38 V		3			A
T_{OTW}	Thermal warning temperature	Die temperature T_j (1)			160		°C
$T_{OTW\ HYS}$	Thermal warning hysteresis	Die temperature T_j			15		°C
T_{OTS}	Thermal shutdown temperature	Die temperature T_j (2)			175		°C
$T_{OTS\ HYS}$	Thermal shutdown hysteresis	Die temperature T_j			15		°C

(1) Once the device reaches the thermal warning temperature of 160°C, the device remains in thermal warning until the device cools to 145°C. This is known as the thermal-warning hysteresis of the device.

(2) Once the device reaches the thermal shutdown temperature of 175°C, the device remains in thermal shutdown until the device cools to 160°C. This is known as the thermal-shutdown hysteresis of the device.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{pd}	Propagation delay time	Input edge to source or sink ON		600		ns
		Input edge to source or sink OFF		100		
t_{COD}	Crossover delay			500		ns
t_{DEG}	Overcurrent deglitch time			3		µs
t_{OCP}	Overcurrent retry time			1.2		ms

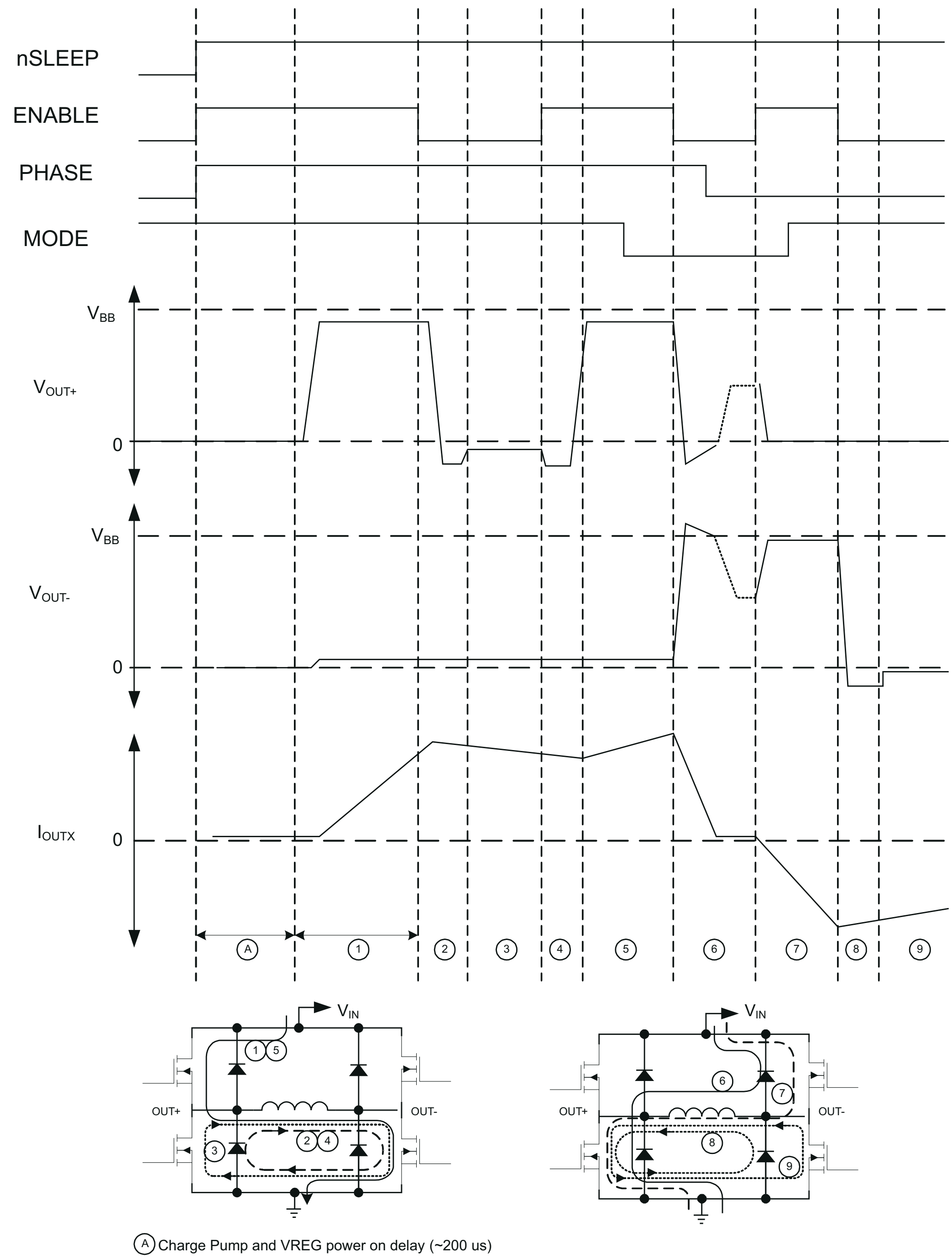


Figure 6-1. PWM Control Timing

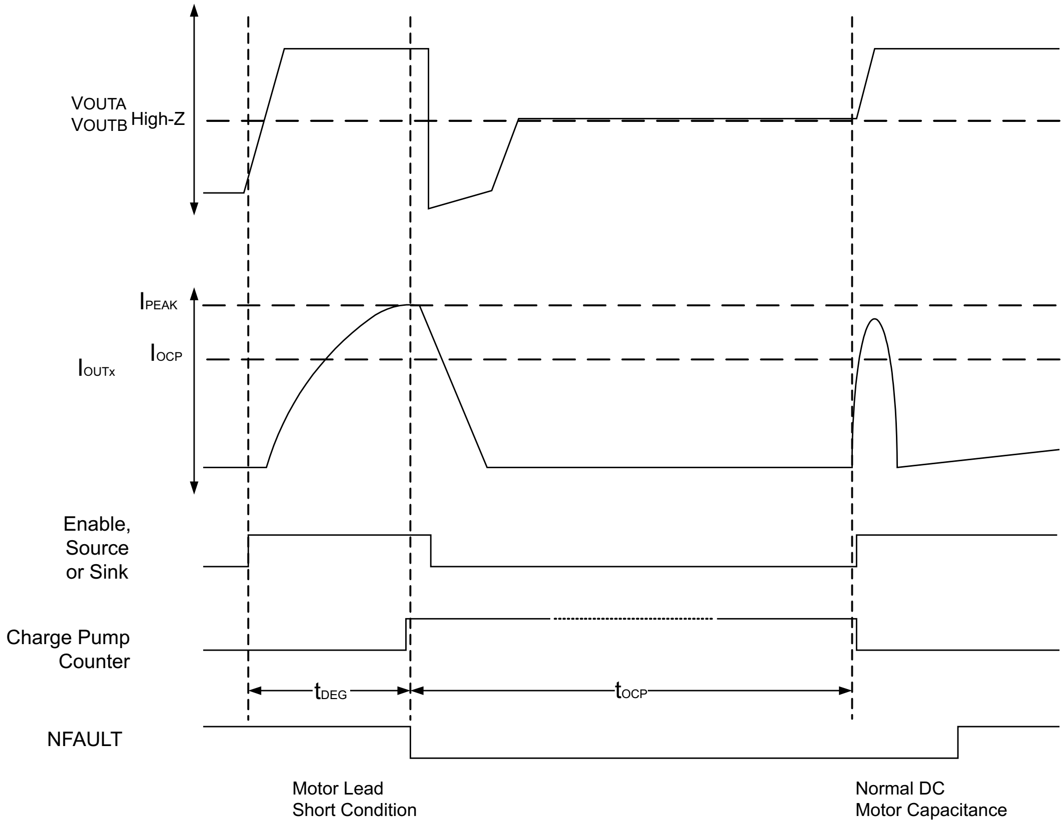


Figure 6-2. Overcurrent Control Timing

6.7 Typical Characteristics

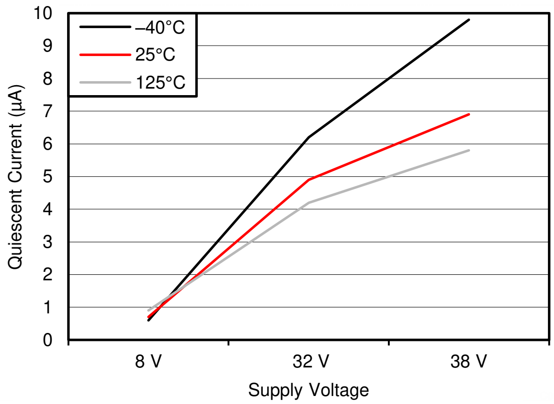


Figure 6-3. I_{VBBQ}vs VBB

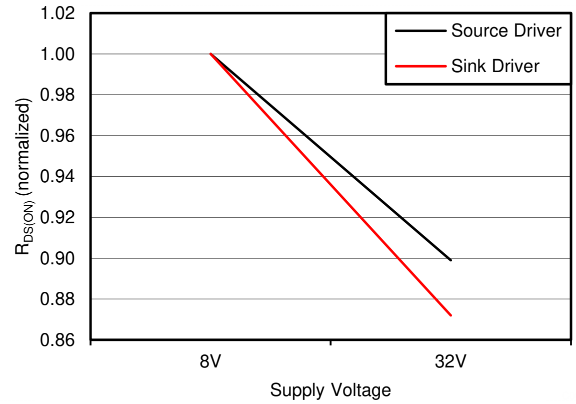


Figure 6-4. $R_{DS(ON)}$ vs VBB (Normalized to VBB = 8 V)

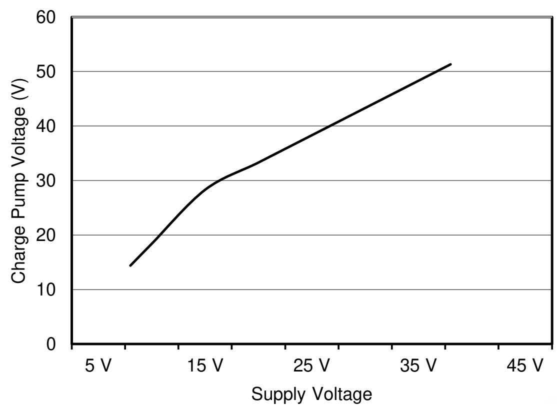


Figure 6-5. VCP vs VBB

7 Detailed Description

7.1 Overview

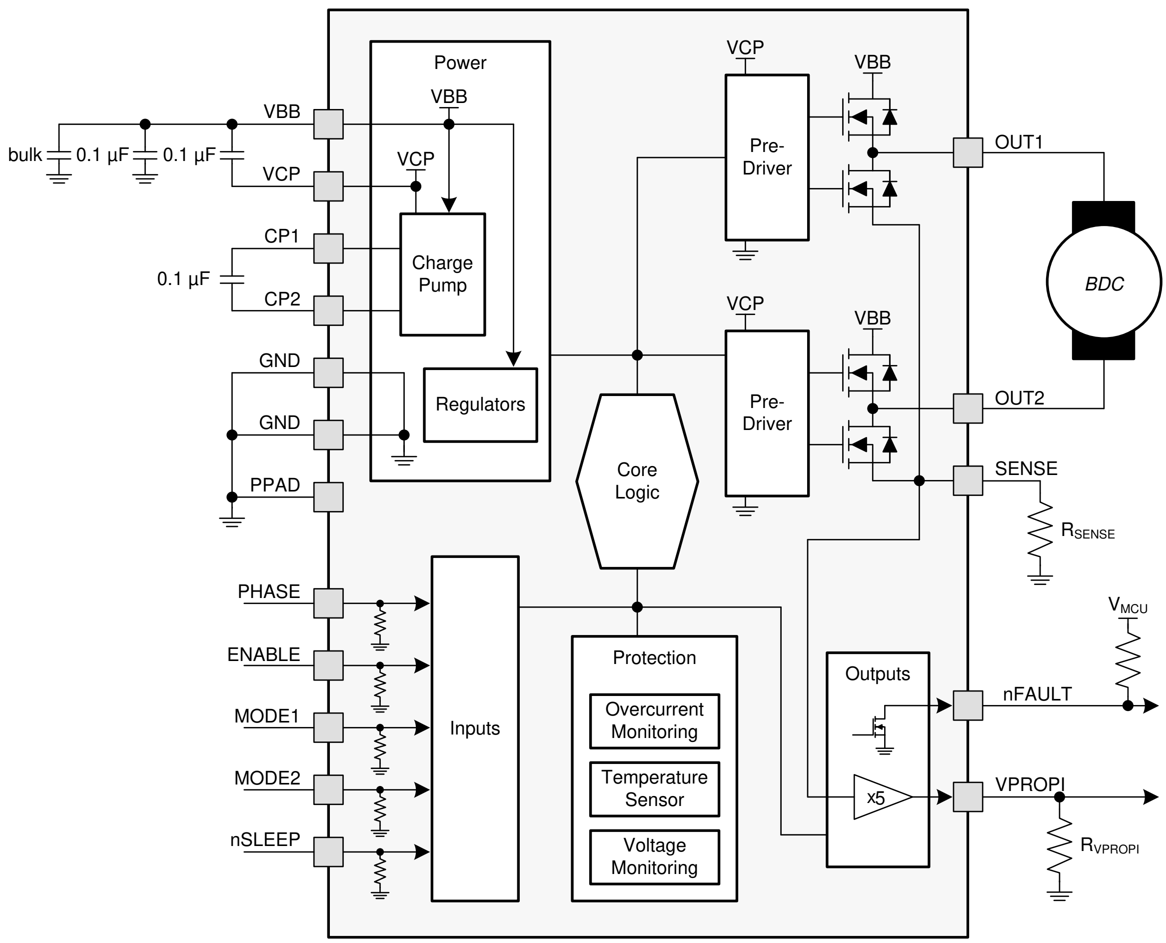
The DRV8801-Q1 is an integrated motor driver solution for brushed-DC motors. The device integrates a DMOS H-bridge and current sense and protection circuitry. The device can be powered with a supply voltage between 8 and 38 V, and is capable of providing an output current up to 2.8 A peak.

A simple PHASE-ENABLE interface allows control of the motor speed and direction.

A shunt amplifier output is provided for accurate current measurements by the system controller. The VPROPI pin will output a voltage that is 5 times the voltage seen at the SENSE pin.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supervisor

The control input, nSLEEP, is used to minimize power consumption when the DRV8801-Q1 device is not in use. A logic low on the nSLEEP input disables much of the internal circuitry, including the internal voltage rails and charge pump. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

7.3.2 Bridge Control

Table 7-1 shows the logic for the DRV8801-Q1:

Table 7-1. Bridge Control Logic Table

nSLEEP	PHASE	ENABLE	MODE1	MODE2	OUTA	OUTB	OPERATION
0	X	X	X	X	Z	Z	Sleep mode
1	0	1	X	X	L	H	Reverse
1	1	1	X	X	H	L	Forward
1	0	0	0	X	H	L	Fast decay
1	1	0	0	X	L	H	Fast decay
1	X	0	1	0	L	L	Low-side Slow decay
1	X	0	1	1	H	H	High-side Slow decay

To prevent reversal of current during fast-decay synchronous rectification, outputs go to the high impedance state as the current approaches 0 A.

The path of current flow for each of the states in the above logic table is shown in Figure 7-1.

7.3.2.1 MODE 1

Input MODE 1 is used to toggle between fast-decay mode and slow-decay mode. A logic high puts the device in slow-decay mode.

7.3.2.2 MODE 2

MODE 2 is used to select which set of drivers (high side versus low side) is used during the slow-decay recirculation. MODE 2 is meaningful only when MODE 1 is asserted high. A logic high on MODE 2 has current recirculation through the high-side drivers. A logic low has current recirculation through the low-side drivers.

7.3.3 Fast Decay with Synchronous Rectification

This decay mode is equivalent to a phase change where the FETs opposite of the driving FETs are switched on (2 in Figure 7-1). When in fast decay, the motor current is not allowed to go negative because this would cause a change in direction. Instead, as the current approaches zero, the drivers turn off. See the *Section 8.2.2.2* section for an equation to calculate power.

7.3.4 Slow Decay with Synchronous Rectification (Brake Mode)

In slow-decay mode, both low-side and high-side drivers turn on, allowing the current to circulate through the low-side and high-side body diodes of the H-bridge and the load (3 and 4 in Figure 7-1). See the *Section 8.2.2.2* section for equations to calculate power for both high-side and low-side slow decay.

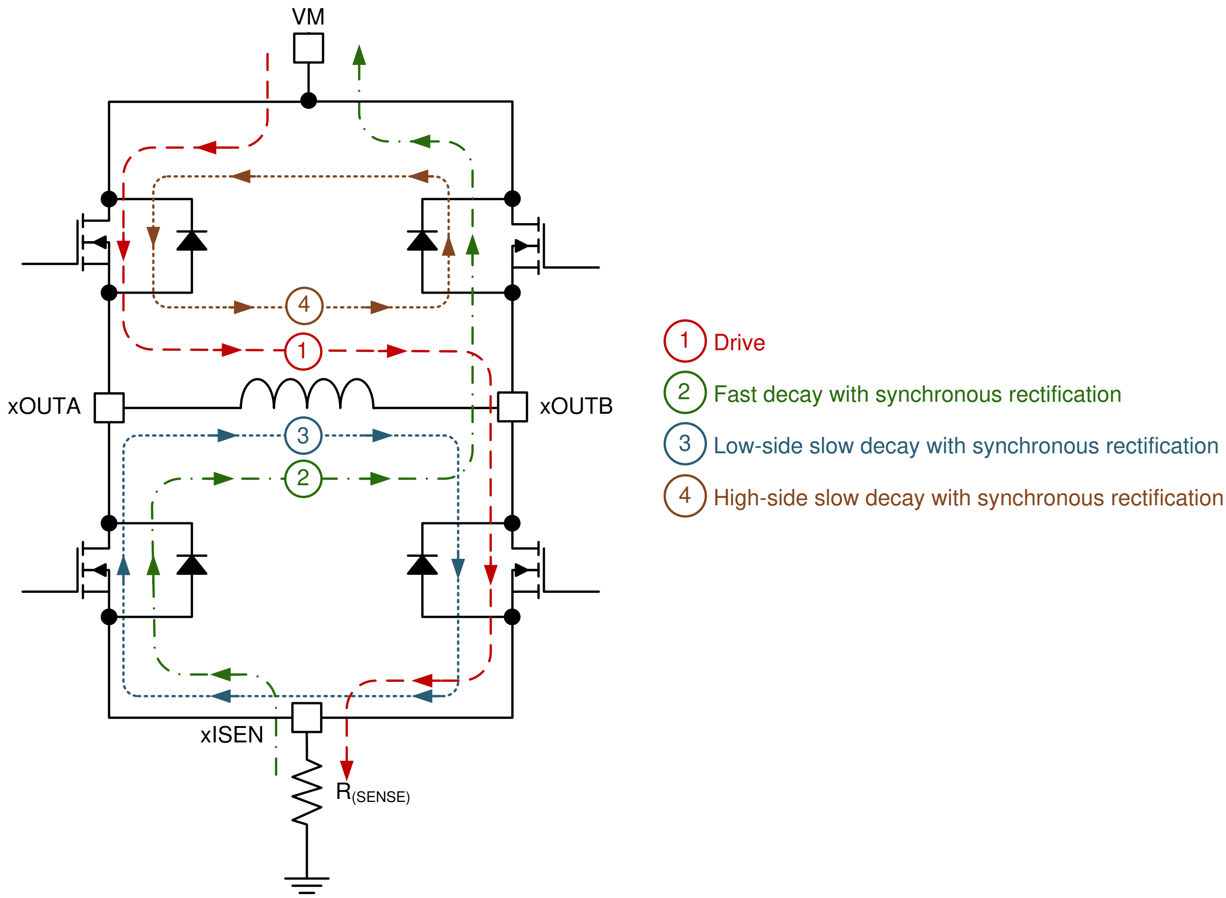


Figure 7-1. H-Bridge Operation Modes

7.3.5 Charge Pump

The charge pump is used to generate a supply above V_{BB} to drive the source-side DMOS gates. A 0.1-µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1-µF ceramic monolithic capacitor should be connected between VCP and V_{BB} to act as a reservoir to run the high-side DMOS devices.

7.3.6 SENSE

A low-value SENSE resistor is used to set an overcurrent threshold lower than the default maximum value of 2.8 A and to provide a voltage for VPROPI. This SENSE resistor must be connected between the SENSE pin and ground. To minimize ground-trace IR drops in sensing the output current level, the current-sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

A direction connection to ground yields a SENSE voltage equal to zero. In that case, maximum current is 2.8 A and VPROPI outputs 0 V. A resistor connected as explained before, will yield a VPROPI output as detailed in the Section 7.3.7. Size the sense resistor such that voltage drop across the sense resistor is less than 500mV under normal loading conditions. Any voltage equal or larger to 500 mV will signal the device to hi-Z the H-bridge output as overcurrent trip threshold has been reached. In this case, device will enter recirculation as stipulated by the MODE input pin. The device automatically retries with a period of $t_{(OCP)}$.

Equation 1 shows the value of the resistor to a particular current setting.

$$R_{sense} = \frac{500\ \text{mV}}{I_{trip}} \tag{1}$$

The overcurrent trip level selected cannot be greater than $I_{(OCP)}$.

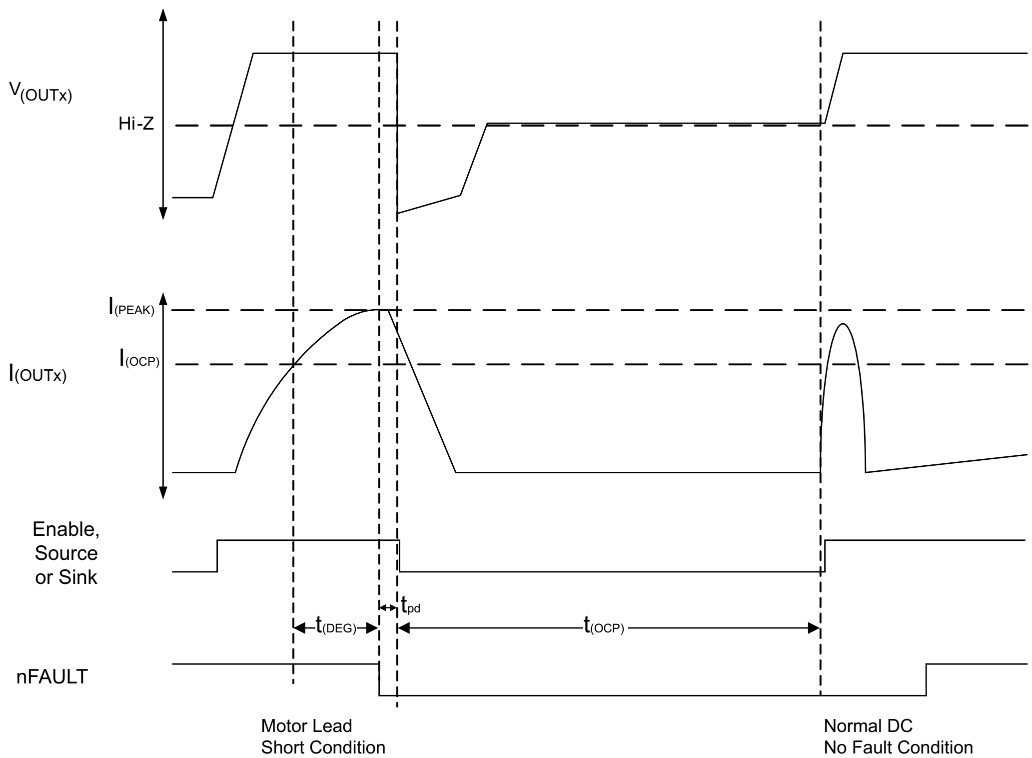


Figure 7-2. Overcurrent Control Timing

7.3.7 VPROPI

The analog output VPROPI offers SENSE current information as an analog voltage proportional to the current flowing through the DC motor winding. This voltage can be used by an analog to digital converter and microcontroller to accurately determine how much current is flowing through the controlled DC motor. The later section discussing the SENSE resistor provides guidance on how to choose the SENSE resistor value.

7.3.7.1 Connecting VPROPI Output to ADC

The analog output VPROPI varies proportionally with the SENSE voltage according to Equation 2. It's important to note even if V_{SENSE} is negative VPROPI will remain at 0 V.

$$\mathrm{VPROPI} = 5 \times V_{SENSE} \tag{2}$$

An RC network in series with the VPROPI output is recommended, if this voltage is to be sampled by an analog to digital converter.

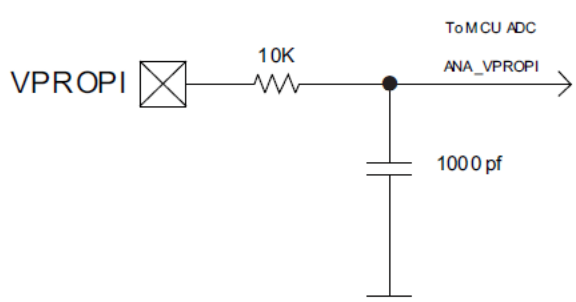


Figure 7-3. RC Network in Series With the VPROPI Output

It is imperative to realize that VPROPI will decrease to 0 V while the H-Bridge enters slow decay recirculation.

7.3.8 Protection Circuits

The DRV8801-Q1 device is fully protected against V_{BB} undervoltage, overcurrent, and overtemperature events.

Table 7-2. DRV8801-Q1 Fault Responses

FAULT	ERROR REPORT	H-BRIDGE	CHARGE PUMP	RECOVERY
V_{BB} undervoltage (UVLO)	No error report – nFAULT is hi-Z	Disabled	Shut Down	V_{BB} > VUVLO RISING
Overcurrent (OCP)	nFAULT pulled low	Disabled	Operating	Retry time, $t_{(OCP)}$
Overtemperature Warning (OTW)	nFAULT pulled low	Enabled	Operating	$T_J < T_{(OTW)} – T_{hys(OTW)}$
Overtemperature Shutdown (OTS)	nFAULT remains pulled low (set during OTW)	Disabled	Shut Down	$T_J < T_{(OTS)} – T_{hys(OTS)}$

7.3.8.1 V_{BB} Undervoltage Lockout (UVLO)

If at any time the voltage on the V_{BB} pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled and the charge pump is disabled. The nFAULT pin does not report the UVLO fault condition and remains hi-Z. Operation resumes when V_{BB} rises above the UVLO threshold.

7.3.8.2 Overcurrent Protection (OCP)

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, all FETs in the H-bridge are disabled, nFAULT is driven low, and a $t_{(OCP)}$ fault timer is started. After this period, $t_{(OCP)}$, the device is then allowed to follow the input commands and another turn-on is attempted (nFAULT releases during this attempt). If there is still a fault condition, the cycle repeats. If the short condition is not present after $t_{(OCP)}$ expires, normal operation resumes and nFAULT is released.

7.3.8.3 Overtemperature Warning (OTW)

If the die temperature increases past the thermal warning threshold the nFAULT pin is driven low. When the die temperature has fallen below the hysteresis level, the nFAULT pin is released. If the die temperature continues to increase, the device enters overtemperature shutdown as described in the *Section 7.3.8.4* section.

7.3.8.4 Overtemperature Shutdown (OTS)

If the die temperature exceeds the thermal shutdown temperature, all FETs in the H-bridge are disabled and the charge pump shuts down. The nFAULT pin remains pulled low during this fault condition. When the die temperature falls below the hysteresis threshold, operation automatically resumes.

7.3.9 Thermal Shutdown (TSD)

Two die-temperature monitors are integrated on the chip. As die temperature increases toward the maximum, a thermal warning signal is triggered at 160°C. This fault drives nFAULT low, but does not disable the operation of the chip. If the die temperature increases further, to approximately 175°C, the full-bridge outputs are disabled until the internal temperature falls below a hysteresis of 15°C.

7.4 Device Functional Modes

The DRV8801-Q1 device is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled and the H-bridge FETs are disabled hi-Z. The DRV8801-Q1 device is brought out of sleep mode automatically if nSLEEP is brought logic high.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8801-Q1 device is used in medium voltage brushed DC motor control applications.

8.2 Typical Application

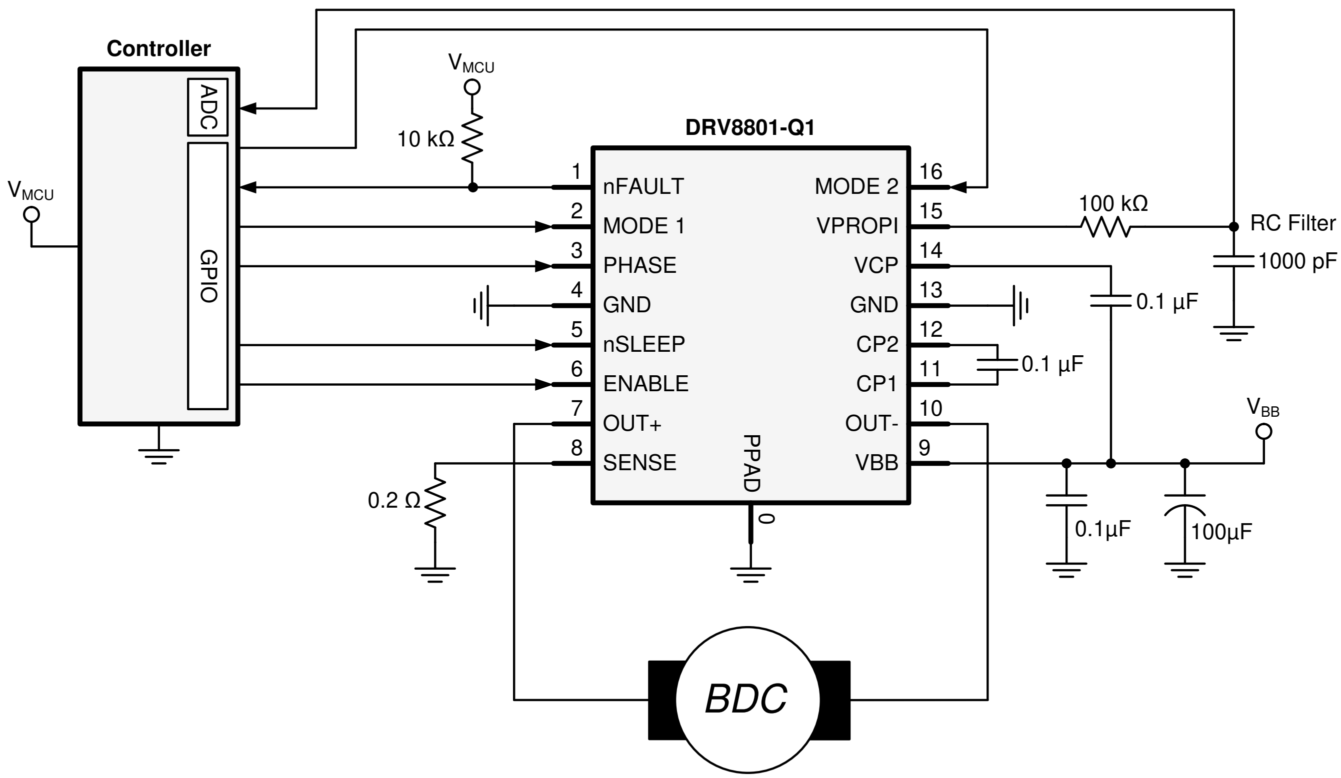


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor Voltage	VBB	24 V
Motor RMS Current	IRMS	0.8 A
Motor Startup Current	ISTART	2 A
Motor Current Trip Point	ITRIP	2.5 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Power Dissipation

The power dissipation of the DRV8801-Q1 is a function of the RMS motor current and the each output's FET resistance ($R_{DS(ON)}$).

$$\text{Power} \approx I_{RMS}{}^{2} \times (\text{High-Side } R_{DS(ON)} + \text{Low-Side } R_{DS(ON)}) \tag{3}$$

For this example, the ambient temperature is 35°C, and the junction temperature reaches 65°C. At 65°C, the sum of RDS(ON) is about 1 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat will be 0.8 A^2x 1 Ω = 0.64 W.

The temperature that the DRV8801-Q1 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device thermal pad to the PCB ground plane, with vias to the top and bottom board layers, to dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8801-Q1 had an effective thermal resistance $R_{\theta JA}$ of 47°C/W, and:

$$T_J = T_A + (P_D \times R_{\theta JA}) = 35°C + (0.64\ W \times 47°C/W) = 65°C \tag{4}$$

8.2.2.3 Thermal Considerations

Although DRV8801-Q1 is rated at 2.8-A of current handling, the previous only holds true as long as the internal temperature does not exceed 170°C. In order to operate at this rate, the following measures must be taken under consideration.

8.2.2.3.1 Junction-to-Ambiant Thermal Impedance (ϴJA)

At any given time during the steady state portion of the cycle, two FETs are enabled: A high side sourcing FET and a low side sinking FET. The increase in die temperature above ambient can be estimated by Equation 5

$$T_{die} = \theta_{JA} \frac{°C}{W} \times I_{winding}{}^{2} \times RDS_{ON} + T_A \tag{5}$$

8.2.2.4 Motor Current Trip Point

When the voltage on pin SENSE exceeds V_{TRIP} (0.5 V), overcurrent is detected. The R_{SENSE} resistor should be sized to set the desired I_{TRIP} level.

$$R_{SENSE} = 0.5\ V / I_{TRIP} \tag{6}$$

To set I_{TRIP} to 2.5 A, R_{SENSE} = 0.5 V / 2.5 A = 0.2 Ω.

To prevent false trips, I_{TRIP} must be higher than regular operating current. Motor current during startup is typically much higher than steady-state spinning, because the initial load torque is higher, and the absence of back-EMF causes a higher voltage and extra current across the motor windings.

It is beneficial to limit startup current by using series inductors on the DRV8801-Q1 output, as that allows I_{TRIP} to be lower, and it may decrease the system's required bulk capacitance. Startup current can also be limited by ramping the forward drive duty cycle.

8.2.2.5 Sense Resistor Selection

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance

- Rated for high enough power
- Placed closely to the motor driver

8.2.2.6 Drive Current

This current path is through the high-side sourcing DMOS driver, motor winding, and low-side sinking DMOS driver. Power dissipation I^2R losses in one source and one sink DMOS driver, as shown in Equation 7.

$$P_D = I^2(r_{DS(on)Source} + r_{DS(on)Sink}) \tag{7}$$

8.2.3 Pulse-Width Modulating

8.2.3.1 Pulse-Width Modulating ENABLE

The most common H-Bridge direction/speed control scheme is to use a conventional GPIO output for the PHASE (selects direction) and pulse-width modulate ENABLE for speed control.

8.2.3.2 Pulse-Width Modulating PHASE

A technique that uses a speed/direction control scheme where ENABLE is connected to a GPIO output and the PHASE is pulse-width modulated. In this case, both direction and speed are controlled with a single signal. ENABLE is only used to disable the motor and stop all current flow.

When pulse-width modulating PHASE, a 50% duty cycle will stop the motor. Duty cycles above 50% will have the motor moving on the clockwise direction with proportional control; 100% duty cycle represents full speed.

Duty cycles below 50% will have the motor rotating with a counter clockwise direction; 0% duty cycle represents full speed.

8.2.4 Application Curves

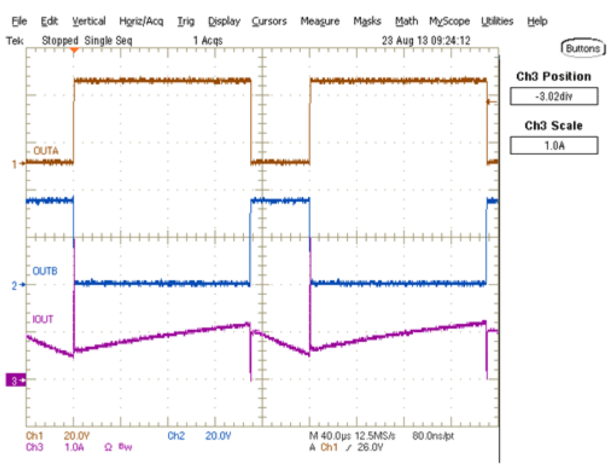


Figure 8-2. Forward Drive, Fast Decay

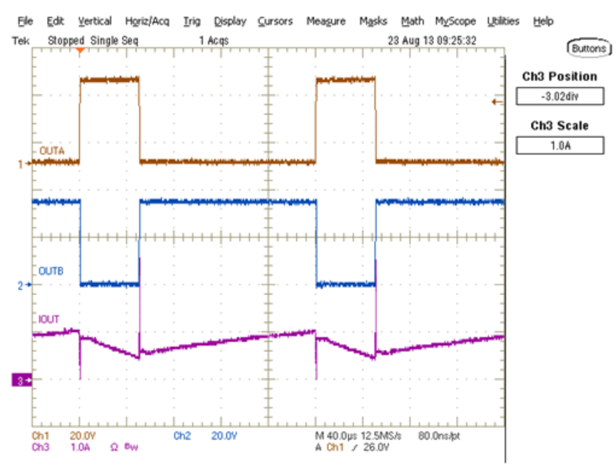


Figure 8-3. Reverse Drive, Fast Decay

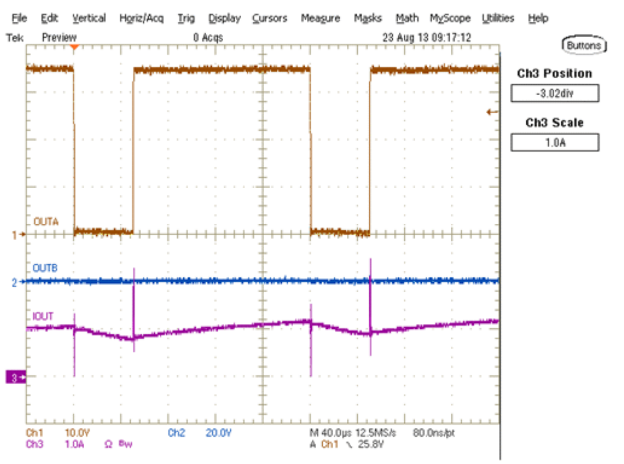


Figure 8-4. Forward Drive, Slow Decay

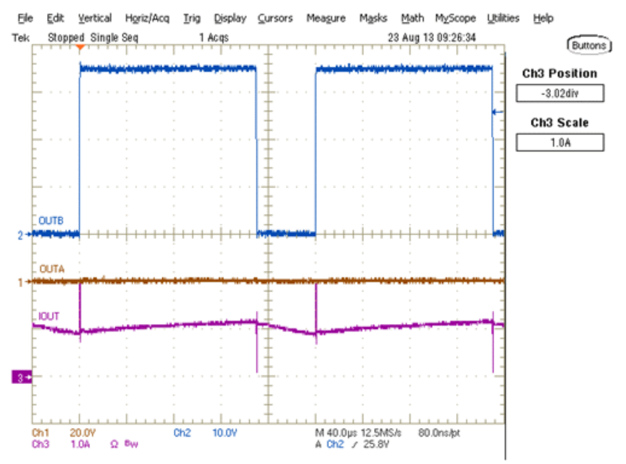


Figure 8-5. Reverse Drive, Slow Decay

8.3 Parallel Configuration

It is possible to drive higher than the 2.8 A of current by connecting more than one devices in parallel. To properly use this option the guidelines documented below must be followed.

8.3.1 Parallel Connections

Figure 8-6 shows the signals that need to be connected together. ENABLE, PHASE, MODE 1, MODE 2, nSLEEP, OUT+, OUT-, SENSE, VBB and GND.

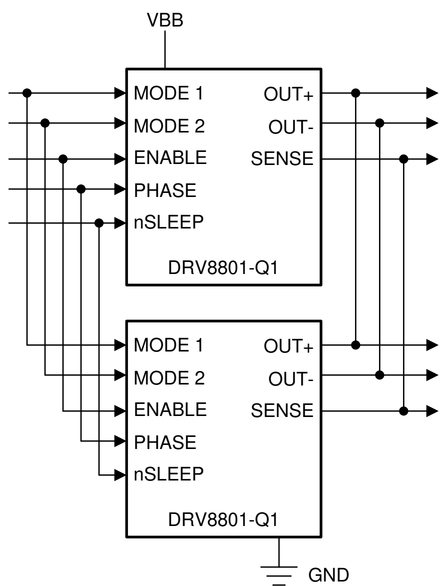


Figure 8-6. Functional Block Diagram (Connected Signals)

8.3.2 Non – Parallel Connections

Figure 8-7 shows the signals that should not be connected together and will be driven on an individual basis. These are: VCP, CP1, CP2, and VPROPI.

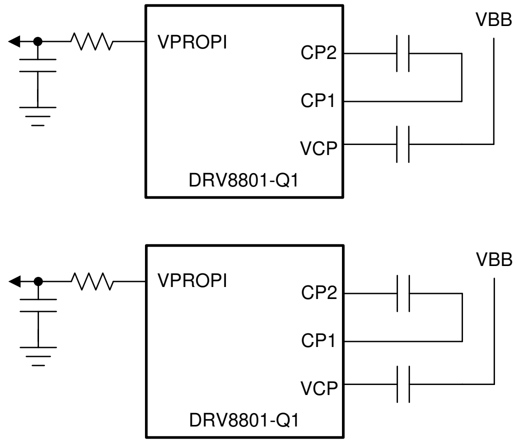


Figure 8-7. Functional Block Diagram (Individual Signals)

8.3.3 Wiring nFAULT as Wired OR

Since nFAULT is an open drain output, multiple nFAULT outputs can be paralleled with a single resistor. The end result is a wired OR configuration. When any individual nFAULT output goes to a logic low, the wired OR output will go to the same logic low. There is no need to determine which device signaled the fault condition, as once they are connected in parallel they function as a single device.

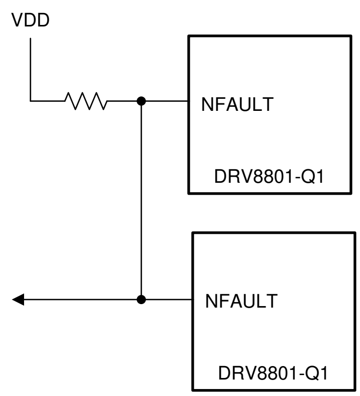


Figure 8-8. nFAULT as Wired OR

8.3.4 Electrical Considerations

8.3.4.1 Device Spacing

It is recommended that devices be connected as close as possible and with trace lengths as short as possible. Doing this minimizes the potential of generating timing differences between devices. Although it may seem like a harmful situation for the power stage, DRV8801-Q1 contains enough protection to effectively deal with enable time skews from device to device. This consideration focuses on motion quality, as total current needed for acceleration and proper speed control will only be available when all power stages are brought online.

8.3.4.2 Recirculation Current Handling

During recirculation, it is not possible to synchronize all devices connected in parallel so that the current is equally distributed. Also, during the asynchronous portion of the current decay, the body diode with the lowest forward voltage will start conducting and sink all of the current. Said body diode is not meant to handle the new increased current capacity and will be severely affected if allowed to sink current of said magnitude.

In order to assure proper operation when devices are connected in parallel, it is imperative that external schottky diodes be used. These schottky diodes will conduct during the asynchronous portion of the recirculation mode and will sink the inductive load current until the respective FET switches are brought online.

Schottky diodes should be connected as shown in Figure 8-9.

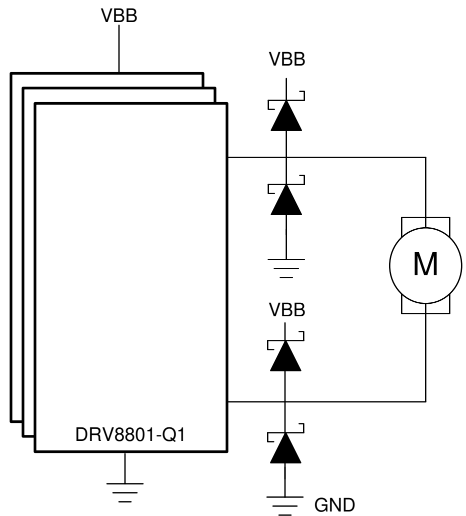


Figure 8-9. Schottky Diodes Connection

8.3.4.3 Sense Resistor Selection

The guideline for the SENSE resistor chosen doesn't change in parallel mode. As the goal of this configuration is to evenly distribute the current load across multiple devices, each device should be configured with the same I_{TRIP} setting. Therefore, the same SENSE resistor should be used for all devices connected in parallel.

Connection of the SENSE resistors should be as shown in Figure 8-10.

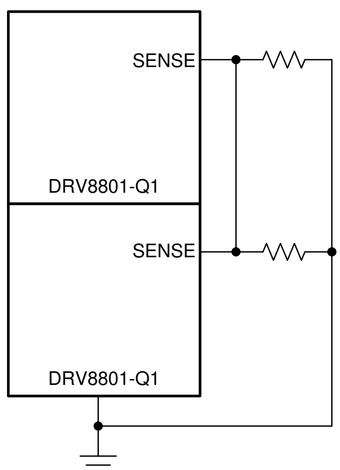


Figure 8-10. SENSE Resistors Connection

8.3.4.4 Maximum System Current

The idea behind placing multiple devices in parallel is to increase maximum drive current. At first glance, it may seem that the new increased I_{TRIP} setting is given by Equation 8.

$$\text{System}I_{TRIP} = \left(I_{TRIP} \times N\right) \tag{8}$$

Where:

N is the number of devices connected in parallel.

I_{TRIP} is the individual I_{TRIP} value per device.

However, although in theory accurate, due to tolerances in internal SENSE amplifier/comparator circuitry, the system I_{TRIP} should be expected to be less than the addition of all the individual I_{TRIP}. The reason for this is that as soon as one of the devices senses a current for which the H Bridge should be disabled, the remaining devices will end up having to conduct the same current but with less capacity. Therefore, remaining devices are expected to get disabled shortly after.

A good rule of thumb is to expect 90% of the theoretical maximum.

By way of example, if the system level requirements indicate that 6 A of current are required to meet the motion control requirements, then:

6 A = (2.8 A x 0.9)N

N = (6 A) / (2.8 A x 0.9)

N = 2.38

In this example, three devices would be required to safely meet the needs of the system.

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The capacitance of the power supply and its ability to source current.
- The amount of parasitic inductance between the power supply and motor systems.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

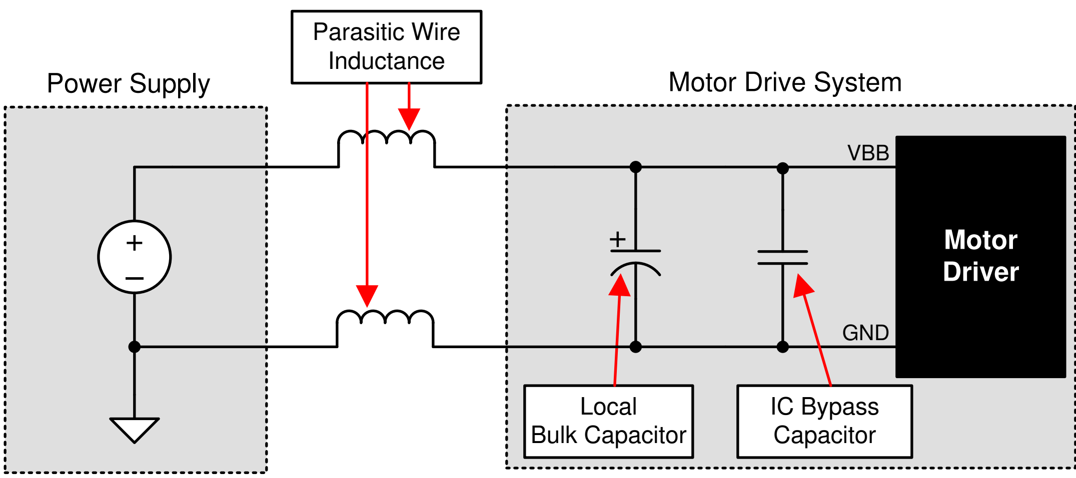


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

- The printed-circuit-board (PCB) should use a heavy ground plane. For optimal electrical and thermal performance, the DRV8801-Q1 must be soldered directly onto the board. On the underside of the DRV8801-Q1 is a thermal pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.
- The load supply pin VBB, should be decoupled with an electrolytic capacitor (typically 100 µF) in parallel with a ceramic capacitor (0.1 µF) placed as close as possible to the device.
- The ceramic capacitors (0.1 µF) between VCP and VBB and between CP1 and CP2 should be placed as close as possible to the device.
- The SENSE resistor should be close as possible to the SENSE pin and ground return to minimize parasitic inductance.

10.2 Layout Example

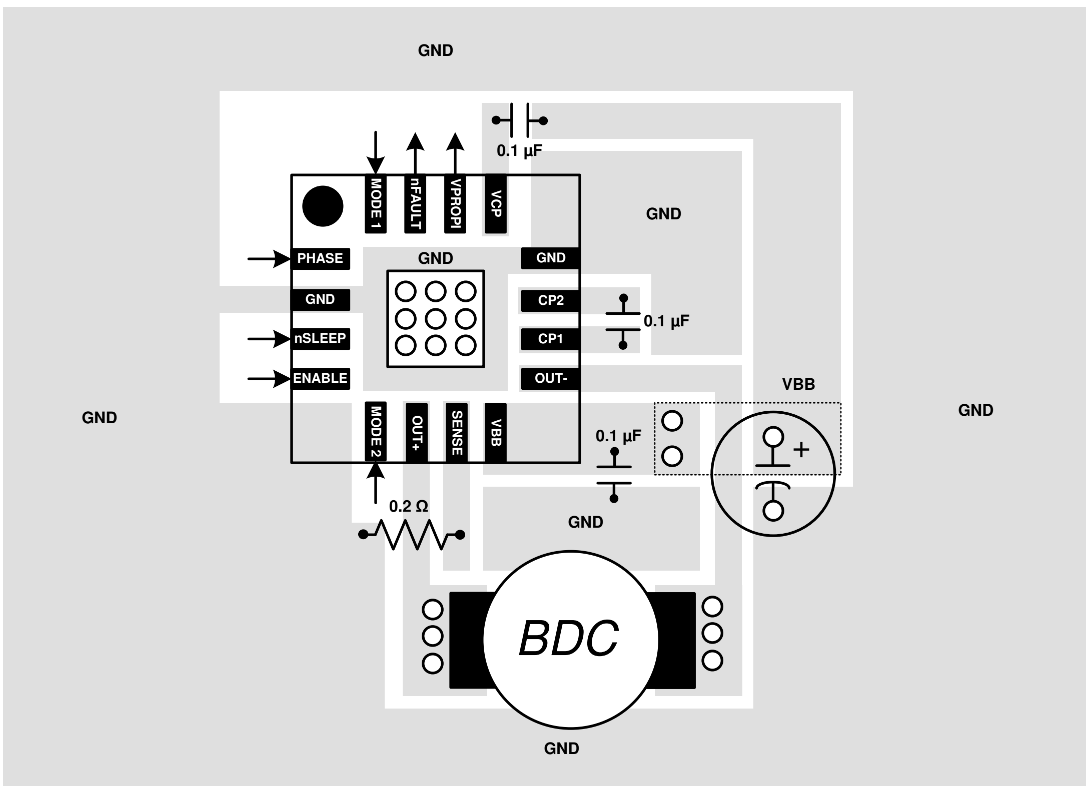


Figure 10-1. RTY Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

QFN/SON PCB Attachment

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8801QRTYRQ1	Active	Production	QFN (RTY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV 8801Q
DRV8801QRTYRQ1.A	Active	Production	QFN (RTY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV 8801Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

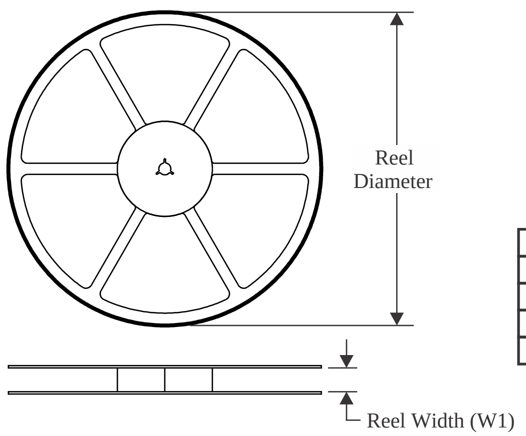
OTHER QUALIFIED VERSIONS OF DRV8801-Q1 :

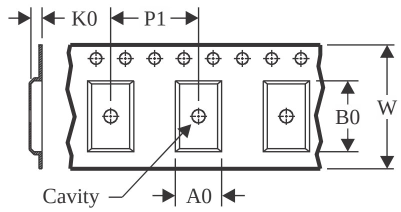
- Catalog : DRV8801

NOTE: Qualified Version Definitions:

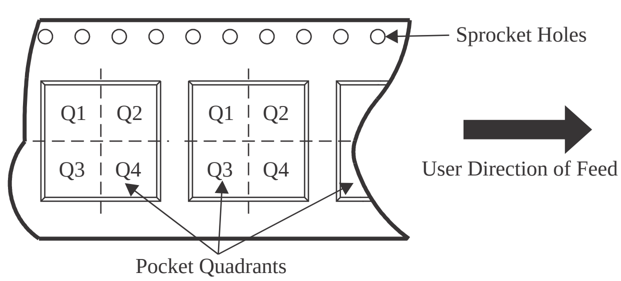
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





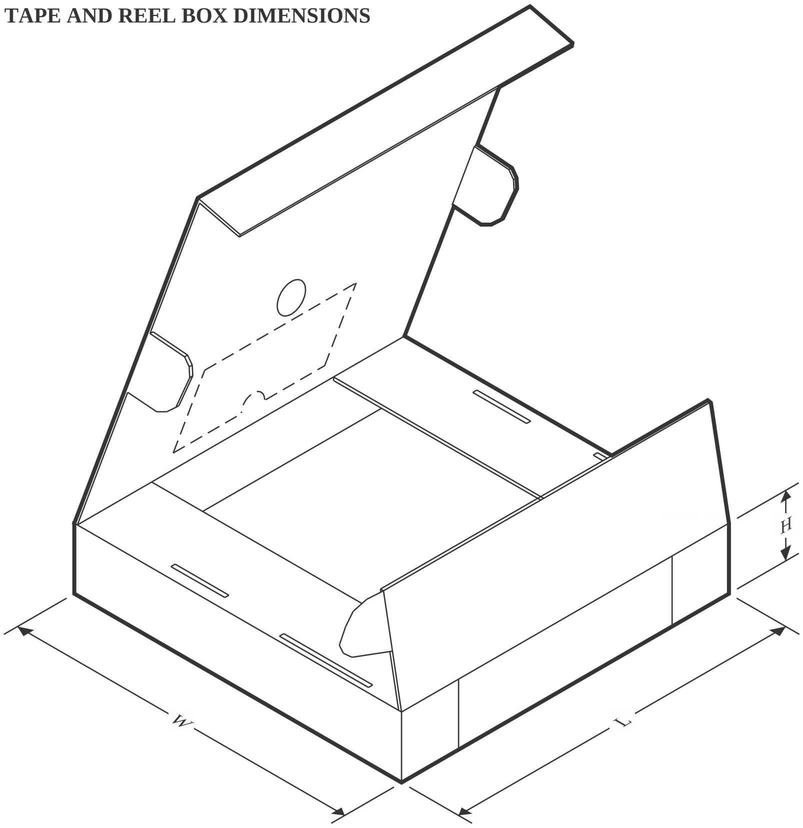
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8801QRTYRQ1	QFN	RTY	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

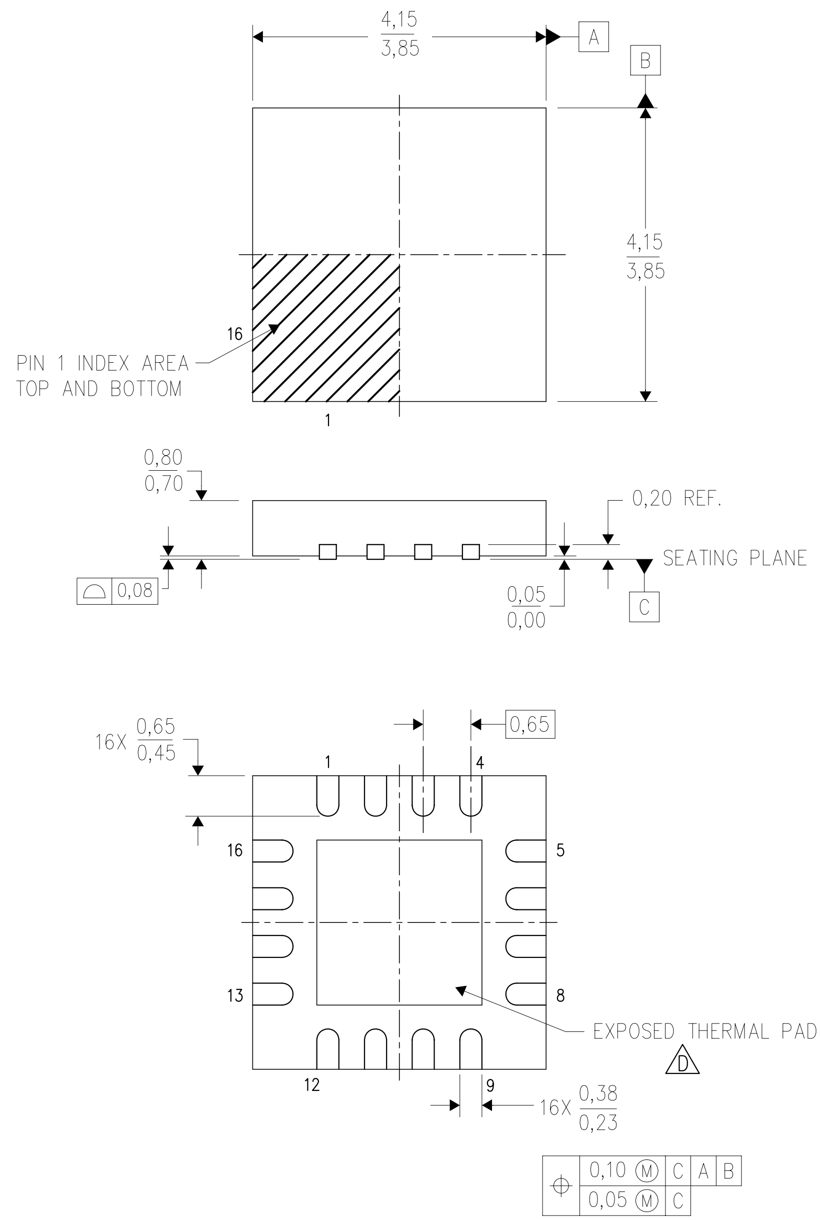
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8801QRTYRQ1	QFN	RTY	16	3000	356.0	356.0	35.0

RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

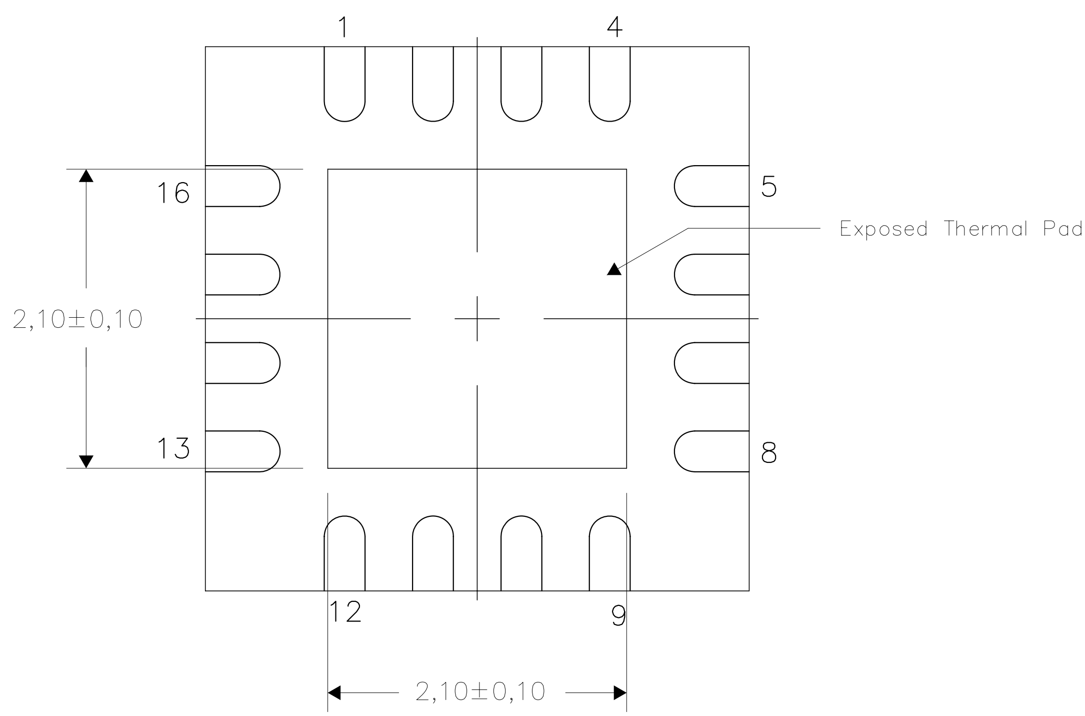
RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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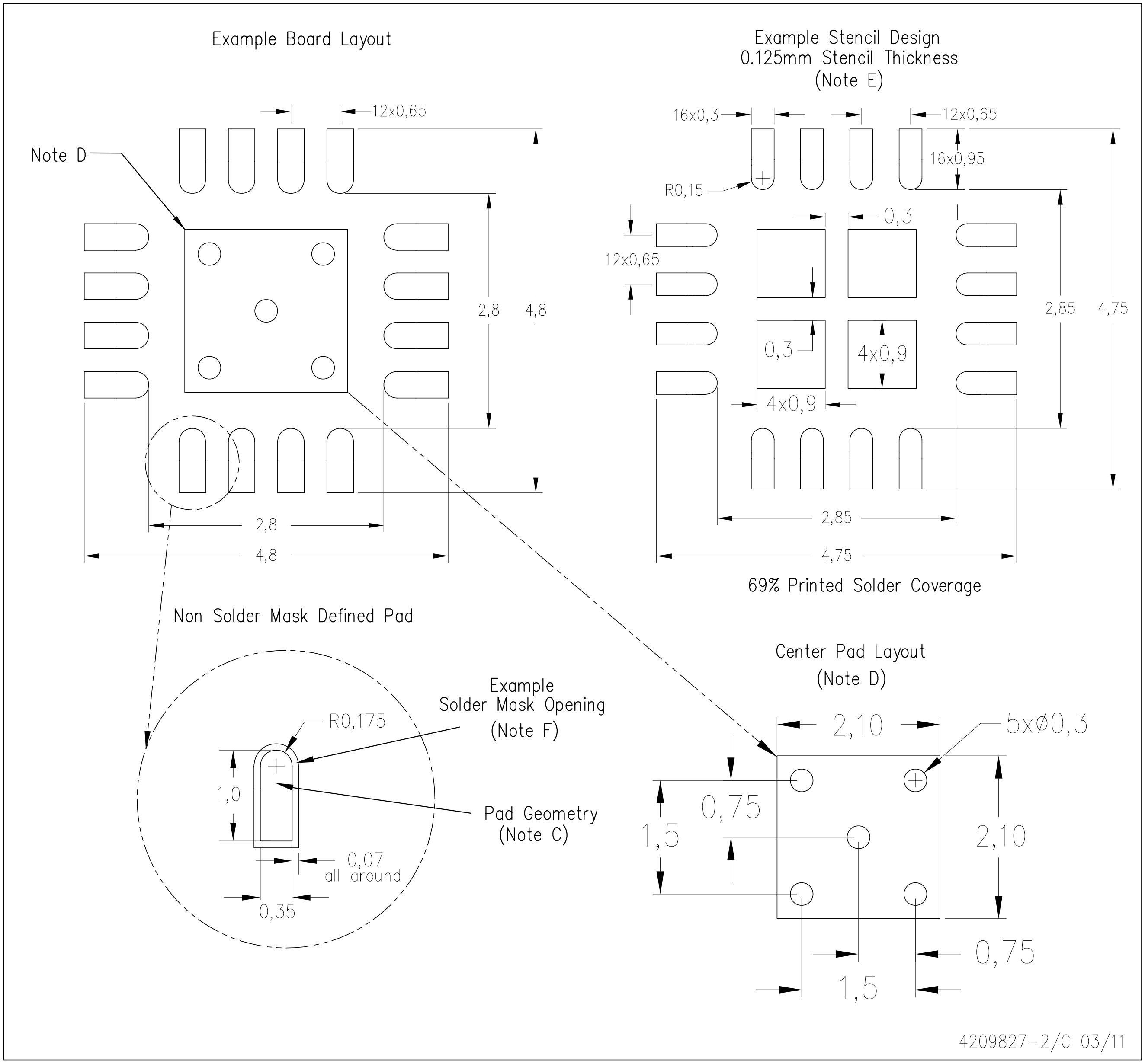
NOTE: A. All linear dimensions are in millimeters

RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265