DRV8452: 55 V, 5 A Stepper Motor Driver for High Efficiency and Noiseless Operation

1 Features

- Stepper motor driver
  - SPI or H/W interface with STEP/DIR pins
  - Up to **1/256** microstepping indexer
- **4.5 V to 55 V** operating supply voltage range
  - Supports standard 24 V and 36 V rails
- Low $R_{DS(ON)}$: **100 mΩ** HS + LS at 24 V, 25°C
- High current capacity per bridge:
  - DDW Package: **5 A** full-scale, 3.5A RMS
  - PWP Package: **4 A** full-scale, 2.8A RMS
- DDW package **pin-to-pin compatible** with -
  - DRV8462/61: 65 V, 3-10A
- PWP package **pin-to-pin compatible** with -
  - SPI: DRV8434S: 48 V, 2.5 A
  - H/W Interface: DRV8424/26: 33 V, 1.5-2.5 A
- Integrated current sensing and regulation
  - **5%** full-scale current accuracy
- Smart tune and mixed decay regulation options
- **Silent step** decay mode for silent operation at standstill and low speed
- **Automatic Microstepping** mode for step frequency interpolation
- **Customizable microstepping** indexer table
- **Auto-torque** for load dependent current control
- **Standstill Power Saving** mode
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (3 µA)
- Separate logic supply voltage (**VCC**)
- Protection and diagnostic features
  - Sensorless **Stall Detection**
  - VM undervoltage lockout (UVLO)
  - Open-load detection (OL)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)
  - Indexer zero position output (**nHOME**)

2 Applications

- Textile Machines, Sewing machines
- Factory Automation, Stepper Drives and Robotics
- Medical Imaging, Diagnostics and Equipment
- Stage Lighting
- ATMs, Currency Counters
- PLC, DCS & PAC
- Multifunction Printers
- 3D Printer
- Outdoor IP Camera

3 Description

The DRV8452 is a wide-voltage, high-power, high-performance stepper motor driver. The device supports up to 55-V supply voltage, and integrated MOSFETs with 100 mΩ HS + LS on-resistance allow up to 5-A current.

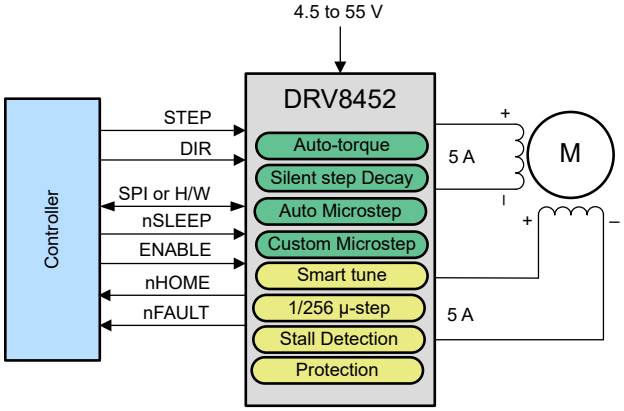
The auto-torque feature boosts efficiency by adjusting the current according to load torque. Standstill power saving mode reduces power loss during motor holding condition. Silent step guarantees noiseless operation at low speeds and standstill. Internal current sense eliminates the need for sense resistors, therefore saving PCB area and cost. Built-in indexer supports up to 1/256 microstepping, and the automatic microstepping mode interpolates the input STEP signal to reduce overhead on the controller. Sensorless stall detection eliminates end stops from the system. The device supports other protection and diagnostic features for robust and reliable operation.

The DRV8452 requires minimal tuning to configure the features. It supports higher power density than external FET drivers, with a smaller PCB area. High energy efficiency coupled with precise, noiseless operation makes the DRV8452 an ideal choice for high-performance stepper systems.

Device Information

Part Number	Interface	Package(1)	Body Size
DRV8452DDWR	SPI or H/W	HTSSOP (44)	14 x 6.1 mm
DRV8452SPWPR	SPI	HTSSOP (28)	9.7 x 4.4 mm
DRV8452PWPR	H/W	HTSSOP (28)	9.7 x 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2022) to Revision B (October 2023)	Page
• Increased voltage rating 48 V has been replaced by 55 V and 50 V has been replaced by 60 V.	1
• PWP package has moved to production data.	1

Changes from Revision * (August 2022) to Revision A (December 2022)	Page
• Updated device status to "Production Data" from "Advanced Information"	1

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5 Pin Configuration and Functions

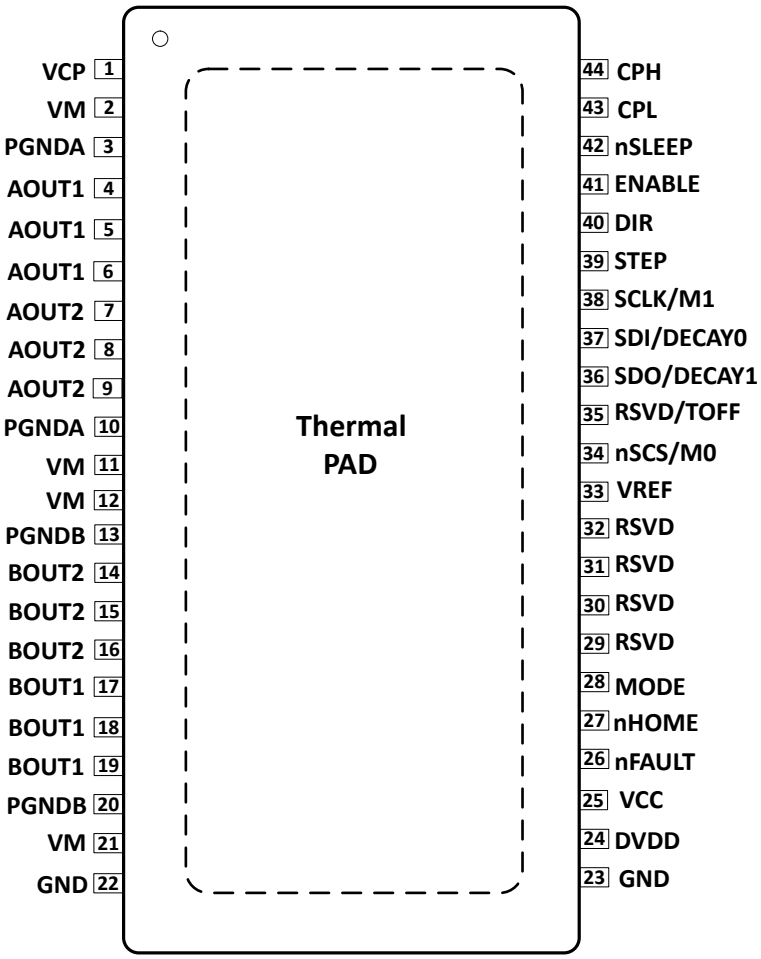

Figure 5-1. DDW Package (44-Pin HTSSOP), Top View

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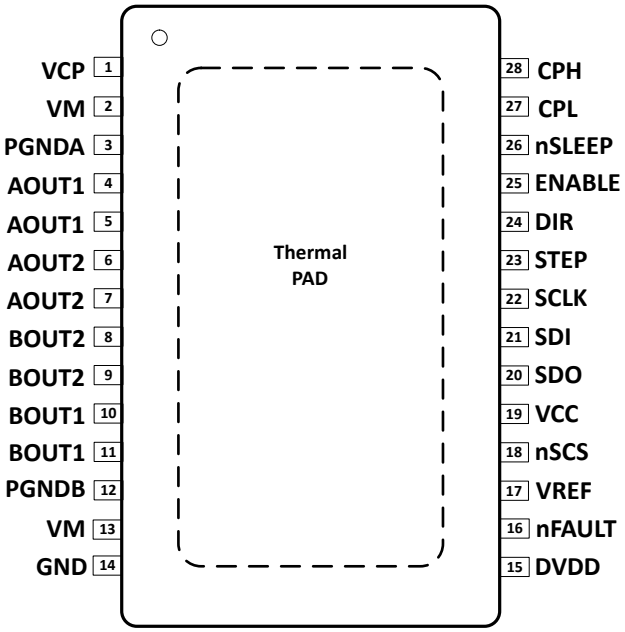

Figure 5-2. PWP Package (28-Pin HTSSOP) with SPI Interface, Top View

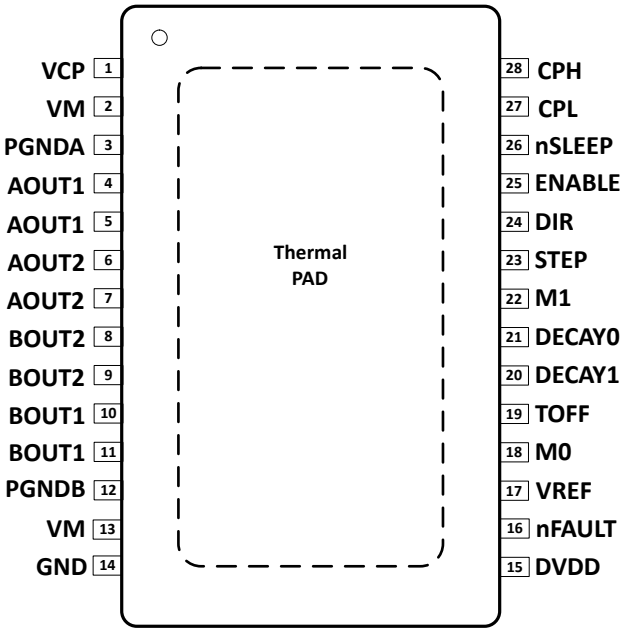

Figure 5-3. PWP Package (28-Pin HTSSOP) with H/W Interface, Top View

Table 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DDW	PWP			
		SPI Interface	H/W Interface		
VCC	25	19	-	Power	Supply voltage for internal logic blocks. When separate logic supply voltage is not available, tie the VCC pin to the DVDD pin. When configured with SPI interface, the VCC pin also acts as the supply pin for SDO output. See Section 7.3.16 for details.

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Table 5-1. Pin Functions (continued)

PIN				TYPE	DESCRIPTION
NAME	DDW	PWP			
		SPI Interface	H/W Interface		
RSVD/TOFF	35	-	19	Input	This pin is not used with SPI interface. With H/W interface, this pin programs the OFF time for PWM current regulation.
VCP	1	1		Power	Charge pump output. Connect a X7R, 1-µF, 16-V ceramic capacitor from VCP to VM.
VM	2, 11, 12, 21	2, 13		Power	Power supply. Connect to motor supply voltage and bypass to PGNDA and PGNDB with two 0.01-µF ceramic capacitors plus a bulk capacitor rated for VM.
PGNDA	3, 10	3		Power	Power ground. Connect to system ground.
PGNDB	13, 20	12		Power	Power ground. Connect to system ground.
AOUT1	4, 5, 6	4, 5		Output	Winding A output. Connect to motor winding.
AOUT2	7, 8, 9	6, 7		Output	Winding A output. Connect to motor winding.
BOUT2	14, 15, 16	8, 9		Output	Winding B output. Connect to motor winding.
BOUT1	17, 18, 19	10, 11		Output	Winding B output. Connect to motor winding.
GND	22, 23	14		Power	Device ground. Connect to system ground.
DVDD	24	15		Power	Internal LDO output. Connect a X7R, 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
nFAULT	26	16		Open Drain	Fault indication output. Pulled logic low with fault condition. Open-drain nFAULT requires an external pullup resistor.
nHOME	27	-		Open Drain	Pulled logic low when the internal indexer is at home position (45°) of step table. The nHOME pin outputs one low pulse per 360º electrical rotation (four fullsteps). See Section 7.3.5.1 for details. Only available with DDW package.
MODE	28	-		Input	MODE pin programs the device to operate with either SPI or hardware (H/W) pin interface. See Section 7.3.1 for details.
RSVD	29, 30, 31, 32	-		-	Reserved. Leave unconnected.
VREF	33	17		Input	Voltage reference input for setting full-scale current. DVDD can be used to generate VREF through a resistor divider. When configured with SPI interface, the VREF pin can be left unconnected if VREF_INT_EN bit is 1b.
nSCS/M0	34	18		Input	With SPI interface, this pin acts as serial chip select. An active low on this pin enables the serial interface communications. With H/W interface, this pin programs the microstepping mode.
SDO/ DECAY1	36	20		Push-Pull/Input	With SPI interface, this pin acts as serial data output. Data is shifted out on the rising edge of the SCLK pin. With H/W interface, this pin programs the decay-mode.
SDI/DECAY0	37	21		Input	With SPI interface, this pin acts as serial data input. Data is captured on the falling edge of the SCLK pin. With H/W interface, this pin programs the decay-mode.
SCLK/M1	38	22		Input	With SPI interface, this pin acts as serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. With H/W interface, this pin programs the microstepping mode.
STEP	39	23		Input	Step input. An active edge causes the indexer to advance one step. With SPI interface, STEP active edge can be either rising edge or both rising and falling edge. With H/W interface, STEP active edge is always the rising edge.
DIR	40	24		Input	Direction input. Logic level sets the direction of stepping.

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Table 5-1. Pin Functions (continued)

PIN				TYPE	DESCRIPTION
NAME	DDW	PWP			
		SPI Interface	H/W Interface		
ENABLE	41	25		Input	Logic low to disable device outputs; logic high to enable. When the device operates with H/W interface, the ENABLE pin also determines the OCP, OL and OTSD fault recovery methods.
nSLEEP	42	26		Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. A narrow nSLEEP reset pulse clears latched faults.
CPL	43	27		Power	Charge pump switching node. Connect a X7R, 0.1-µF, VM-rated ceramic capacitor from CPH to CPL.
CPH	44	28		Power	
PAD	-	-		-	Thermal pad. Connect to system ground.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	60	V
Charge pump voltage (VCP, CPH)	-0.3	V_{VM} + 5.75	V
Charge pump negative switching pin (CPL)	-0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
External logic supply (VCC)	-0.3	5.75	V
Control pin voltage	–0.3	5.75	V
Reference input pin voltage (VREF)	–0.3	5.75	V
PGNDx to GND voltage	-0.5	0.5	V
PGNDx to GND voltage, < 1 µs	-2.5	2.5	V
Open drain output current (nFAULT, nHOME)	0	10	mA
Continuous Output pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns Output pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

1. *Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*
2. *All voltage values are with respect to network ground terminal GND.*

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	Corner pins	±750	
			Other pins	±500	

(1) *JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.*
(2) *JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.*

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	55	V
V_I	Logic level input voltage	0	5.5	V
V_{VCC}	VCC pin voltage	3.05	5.5	V
V_{REF}	Reference voltage (VREF)	0.05	3.3	V
f_{STEP}	Applied STEP signal (STEP)	0	100 (1)	kHz

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6.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
I_{FS}	Motor full-scale current with DDW package (xOUTx)	0	5 (2)	A
I_{FS}	Motor full-scale current with PWP package (xOUTx)	0	4 (2)	A
I_{RMS}	Motor RMS current with DDW package (xOUTx)	0	3.5 (2)	A
I_{RMS}	Motor RMS current with PWP package (xOUTx)	0	2.8 (2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

1. *STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.*
2. *Power dissipation and thermal limits must be observed.*

6.4 Thermal Information

THERMAL METRIC		DDW	PWP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.5	24.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.8	13.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.9	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.8	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	0.9	°C/W

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load, VCC = External 5V		5	8.5	mA
		ENABLE = 1, nSLEEP = 1, No motor load, VCC = DVDD		8	12	
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		3	8	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	H/W interface, nSLEEP = 1 to output transition		0.85	1.2	ms
		SPI interface, nSLEEP = 1 to SPI ready		0.15	0.25	ms
t_{ON}	Turn-on time(1)	VM > UVLO to output transition		1	1.3	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 55 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.35	4.45		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 55 V		V_{VM} + 5		V
f_{VCP}	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		357		kHz
f_{CLK}	Internal digital clock frequency	V_{VM} > UVLO; nSLEEP = 1		10		MHz

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC-LEVEL INPUTS (STEP, DIR, MODE, DECAY1, nSCS, SCLK, SDI, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage (all pins except DECAY1)		1.5		5.5	V
V_{IH_DECAY1}	Input logic-high voltage (DECAY1 pin)		2.7		5.5	V
V_{HYS}	Input logic hysteresis (all pins except nSLEEP)			100		mV
V_{HYS_SLEEP}	nSLEEP logic hysteresis			300		mV
I_{IL}	Input logic-low current (all pins except nSCS)	V_{IN} = 0 V	–1		1	µA
I_{IL_nSCS}	nSCS logic-low current	nSCS = 0V	8		12	µA
I_{IH}	Input logic-high current (all pins except nSCS, 200k internal pull-down resistance)	V_{IN} = DVDD			50	µA
I_{IH_nSCS}	nSCS logic-high current	nSCS = DVDD			0.1	µA
TRI-LEVEL INPUTS (M0, DECAY0, ENABLE)						
V_{I1_tri}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2_tri}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3_tri}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_{O_tri}	Output pull-up current			10.5		µA
QUAD-LEVEL INPUTS (M1, TOFF)						
V_{I1_quad}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2_quad}	Input second level voltage	330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3_quad}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4_quad}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_{O_quad}	Output pull-up current			10.5		µA
PUSH-PULL OUTPUT (SDO)						
$R_{PD,SDO}$	Internal pull-down resistance	5mA load, with respect to GND		30	70	Ω
$R_{PU,SDO}$	Internal pull-up resistance	5mA load, with respect to VCC		60	110	Ω
I_{SDO}	SDO Leakage Current[(1)]	V_{VM} > 6 V, SDO = VCC and 0V	-2.5		2.5	µA
CONTROL OUTPUTS (nFAULT, nHOME)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.35	V
I_{OH}	Output logic-high leakage		-1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH,DDW)}$	High-side FET on resistance, DDW Package	T_J = 25 °C, I_O = -5 A		53	60	mΩ
		T_J = 125 °C, I_O = -5 A		80	94	mΩ
		T_J = 150 °C, I_O = -5 A		90	105	mΩ
$R_{DS(ONL,DDW)}$	Low-side FET on resistancec, DDW Package	T_J = 25 °C, I_O = 5 A		53	60	mΩ
		T_J = 125 °C, I_O = 5 A		80	94	mΩ
		T_J = 150 °C, I_O = 5 A		90	105	mΩ

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ONH,PWP)}$	High-side FET on resistance, PWP Package	T_J = 25 °C, I_O = -4 A		57	68	mΩ
		T_J = 125 °C, I_O = -4 A		76	100	mΩ
		T_J = 150 °C, I_O = -4 A		86	112	mΩ
$R_{DS(ONL,PWP)}$	Low-side FET on resistance, PWP Package	T_J = 25 °C, I_O = 4 A		60	72	mΩ
		T_J = 125 °C, I_O = 4 A		81	105	mΩ
		T_J = 150 °C, I_O = 4 A		90	116	mΩ
I_{LEAK}	Output leakage current to ground in Disable mode[1]	H-bridges are Hi-Z, V_{VM} = 55 V			200	µA
t_{RF}	Output rise/fall time	H/W Interface, I_O = 5 A, between 10% and 90%		140		ns
		SPI Interface, SR = 0b, I_O = 5 A, between 10% and 90%		140		
		SPI Interface, SR = 1b, I_O = 5 A, between 10% and 90%		70		
t_D	Output dead time	VM = 24V, I_O = 5 A		300		ns
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain	VREF = 3.3 V	0.625	0.66	0.695	V/A
I_{VREF}	VREF Pin Leakage Current	VREF = 3.3 V			20	nA
t_{OFF}	PWM off-time	TOFF = 0 or TOFF = 00b		9		µs
		TOFF = 1 or TOFF = 01b		19		
		TOFF = Hi-Z or TOFF = 10b		27		
		TOFF = 330kΩ to GND or TOFF = 11b		35		
ΔI_{TRIP_EXT}	Current trip accuracy, external VREF input	10% to 20% full-scale current	-12		12	%
		20% to 40% full-scale current	-7.5		7.5	
		40% to 100% full-scale current	-5		5	
ΔI_{TRIP_INT}	Current trip accuracy, internal VREF	10% to 20% full-scale current	-12		12	%
		20% to 40% full-scale current	-8		8	
		40% to 100% full-scale current	-6		5	
$I_{O,CH}$	AOUT and BOUT current matching	100% full-scale current	-2.5		2.5	%
t_{BLK}	Current regulation blanking time	SPI interface, TBLANK_TIME = 00b		1		µs
		H/W interface or SPI interface, TBLANK_TIME = 01b		1.5		
		SPI interface, TBLANK_TIME = 10b		2		
		SPI interface, TBLANK_TIME = 11b		2.5		
t_{DEG}	Current regulation deglitch time			0.5		µs
PROTECTION CIRCUITS						
VM_{UVLO}	VM UVLO lockout	VM falling	4.1	4.23	4.35	V
		VM rising	4.2	4.35	4.47	

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC_{UVLO}	VCC UVLO lockout	VCC connected to external voltage, VCC falling	2.7	2.8	2.9	V
		VCC connected to external voltage, VCC rising	2.75	2.92	3.05	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		110		mV
V_{RST}	VM UVLO reset	VCC = DVDD, SPI Interface, VM falling, device reset, no SPI communications			3.4	V
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	7.6			A
t_{OCP}	Overcurrent detection delay	H/W Interface		2.2		µs
		SPI Interface, TOCP = 0b		1.2		
		SPI Interface, TOCP = 1b		2.2		
t_{RETRY}	Overcurrent retry time			4.1		ms
t_{OL}	Open load detection time	H/W Interface			60	ms
		SPI Interface, OL_T = 00b			30	
		SPI Interface, OL_T = 01b			60	
		SPI Interface, OL_T = 10b			120	
I_{OL}	Open load current threshold			190		mA
T_{OTW}	Overtemperature warning	SPI Interface, Die temperature T_J	135	150	165	°C
T_{HYS_OTW}	Overtemperature warning hysteresis	SPI Interface, Die temperature T_J		20		°C
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

(1) Guaranteed by design

6.5.1 SPI Timing Requirements

SPI Timing Diagram

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready, VM > V_{RST}		1		ms
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input setup time	20			ns
t_{H_SDI}	SDI input hold time	30			ns
t_{D_SDO}	SDO output delay time, SCLK high to SDO valid, C_L = 20 pF			30	ns
t_{SU_nSCS}	nSCS input setup time	50			ns
t_{H_nSCS}	nSCS input hold time	50			ns
t_{HI_nSCS}	nSCS minimum high time before active low			2	µs
t_{DIS_nSCS}	nSCS disable time, nSCS high to SDO high impedance		10		ns

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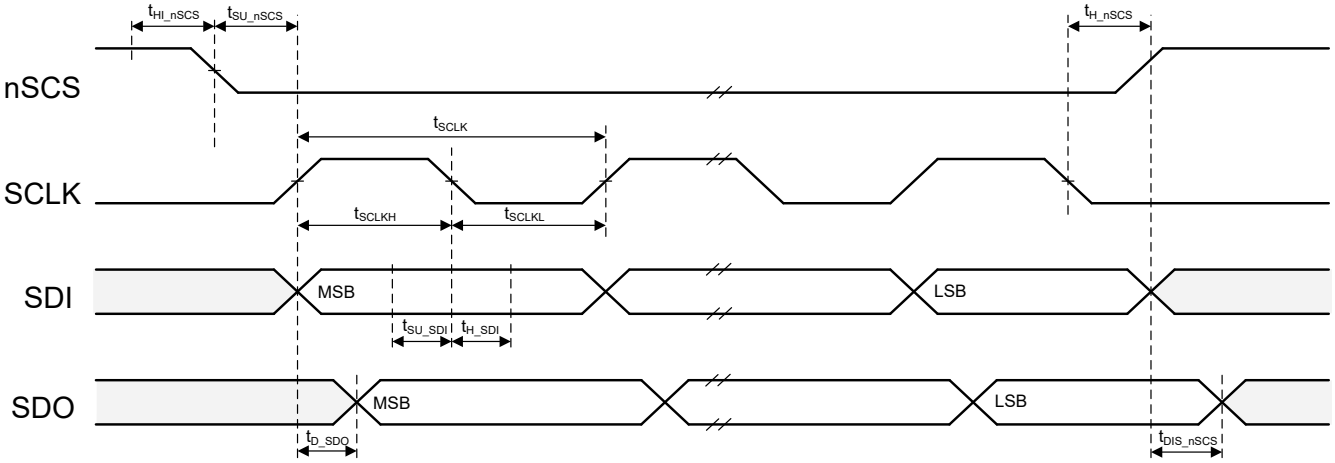

6.5.2 STEP and DIR Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500(1)	kHz
2	t_{WH_STEP}	Pulse duration, STEP high	970		ns
3	t_{WL_STEP}	Pulse duration, STEP low	970		ns
4	$t_{SU\_DIR, Mx}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H\_DIR, Mx}$	Hold time, DIR or Mx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

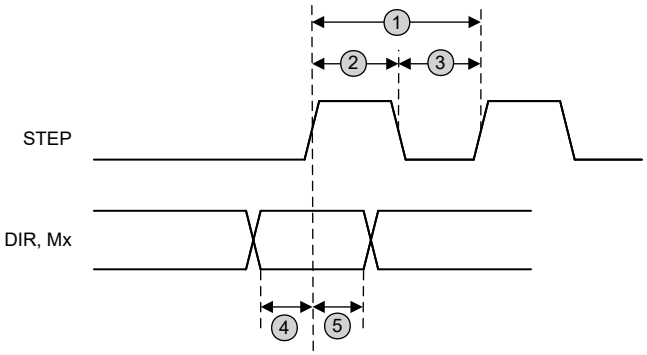

Figure 6-1. STEP and DIR Timing Diagram

6.6 Typical Characteristics

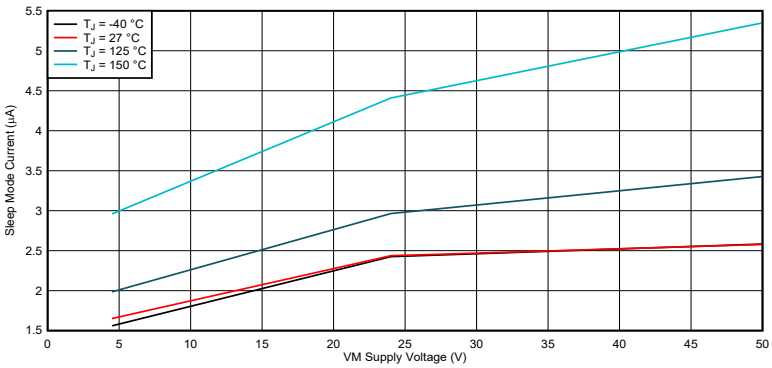

Figure 6-2. Sleep mode supply current

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6.6 Typical Characteristics

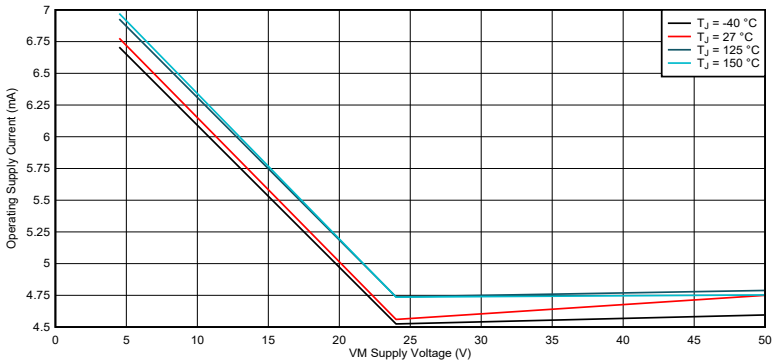

Figure 6-3. Operating supply current, VCC = External 5 V

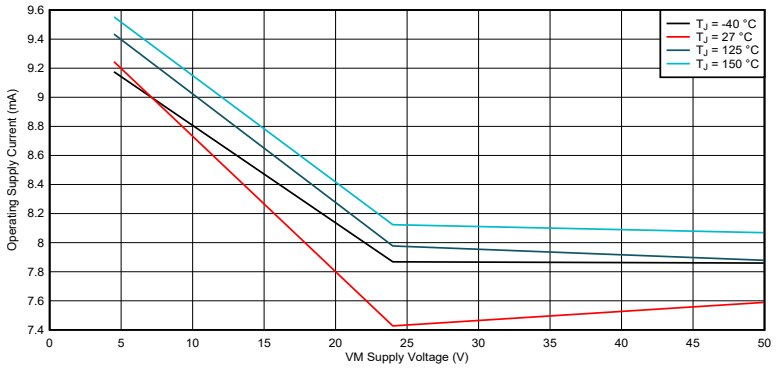

Figure 6-4. Operating supply current, VCC = DVDD

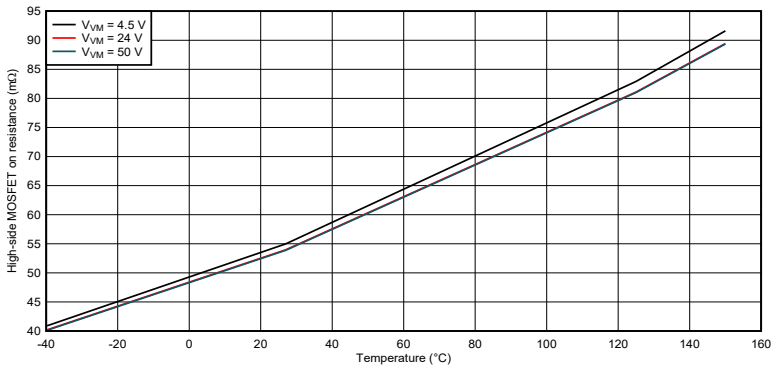

Figure 6-5. High-side FET on resistance, DDW Package

6.6 Typical Characteristics

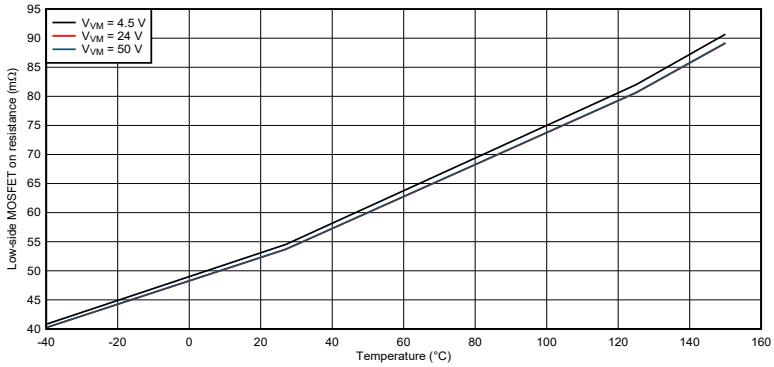

Figure 6-6. Low-side FET on resistance, DDW Package

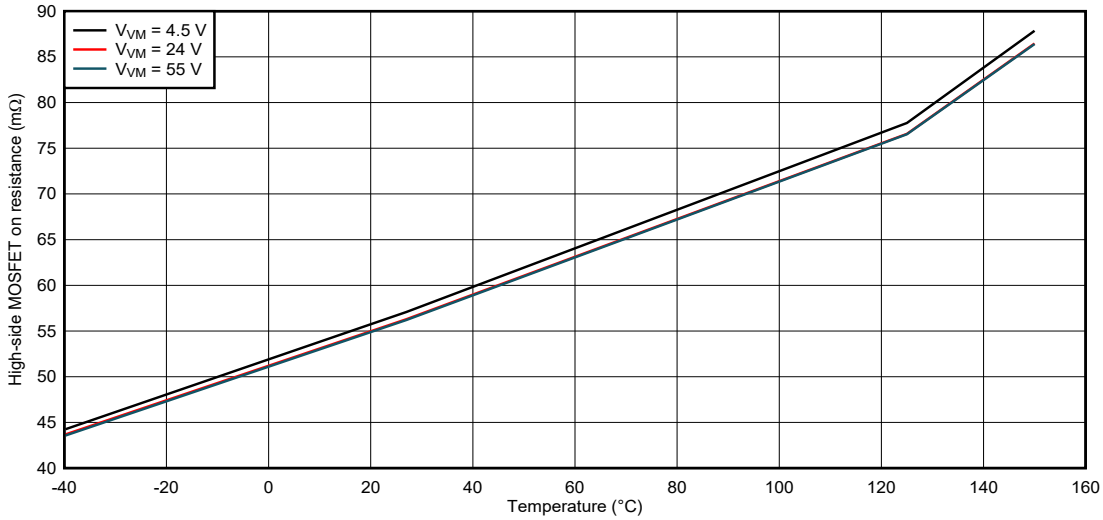

Figure 6-7. High-side FET on resistance, PWP Package

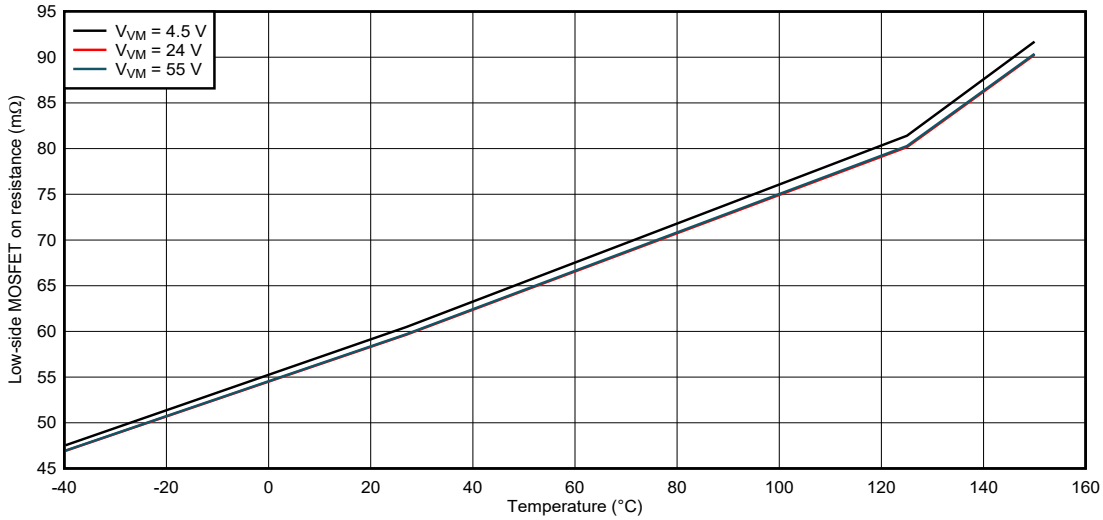

Figure 6-8. Low-side FET on resistance, PWP Package

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7 Detailed Description

7.1 Overview

The DRV8452 is an integrated motor-driver solution for bipolar stepper motors. The device integrates two N-channel power MOSFET H-bridges, current sense resistors, current regulation circuitry, and a microstepping indexer. The DRV8452 is capable of supporting wide supply voltage of 4.5 V to 55 V. The device is available in two packages - a 44-pin HTSSOP (DDW) package; and another 28-pin HTSSOP (PWP) package. The DDW package provides an output current up to 5-A full-scale, or 3.5-A root mean square (rms). The PWP package provides an output current up to 4-A full-scale, or 2.8-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal design. To provide scalable voltage and current solutions for the system design, the PWP package with SPI interface is pin-to-pin compatible with the DRV8434S. The PWP package with H/W interface is pin-to-pin compatible with the DRV8424, DRV8426 and DRV8434. The DDW package is pin-to-pin compatible with the DRV8462 and DRV8461.

The DRV8452 integrates the auto-torque feature to reduce power loss and improve system efficiency by adjusting output current according to the load torque. The SPI interface provides various options to optimize the performance of the auto-torque algorithm for specific motor and system use case. The stall detection feature detects and reports a motor stall condition to the system controller when the motor is obstructed or has reached an end-of-travel stop. Additionally, the standstill power saving mode reduces power loss when the motor is at holding position.

The DRV8452 uses an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture eliminates the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. Optional external power sense resistors can also be connected between the PGND pins and board ground to monitor motor health and for implementing closed-loop algorithms such as Field Oriented Control. The current regulation set point is adjusted by the voltage at the VREF pin. For the SPI interface, an 8-bit register allows the controller to scale the output current without needing to scale the VREF voltage reference; and another 8-bit register allows configuration of the holding current level for the purpose of reducing power loss at motor standstill.

A STEP/DIR pin interface allows an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4,1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. The automatic microstepping mode interpolates the input step frequency to high resolution, thereby improving current regulation and reducing audible noise while running with a low frequency step input from the controller. The custom microstepping table allows adjusting the current waveform to the needs of a particular motor.

Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes, such as slow decay, mixed decay and fast decay. The DRV8452 supports smart tune decay modes. The smart tune is an innovative decay mechanism that automatically adjusts for optimal current regulation performance agnostic of supply voltage and motor speed variations and aging effects. Smart tune Ripple Control uses a variable off-time ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time dynamic fast decay percentage scheme. Along with the smart tune decay modes, the DRV8452 also features a silent step decay mode for noiseless operation at standstill and low speeds of rotation.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature minimizes the electromagnetic emissions from the device. A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

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7.2 Functional Block Diagram

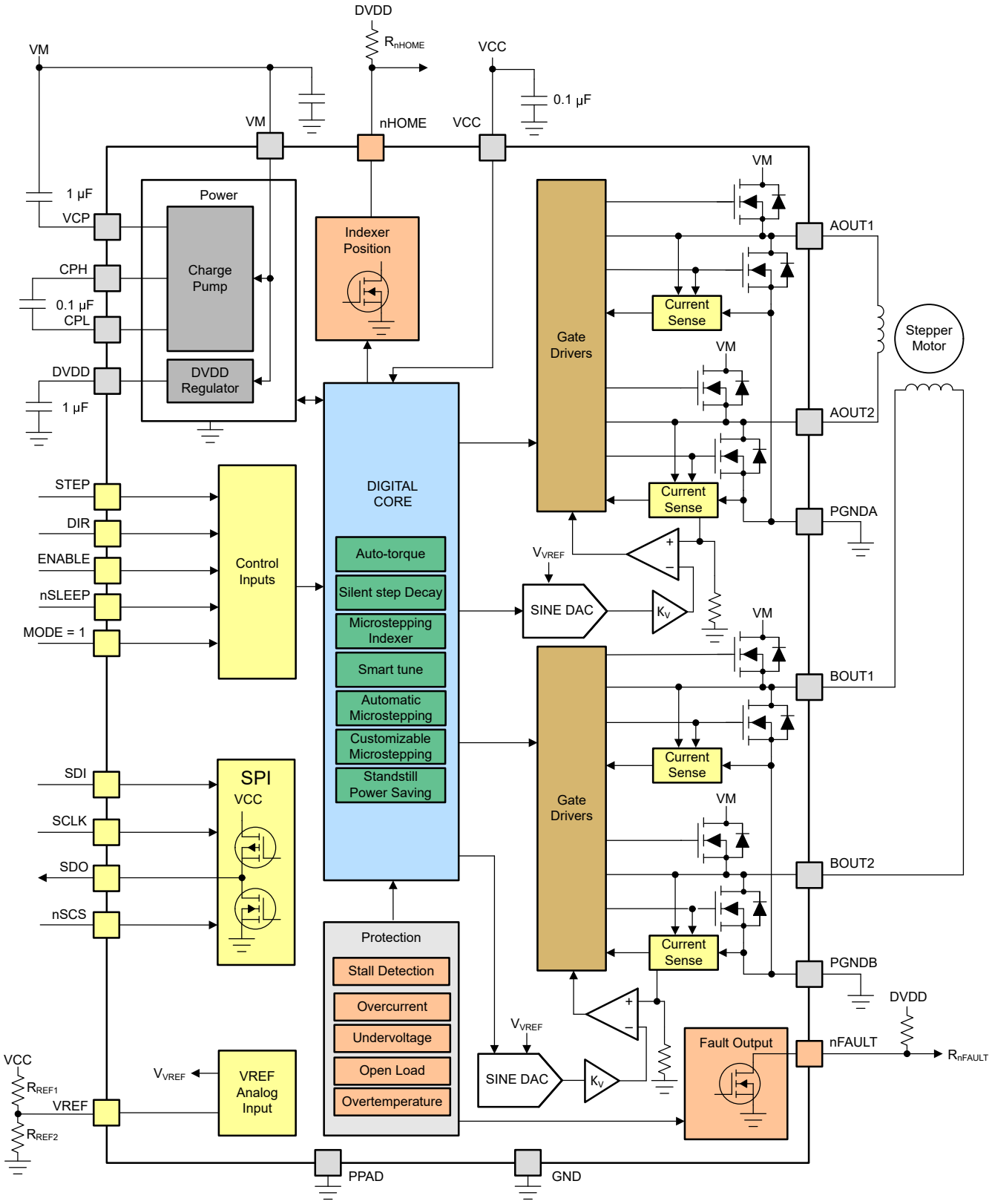

Figure 7-1. DRV8452 Block Diagram with SPI Interface

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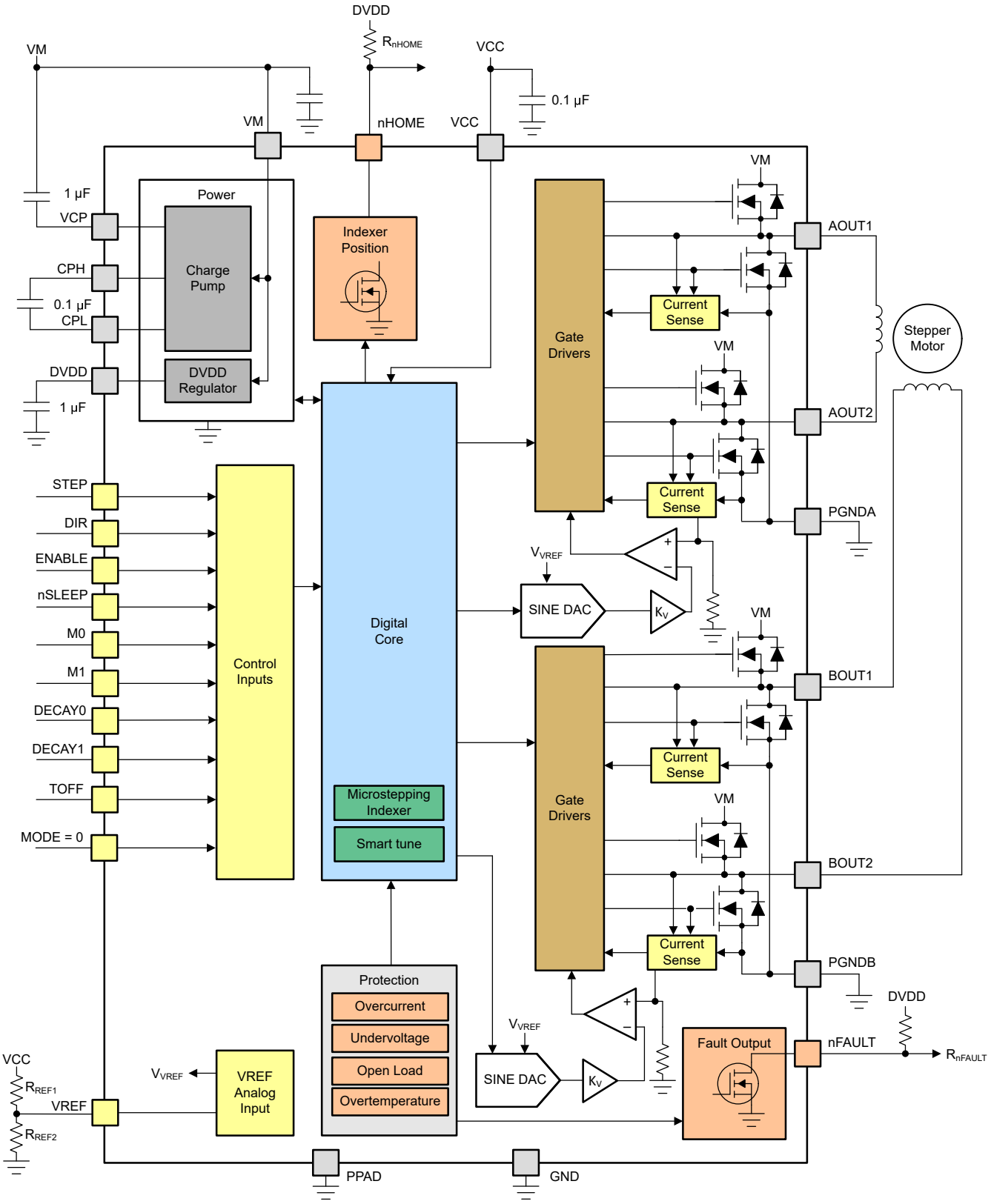

Figure 7-2. DRV8452 Block Diagram with H/W Interface

7.3 Feature Description

Table 7-1 lists the recommended external components for the DRV8452.

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGNDA	X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGNDB	X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM3}	VM	PGNDA	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 1-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.1-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 1-µF, 6.3-V ceramic capacitor
C_{VCC}	VCC	GND	X7R, 0.1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	DVDD or VCC	nFAULT	10-kΩ resistor
R_{nHOME} (only for DDW)	DVDD or VCC	nHOME	10-kΩ resistor
R_{REF1}	VREF	DVDD or VCC	Resistor to set chopping current. Not required if VREF_INT_EN = 1b.
R_{REF2}	VREF	GND	

7.3.1 Interface of Operation

The DRV8452 can operate with hardware (H/W) pin interface or SPI interface. When operating with SPI interface, the device supports additional features and detailed diagnostics, as shown in Table 7-4.

For the DDW package option, the logic-level MODE pin latches the operating interface information at power up or after nSLEEP cycling -

- If the MODE pin is grounded at this time, the device operates with H/W pin interface.
- If the MODE pin is logic high at this time, the device operates with SPI interface.

Note

Do not change MODE pin logic level on the fly after power up or after nSLEEP = 1.

The functionality of five pins depend on the interface of operation, as shown in Table 7-2 and Table 7-3 -

Table 7-2. Pin function, DDW package

Pin Number	H/W interface	SPI Interface
34	M0	nSCS
35	TOFF	Reserved
36	DECAY1	SDO
37	DECAY0	SDI
38	M1	SCLK

Table 7-3. Pin function, PWP package

Pin Number	DRV8452SPWPR (SPI Interface)	DRV8452PWPR (H/W Interface)
18	nSCS	M0
19	VCC	TOFF
20	SDO	DECAY1

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Table 7-3. Pin function, PWP package (continued)

Pin Number	DRV8452SPWPR (SPI Interface)	DRV8452PWPR (H/W Interface)
21	SDI	DECAY0
22	SCLK	M1

Table 7-4 compares the feature set and diagnostic features for the two operating interfaces -

Table 7-4. Feature Set Difference

Feature	H/W interface	SPI interface
Smart tune	Yes	Yes
Up to 1/256 microstepping	Yes	Yes
VCC logic supply	Yes	Yes
nHOME output	Yes	Yes
nFAULT output	Yes	Yes
Automatic microstepping	No	Yes
Customizable microstepping	No	Yes
Indexer output	No	Yes
Internal 3.3V reference voltage	No	Yes
Dual STEP active edge	No	Yes
Silent step decay	No	Yes
Auto-torque	No	Yes
Standstill power saving	No	Yes
Spread spectrum	No	Yes
Protection features		
VM and VCP UVLO	Yes	Yes
VCC Power on Reset	Yes	Yes
Overcurrent Protection	Yes	Yes
Open-load detection	Yes	Yes
Thermal shutdown	Yes	Yes
Stall detection	No	Yes
Overtemperature warning	No	Yes

7.3.2 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

7.3.2.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8452, the peak current rating is 7.6 A per bridge.

7.3.2.2 RMS Current Rating

The RMS current is determined by the thermal considerations of the IC. The RMS current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a

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typical system at 25°C. The actual operating RMS current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8452 in DDW package, the RMS current rating is 3.5 A per bridge. For the PWP package, the RMS current rating is 2.8 A per bridge.

7.3.2.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the RMS current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$ for a sinusoidal current waveform, and I_{RMS} for a square wave current waveform (full step).

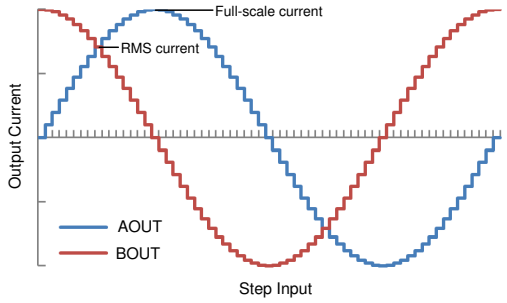

Figure 7-3. Full-Scale and RMS Current

7.3.3 PWM Motor Drivers

The DRV8452 has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 7-4 shows the block diagram of the circuitry.

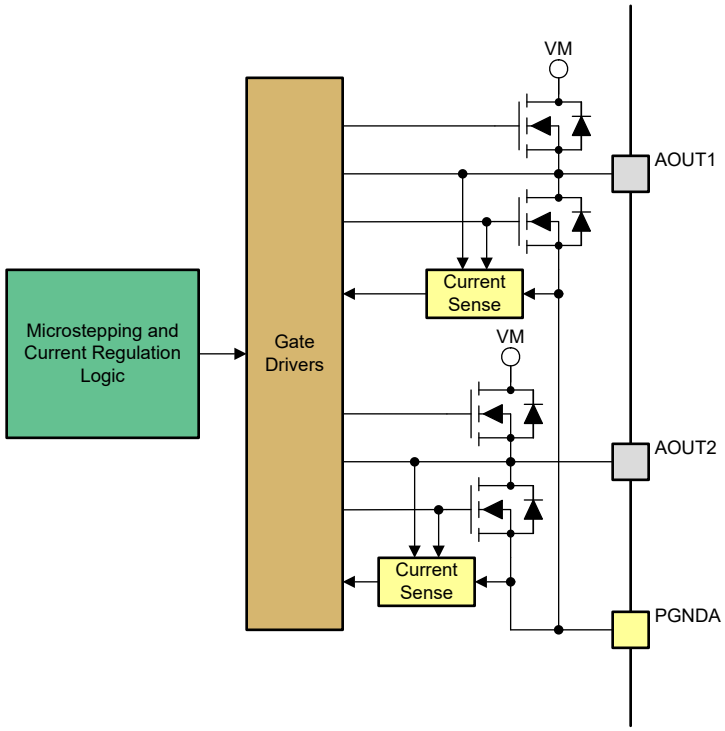

Figure 7-4. PWM Motor Driver Block Diagram

7.3.4 Microstepping Indexer

Built-in indexer logic in the device allows a number of different step modes. The MICROSTEP_MODE bits in the SPI register or the M0 and M1 pins are used to configure the step mode as shown in Table 7-5.

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Table 7-5. Microstepping Indexer Settings

MODE = 1	MODE = 0		
MICROSTEP_MODE	M0	M1	STEP MODE
0000b	0	0	Full step (2-phase excitation) with 100% current
0001b	0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
0010b	1	0	Non-circular 1/2 step
0011b	Hi-Z	0	1/2 step
0100b	0	1	1/4 step
0101b	1	1	1/8 step
0110b	Hi-Z	1	1/16 step
0111b	0	Hi-Z	1/32 step
1000b	Hi-Z	330kΩ to GND	1/64 step
1001b	Hi-Z	Hi-Z	1/128 step
1010b	1	Hi-Z	1/256 step

When operating with SPI interface, the device allows stepping and direction change over SPI interface as well, as shown in Table 7-6. Four bits are dedicated for this purpose -

Table 7-6. STEP and DIR control over SPI

Bit	0b (default)	1b
SPI_DIR	Driver changes direction based on DIR pin inputs	Direction changes depend on the DIR bit
SPI_STEP	Stepping depends on the STEP pin inputs	Step changes depend on the STEP bit
DIR	Motor moves in the reverse direction	Motor moves in the forward direction
STEP	X	Indexer advances by one step. STEP bit is self-clearing, becomes '0' after writing '1' to it.

Table 7-7 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation for the case when DIR pin is logic high or DIR bit is '1'. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

Table 7-7. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25

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Table 7-7. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 7-8 shows the full step operation with 100% full-scale current for the DIR = 1 case. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 7-8. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	100	-100	135
3	-100	-100	225
4	-100	100	315

Table 7-9 shows the noncircular 1/2–step operation for the DIR = 1 case. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 7-9. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270

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Table 7-9. Non-Circular 1/2-Stepping Current (continued)

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
8	–100	100	315

When operating with the SPI interface, depending on the STEP_EDGE bit, STEP active edge can be either rising edge or both rising and falling edge, as shown in Table 7-10. When configured with H/W interface, the STEP active edge is only the rising edge. For applications that need to run at high input STEP rate, configuring both edges as active edge reduces controller overhead by half, because the input STEP rate is effectively doubled.

Table 7-10. STEP Active Edge

Interface	STEP_EDGE	STEP Active Edge
SPI	0b (default)	Rising edge
	1b	Rising edge and falling edge
H/W	X	Rising edge

At each active edge of the STEP input the indexer advances to the next state in the table. The direction shown is with the DIR pin logic high. If the DIR pin is logic low, the sequence table is reversed. If the step mode is changed dynamically while stepping, the indexer advances to the next valid state for the new step mode setting at the active edge of STEP.

After power-up, after exiting logic undervoltage lockout, or after exiting sleep mode, the indexer moves to an initial excitation state (home position) of 45° electrical angle, corresponding to 71% of full-scale current in both coils. All the registers are restored to their deafult values in such scenario.

When operating with the SPI interface, if the IDX_RST bit is 1b, it resets the indexer to 45° electrical angle as shown in Figure 7-5, but the contents of the memory map registers do not change.

Traces from top to bottom: AOUT2, AOUT1, STEP, coil B current, coil A current, nSCS

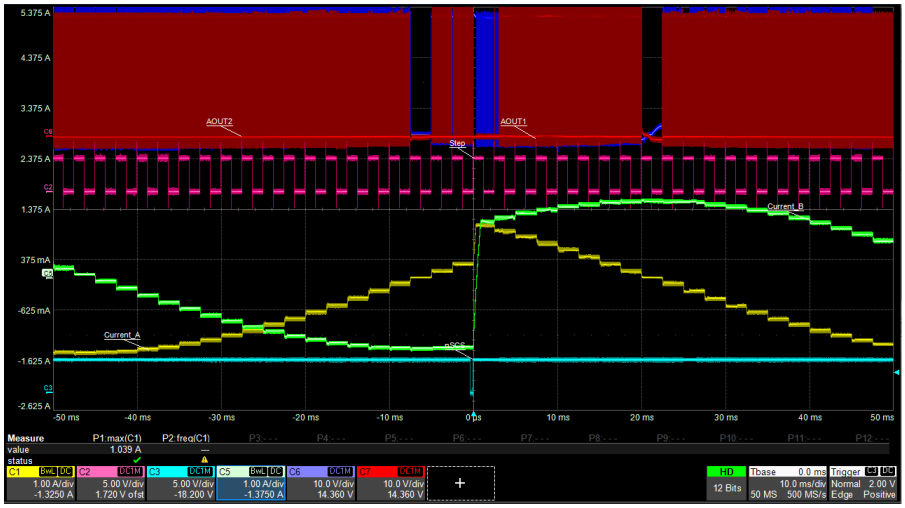

Figure 7-5. Indexer reset

If the STEP input frequency is jittery, the device filters the signal for the purpose of stall detection. The FRQ_CHG and STEP_FRQ_TOL bits program the filter setting, as shown in Table 7-11. 2% filtering means up to 2% jitter around the center frequency will be filtered out to generate a clean STEP signal for internal circuits to detect motor stall.

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Table 7-11. STEP frequency filtering

FRQ_CHG	STEP_FRQ_TOL	Filtering
0b (default)	00b	1%
	01b (default)	2%
	10b	4%
	11b	6%
1b	X	No filtering

7.3.5 Indexer Output

The DRV8452 features the INDEX registers to indicate the expected microstep current and position of the motor to the user.

- CUR_A_POS register and CUR_A_SIGN bit indicate the position of coil A current in the indexer table.
- CUR_B_POS register and CUR_B_SIGN bit indicate the position of coil B current in the indexer table.
- CUR_A register indicates the value of expected coil A current, which is sin (90° x CUR_A_POS / 255).
- Current will be positive if the corresponding sign bit is 1b and negative if the sign bit is 0b.

Table 7-12 shows the outputs of the CUR_A_POS and CUR_B_POS registers for a current waveform corresponding to 1/256 microstepping.

Table 7-12. Indexer Output Table

Current Quadrant	CUR_A_POS	CUR_A_SIGN	CUR_B	CUR_B_SIGN
First (0° -> 90°)	0 -> 255	1b	255 -> 0	1b
Second (90° -> 180°)	255 -> 0	1b	0 -> 255	0b
Third (180° -> 270°)	0 -> 255	0b	255 -> 0	0b
Fourth (270° -> 360°)	255 -> 0	0b	0 -> 255	1b

The Indexer outputs together with the nHOME signal allow determination of the motor position within the electrical wave. They can be compared with an encoder output to detect discrepancies in the movement of the motor - such as detecting step loss.

7.3.5.1 nHOME Output

For the DDW package, when the microstepping indexer reaches the home position (electrical angle of 45°), corresponding to 71% of full-scale current in both coils, the open-drain nHOME output is pulled low. At all other times, the nHOME output will be pulled high. When the device operates with SPI interface, additionally the NHOME bit in SPI register becomes 0b when the indexer reaches home position.

Therefore, the nHOME output gives one low pulse per electrical rotation, i.e. one pulse per each four fullsteps, as shown in Figure 7-6. The nHOME low pulse thus corresponds to a defined position of the motor for every four fullsteps. A more precise homing of the motor can be achieved by combining nHOME with a mechanical home switch.

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Pull up the nHOME to a 5-V, 3.3-V or 1.8-V supply using a pull-up resistor. For a 5-V pullup, the nHOME pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

Traces from top to bottom: BOUT2, BOUT1, coil B current, coil A current, nHOME

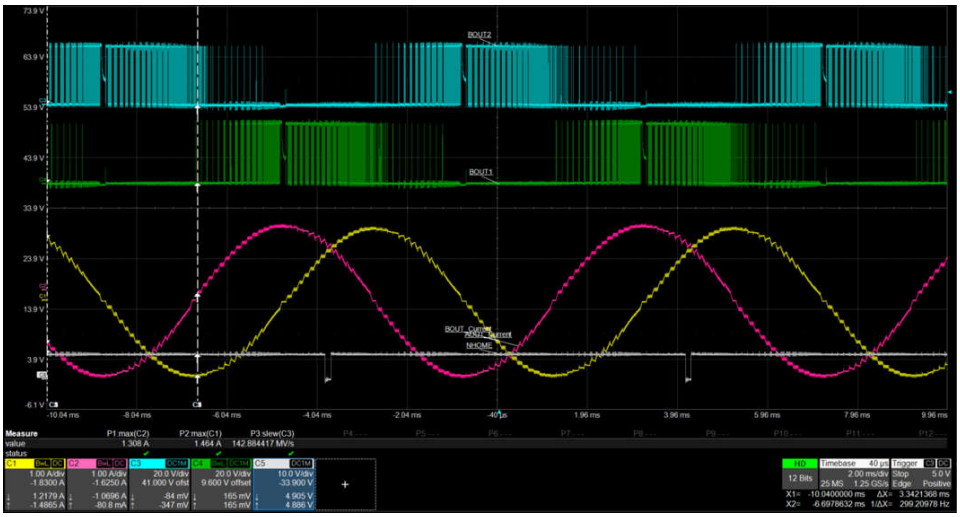

Figure 7-6. nHOME Output Waveform

7.3.6 Automatic Microstepping Mode

When the DRV8452 is operating with SPI interface, automatic microstepping mode interpolates the input step pulses to generate a current waveform corresponding to higher resolution microstep. This results in smooth sinusoidal current and noiseless operation at any step frequency.

- If automatic microstepping is disabled, the system controller will be forced to output high frequency STEP signals to generate high resolution microstepping current waveforms.
- With automatic microstepping enabled, smooth current waveform can be generated by low frequency STEP signals.
  - This drastically reduces controller overhead and is beneficial for applications such as 3D printer, factory automation and medical.
- It should be ensured that the interpolated frequency does not fall in the resonant frequency band of the stepper motor.

The EN_AUTO bit should be 1b to enable the automatic microstepping mode.

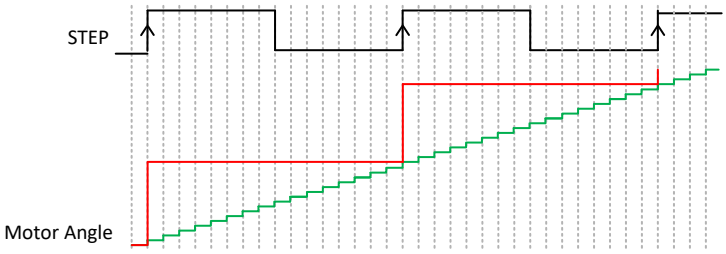

Figure 7-7. Automatic Microstepping Interpolation

Figure 7-7 shows increment in motor angle with and without automatic microstepping. Without automatic microstepping (red plot), the motor angle increments by a large amount on every step input active edge. Automatic microstepping (green plot) results in a much smoother change in motor angle.

The DRV8452 supports interpolation to 1/32, 1/64, 1/128 or 1/256 microstepping levels, configured by the RES_AUTO bits as shown in Table 7-13. Interpolation setting can be changed on the fly.

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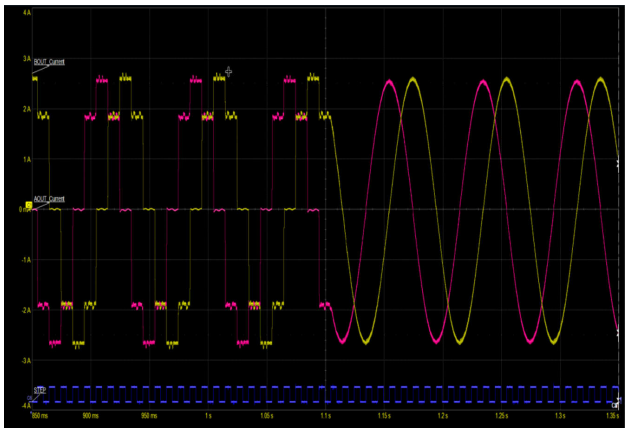
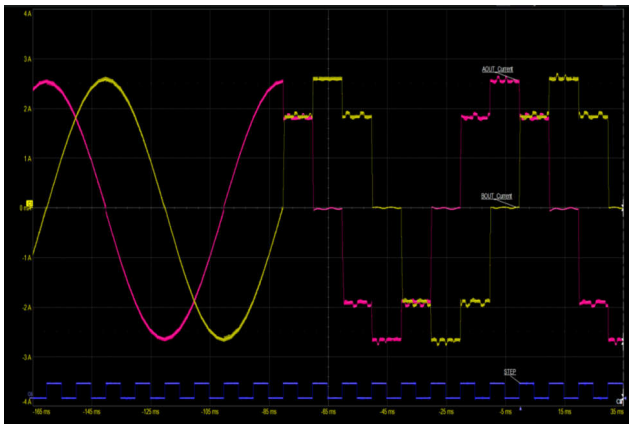
Table 7-13. Automatic Microstepping Interpolation Level

RES_AUTO	Interpolation
00b (default)	1/256
01b	1/128
10b	1/64
11b	1/32

Table 7-14 show both coil currents and the smooth transition between half-step mode and automatic microstepping mode by writing 1b and 0b respectively to the EN_AUTO bit. Notice that the step frequency is same in both half-step and 1/256 automatic microstepping modes.

Table 7-14. Transition between half-step and automatic microstepping

	
Transition from half-step mode to 1/256 automatic microstepping	Transition from 1/256 automatic microstepping to half-step mode

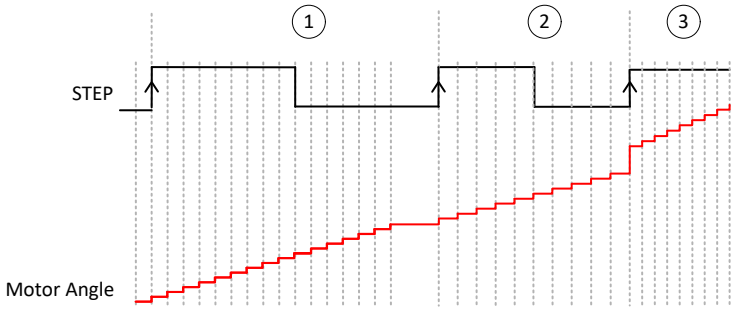


Figure 7-8. Automatic Microstepping with Changing STEP Frequency

As shown in Figure 7-8, the interpolation is done based on the time between the two previous step pulses. The previous interval time is interpolated to equal divisions, depending on the RES_AUTO bit setting.

When input step frequency reduces from previous interval (shown in segment '1'), the motor holds its position till the next STEP active edge occurs. Device will go to standstill power saving mode if the EN_STSL bit is 1b, and the next active edge does not come before t_{STSL_DLY} expires. Standstill power saving mode is exited on the next STEP active edge.

When step frequency increases from previous interval (shown in segment '2'), the motor angle smoothly auto-corrects when the next STEP active edge comes, and the indexer moves to a position corresponding to the STEP input. In segment '3', the motor angle is incremented at a faster rate, corresponding to the step frequency of segment '2'.

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Note

- The frequency of the STEP input in automatic microstepping mode should be between 10 Hz and 300 kHz.
- To realize automatic microstepping for lower than 10 Hz full step equivalent step frequency, use a higher resolution microstepping setting before enabling automatic microstepping.
  - For example, 1 Hz step frequency in full step mode corresponds to 16 Hz step frequency in 1/16 microstepping mode. So, if one wants to use automatic microstepping for a full step 1 Hz step input, MICROSTEP_MODE can be set to 0110b (1/16 microstep), and use RES_AUTO bits for desired interpolation level.

7.3.7 Custom Microstepping Table

The performance and audible noise of any stepper motor system depends on the torque ripple generated by both the motor and the load. The torque ripple is defined by the variation in torque at each microstep. For most stepper motors, the standard sinusoidal microstep indexer is sufficient to achieve acceptable torque ripple and a good performance.

However, for some motor and load torque combinations, altering the current profile can reduce torque ripple, resulting in lower vibration and audible noise. When properly programmed, the customized current waveform ensures equally distanced microstep positions with constant torque and therefore also the best positional accuracy.

For example, in case of permanent magnet motors, variations in torque are more prominent due to larger step angle (3.6° to 18°) than that of hybrid motors (0.9° or 1.8°). Due to fewer number of stator teeths, less amount of flux interacts between the stator teeth and the rotor when the rotor is in between two stator teeths. If the current level is increased at these intermediate positions, the torque ripple will be lower compared to the default sinusoidal indexer.

The DRV8452 features a lookup table for tailoring the microstepping current profile to suit the requirements of a specific motor. The modified current profile is used in place of the default sinusoidal profile by writing '1' to the EN_CUSTOM bit. The frequency of the STEP input in custom microstepping mode should not exceed 300 kHz. The details of the interpolation process is described below -

- The user should program the current (% of TRQ_DAC) corresponding to the first quadrant of coil A current in a 1/8 microstepping setting.
- These current values are stored in CUSTOM_CURRENT1 to CUSTOM_CURRENT8 registers.
- The position for these current values correspond to 11.25°, 22.5°, 33.75°, 45°, 56.25°, 67.5°, 78.75° and 90° electrical angles.
- The current value for 0° position is assumed to be zero.
- The nine current values (including 0% full-scale current) are interpolated to a total of 256 points using a piecewise-linear approach to build the complete current waveform. The interpolated waveform always corresponds to 1/256 microstep, irrespective of the programmed microstepping mode.
- The values for the first quadrant are then mirrored and repeated for the other three quadrants of coil A and again for the four quadrants of coil B current to construct the complete current waveform.

Table 7-15 shows an example of the user inputs.

Table 7-15. Custom Microstepping Table Values

Position (degrees)	Sine Indexer Value	Modified Value (CUSTOM_CURRENTx)
0	0	0
11.25	49.7	24
22.5	97.6	56
33.75	141.7	96
45	180.3	152

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Table 7-15. Custom Microstepping Table Values (continued)

Position (degrees)	Sine Indexer Value	Modified Value (CUSTOM_CURRENTx)
56.25	212	192
67.5	235.6	224
78.75	250.1	240
90	255	255

Figure 7-9 shows the corresponding modified current waveform of coil A for one full electrical angle, compared to waveform generated by sine indexer.

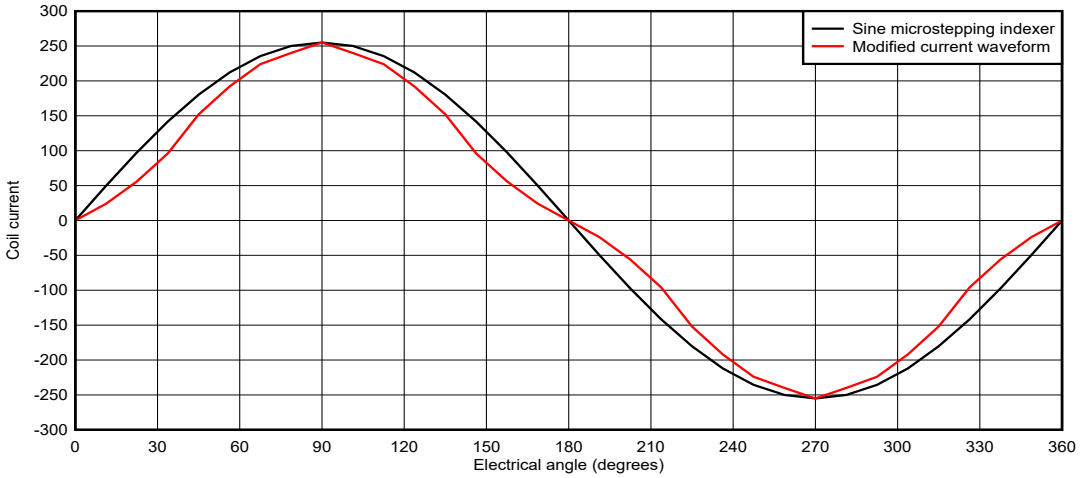

Figure 7-9. Customizable Microstepping

7.3.8 Current Regulation

The current through the motor windings is regulated by a PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for the OFF time to decrease the current, as shown in Figure 7-10. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

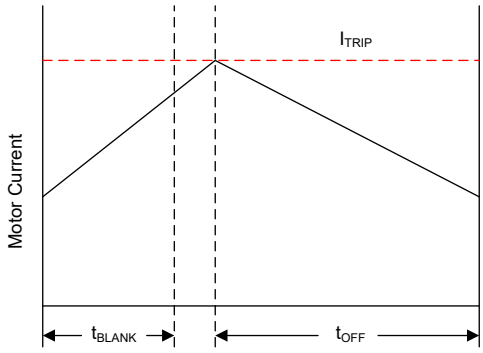

Figure 7-10. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. When the device is configured with H/W interface, the current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin. When operating with SPI interface, two registers (TRQ_DAC and ISTSL) can further scale the reference current.

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Use Equation 1 to calculate the full-scale regulation current for H/W interface.

$$I_{FS}\ (A) = VREF\ (V) / K_V\ (V/A) \quad (1)$$

For the SPI interface, the 8-bit TRQ_DAC register further scales the full-scale current as shown in Equation 1. See Table 7-16 for TRQ_DAC settings.

$$I_{FS}\ (A) = VREF\ (V) \times TRQ\_DAC / K_V\ (V/A) \quad (2)$$

Table 7-16. TRQ_DAC Settings

TRQ_DAC	CURRENT SCALAR
11111111b (default)	100%
11111110b	99.61%
11111101b	99.22%
11111100b	98.83%
.....	.....
00000000b	0.39%

Another 8-bit register ISTSL programs the holding current (I_{HOLD}) when STEP pulses are not applied and the motor is being held at same position. Transitioning to a lower value of holding current reduces motor and driver power loss. See Section 7.3.9 for details.

$$I_{HOLD}\ (A) = VREF\ (V) \times ISTSL / K_V\ (V/A) \quad (3)$$

Table 7-17. ISTSL Settings

ISTSL	Holding Current Value
11111111b	100%
11111110b	99.61%
11111101b	99.22%
11111110b	98.83%
.....	.....
10000000b (default)	50.39%
.....	.....
00000000b	0.39%

7.3.8.1 Internal Reference Voltage

When operating with the SPI interface, the DRV8452 supports an internal 3.3V reference voltage. This internal reference can be enabled by writing 1b to the VREF_INT_EN bit. The voltage on the VREF pin will be ignored in that case, and the VREF pin can be left open or connected to ground.

The full-scale current and the holding current will be calculated as shown in Equation 4 and Equation 4 -

$$I_{FS}\ (A) = 3.3\ V \times TRQ\_DAC / K_V\ (V/A) \quad (4)$$

$$I_{HOLD}\ (A) = 3.3\ V \times ISTSL / K_V\ (V/A) \quad (5)$$

Using the internal 3.3V as reference will save BOM cost by eliminating the two resistors connected to the VREF pin.

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Figure 7-11 shows current regulation with VREF_INT_EN = 1b and 5 A full-scale current.

Traces from top to bottom: AOUT2, coil A current, AOUT1

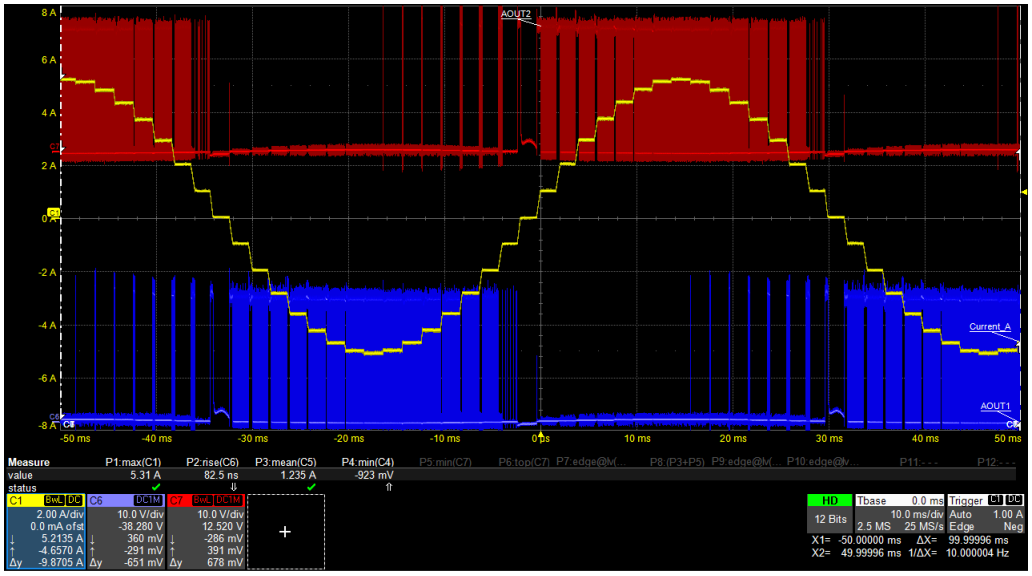

Figure 7-11. Current regulation with internal reference voltage

7.3.9 Standstill Power Saving Mode

When the controller is not sending any step pulses and the motor is holding the same position, the DRV8452 can be configured to operate in the standstill power saving mode. When this mode is enabled by writing 1b to the EN_STSL bit, the power dissipation of the system can be reduced by lowering the coil current from run current to holding current.

After the last STEP pulse, the device waits for an amount of time programmed by the TSTSL_DLY register, after which the coil currents are ramped down from run current to holding current over a time period programmed by the TSTSL_FALL register, as shown in Figure 7-12. The STSL flag goes up to indicate that the device is in standstill power saving mode. Once the next STEP pulse is detected, the coil current immediately ramps up to run current. The available options for TSTSL_FALL and TSTSL_DLY are shown in Table 7-18.

The run current is programmed by the TRQ_DAC register and the holding current is programmed by the ISTSL register, as shown in Section 7.3.8.

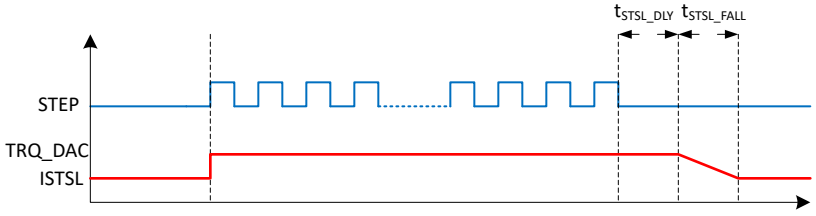

Figure 7-12. Standstill Power Saving Mode

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Table 7-18. Standstill fall time and delay time

Parameter	Description
TSTSL_FALL[3:0]	Controls the time taken by the current to reduce from TRQ_DAC to ISTSL after TSTSL_DLY time has elapsed. For each TSTSL_FALL, TRQ_DAC will fall by 1b til the current reaches ISTSL. Total fall time = (TRQ_DAC - ISTSL) * fall time for each current step. • 0000b: fall time = 0 • 0001b: fall time for each current step = 1 ms • ..... • 0100b: fall time for each current step = 4 ms (default) • ..... • 1111b: fall time for each current step = 15 ms
TSTSL_DLY[5:0]	Controls the delay between last STEP pulse and activation of standstill power saving mode. • 000000b: Reserved • 000001b: Delay = 1 x 16 ms = 16 ms • ..... • 000100b: Delay = 4 x 16 ms = 64 ms (default) • ..... • 111111b: Delay = 63 x 16 ms = 1.008 s

Note

- If ISTSL has to be changed while the device is in standstill power saving mode, first cycle the EN_STSL bit from 1b to 0b and then back to 1b.
- While auto-torque is disabled:
  - I_{HOLD} = ISTSL if ISTSL < TRQ_DAC
  - I_{HOLD} = TRQ_DAC if ISTSL > TRQ_DAC
- While auto-torque is enabled:
  - I_{HOLD} = ISTSL if ISTSL < TRQ_DAC
  - I_{HOLD} = ATQ_TRQ_DAC if ISTSL > ATQ_TRQ_DAC
  - Best practice will be to program ISTSL to a value lower than ATQ_TRQ_MIN

7.3.10 Current Regulation Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the chopping current threshold is reached. This is shown in Figure 7-13, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

- In fast decay mode, as soon as the PWM chopping current level is reached, the H-bridge reverses state by switching on the opposite arm MOSFETs to allow the winding current to flow in the opposite direction. As the winding current approaches zero, the H-bridge is disabled to prevent further reverse current flow. Fast decay mode is shown in Figure 7-13, item 2.
- In slow decay mode, the winding current is re-circulated by enabling both low-side MOSFETs in the H-bridge. This is shown in Figure 7-13, Item 3.

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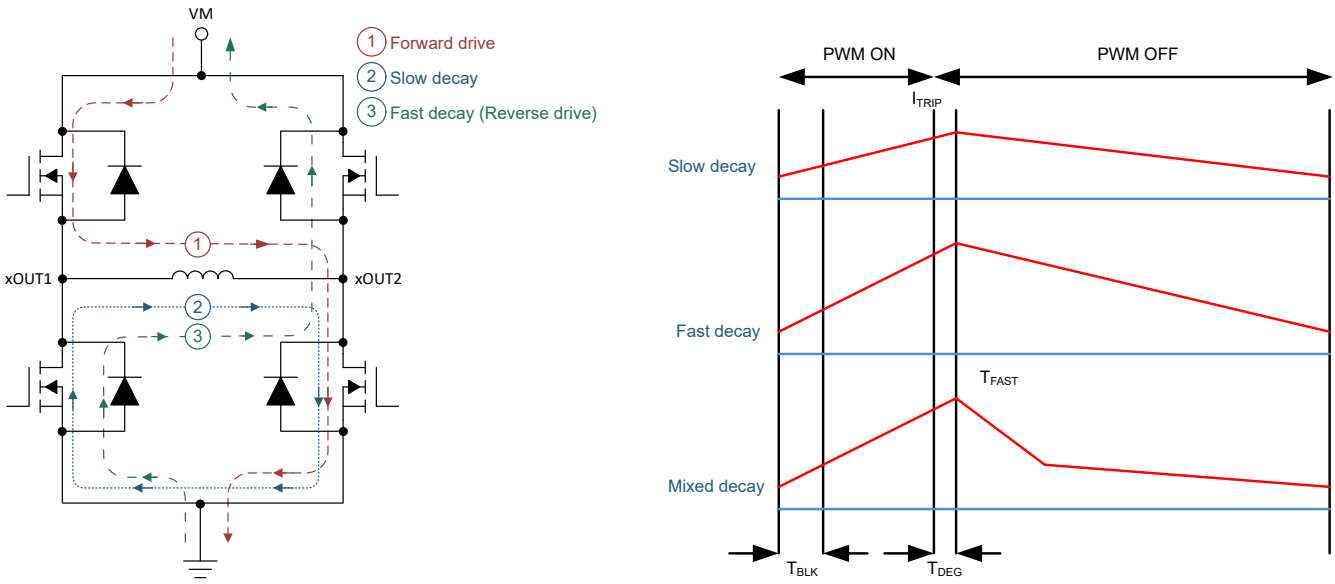

Figure 7-13. Decay Modes

The decay mode is selected by the DECAY register or the DECAY0 and DECAY1 pins, as shown in Table 7-19. The decay modes can be changed on the fly.

Table 7-19. Decay Mode Settings

SPI Interface	H/W Interface		DECAY MODE
DECAY	DECAY0	DECAY1	
000b	Hi-Z	1	Slow decay
100b	1	0	Mixed decay: 30% fast
101b	Hi-Z	0	Mixed decay: 60% fast
110b	0	0	Smart tune Dynamic Decay
111b (default)	0	1	Smart tune Ripple Control

Note

The remaining settings of DECAY bit (001b, 010b, 011b) and the (DECAY0 = 1, DECAY1 = 1) setting are reserved.

The DRV8452 also features the silent step decay mode for ultra-silent operation at low speed and standstill. See Section 7.3.12 for details.

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7.3.10.1 Slow Decay

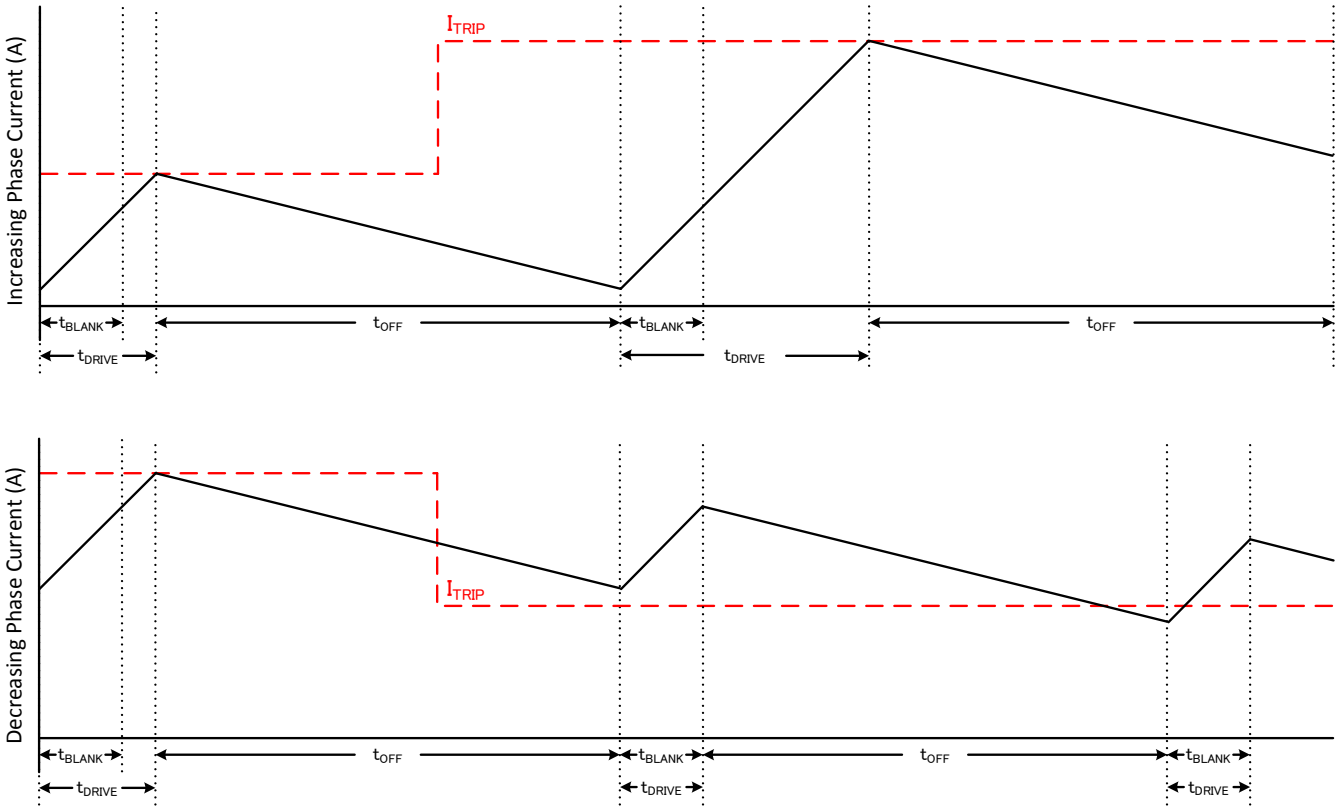

Figure 7-14. Slow Decay Mode

During slow decay, both the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated. Here are the points to consider when selecting slow decay mode -

- Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}.
- However on decreasing current steps, slow decay will take a long time to settle to the new I_{TRIP} level because the current decreases very slowly.
  - If the current at the end of the off time is above the I_{TRIP} level, slow decay will be extended for another off time duration and so on, till the current at the end of the off time is below I_{TRIP} level.
- In cases where current is held at the same level for a long time (no STEP input), or the target regulation current level is low, or at very low stepping speeds, slow decay may not properly regulate current because the back-EMF across the motor windings may be very small to discharge the current during the off time. In this state, motor current can rise very quickly, and may require a large off time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

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7.3.10.2 Mixed Decay

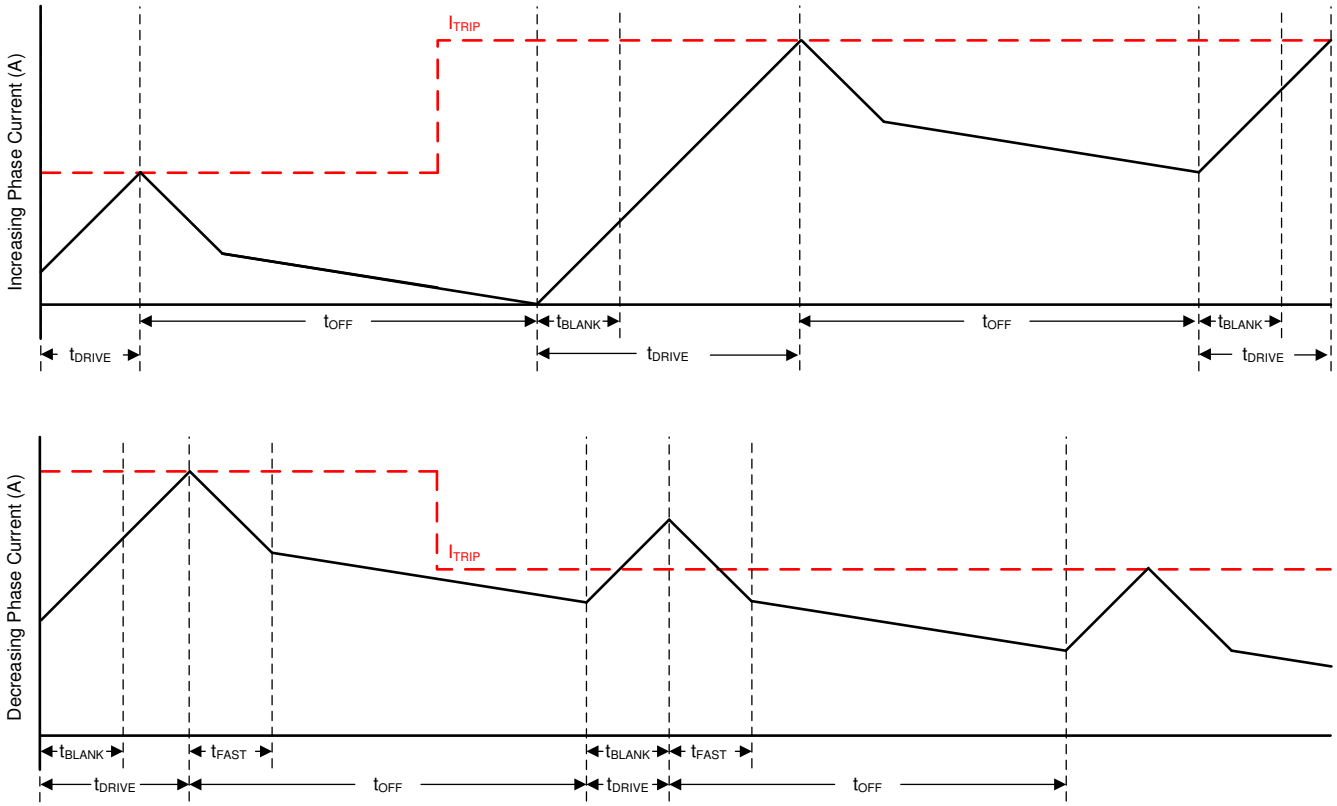

Figure 7-15. Mixed Decay Mode

Mixed decay begins as fast decay for a fixed initial duration of the t_{OFF} time (30% or 60%), followed by slow decay for the remainder of t_{OFF} time. Following points should be considered when selecting mixed decay mode -

- This mode exhibits ripple larger than slow decay.
- On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.
- In cases where current is held at the same level for a long time (no STEP input), or at very low stepping speeds, mixed decay allows the current to stay in regulation when no back-EMF is present across the motor windings.
- Fixed 30% or 60% mixed decay schemes can result in repeated patterns in current regulation that fall in the audible frequency range, resulting in a noisy motor operation.

7.3.10.3 Smart tune Dynamic Decay

The smart tunes are advanced current regulation schemes compared to traditional mixed decay modes. Smart tune helps the stepper motor driver adjust the decay scheme based on changes in operating factors such as:

- Motor winding resistance and inductance
- Motor aging
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The DRV8452 supports two different smart tune schemes - smart tune Dynamic Decay and smart tune Ripple Control.

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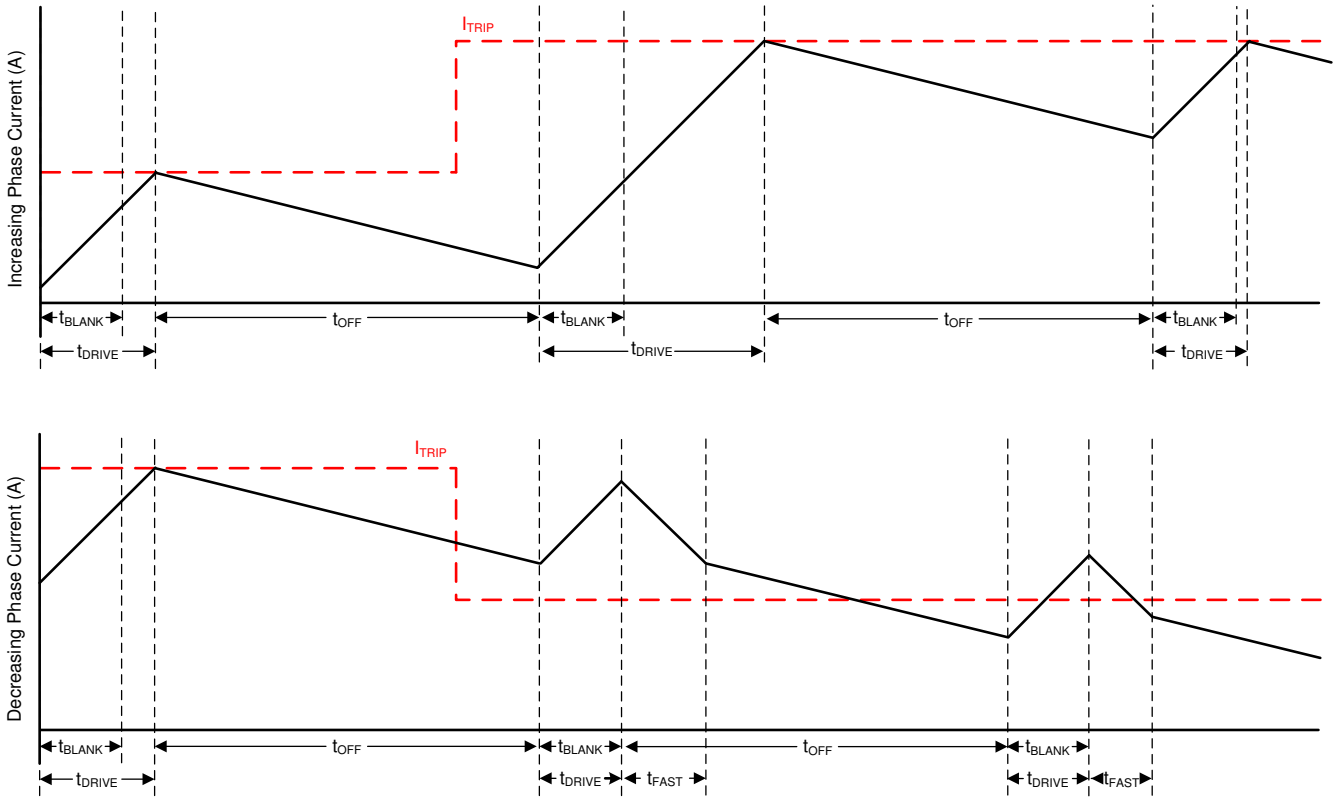

Figure 7-16. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay dynamically adjusts the fast decay percentage of the total mixed decay time. This eliminates the need for motor decay tuning by automatically determining the best mixed decay setting that results in the lowest ripple and best performance for the motor.

The fast decay percentage is optimized iteratively each PWM cycle. If the motor current overshoots the target I_{TRIP} level, then the mixed decay mode becomes more aggressive (by increasing fast decay percentage) on the next cycle to prevent loss of current regulation. If a long drive time must occur to reach the target I_{TRIP} level, the decay mode becomes less aggressive (by reducing fast decay percentage) on the next cycle to operate with less ripple. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

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7.3.10.4 Smart tune Ripple Control

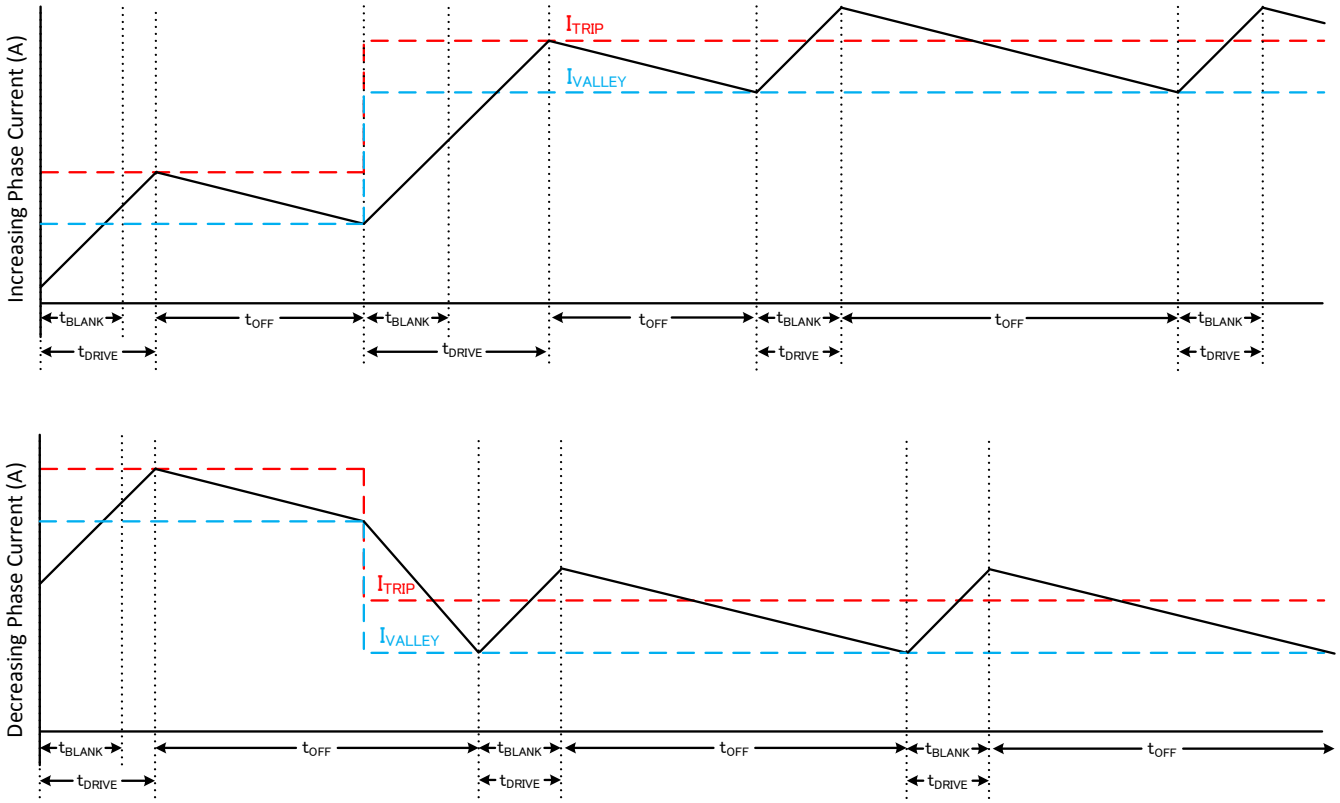

Figure 7-17. Smart tune Ripple Control Decay Mode

In smart tune Ripple Control decay mode, the PWM off time is variable depending on the current level and operating parameters. It operates by setting an I_{VALLEY} level along with the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached.

The magnitude of the ripple current in smart tune ripple control mode is programmed by the RC_RIPPLE[1:0] bits or the TOFF pin, as shown in Table 7-20.

Table 7-20. Current Ripple Settings

H/W Interface	SPI Interface	Current Ripple at a specific microstep level
TOFF	RC_RIPPLE	
0	00b (default)	25 mA + 1% of I_{TRIP}
1	01b	25 mA + 2% of I_{TRIP}
Hi-Z	10b	25 mA + 4% of I_{TRIP}
330kΩ to GND	11b	25 mA + 6% of I_{TRIP}

The smart tune ripple control scheme allows much tighter regulation of the ripple current, thereby improving motor efficiency and reducing audible noise. Select a ripple current setting that ensures the PWM frequency is not in the audible range (< 20 kHz).

7.3.10.5 PWM OFF Time

The TOFF bits or the TOFF pin configure the PWM OFF time for all decay modes, except smart tune ripple control and silent step decay modes, as shown in Table 7-21. The OFF time settings can be changed on-the-fly.

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Table 7-21. OFF Time Settings

SPI Interface	H/W Interface	OFF Time
TOFF	TOFF	
00b	0	9 µs
01b (default)	1	19 µs
10b	Hi-Z	27 µs
11b	330kΩ to GND	35 µs

7.3.10.6 Current Regulation Blanking Time and Deglitch Time

After the start of drive phase in an H-bridge, the current sense comparator is ignored for a period of time (blanking time) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM.

- When the device operates with hardware interface, the blanking time is fixed at 1.5 µs.
- When the device is operating with SPI interface, the blanking time can be programmed by the TBLANK_TIME bits as shown in Table 7-22, with a default value of 1.5 µs.

Table 7-22. TBLANK_TIME Settings

TBLANK_TIME	Blanking Time
00b	1 µs
01b (default)	1.5 µs
10b	2 µs
11b	2.5 µs

When the current is close to the I_{TRIP} level, a 0.5 µs deglitch time is added to ensure proper current regulation.

7.3.11 Current Sensing with External Resistor

PWM current regulation is based on the voltage sensed across the internal sense resistor of the DRV8452. Optional external resistors can be placed between the PGND pins and system ground (or in series with the VM pins) to sense the coil current, as shown in Figure 7-18. The DRV8452 has two PGNDA pins and two PGNDB pins - one pair for each H-bridge. So, the current of each stepper motor coil can be sensed separately by placing sense resistors between PGND pins and system ground. All the four VM pins are shorted internally - so if a sense resistor is placed in the VM path, it will sense the combined current of both the H-bridges.

The voltage drop across the external sense resistor connected between PGND pins and system ground should not exceed 300 mV. The sensed coil current can be processed to monitor motor health, or used to generate necessary signals in a field-oriented-control loop to improve overall system efficiency.

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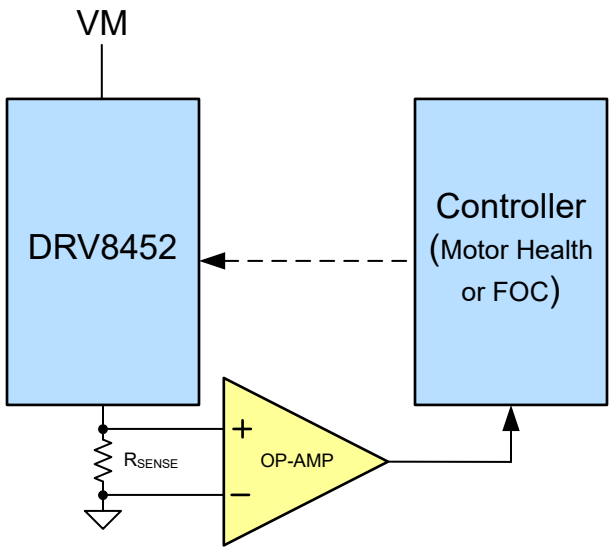

Figure 7-18. Current Sensing with External Resistor

No current flows through the sense resistor during the slow decay, so the sense resistor conducts less than the coil RMS current. Place the sense resistors as close as possible to the corresponding IC pins. Use a symmetrical sense resistor layout to ensure good matching. Low-inductance sense resistors should be used to prevent voltage spikes and ringing. For optimal performance, the sense resistor should be a surface-mount resistor rated for high enough power.

7.3.12 Silent step decay mode

Conventional peak current mode control looks at instantaneous current in the sensing MOSFETs to determine drive and decay durations. As a result, the motor driver reacts to instantaneous inaccuracies in the system. These sudden changes in current cause audible noise from the motor.

To ensure noiseless stepper motor operation, the DRV8452 features the silent step decay mode. The silent step is a voltage mode PWM regulation scheme to remove noise due to PWM switching at standstill and low speeds. Thus, silent step operated stepper motor applications are highly suitable for applications such as 3D printer, medical equipment and factory automation, where low noise operation is critical.

Note

When the device is operating with silent step decay mode -

- Open-load fault detection works only when the motor is in motion, but not if the motor is in standstill.
- Stall detection is not supported.
- Spread spectrum feature is disabled.

The silent step loop is designed for low bandwidth operation, therefore at moderate to high motor speeds, the decay mode can be switched back to one of the conventional current-mode decay schemes programmed by the DECAY bits. Transition from silent step to another decay mode is immediate, whereas the transition from other decay modes to silent step happens at the boundary of electrical half-cycles.

Figure 7-19 shows the block diagram of the silent step decay mode implementation -

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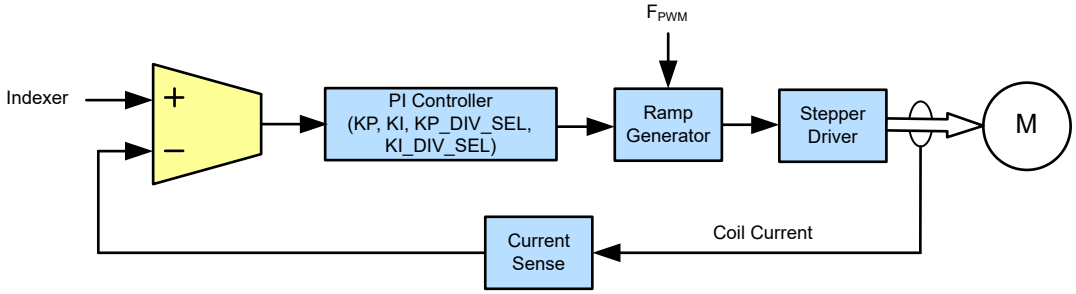

Figure 7-19. Silent step block diagram

Table 7-23 shows the SPI register parameters related to the silent step decay mode.

Table 7-23. Silent step Parameter Table

Parameter	Description
EN_SS	When EN_SS bit is 1b, silent step decay mode is enabled. Device starts operating with silent step after one zero cross each for currents in coil A and coil B. Writing 0b to EN_SS disables silent step decay mode, and the decay mode changes as per DECAY bit setting.
SS_PWM_FREQ[1:0]	Represents the PWM frequency (F_{PWM}) in silent step decay mode. • 00b = 25 kHz (default) • 01b = 33 kHz • 10b = 42 kHz • 11b = 50 kHz Higher PWM frequency results in more switching loss.
SS_SMPL_SEL[1:0]	Silent step current zero cross sampling time. Default value is 2 µs. If current waveform is distorted around zero crossing, increase the sampling time. • 00b = 2 µs (default) • 01b = 3 µs • 10b = 4 µs • 11b = 5 µs
SS_KP[6:0]	Represents the proportional gain of the silent step PI controller. Has a range of 0 to 127, with a default value of 0.
SS_KI[6:0]	Represents the integral gain of the silent step PI controller. Has a range of 0 to 127, with a default value of 0.
SS_KP_DIV_SEL[2:0]	Divider factor for KP. Actual KP = SS_KP / SS_KP_DIV_SEL. • 000b - SS_KP/32 (default) • 001b - SS_KP/64 • 010b - SS_KP/128 • 011b - SS_KP/256 • 100b - SS_KP/512 • 101b - SS_KP/16 • 110b - SS_KP
SS_KI_DIV_SEL[2:0]	Divider factor for KI. Actual KI = SS_KI / SS_KI_DIV_SEL. • 000b - SS_KI/32 (default) • 001b - SS_KI/64 • 010b - SS_KI/128 • 011b - SS_KI/256 • 100b - SS_KI/512 • 101b - SS_KI/16 • 110b - SS_KI

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Table 7-23. Silent step Parameter Table (continued)

Parameter	Description
SS_THR[7:0]	Programs the frequency at which the device transitions from silent step decay mode to another decay mode programmed by the DECAY bits. This frequency corresponds to the frequency of the sinusoidal current waveform. • 00000001b = 2 Hz • 00000010b = 4 Hz • . • . • 11111111b = 510 Hz (default)

To convert the SS_THR threshold to STEP frequency (f_{STEP}) for a specified microstepping setting, Equation 6 should be used -

$$f_{STEP} = (SS\_THR * 1000 * usm) / 256 \quad (6)$$

Where usm corresponds to the number of microsteps (4, 16, 256 etc.). When the device is operating with custom microstepping mode, use usm = 256 in Equation 6 when calculating the STEP frequency.

The gain vs frequency plot of the silent step loop is shown below -

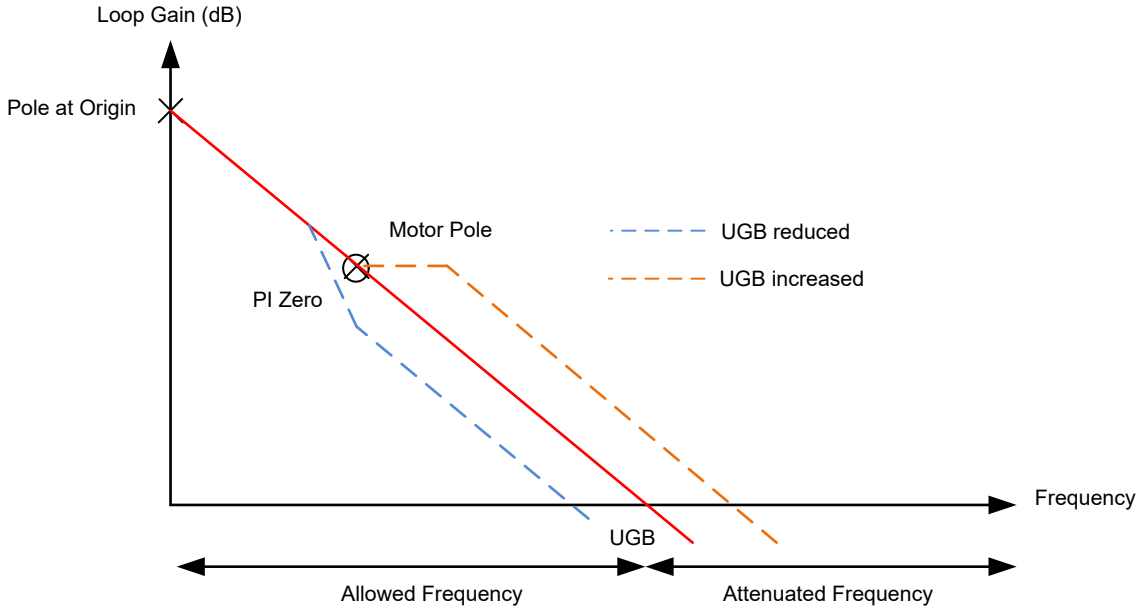

Figure 7-20. Silent step Gain vs. Frequency

The loop transfer function has two poles and one zero -

- One pole at origin
- One pole (f_P) due to the motor coil resistance and inductance -

$$f_P = R_{MOTOR} / (2 * \pi * L_{MOTOR}) \quad (7)$$

- One zero (f_Z) created by the PI loop

$$f_Z = (KI * F_{PWM}) / (2 * \pi * KP) \quad (8)$$

The proportional gain KP should be chosen to achieve the desired loop gain. Use the following equation to calculate the KP -

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$$KP = 10 * \pi * UGB * L_{MOTOR} / VM \quad (9)$$

Where UGB is the unity-gain bandwidth of the loop, R_{MOTOR} is the motor coil resistance, L_{MOTOR} is the motor coil inductance, I_{FS} is the full-scale current and VM is the supply voltage.

- If any frequency is less than UGB, it is allowed to pass.
- Frequencies higher than UGB, such as PWM frequency or STEP frequency are attenuated and do not contribute to motor noise.
- 200 Hz is a reasonable choice for UGB to attenuate most frequencies in the audible range.
- In the event of supply voltage change, UGB can be changed by modifying the value of KP. This way similar audio noise suppression can be achieved across a wide range of operating conditions.
- If the zero is chosen to be at a lower frequency than the motor pole, UGB will increase, as shown in the gain vs frequency plot.

The zero should be placed to cancel the motor pole. By equating f_P and f_Z for a discretized implementation, the following equation can be used to calculate KI.

$$KI = KP * R_{MOTOR} / (F_{PWM} * L_{MOTOR}) \quad (10)$$

As an example, consider the following use case -

- VM = 24 V
- I_{FS} = 5 A
- R_{MOTOR} = 0.3 Ω
- L_{MOTOR} = 0.7 mH
- UGB = 200 Hz
- F_{PWM} = 25 kHz
- Above 50 RPM, the decay mode should change from silent step to smart tune ripple control.

Using the previous equations, KP = 0.18326 and KI = 0.00314. The following register values can be set -

- SS_KP = 0101111b = 47
- SS_KI = 0000001b = 1
- SS_KP_DIV_SEL = 011b = 1/256
- SS_KI_DIV_SEL = 011b = 1/256
- 50 RPM corresponds to roughly 42.6 kpps at 1/256 microstepping, which is equivalent to 42 Hz frequency of the sinusoidal current waveform. So SS_THR = 00010101b = 21.

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Figure 7-21 shows the smooth sinusoidal coil current waveforms when the motor operates in silent step decay mode.

Traces from top to bottom: coil A current, coil B current

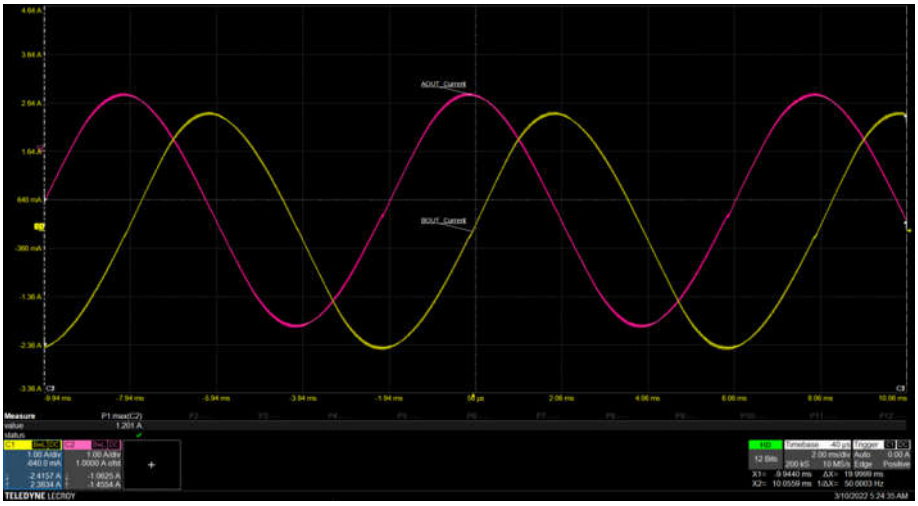

Figure 7-21. Coil Current Waveform with Silent Step Decay

The SS_SMPL_SEL bits influence the smoothness of current waveform around zero crossing point. Default value of 2 µs sampling time will work well for most motors and applications. In case current waveform distortion is oberved around the zero crossing, the value of sampling time can be increased to a maximum of 5 µs. Figure 7-22 is an example of transition from silent step decay mode to smart tune ripple control decay mode with a sampling time of 5 µs.

Traces from top to bottom: AOUT2, AOUT1, coil A current, coil B current, nSCS

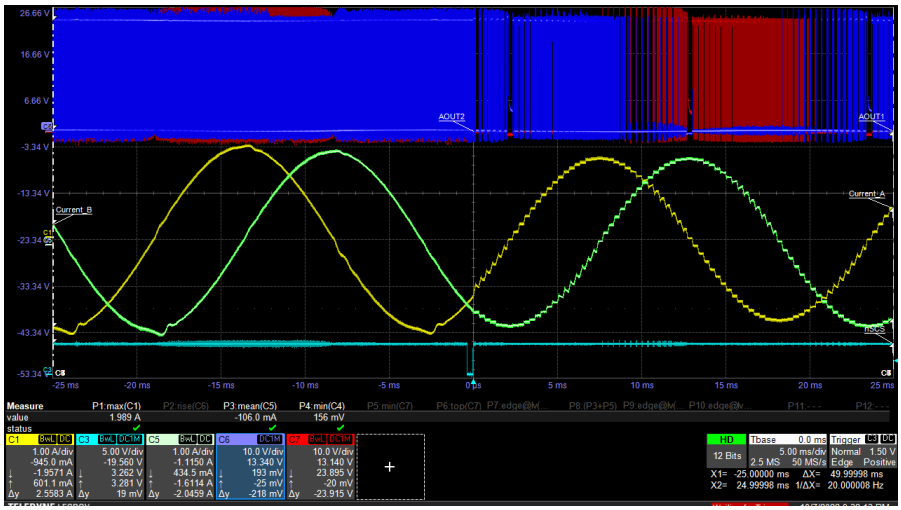

Figure 7-22. Silent step to smart tune transition

7.3.13 Auto-torque Dynamic Current Adjustment

For a typical stepper motor driver, the full-scale current is designed based on the peak load torque demand. This ensures that the motor does not lose steps any time peak load is demanded. The current therefore is constant irrespective of the load torque. As a result, when load torque is lower than the peak load, the driver and the motor dissipate some of the input power as resistive power loss as represented in Figure 7-23.

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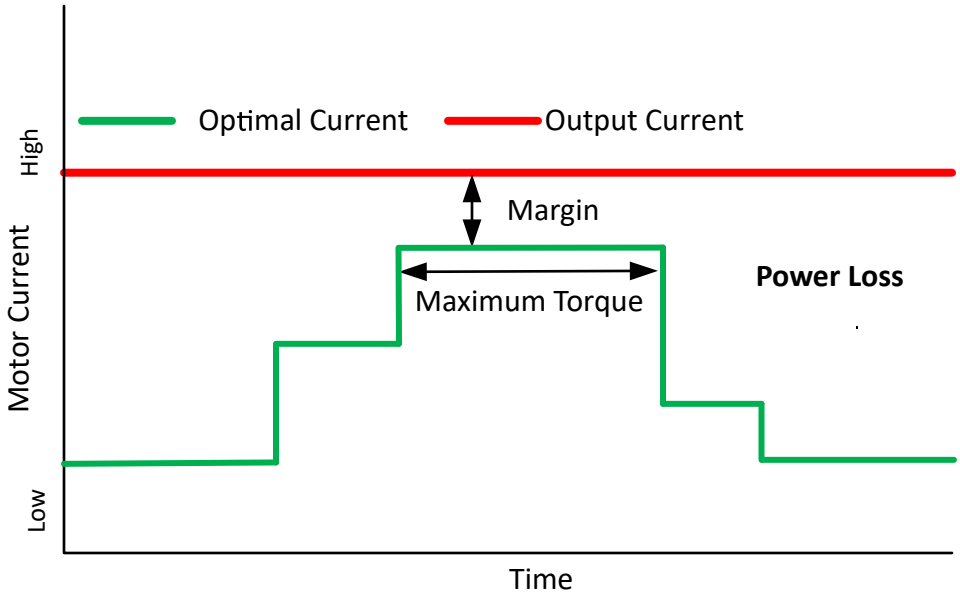

Figure 7-23. Power Loss with Conventional Stepper Driver

In most systems, the demand for peak load torque occurs only rarely. For example, in an ATM machine, the stepper motors might be needed to deliver peak load for less than 15% of their overall run time. A typical stepper driver though ends up delivering full-scale current to the motors all the time - leading to lower system efficiency due to the unwanted power loss, larger system size and shorter lifetime of components.

The Auto-torque algorithm implemented in the DRV8452 improves system efficiency by dynamically changing the output current according to the load torque. Whenever the load torque is low, the output current is lowered to reduce resistive losses; and when the load torque goes up, the output current increases immediately to prevent motor step loss. This concept is shown in Figure 7-24. As a result of improved efficiency due to auto-torque, the system runs at a lower temperature, which extends the lifetime of the components. Auto-torque can also enable the use of cheaper and smaller sized stepper motors.

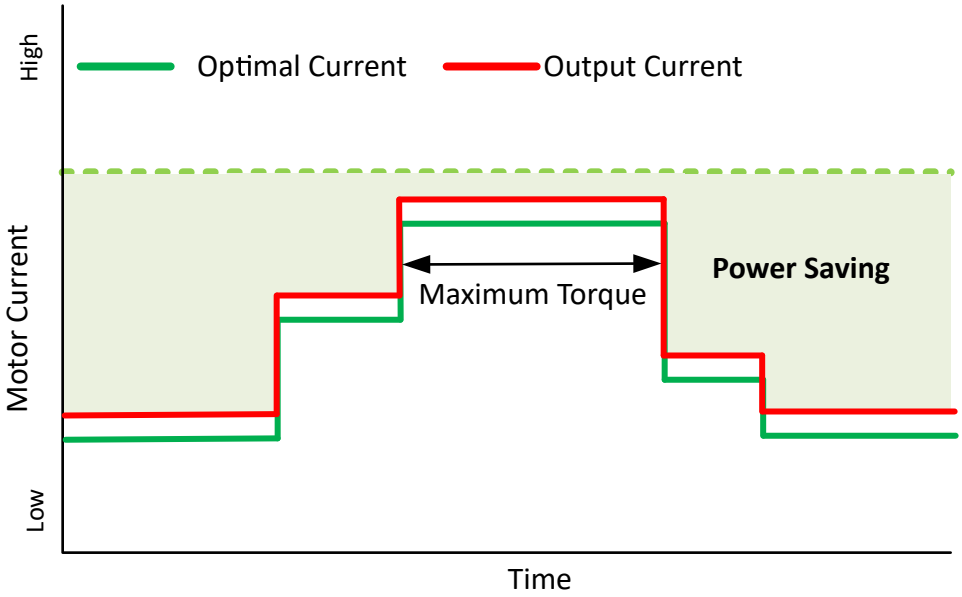

Figure 7-24. Power Saving with Auto-torque

The auto-torque feature is enabled by writing 1b to the ATQ_EN bit.

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7.3.13.1 Auto-torque Learning Routine

In a stepper motor system, the total power delivered by the power supply goes into providing for the torque requirement of the load and into power losses such as resistive losses caused by motor winding resistance and driver ON resistance. This is represented by Equation 11:

$$\text{Power delivered by supply} = \text{Constant losses} + \tau \times \omega \tag{11}$$

where τ is load torque and ω is motor speed.

From Equation 11, we can observe that when the load torque increases, the power delivered by the supply increases as well. The auto-torque algorithm obtains information about the load-torque by monitoring the power delivered by the supply. The constant losses are represented by the ATQ_LRN parameter, and the ATQ_CNT parameter represents the power required to support the load torque.

For any given motor, ATQ_LRN is directly proportional to the coil current. This can be expressed by Equation 12:

$$\text{ATQ\_LRN} = \frac{k \times I_M}{V_{VM}} \tag{12}$$

where I_M is the motor current, V_{VM} is the supply voltage to the driver and k is a constant. Equation 12 gives a linear relationship between the ATQ_LRN and the motor current. The auto-torque learning routine learns ATQ_LRN values at any two currents at no load, and then uses this relation to interpolate ATQ_LRN value at any other current.

The ATQ_CNT parameter represents the component of the delivered power that supports the load torque. This relation can be expressed by Equation 13.

$$\text{ATQ\_CNT} = \frac{k_1 \times \tau \times \omega}{I_{FS}} \tag{13}$$

where k_1 is a constant at a given operating condition and I_{FS} is the full-scale current (peak of the sinusoidal current waveform) of the stepper driver.

Equation 13 defines the basic working principle of the auto-torque algorithm. The ATQ_CNT parameter can be used to perform motor coil current regulation based on applied load torque on the stepper motor.

Figure 7-25 shows (ATQ_LRN + ATQ_CNT) measured as a function of load torque at 2.5A full-scale current for a hybrid bipolar NEMA 24 stepper motor rated for 2.8A. ATQ_LRN does not change with load torque, whereas ATQ_CNT changes linearly with load torque.

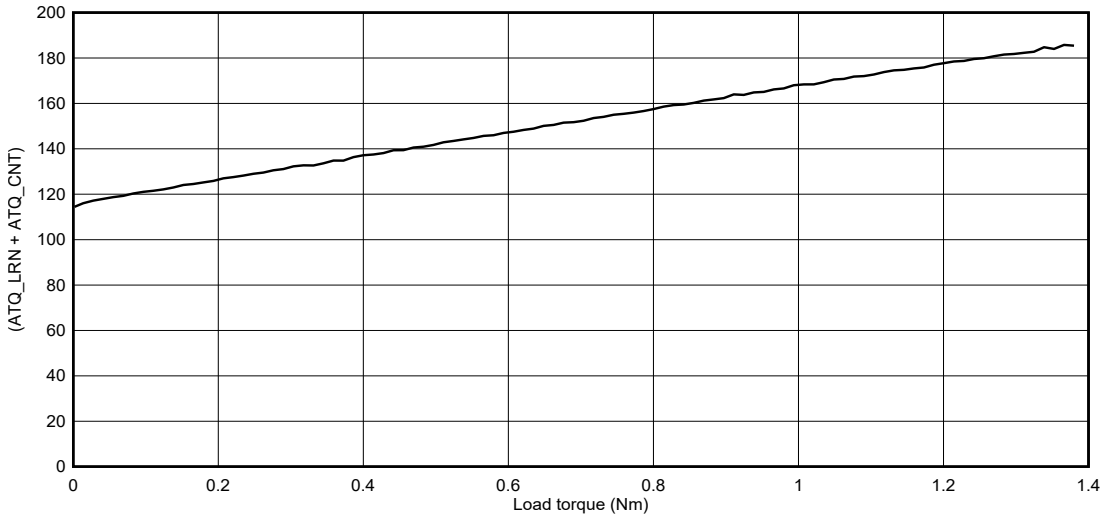

Figure 7-25. (ATQ_LRN + ATQ_CNT) vs. load torque

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After auto-torque algorithm is enabled, the learning routine must be run to estimate the ATQ_LRN parameters.

The learning routine uses the linear relation between ATQ_LRN and motor current described in Equation 12. The user has to select two current values at which learning will be performed, with no load torque applied on the motor. These two current values are programmed by the ATQ_LRN_MIN_CURRENT and ATQ_LRN_STEP registers.

- Initial current level = ATQ_LRN_MIN_CURRENT x 8
- Final current level = Initial current level + ATQ_LRN_STEP

The ATQ_LRN values at these two currents are saved in the ATQ_LRN_CONST1 and ATQ_LRN_CONST2 registers. These two registers are used to interpolate ATQ_LRN value for all other currents within the operating range of the application.

Table 7-24 lists the registers associated with auto-torque learning routine.

Table 7-24. Registers for auto-torque learning routine

Register Name	Description
ATQ_LRN_MIN_CURRENT[4:0]	Represents the initial current level for auto-torque learning routine.
ATQ_LRN_STEP[1:0]	Represents the increment to initial current level. It supports four options - • 00b : ATQ_LRN_STEP = 128 • 01b : ATQ_LRN_STEP = 16 • 10b : ATQ_LRN_STEP = 32 • 11b : ATQ_LRN_STEP = 64 Example : If ATQ_LRN_STEP = 10b and ATQ_LRN_MIN_CURRENT = 11000b, then - • Initial learn current level = 24*8 = 192 • Final learn current level = 192 + 32 = 224
ATQ_LRN_CYCLE_SELECT[1:0]	Represents the number of electrical half cycles spent in one current level after which the learning routine allows the current to jump to the other level. It supports four options - • 00b : 8 half-cycles • 01b : 16 half-cycles • 10b : 24 half-cycles • 11b : 32 half-cycles
LRN_START	Writing 1b to this bit enables the auto-torque learning routine. After learning is completed, this bit automatically goes to 0b.
LRN_DONE	This bit becomes 1b after learning is complete.
ATQ_LRN_CONST1[10:0]	Indicates the ATQ_LRN parameter at the initial learning current level.
ATQ_LRN_CONST2[10:0]	Indicates the ATQ_LRN parameter at the final learning current level.
VM_SCALE	When this bit is 1b, the auto-torque algorithm automatically adjusts the ATQ_UL, ATQ_LL and ATQ_LRN parameters as per the supply voltage variation.

Here are few points to consider while setting up the learning routine parameters:

- It is recommended to select the initial current level between 30% to 50% of the maximum operating current.
- Final current level must not exceed 255 and can be selected between 80% and 100% of the maximum operating current.
- Current waveform distortions (due to high speed or low supply voltage) can cause incorrect reading of the ATQ_LRN parameters. The learning current levels should be chosen away from the currents where waveform distortions are observed.
- Low values of ATQ_LRN_CYCLE_SELECT result in quicker learning. However, in systems prone to noise, higher ATQ_LRN_CYCLE_SELECT can result in more stable ATQ_LRN parameter values.
- Learning should be done when the motor attains the steady-state speed.

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- Re-learning should be done if the motor is changed, or the motor speed changes by ± 10%.

For a quick summary, following sequence of commands should be applied to enable automatic learning:

- Write 1b to ATQ_EN
- Run the motor with no load
- Program ATQ_LRN_MIN_CURRENT
- Program ATQ_LRN_STEP
- Program ATQ_LRN_CYCLE_SELECT
- Write 1b to ATQ_LRN_START
- The algorithm runs the motor with initial current level for ATQ_LRN_CYCLE_SELECT number of electrical half cycles
- Next, the algorithm runs the motor with final current level for ATQ_LRN_CYCLE_SELECT number of electrical half cycles
- After learning is complete,
  - ATQ_LRN_START bit is auto cleared to 0b
  - ATQ_LRN_DONE bit becomes 1b
- ATQ_LRN_CONST1 and ATQ_LRN_CONST2 are populated in their respective registers
- Motor current goes to ATQ_TRQ_MAX

Once the ATQ_LRN_CONST1 and ATQ_LRN_CONST2 are known from the prototyping tests, they can be used for mass production without invoking the learning routine again. The following sequence of commands should be applied in mass production:

- VREF set to the same value as during learning in prototype tests
- Program ATQ_LRN_MIN_CURRENT
- Program ATQ_LRN_STEP
- Program ATQ_LRN_CONST1
- Program ATQ_LRN_CONST2
- Write 1b to ATQ_EN

Figure 7-26 shows the consolidated flowchart of the auto-torque learning routine.

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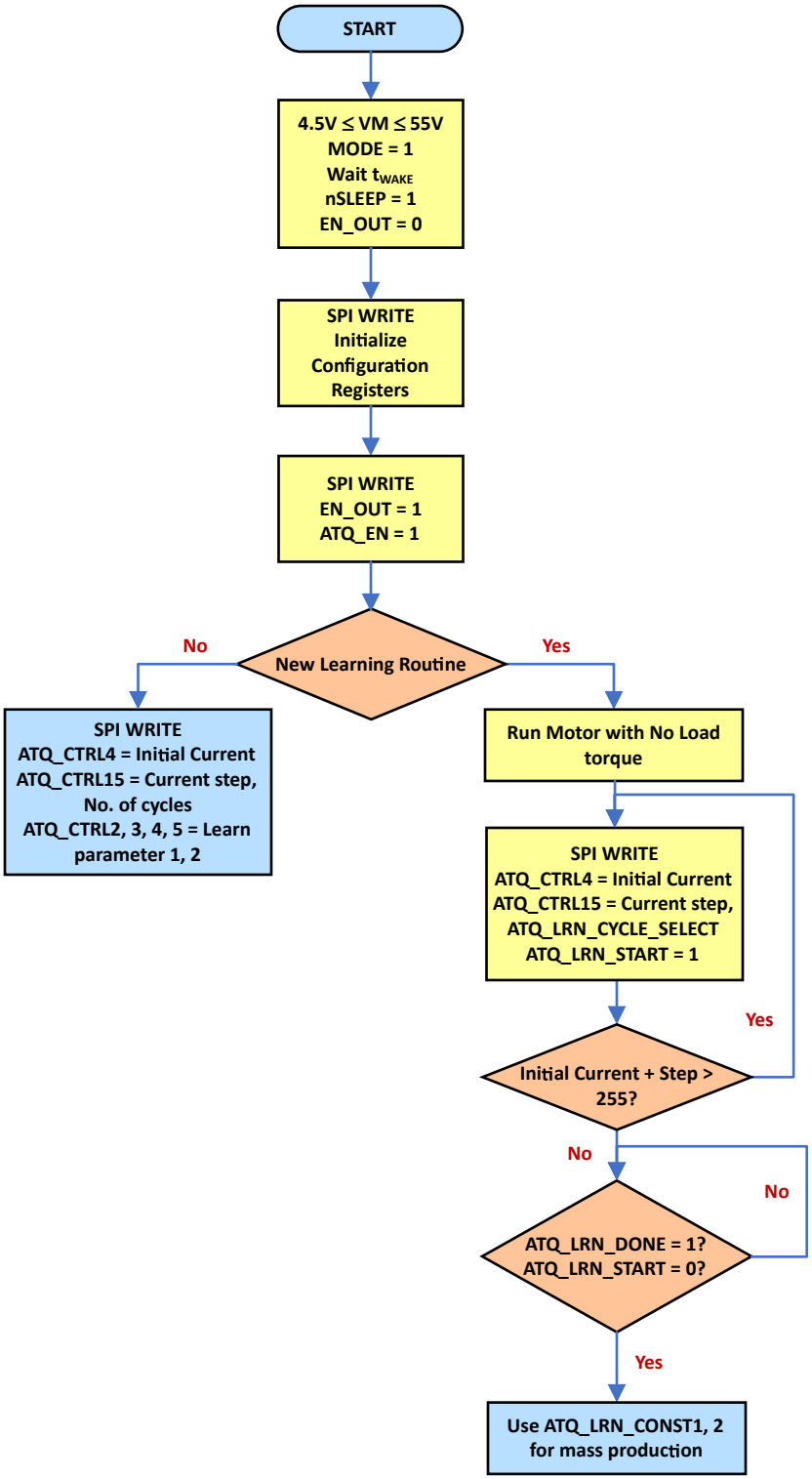

Figure 7-26. Auto-torque Learning Flowchart

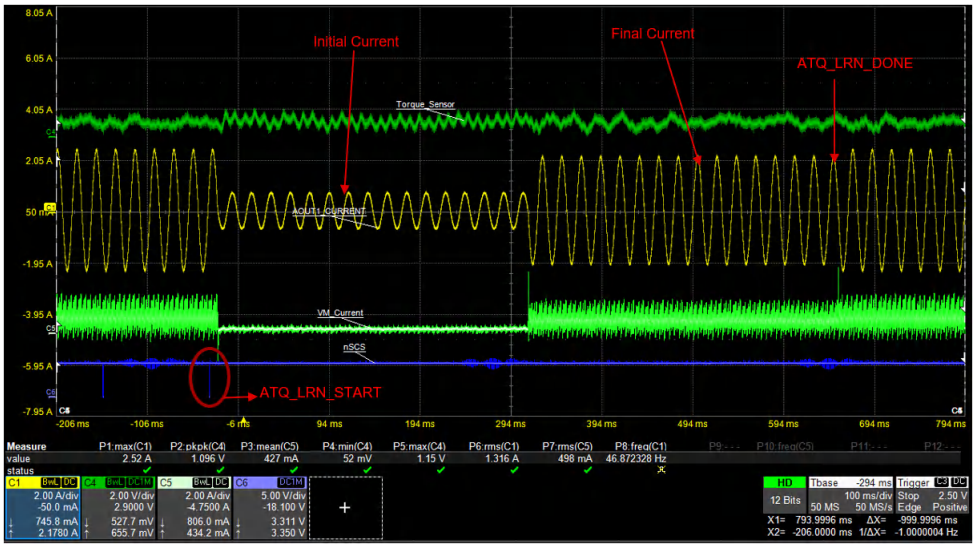

Figure 7-27. Auto-torque learning

Figure 7-27 shows an automatic learning process with 740 mA initial current (I_{FS1}) and 2.2 A final current (I_{FS2}). The ATQ_LEARN_CYCLE_SELECT corresponds to 32 half-cycles.

7.3.13.2 Current Control Loop

Table 7-25 lists the registers associated with current control.

Table 7-25. Registers for Current Control

Parameter	Description
ATQ_UL[7:0] ATQ_LL[7:0]	Upper and lower boundaries of the hysteretic band within which ATQ_CNT is controlled by modifying the motor current.
ATQ_TRQ_MIN[7:0] ATQ_TRQ_MAX[7:0]	Programmable minimum and maximum current limit when auto-torque is enabled.
ATQ_TRQ_DAC[7:0]	Outputs the value of motor current when auto-torque is enabled. ATQ_TRQ_DAC can vary between ATQ_TRQ_MIN and ATQ_TRQ_MAX.
CNT_OFLW	The CNT_OFLW flag becomes 1b if ATQ_CNT is more than ATQ_UL.
CNT_UFLW	the CNT_UFLW flag becomes 1b if ATQ_CNT is less than ATQ_LL.

The ATQ_CNT parameter is proportional to the load torque and inversely proportional to the current setting of the stepper driver. An idealized representation of this relation is shown in Figure 7-28 -

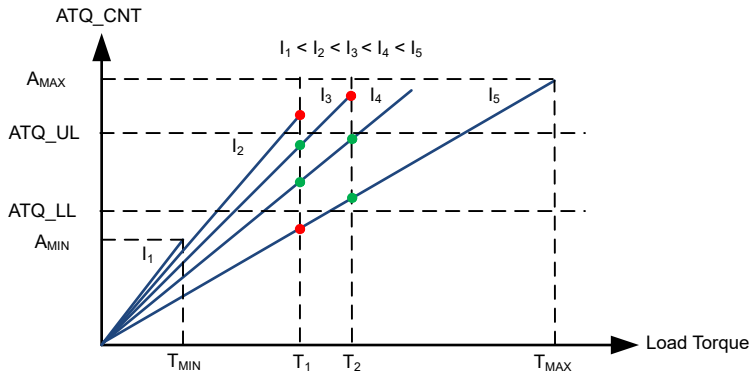

Figure 7-28. ATQ_CNT as a function of load torque

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The auto-torque algorithm confines the ATQ_CNT within the hysteretic band defined by the user programmable ATQ_UL and ATQ_LL parameters, by modulating the motor current, as shown in Figure 7-28.

- If load torque demand increases (T_1 to T_2), the ATQ_CNT goes above the ATQ_UL threshold, and in response, the algorithm brings the ATQ_CNT within the band by increasing the current (I_3 to I_4).
- When load torque demand drops (T_2 to T_1) and ATQ_CNT goes below ATQ_LL, the algorithm reduces the current to bring the ATQ_CNT within the hysteretic band (I_5 to I_4).

The following methodology explains how user should select the values of the current control parameters -

- ATQ_TRQ_MIN is the minimum motor current needed to support the minimum load torque applied to the motor. To find this parameter -
  - Load the motor with minimum load torque (T_{MIN}) and drive the motor with full-scale current (I_{FS})
  - Set ATQ_UL and ATQ_LL to zero and set KP as 1
  - Reduce current till the motor stalls
  - Note the current (I_A) at which the motor stalls
  - Set ATQ_TRQ_MIN = 1.1 x I_A
- To find ATQ_TRQ_MAX -
  - With the motor current at I_A, load the motor with maximum load torque (T_{MAX}). The motor will get stalled.
  - Start increasing the motor current
  - Note the current (I_B) at which the motor comes out of stall
  - Set ATQ_TRQ_MAX = 1.1 x I_B
  - Note the ATQ_CNT (A_{MAX}) with current at ATQ_TRQ_MAX and load torque at T_{MAX}.
- For the ATQ_UL -
  - Set an initial value of 0.5 x A_{MAX}.
  - Apply the load profile (peak load and idle load) specific to the application.
    - If the motor stalls, decrease the value ATQ_UL till the motor is no longer stalled.
    - If the motor does not stall after applying the load profile, ATQ_UL can be increased till the motor stalls.
  - Higher value of ATQ_UL saves more power at peak load, but in case of a fast load transient, the motor can stall.
  - Lower value of ATQ_UL reduces the power saving at peak load, but also reduces the chances of motor stall and step loss.
- For most applications, a difference of 2 between ATQ_UL and ATQ_LL is a good starting point.
- VM_SCALE bit should be made 1b only after ATQ_UL and ATQ_LL have been set by the user.

The flowchart for selecting ATQ_UL, ATQ_LL, ATQ_TRQ_MAX and ATQ_TRQ_MIN parameters is shown below.

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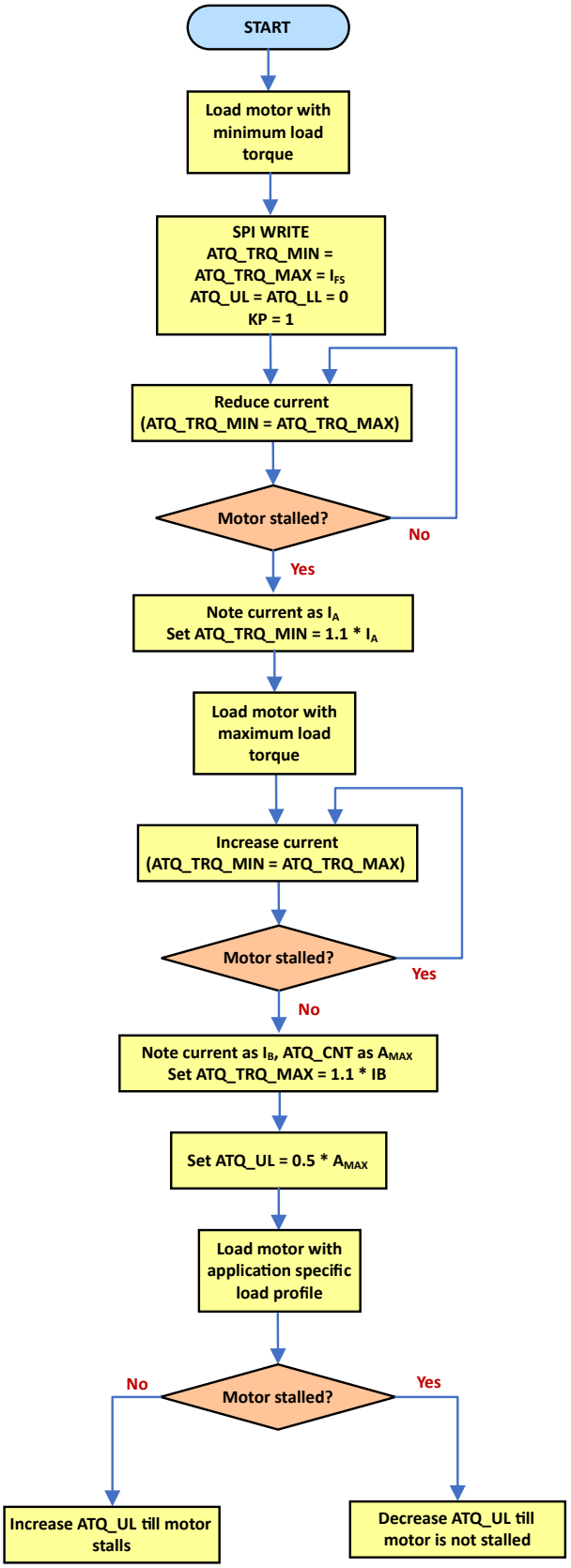

Figure 7-29. Selecting ATQ_TRQ_MIN, ATQ_TRQ_MAX, ATQ_UL, ATQ_LL

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7.3.13.3 PD Control Loop

Table 7-26 describes the major parameters associated with the PD control loop -

Table 7-26. Parameters for PD control loop

Parameter	Description
KP[7:0], KD[3:0]	Proportional and differential gain parameters for the PD control loop.
ATQ_AVG[2:0]	The ATQ_CNT parameter is a moving average of ATQ_AVG number of half-cycles. Therefore, a high value for ATQ_AVG slows down the loop response time to a sudden peak load demand, but ensures smooth jerk-free transition to higher torque output. A low value causes the loop to respond immediately to a sudden load demand. • 010b - 2 cycle average • 100b - 4 cycle average • 111b - 8 cycle average • Other values : no averaging
ATQ_FRZ[2:0]	Delay in electrical half-cycles after which current is changed in response to the PD loop. A small value increases the current quickly to meet peak load demand. This parameter has a range of 1 to 7. 001b - Fastest response time, but the loop can become unstable 111b - Slowest response, but the loop will be stable
ATQ_D_THR[7:0]	If error change is less then ATQ_D_THR, then KD does not contribute to correction. KD contributes only when error change is greater than ATQ_D_THR. For example: if ATQ_D_THR = 10, If error change is 9, u(t) = KP * e(t) If error change is 12, then u(t) = KP * e(t) + KD * de(t)/dt
ATQ_ERROR_TRUNCATE[3:0]	Number of LSB bits truncated from error before used in PD loop equations. A high value reduces any oscillation in the current waveform.

The PD control algorithm is expressed as -

$$u(t) = KP * e(t) + KD * de(t)/dt \quad (14)$$

where,

KP and KD = PD loop constants

$u(t)$ = output of controller

$e(t)$ = error signal

- In general, increasing the KP will increase the speed of the control system response.
- However, if KP is too large, the current waveform will start to oscillate.
- If KP is increased further, the oscillations will become larger. The system will become unstable and may even oscillate out of control.
- Increasing the value of KD will cause the control system to react more strongly to changes in the error term and will increase the speed of the overall control system response.
- It is recommended to use small value of KD, because the derivative response is highly sensitive to noise.
- When non-zero values of KD is selected, to improve noise immunity of the system, a high value of ATQ_D_THR should be used.

Guidelines to tune the PD loop parameters are as follows -

- Set KP = 1, KD = 0, all other PD loop parameters should be at their default values
- Apply load profile specific to the application
- If the motor stalls, increase KP, KD and decrease ATQ_D_THR till the motor stops stalling
- Once the motor does not stall any more, observe the current waveform at constant load torques
- If the current waveform has oscillations, increase ATQ_FRZ, ATQ_AVG and ATQ_ERROR_TRUNCATE

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- Very high values of ATQ_FRZ, ATQ_AVG and ATQ_ERROR_TRUNCATE can deteriorate load transient response, so it is recommended to check load transient response once more to ensure the PD control loop is stable.

Figure 7-30 is the flowchart for selecting PD control loop parameters.

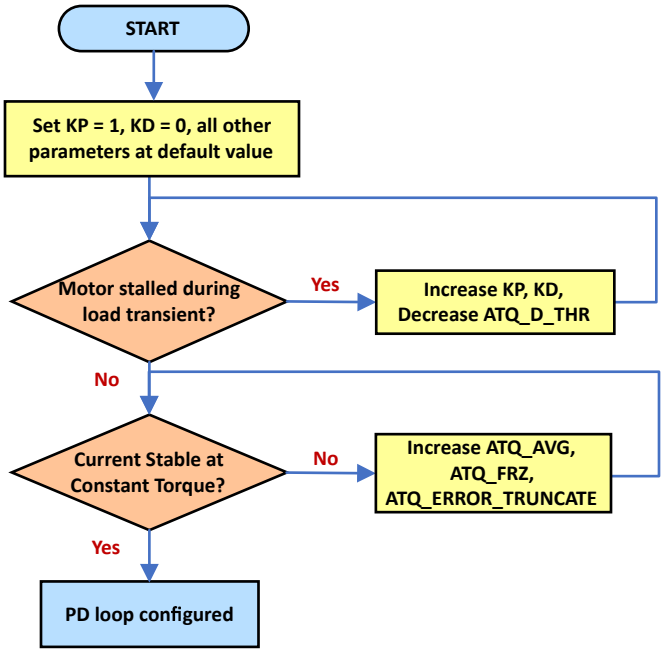

Figure 7-30. Selecting PD control loop parameters

7.3.13.4 Efficiency Improvement with Auto-torque

Table 7-27 shows the thermal performance improvements as a result of auto-torque. The thermal images are captured at the following condition:

VM = 24 V, 1/16 microstep, 4A full-scale current, 3000 pps speed, No load, Room temperature ambient

Table 7-27. Thermal performance improvement with Auto-torque

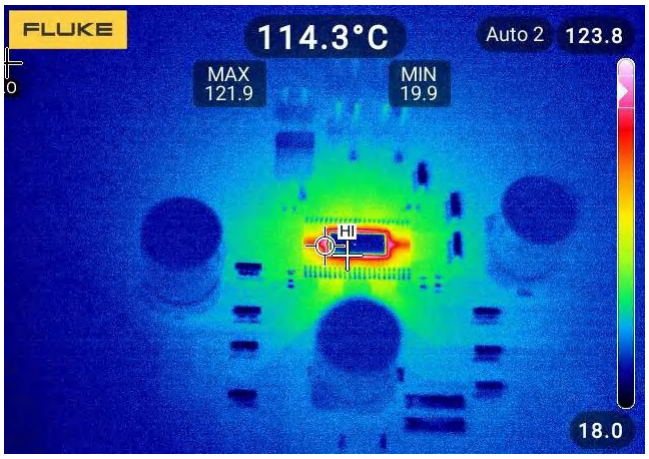	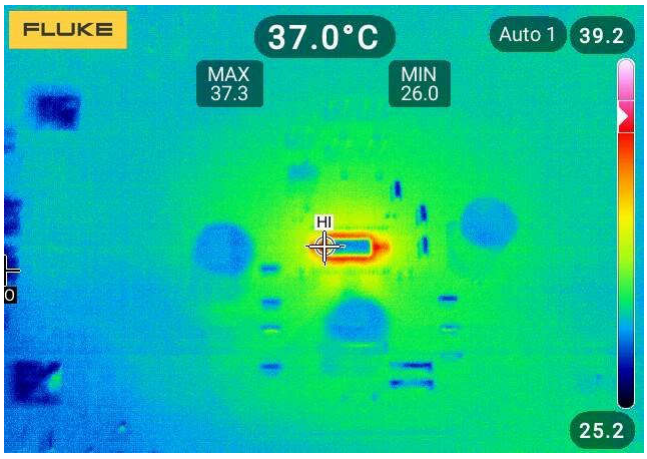
Thermal image: auto-torque disabled, IC temperature = 114.3 °C	Thermal image: auto-torque enabled, IC temperature = 37 °C

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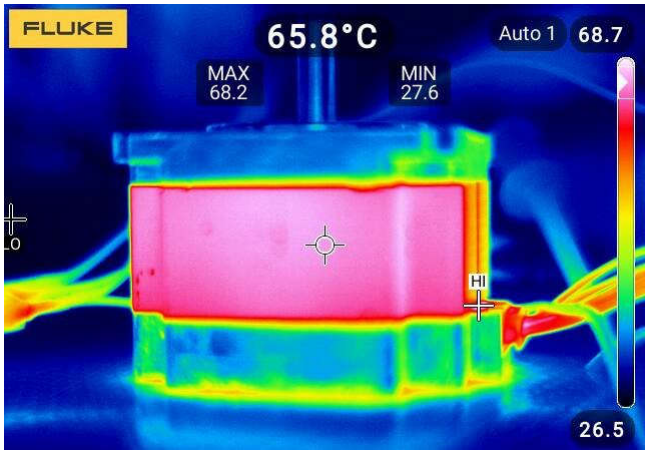
Table 7-27. Thermal performance improvement with Auto-torque (continued)

	
Thermal image: auto-torque disabled, motor temperature = 65.8 °C	Thermal image: auto-torque enabled, motor temperature = 28.1 °C

Reduction in IC and motor temperature as a result of auto-torque improves long term reliability of the stepper motor system.

7.3.14 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

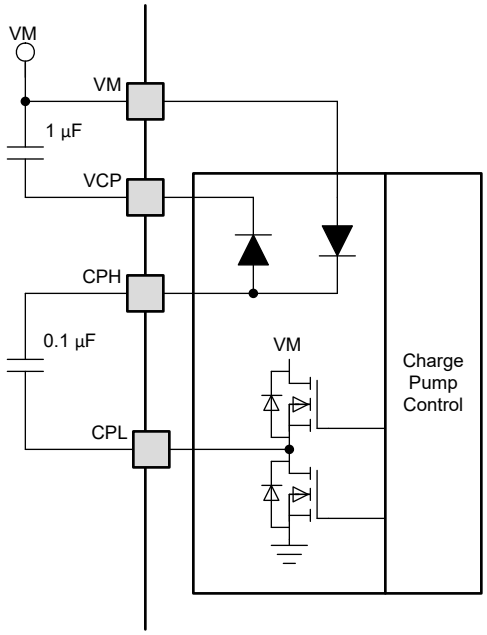


Figure 7-31. Charge Pump Block Diagram

7.3.15 Linear Voltage Regulator

A linear voltage regulator is integrated within the device. When the VCC pin is connected to DVDD, the DVDD regulator provides power to the low-side gate driver and all the internal circuits. For proper operation, bypass the DVDD pin to GND using a 1 µF ceramic capacitor. The DVDD output is nominally 5 V. When the DVDD LDO current load exceeds 5 mA, the output voltage drops significantly.

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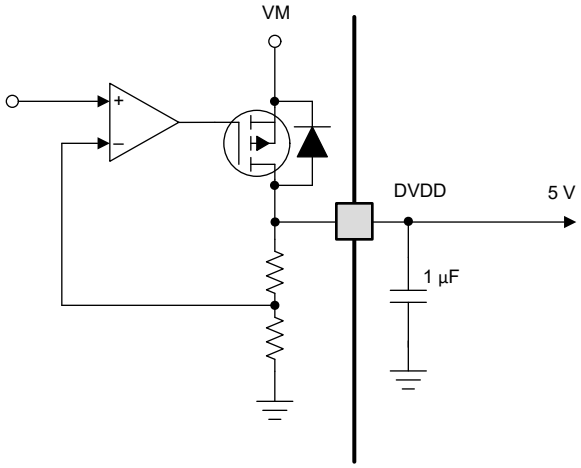

Figure 7-32. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.16 VCC Voltage Supply

An external voltage can be applied to the VCC pin to power the internal logic circuitry. The voltage on the VCC pin should be between 3.05V and 5.5V and should be well regulated. When an external supply is not available, VCC pin must be connected to the DVDD pin of the device.

When powered by the VCC, the internal logic blocks do not consume power from the VM supply rail - thereby reducing the power loss in the DRV8452. This is highly beneficial in high voltage applications, and when thermal conditions are critical. Bypass the VCC pin to ground using a 0.1 µF ceramic capacitor.

7.3.17 Logic Level, Tri-Level and Quad-Level Pin Diagrams

Figure 7-33 shows the input structure for M0, DECAY0 and ENABLE pins.

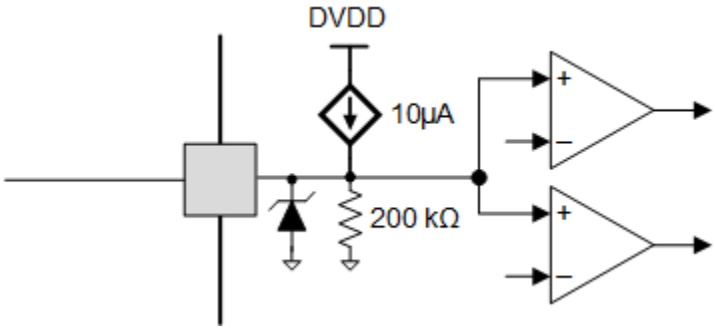

Figure 7-33. Tri-Level Input Pin Diagram

Figure 7-34 shows the input structure for M1 and TOFF pins.

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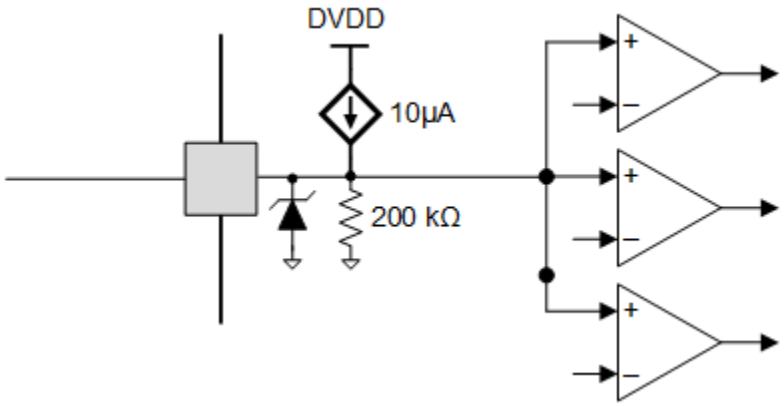

Figure 7-34. Quad-Level Input Pin Diagram

Figure 7-35 shows the input structure for STEP, DIR, MODE, SDI, SCLK, DECAY1 and nSLEEP pins.

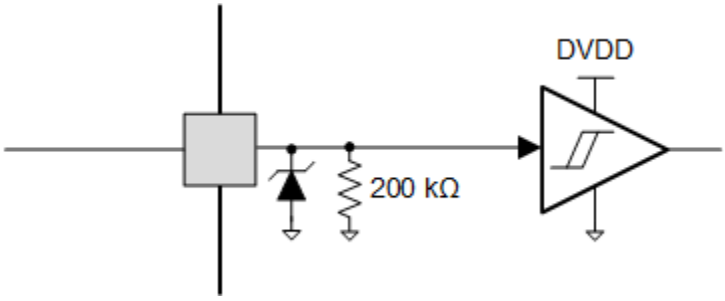

Figure 7-35. Logic-Level Input Pin Diagram

The following diagram shows the input structure for the logic-level pin nSCS.

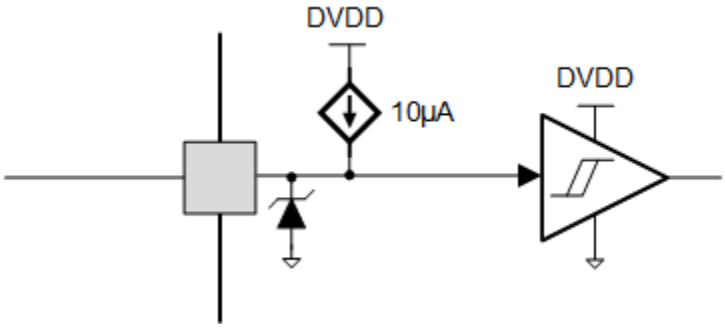

Figure 7-36. nSCS Input Pin Diagram

7.3.18 Spread Spectrum

Spread spectrum or frequency dithering is used to reduce the effect of EMI by converting a narrowband signal into a wideband signal, which will spread the energy across multiple frequencies. Figure 7-37 illustrates how manipulating the clock frequency over time has the effect of spreading the energy.

In the context of the DRV8452, the frequencies of the internal clock for digital circuits (10 MHz typical) and the clock for charge pump (357 kHz typical) are manipulated to reduce the peak energy and is distributed to other frequencies and their harmonics. This feature combined with output slew rate control minimizes the radiated emissions from the device and helps pass strict EMI standards.

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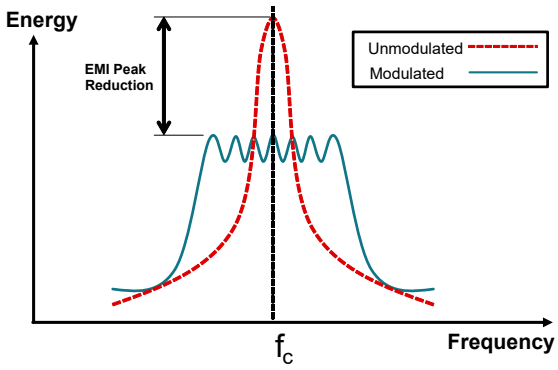

Figure 7-37. EMI Reduction by Spread Spectrum, Frequency Modulation

When the DRV8452 is configured with the SPI interface, spread spectrum can be enabled or disabled by the DIS_SSC bit. By default, spread spectrum is disabled after power-up. Writing 0b to the DIS_SSC bit enables spread spectrum. If the device is operating with silent step decay mode, spread spectrum is disabled. Additionally, when the DRV8452 is configured with the GPIO interface, spread spectrum is disabled.

There are many ways to implement spread spectrum. The DRV8452 uses the triangular analog modulation profile. Figure 7-38 and Figure 7-39 show the spread spectrum profiles of the internal digital clock and the charge pump clock around their respective centre frequencies. The digital clock varies by equal amounts over 14 steps between 9 MHz and 11 MHz.

Note that the centre frequencies themselves will vary with process and temperature changes, and the variations due to spread spectrum will be in addition to those.

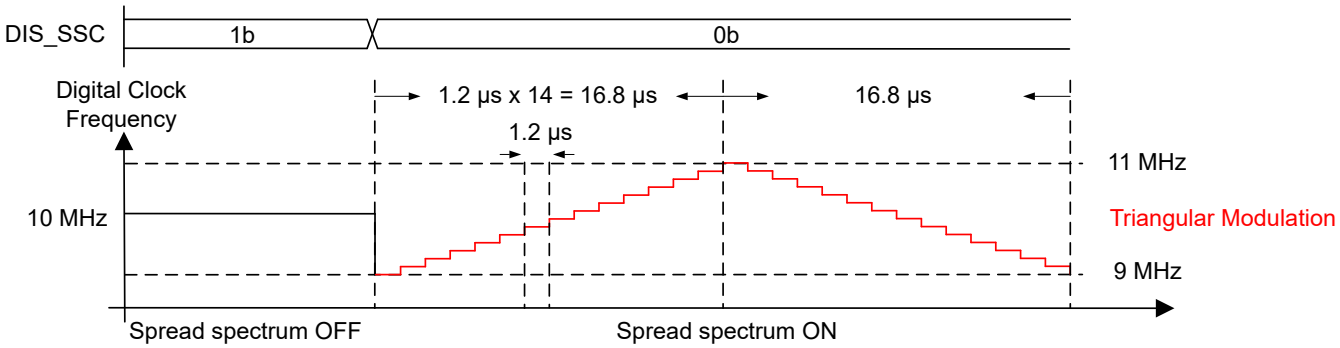

Figure 7-38. Triangular Spread Spectrum of Internal Digital Clock

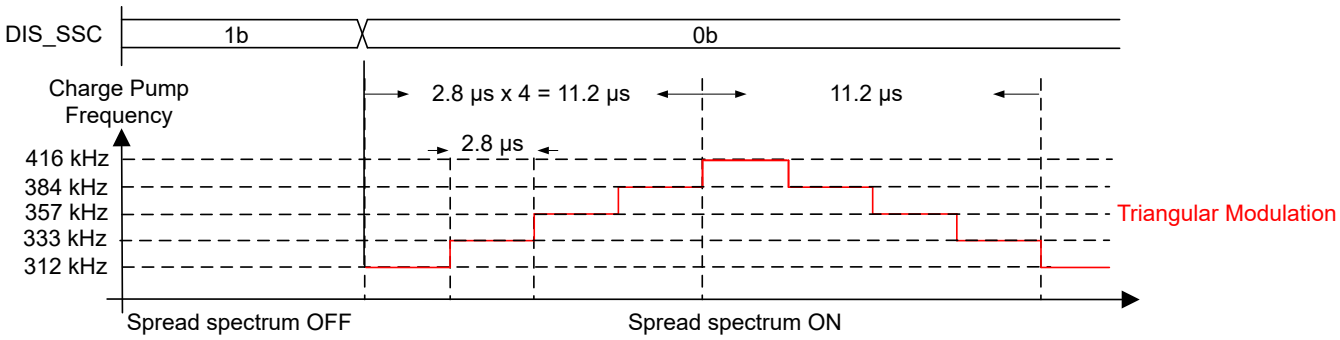

Figure 7-39. Triangular Spread Spectrum of Charge Pump Clock

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7.3.19 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, open load, and device overtemperature events. In addition, when operating with SPI interface, the device is protected against stall detection in the event of overload or end-of-line movement.

7.3.19.1 VM Undervoltage Lockout

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage:

- All the outputs are disabled (High-Z)
- The charge pump is disabled
- nFAULT is driven low

Normal operation resumes (motor driver and charge pump) when the VM voltage recovers above the UVLO rising threshold voltage.

When operating with SPI interface, if the voltage on the VM pin falls below the UVLO falling threshold voltage, but is above the V_{RST} or VCC UVLO (shown in Figure 7-40) :

- SPI communication is available and the digital core of the device is active
- The FAULT and UVLO bits are made 1b
- The nFAULT pin is driven low

From this condition, if the VM voltage recovers above the UVLO rising threshold voltage:

- nFAULT pin is released (is pulled-up to the external voltage)
- The FAULT bit becomes 0b
- The UVLO bit remains latched 1b until cleared through the CLR_FLT bit or an nSLEEP reset pulse.

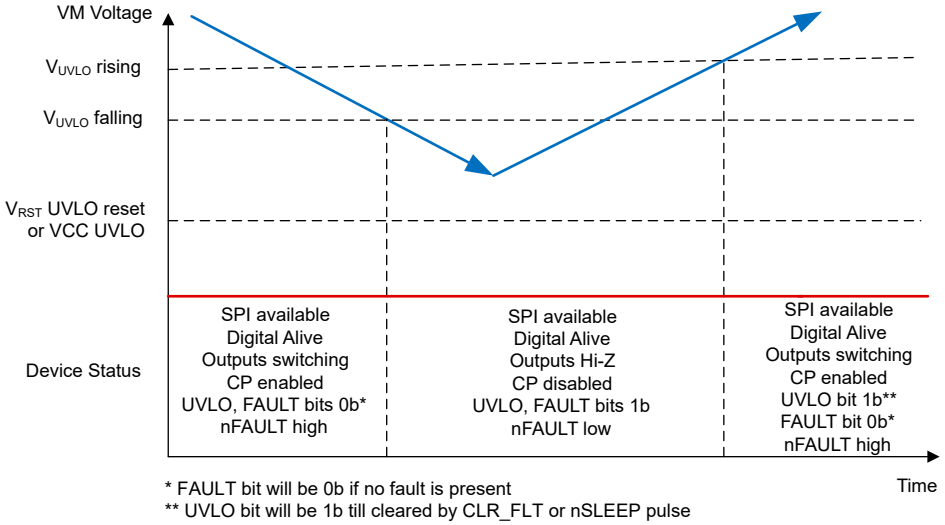

Figure 7-40. Supply Voltage Ramp Profile

When the voltage on the VM pin falls below the V_{RST} or VCC UVLO (shown in Figure 7-41) :

- SPI communication is unavailable and the digital core is shutdown
- The FAULT and UVLO bits are 0b
- The nFAULT pin is high

During a subsequent power-up, when the VM voltage exceeds the V_{RST} voltage:

- The digital core comes alive
- UVLO bit stays at 0b
- The FAULT bit is made 1b
- The nFAULT pin is pulled low
- When the VM voltage exceeds the VM UVLO rising threshold

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– FAULT bit becomes 0b
– UVLO bit stays at 0b
– nFAULT pin is pulled high.

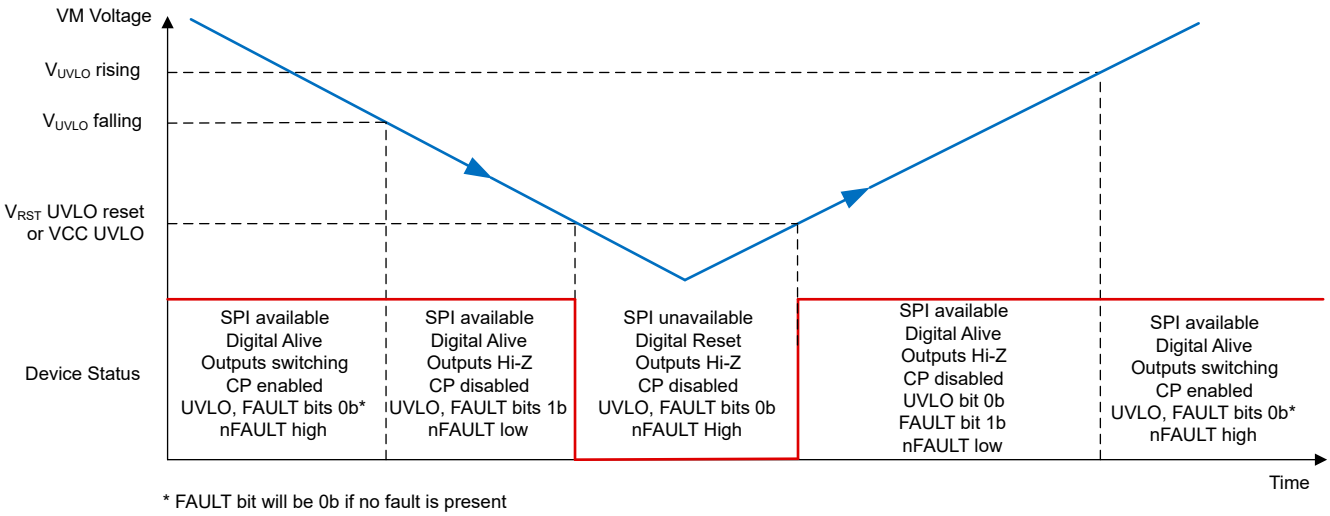

Figure 7-41. Supply Voltage Ramp Profile

7.3.19.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump remains active
- For the SPI version, the FAULT and CPUV bits are made 1b

Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains at 1b until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

7.3.19.3 Logic Supply Power on Reset (POR)

If at any time the voltage on the VCC pin falls below the VCC_{UVLO} threshold:

- All the outputs are disabled (High-Z)
- Charge pump is disabled.

VCC UVLO is not reported on the nFAULT pin. Normal motor-driver operation resumes when the VCC undervoltage condition is removed.

When device operates with SPI interface:

- The NPOR bit is reset and latched 0b once VCC goes above the UVLO threshold.
- NPOR remains in reset condition until cleared through the CLR_FLT bit or nSLEEP reset pulse.
- After power up, NPOR is automatically latched 1b once the CLR_FLT command is issued.

The VCC UVLO scenario is shown in Figure 7-42.

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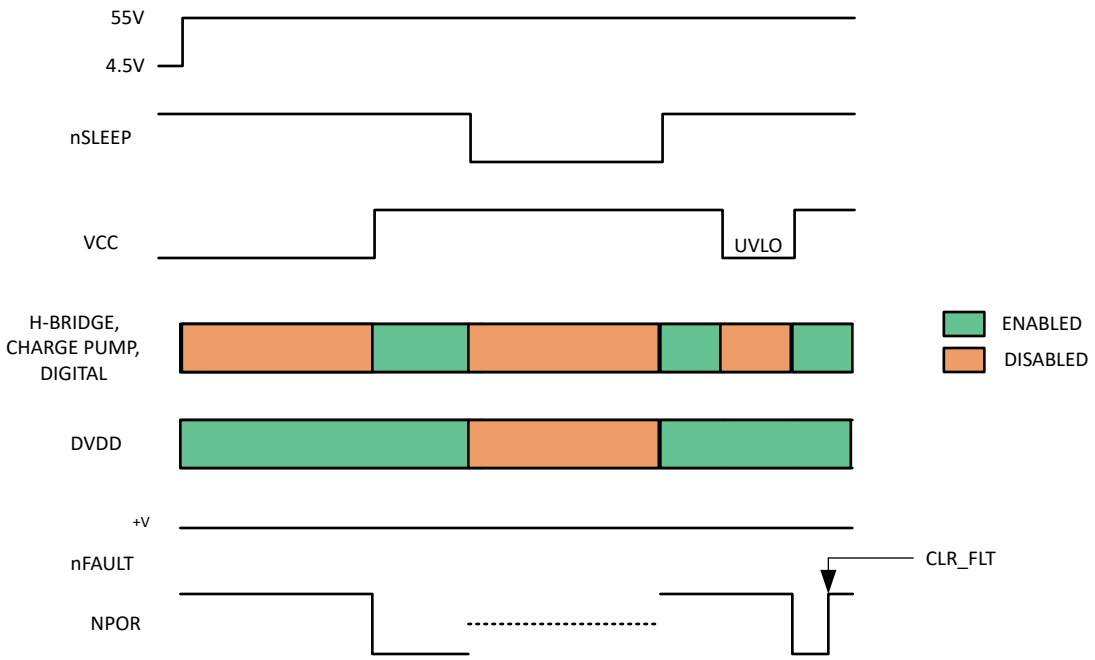

Figure 7-42. Logic Supply POR

7.3.19.4 Overcurrent Protection (OCP)

An analog current-limit circuit on any MOSFET limits the current through that MOSFET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, an overcurrent fault is detected.

- The MOSFETs in both H-bridges are disabled
- nFAULT is driven low
- Charge pump remains active.
- When operating with SPI interface -
  - FAULT and OCP bits are latched 1b
  - For xOUTy to VM short, corresponding OCP_LSy_x bit becomes 1b
  - For xOUTy to ground short, corresponding OCP_HSxy_x bit becomes 1b
  - The TOCP bit programs the overcurrent protection deglitch time.

The overcurrent protection can operate in two different modes: latched shutdown and automatic retry. The operating modes can be changed on the fly.

7.3.19.4.1 Latched Shutdown

To select latched shutdown mode:

- For H/W interface, the ENABLE pin has to be Hi-Z
- For SPI interface, the OCP_MODE bit should be 0b

In this mode, once the OCP condition is removed, normal operation resumes after applying a CLR_FLT command, an nSLEEP reset pulse or a power cycling.

7.3.19.4.2 Automatic Retry

To select automatic retry mode:

- For H/W interface, the ENABLE pin has to be HIGH (> 2.7 V)
- For SPI interface, the OCP_MODE bit should be 1b

In this mode, normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

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7.3.19.5 Stall Detection

When operating with the SPI interface, the DRV8452 supports stall detection.

Stepper motors have a distinct relation between the winding current, back-EMF, and mechanical torque load of the motor, as shown in Figure 7-43. For an unloaded motor, the back-EMF is 90° out-of-phase with the winding current. As motor load approaches the maximum torque capability of the motor for a given winding current, the back-EMF will move in phase with the winding current. By detecting back-EMF phase shift between rising and falling current quadrants of the motor current, the DRV8452 can detect a motor overload stall condition or an end-of-line travel.

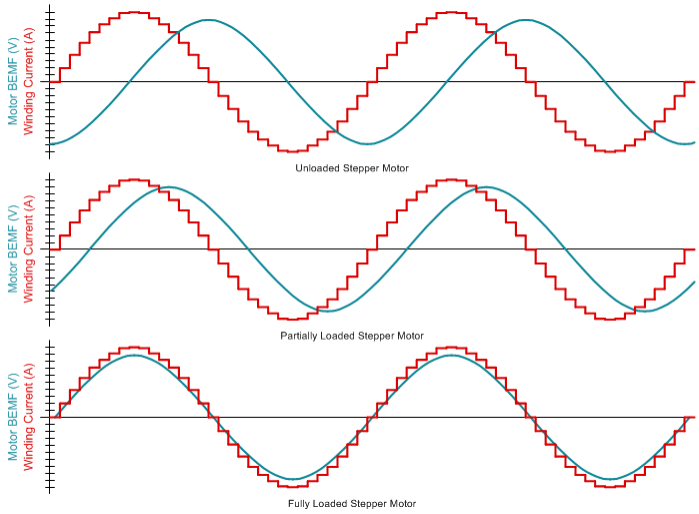

Figure 7-43. Stall Detection by Monitoring Motor Back-EMF

The Stall Detection algorithm is enabled when -

- The device is programmed to operate with the SPI interface (MODE = 1)
- The decay mode is programmed as smart tune Ripple Control (DECAY = 111b)
- EN_STL is 1b
- No fault condition exists (UVLO, OCP, OL, OTSD etc.).

The algorithm compares the back-EMF between the rising and falling current quadrants by monitoring PWM off time and generates a parameter called torque count, represented by the TRQ_COUNT register. The comparison is done in such a way that the TRQ_COUNT is largely independent of motor current, ambient temperature and supply voltage. Motor stall can be detected even if the driver is operating in full step mode.

TRQ_COUNT is calculated as a running average from the most recent four electrical half-cycles. TRQ_COUNT register is updated once every electrical half-cycle. The updated TRQ_COUNT is compared with the STALL_TH, and if a stall condition is detected, stall fault will be reported and latched at the electrical half-cycle current zero crossing.

For a lightly loaded motor, the TRQ_COUNT will be a non-zero value. As the motor approaches stall condition, TRQ_COUNT will approach zero and can be used to detect stall condition.

- If anytime TRQ_COUNT falls below the stall threshold (represented by the STALL_TH register), the device will detect a stall.
- STALL, STL and FAULT bits are latched 1b in the SPI register.
- The STL_REP bit controls how stall is reported.
  - If STL_REP is 1b, the nFAULT pin will be driven low when a stall is detected.
  - If STEL_REP is 0b, the nFAULT pin will stay high even if stall is detected.

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In the stalled condition, the motor shaft does not spin. The motor starts to spin again when the stall condition is removed and the motor ramps to its target speed. The nFAULT is released and the fault registers are cleared when a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

High motor coil resistance can result in low TRQ_COUNT. The TRQ_SCALE bit allows scaling up low TRQ_COUNT values, for ease of further processing.

- If the initially calculated TRQ_COUNT value is less than 500 and the TRQ_SCALE bit is 1b, then the TRQ_COUNT output in register is multiplied by a factor of 8.
- If the TRQ_SCALE bit is 0b, TRQ_COUNT retains the value originally calculated by the algorithm.

Stall threshold can be set in two ways –

- The user can write the STALL_TH bits by observing the behavior of the TRQ_COUNT output at all operating conditions.
- The algorithm can learn the stall threshold using the automatic stall learning process, described below:
  - Before learning, ensure that the motor has reached its target speed. Do not learn stall threshold while the motor speed is ramping up or down.
  - Start learning by setting the STL_LRN bit to 1b.
  - Run motor with no load.
  - Wait for 32 electrical cycles for the driver to learn the steady-state count.
  - Stall the motor.
  - Wait for 16 electrical cycles for the driver to learn the stall count.
  - The STL_LRN_OK bit becomes 1b if learning is successful.
  - Stall threshold is calculated as the average of steady count and stall count and stored in the STALL_TH register.

The flowchart on how to set stall threshold is shown below.

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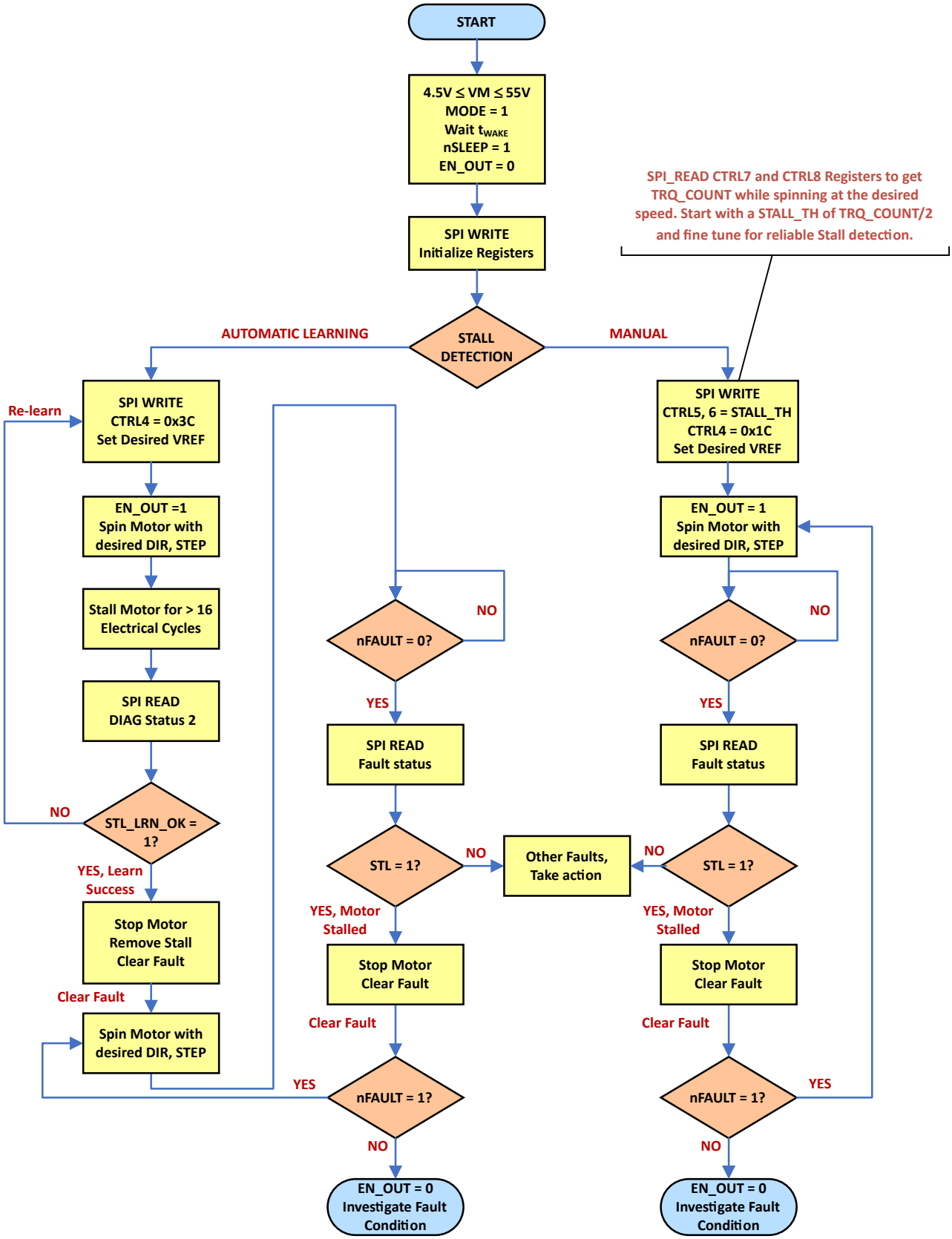

Figure 7-44. Stall learning flowchart

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Sometimes the automatic stall learning process might not be successful due to unstable torque count while the motor is running or is stalled. For example, when the motor has high coil resistance or is running at very high or low speeds, the torque count might vary a lot over time and the difference between steady count and stall count might be small. In such cases, it is recommended not to use the automatic stall learning method. Instead, the user should carefully study the steady count and torque count across the range of operating conditions and set the threshold midway between the minimum steady count and the maximum stall count.

A stall threshold learnt at one speed may not work well for another speed. It is recommended to re-learn the stall threshold every time the motor speed is changed by more than ± 10%.

Note

- The stall detection algorithm depends on back-EMF modifying the PWM off time. The back-EMF is directly proportional to the speed of the motor. In order for stall detection to work reliably, motor speed should be sufficiently high to be able to generate back-EMF of sufficient amplitude. Higher motor coil resistance would require higher minimum speed for reliable stall detection.
- When the device goes from Disable mode (H-bridges Hi-z) to Active mode by toggling EN_OUT bit or ENABLE pin; or when the device recovers from a fault by issuing a CLR_FLT, stall detection fault may also be flagged. This is because of the time taken by TRQ_CNT to reach a value higher than STL_TH. As a result of the stall fault, nFAULT may stay low (if STL_REP = 1b), and another CLR_FLT will be needed to release stall fault and nFAULT pin. This can be prevented by -
  - Enabling stall detection after enabling active mode (write EN_STALL = 1b only after writing EN_OUT = 1b and making ENABLE = logic high)
  - By starting the STEP pulses only after the bridge is in active mode or after a CLR_FLT command has been issued to clear a fault condition.
- If there is loss of current regulation due to low supply voltage, high coil resistance or high speed of the motor, stall detection may not work reliably, because the TRQ_COUNT can be erratic and may jump to a high value. This can be checked and confirmed by looking at the coil current waveform. If the coil current has a standard sinusoidal waveform, and the peak of the sinusoid reaches the desired full-scale current, then stall detection will work reliably. If the current waveform is triangular due to high speed or low supply voltage, stall detection algorithm might not work reliably.
- If EN_STL = 1b and auto-torque is also enabled, coil current goes to ATQ_TRQ_MAX when motor stall is detected.
- If EN_STL = 0b and auto-torque is enabled, coil current goes to ATQ_TRQ_MIN when motor is stalled.

7.3.19.6 Open-Load Detection (OL)

Open-load fault is detected -

- When the motor is running -
  - If coil current drops below the open-load current threshold (I_{OL})
- When the motor is in a holding condition -
  - If coil current drops below the I_{TRIP} level set by the indexer
- If either of the above conditions persists for more than the open-load detection time (t_{OL})

When the device is operating with SPI interface, the EN_OL bit must be 1b to enable open-load detection.

The open-load detection time (t_{OL}) is set as shown in Table 7-28 -

Table 7-28. Open-load Detection Time

Interface	OL_T	Maximum t_{OL} (ms)
H/W interface	NA	60

Table 7-28. Open-load Detection Time (continued)

Interface	OL_T	Maximum t_{OL} (ms)
SPI interface	00b	30
	01b (default)	60
	10b	120

Once the open-load fault is detected -

- nFAULT is pulled low.
- If the device is operating with SPI interface -
  - OL and FAULT bits are latched 1b
  - If the OL_A bit is 1b, it indicates an open load fault in winding A, between AOUT1 and AOUT2.
  - An open load fault between BOUT1 and BOUT2 causes the OL_B bit to become 1b.

When the open-load condition is removed, the behavior depends on whether the device is configured with H/W interface or SPI interface.

When the device is configured with H/W interface and open-load condition is removed:

- If the ENABLE pin is logic HIGH, nFAULT is released immediately.
- If the ENABLE pin is Hi-Z, nFAULT is released after a nSLEEP reset pulse has been applied.

When the device is configured with SPI interface and open-load condition is removed:

- If the OL_MODE bit is 1b, nFAULT is released immediately. OL bit in FAULT register and OL_X bits in DIAG2 register are cleared only after a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.
- If the OL_MODE bit is 0b, nFAULT and the fault bits are released after a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

The open-load fault also clears when the device is power cycled or comes out of sleep mode.

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Figure 7-45 and Figure 7-46 show open-load detection in cases where coil A and coil B were opened respectively. The open load detection time was selected to be 60 ms maximum, and the OL_MODE bit was 0b.

Traces from top to bottom: AOUT2, coil A current, coil B current, nFAULT

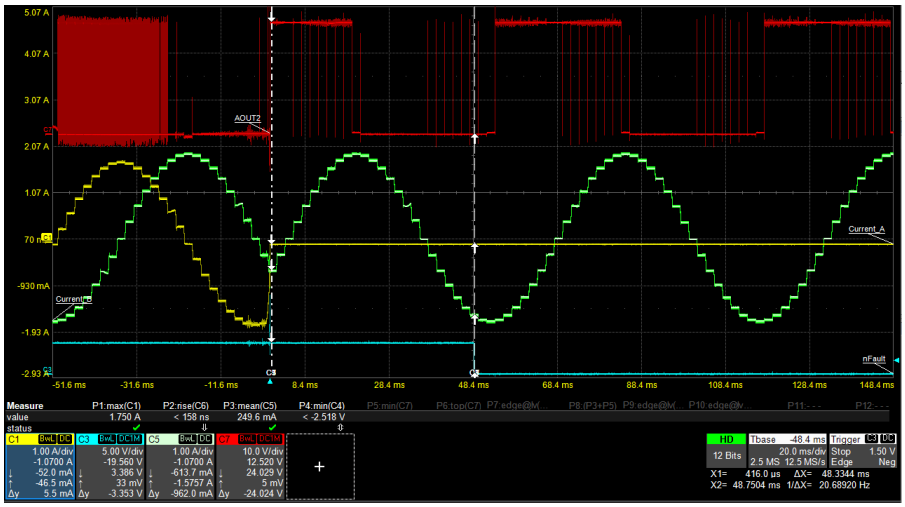

Figure 7-45. Coil A open-load detection

Traces from top to bottom: AOUT2, coil A current, coil B current, nFAULT

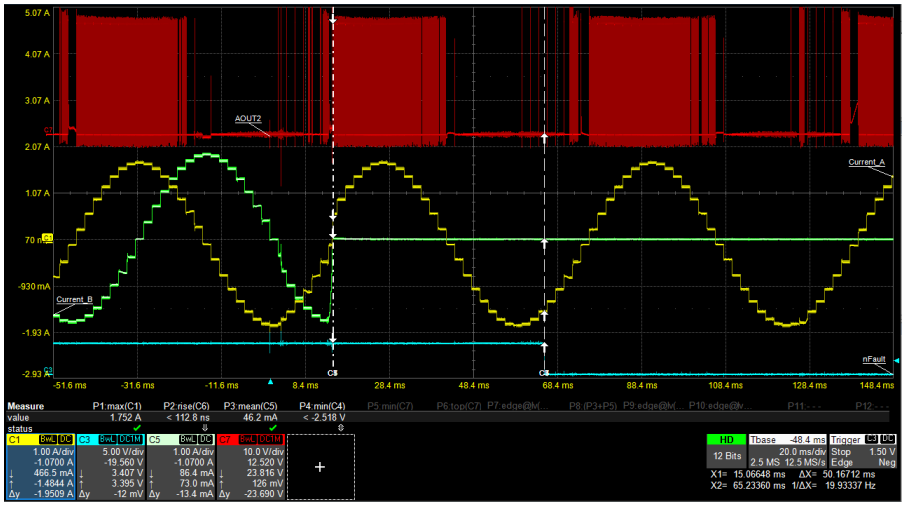

Figure 7-46. Coil B open-load detection

Note

- In silent step decay mode, open-load fault detection works only if the motor is in motion. If the motor is in standstill, open-load detection is not supported.
- When open-load fault is detected -
  - If ENABLE pin is changed from logic HIGH to Hi-Z on-the-fly, apply a nSLEEP reset pulse once the open-load condition is removed.
  - If OL_MODE is changed from 1b to 0b or EN_OL is changed from 1b to 0b, apply a clear faults command once the open-load condition is removed.
- When the device is operating with auto-torque enabled, if open-load fault is detected, the coil current goes to a value corresponding to TRQ_DAC.

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7.3.19.7 Overtemperature Warning (OTW)

Overtemperature warning is detected if the die temperature exceeds the trip point of the overtemperature warning (T_{OTW}). This feature is supported only if the device is operating with SPI interface.

When the OTW is detected -

- OTW and TF bits are made 1b
- The device performs no additional action and continues to function.
- The charge pump remains active.
- If the TW_REP bit is 1b -
  - nFAULT is pulled low in the event of OTW
  - FAULT bit is made 1b

When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW and TF bits clear automatically.

7.3.19.8 Thermal Shutdown (OTSD)

Thermal shutdown is detected if the die temperature exceeds the thermal shutdown limit (T_{OTSD}). When thermal shutdown is detected -

- All MOSFETs in the H-bridges are disabled
- nFAULT is driven low
- Charge pump is disabled
- For operation with SPI interface
  - FAULT, TF and OTS bits are set to 1b

The recovery from thermal shutdown protection can be in two different modes: latched shutdown and automatic retry. The recovery modes can be changed on the fly.

7.3.19.8.1 Latched Shutdown

To select latched shutdown mode,

- If device is operating with H/W interface, the ENABLE pin should be Hi-Z
- If device is operating with SPI interface, OTSD_MODE should be 0b

In this mode, after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.19.8.2 Automatic Retry

To select automatic retry mode,

- For H/W interface, the ENABLE pin has to be logic HIGH (>2.7V)
- For SPI interface, OTSD_MODE bit should be 1b

In this mode, normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$). When operating with SPI interface, the TF and OTS bits remain latched to 1b indicating that a thermal event occurred until a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

7.3.19.9 Supply voltage sensing

An internal ADC monitors the supply voltage applied to the motor driver and outputs the value on the VM_ADC bits in the CTRL14 register. The default value is 01011b, corresponding to 24 V.

This supply voltage reading can be used to implement overvoltage protection by the controller, by disabling the motor driver when the supply voltage exceeds a predetermined threshold.

7.3.19.10 nFAULT Output

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. nFAULT pin will be high after power-up. When a fault is detected, the nFAULT pin will be logic low. For a 5-V pullup, the

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nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

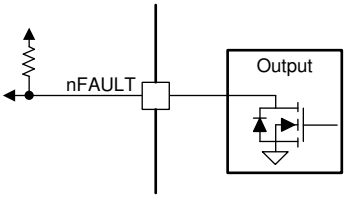

Figure 7-47. nFAULT Pin

7.3.19.11 Fault Condition Summary

Table 7-29. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT / SPI	Disabled	Disabled	Disabled	Reset	VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	—	nFAULT / SPI	Disabled	Operating	Operating	Operating	VCP > V_{CPUV}
Logic Supply POR	VCC < VCC_{UVLO}	—	SPI	Disabled	Disabled	Disbaled	Reset	VCC > VCC_{UVLO}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	OCP_MODE = 0b / ENABLE = Hi-Z	nFAULT / SPI	Disabled	Operating	Operating	Operating	Latched: CLR_FLT / nSLEEP reset pulse
		OCP_MODE = 1b / ENABLE = 1	nFAULT / SPI	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	OL_MODE = 1b / ENABLE = 1	nFAULT / SPI	Operating	Operating	Operating	Operating	Automatic
		OL_MODE = 0b / ENABLE = Hi-Z	nFAULT / SPI	Operating	Operating	Operating	Operating	Latched: CLR_FLT / nSLEEP reset pulse
Stall Detection (STALL)	Stall / stuck motor	STL_REP = 0b	SPI	Operating	Operating	Operating	Operating	CLR_FLT / nSLEEP reset pulse
		STL_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	
Overtemperature Warning (OTW)	T_J > T_{OTW}	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Automatic: T_J < T_{OTW} - T_{HYS_OTW}
		TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	
Thermal Shutdown (OTSD)	T_J > T_{OTSD}	OTSD_MODE = 0b / ENABLE = Hi-Z	nFAULT / SPI	Disabled	Disabled	Operating	Operating	Latched: CLR_FLT / nSLEEP reset pulse
		OTSD_MODE = 1b / ENABLE = 1	nFAULT/ SPI	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.3.20 Device Functional Modes

7.3.20.1 Sleep Mode

When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs, the DVDD regulator, SPI and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.3.20.2 Disable Mode

The ENABLE pin is used to enable or disable the half bridges in the device. When the ENABLE pin is low, the output drivers are disabled (Hi-Z). For operation with SPI interface, the EN_OUT bit can also be used to disable the output drivers, as shown in Table 7-30. When the EN_OUT bit is 0b, the output drivers are disabled (Hi-Z).

Table 7-30. Conditions to Enable or Disable Output Drivers

nSLEEP	ENABLE	EN_OUT	H-BRIDGE
0	X	X	Disabled
1	0	0b	Disabled
1	0	1b	Disabled
1	1	0b	Disabled
1	1	1b	Enabled

7.3.20.3 Operating Mode

This mode is enabled when -

- nSLEEP is high
- ENABLE pin is Hi-Z or logic high
- EN_OUT = 1b for SPI interface
- VM > UVLO

The t_{WAKE} time must elapse before the device is ready for inputs.

7.3.20.4 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20 µs and smaller than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in Figure 7-48. This reset pulse does not affect the status of the charge pump or other functional blocks.

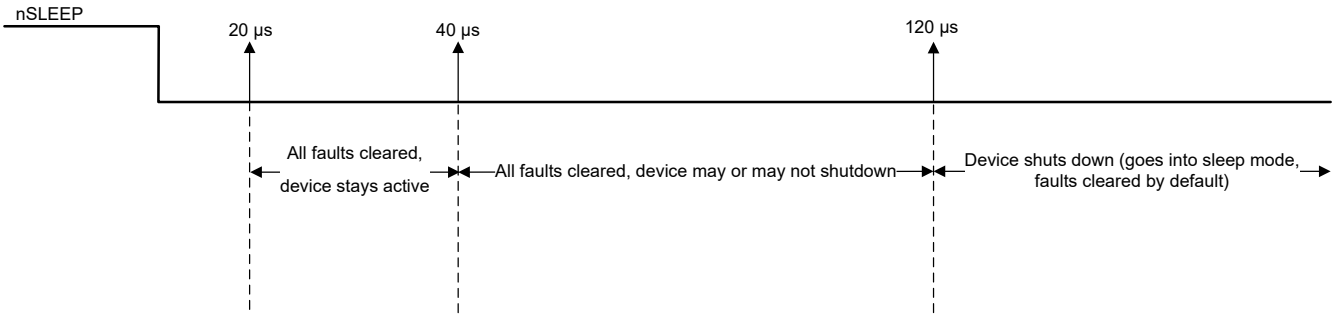

Figure 7-48. nSLEEP Reset Pulse

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7.3.20.5 Functional Modes Summary

Table 7-31. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 55 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 55 V	nSLEEP pin = 1 ENABLE = 1 and EN_OUT = 1b	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 55 V	nSLEEP pin = 1 ENABLE pin = 0 or EN_OUT = 0b	Disabled	Operating	Operating	Operating	Operating

7.4 Programming

7.4.1 Serial Peripheral Interface (SPI) Communication

When configured to operate with SPI interface, the device has full duplex, 4-wire synchronous communication that is used to set device configurations, operating parameters, and read out diagnostic information from the device. This section describes the SPI protocol, the command structure, and the control and status registers. The SPI operates in target mode and can be connected with a controller in the following configurations:

- One target device
- Multiple target devices in parallel connection
- Multiple target devices in series (daisy chain) connection

7.4.1.1 SPI Format

The serial data input (SDI) word consists of a 16-bit word, with an 8 bit-command (A1), followed by 8-bit data (D1). The serial data output (SDO) word consists of 8 bits of status register with fault status indication (S1), followed by a report byte (R1). Figure 7-49 shows the data sequence between the controller and the SPI target driver.

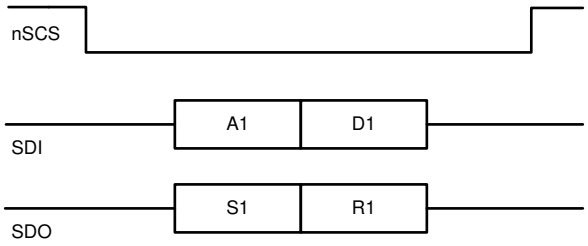

Figure 7-49. SPI Format - Standard "16-bit" Frame

A valid frame must meet the following conditions:

- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
- A full 16 SCLK cycles must occur for a valid transaction for a standard frame, or alternately, for a daisy chainframe with "n" number of peripheral devices, 16 + (n x 16) SCLK cycles must occur for a valid transaction. Else, a frame error (SPI_ERROR) is reported and the data is ignored if it is a WRITE operation.
- Data on SDO from the device is propagated on the rising edge of SCLK, while data on SDI is captured by thedevice on the subsequent falling edge of SCLK.
- The most-significant bit (MSB) is shifted in and out first.

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- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

The SDI input data word is 16 bits long and consists of the following format, as shown in Table 7-32:

- Command byte (first 8 bits)
  - MSB bit indicates frame type (bit B15 = 0 for standard frame).
  - Next to MSB bit, W0, indicates read or write operation (bit B14, write = 0, read = 1)
  - Followed by 6 address bits, A[5:0] (bits B13 through B8)
- Data byte (last 8 bits)
  - Last 8 bits indicate data, D[7:0] (bits B7 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

Table 7-32. SDI - Standard Frame Format

	R/W	ADDRESS						DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The SDO output data word is 16 bits long and consists of the following format, as shown in Table 7-33:

- Status byte (first 8 bits)
  - 2 MSB bits are forced high (B15, B14 = 1).
  - Following 6 bits are from the FAULT register (bits B13 through B8)
- Report byte (last 8 bits)
  - The last 8 bits (B7:B0) are either the data currently in the register being read for a read operation (W0 =1), or, existing data in the register being written to for a write command (W0 = 0).

Table 7-33. SDO Output Data Word Format

STATUS								REPORT							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	UVLO	CPUV	OCP	STL	TF	OL	D7	D6	D5	D4	D3	D2	D1	D0

7.4.1.2 SPI for Multiple Target Devices in Daisy Chain Configuration

Multiple devices can be connected to the controller with and without the daisy chain. For connecting a 'n' number of devices to a controller without using a daisy chain, 'n' number of GPIO resources from controller have to be utilized for nSCS pins. Whereas, if the daisy chain configuration is used, a single nSCS line can be used for connecting multiple devices.

Figure 7-50 shows the topology when three devices are connected in daisy chain. This configuration saves GPIO ports when multiple devices are communicating to the same controller.

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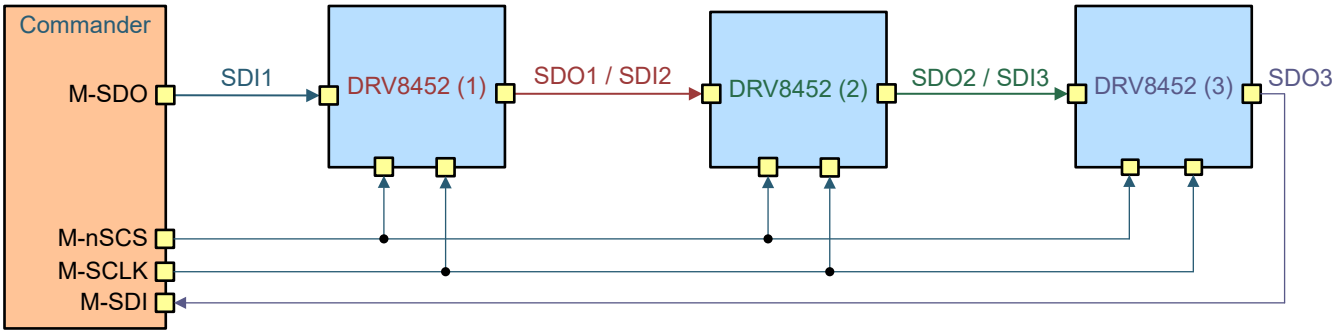

Figure 7-50. Three Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU as shown in Figure 7-51 for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

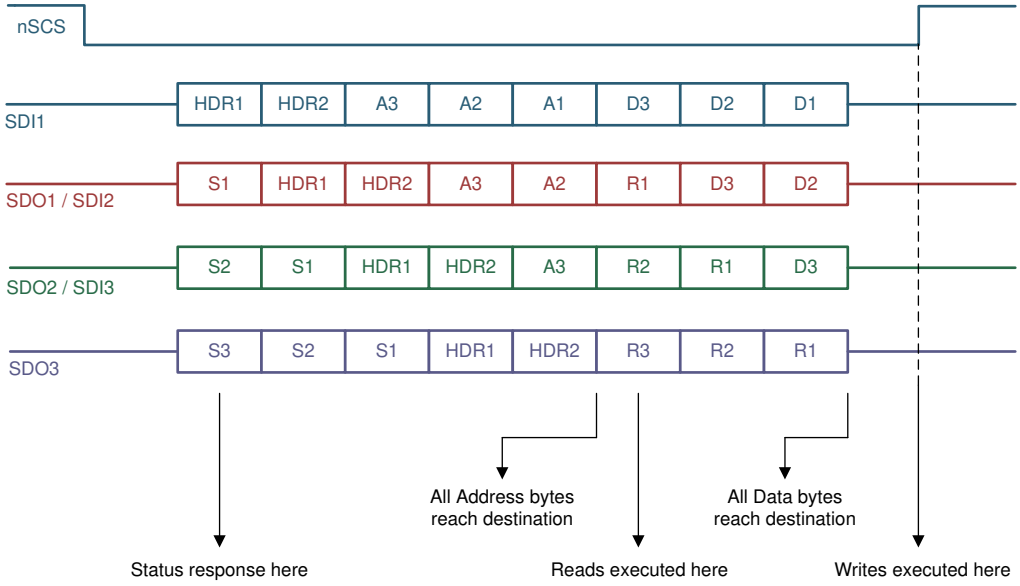

Figure 7-51. SPI Frame With Three Devices

After the data has been transmitted through the chain, the MCU receives the data string in the format shown in Figure 7-52 for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

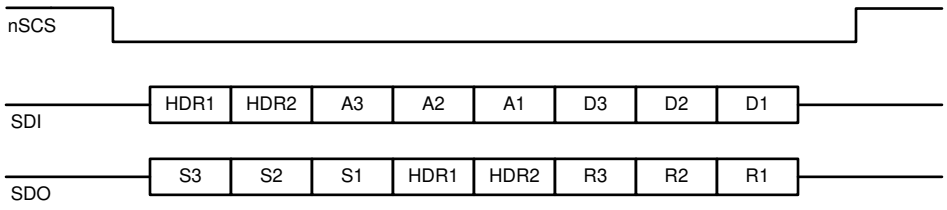

Figure 7-52. SPI Data Sequence for Three Devices

The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

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The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

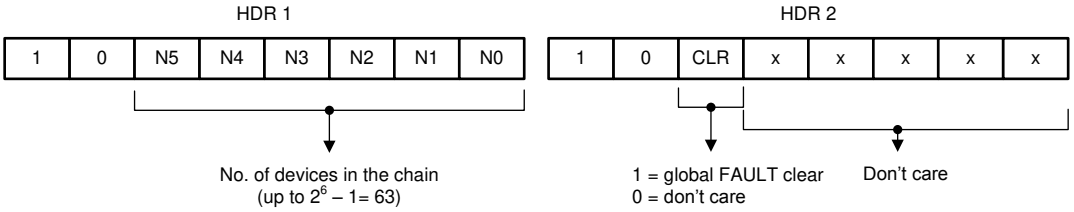

Figure 7-53. Header Bytes

The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

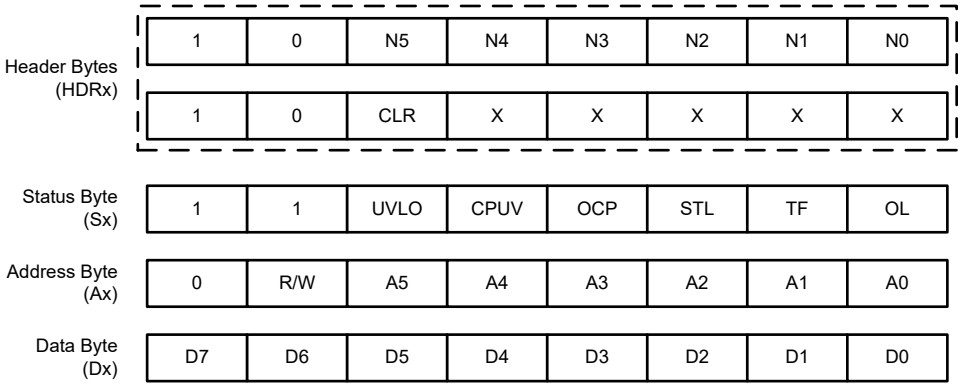

Figure 7-54. Contents of Header, Status, Address, and Data Bytes

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in Figure 7-51, are the content of the register being accessed.

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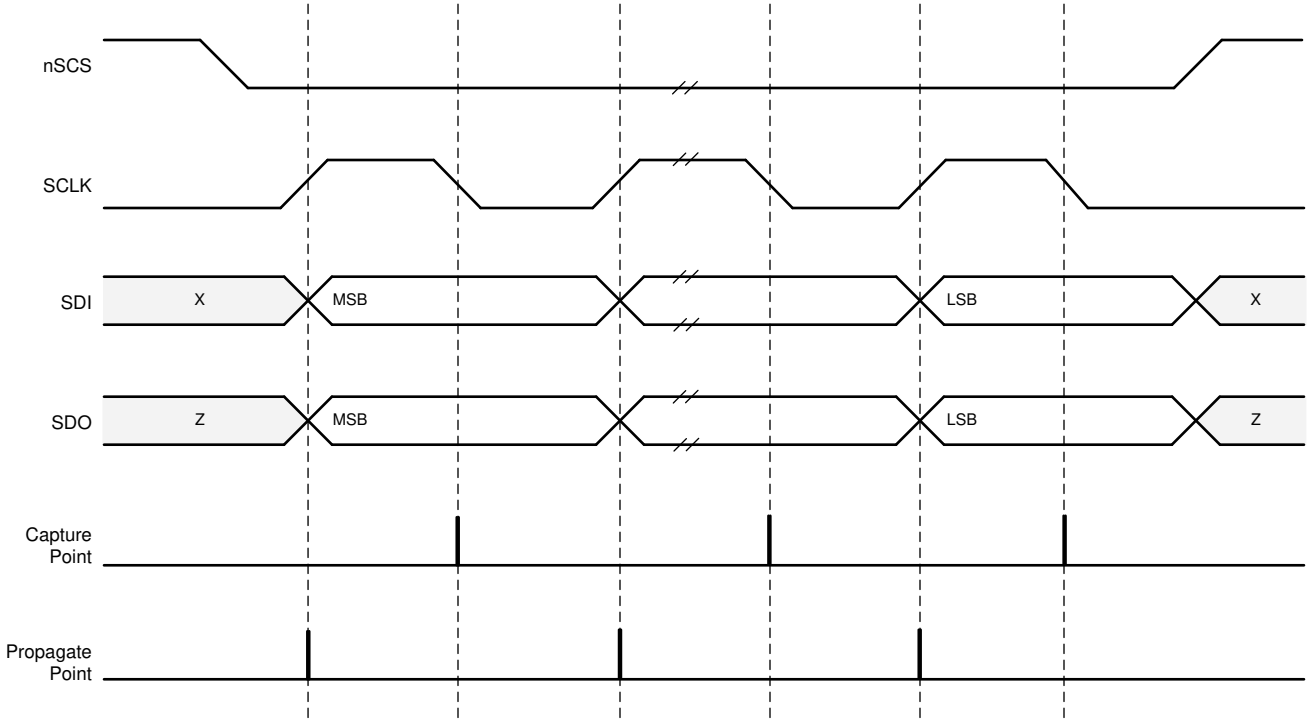

Figure 7-55. SPI Transaction

7.4.1.3 SPI for Multiple Target Devices in Parallel Configuration

Figure 7-56 shows three DRV8452 devices connected in parallel configuration.

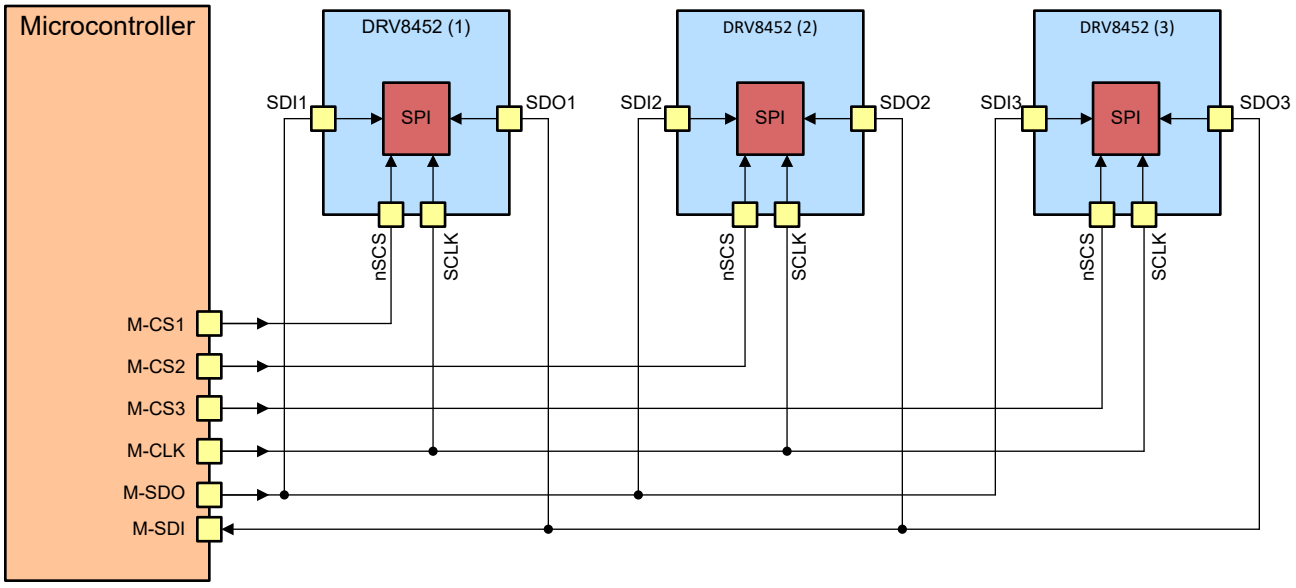

Figure 7-56. Three Devices Connected in Parallel Configuration

7.5 Register Maps

Table 7-34 lists the memory-mapped registers for the device. All register addresses not listed in Table 7-34 should be considered as reserved locations and the register contents must not be modified.

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Table 7-34. Memory Map

Register	7	6	5	4	3	2	1	0	Type	Address
FAULT	FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL	R	0x00
DIAG1	OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A	R	0x01
DIAG2	STSL	OTW	OTS	STL_LRN_OK	STALL	LRN_DONE	OL_B	OL_A	R	0x02
DIAG3	RSVD	NHOME	CNT_OFLW	CNT_UFLW	RSVD	NPOR	RSVD		R	0x03
CTRL1	EN_OUT	SR	IDX_RST	TOFF [1:0]		DECAY [2:0]			RW	0x04
CTRL2	DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]				RW	0x05
CTRL3	CLR_FLT	LOCK [2:0]			TOCP	OCP_MODE	OTSD_MODE	OTW_REP	RW	0x06
CTRL4	TBLANK_TIME[1:0]		STL_LRN	EN_STL	STL_REP	STL_FRQ	STEP_FRQ_TOL[1:0]		RW	0x07
CTRL5	STALL_TH [7:0]								RW	0x08
CTRL6	RC_RIPPLE[1:0]		DIS_SSC	TRQ_SCALE	STALL_TH[11:8]				RW	0x09
CTRL7	TRQ_COUNT [7:0]								R	0x0A
CTRL8	RSVD				TRQ_COUNT[11:8]				R	0x0B
CTRL9	EN_OL	OL_MODE	OL_T[1:0]		STEP_EDGE	RES_AUTO[1:0]		EN_AUTO	RW	0x0C
CTRL10	ISTSL[7:0]								RW	0x0D
CTRL11	TRQ_DAC[7:0]								RW	0x0E
CTRL12	EN_STSL	TSTSL_FALL[3:0]				RSVD			RW	0x0F
CTRL13	TSTSL_DLY[5:0]						VREF_INT_EN	RSVD	RW	0x10
INDEX1	CUR_A_POS[7:0]								R	0x11
INDEX2	CUR_A_SIGN	RSVD							R	0x12
INDEX3	CUR_B_POS[7:0]								R	0x13
INDEX4	CUR_B_SIGN	RSVD					CUR_A[1:0]		R	0x14
INDEX5	CUR_A[9:2]								R	0x15
CUSTOM_CTRL1	RSVD							EN_CUSTOM	RW	0x16
CUSTOM_CTRL2	CUSTOM_CURRENT1[7:0]								RW	0x17
CUSTOM_CTRL3	CUSTOM_CURRENT2[7:0]								RW	0x18
CUSTOM_CTRL4	CUSTOM_CURRENT3[7:0]								RW	0x19
CUSTOM_CTRL5	CUSTOM_CURRENT4[7:0]								RW	0x1A
CUSTOM_CTRL6	CUSTOM_CURRENT5[7:0]								RW	0x1B
CUSTOM_CTRL7	CUSTOM_CURRENT6[7:0]								RW	0x1C
CUSTOM_CTRL8	CUSTOM_CURRENT7[7:0]								RW	0x1D
CUSTOM_CTRL9	CUSTOM_CURRENT8[7:0]								RW	0x1E
ATQ_CTRL1	ATQ_CNT[7:0]								R	0x1F
ATQ_CTRL2	ATQ_CNT[10:8]			RSVD		ATQ_LRN_CONST1[10:8]			RW	0x20
ATQ_CTRL3	ATQ_LRN_CONST1[7:0]								RW	0x21
ATQ_CTRL4	ATQ_LRN_MIN_CURRENT[4:0]					ATQ_LRN_CONST2[10:8]			RW	0x22
ATQ_CTRL5	ATQ_LRN_CONST2[7:0]								RW	0x23
ATQ_CTRL6	ATQ_UL[7:0]								RW	0x24
ATQ_CTRL7	ATQ_LL[7:0]								RW	0x25
ATQ_CTRL8	KP[7:0]								RW	0x26
ATQ_CTRL9	RSVD				KD[3:0]				RW	0x27
ATQ_CTRL10	ATQ_EN	LRN_START	ATQ_FRZ[2:0]			ATQ_AVG[2:0]			RW	0x28

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Table 7-34. Memory Map (continued)

Register	7	6	5	4	3	2	1	0	Type	Address
ATQ_CTRL11	ATQ_TRQ_MIN[7:0]								RW	0x29
ATQ_CTRL12	ATQ_TRQ_MAX[7:0]								RW	0x2A
ATQ_CTRL13	ATQ_D_THR[7:0]								RW	0x2B
ATQ_CTRL14	RSVD								RW	0x2C
ATQ_CTRL15	ATQ_ERROR_TRUNCATE[3:0]				ATQ_LRN_STEP[1:0]		ATQ_LRN_CYCLE_SELECT[1:0]		RW	0x2D
ATQ_CTRL16	ATQ_TRQ_DAC[7:0]								R	0x2E
ATQ_CTRL17	RSVD	VM_SCALE	RSVD						RW	0x2F
ATQ_CTRL18	RSVD								RW	0x30
SS_CTRL1	SS_SMPL_SEL[1:0]		RSVD		SS_PWM_FREQ[1:0]		RSVD	EN_SS	RW	0x31
SS_CTRL2	SS_KP[7:0]								RW	0x32
SS_CTRL3	SS_KI[7:0]								RW	0x33
SS_CTRL4	RSVD	SS_KI_DIV_SEL[2:0]			RSVD	SS_KP_DIV_SEL[2:0]			RW	0x34
SS_CTRL5	SS_THR[7:0]								RW	0x35
CTRL 14	VM_ADC[4:0]					RSVD			RW	0x3C

Complex bit access types are encoded to fit into small table cells. Table 7-35 shows the codes that are used for access types in this section.

Table 7-35. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1 Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers.

Table 7-36 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 7-36 should be considered as reserved locations and the register contents should not be modified.

Table 7-36. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT	Go
0x01	DIAG1	Go
0x02	DIAG2	Go
0x03	DIAG3	Go

7.5.1.1 FAULT (address = 0x00) [Default = 00h]

FAULT status is shown in Figure 7-57 and described in Table 7-37.

Read-only

Return to the Register Maps Table

Figure 7-57. FAULT Register

7	6	5	4	3	2	1	0
FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-37. FAULT Register Field Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	FAULT bit is 1b when device has any fault condition. During normal operation, FAULT bit is 0b. nFAULT pin is pulled down when FAULT bit is 1b. nFAULT pin is released during normal operation.
6	SPI_ERROR	R	0b	Indicates SPI protocol errors, such as more SCLK pulses than are required or SCLK is absent even though nSCS is low. SPI_ERROR becomes 1b in fault and the nFAULT pin is driven low. Normal operation resumes when the protocol error is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.
5	UVLO	R	0b	When this bit is 1b, it indicates an supply undervoltage lockout fault condition.
4	CPUV	R	0b	When this bit is 1b, it indicates charge pump undervoltage fault condition.
3	OCP	R	0b	When this bit is 1b, it indicates overcurrent fault condition
2	STL	R	0b	When this bit is 1b, it indicates motor stall condition.
1	TF	R	0b	Logic OR of the overtemperature warning (OTW) and overtemperature shutdown (OTSD). When this bit is 1b, it indicates overtemperature fault.
0	OL	R	0b	When this bit is 1b, it indicates open-load fault condition.

7.5.1.2 DIAG1 (address = 0x01) [Default = 00h]

DIAG1 is shown in Figure 7-58 and described in Table 7-38.

Read-only

Return to the Register Maps Table

Figure 7-58. DIAG1 Register

7	6	5	4	3	2	1	0
OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-38. DIAG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OCP_LS2_B	R	0b	When this bit is 1b, it indicates overcurrent fault on the low-side FET of half bridge connected to BOUT2
6	OCP_HS2_B	R	0b	When this bit is 1b, it indicates overcurrent fault on the high-side FET of half bridge connected to BOUT2
5	OCP_LS1_B	R	0b	When this bit is 1b, it indicates overcurrent fault on the low-side FET of half bridge connected to BOUT1
4	OCP_HS1_B	R	0b	When this bit is 1b, it indicates overcurrent fault on the high-side FET of half bridge connected to BOUT1
3	OCP_LS2_A	R	0b	When this bit is 1b, it indicates overcurrent fault on the low-side FET of half bridge connected to AOUT2

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Table 7-38. DIAG1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	OCP_HS2_A	R	0b	When this bit is 1b, it indicates overcurrent fault on the high-side FET of half bridge connected to AOUT2
1	OCP_LS1_A	R	0b	When this bit is 1b, it indicates overcurrent fault on the low-side FET of half bridge connected to AOUT1
0	OCP_HS1_A	R	0b	When this bit is 1b, it indicates overcurrent fault on the high-side FET of half bridge connected to AOUT1

7.5.1.3 DIAG2 (address = 0x02) [Default = 00h]

DIAG2 is shown in Figure 7-59 and described in Table 7-39.

Read-only

Return to the Register Maps Table

Figure 7-59. DIAG2 Register

7	6	5	4	3	2	1	0
STSL	OTW	OTS	STL_LRN_OK	STALL	LRN_DONE	OL_B	OL_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-39. DIAG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	STSL	R	0b	When this bit is 1b, it indicates that the device is operating with standstill power saving mode.
6	OTW	R	0b	When this bit is 1b, it indicates overtemperature warning.
5	OTS	R	0b	When this bit is 1b, it indicates overtemperature shutdown.
4	STL_LRN_OK	R	0b	When this bit is 1b, it indicates stall detection learning is successful.
3	STALL	R	0b	When this bit is 1b, it indicates motor is stalled.
2	LRN_DONE	R	0b	When this bit is 1b, it indicates auto torque learning is successful.
1	OL_B	R	0b	When this bit is 1b, it indicates open-load detection in BOUT coil.
0	OL_A	R	0b	When this bit is 1b, it indicates open-load detection in AOUT coil.

7.5.1.4 DIAG3 (address = 0x03) [Default = 00h]

DIAG3 is shown in Figure 7-60 and described in Table 7-40.

Read-only

Return to the Register Maps Table

Figure 7-60. DIAG3 Register

7	6	5	4	3	2	1	0
RSVD	NHOME	CNT_OFLW	CNT_UFLW	RSVD	NPOR	RSVD	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b	

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Table 7-40. DIAG3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Reserved
6	NHOME	R	0b	When this bit is 1b, it indicates indexer is at a position other than the home position.
5	CNT_OFLW	R	0b	When this bit is 1b, it indicates ATQ_CNT is more than ATQ_UL
4	CNT_UFLW	R	0b	When this bit is 1b, it indicates ATQ_CNT is less than ATQ_LL
3	RSVD	R	0b	Reserved
2	NPOR	R	0b	• 0b = Indicates a prior VCC UVLO event • 1b = Indicates that the NPOR bit has been cleared by a CLR_FLT or nSLEEP reset pulse input after a VCC UVLO event
1-0	RSVD	R	00b	Reserved

7.5.2 Control Registers

The IC control registers are used to configure the device. Control registers are read and write capable.

Table 7-41 lists the memory-mapped registers for the control registers. All register offset addresses not listed in Table 7-41 should be considered as reserved locations and the register contents should not be modified.

Table 7-41. Control Registers Summary Table

Address	Register Name	Section
0x04	CTRL1	Go
0x05	CTRL2	Go
0x06	CTRL3	Go
0x07	CTRL4	Go
0x08	CTRL5	Go
0x09	CTRL6	Go
0x0A	CTRL7	Go
0x0B	CTRL8	Go
0x0C	CTRL9	Go
0x0D	CTRL10	Go
0x0E	CTRL11	Go
0x0F	CTRL12	Go
0x1A	CTRL13	Go
0x3C	CTRL14	Go

7.5.2.1 CTRL1 (address = 0x04) [Default = 0Fh]

CTRL1 is shown in Figure 7-61 and described in Table 7-42.

Read/Write

Return to the Register Maps Table

Figure 7-61. CTRL1 Control Register

7	6	5	4	3	2	1	0
EN_OUT	SR	IDX_RST	TOFF [1:0]		DECAY [2:0]		
R/W-0b	R/W-0b	R/W-0b	R/W-01b		R/W-111b		

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Table 7-42. CTRL1 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_OUT	R/W	0b	0b = All outputs are disabled 1b = All outputs are enabled
6	SR	R/W	0b	0b = Output rise/fall time 140 ns 1b = Output rise/fall time 70 ns
5	IDX_RST	R/W	0b	When this bit is 1b, it resets the indexer to 45° electrical angle, but the contents of the memory map registers will not change.
4-3	TOFF [1:0]	R/W	01b	• 00b = 9.5 µs • 01b = 19 µs • 10b = 27 µs • 11b = 35 µs
2-0	DECAY [2:0]	R/W	111b	• 000b = Slow decay • 100b = Mixed 30% decay • 101b = Mixed 60% decay • 110b = Smart tune Dynamic Decay • 111b = Smart tune Ripple Control • 001b, 010b, 011b = Reserved

7.5.2.2 CTRL2 (address = 0x05) [Default = 06h]

CTRL2 is shown in Figure 7-62 and described in Table 7-43.

Read/Write

Return to the Register Maps Table

Figure 7-62. CTRL2 Control Register

7	6	5	4	3	2	1	0
DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0110b			

Table 7-43. CTRL2 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	DIR	R/W	0b	Direction input. When SPI_DIR = 1b, if DIR = 1b, motor moves in the forward direction; and when DIR = 0b, motor moves in the reverse direction.
6	STEP	R/W	0b	Step input. Logic 1b causes the indexer to advance one step, when SPI_STEP = 1b. This bit is self-clearing, automatically becomes 0b after writing 1b.
5	SPI_DIR	R/W	0b	0b = Outputs follow input DIR pin for direction of stepping 1b = Outputs follow DIR bit in SPI register for direction of stepping
4	SPI_STEP	R/W	0b	0b = Outputs follow input STEP pin for stepping 1b = Outputs follow STEP bit in SPI register for stepping

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Table 7-43. CTRL2 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3-0	MICROSTEP_MODE [3:0]	R/W	0110b	• 0000b = Full step (2-phase excitation) with 100% current • 0001b = Full step (2-phase excitation) with 71% current • 0010b = Non-circular 1/2 step • 0011b = 1/2 step • 0100b = 1/4 step • 0101b = 1/8 step • 0110b = 1/16 step • 0111b = 1/32 step • 1000b = 1/64 step • 1001b = 1/128 step • 1010b = 1/256 step • 1011b to 1111b = Reserved

7.5.2.3 CTRL3 (address = 0x06) [Default = 38h]

CTRL3 is shown in Figure 7-63 and described in Table 7-44.

Read/Write

Return to the Register Maps Table

Figure 7-63. CTRL3 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	LOCK [2:0]			TOCP	OCP_MODE	OTSD_MODE	OTW_REP
R/W-0b	R/W-011b			R/W-1b	R/W-0b	R/W-0b	R/W-0b

Table 7-44. CTRL3 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write 1b to this bit to clear all latched fault bits. This bit automatically resets to 0b after 1b is written.
6-4	LOCK [2:0]	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x06h bit 7 (CLR_FLT). Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
3	TOCP	R/W	1b	1b = Overcurrent protection deglitch time is 2.2 µs 0b = Overcurrent protection deglitch time is 1.2 µs
2	OCP_MODE	R/W	0b	0b = Overcurrent condition causes a latched fault 1b = Overcurrent condition fault recovery is auto-retry
1	OTSD_MODE	R/W	0b	0b = Overtemperature condition causes a latched fault 1b = Overtemperature condition fault recovery is auto-retry
0	TW_REP	R/W	0b	0b = Overtemperature or undertemperature warning is not reported on nFAULT 1b = Overtemperature or undertemperature warning is reported on nFAULT

7.5.2.4 CTRL4 (address = 0x07) [Default = 49h]

CTRL4 control is shown in Figure 7-64 and described in Table 7-45.

Read/Write

Return to the Register Maps Table

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Figure 7-64. CTRL4 Control Register

7	6	5	4	3	2	1	0
TBLANK_TIME[1:0]		STL_LRN	EN_STL	STL_REP	FRQ_CHG	STEP_FREQ_TOL[1:0]	
R/W-01b		R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-01b	

Table 7-45. CTRL4 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	TBLANK_TIME[1:0]	R/W	01b	Controls the current sense blanking time. • 00b = 1 µs blanking time • 01b = 1.5 µs blanking time • 10b = 2 µs blanking time • 11b = 2.5 µs blanking time
5	STL_LRN	R/W	0b	Write 1b to enable automatic learning of stall detection threshold. This bit automatically returns to 0b when the stall learning process is complete.
4	EN_STL	R/W	0b	0b = Stall detection is disabled 1b = Stall detection is enabled
3	STL_REP	R/W	1b	0b = Stall detection is not reported on nFAULT 1b = Stall detection is reported on nFAULT
2	FRQ_CHG	R/W	0b	0b = STEP input is filtered as per the STEP_FRQ_TOL bits 1b = STEP input is not filtered
1-0	STEP_FRQ_TOL[1:0]	R/W	01b	Programs the filter setting for the STEP input. • 00b = 1% filtering • 01b = 2% filtering • 10b = 4% filtering • 11b = 6% filtering

7.5.2.5 CTRL5 (address = 0x08) [Default = 03h]

CTRL5 is shown in Figure 7-65 and described in Table 7-46.

Read/Write

Return to the Register Maps Table

Figure 7-65. CTRL5 Control Register

7	6	5	4	3	2	1	0
STALL_TH [7:0]							
R/W-00000011b							

Table 7-46. CTRL5 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	STALL_TH [7:0]	R/W	00000011b	Lower 8-bits of stall threshold. • 000000000000b = 0 count • ..... • 000000000011b = 3 counts (default) • ..... • 111111111111b = 4095 counts

7.5.2.6 CTRL6 (address = 0x09) [Default = 20h]

CTRL6 is shown in Figure 7-66 and described in Table 7-47.

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Read/Write

Return to the Register Maps Table

Figure 7-66. CTRL6 Control Register

7	6	5	4	3	2	1	0
RC_RIPPLE[1:0]		DIS_SSC	TRQ_SCALE	STALL_TH[11:8]			
R/W-00b		R/W-1b	R/W-0b	R/W-0000b			

Table 7-47. CTRL6 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RC_RIPPLE[1:0]	R/W	00b	Controls the current ripple in smart tune ripple control decay mode. • 00b = 1% ripple (default) • 01b = 2% ripple • 10b = 4% ripple • 11b = 6% ripple
5	DIS_SSC	R/W	1b	0b = spread-spectrum enabled 1b = spread-spectrum disabled
4	TRQ_SCALE	R/W	0b	0b = No torque count scaling is applied 1b = Torque count is scaled up by a factor of 8
3-0	STALL_TH[11:8]	R/W	0000b	4 MSB bits of stall threshold.

7.5.2.7 CTRL7 (address = 0x0A) [Default = FFh]

CTRL7 is shown in Figure 7-67 and described in Table 7-48.

Read-only

Return to the Register Maps Table

Figure 7-67. CTRL7 Control Register

7	6	5	4	3	2	1	0
TRQ_COUNT[7:0]							
R-11111111b							

Table 7-48. CTRL7 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_COUNT[7:0]	R	11111111b	8 LSB bits of TRQ_COUNT. 000000000000b = 0 count XXXXXXXXXXXXb = 1 to 4094 counts 111111111111b = 4095 counts

7.5.2.8 CTRL8 (address = 0x0B) [Default = 0Fh]

CTRL8 is shown in Figure 7-68 and described in Table 7-49.

Read-only

Return to the Register Maps Table

Figure 7-68. CTRL8 Control Register

7	6	5	4	3	2	1	0
RSVD				TRQ_COUNT[11:8]			
R-0000b				R-1111b			

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Table 7-49. CTRL8 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RSVD	R	0000b	Reserved.
3-0	TRQ_COUNT[11:8]	R	1111b	4 MSB bits of TRQ_COUNT.

7.5.2.9 CTRL9 (address = 0x0C) [Default = 10h]

CTRL9 is shown in Figure 7-69 and described in Table 7-50.

Read/Write

Return to the Register Maps Table

Figure 7-69. CTRL9 Control Register

7	6	5	4	3	2	1	0
EN_OL	OL_MODE	OL_T[1:0]		STEP_EDGE	RES_AUTO[1:0]		EN_AUTO
R/W-0b	R/W-0b	R/W-01b		R/W-0b	R/W-00b		R/W-0b

Table 7-50. CTRL9 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_OL	R/W	0b	Write 1b to enable open load detection. When this bit is 0b, open load detection is disabled.
6	OL_MODE	R/W	0b	0b = nFAULT is released after latched OL fault is cleared using CLR_FLT bit or nSLEEP reset pulse 1b = nFAULT is released immediately after OL fault condition is removed
5-4	OL_T[1:0]	R/W	01b	Controls the open load fault detection time. • 00b = 30 ms (max) • 01b = 60 ms (max) • 10b = 120 ms (max) • 11b = Reserved
3	STEP_EDGE	R/W	0b	0b = Active edge for STEP input is only rising edge 1b = Active edge for STEP input is both rising and falling edges
2-1	RES_AUTO[1:0]	R/W	00b	Controls the microstepping resolution in automatic microstepping mode. • 00b = 1/256 • 01b = 1/128 • 10b = 1/64 • 11b = 1/32
0	EN_AUTO	R/W	0b	0b = Automatic microstepping disabled 1b = Automatic microstepping enabled

7.5.2.10 CTRL10 (address = 0x0D) [Default = 80h]

CTRL10 control is shown in Figure 7-70 and described in Table 7-51.

Read/Write

Return to the Register Maps Table

Figure 7-70. CTRL10 Control Register

7	6	5	4	3	2	1	0
ISTSL[7:0]							

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Figure 7-70. CTRL10 Control Register (continued)

R/W-10000000b

Table 7-51. CTRL10 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ISTSL[7:0]	R/W	10000000b	Determines the holding current. 11111111b = 256/256 x 100% 11111110b = 255/256 x 100% 11111101b = 254/256 x 100% 11111100b = 253/256 x 100% ..... 00000000b = 1/256 x 100%

7.5.2.11 CTRL11 (address = 0x0E) [Default = FFh]

CTRL11 control is shown in Figure 7-71 and described in Table 7-52.

Read/Write

Return to the Register Maps Table

Figure 7-71. CTRL11 Control Register

7	6	5	4	3	2	1	0
TRQ_DAC[7:0]							
R/W-11111111b							

Table 7-52. CTRL11 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_DAC[7:0]	R/W	11111111b	Determines the run current. • 11111111b = 256/256 x 100% • 11111110b = 255/256 x 100% • 11111101b = 254/256 x 100% • 11111100b = 253/256 x 100% • ..... • 00000000b = 1/256 x 100%

7.5.2.12 CTRL12 (address = 0x0F) [Default = 20h]

CTRL12 is shown in Figure 7-72 and described in Table 7-53.

Read/Write

Return to the Register Maps Table

Figure 7-72. CTRL12 Control Register

7	6	5	4	3	2	1	0
EN_STSL	TSTSL_FALL[3:0]				RSVD		
R/W-0b	R/W-0100b				R/W-000b		

Table 7-53. CTRL12 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_STSL	R/W	0b	0b = Standstill power saving mode disabled 1b = Standstill power saving mode enabled

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Table 7-53. CTRL12 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6-3	TSTSL_FALL[3:0]	R/W	0100b	Controls the time it takes the current to reduce from TRQ_DAC to ISTSL after TSTSL_DLY time has elapsed • 0000b: fall time = 0 • 0001b: fall time for each current step = 1 ms • ..... • 0100b: fall time for each current step = 4 ms • ..... • 1111b: fall time for each current step = 15 ms
2-0	RSVD	R/W	000b	Reserved

7.5.2.13 CTRL13 (address = 0x10) [Default = 10h]

CTRL13 is shown in Figure 7-73 and described in Table 7-54.

Read/Write

Return to the Register Maps Table

Figure 7-73. CTRL13 Control Register

7	6	5	4	3	2	1	0
TSTSL_DLY[5:0]						VREF_INT_EN	RSVD
R/W-000100b						R/W-0b	R/W-0b

Table 7-54. CTRL13 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-2	TSTSL_DLY[5:0]	R/W	000100b	Controls the delay between last STEP pulse and activation of standstill power saving mode. • 000000b: Reserved • 000001b: Delay = 1 x 16 ms = 16 ms • ..... • 000100b: Delay = 4 x 16 ms = 64 ms • ..... • 111111b: Delay = 63 x 16 ms = 1.008 s
1	VREF_INT_EN	R/W	0b	When this bit is 1b, the device uses the internal 3.3 V reference for current regulation, and the voltage on the VREF pin is ignored.
0	RSVD	R/W	0b	Reserved

Note

Do not set TSTSL_DLY to 000000b.

7.5.3 Indexer Registers

The indexer registers provide current values for coil A, and the position in the microstep table for the currents in coil A and coil B. Indexer registers are read only.

Table 7-55 lists the memory-mapped registers for the indexer registers. All register offset addresses not listed in Table 7-55 should be considered as reserved locations and the register contents should not be modified.

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Table 7-55. Indexer Registers Summary Table

Address	Register Name	Section
0x11	INDEX1	Go
0x12	INDEX2	Go
0x13	INDEX3	Go
0x14	INDEX4	Go
0x15	INDEX5	Go

7.5.3.1 INDEX1 (address = 0x11) [Default = 80h]

INDEX1 is shown in Figure 7-74 and described in Table 7-56.

Read only

Return to the Register Maps Table

Figure 7-74. INDEX1 Register

7	6	5	4	3	2	1	0
CUR_A_POS[7:0]							
R-10000000b							

Table 7-56. INDEX1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUR_A_POS[7:0]	R	10000000b	Indicates the position of coil A current in the indexer table.

7.5.3.2 INDEX2 (address = 0x12) [Default = 80h]

INDEX2 is shown in Figure 7-75 and described in Table 7-57.

Read only

Return to the Register Maps Table

Figure 7-75. INDEX2 Register

7	6	5	4	3	2	1	0
CUR_A_SIGN	RSVD						
R-1b	R-0000000b						

Table 7-57. INDEX2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CUR_A_SIGN	R	1b	Outputs the sign of coil A current for the position indicated by the CUR_A_POS bits. 1b = Coil A current is positive 0b = Coil A current is negative
6-0	RSVD	R	0000000b	Reserved

7.5.3.3 INDEX3 (address = 0x13) [Default = 80h]

INDEX3 is shown in Figure 7-76 and described in Table 7-58.

Read only

Return to the Register Maps Table

Figure 7-76. INDEX3 Register

7	6	5	4	3	2	1	0

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Figure 7-76. INDEX3 Register (continued)

CUR_B_POS[7:0]
R-10000000b

Table 7-58. INDEX3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUR_B_POS[7:0]	R	10000000b	Indicates the position of coil B current in the indexer table.

7.5.3.4 INDEX4 (address = 0x14) [Default = 82h]

INDEX4 is shown in Figure 7-77 and described in Table 7-59.

Read only

Return to the Register Maps Table

Figure 7-77. INDEX4 Register

7	6	5	4	3	2	1	0
CUR_B_SIGN	RSVD					CUR_A[1:0]	
R-1b	R-00000b					R-10b	

Table 7-59. INDEX4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CUR_B_SIGN	R	1b	Outputs the sign of coil B current for the position indicated by the CUR_B_POS bits. 1b = Coil B current is positive 0b = Coil B current is negative
6-2	RSVD	R	00000b	Reserved
1-0	CUR_A[1:0]	R	10b	Lower two LSBs of the current in coil A

7.5.3.5 INDEX5 (address = 0x15) [Default = B5h]

INDEX5 is shown in Figure 7-78 and described in Table 7-60.

Read only

Return to the Register Maps Table

Figure 7-78. INDEX5 Register

7	6	5	4	3	2	1	0
CUR_A[9:2]							
R-10110101b							

Table 7-60. INDEX5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUR_A[9:2]	R	10110101b	Outputs the upper 8 bits of the current in coil A

7.5.4 Custom Microstepping Registers

The custom microstep registers store the current values corresponding to the first quadrant of coil A current. Custom microstep registers are read and write capable.

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Table 7-61 lists the memory-mapped registers for the custom microstep registers. All register offset addresses not listed in Table 7-61 should be considered as reserved locations and the register contents should not be modified.

Table 7-61. Custom microstep Registers Summary Table

Address	Register Name	Section
0x16	CUSTOM_CTRL1	Go
0x17	CUSTOM_CTRL2	Go
0x18	CUSTOM_CTRL3	Go
0x19	CUSTOM_CTRL4	Go
0x1A	CUSTOM_CTRL5	Go
0x1B	CUSTOM_CTRL6	Go
0x1C	CUSTOM_CTRL7	Go
0x1D	CUSTOM_CTRL8	Go
0x1E	CUSTOM_CTRL9	Go

7.5.4.1 CUSTOM_CTRL1 (address = 0x16) [Default = 00h]

CUSTOM_CTRL1 is shown in Figure 7-79 and described in Table 7-62.

Read/Write

Return to the Register Maps Table

Figure 7-79. CUSTOM_CTRL1 Register

7	6	5	4	3	2	1	0
RSVD							EN_CUSTOM
R/W-0000000b							R/W-0b

Table 7-62. CUSTOM_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	RSVD	R/W	0000000b	Reserved
0	EN_CUSTOM	R/W	0b	0b = Custom microstepping table is disabled 1b = Custom microstepping table is enabled

7.5.4.2 CUSTOM_CTRL2 (address = 0x17) [Default = 00h]

CUSTOM_CTRL2 is shown in Figure 7-80 and described in Table 7-63.

Read/Write

Return to the Register Maps Table

Figure 7-80. CUSTOM_CTRL2 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT1[7:0]							
R/W-00000000b							

Table 7-63. CUSTOM_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT1[7:0]	R/W	00000000b	Current value for position 1 in first quadrant

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7.5.4.3 CUSTOM_CTRL3 (address = 0x18) [Default = 00h]

CUSTOM_CTRL3 is shown in Figure 7-81 and described in Table 7-64.

Read/Write

Return to the Register Maps Table

Figure 7-81. CUSTOM_CTRL3 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT2[7:0]							
R/W-00000000b							

Table 7-64. CUSTOM_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT2[7:0]	R/W	00000000b	Current value for position 2 in first quadrant

7.5.4.4 CUSTOM_CTRL4 (address = 0x19) [Default = 00h]

CUSTOM_CTRL4 is shown in Figure 7-82 and described in Table 7-65.

Read/Write

Return to the Register Maps Table

Figure 7-82. CUSTOM_CTRL4 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT3[7:0]							
R/W-00000000b							

Table 7-65. CUSTOM_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT3[7:0]	R/W	00000000b	Current value for position 3 in first quadrant

7.5.4.5 CUSTOM_CTRL5 (address = 0x1A) [Default = 00h]

CUSTOM_CTRL5 is shown in Figure 7-83 and described in Table 7-66.

Read/Write

Return to the Register Maps Table

Figure 7-83. CUSTOM_CTRL5 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT4[7:0]							
R/W-00000000b							

Table 7-66. CUSTOM_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT4[7:0]	R/W	00000000b	Current value for position 4 in first quadrant

7.5.4.6 CUSTOM_CTRL6 (address = 0x1B) [Default = 00h]

CUSTOM_CTRL6 is shown in Figure 7-84 and described in Table 7-67.

Read/Write

Return to the Register Maps Table

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Figure 7-84. CUSTOM_CTRL6 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT5[7:0]							
R/W-00000000b							

Table 7-67. CUSTOM_CTRL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT5[7:0]	R/W	00000000b	Current value for position 5 in first quadrant

7.5.4.7 CUSTOM_CTRL7 (address = 0x1C) [Default = 00h]

CUSTOM_CTRL7 is shown in Figure 7-85 and described in Table 7-68.

Read/Write

Return to the Register Maps Table

Figure 7-85. CUSTOM_CTRL7 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT6[7:0]							
R/W-00000000b							

Table 7-68. CUSTOM_CTRL7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT6[7:0]	R/W	00000000b	Current value for position 6 in first quadrant

7.5.4.8 CUSTOM_CTRL8 (address = 0x1D) [Default = 00h]

CUSTOM_CTRL8 is shown in Figure 7-86 and described in Table 7-69.

Read/Write

Return to the Register Maps Table

Figure 7-86. CUSTOM_CTRL8 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT7[7:0]							
R/W-00000000b							

Table 7-69. CUSTOM_CTRL8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT7[7:0]	R/W	00000000b	Current value for position 7 in first quadrant

7.5.4.9 CUSTOM_CTRL9 (address = 0x1E) [Default = 00h]

CUSTOM_CTRL9 is shown in Figure 7-87 and described in Table 7-70.

Read/Write

Return to the Register Maps Table

Figure 7-87. CUSTOM_CTRL9 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT8[7:0]							
R/W-00000000b							

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Table 7-70. CUSTOM_CTRL9 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT8[7:0]	R/W	00000000b	Current value for position 8 in first quadrant

7.5.5 Auto torque Registers

The auto torque registers control the auto torque feature. Auto torque registers are read and write capable.

Table 7-71 lists the memory-mapped registers for the auto torque registers. All register offset addresses not listed in Table 7-71 should be considered as reserved locations and the register contents should not be modified.

Table 7-71. Auto torque Registers Summary Table

Address	Register Name	Section
0x1F	ATQ_CTRL1	Go
0x20	ATQ_CTRL2	Go
0x21	ATQ_CTRL3	Go
0x22	ATQ_CTRL4	Go
0x23	ATQ_CTRL5	Go
0x24	ATQ_CTRL6	Go
0x25	ATQ_CTRL7	Go
0x26	ATQ_CTRL8	Go
0x27	ATQ_CTRL9	Go
0x28	ATQ_CTRL10	Go
0x29	ATQ_CTRL11	Go
0x2A	ATQ_CTRL12	Go
0x2B	ATQ_CTRL13	Go
0x2C	ATQ_CTRL14	Go
0x2D	ATQ_CTRL15	Go
0x2E	ATQ_CTRL16	Go
0x2F	ATQ_CTRL17	Go
0x30	ATQ_CTRL18	Go

7.5.5.1 ATQ_CTRL1 (address = 0x1F) [Default = 00h]

ATQ_CTRL1 is shown in Figure 7-88 and described in Table 7-72.

Read ONLY

Return to the Register Maps Table

Figure 7-88. ATQ_CTRL1 Register

7	6	5	4	3	2	1	0
ATQ_CNT[7:0]							
R-00000000b							

Table 7-72. ATQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_CNT[7:0]	R	00000000b	Read-only. Indicates the 8 LSB bits of the ATQ_CNT output. ATQ_CNT is proportional to the mechanical load torque.

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7.5.5.2 ATQ_CTRL2 (address = 0x20) [Default = 00h]

ATQ_CTRL2 is shown in Figure 7-89 and described in Table 7-73.

Read/Write

Return to the Register Maps Table

Figure 7-89. ATQ_CTRL2 Register

7	6	5	4	3	2	1	0
ATQ_CNT[10:8]			RSVD		ATQ_LRN_CONST1[10:8]		
R/W-000b			R/W-00b		R/W-000b		

Table 7-73. ATQ_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	ATQ_CNT[10:8]	R/W	000b	Indicates the 3 MSB bits of the ATQ_CNT output
4-3	RSVD	R/W	00b	Reserved
2-0	ATQ_LRN_CONST1[10:8]	R/W	000b	Indicates the 3 MSB bits of the ATQ_LRN parameter at the initial learning current level.

7.5.5.3 ATQ_CTRL3 (address = 0x21) [Default = 00h]

ATQ_CTRL3 is shown in Figure 7-90 and described in Table 7-74.

Read/Write

Return to the Register Maps Table

Figure 7-90. ATQ_CTRL3 Register

7	6	5	4	3	2	1	0
ATQ_LRN_CONST1[7:0]							
R/W-00000000b							

Table 7-74. ATQ_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LRN_CONST1[7:0]	R/W	00000000b	8 LSB bits of the ATQ_LRN parameter at the initial learning current level.

7.5.5.4 ATQ_CTRL4 (address = 0x22) [Default = 20h]

ATQ_CTRL4 is shown in Figure 7-91 and described in Table 7-75.

Read/Write

Return to the Register Maps Table

Figure 7-91. ATQ_CTRL4 Register

7	6	5	4	3	2	1	0
ATQ_LRN_MIN_CURRENT[4:0]					ATQ_LRN_CONST2[10:8]		
R/W-00100b					R/W-000b		

Table 7-75. ATQ_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-3	ATQ_LRN_MIN_CURRENT[4:0]	R/W	00100b	Represents the initial current level for auto torque learning. Initial learning current = ATQ_LRN_MIN_CURRENT * 8

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Table 7-75. ATQ_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2-0	ATQ_LRN_CONST2[10:8]	R/W	000b	3 MSB bits of the ATQ_LRN parameter at the final learning current level.

7.5.5.5 ATQ_CTRL5 (address = 0x23) [Default = 00h]

ATQ_CTRL5 is shown in Figure 7-92 and described in Table 7-76.

Read/Write

Return to the Register Maps Table

Figure 7-92. ATQ_CTRL5 Register

7	6	5	4	3	2	1	0
ATQ_LRN_CONST2[7:0]							
R/W-00000000b							

Table 7-76. ATQ_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LRN_CONST2[7:0]	R/W	00000000b	8 LSB bits of the ATQ_LRN parameter at the final learning current level.

7.5.5.6 ATQ_CTRL6 (address = 0x24) [Default = 00h]

ATQ_CTRL6 is shown in Figure 7-93 and described in Table 7-77.

Read/Write

Return to the Register Maps Table

Figure 7-93. ATQ_CTRL6 Register

7	6	5	4	3	2	1	0
ATQ_UL[7:0]							
R/W-00000000b							

Table 7-77. ATQ_CTRL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_UL[7:0]	R/W	00000000b	Programs the upper limit of the auto torque hysterestic band.

7.5.5.7 ATQ_CTRL7 (address = 0x25) [Default = 00h]

ATQ_CTRL7 is shown in Figure 7-94 and described in Table 7-78.

Read/Write

Return to the Register Maps Table

Figure 7-94. ATQ_CTRL7 Register

7	6	5	4	3	2	1	0
ATQ_LL[7:0]							
R/W-00000000b							

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Table 7-78. ATQ_CTRL7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LL[7:0]	R/W	00000000b	Programs the lower limit of the auto torque hysterestic band.

7.5.5.8 ATQ_CTRL8 (address = 0x26) [Default = 00h]

ATQ_CTRL8 is shown in Figure 7-95 and described in Table 7-79.

Read/Write

Return to the Register Maps Table

Figure 7-95. ATQ_CTRL8 Register

7	6	5	4	3	2	1	0
KP[7:0]							
R/W-00000000b							

Table 7-79. ATQ_CTRL8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	KP[7:0]	R/W	00000000b	Proportional constant for tuning the auto torque PD control loop.

7.5.5.9 ATQ_CTRL9 (address = 0x27) [Default = 00h]

ATQ_CTRL9 is shown in Figure 7-96 and described in Table 7-80.

Read/Write

Return to the Register Maps Table

Figure 7-96. ATQ_CTRL9 Register

7	6	5	4	3	2	1	0
RSVD				KD[3:0]			
R/W-0000b				R/W-0000b			

Table 7-80. ATQ_CTRL9 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RSVD	R/W	0000b	Reserved.
3-0	KD[3:0]	R/W	0000b	Differential constant for tuning the auto torque PD control loop.

7.5.5.10 ATQ_CTRL10 (address = 0x28) [Default = 08h]

ATQ_CTRL10 is shown in Figure 7-97 and described in Table 7-81.

Read/Write

Return to the Register Maps Table

Figure 7-97. ATQ_CTRL10 Register

7	6	5	4	3	2	1	0
ATQ_EN	LRN_START	ATQ_FRZ[2:0]			ATQ_AVG[2:0]		
R/W-0b	R/W-0b	R/W-001b			R/W-000b		

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Table 7-81. ATQ_CTRL10 Register Field Descriptions

Bit	Field	Type	Default	Description
7	ATQ_EN	R/W	0b	0 = auto torque is disabled 1 = auto torque is enabled
6	LRN_START	R/W	0b	Writing 1b to this bit enables the auto torque learning process. After learning is completed, the bit automatically goes to 0b.
5-3	ATQ_FRZ[2:0]	R/W	001b	Delay in electrical half-cycles after which current is changed in response to the PD loop. A small value increases the current quickly to meet peak load demand. This parameter has a range of 1 to 7. 001b - Fastest response time, but the loop can become unstable 111b - Slowest response, but the loop will be stable
2-0	ATQ_AVG[2:0]	R/W	000b	The ATQ_CNT parameter is a moving average of ATQ_AVG number of half-cycles. Therefore, a high value for ATQ_AVG slows down the loop response time to a sudden peak load demand, but ensures smooth jerk-free transition to higher torque output. A low value causes the loop to respond immediately to a sudden load demand. • 010b - 2 cycle average • 100b - 4 cycle average • 111b - 8 cycle average • Other values : no averaging

7.5.5.11 ATQ_CTRL11 (address = 0x29) [Default = 0Ah]

ATQ_CTRL11 is shown in Figure 7-98 and described in Table 7-82.

Read/Write

Return to the Register Maps Table

Figure 7-98. ATQ_CTRL11 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_MIN[7:0]							
R/W-00001010b							

Table 7-82. ATQ_CTRL11 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_MIN[7:0]	R/W	00001010b	Minimum coil current when auto-torque is enabled.

7.5.5.12 ATQ_CTRL12 (address = 0x2A) [Default = FFh]

ATQ_CTRL12 is shown in Figure 7-99 and described in Table 7-83.

Read/Write

Return to the Register Maps Table

Figure 7-99. ATQ_CTRL12 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_MAX[7:0]							
R/W-11111111b							

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Table 7-83. ATQ_CTRL12 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_MAX[7:0]	R/W	11111111b	Maximum coil current when auto-torque is enabled.

7.5.5.13 ATQ_CTRL13 (address = 0x2B) [Default = 05h]

ATQ_CTRL13 is shown in Figure 7-100 and described in Table 7-84.

Read/Write

Return to the Register Maps Table

Figure 7-100. ATQ_CTRL13 Register

7	6	5	4	3	2	1	0
ATQ_D_THR[7:0]							
R/W-00000101b							

Table 7-84. ATQ_CTRL13 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_D_THR	R/W	00000101b	If error change is less then ATQ_D_THR, then KD does not contribute to correction. KD contributes only when error change is greater than ATQ_D_THR. For example: if ATQ_D_THR = 10, If error change is 9, u(t) = KP * e(t) If error change is 12, then u(t) = KP * e(t) + KD * de(t)/dt

7.5.5.14 ATQ_CTRL14 (address = 0x2C) [Default = 0Fh]

ATQ_CTRL14 is shown in Figure 7-101 and described in Table 7-85.

Read/Write

Return to the Register Maps Table

Figure 7-101. ATQ_CTRL14 Register

7	6	5	4	3	2	1	0
RSVD							
R/W-00001111b							

Table 7-85. ATQ_CTRL14 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	RSVD	R/W	00001111b	Reserved

7.5.5.15 ATQ_CTRL15 (address = 0x2D) [Default = 00h]

ATQ_CTRL15 is shown in Figure 7-102 and described in Table 7-86.

Read/Write

Return to the Register Maps Table

Figure 7-102. ATQ_CTRL15 Register

7	6	5	4	3	2	1	0
ATQ_ERROR_TRUNCATE[3:0]				ATQ_LRN_STEP[1:0]		ATQ_LRN_CYCLE_SELECT[1:0]	
R/W-0000b				R/W-00b		R/W-00b	

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Table 7-86. ATQ_CTRL15 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	ATQ_ERROR_TRUNCATE[3:0]	R/W	0000b	Number of LSB bits truncated from error before used in PD loop equations. This option helps removing noise in current.
3-2	ATQ_LRN_STEP[1:0]	R/W	00b	Represents the increment to initial current level. It supports four options - • 00b : ATQ_LRN_STEP = 128 • 01b : ATQ_LRN_STEP = 16 • 10b : ATQ_LRN_STEP = 32 • 11b : ATQ_LRN_STEP = 64 Example : If ATQ_LRN_STEP = 10b and ATQ_LRN_MIN_CURRENT = 11000b, then - • Initial learn current level = 24*8 = 192 • Final learn current level = 192 + 32 = 224
1-0	ATQ_LRN_CYCLE_SELECT[1:0]	R/W	00b	Represents the number of electrical half cycles spent in one current level after which the learning routine allows the current to jump to the other level. It supports four options - • 00b : 8 half-cycles • 01b : 16 half-cycles • 10b : 24 half-cycles • 11b : 32 half-cycles

7.5.5.16 ATQ_CTRL16 (address = 0x2E) [Default = FFh]

ATQ_CTRL16 is shown in Figure 7-103 and described in Table 7-87.

Read only

Return to the Register Maps Table

Figure 7-103. ATQ_CTRL16 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_DAC[7:0]							
R-11111111b							

Table 7-87. ATQ_CTRL16 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_DAC[7:0]	R	11111111b	Outputs the value of motor current when auto-torque is enabled. ATQ_TRQ_DAC can vary between ATQ_TRQ_MIN and ATQ_TRQ_MAX.

Note

When auto-torque is disabled, ATQ_TRQ_DAC reads the value programmed to ATQ_TRQ_MAX.

7.5.5.17 ATQ_CTRL17 (address = 0x2F) [Default = 00h]

ATQ_CTRL17 is shown in Figure 7-104 and described in Table 7-88.

Read/Write

Return to the Register Maps Table

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Figure 7-104. ATQ_CTRL17 Register

7	6	5	4	3	2	1	0
RSVD	VM_SCALE	RSVD					
R/W-0b	R/W-0b	R/W-000000b					

Table 7-88. ATQ_CTRL17 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved.
6	VM_SCALE	R/W	0b	When this bit is 1b, the learning routine will automatically modify the values of the learning parameters in the event of a supply voltage change.
5-0	RSVD	R/W	000000b	Reserved.

7.5.5.18 ATQ_CTRL18 (address = 0x30) [Default = 00h]

ATQ_CTRL18 is shown in Figure 7-105 and described in Table 7-89.

Read/Write

Return to the Register Maps Table

Figure 7-105. ATQ_CTRL18 Register

7	6	5	4	3	2	1	0
RSVD							
R/W-00000000b							

Table 7-89. ATQ_CTRL18 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	RSVD	R/W	00000000b	Reserved.

7.5.6 Silent Step Registers

The silent step registers control the silent step decay mode. Silent step registers are read and write capable.

Table 7-90 lists the memory-mapped registers for the silent step registers. All register offset addresses not listed in Table 7-90 should be considered as reserved locations and the register contents should not be modified.

Table 7-90. Silent step Registers Summary Table

Address	Register Name	Section
0x31	SS_CTRL1	Go
0x32	SS_CTRL2	Go
0x33	SS_CTRL3	Go
0x34	SS_CTRL4	Go
0x35	SS_CTRL5	Go

7.5.6.1 SS_CTRL1 (address = 0x31) [Default = 00h]

SS_CTRL1 is shown in Figure 7-106 and described in Table 7-91.

Read/Write

Return to the Register Maps Table

Figure 7-106. SS_CTRL1 Register

7	6	5	4	3	2	1	0

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Figure 7-106. SS_CTRL1 Register (continued)

SS_SMPL_SEL[1:0]	RSVD	SS_PWM_FREQ[1:0]	RSVD	EN_SS
R/W-00b	R/W-00b	R/W-00b	R/W-0b	R/W-0b

Table 7-91. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	SS_SMPL_SEL[1:0]	R/W	00b	Silent step current zero cross sampling time. Default value is 2 µs. If current waveform is distorted around zero crossing, increase the sampling time. • 00b = 2 µs (default) • 01b = 3 µs • 10b = 4 µs • 11b = 5 µs
5-4	RSVD	R/W	00b	Reserved.
3-2	SS_PWM_FREQ[1:0]	R/W	00b	Represents the PWM frequency (F_{PWM}) in silent step decay mode. • 00b - 25KHz • 01b - 33KHz • 10b - 42KHz • 11b - 50KHz
1	RSVD	R/W	0b	Reserved
0	EN_SS	R/W	0b	0b = silentstep decay mode is disabled 1b = silentstep decay mode is enabled

7.5.6.2 SS_CTRL2 (address = 0x32) [Default = 00h]

SS_CTRL2 is shown in Figure 7-107 and described in Table 7-92.

Read/Write

Return to the Register Maps Table

Figure 7-107. SS_CTRL2 Register

7	6	5	4	3	2	1	0
RSVD	SS_KP[6:0]						
R/W - 0b	R/W-0000000b						

Table 7-92. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved.
6-0	SS_KP[6:0]	R/W	0000000b	Represents the proportional gain of the silent step PI controller. Has a range of 0 to 127, with a default value of 0.

7.5.6.3 SS_CTRL3 (address = 0x33) [Default = 00h]

SS_CTRL3 is shown in Figure 7-108 and described in Table 7-93.

Read/Write

Return to the Register Maps Table

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Figure 7-108. SS_CTRL3 Register

7	6	5	4	3	2	1	0
RSVD	SS_KI[6:0]						
R/W-0b	R/W-0000000b						

Table 7-93. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved.
6-0	SS_KI[6:0]	R/W	0000000b	Represents the integral gain of the silent step PI controller. Has a range of 0 to 127, with a default value of 0.

7.5.6.4 SS_CTRL4 (address = 0x34) [Default = 00h]

SS_CTRL4 is shown in Figure 7-109 and described in Table 7-94.

Read/Write

Return to the Register Maps Table

Figure 7-109. SS_CTRL4 Register

7	6	5	4	3	2	1	0
RSVD	SS_KI_DIV_SEL[2:0]			RSVD	SS_KP_DIV_SEL[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 7-94. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved
6-4	SS_KI_DIV_SEL[2:0]	R/W	000b	Divider factor for KI. Actual KI = SS_KI / SS_KI_DIV_SEL • 000b - SS_KI/32 • 001b - SS_KI/64 • 010b - SS_KI/128 • 011b - SS_KI/256 • 100b - SS_KI/512 • 101b - SS_KI/16 • 110b - SS_KI
3-1	RSVD	R/W	0b	Reserved
0	SS_KP_DIV_SEL[2:0]	R/W	000b	Divider factor for KP. Actual KP = SS_KP / SS_KP_DIV_SEL. • 000b - SS_KP/32 • 001b - SS_KP/64 • 010b - SS_KP/128 • 011b - SS_KP/256 • 100b - SS_KP/512 • 101b - SS_KP/16 • 110b - SS_KP

7.5.6.5 SS_CTRL5 (address = 0x35) [Default = FFh]

SS_CTRL5 is shown in Figure 7-110 and described in Table 7-95.

Read/Write

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Return to the Register Maps Table

Figure 7-110. SS_CTRL5 Register

7	6	5	4	3	2	1	0
SS_THR[7:0]							
R/W-11111111b							

Table 7-95. SS_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	SS_THR[7:0]	R/W	11111111b	Programs the frequency at which the device transitions from silent step decay mode to another decay mode programmed by the DECAY bits. This frequency corresponds to the frequency of the sinusoidal current waveform. • 00000001b = 2 Hz • 00000010b = 4 Hz • . • . • **11111111b = 510 Hz**

Note

Do not set SS_THR to 00000000b.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV8452 is used to control bipolar stepper motors.

8.2 Typical Application

The following design procedure can be used to configure the DRV8452.

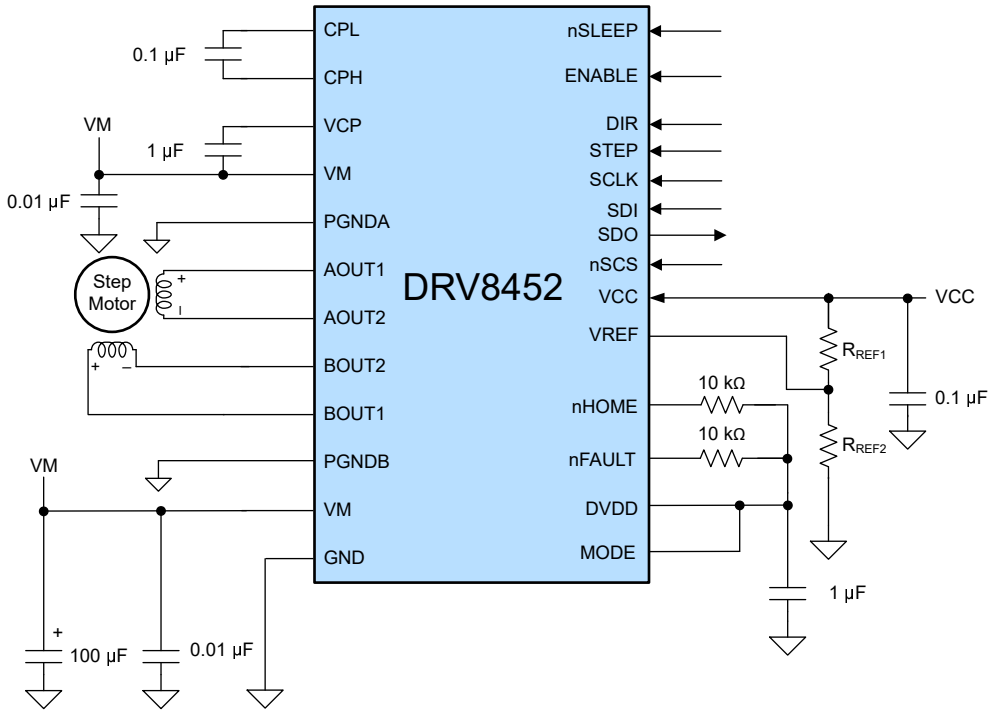

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	0.5 Ω/phase
Motor winding inductance	L_L	0.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/16 step
Target motor speed	v	7.5 rpm
Target full-scale current	I_{FS}	5 A (DDW), 4 A (PWP)

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8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8452 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed. Use Equation 15 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{step}\ (\text{steps}/\text{s}) = \frac{\text{v}\ (\text{rpm}) \times 360\ (^\circ/\text{rot})}{\theta_{step}\ (^\circ/\text{step}) \times n_m\ (\text{steps}/\text{microstep}) \times 60\ (\text{s}/\text{min})} \tag{15}$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor. For example, the motor in this application is required to rotate at 1.8°/step for a target of 7.5 rpm at 1/16 microstep mode. Using Equation 15, f_{step} can be calculated as 400 Hz.

The microstepping level is set by the M0 and M1 pins or the MICROSTEP_MODE bits and can be any of the settings listed in Table 7-5. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher f_{step} to achieve the same motor speed.

8.2.3 Application Performance Plots

Ch 1 = Coil A current, Ch 5 = Coil B current, Ch 6 = AOUT1, Ch 7 = AOUT2

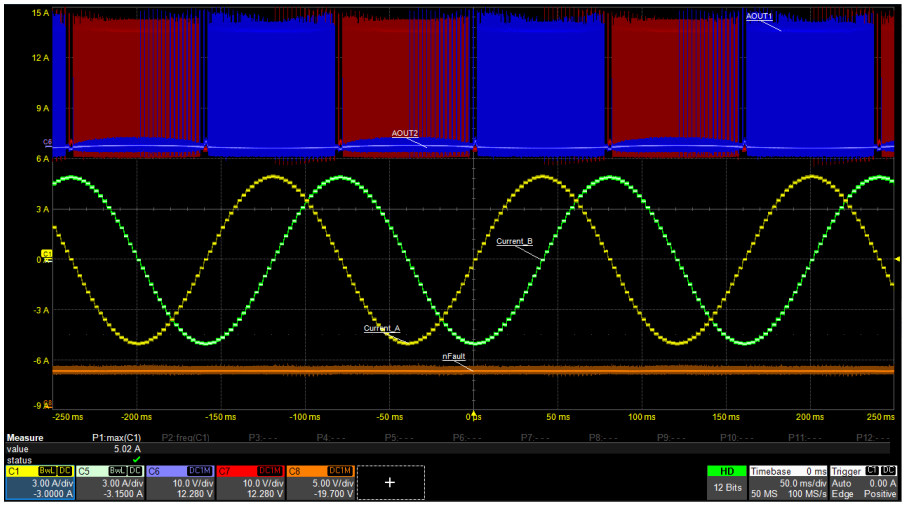

Figure 8-2. 1/16 microstepping at 400 pps with I_{FS} = 5 A

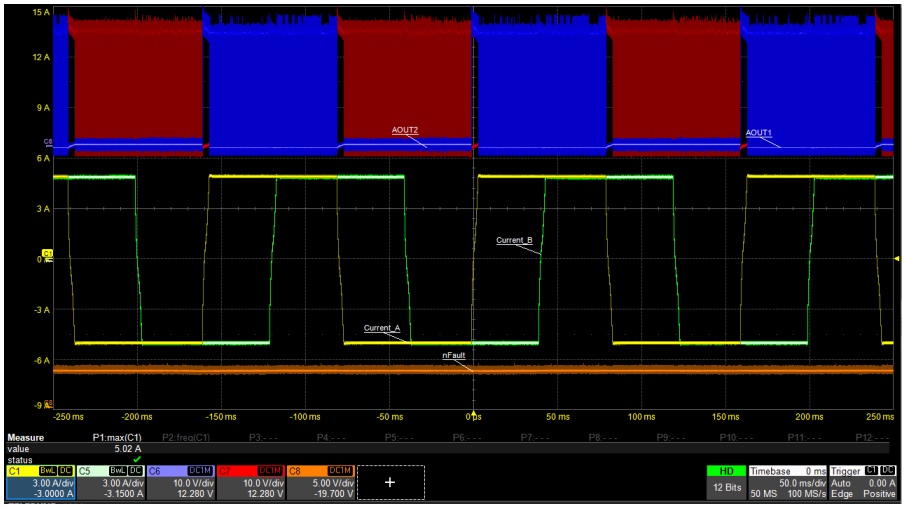

Figure 8-3. Full-step at 25 pps with I_{FS} = 5 A

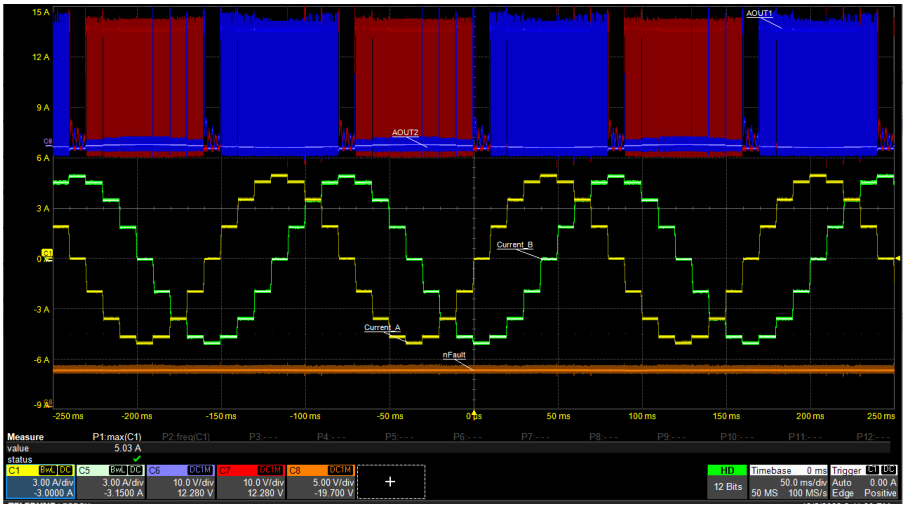

Figure 8-4. 1/4 microstepping at 100 pps with I_{FS} = 5 A

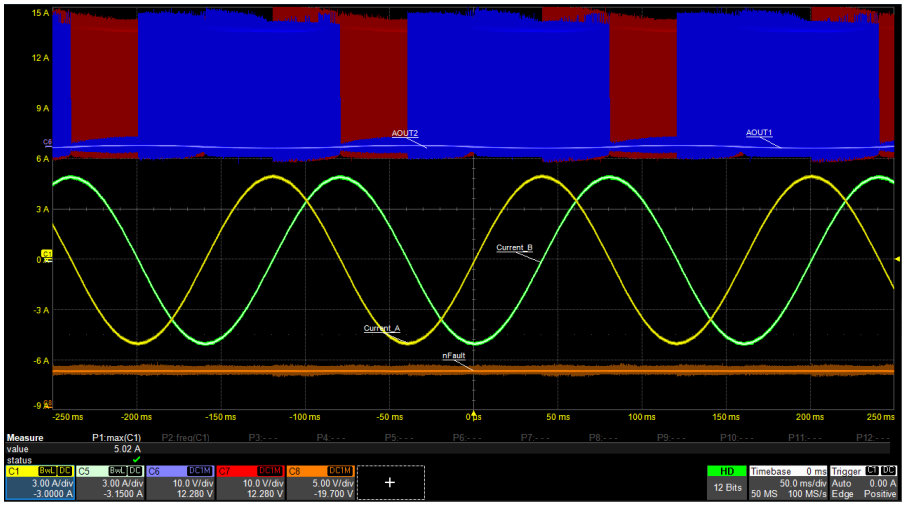

Figure 8-5. 1/256 microstepping at 6400 pps with I_{FS} = 5 A

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8.2.4 Thermal Application

This section presents the power dissipation calculation and junction temperature estimation of the device.

8.2.4.1 Power Dissipation

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

8.2.4.2 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 16.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \quad (16)$$

The conduction loss for the typical application shown in Table 8-1 is calculated below.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (5\text{-A} / \sqrt{2})^2 \times (0.106\text{-}\Omega) = 2.65\text{-W, for the DDW package} \quad (17)$$

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (4\text{-A} / \sqrt{2})^2 \times (0.117\text{-}\Omega) = 1.872\text{-W, for the PWP package} \quad (18)$$

Note

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

8.2.4.3 Switching Loss

The power loss due to the PWM switching frequency depends on the output voltage rise/fall time (t_{RF}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in Equation 19 and Equation 20.

$$P_{SW\_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (19)$$

$$P_{SW\_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (20)$$

The DRV8452 features two values of output rise/fall time (t_{RF}) - 140 ns and 70 ns. The smaller rise/fall time obviously results in lesser switching loss. Assuming t_{RF} = 140 ns and 30-kHz PWM frequencyfor this exercise, and after substituting the values of various parameters, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (140\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W, for the DDW package} \quad (21)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (140\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W, for the DDW package} \quad (22)$$

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (4\text{-A} / \sqrt{2}) \times (140\text{ ns}) \times 30\text{-kHz} = 0.143\text{-W, for the PWP package} \quad (23)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (4\text{-A} / \sqrt{2}) \times (140\text{ ns}) \times 30\text{-kHz} = 0.143\text{-W, for the PWP package} \quad (24)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.178\text{-W} + 0.178\text{-W}) = 0.712\text{-W for the DDW package} \quad (25)$$

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$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.143\text{-W} + 0.143\text{-W}) = 0.572\text{-W for the PWP package} \quad (26)$$

Note

The output rise/fall time (t_{RF}) is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application will depend on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

8.2.4.4 Power Dissipation Due to Quiescent Current

When the VCC pin is connected to an external voltage, the quiescent current is typically 5 mA. The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (27)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 5\text{-mA} = 0.12\text{-W} \quad (28)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variations.

8.2.4.5 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown below.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 2.65\text{-W} + 0.712\text{-W} + 0.12\text{-W} = 3.482\text{-W for the DDW package} \quad (29)$$

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 1.872\text{-W} + 0.572\text{-W} + 0.12\text{-W} = 2.564\text{-W for the PWP package} \quad (30)$$

8.2.4.6 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 22.5 °C/W for the DDW package and 24.5 °C/W for the PWP package.

Assuming 25°C ambient temperature, the junction temperature for the DDW package is calculated as shown below -

$$T_J = 25°C + (3.482\text{-W} \times 22.5\ °C/W) = 103.3\ °C \quad (31)$$

The junction temperature for the PWP package is calculated as shown below -

$$T_J = 25°C + (2.564\text{-W} \times 24.5\ °C/W) = 87.8\ °C \quad (32)$$

As explained in Section 8.2.4.2, for more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in Section 6.6.

For example,

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- At 103.3 °C junction temperature, the on-resistance will likely increase by a factor of 1.3 compared to the on-resistance at 25 °C.
- The initial estimate of conduction loss was 2.65 W.
- New estimate of conduction loss will therefore be 2.65 W x 1.3 = 3.445 W.
- New estimate of the total power loss will accordingly be 4.277 W.
- New estimate of junction temperature for the DDW package will be 121.2 °C.
- Further iterations are unlikely to increase the junction temperature estimate by significant amount.

8.2.4.7 Thermal Images

Figure 8-6 and Figure 8-7 show the thermal images of the DRV8452 EVM at room temperature ambient for the DDW package at 24V, 5A, 1/16 microstep, 6 kpps speed; with and without auto-torque enabled.

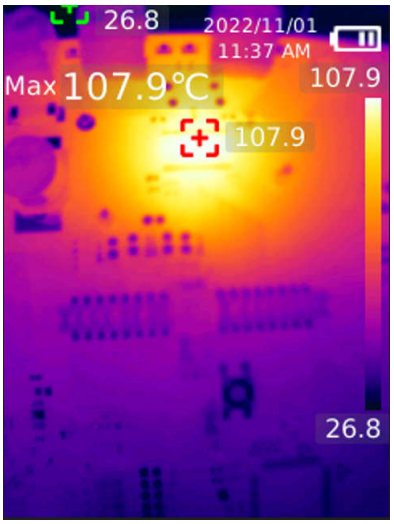

Figure 8-6. DDW package, auto-torque disabled

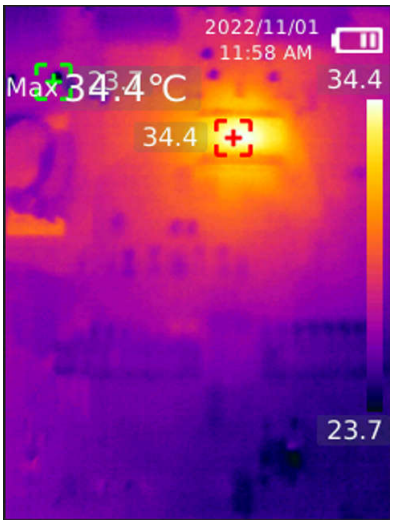

Figure 8-7. DDW package, auto-torque enabled

9 Thermal Considerations

9.1 Thermal Pad

Thermal pad of both DDW and PWP packages is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB in order to deliver the power specified in the datasheet. Refer to the Layout Guidelines section for more details.

9.2 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper on both top and bottom layer is recommended for improved thermal performance and better EMI margin (due to lower PCB trace inductance).

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10 Power Supply Recommendations

- The DRV8452 is designed to operate from an input voltage supply (VM) from 4.5 V to 55 V.
- A 0.01-µF ceramic capacitor rated for VM must be placed close to the VM pins of DRV8452.
- In addition, a bulk capacitor must be included on VM.

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

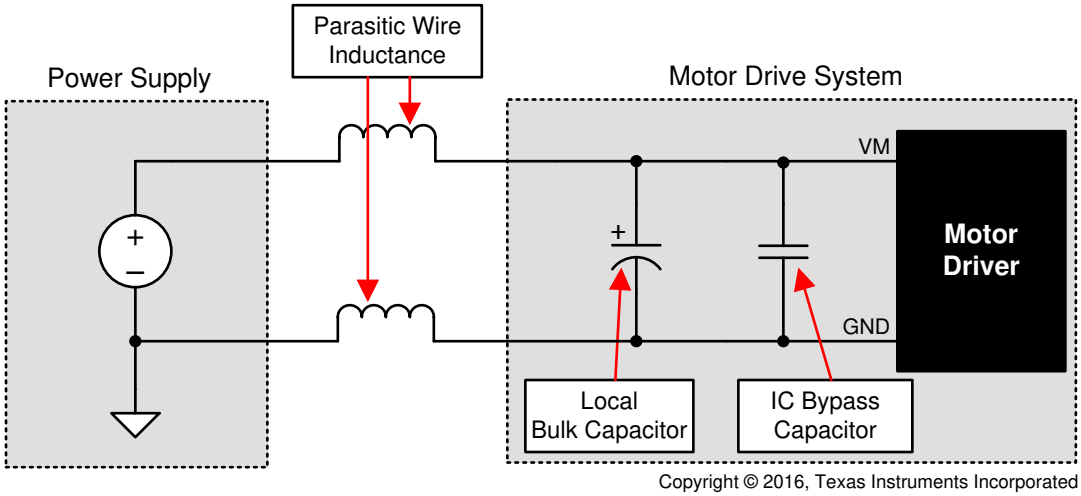

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Figure 10-1. Example Setup of Motor Drive System With External Power Supply

10.2 Power Supplies

The DRV8452 needs only a single supply voltage connected to the VM pins to operate properly.

- The VM pin provides the power supply to the H-Bridges.
- An internal voltage regulator provides a 5V supply (DVDD) for the digital and low-voltage analog circuitry. The DVDD pin is not recommended to be used as a voltage source for external circuitry.
- An optional external low-voltage supply can be connected to the VCC pin to power the internal circuitry. A 0.1-µF decoupling capacitor should be placed close to the VCC pin to provide a constant voltage during transient.

- Additionally, the high-side gate drive requires a higher voltage supply, which is generated by the built-in charge pump. The charg pump requires external capacitors.

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11 Layout

11.1 Layout Guidelines

- The VM pins should be bypassed to PGND pins using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VM. The capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device PGND pins.
- The VM pins should be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.
- A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.
- Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- Bypass the VCC pin to ground with a low-ESR ceramic capacitor. A value of 0.1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the package must be connected to system ground.
  - It is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer.
  - In order to minimize the impedance and inductance, the traces from ground pins should be as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Multiple vias are suggested to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD will also help spreading the heat and reduce the thermal resistance.

11.2 Layout Example

Follow the layout example of the DRV8452 EVM. The design files can be downloaded from the DRV8452EVM product folder.

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12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Related Documentation

- Texas Instruments, *Stepper motor system power loss reduction using auto-torque* application report
- Texas Instruments, *Integrated FETs vs External FETs: Performance Comparison of Motor Drivers* application report
- Texas Instruments, *How to Reduce Audible Noise in Stepper Motors* application report
- Texas Instruments, *How to Improve Motion Smoothness and Accuracy* application report
- Texas Instruments, *How smart tune regulates current in stepper motors* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *How to Drive Unipolar Stepper Motors with DRV8xxx* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Motor Drives Layout Guide* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8452DDWR	Active	Production	HTSSOP (DDW) | 44	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8452
DRV8452DDWR.A	Active	Production	HTSSOP (DDW) | 44	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8452
DRV8452PWPR	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8452
DRV8452PWPR.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8452
DRV8452SPWPR	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8452S
DRV8452SPWPR.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8452S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

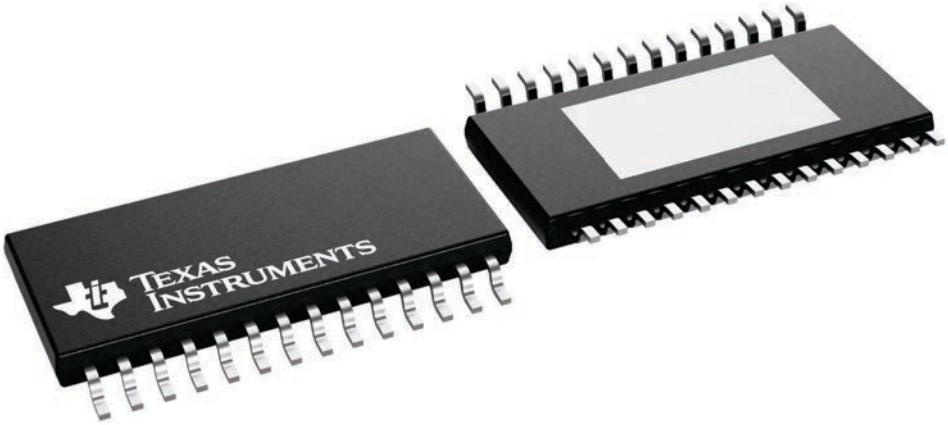
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

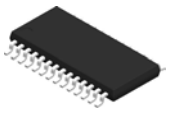
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

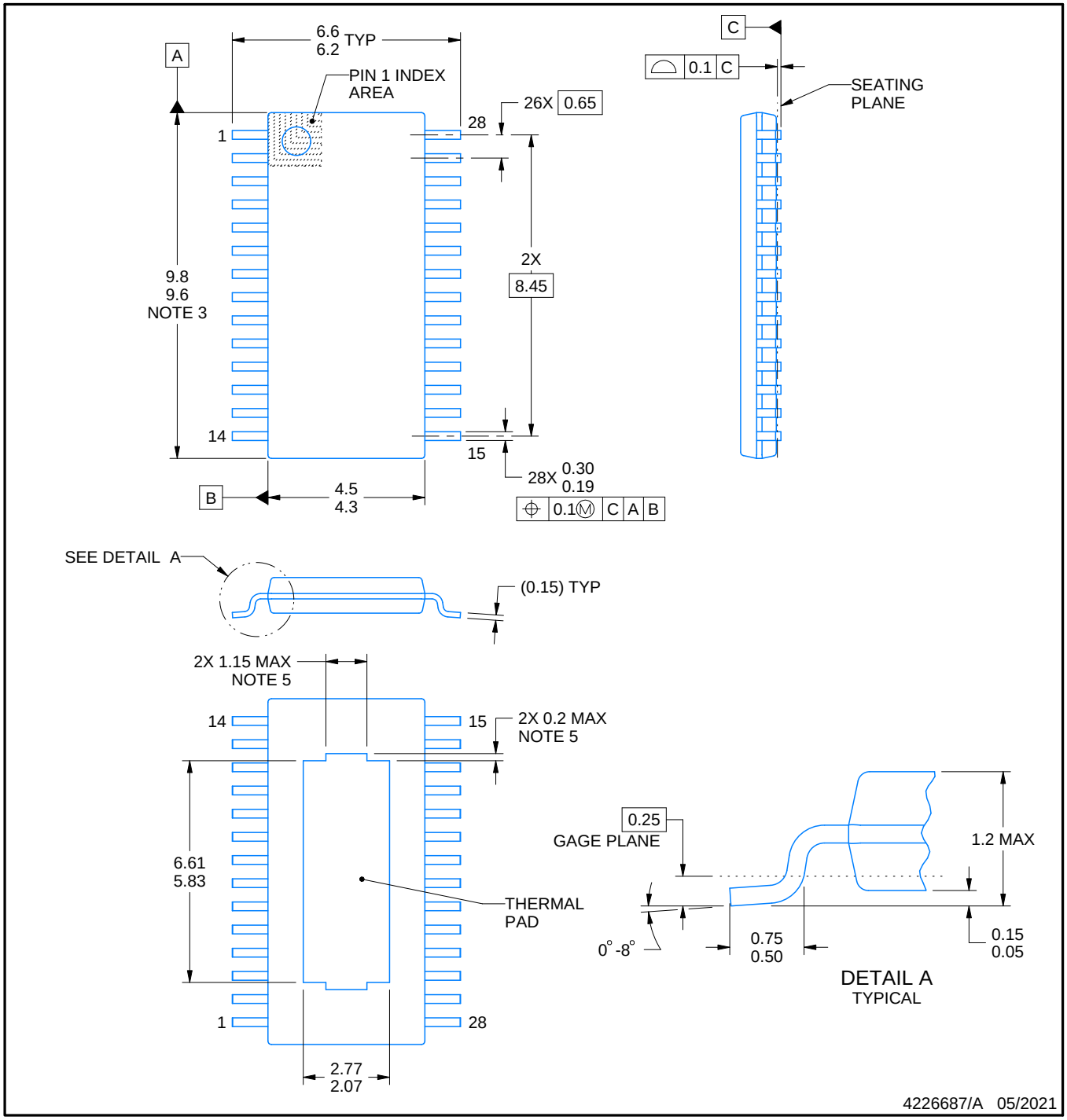
PACKAGE OUTLINE

PWP0028T



PowerPAD™ TSSOP - 1.2 mm max height

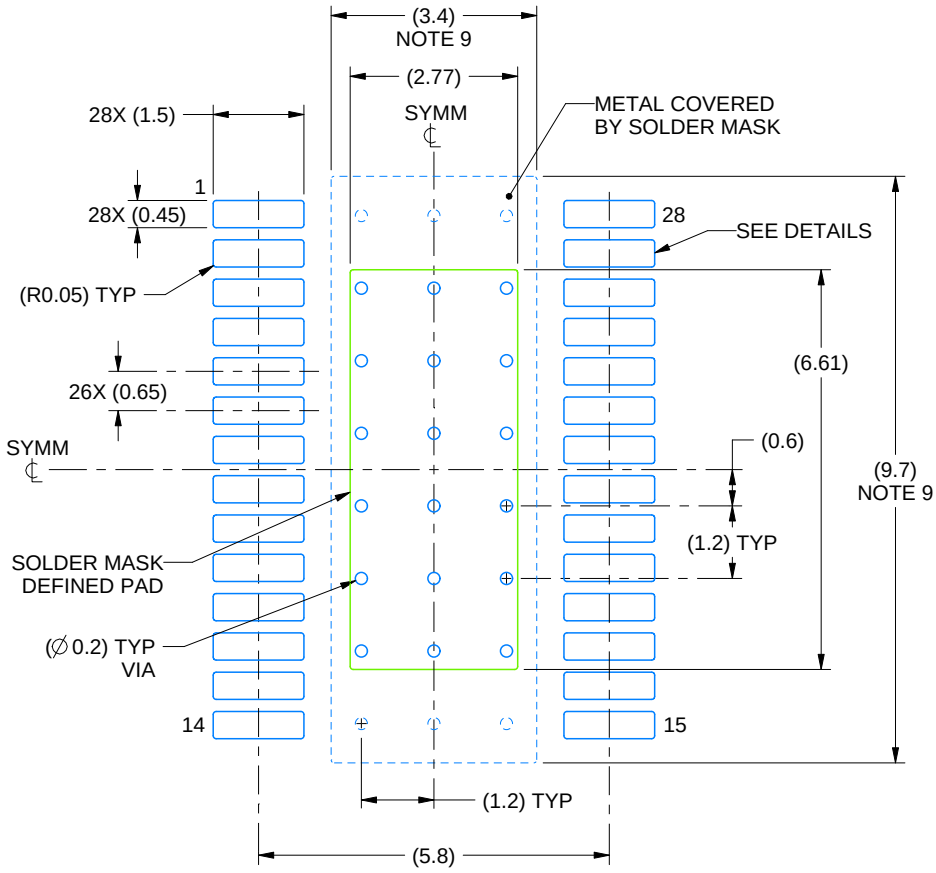
SMALL OUTLINE PACKAGE



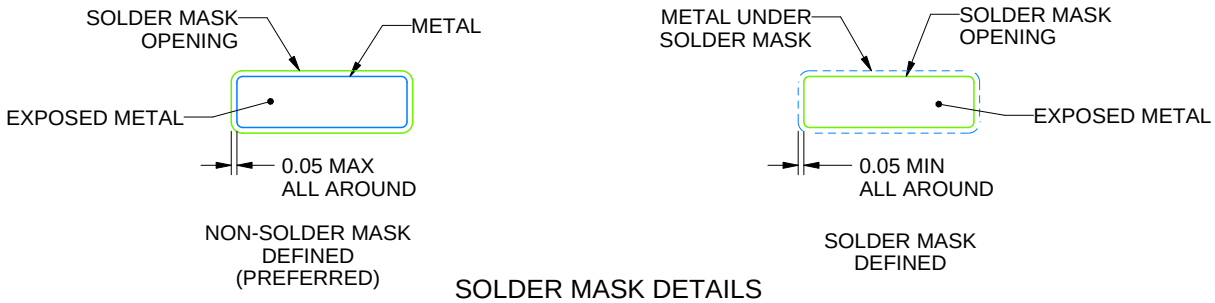
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

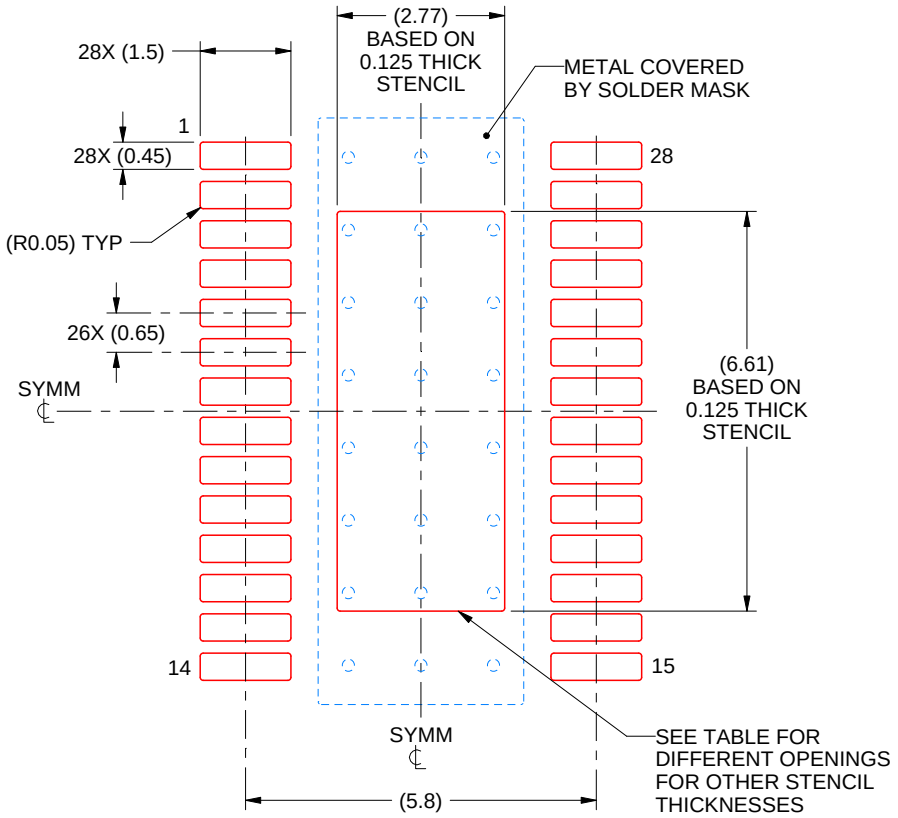


SOLDER MASK DETAILS

4226687/A 05/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

4226687/A 05/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

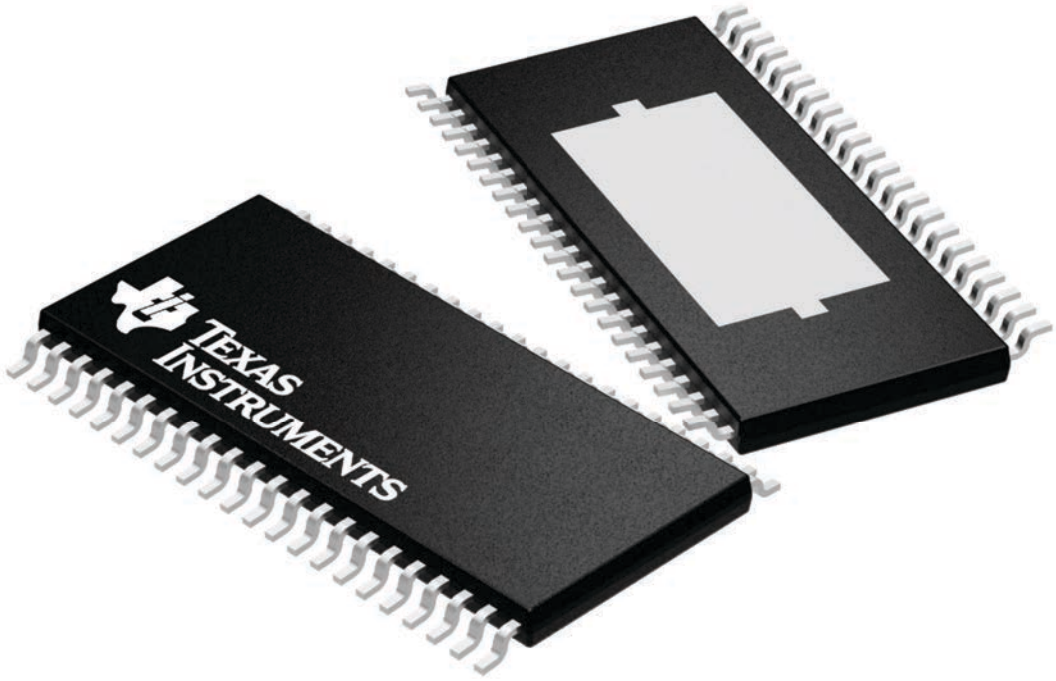
DDW 44

PowerPAD TSSOP - 1.2 mm max height

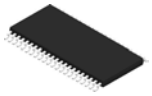
6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224876/A

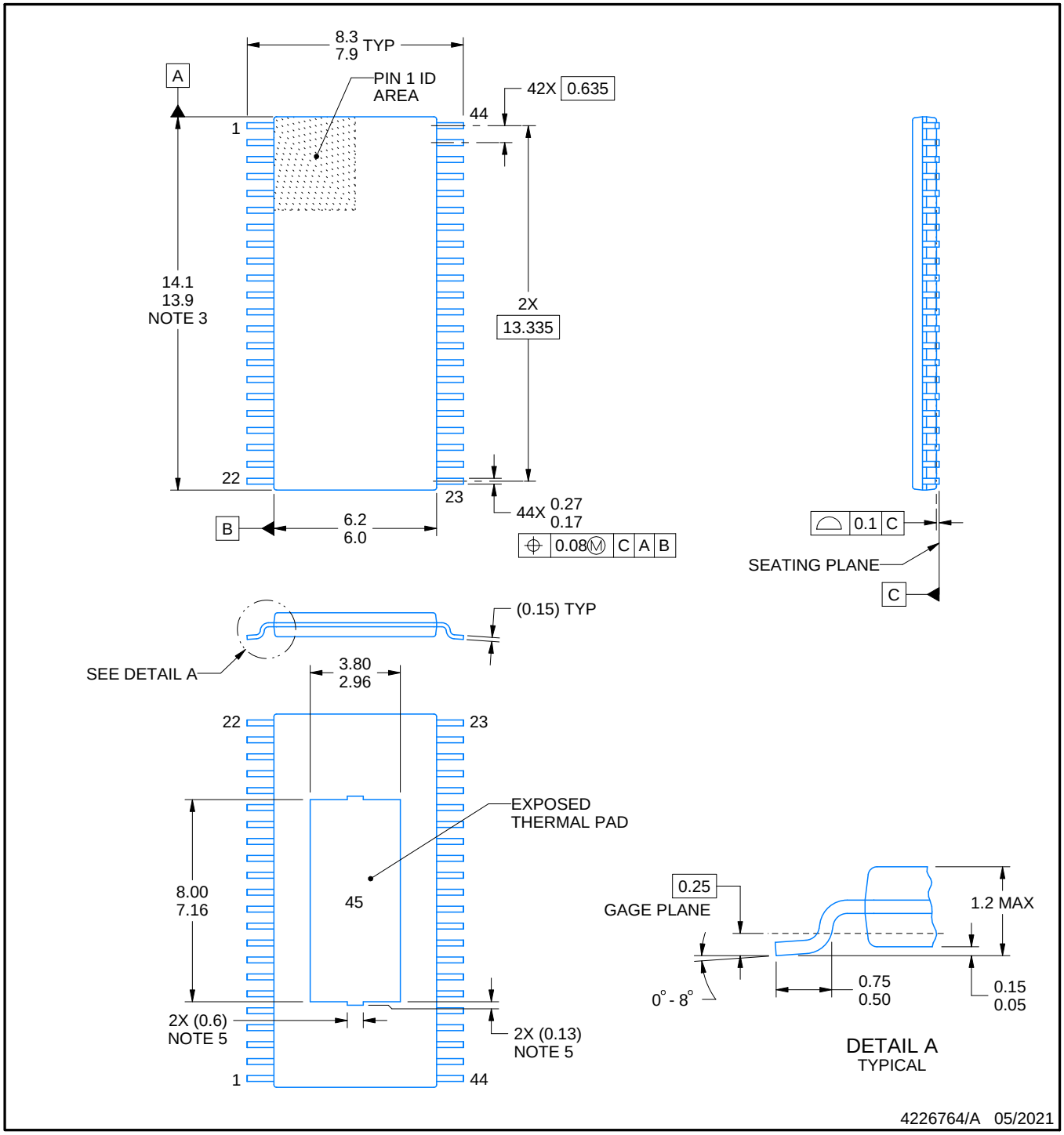


PACKAGE OUTLINE

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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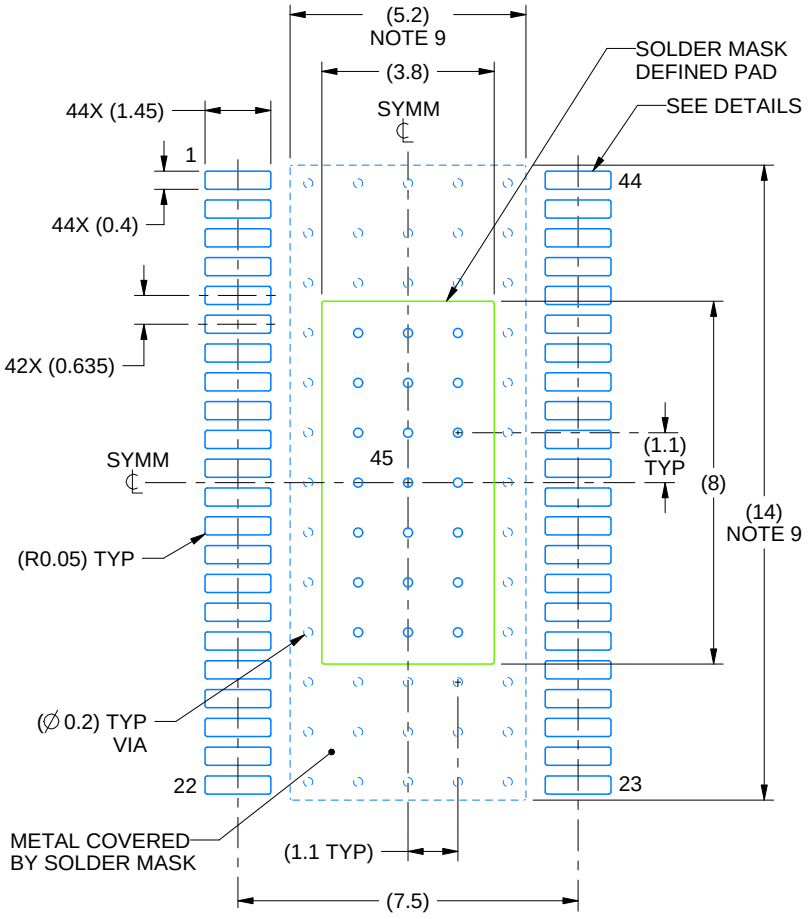
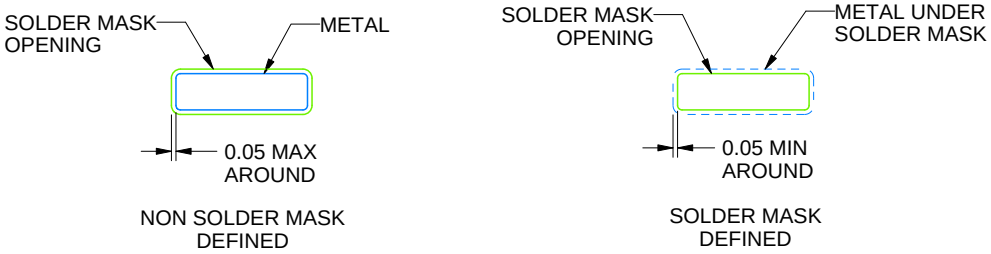
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

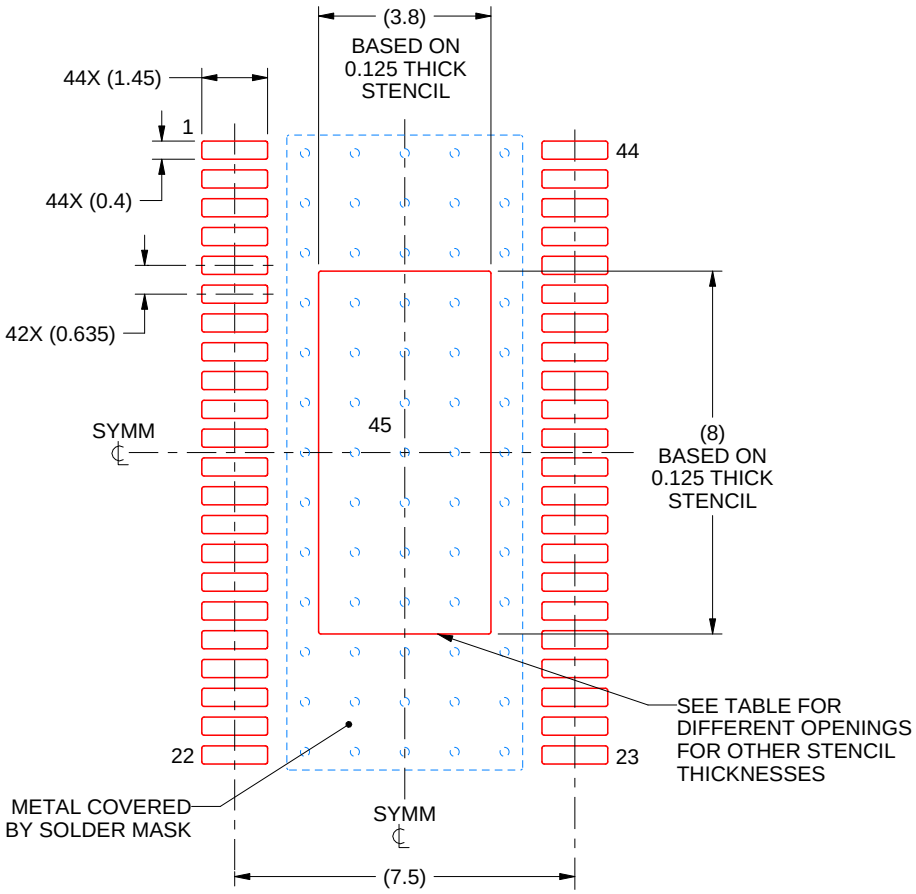


SOLDER MASK DETAILS
NOT TO SCALE

4226764/A 05/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

4226764/A 05/2021

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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