DRV8363-Q1 48V Battery Three-Phase Smart Gate Driver with Accurate Current Sensing and Advanced Monitoring

1 Features

- AEC-Q100 Test Guidance for automotive applications
  - Device ambient temperature: –40°C to +125°C
- Three phase half-bridge gate driver
  - Drives six N-channel MOSFETs (NMOS)
  - 8 to 85V wide operating voltage range
  - Bootstrap architecture for high-side gate driver
  - Supports 50mA average gate switching current enables driving 400nC MOSFETs at 20kHz
  - Trickle charge pump to support 100% PWM duty cycle and to generate overdrive supply to drive external cut-off or reverse polarity protection circuit
- Smart Gate Drive architecture
  - 15-level configurable peak gate drive current up to 1000 / 2000mA (source / sink)
  - Closed-loop automatic deadtime insertion based on gate-source voltage monitoring
  - Configurable soft shutdown to minimize inductive voltage spikes during overcurrent shutdown
- Low-side Current Sense Amplifier
  - 1mV low input offset across temperature
  - 4-level adjustable gain
  - Adjustable output bias to support unidirectional or bidirectional sensing
- SPI-based detailed configuration and diagnostics
- DRVOFF pin to disable driver independently
- High voltage wake up pin (nSLEEP)
- Dedicated ASCIN pin to control motor braking (active short circuit)
- 6x, 3x, 1x, and Independent PWM Modes
- Supports 3.3V and 5V Logic Inputs
- Integrated protection features
  - Battery and power supply voltage monitors
  - MOSFET V_{DS} and R_{sense} over current monitors
  - MOSFET V_{GS} gate fault monitors
  - Device thermal warning and shutdown
  - Fault condition indicator pin

2 Applications

- 48V Automotive Motor Control Applications
  - Fuel, Water and Oil Pumps
  - Automotive Fans and Blowers
  - Automotive Body Motors
  - Transmission Actuators
  - Automotive BLDC and PMSM motors
- E-Mobility, E-Bikes, E-Scooters

3 Description

The DRV8363-Q1 is an integrated smart gate driver for 48V automotive three-phase BLDC applications. The device provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV8363-Q1 generates the correct gate drive voltages using an external 12V supply and an integrated bootstrap diode for the high-side MOSFETs. The Smart Gate Drive architecture supports configurable peak gate drive current from 16mA up to 1A source and 2A sink. The DRV8363-Q1 can operate with a wide input range from 8V to 85V at the motor connection. A trickle charge pump allows for the gate drivers to support 100% PWM duty cycle control and provides overdrive gate drive voltage of external switches.

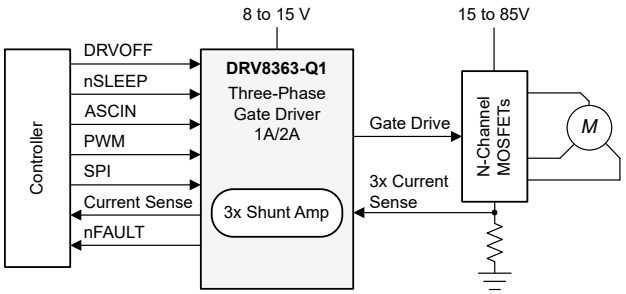
The DRV8363-Q1 provides low-side current sense amplifiers to support resistor based low-side current sensing. The low offset of the amplifiers enables the system to obtain precise motor current measurements.

A wide range of diagnostics and protection features are integrated with the DRV8363-Q1 enables a robust motor drive system design and helps eliminate the need of external components. The highly configurable device response allows the device to be integrated seamlessly into a variety of system designs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)(2)
DRV8363-Q1	QFN (48)	7mm × 7mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Functions 48-Pin DRV8363-Q1

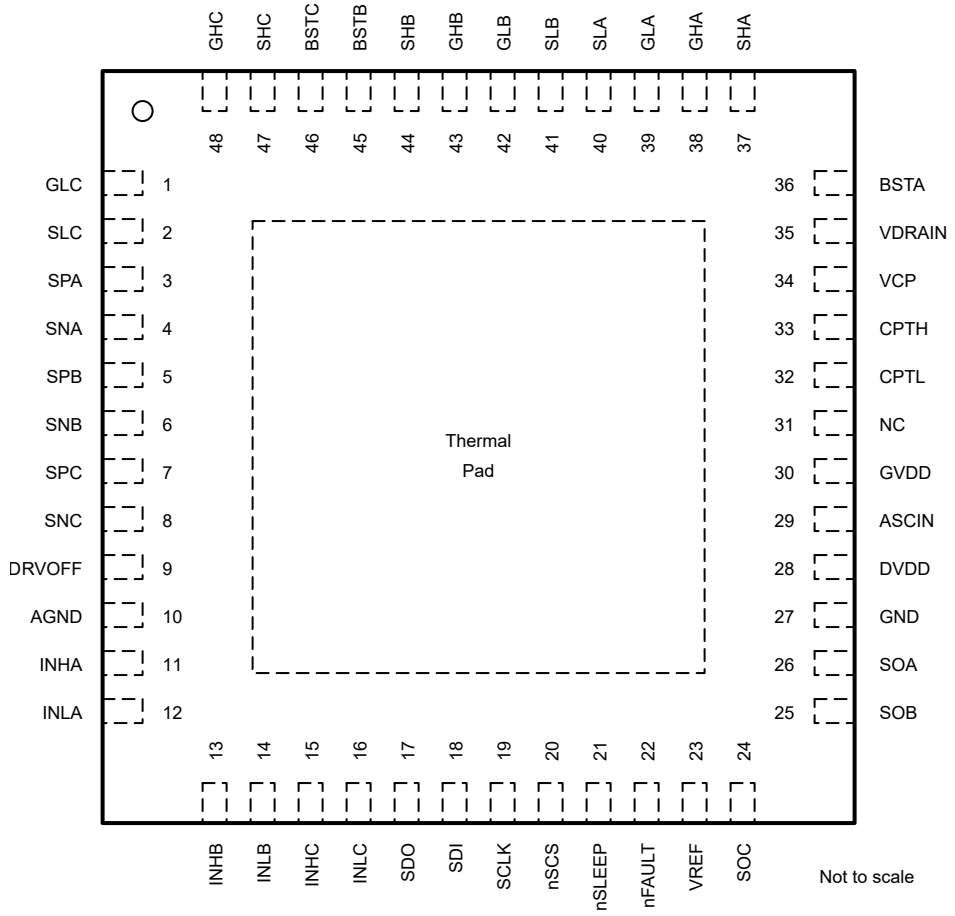

Figure 4-1. DRV8363-Q1 Package 48-Pin QFN With Exposed Thermal Pad Top View

Table 4-1. Pin Functions (48-QFN)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
GLC	1	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
SLC	2	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SPA	3	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SNA	4	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SPB	5	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SNB	6	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SPC	7	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SNC	8	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
DRVOFF	9	I	Active high shutdown input to pull-down gate driver outputs GHx and GLx.
AGND	10	PWR	Device ground.
INHA	11	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	12	I/O	Low-side gate driver control input. This pin controls the output of the low-side gate driver.

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Table 4-1. Pin Functions (48-QFN) (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
INHB	13	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLB	14	I/O	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INHC	15	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLC	16	I/O	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
SDO	17	O	Serial data output.
SDI	18	I	Serial data input.
SCLK	19	I	Serial clock input.
nSCS	20	I	Serial chip select.
nSLEEP	21	I	Gate driver nSLEEP. When this pin is logic low the device goes to a low-power sleep mode.
nFAULT	22	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
VREF	23	PWR	External voltage reference for current sense amplifiers.
SOC	24	O	Current sense amplifier output.
SOB	25	O	Current sense amplifier output.
SOA	26	O	Current sense amplifier output.
GND	27	PWR	Device ground
DVDD	28	PWR	3.3V / 5V LDO output. Connect to adjacent GND with a >10V-rated ceramic capacitor.
ASCIN	29	I	ASC external trigger pin. When this pin is logic high, the device turns on all three low-side or high-side gates.
GVDD	30	PWR	Gate driver power supply output. Connect an externally regulated 10V-15V supply with a GVDD-rated ceramic between the GVDD and GND pins.
NC	31	NC	Not connected. Leave pin floating.
CPTL	32	PWR	Trickle charge pump switching node. Connect a charge pump flying capacitor between CPTL and CPTH pins.
CPTH	33	PWR	Trickle charge pump switching node. Connect a charge pump flying capacitor between CPTL and CPTH pins.
VCP	34	PWR	Trickle charge pump storage capacitor. Connect a ceramic capacitor between VCP and VDRAIN pins.
VDRAIN	35	PWR	High-side drain sense and charge pump power supply input.
BSTA	36	O	Bootstrap output pin. Connect a bootstrap capacitor between BSTA and SHA
SHA	37	I	High-side source sense input. Connect to the high-side power MOSFET source.
GHA	38	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	39	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
SLA	40	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SLB	41	I	Low-side source sense input. Connect to the low-side power MOSFET source.
GLB	42	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GHB	43	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
SHB	44	I	High-side source sense input. Connect to the high-side power MOSFET source.
BSTB	45	O	Bootstrap output pin. Connect a bootstrap capacitor between BSTB and SHB
BSTC	46	O	Bootstrap output pin. Connect a bootstrap capacitor between BSTC and SHC
SHC	47	I	High-side source sense input. Connect to the high-side power MOSFET source.
GHC	48	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output., PWR = Power

5 Specification

5.1 Absolute Maximum Ratings

Over recommended operating conditions (unless otherwise noted)(1)

		MIN	MAX	UNIT
Gate driver regulator pin voltage	GVDD	-0.3	20	V
High-side drain pin voltage	VDRAIN	-0.3	85	V
Bootstrap pin voltage	BSTx	-0.3	105	V
Bootstrap pin voltage	BST with respect to SH	-0.3	20	V
Logic pin voltage	nSLEEP, DRVOFF, BRAKE	-0.3	35	V
Logic pin voltage	nFAULT	-0.3	6	V
	INHx, INLx	-0.3	35	
	SCLK, nSCS, SDI, SDO	-0.3	6	
High-side gate drive pin voltage	GH	-5	105	V
Transient high-side gate drive pin negative voltage	GH, 1 µs	-20		V
High-side gate drive pin voltage	GH with respect to SH	-0.3	20	V
High-side source pin voltage	SH, DC	-5	105	V
Transient high-side source pin negative voltage	SH, 1 µs	-20		V
High-side source pin slew rate	SH , V_{BST-SH} >4.3V		20	V/ns
Low-side gate drive pin voltage	GL with respect to SL	-0.3	20	V
Low-side source sense pin voltage	SL	-5	V_{GVDD}+0.3	V
Transient low-side source sense pin negative voltage	SL, 1 µs	-16		V
Current sense amplifer reference input pin voltage	CSAREF	-0.3	5.5	V
Shunt amplifier input pin voltage	SN, SP	-1	1	V
Transient 500-ns shunt amplifier input pin voltage	SN, SP, 500ns	-16	20	V
Shunt amplifier output pin voltage	SO	-0.3	V_{CSAREF} + 0.3	V
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

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5.2 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{GVDD}	Power supply voltage	GVDD	8		20	V
V_{VDRAIN}	High-side drain pin voltage	VDRAIN, low-side gate drive, and high-side gate drive switching with bootstrap	0		85	V
	High-side drain pin voltage	VDRAIN, to support trickle charge pump capability V_{TCP} min > V_{BST_UV} max (falling), for high-side gate drive 100% and no BST_UV detection. VDRAIN>GVDD+4V, GVDD>9V	13			V
V_{BST-SH}	Bootstrap pin voltage with respect to SH	BST (V_{BST} - V_{SH}), high-side gate drive switching and no BST_UV detection, V_{BST-SH} min > V_{BST_UV} max (rising),	6.1		20	V
V_{BST}	Bootstrap pin voltage	BST	0		105	V
V_{SH}	High-side source pin voltage	SH	-2		85	V
$I_{TRICKLE}$	Trickle charge pump external load current	BST/phase			130	µA
V_I	Input voltage	INH, INL, SDI, SCLK, nSCS	0		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT			5.5	V
I_{OD}	Open drain output current	nFAULT			–5	mA
V_{CSAREF}	Current sense amplifier reference voltage	CSAREF	3.0		5.5	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

5.3 Thermal Information 1pkg

THERMAL METRIC[1]		DRV8363 RGZ (QFN) 48	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (GVDD, VDRAIN, DVDD)						
I_{VDRAIN_UNPWR}	VDRAIN sleep current under GVDD unpowered	GVDD = 0V, VDRAIN = 48V, V_{BST-SH} = 0V, nSLEEP=0V, Tj 25C; SH=VDRAIN & 0V Leakage current of VDRAIN when SH=0V; Leakage current of VDRAIN+SH when SH=VDRAIN [all 3 predriver phases put together]	2	4.5	13.5	µA
I_{GVDD}	GVDD standby mode current	GVDD = 12V, VDRAIN = 48V, INH = INL = 0; DRVOFF = Low, SHx=0V. TCP = ON No external Load on VCP. [TCP switches will be toggling]	9.5	13.4	17.5	mA
I_{GVDD}	GVDD standby mode current	GVDD = 12V, VDRAIN = 48V, INH = INL = 0; DRVOFF = High, SHx=VDRAIN TCP = ON No external Load on VCP. [TCP switches will be ON]	9.7	11.7	16.6	mA
I_{GVDD}	GVDD active mode current	GVDD = 12V, VDRAIN = 48V, INH = INL = Switching @ 20kHz; SH=0 when INL=1, SH=VDRAIN when INH=1; SH retains voltage when INH=INL=0; NO FETs connected. TCP is ON, TCP switches will toggle	9.8	13.1	20	mA
t_{WAKE}	Turnon time	GVDD = 12V nSLEEP = High to active mode (outputs ready) (nFAULT = High)			10	ms
V_{DVDD_RT}	DVDD Digital regulator voltage (Room Temperature)	V_{GVDD} ≥ GVDD_UVH, 0 mA ≤ I_{DVDD} ≤ 30 mA external load + 0mA-5mA internal digital load, T_J= 25°C, LDO_5P0=0	3.2	3.3	3.4	V
V_{DVDD_RT}	DVDD Digital regulator voltage (Room Temperature)	V_{GVDD} ≥ GVDD_UVH, 30 mA ≤ I_{DVDD} ≤ 100 mA external load + 0mA-5mA internal digital load, T_J= 25°C, LDO_5P0=0	3.2	3.3	3.4	V
V_{DVDD}	DVDD Digital regulator voltage	V_{GVDD} ≥ GVDD_UVH, 0 mA ≤ I_{DVDD} ≤ 30 mA external load + 0mA-5mA internal digital load, LDO_5P0=0	3.1	3.3	3.5	V
V_{DVDD}	DVDD Digital regulator voltage	V_{GVDD} ≥ GVDD_UVH, 30 mA ≤ I_{DVDD} ≤ 100 mA external load + 0mA-5mA internal digital load, LDO_5P0=0	3.1	3.3	3.5	V
V_{DVDD_RT}	DVDD Digital regulator voltage (Room Temperature)	V_{GVDD} ≥ 6.5V, 0 mA ≤ I_{DVDD} ≤ 30 mA external load + 0mA-5mA internal digital load, T_J= 25°C, LDO_5P0=1	4.85	5	5.15	V
V_{DVDD_RT}	DVDD Digital regulator voltage (Room Temperature)	V_{GVDD} ≥ 6.5V, 30 mA ≤ I_{DVDD} ≤ 100 mA external load + 0mA-5mA internal digital load, T_J= 25°C, LDO_5P0=1	4.85	5	5.15	V
V_{DVDD}	DVDD Digital regulator voltage	V_{GVDD} ≥ 6.5V, 0 mA ≤ I_{DVDD} ≤ 30 mA external load + 0mA-5mA internal digital load, LDO_5P0=1	4.7	5	5.3	V
V_{DVDD}	DVDD Digital regulator voltage	V_{GVDD} ≥ 6.5V, 30 mA ≤ I_{DVDD} ≤ 100 mA external load + 0mA-5mA internal digital load, LDO_5P0=1	4.7	5	5.3	V
LOGIC-LEVEL INPUTS (INHx, INLx, nSLEEP, etc.)						
V_{IL}	Input logic low voltage	NSLEEP pin. GVDD>4.5V			0.8	V
V_{IL}	Input logic low voltage	DRVOFF pin. GVDD>4.5V			0.8	V
V_{IL}	Input logic low voltage	INLx, INHx, BRAKE, SDI, SCLK, nSCS. GVDD>4.5V			0.8	V

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(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input logic high voltage	NSLEEP pin. GVDD>4.5V	2.2			V
V_{IH}	Input logic high voltage	DRVOFF pin. GVDD>4.5V	2.2			V
V_{IH}	Input logic high voltage	INLx, INHx, DRVOFF, BRAKE, SDI, SCLK, nSCS GVDD>4.5V DVDD<4V	2.2			V
V_{IH}	Input logic high voltage	INLx, INHx, DRVOFF, BRAKE, SDI, SCLK, nSCS GVDD>4.5V DVDD<5.25V	2.6			V
V_{IH}	Input logic high voltage	INLx, INHx, DRVOFF, BRAKE, SDI, SCLK, nSCS GVDD>4.5V DVDD<6V	2.9			V
V_{HYS}	Input hysteresis	NSLEEP	100	250	500	mV
V_{HYS}	Input hysteresis	DRVOFF	50	200	400	mV
I_{IL}	Input logic low current	INLx, INHx, DRVOFF, EBRAKE, SDI, SCLK = 0V	-1	0	1	µA
R_{PU}	Input pullup resistance	nSCS to DVDD pin	50	100	200	kΩ
R_{PD}	Input pulldown resistance	SDI, SCLK to GND [Measurement condition : Pin at 2.2V]	50	100	200	kΩ
R_{PD}	Input pulldown resistance	INLx, INHx, DRVOFF, BRAKE,NSLEEP to GND.[Measurement condition : Pin at 2.2V]	150	250	350	kΩ
tNSLEEP_DG	NSLEEP input deglitch time	NSLEEP to EN_2US falling and rising	1	2	4	µs
tDRVOFF_DG	DRVOFF input deglitch time	DRVOFF to DRVOFF_DG1 falling and rising	1	2	4	µs
OPEN-DRAIN OUTPUT (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA, GVDD > 4V			0.4	V
I_{OZ}	Output logic high current	V_{OD} = 5 V	-1		1	µA
BOOTSTRAP DIODE (BST)						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA			0.82	V
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 10 mA			1	V
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 mA			1.6	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 50 mA	3.9	4.8	9	Ω
TRICKLE CHARGE PUMP (VCP)						
V_{TCP}	Trickle charge pump output voltage	$V_{VCP-VDRAIN}$, VDRAIN > 15V, GVDD>11V, VDRAIN>GVDD+4V; External load I_{VCP} < 4mA	10.3	10.7	10.9	V
V_{TCP}	Trickle charge pump output voltage	$V_{VCP-VDRAIN}$, VDRAIN > 15V, 8V<GVDD<11V, VDRAIN>GVDD+4V; External load I_{VCP} < 2mA	7.5	7.8	8.0	V
	Trickle charge pump output voltage	$V_{VCP-VDRAIN}$, VDRAIN=GVDD, 8V<GVDD<11V, External load I_{VCP} < 2mA	4.0	5.4	6.7	V
V_{BST_TCPOFF}	BST monitor voltage for VCP to stop charging the BST cap (rising voltage)	INLx = 0; SHx = 0, VDRAIN; VDRAIN = 48V, 85V	12.0	13.2	14.6	V
$T_{PRECHARGE}$	Startup time for bootstrap precharge	INH=INL=0; BST_UVLO=highest level; TCP_SWITCH=PRECHARGE mode (5mA); GVDD > 11V, VDRAIN > GVDD + 4V; SHx=VDRAIN; I_EXT_LOAD=6.25K Ohm between VCP->VDRAIN; spec time is 200us after BST_UVLO clears (Garret agreed to 6.25K and BST_UVLO+200us 12/12/23); BST_UVLO=0 (high UVLO level)		1.5	3	ms
GATE DRIVERS (GH, GL, SH, SL)						

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(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GSHx_LO}	High-side gate drive low level voltage (V_{GH} - V_{SH})	I_{GHx} = -10 mA; V_{GVDD} = 12V; IDRIVE = 1000mA, No FETs connected	0	0.022	0.2	V
V_{GSHx_HI}	High-side gate drive high level voltage (V_{BST} - V_{GH})	I_{GHx} = 10 mA; V_{GVDD} = 12V; IDRIVE = 500mA, No FETs connected	0	0.09	0.2	V
V_{GSLx_LO}	Low-side gate drive low level voltage (V_{GL} - V_{SL})	I_{GLx} = -10 mA; V_{GVDD} = 12V; IDRIVE = 1000mA, No FETs connected	0	0.022	0.2	V
V_{GSLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GL})	I_{GLx} = 10 mA; V_{GVDD} = 12V; IDRIVE = 500mA, No FETs connected	0	0.09	0.2	V
$I_{DRIVEP0}$	Peak source gate current	V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x0	9	16	26	mA
$I_{DRIVEP1}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x1	19	32	52	mA
$I_{DRIVEP2}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x2	38	64	103	mA
$I_{DRIVEP3}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x3	57	96	154	mA
$I_{DRIVEP4}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x4	76	128	205	mA
$I_{DRIVEP5}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x5	96	160	256	mA
$I_{DRIVEP6}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x6	115	192	308	mA
$I_{DRIVEP7}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x7	134	224	359	mA
$I_{DRIVEP8}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x8	153	256	410	mA
$I_{DRIVEP9}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0x9	172	288	461	mA
$I_{DRIVEP10}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0xA	192	320	512	mA
$I_{DRIVEP11}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0xB	230	384	615	mA
$I_{DRIVEP12}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0xC	307	512	820	mA
$I_{DRIVEP13}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0xD	460	768	1229	mA
$I_{DRIVEP14}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVP_xx = 0xE	614	1024	1639	mA
$I_{DRIVEP15}$		V_{BST}-V_{SH} = V_{GVDD} = 12V,, IDRVP_xx = 0xF	614	1024	1639	mA

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(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRIVEN0}$	Peak sink gate current	V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x0	19	32	52	mA
$I_{DRIVEN1}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x1	38	64	103	mA
$I_{DRIVEN2}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x2	76	128	205	mA
$I_{DRIVEN3}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x3	115	192	308	mA
$I_{DRIVEN4}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x4	153	256	410	mA
$I_{DRIVEN5}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x5	192	320	512	mA
$I_{DRIVEN6}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x6	230	384	615	mA
$I_{DRIVEN7}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x7	268	448	717	mA
$I_{DRIVEN8}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x8	307	512	820	mA
$I_{DRIVEN9}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0x9	345	576	922	mA
$I_{DRIVEN10}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0xA	384	640	1024	mA
$I_{DRIVEN11}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0xB	460	768	1229	mA
$I_{DRIVEN12}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0xC	614	1024	1639	mA
$I_{DRIVEN13}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0xD	921	1536	2458	mA
$I_{DRIVEN14}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0xE	1228	2048	3277	mA
$I_{DRIVEN15}$		V_{BST}-V_{SH} = V_{GVDD} = 12V, IDRVN_xx = 0xF	1228	2048	3277	mA
R_{PD_LS}	Low-side passive pull down	GL to SL, V_{GL} - V_{SL} = 2V	60	85	120	kΩ
R_{PDSA_HS}	High-side semiactive pull down	GVDD_UV = 1 GH to SH, V_{GH} - V_{SH} = 2V	2	4	8	kΩ
I_{PUHOLD_L}	High-side pull-up hold low current		614	1024	1639	mA
I_{PUHOLD_H}	High-side pull-up hold high current		153	256	410	mA
$I_{PDSTRONG\_LS}$	Low-side pull-down strong current		1228	2048	3277	mA
$I_{PDSTRONG\_HS}$	High-side pull-down strong current		1228	2048	3277	mA
GATE DRIVERS TIMINGS						
t_{PDR_LS}	Low-side rising propagation delay	INL to GL rising, V_{GVDD} > 8V	45	63	90	ns
t_{PDF_LS}	Low-side falling propagation delay	INL to GL falling, V_{GVDD} > 8V	45	64	90	ns
t_{PDR_HS}	High-side rising propagation delay	INH to GH rising, V_{GVDD} = V_{BST} - V_{SH} > 8V	45	62	90	ns
t_{PDF_HS}	High-side falling propagation delay	INH to GH falling, V_{GVDD} = V_{BST} - V_{SH} > 8V	45	65	90	ns

ADVANCE INFORMATION

(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD_MATCH}	Matching propagation delay of low-side gate driver	GL turning ON to GL turning OFF, From V_{GL-SL} = 1V to V_{GL-SL} = V_{GVDD} - 1V; V_{GVDD} = V_{BST} - V_{SH} > 8V; V_{SH} = 0V to 90V, no load on GH and GL	-8	±4	8	ns
	Matching propagation delay of high-side gate driver	GH turning ON to GH turning OFF, From V_{GH-SH} = 1V to V_{GH-SH} = V_{BST-SH} - 1V; V_{GVDD} = V_{BST} - V_{SH} > 8V; V_{SH} = 0V to 90V, no load on GH and GL	-10	±4	10	ns
$t_{PD\_MATCH\_PH}$	Matching propagation delay per phase	Deadtime disabled. GL turning OFF to GH turning ON, From V_{GL-SL} = V_{GVDD} - 1V to V_{GH-SH} = 1V; V_{GVDD} = V_{BST} - V_{SH} > 8V; V_{SH} = 0V to 90V, no load on GH and GL, dead time disabled	-12	±4	12	ns
		Deadtime disabled. GH turning OFF to GL turning ON, From V_{GH-SH} = V_{BST-SH} - 1V to V_{GL-SL} = 1V ; V_{GVDD} = V_{BST} - V_{SH} > 8V; V_{SH} = 0V to 90V, no load on GH and GL	-11	±4	11	ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0000b = 0h		70		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0001b = 1h		120		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0010b = 2h		180		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0011b = 3h		300		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0100b = 4h		400		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0101b = 5h		500		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0110b = 6h		600		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 0111b = 7h		750		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 1000b = 8h		1000		ns
t_{DEAD}	Digital gate drive dead time	DEADT = 1001b = 9h		1.5		us
t_{DEAD}	Digital gate drive dead time	DEADT = 1010b = Ah		2		us
t_{DEAD}	Digital gate drive dead time	DEADT = 1011b = Bh		2.5		us
t_{DEAD}	Digital gate drive dead time	DEADT = 1100b = Ch		3		us
t_{DEAD}	Digital gate drive dead time	DEADT = 1101b = Dh		3.5		us
t_{DEAD}	Digital gate drive dead time	DEADT = 1110b = Eh		5		us
t_{DEAD}	Digital gate drive dead time	DEADT = 1111b = Fh		10		us
t_{DEAD}	Analog propagation delay dead time variation	Inserted on top of digital deadtime	-12	4	12	ns
CURRENT SHUNT AMPLIFIERS (SNx, SOx, SPx, CSAREF)						
A_{CSA}	Sense amplifier gain	CSAGAIN = 00b		5		V/V
		CSAGAIN = 01b		10		V/V
		CSAGAIN = 10b		20		V/V
		CSAGAIN = 11b		40		V/V
A_{CSA}	Sense amplifier gain	CSAGAIN = 00b	4.9	5	5.08	V/V
		CSAGAIN = 01b	9.85	10	10.15	V/V
		CSAGAIN = 10b	19.7	20	20.3	V/V
		CSAGAIN = 11b	39.4	40	40.8	V/V
$A_{CSA\_ERR\_DRIFT}$	Sense amplifier gain error temperature drift		-30		30	ppm/℃
NL	Non linearity Error			0.01	0.05	%

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(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, C_{SO} = 500pF; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		0.6	1.6	µs
		V_{STEP} = 1.6 V, A_{CSA} = 10 V/V, C_{SO} = 500pF; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		0.65	1.6	µs
		V_{STEP} = 1.6 V, A_{CSA} = 20 V/V, C_{SO} = 500pF; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		0.7	1.6	µs
		V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, C_{SO} = 500pF; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		1.25	2.1	µs
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, C_{SO} = 60pF ; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		0.3	0.6	µs
		V_{STEP} = 1.6 V, A_{CSA} = 10 V/V, C_{SO} = 60pF; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		0.35	0.6	µs
		V_{STEP} = 1.6 V, A_{CSA} = 20 V/V, C_{SO} = 60pF; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		0.35	0.7	µs
		V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, C_{SO} = 60pF; VREF=4.5V-5.5V; k=1/2; Cboardroute=0pF-60pF		0.6	0.9	µs
BW	Bandwidth	A_{CSA} = 5 V/V, C_{LOAD} = 60-pF, small signal -3 dB	3	5	7	MHz
		A_{CSA} = 10 V/V, C_{LOAD} = 60-pF, small signal -3 dB	2.5	4.8	6.6	MHz
		A_{CSA} = 20 V/V, C_{LOAD} = 60-pF, small signal -3 dB	2	4	5.4	MHz
		A_{CSA} = 40 V/V, C_{LOAD} = 60-pF, small signal -3 dB	1.75	3	4.2	MHz
t_{SR}	Output slew rate	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, C_{LOAD} = 60-pF, low to high transition		14		V/µs
		V_{STEP} = 1.6 V, A_{CSA} = 10 V/V, C_{LOAD} = 60-pF, low to high transition		13		V/µs
		V_{STEP} = 1.6 V, A_{CSA} = 20 V/V, C_{LOAD} = 60-pF, low to high transition		13		V/µs
		V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, C_{LOAD} = 60-pF, low to high transition		6		V/µs
V_{SWING}	Output voltage range	V_{CSAREF} = 3	0.25		2.75	V
V_{SWING}	Output voltage range	V_{CSAREF} = 5.5	0.25		5.25	V
V_{SWING}	Output voltage range	V_{CSAREF} = 3 to 5.5 V	0.25		V_{CSAREF} - 0.25	V
V_{COM}	Common-mode input range		-0.15		0.15	V
V_{DIFF}	Differential-mode input range	Gain A_{CSA} = 5 V/V	-0.3		0.3	V
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = -40°C, G=5V/V	-2.6		2.6	mV
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = 25°C, G=5V/V	-2.6		2.6	mV
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = 150°C, G=5V/V	-2.6		2.6	mV
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND;G=5V/V	-2.6		2.6	mV
V_{OFF_DRIFT}	Input drift offset voltage	V_{SP} = V_{SN} = GND	-10	0		µV/°C
V_{BIAS}	Output voltage bias ratio	V_{SP} = V_{SN} = GND		0.5		
V_{BIAS_ACC}	Outpu voltage bias ratio accuracy		-1.2		1.8	%

ADVANCE INFORMATION

(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BIAS}	Input bias current	V_{SP} = V_{SN} = GND, V_{CSAREF} = 3V to 5.5V			100	µA
I_{BIAS_OFF}	Input bias current offset	I_{SP} – I_{SN}	-2.5		2.5	µA
CMRR	Common-mode rejection ratio	DC		80		dB
		20 kHz		60		dB
PSRR	Power-supply rejection ratio	PVDD to SOx, DC		100		dB
PSRR	Power-supply rejection ratio	PVDD to SOx, 20 kHz		63		dB
PSRR	Power-supply rejection ratio (CSAREF)	CSAREF to SOx, DC, Differential		85		dB
		CSAREF to SOx, 20 kHz, Differential		90		dB
PSRR	Power-supply rejection ratio (CSAREF)	CSAREF to SOx, 20 kHz, Single Ended		40		dB
I_{CSA_SUP}	Supply leakage current for CSA during GVDD unpowered	CSAREF, V_{CSAREF} = 3.V to 5.5V, GVDD = 0V, VDRAIN = 48V / 0V			1000	nA
I_{CSA_SUP}	Supply current for CSA	CSAREF, V_{CSAREF} = 3.V to 5.5V		4.5	6.5	mA
T_{CMREC}	Common mode recovery time			2	2.5	us
RIPPLE	SOx output ripple voltage	Peak to peak , CSAREF = 3 to 5.5V, SOx cap = 500pf, Input refered, SOx/ GAIN		850	1100	uV
C_{LOAD}	Maximum load capacitance			10		nF
PROTECTION CIRCUITS						
$V_{GVDD\_UV\_BST}$	GVDD undervoltage warning threshold rising	GVDD_UV_BST_LV = 1b	9.25	9.6	9.95	V
$V_{GVDD\_UV\_BST}$	GVDD undervoltage warning threshold falling	GVDD_UV_BST_LVL = 1b	9.1	9.45	9.8	V
$V_{GVDD\_UV\_BST}$	GVDD undervoltage warning threshold rising	GVDD_UV_BST_LVL = 0b	10.25	10.65	10.95	V
$V_{GVDD\_UV\_BST}$	GVDD undervoltage warning threshold falling	GVDD_UV_BST_LVL = 0b	10.1	10.45	10.8	V
V_{GVDD_UVH}	GVDD undervoltage fault threshold rising		7.2	7.55	7.9	V
V_{GVDD_UVH}	GVDD undervoltage fault threshold falling		7	7.35	7.7	V
V_{GVDD_UVL}	GVDD undervoltage lockout threshold		5.35	5.65	5.95	V
V_{GVDD_UVL}	GVDD undervoltage lockout threshold		5.25	5.55	5.85	V
V_{GVDD_OV}	GVDD overvoltage threshold rising		16.9	17.65	18.4	V
V_{GVDD_OV}	GVDD overvoltage threshold falling		16.5	17.25	18	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold rising	VDRAIN_UVH_LVL = 0b	18	19	20	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold falling	VDRAIN_UVH_LVL = 0b	17	18	19	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold rising	VDRAIN_UVH_LVL = 01b	20	21	22	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold falling	VDRAIN_UVH_LVL = 01b	19	20	21	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold rising	VDRAIN_UVH_LVL = 10b	22	23	24	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold falling	VDRAIN_UVH_LVL = 10b	21	22	23	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold rising	VDRAIN_UVH_LVL = 11b	24	25	26	V
V_{VDRAIN_UVH}	VDRAIN undervoltage fault threshold falling	VDRAIN_UVH_LVL = 11b	23	24	25	V

ADVANCE INFORMATION

(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDRAIN_UVL}	VDRAIN undervoltage threshold to disable TCP rising	VDRAIN_UVL_LVL = 0b	10.2	10.7	11.2	
V_{VDRAIN_UVL}	VDRAIN undervoltage threshold to disable TCP falling	VDRAIN_UVL_LVL = 0b	10	10.5	11	V
V_{VDRAIN_UVL}	VDRAIN undervoltage threshold to disable TCP rising	VDRAIN_UVL_LVL = 1b	5.15	5.65	5.95	V
V_{VDRAIN_UVL}	VDRAIN undervoltage threshold to disable TCP falling	VDRAIN_UVL_LVL = 1b	5.05	5.55	5.85	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold rising	VDRAIN_OV_LVL = 0b.	55.5	58	60.5	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold falling	VDRAIN_OV_LVL = 0b.	53.5	56	58.5	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold rising	VDRAIN_OV_LVL = 1b.	57.5	60	62.5	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold falling	VDRAIN_OV_LVL = 1b.	55.5	58	60.5	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold rising	VDRAIN_OV_LVL = 10b.	59.5	62	64.5	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold falling	VDRAIN_OV_LVL = 10b.	57.5	60	62.5	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold rising	VDRAIN_OV_LVL = 11b.	78	81.5	84	V
V_{VDRAIN_OV}	VDRAIN overvoltage fault threshold falling	VDRAIN_OV_LVL = 11b.	76	79.5	82	V
V_{VCP_UV}	VCP undervoltage fault threshold rising		6.7	7.6	8.4	V
V_{VCP_UV}	VCP undervoltage fault threshold falling		6.5	7.4	8.2	V
$V_{BST\_UV\_HI}$	Bootstrap undervoltage level (high) rising	8V < GVDD < 9V; PREDRV_BST_UVLO=1	4.5	5.15	5.8	V
$V_{BST\_UV\_HI}$	Bootstrap undervoltage level (high) falling	8V < GVDD < 9V; PREDRV_BST_UVLO=1	4.4	5.05	5.7	V
$V_{BST\_UV\_LO}$	Bootstrap undervoltage level (low) rising	GVDD > 9V; PREDRV_BST_UVLO=0	5.45	6.1	6.8	V
$V_{BST\_UV\_LO}$	Bootstrap undervoltage level (low) falling	GVDD > 9V; PREDRV_BST_UVLO=0	5.35	6	6.65	V
V_{DVDD_UV}	DVDD undervoltage fault threshold rising		2.6	2.75	2.9	V
V_{DVDD_UV}	DVDD undervoltage fault threshold falling		2.5	2.65	2.8	V
V_{DVDD_OV}	DVDD overvoltage fault threshold rising	DVDD_LDO_SEL = 0b (3.3V)	3.7	3.85	4.0	V
V_{DVDD_OV}	DVDD overvoltage fault threshold falling	DVDD_LDO_SEL = 0b (3.3V)	3.65	3.8	3.95	V
V_{DVDD_OV}	DVDD overvoltage fault threshold rising	DVDD_LDO_SEL = 1b (5V)	5.55	5.75	5.95	V
V_{DVDD_OV}	DVDD overvoltage fault threshold falling	DVDD_LDO_SEL = 1b (5V)	5.5	5.7	5.9	V
V_{VREF_UV}	VREF undervoltage fault threshold rising	VREF Rising	2.05	2.2	2.35	V
V_{VREF_UV}	VREF undervoltage fault threshold falling	VREF falling	1.85	2	2.15	V
TOTW	Overtemperature warning threshold rising		127	142	157	°C
TOTW	Overtemperature warning threshold falling		121	136	151	°C
TOTSD	Overtemperature shutdown threshold rising		161	176	191	°C
TOTSD	Overtemperature shutdown threshold falling		155	170	185	°C
VVDS_LVL0	VDS overcurrent fault level	VDS_LVL_x = 0000b	0.085	0.1	0.115	V
VVDS_LVL1	VDS overcurrent fault level	VDS_LVL_x = 0001b	0.135	0.15	0.165	V

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(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VVDS_LVL2	VDS overcurrent fault level	VDS_LVL_x = 0010b	0.185	0.2	0.215	V
VVDS_LVL3	VDS overcurrent fault level	VDS_LVL_x = 0011b	0.28	0.3	0.32	V
VVDS_LVL4	VDS overcurrent fault level	VDS_LVL_x = 0100b	0.38	0.4	0.42	V
VVDS_LVL5	VDS overcurrent fault level	VDS_LVL_x = 0101b	0.475	0.5	0.525	V
VVDS_LVL6	VDS overcurrent fault level	VDS_LVL_x = 0110b	0.57	0.6	0.63	V
VVDS_LVL7	VDS overcurrent fault level	VDS_LVL_x = 0111b	0.67	0.7	0.73	V
VVDS_LVL8	VDS overcurrent fault level	VDS_LVL_x = 1000b	0.76	0.8	0.84	V
VVDS_LVL9	VDS overcurrent fault level	VDS_LVL_x = 1001b	0.86	0.9	0.94	V
VVDS_LVL10	VDS overcurrent fault level	VDS_LVL_x = 1010b	0.95	1.0	1.05	V
VVDS_LVL11	VDS overcurrent fault level	VDS_LVL_x = 1011b	1.43	1.5	1.57	V
VVDS_LVL12	VDS overcurrent fault level	VDS_LVL_x = 1100b	1.9	2.0	2.1	V
VVGS_FLT	VGS fault threshold rising	Fault VGS monitor mode. VGS rising	0.6	1.2	1.7	V
VVGS_FLT	VGS fault threshold falling	Fault VGS monitor mode. VGS falling	0.5	1.1	1.6	V
RSHUNT_OCP						
V_RSHUNT_OCP	RSHUNT OCP threshold	RSHUNT_OCP_LVL=0	VREF*0.20		VREF*0.80	
V_RSHUNT_OCP	RSHUNT OCP threshold	RSHUNT_OCP_LVL=1	VREF*0.10		VREF*0.90	
RSHUNT_OCP_VAR	RSHUNT OCP threshold variation	RSHUNT_OCP_LVL=0,1, k=1/2, SN/SP Common mode =0V	-3.2		3.2	%
RSHUNT_OCP_VAR	RSHUNT OCP threshold variation	RSHUNT_OCP_LVL=0,1, k=1/2, SN/SP Common mode =-0.175V	-3.5		3.5	%
RSHUNT_OCP_VAR	RSHUNT OCP threshold variation	RSHUNT_OCP_LVL=0,1, k=1/2, SN/SP Common mode =0.7V	-3.8		3.8	%
RSHUNT_OCP_VAR	RSHUNT OCP threshold variation	RSHUNT_OCP_LVL=0,1, k=1/8, SN/SP Common mode =0V	-2		2	%
RSHUNT_OCP_VAR	RSHUNT OCP threshold variation	RSHUNT_OCP_LVL=0,1, k=1/8, SN/SP Common mode =-0.175V	-2		2	%
RSHUNT_OCP_VAR	RSHUNT OCP threshold variation	RSHUNT_OCP_LVL=0,1, k=1/8, SN/SP Common mode =0.7V	-2		2	%

ADVANCE INFORMATION

5.5 SPI Timing Requirements

V_{PVDD} = 5 to 15 V, over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{CLK}	SCLK minimum period		100			ns
t_{CLKH}	SCLK minimum high time		50			ns
t_{CLKL}	SCLK minimum low time		50			ns
t_{SU_SDI}	SDI input data setup time		15			ns
t_{H_SDI}	SDI input data hold time		25			ns
t_{D_SDO}	SDO output data delay time,CL = 20pF	SCLK high to SDO valid, C_L = 20 pF	0		50	ns
t_{SU_nSCS}	nSCS input setup time		25			ns
t_{H_nSCS}	nSCS input hold time		25			ns
t_{HI_nSCS}	nSCS minimum high time before active low		450			ns
t_{ACC_nSCS}	nSCS access time	nSCS low to SDO ready			50	ns
t_{DIS_nSCS}	nSCS disable time	nSCS high to SDO high impedance			50	ns

5.6 SPI Timing Diagrams

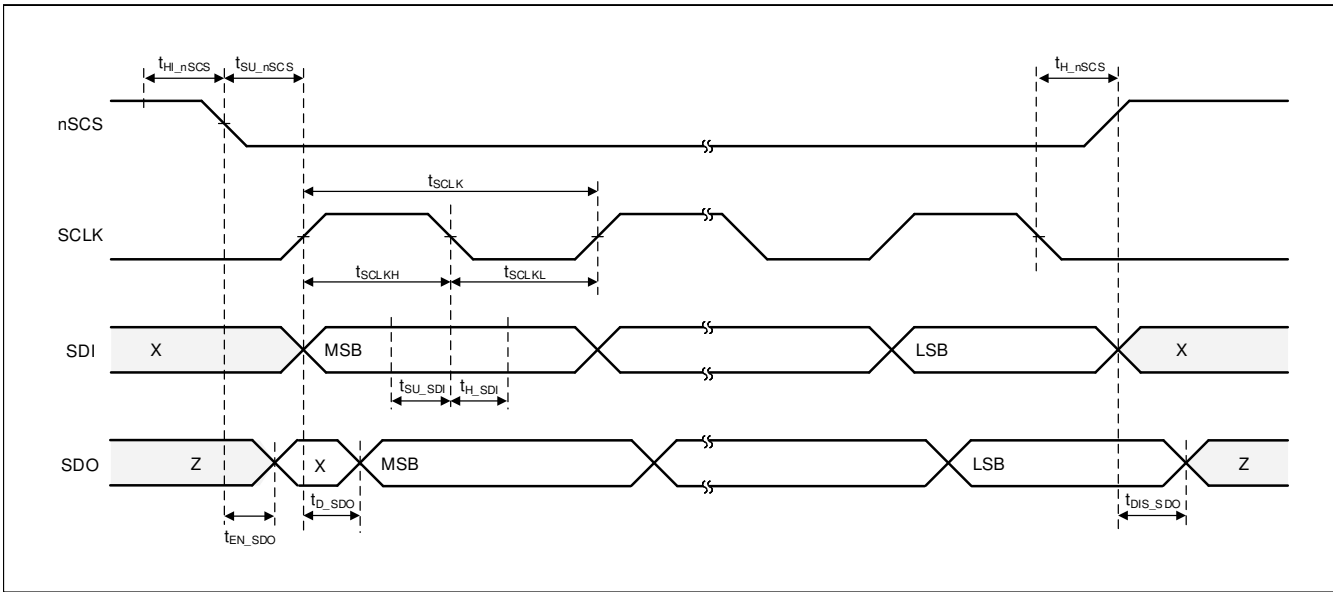

Figure 5-1. SPI Peripheral Mode Timing Diagram

ADVANCE INFORMATION

6 Detailed Description

6.1 Overview

The DRV8363-Q1 is an integrated 8V to 85V gate driver for three-phase motor drive applications. These devices decrease system component count, cost, and complexity by integrating three independent half-bridge gate drivers, a trickle charge pump, and a linear regulator for the supply of a low power microcontroller. The device also integrates up to three current shunt (or current sense) amplifiers. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1-A source, and 2A sink peak currents. A bootstrap capacitor generates the supply voltage of the high-side gate drive. The supply voltage of the low-side gate driver is supplied externally at a nominal 12V.

A Smart Gate Drive architecture provides the ability to dynamically adjust the strength of the gate drive output current which lets the gate driver control the VDS switching speed of the power MOSFET. This feature lets the user remove the external gate drive resistors and diodes, reducing the component count in the bill of materials (BOM), cost, and area of the printed circuit board (PCB). The architecture also uses an internal state machine to protect against short-circuit events in the gate driver, control the half-bridge dead time, and protect against dV/dt parasitic turn on of the external power MOSFET.

The DRV8363-Q1 integrates current sense amplifiers for monitoring current level through all the external half-bridges using a low-side shunt resistor. The gain setting of the current sense amplifier can be adjusted through SPI commands.

In addition to the high level of device integration, the DRV8363-Q1 provides a wide range of integrated protection features. These features include power supply undervoltage/overvoltage monitoring (GVDD UV/OV), drain supply undervoltage/overvoltage monitoring (VDRAIN UV/OV), VDS overcurrent monitoring, R_{SENSE} over current monitoring (SNS_OCP), and overtemperature monitoring/shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin.

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6.2 Functional Block Diagram

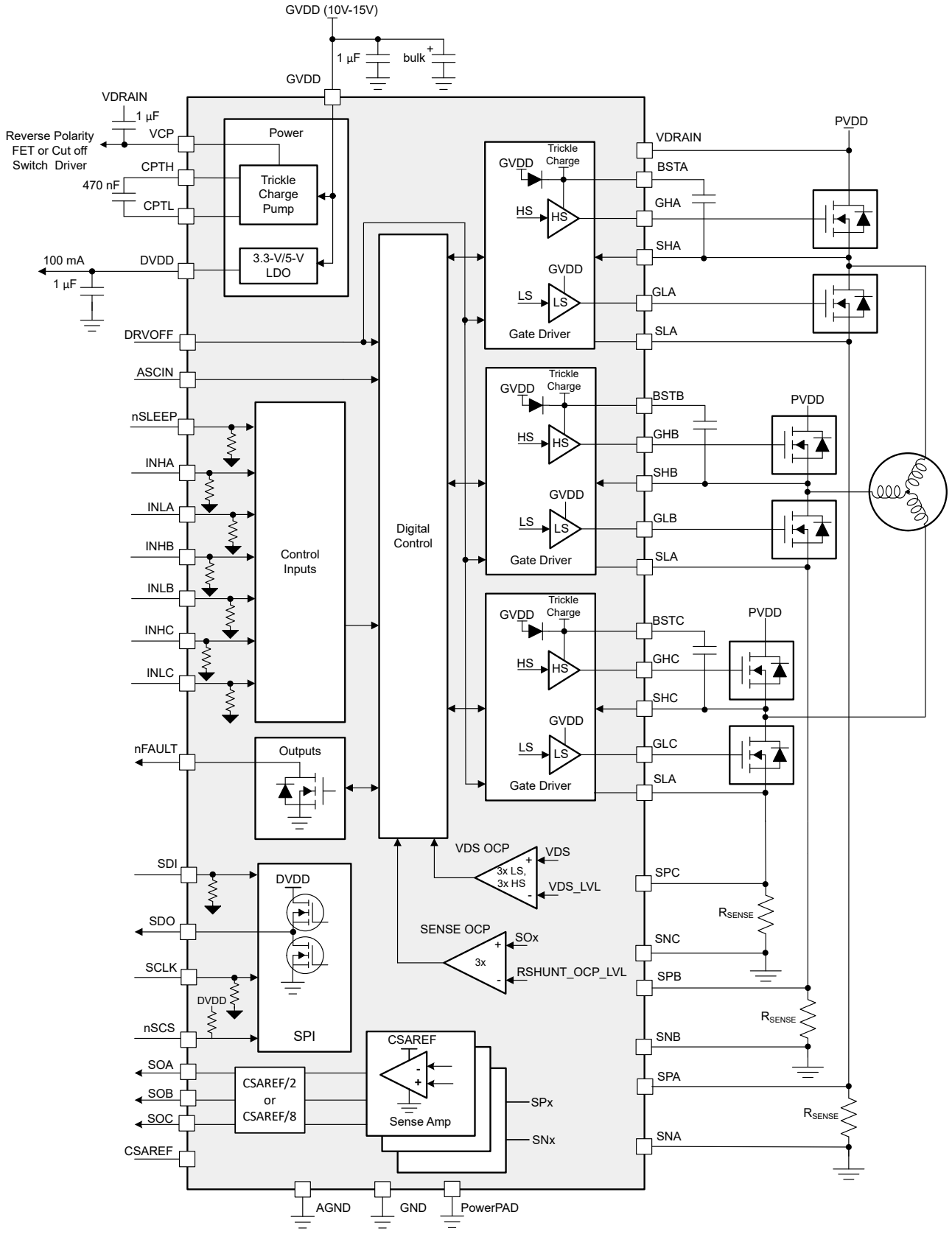

Figure 6-1. Block Diagram of DRV8363-Q1

6.3 Feature Description

6.3.1 Three BLDC Gate Drivers

The DRV8363-Q1 integrates three, half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The bootstrap circuit provides the correct gate bias voltage to the high-side MOSFET across a wide operating condition, and an integrated trickle charge pump supports 100% duty cycle operation. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

6.3.1.1 PWM Control Modes

The DRV8363-Q1 provides four different PWM control modes to support various commutation and control methods. PWM control mode is adjustable through PWM_MODE register bits.

6.3.1.1.1 6x PWM Mode

In 6x PWM mode, the corresponding INHx and INLx signals control the output state as listed in Table 6-1.

Table 6-1. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	Note
0	0	L	L	
0	1	L	H	
1	0	H	L	
1	1	L	L	Shoot through protection

6.3.1.1.2 3x PWM Mode with INLx enable control

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put both high-side and low-side gate drive outputs low. If the state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in Table 6-2.

Table 6-2. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx
0	X	L	L
1	0	H	L
1	1	L	H

6.3.1.1.3 1x PWM Mode

In 1x PWM mode, the device uses 6-step block commutation tables that are stored internally. This feature allows for a three-phase BLDC motor to be controlled using one PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to the digital outputs of the Hall effect sensor from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation).

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when Hall effect sensors are directly controlling the state of the INLA, INHB, and INLB inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when the INLC pin is pulled low. This brake is independent of the state of the other input pins. Tie the INLC pin high if this feature is not required.

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Table 6-3. Synchronous 1x PWM Mode (PWM1X_COM = 0b)

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS[1]						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

(1) *!PWM* is the inverse of the PWM signal.

Table 6-4. Asynchronous 1x PWM Mode (PWM1X_COM = 1b)

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

Figure 6-2 and Figure 6-3 show the different possible configurations in 1x PWM mode.

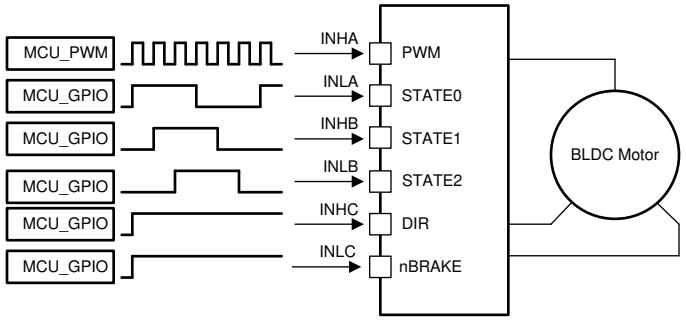

Figure 6-2. 1x PWM—Simple Controller

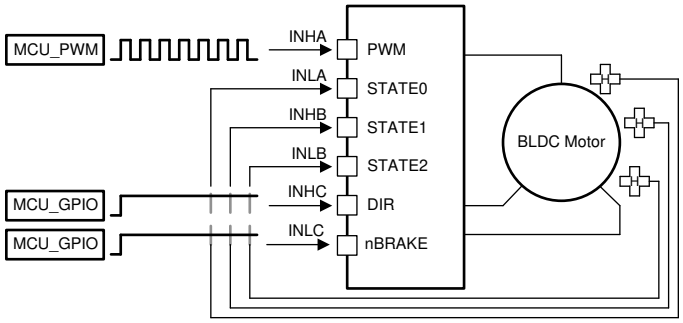

Figure 6-3. 1x PWM—Hall Effect Sensor

6.3.1.2 Gate Drive Architecture

The gate driver uses a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate drivers are supplied directly from the GVDD supply. For the high-side gate drivers, a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used on the BSTx pin. To support 100% duty cycle control, a trickle charge pump is integrated into the device. The trickle charge pump is connected to the BSTx node to prevent voltage drop due to the leakage currents of the driver and external MOSFET.

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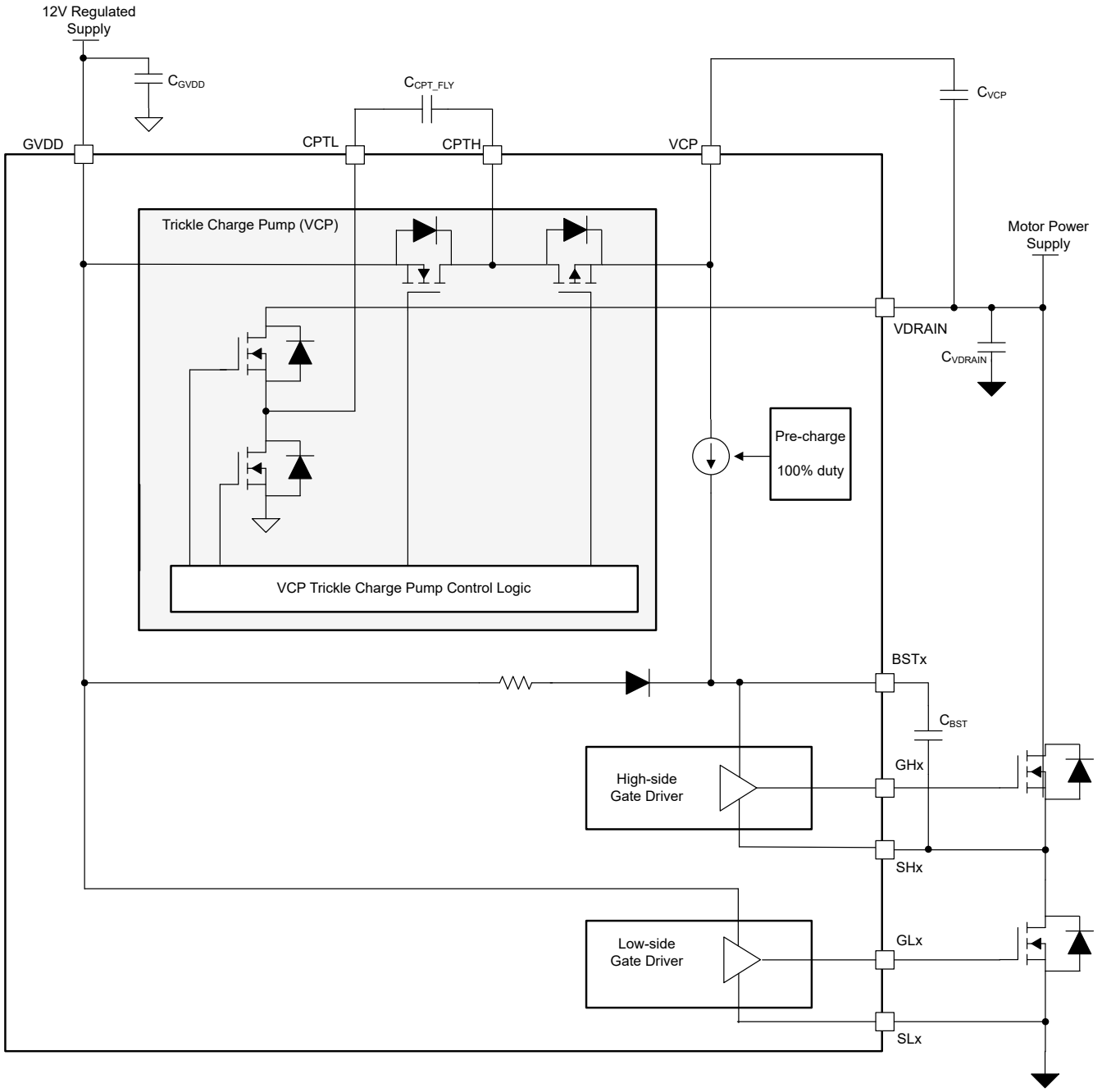

Figure 6-4. DRV8363-Q1 Gate Driver Power Supply Architecture

6.3.1.2.1 Bootstrap diode

The bootstrap diode is necessary to generate the high-side bias and is included in the driver device. The diode anode is connected to GVDD through an internal resistor and cathode connected to BSTx. With the C_{BST} capacitor connected to BSTx and the SHx pins, the C_{BST} capacitor charge is refreshed every switching cycle when SHx transitions to ground. The capacitor value C_{BST} is dependent on the gate charge of the high-side MOSFET and must be selected considering PWM control and voltage drop of the MOSFET gate. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

6.3.1.2.2 VCP Trickle Charge pump

The device has charge pump that provides current to C_{BST} bootstrap capacitor so that the bootstrap capacitor stays charged. This allows the gate driver to operate at 100% duty cycle. The charge pump also supports pre-charge of C_{BST} capacitor at power up.

In addition to the support of 100% PWM duty cycle operation, the VCP charge pump is designed to support an overdrive supply for external components. The supply voltage V_{VCP} is available on VCP pin and the voltage is regulated with respect to VDRAIN, where a capacitor is connected between VCP and VDRAIN pins. The VCP voltage can be used for an overdrive supply of external switch control circuits such as battery reverse protection switch, high-side switch, or motor phase isolation switches. While the VCP charge pump is designed to support these external loads, care must be taken to avoid exceeding the total current limit of the overdrive supply.

6.3.1.2.3 Gate Driver Output

The gate drivers use a Smart Gate Drive architecture to provide switching control of the external power MOSFETs, additional steps to protect the MOSFETs, and tradeoffs between efficiency and robustness. This architecture is implemented through two components called IDRIVE and TDRIVE. The IDRIVE gate drive current and TDRIVE gate drive time is initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times.

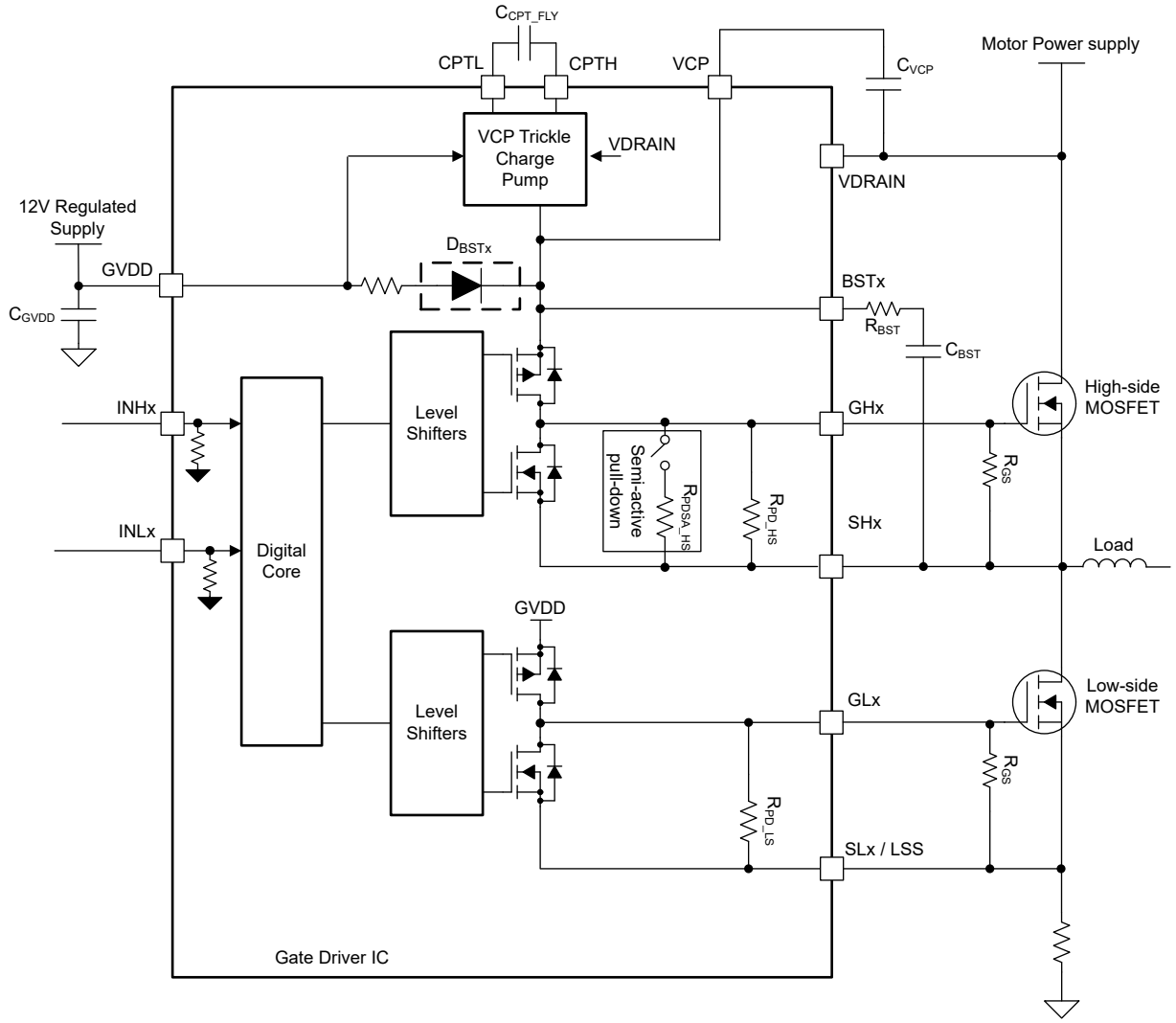

Figure 6-5. Gate Driver Architecture

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6.3.1.2.4 Passive and Semi-active pull-down resistor

Each gate driver has a passive pull down between the gate and source to keep the external MOSFETs turned off in unpowered conditions. In addition a semi-active pull down circuit of low-side gate driver reduces the gate impedance during SLEEP mode.

6.3.1.2.5 TDRIVE Gate Drive Timing Control

The device integrates TDRIVE gate drive timing control to prevent parasitic dV/dt gate turn on of external MOSFETs. Strong pull-down I_{STRONG} current is enabled on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown lasts for the TDRIVE duration. This feature helps to remove parasitic charge that couples into the MOSFET gate when the half-bridge switch-node voltage slews rapidly.

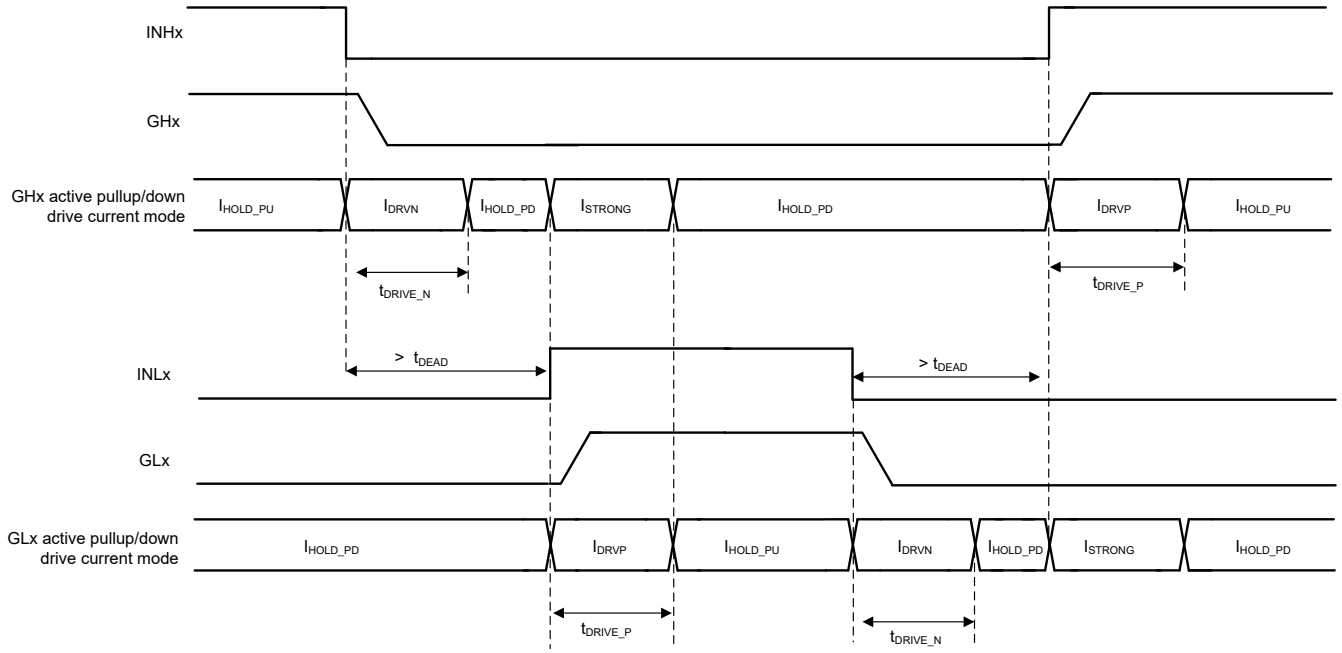

Figure 6-6. TDRIVE Gate Drive Timing Control (DEADT_MODE = 0b)

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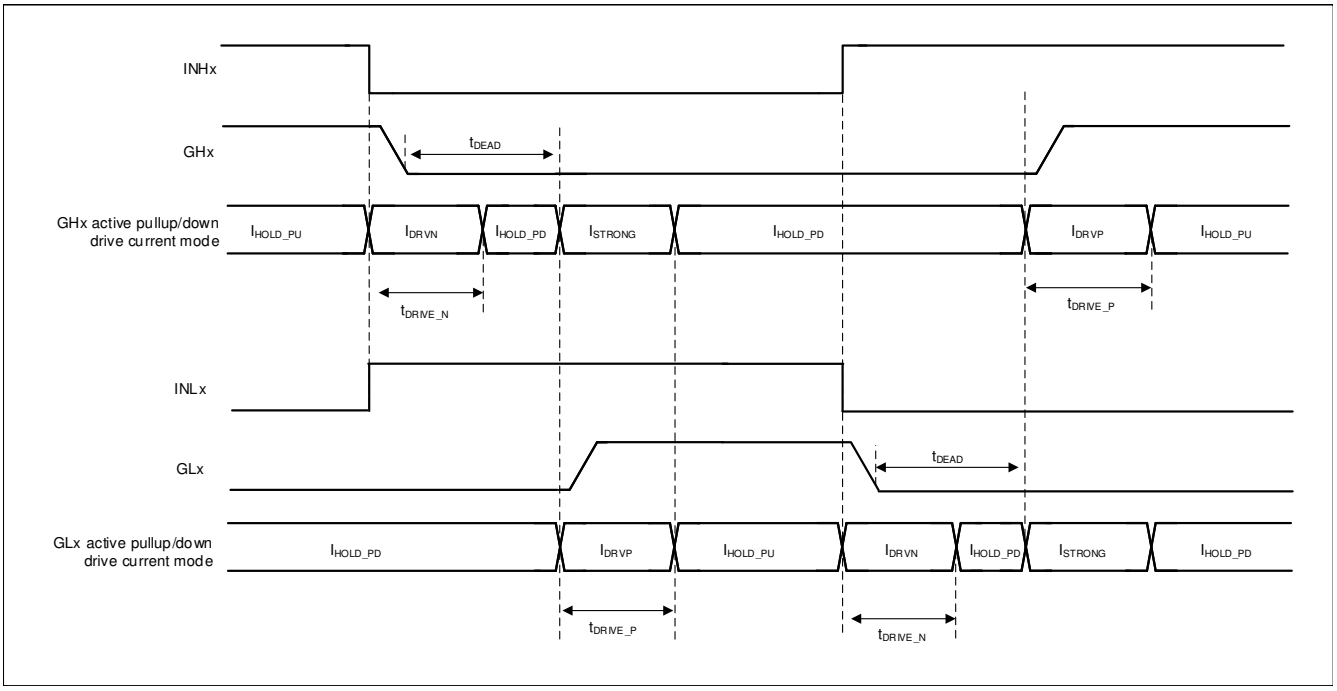

Figure 6-7. TDRIVE Gate Drive Timing Control (DEADT_MODE = 1b)

6.3.1.2.6 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the digital propagation delay, and the delay through the analog gate drivers.

To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

6.3.1.2.7 Deadtime and Cross-Conduction Prevention

In 6xPWM mode of DRV8363-Q1, high-side INHx and low-side INLx inputs operate independently, with an exception to prevent cross conduction when the high and low side of the same half-bridge are turned ON at same time. The device pulls high- and low- side gate outputs low to prevent shoot through condition of power stage and a fault STP_FLT is reported when high- and low-side inputs are logic high at the same time.

In 6xPWM mode, if SPI register bit DEADT_MODE is 0b and DEADT_MODE_6X is 00b, the device monitors INHx and INLx and inserts dead time if the period of INHx=INLx=low is shorter than t_{DEAD}. Other than 6xPWM mode, dead time is always inserted regardless of the configuration.

Note

If PWM_MODE is set to 001b - 101b, the STP_MODE bit shall be set to 1b to avoid a false flag of STP_FLT. The SPI register bit STP_MODE = 0b can be used only for PWM_MODE = 000b (6xPWM mode).

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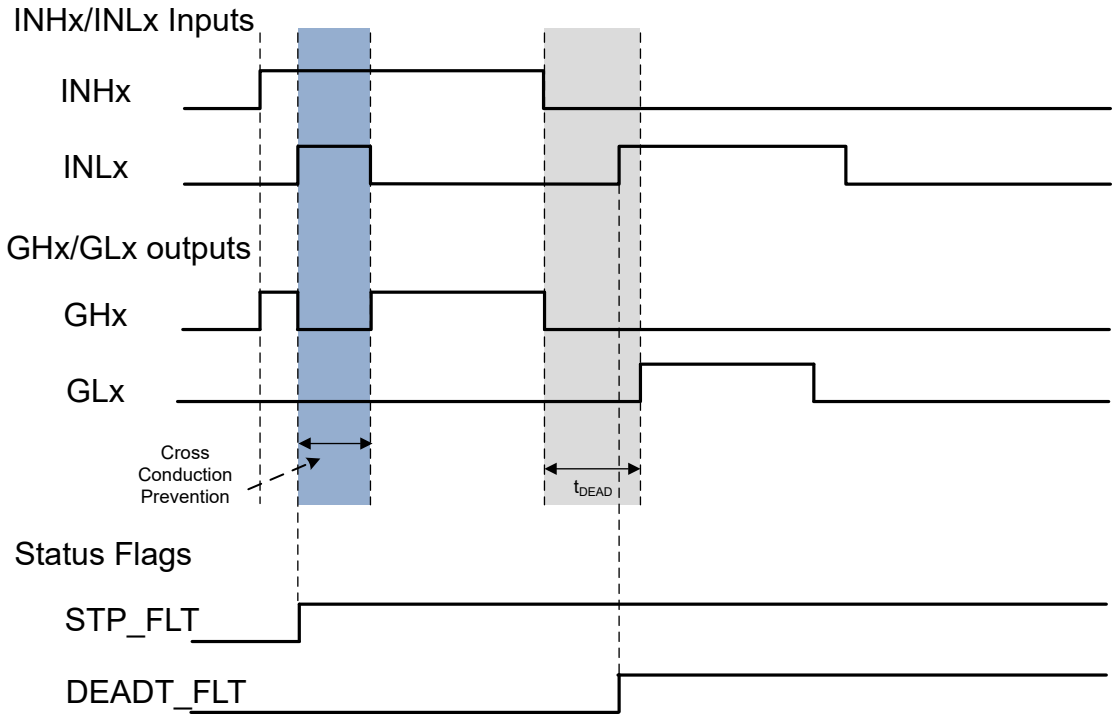

Figure 6-8. Cross Conduction Prevention and Dead time Insertion

6.3.2 DVDD Linear Voltage Regulator

A 100mA output linear regulator is integrated into the device and is available for use by external circuitry. The LDO can be configured for 3.3V or 5V output. This regulator can provide the supply voltage for a low-power MCU or other circuitry supporting low current. The output of the DVDD regulator is bypassed near the DVDD pin with a 1µF ceramic capacitor. TI recommends to use an X5R or X7R capacitor rated for 16V or greater to maintain sufficient effective capacitance. The ground return from the capacitor is routed back to the adjacent GND ground pin.

The output voltage of LDO can be selected through LDO_SEL register bit.

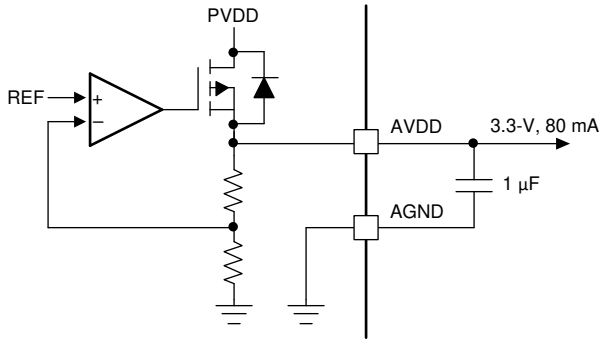

Figure 6-9. DVDD Linear Regulator Block Diagram

The power is dissipated in the device by the DVDD linear regulator. P = (V_{GVDD}- V_{DVDD}) x I_{DVDD}

For example, at a V_{GVDD} of 12V, drawing 20mA out of DVDD results in power dissipation as shown in Equation 1.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (1)$$

6.3.3 Low-Side Current Sense Amplifiers

The DRV8363-Q1 devices integrate high-performance low-side current sense amplifier for current measurements using low-side shunt resistors. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. The current sense amplifiers feature nine configurable gain settings between 5 and 40 V/V, which can be configured through SPI commands. The CSA output is referenced to the external voltage reference pin (VREF). The CSA output offset can be configured between 1/2 xVREF or 1/8 xVREF to support bidirectional or unidirectional current sensing as needed.

Note

By default, CSA output is disabled. CSA output can be enabled in SPI register IC_CTRL2.

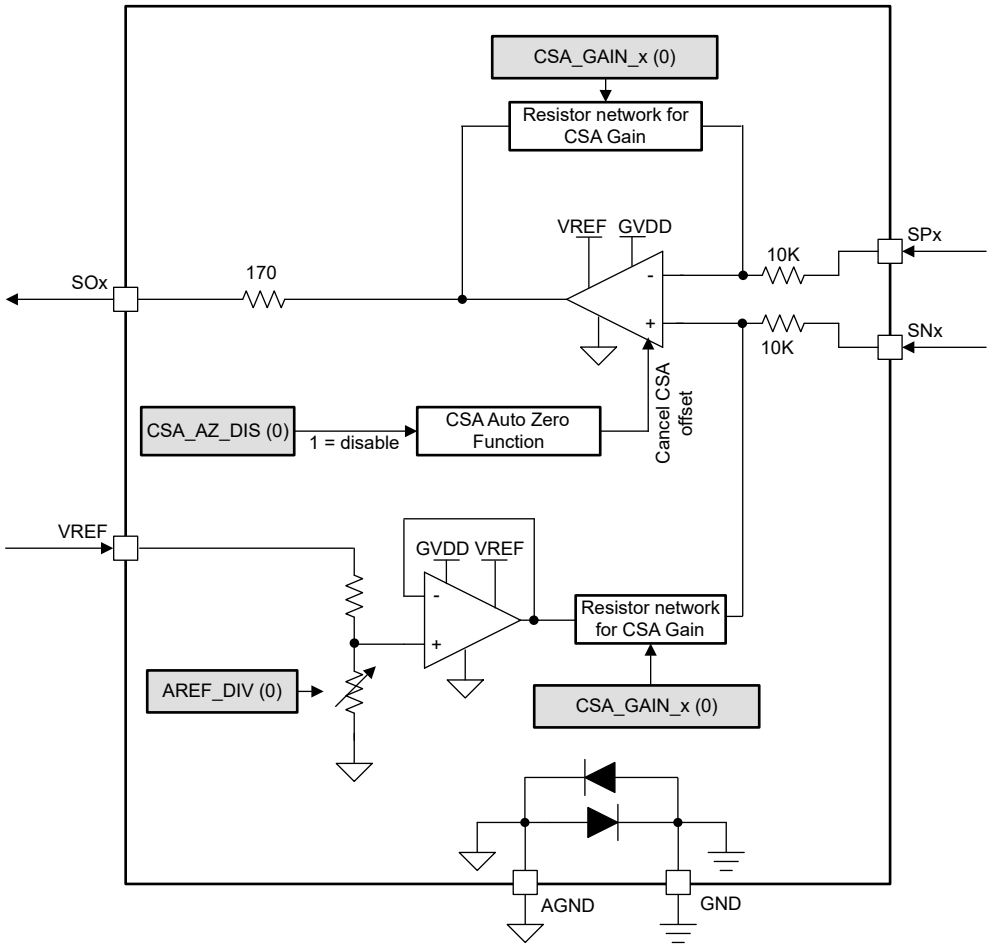

Figure 6-10. Current-Sense Amplifier Diagram

6.3.3.1 Unidirectional Current Sense Operation

The DRV8363-Q1 internally generates a common mode voltage of 1/8 x VREF to obtain maximum resolution for current measurement. The current sense amplifier operates in a unidirectional mode and the SO pin outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by the gain setting (G_{CSA}).

Use Equation 2 to calculate the current through the shunt resistor.

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$$I = \frac{V_{SOx} - V_{VREF}/8}{G_{CSA} \times R_{SENSE}} \quad (2)$$

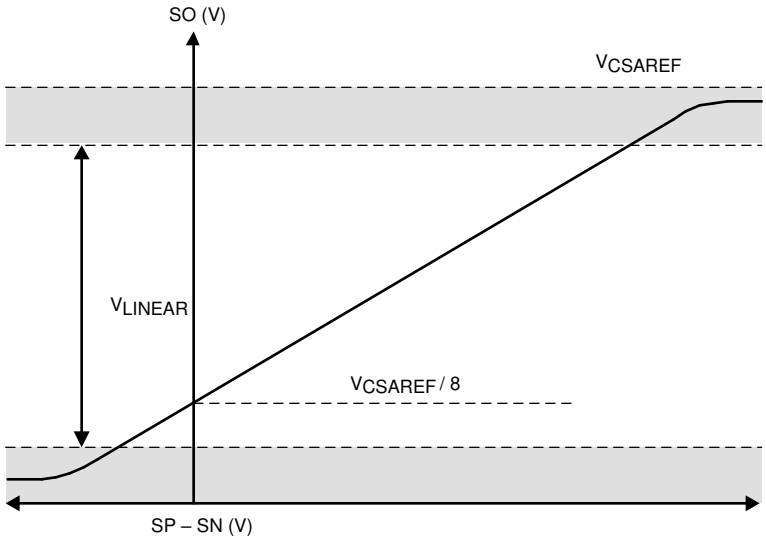

Figure 6-11. Unidirectional Current-Sense Output

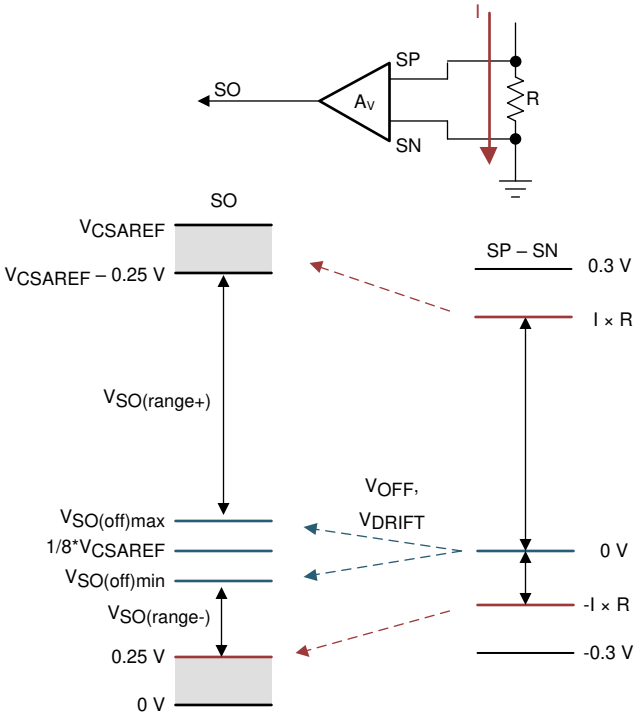

Figure 6-12. Unidirectional Current-Sense Regions

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6.3.3.2 Bidirectional Current Sense Operation

In this mode, DRV8363-Q1 internally generates a common mode voltage of ½ x VREF to enable bidirectional current measurement. The current sense amplifier operates in a bidirectional mode and the SO pin outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by the gain setting (G_{CSA}).

Use Equation 3 to calculate the current through the shunt resistor (AREF_DIV = VREF / 2 case) .

$$I = \frac{V_{SOx} - \frac{V_{VREF}}{2}}{G_{CSA} \times R_{SENSE}} \quad (3)$$

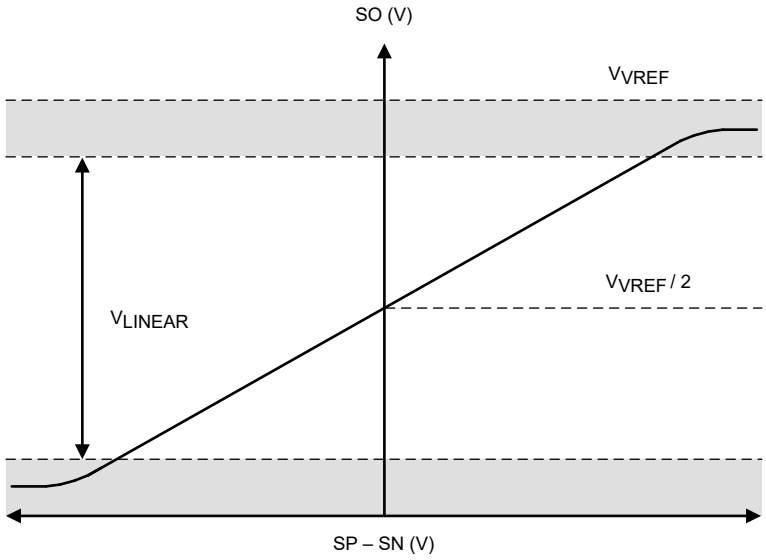

Figure 6-13. Bidirectional Current Sense Output

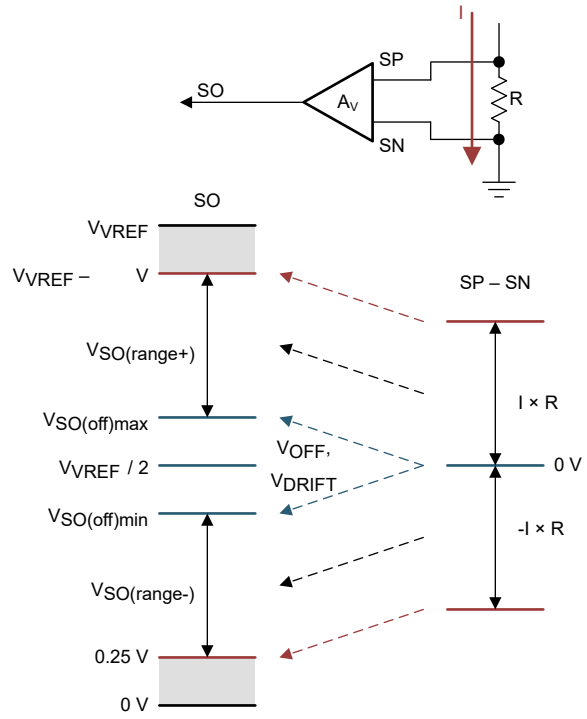

Figure 6-14. Bidirectional Current Sense Regions

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6.3.4 Gate Driver Shutdown

If a fault condition is detected or DRVOFF pin is driven by system, the device takes an action of gate driver shutdown. The high-side and low-side gate driver outputs are pulled down to turn off external MOSFETs.

6.3.4.1 DRVOFF Gate Driver Shutdown

When DRVOFF is driven high, the gate driver goes into shutdown mode, overriding signals on inputs pins INHx and INLx. DRVOFF bypasses the internal digital logic and is connected directly to the predriver. This pin provides a mechanism for externally monitored faults to disable the gate driver directly bypassing the external controller. When the DRVOFF pin is driven high, the device disables the gate driver and triggers the shutdown sequence.

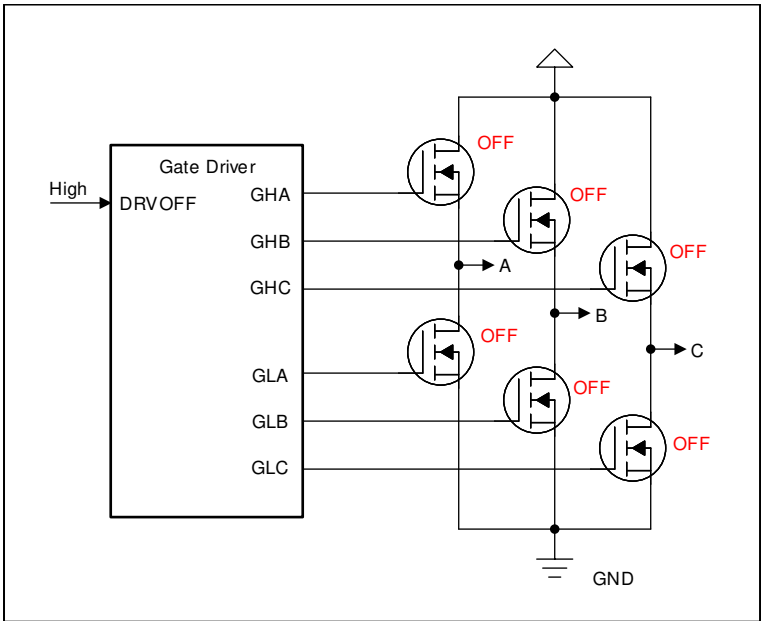

Figure 6-15. DRVOFF Gate Driver Output State

6.3.4.2 Gate Driver Shutdown Timing Sequence

The device initiates gate driver shutdown sequence as shown in figure. The shutdown drive current can be programmed with SPI register IDRVN_SD. The gate driver uses I_{DRVN_SDD} for t_{DRVN_SDD} time to discharge gate of MOSFET. The shutdown current changes to I_{DRVN_SD} current and is hold until end of t_{DRVN_SD} time. After completion of shutdown sequence, gate driver outputs are in semi-active pull-down mode.

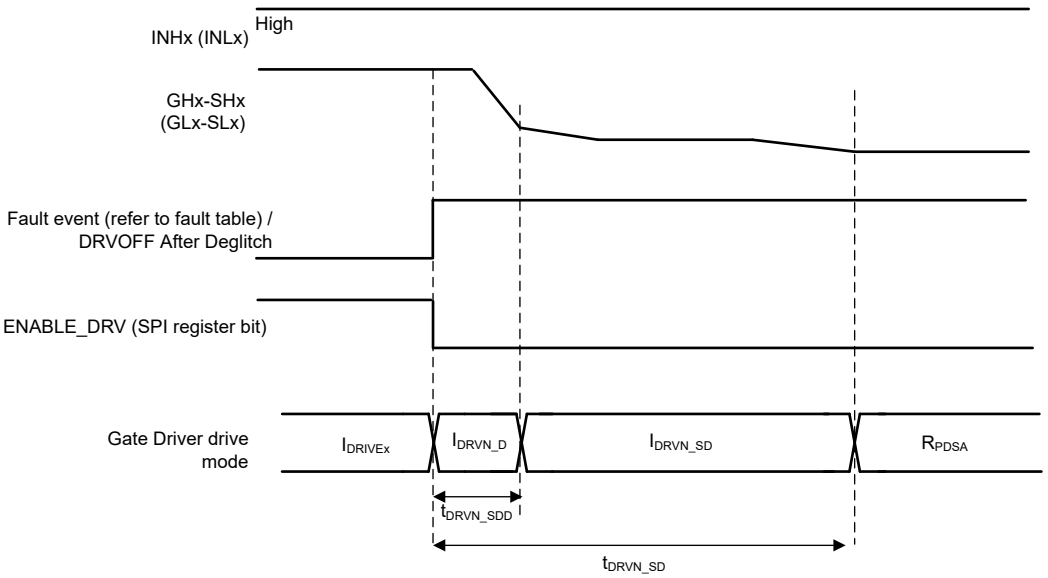

Figure 6-16. Gate Drive Shutdown Sequence

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6.3.5 Gate Driver Protective Circuits

The DRV832x family of devices is protected against PVDD undervoltage and overvoltage, AVDD POR, Bootstrap undervoltage, GVDD undervoltage, MOSFET V_{DS} and V_{SENSE}overcurrent events.

6.3.5.1 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold voltage for longer than the $t_{GVDD\_UV\_DG}$ time, the device detects a GVDD undervoltage event. After detecting the GVDD_UV undervoltage event, the gate driver disabled, charge pump disabled and nFAULT pin is driven low. After GVDD_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.5.2 GVDD Overvoltage Fault (GVDD_OV)

If at any time the power supply voltage on the GVDD pin exceeds the V_{GVDD_OV} threshold for longer than the $t_{GVDD\_OV\_DG}$ time, the DRV8363-Q1 detects a GVDD overvoltage event. After detecting the overvoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After GVDD_OV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.5.3 VDRAIN Undervoltage Fault (VDRAIN_UV)

If at any time the supply voltage on the VDRAIN pins falls below the V_{DRAIN_UV} threshold for longer than the $t_{vdrain\_uv\_dg}$ time, the DRV8363-Q1 detects a VDRAIN undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After the VDARIN_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.5.4 VDRAIN Overvoltage Fault (VDRAIN_OV)

If at any time the power supply voltage on the VDRAIN pin exceeds the V_{DRFAIN_OV} threshold for longer than the $t_{VDRAIN\_OV\_DG}$ time, the DRV8363-Q1 detects a VDRAIN overvoltage event. After detecting the overvoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After the VDRAIN_OV condition is cleared, the fault state remains latched and can be cleared through an SPI command. The VDRAIN_OV threshold can be adjusted based on expected supply range using the VDRAIN_OV_LVL register field.

6.3.5.5 VCP Undervoltage Fault (CP_OV)

If at any time the voltage between the VCP and VDRAIN pins falls below the V_{CP_UV} threshold for longer than the $t_{CP\_UV\_DG}$ time, the DRV8363-Q1 detects a VCP undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After the VCP_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.5.6 BST Undervoltage Lockout (BST_UV)

If at any time the voltage across BTSx and SHx pins falls lower than the V_{BST_UV} threshold voltage for longer than the $t_{BST\_UV\_DG}$ time, the device detects a BST undervoltage event. After detecting the BST_UV undervoltage event, the gate driver disabled and nFAULT pin is driven low. After BST_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command

6.3.5.7 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

The device has adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. The high-side VDS monitors measure between the VDRAIN and SHx pins and the low-side VDS monitors measure between the SHx and SLx pins. If the voltage across external MOSFET exceeds the V_{DS_LVL} threshold for longer than the t_{DS_DG} deglitch time, a VDS_OCP event is recognized. After detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. VDS level and deglitch time are programmable.

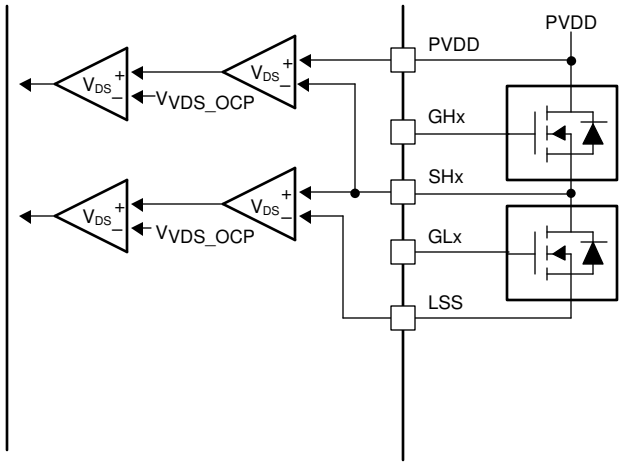

Figure 6-17. DRV8363-Q1 V_{DS} Monitors

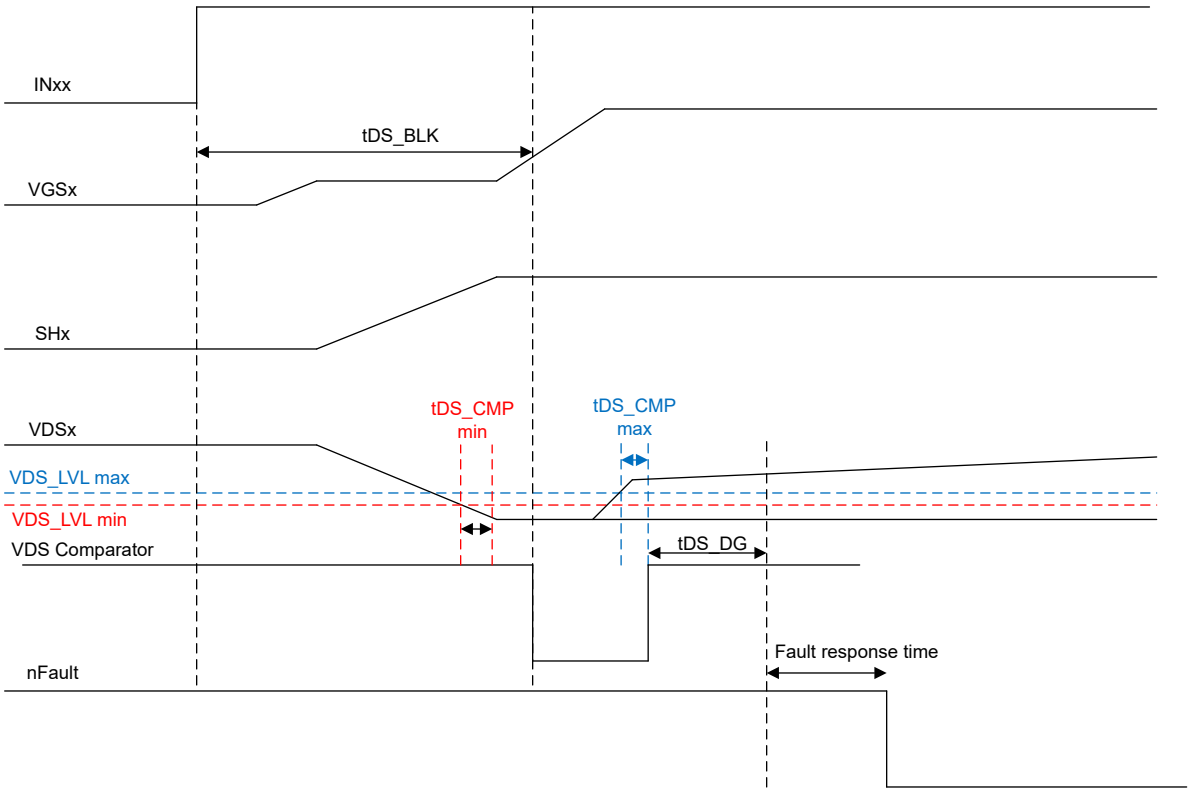

Figure 6-18. DRV8363-Q1 V_{DS} Monitor Timing

6.3.5.8 MOSFET VGS Monitoring Protection

The DRV8363-Q1 utilizes integrated gate to source voltage (VGS) monitors to monitor the state of the external MOSFETs. When the output state of the MOSFETs is commanded OFF (INxx = low), the monitor verifies that the output turns off and stays off. If at any point the VGS voltage exceeds the VGS threshold for a duration longer than tvgs_dg, the nFAULT pin is driven low and the VGS_XX flag is set for the corresponding output channel. When the output state of the MOSFETs is commanded ON (INxx = high), the monitor verifies that the output turns on. If at any point the VGS drops below the VGS threshold for a duration longer than tvgs_dg, the nFAULT pin is driven low and the VGS_XX flag is set for the corresponding output channel. The VGS monitor blanking time is shared with the VDS monitor can be adjusted through the VDS_VGS_BLK register field. TI recommends to set this value based on the expected switching time for the external MOSFETs. The VGS monitor deglitch time

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can be adjusted through the VGS_DEG register field. The deglitch timer does not start until after the blanking time has elapsed following a rising/falling PWM signal. TI recommends to set this value based on the system noise level and acceptable fault tolerance timing.

6.3.5.9 V_{SENSE} Overcurrent Protection (SEN_OCP)

Overcurrent is also monitored by sensing the voltage drop across the external current sense resistor between SPx and SNx pin. If at any time the difference voltage of SPx-SNx exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized. After detecting the SEN_OCP over current event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The V_{SENSE} threshold and deglitch time are programmable. After SEN_OCP condition is cleared, the fault state remains latched and can be cleared through SPI command.

6.3.5.10 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), OTSD event is recognized. After detecting the OTSD overtemperature event, if OTSD_MODE is Fault mode, all of the gate driver outputs are driven low to disable the external MOSFETs, charge pump and current sense are disabled, and nFAULT pin is driven low. After OTSD condition is cleared, the fault state remains latched and can be cleared through an SPI command (CLR_FLT). The OTSD_MODE is Fault mode by default. If OTSD condition is detected during device power up, nFAULT stays low and charge pump and current sense remain disabled until OTSD condition is removed and SPI command (CLR_FLT) is sent by MCU.

6.3.5.11 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. After the die temperature falls lower than the hysteresis point of the thermal warning, the OTW bit remains latched and can be cleared through an SPI command CLR_FLT. If OTW bit is 1b, nFAULT stays high when WARN_MODE bit 1b.

6.3.5.12 OTP CRC

After each power up, the device performs an OTP CRC check. If the calculated CRC8 checksum does not match the CRC8 checksum stored in the internal OTP memory, the OTP_CRC failed flag is set.

6.3.5.13 SPI Watchdog Timer

The device integrates a programmable window-type SPI watchdog timer to verify that the external controller is operating. The SPI watchdog timer can be enabled by writing a 1 to WDT_EN SPI register bit. The watchdog timer is disabled by default. When the watchdog timer is enabled, an internal timer starts to count up. A valid SPI access resets the timer. This valid SPI access must be issued between the lower window time and the upper window time. If a watchdog timer fault is detected, nFAULT pin is asserted low.

6.3.5.14 Phase Diagnostic

The device integrates a current source and a switch between VDRAIN and SHx device pins and between SHx device pin and the device ground for each channel. The switches can be individually enabled and disabled via SPI register bits PH_DIAG_Hx and PH_DIAG_Lx. If PH_DIAG_Hx is 1b, the source current I_{PHD_SRC} of SHx pin is enabled. If PH_DIAG_Lx is 1b, the sink current I_{PHD_SNK} of SHx pin is enabled. When any of PHDEN_Hx and PHDEN_Lx register bits are set to 1, the VDS overcurrent detection flags, VDS_Hx and VDS_Lx, change from the fault detection flag to the status flag of VDS comparators. The combination of the integrated current sources and VDS status flags can be used for the phase diagnostics such as an open fault detection of motor load, without activating external MOSFETs.

The DRV8363-Q1 also features automatic open load and MOSFET short detection sequences. To run the automatic open load detection, set the OPEN_DET_EN bit to 1b. To run the automatic MOSFET short detection sequence, set the SHORT_DET_EN bit to 1b. Please note that only one automatic sequence can be run at a time. The results of the sequence is reported in the IC_STAT3 register.

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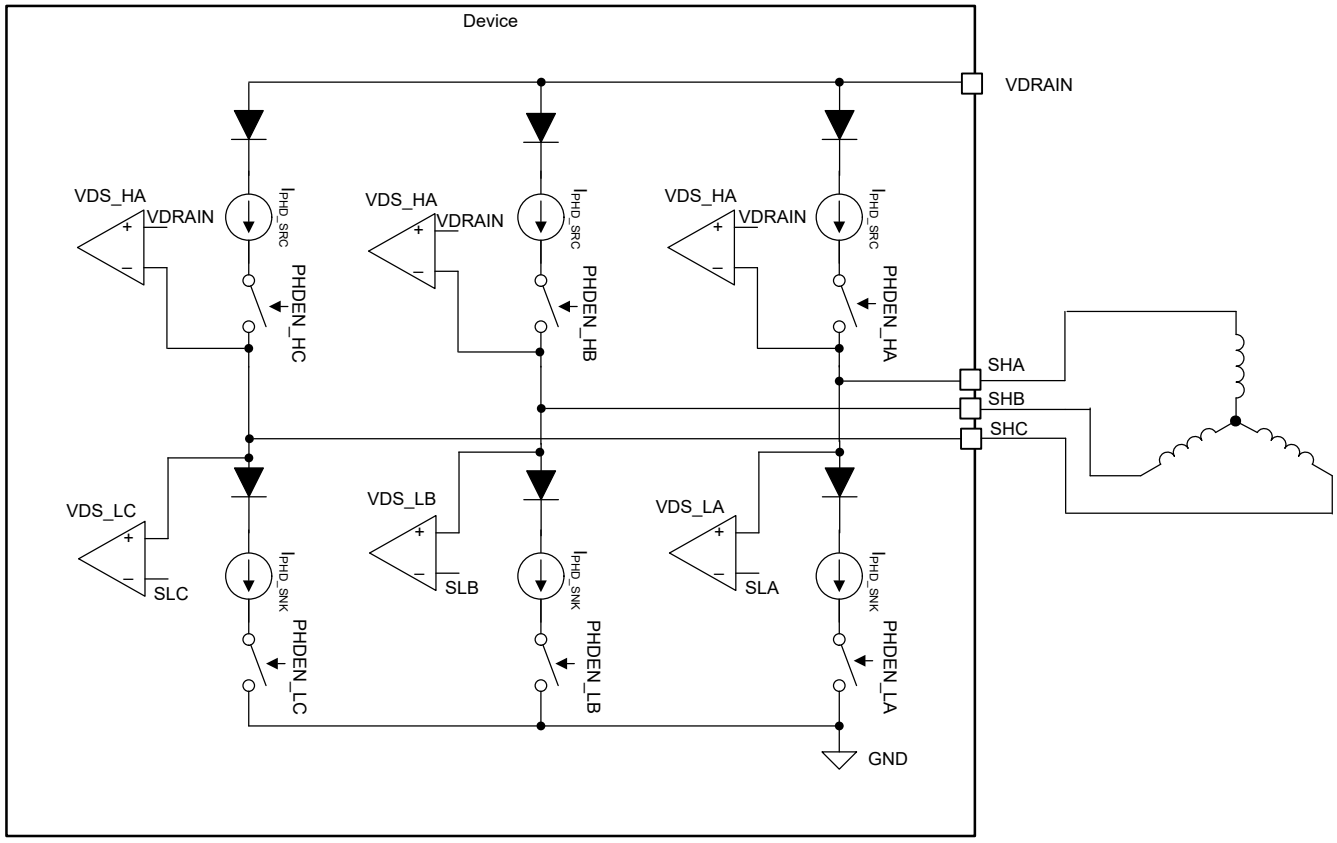

Figure 6-19. Phase Diagnostic

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6.4 Fault Detection and Response Summary Table (Fault Table)

Table 6-5. Fault Detection and Response Summary

NAME	SPI FLAG BIT	CONDITION	MODE	DIGITAL CORE	GATE DRIVERS	CHARGE PUMP	CURRENT SENSE	RESPONSE
GVDD Undervoltage Lockout	N/A	GVDD < GVDD_UVLO	N/A	Reset	Disabled	Disabled	Disabled	Gate drive shutdown, device shutdown, nFAULT
GVDD Undervoltage Warning	GVDD_UVH	GVDD < GVDD_UVH	GVDD_UVH_MODE = 0 (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			GVDD_UVH_MODE = 1 (Fault)	Active	Disabled (Weak Pulldown)	Active	Active	Gate drive shutdown, SPI Report, nFAULT
GVDD Undervoltage BST Warning	GVDD_UV_BST	GVDD < GVDD_UV_BST	GVDD_UV_BST_MODE = 00b (RT Warning)	Active	Active	Active	Active	SPI Report (Unlatched), nFAULT
			GVDD_UV_BST_MODE = 01b (Fault)	Active	Active	Active	Active	SPI Report, VCP_UV disabled, BST_UV_LVL forced to 1b, nFAULT
			GVDD_UV_BST_MODE = 10b (RT Fault)	Active	Active	Active	Active	SPI Report (Unlatched), VCPI_UV disabled, BST_UV_LVL forced to 1b, nFAULT
			GVDD_UV_BST_MODE = 11b (Disabled)	Active	Active	Active	Active	N/A
GVDD overvoltage	GVDD_OV	GVDD > GVDD_OV	GVDD_OV_MODE = 0b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			GVDD_OV_MODE = 1b (Fault)	Active	Disabled (Standard shutdown)	Disabled	Active	SPI Report, Gate drive shutdown, nFAULT

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Table 6-5. Fault Detection and Response Summary (continued)

NAME	SPI FLAG BIT	CONDITION	MODE	DIGITAL CORE	GATE DRIVERS	CHARGE PUMP	CURRENT SENSE	RESPONSE
VDRAIN Undervoltage Low Threshold	VDRAIN_UVL	VDRAIN < VDRAIN_UVL	VDRAIN_UVL_MODE = 00b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			VDRAIN_UVL_MODE = 01b (Warning RT)	Active	Active	Active	Active	SPI Report (Unlatched), nFAULT
			VDRAIN_UVL_MODE = 10b (Fault)	Active	Disabled (Standard shutdown)	Disabled	Active	SPI Report, Gate drive shutdown, nFAULT
			VDRAIN_UVL_MODE = 11b (Disabled)	Active	Active	Active	Active	N/A
VDRAIN Undervoltage High Threshold	VDRAIN_UVH	VDRAIN < VDRAIN_UVH	VDRAIN_UVH_MODE = 00b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			VDRAIN_UVH_MODE = 01b (Warning RT)	Active	Active	Active	Active	SPI Report (Unlatched), nFAULT
			VDRAIN_UVH_MODE = 10b (Fault)	Active	Disabled (Standard shutdown)	Active	Active	SPI Report, Gate drive shutdown, nFAULT
			VDRAIN_UVH_MODE = 11b (Disabled)	Active	Active	Active	Active	N/A
VDRAIN Overvoltage	VDRAIN_OV	VDRAIN > VDRAIN_OV	VDRAIN_OV_MODE = 00b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			VDRAIN_OV_MODE = 01b (Fault)	Active	Disabled (Standard shutdown)	Active	Active	SPI Report, Gate drive shutdown, nFAULT
			VDRAIN_OV_MODE = 10b (ASC Latched)	Active	Active (ASC enabled)	Active	Active	SPI Report, nFAULT
			VDRAIN_OV_MODE = 11b (ASC RT)	Active	Active (ASC enabled)	Active	Active	SPI Report, nFAULT

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Table 6-5. Fault Detection and Response Summary (continued)

NAME	SPI FLAG BIT	CONDITION	MODE	DIGITAL CORE	GATE DRIVERS	CHARGE PUMP	CURRENT SENSE	RESPONSE
DVDD Overvoltage	DVDD_OV	DVDD > DVDD_OV	DVDD_MODE = 0b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			DVDD_MODE = 1b (Fault)	Active	Disabled (Standard shutdown)	Disabled	Active	SPI Report, Gate drive shutdown, nFAULT
Overtemperature Warning	OTW	Internal temperature > OTW	N/A	Active	Active	Active	Active	SPI Report, nFAULT
Overtemperature Shutdown	OTSD	Internal temperature > OTSD	OTSD_MODE = 0b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			OTSD_MODE = 1b (Fault)	Disabled	Disabled (Standard shutdown)	Disabled	Disabled	SPI Report, Gate drive shutdown, nFAULT
Overtemperature Shutdown, Trickle Charge Pump	OTSD_TCP	Internal charge pump temperature > OTSD	N/A	Active	Active	Disabled	Active	SPI Report, nFAULT
VCP Undervoltage	VCP_UV	VCP < VCP_UV	VCP_UV_MODE = 00b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			VCP_UV_MODE = 01b (Fault)	Active	Disabled (Standard shutdown)	Active	Active	SPI Report, Gate drive shutdown, nFAULT
			VCP_UV_MODE = 10b (Fault, TCP Shutdown)	Active	Disabled (Standard shutdown)	Disabled	Active	SPI Report, Gate drive shutdown, nFAULT
			VCP_UV_MODE = 11b (Disabled)	Active	Active	Active	Active	N/A

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Table 6-5. Fault Detection and Response Summary (continued)

NAME	SPI FLAG BIT	CONDITION	MODE	DIGITAL CORE	GATE DRIVERS	CHARGE PUMP	CURRENT SENSE	RESPONSE
Bootstrap Undervoltage	BST_x_UV	BSTx < BST_UV	BST_UV_MODE = 000b, 110b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			BST_UV_MODE = 001b (Fault RT, Active Pulldown)	Active	HS Off (Active Pulldown), LS Active	Active	Active	SPI Report, Gate drive shutdown, nFAULT
			BST_UV_MODE = 010b (Fault RT, Weak Pulldown)	Active	HS Off (Weak Pulldown), LS Active	Active	Active	SPI Report, Gate drive shutdown, nFAULT
			BST_UV_MODE = 011b (Fault, Active Pulldown)	Active	HS Off (Active Pulldown), LS Active	Active	Active	SPI Report, Gate drive shutdown, nFAULT
			BST_UV_MODE = 100b (Fault, Weak Pulldown)	Active	HS Off (Weak Pulldown), LS Active	Active	Active	SPI Report, Gate drive shutdown, nFAULT
			BST_UV_MODE = 101b (Fault, Weak Pulldown, TCP switch off)	Active	HS Off (Weak Pulldown), LS Active	Disabled	Active	SPI Report, Gate drive shutdown, nFAULT
			BST_UV_MODE = 111b (Disabled)	Active	Active	Active	Active	N/A
VREF Undervoltage	VREF_UV	VREF < VREF_UV	N/A	Active	Active	Active	Disabled	SPI Report, nFAULT
VDS OCP	VDS_xx	VDS > VDS_LVL	VDS_OCP_MODE = 0b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			VDS_OCP_MODE = 1b (Fault)	Active	Disabled (Soft shutdown)	Active	Active	SPI Report, Gate drive shutdown, nFAULT

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Table 6-5. Fault Detection and Response Summary (continued)

NAME	SPI FLAG BIT	CONDITION	MODE	DIGITAL CORE	GATE DRIVERS	CHARGE PUMP	CURRENT SENSE	RESPONSE
Sense OCP	OCP_SNS_x	SOx > SNS_OCP_LVL	SNS_OCP_MODE = 000b (Warning)	Active	Active	Active	Active	SPI Report, nFAULT
			SNS_OCP_MODE = 001b (Fault)	Active	Disabled (Soft shutdown)	Active	Active	SPI Report, nFAULT
			SNS_OCP_MODE = 010b (Warning RT)	Active	Active	Active	Active	SPI Report (Unlatched), nFAULT
			SNS_OCP_MODE = 011b (Fault RT)	Active	Disabled (Soft shutdown)	Active	Active	SPI Report (Unlatched), Gate drive shutdown, nFAULT
			SNS_OCP_MODE = 100b (Limit Mode)	Active	Disabled (Standard shutdown)	Active	Active	Gate drive shutdown until next PWM edge
			SNS_OCP_MODE = 111b (Disabled)	Active	Active	Active	Active	N/A
VGS Monitor	VGS_xx	VGS voltage above/below threshold for off/on state	VGS_MODE = 0b (Warn)	Active	Active	Active	Active	SPI Report, nFAULT
			VGS_MODE = 1b (Fault)	Active	Disabled (Standard shutdown)	Active	Active	SPI Report, nFAULT
Watchdog Monitor	WDT_FLT	Watchdog not serviced in window	N/A	Active	Disabled (Standard shutdown)	Active	Active	SPI Report, nFAULT
Deadtime Protection	DEADT_FLT	Deadtime less than DEADT setting	DEADT_MODE_6X = 00b (Fault)	Active	Minimum deadtime enforced	Active	Active	SPI Report, Gate driver outputs enforced, nFAULT
			DEADT_MODE_6X = 01b (Enforce only)	Active	Minimum deadtime enforced	Active	Active	SPI Report, Gate driver outputs enforced, nFAULT
			DEADT_MODE_6X = 10b (Disabled)	Active	Active	Active	Active	N/A
			DEADT_MODE_6X = 11b (Warning)	Active	Minimum deadtime enforced	Active	Active	SPI Report, nFAULT

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Table 6-5. Fault Detection and Response Summary (continued)

NAME	SPI FLAG BIT	CONDITION	MODE	DIGITAL CORE	GATE DRIVERS	CHARGE PUMP	CURRENT SENSE	RESPONSE
Shoot-through Protection	STP_FLT	INHx + INLx simultaneously high	STP_MODE = 0b (Warning + Enforce)	Active	Enforced (Low while both inputs high)	Active	Active	SPI Report, Outputs enforced
			STEP_MODE = 1b (Enforce only)	Active	Enforced (Low while both inputs high)	Active	Active	Outputs enforced
SPI Clock Fault	SPI_CLK_FLT	SPI frame has incorrect number of clocks (not 24 or 32 bits)	N/A	Active	Active	Active	Active	SPI Report, nFAULT, SPI transaction rejected
SPI Address Fault	SPI_ADDR_FLT	SPI Invalid Address Access	N/A	Active	Active	Active	Active	SPI Report, nFAULT, SPI transaction rejected
SPI CRC Fault	SPI_CRC_FLT	SPI CRC value mismatch	N/A	Active	Active	Active	Active	SPI Report, nFAULT, SPI transaction rejected
SPI Parity Fault	SPI_PAR_FLT	SPI parity bit value mismatch	N/A	Active	Active	Active	Active	SPI Report, nFAULT, SPI transaction rejected
OTP CRC Fault	OTP_CRC_FLT	Corruption of internal OTP values	N/A	Active	Disabled (Weak Pulldown)	Active	Active	SPI Report, nFAULT
Device Mode Fault	DEV_MODE_FLT	Device in TI test mode	N/A	Active	Active	Active	Active	SPI Report, nFAULT
Bootstrap Precharge Timeout	BST_TIMEOUT_FLT	Bootstrap precharge not completed by end of timeout period	N/A	Active	Active	Active	Active	SPI Report, nFAULT
Open Load Detection	OPEN_WARN_x	Open load detected by open test sequence	N/A	Active	Active	Active	Active	SPI Report, nFAULT

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Table 6-5. Fault Detection and Response Summary (continued)

NAME	SPI FLAG BIT	CONDITION	MODE	DIGITAL CORE	GATE DRIVERS	CHARGE PUMP	CURRENT SENSE	RESPONSE
Short to Battery Detection	SHT_VDD_WARN_x	Short to battery detected by short test sequence	N/A	Active	Active	Active	Active	SPI Report, nFAULT
Short to GND Detection	SHT_GND_WARN_x	Short to ground detected by short test sequence	N/A	Active	Active	Active	Active	SPI Report, nFAULT

6.5 Device Functional Modes

6.5.1 Gate Driver Functional Modes

6.5.1.1 Sleep Mode

The nSLEEP pin manages the state of the DRV8363-Q1. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, sense amplifiers are disabled, all external MOSFETs are disabled, and the GVDD regulator is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

6.5.1.2 Operating Mode

When the nSLEEP pin is high and the V_{PVDD} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the GVDD regulator and AVDD regulator are active

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6.6 Programming

6.6.1 SPI

The device uses a serial peripheral interface (SPI) bus to set device configurations, operating parameters, and read out diagnostic information. The device SPI operates in secondary mode and connects to an external controller. If SPI CRC (SPI_CRC_EN = 0b) is enabled, the SPI input data (SDI) word consists of a 24 bit word, with one read/write bit, one parity bit, 6-bit address, and 16 bits of data. The SPI output data (SDO) word consists of a 24 bit word, with an 8-bit status data, and 16 bits of register data. If SPI CRC is enabled (SPI_CRC_EN = 1b), an additional 8 bit CRC (initial value 0xFF, polynomial 0x2F) is added to the end of the frame, increasing the total SPI data word length to 32 bits.

A valid frame must meet the following conditions:

- The SCLK pin is low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin is pulled high for at least 400ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is set Hi-Z.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 24 (or 32) SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is not 24 (or 32) bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8 bit command data.
- The SDO pin is a push-pull type output.
- The SPI fault is confirmed at the rising edge of nSCS.

6.6.2 SPI Format

The SDI input data word is 24 (or 32) bits long and consists of the following format:

- 1 parity bit, P. The parity bit uses an even parity scheme, so the number of ones in the SPI frame should be even.
- 6 address bits, A5-A0
- 1 read or write bit, W0. W0 = 0b for write command and W0 = 1b for read command.
- 16 data bits, D15-D0
- 8-bit CRC if SPI_CRC_EN = 1b.

The SDO output data word is 24 (or 32) bits long and consists of the following format.

- 1 fault status bit, F. This bit is identical to IC_STAT1 FAULT register bit.
- 1 parity bit, P. The parity bit uses an even parity scheme, so the number of ones in the SPI frame should be even.
- 6 read back bits, A6-A0. This is the read back of incoming 6 address bits of SDI in the same SPI frame. The device captures SDI at the rising edge of SCLK and pushes SDO out on falling edge of SCLK.
- 16 data bits, D15-D0. This is read data of the addressed register. For write command, it is the data previously stored in the addressed register.
- 8-bit CRC if SPI_CRC_EN = 1b

6.6.3 SPI Format Diagrams

Table 6-6. SDI Input Data Word Format for SPI (24-bit, CRC disabled)

PARITY	ADDRESS						RW	DATA														
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
P	A5	A4	A3	A2	A1	A0	W0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 6-7. SDO Output Data Word Format (24-bit, CRC disabled)

STATUS								DATA														
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
FAULT	P	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 6-8. SDI Input Data Word Format for SPI (32-bit, CRC enabled)

PARITY	ADDRESS							RW	DATA																CRC							
B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
P	A5	A4	A3	A2	A1	A0	W0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0

Table 6-9. SDO Output Data Word Format (32-bit, CRC enabled)

STATUS								DATA																CRC							
B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
FAULT	P	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0

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6.7 Register Maps

This section is a preliminary register map of DRV8363-Q1, and is subject to change.

6.7.1 STATUS Registers

Table 6-10 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in Table 6-10 is considered as reserved locations and the register contents are not to be modified.

Table 6-10. STATUS Registers

Offset	Acronym	Description	Section
0h	IC_STAT1	IC Status Register 1	Section 6.7.1.1
1h	IC_STAT2	IC Status Register 2	Section 6.7.1.2
2h	IC_STAT3	IC Status Register 3	Section 6.7.1.3
3h	IC_STAT4	IC Status Register 4	Section 6.7.1.4
4h	IC_STAT5	IC Status Register 5	Section 6.7.1.5
5h	IC_STAT6	IC Status Register 6	Section 6.7.1.6

Complex bit access types are encoded to fit into small table cells. Table 6-11 shows the codes that are used for access types in this section.

Table 6-11. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

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6.7.1.1 IC_STAT1 Register (Offset = 0h) [Reset = 8000h]

IC_STAT1 is shown in Table 6-12.

Return to the Summary Table.

Table 6-12. IC_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_OK	R	1h	No SPI Fault is detected 0h = SPI Fault is detected 1h = No fault
14	FAULT	R	0h	Logic OR of FAULT status registers. Mirrors nFAULT pin. 0h = nFAULT status logic-low 1h = nFAULT status logic-high. One or multiple fault events detected.
13	WARN	R	0h	Logic OR of WARN status, except OTW 0h = No warning event detected 1h = One or multiple warning event detected
12	VDS	R	0h	Logic OR of VDS overcurrent detection 0h = No VDS events detected. 1h = One or multiple VDS events detected.
11	VGS	R	0h	Logic OR of VGS detection 0h = No VGS events detected. 1h = One or multiple VGS events detected.
10	SNS_OCP	R	0h	Logic OR of Sense overcurrent detection 0h = No sense overcurrent events detected. 1h = One or multiple sense overcurrent events detected.
9	OV	R	0h	Logic OR of supply voltage overvoltage detection 0h = No overvoltage events detected. 1h = One ore more overvoltage events detected.
8	UV	R	0h	Logic OR of supply voltage undervoltage detection 0h = No undervoltage events detected. 1h = One ore more undervoltage events detected.
7	RESET_STAT	R	0h	Digital reset status: follows digital reset signal. Cleared by setting CLR_FLT=1. 0h = Signal has been cleared by setting CLR_FLT to 1 1h = Digital has come out from reset
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	OTW	R	0h	Overtemperature Warning Status Bit 0h = No event is detected 1h = Overtemperature warning event detected
0	DRV_STAT	R	0h	Indicates Driver Enable Status: driver is following INxx inputs 0h = Driver output is disabled 1h = Driver output is enabled

6.7.1.2 IC_STAT2 Register (Offset = 1h) [Reset = 0000h]

IC_STAT2 is shown in Table 6-13.

Return to the Summary Table.

Table 6-13. IC_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	SNS_OCP_A	R	0h	Overcurrent on External Sense Resistor Status Bit on phase A 0h = No fault detected 1h = Fault detected
9	SNS_OCP_B	R	0h	Overcurrent on External Sense Resistor Status Bit on phase B 0h = No fault detected 1h = Fault detected
8	SNS_OCP_C	R	0h	Overcurrent on External Sense Resistor Status Bit on phase C 0h = No fault detected 1h = Fault detected
7	RESERVED	R	0h	Reserved
6	PH_DIAG_ACTIVE	R	0h	PH_DIAG is active (one or more of PH_DIAG_xx is high) 0h = PH_DIAG not currently active 1h = PH_DIAG is currently active
5	VDS_HA	R	0h	VDS Overcurrent Status on the A High-side MOSFET 0h = No fault detected 1h = Fault detected
4	VDS_LA	R	0h	VDS Overcurrent Status on the A Low-side MOSFET 0h = No fault detected 1h = Fault detected
3	VDS_HB	R	0h	VDS Overcurrent Status on the B High-side MOSFET 0h = No fault detected 1h = Fault detected
2	VDS_LB	R	0h	VDS Overcurrent Status on the B Low-side MOSFET 0h = No fault detected 1h = Fault detected
1	VDS_HC	R	0h	VDS Overcurrent Status on the C High-side MOSFET 0h = No fault detected 1h = Fault detected
0	VDS_LC	R	0h	VDS Overcurrent Status on the C Low-side MOSFET 0h = No fault detected 1h = Fault detected

6.7.1.3 IC_STAT3 Register (Offset = 2h) [Reset = 0000h]

IC_STAT3 is shown in Table 6-14.

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Table 6-14. IC_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SHT_VDD_FLT_A	R	0h	Short-to-battery status on phase A 0h = No fault detected 1h = Fault detected
14	SHT_VDD_FLT_B	R	0h	Short-to-battery status on phase B 0h = No fault detected 1h = Fault detected
13	SHT_VDD_FLT_C	R	0h	Short-to-battery status on phase C 0h = No fault detected 1h = Fault detected
12	SHT_GND_FLT_A	R	0h	Short-to-GND status on phase A 0h = No fault detected 1h = Fault detected
11	SHT_GND_FLT_B	R	0h	Short-to-GND status on phase B 0h = No fault detected 1h = Fault detected
10	SHT_GND_FLT_C	R	0h	Short-to-GND status on phase C 0h = No fault detected 1h = Fault detected
9	OPEN_FLT_A	R	0h	Open load status on phase A 0h = No fault detected 1h = Fault detected
8	OPEN_FLT_B	R	0h	Open load status on phase B 0h = No fault detected 1h = Fault detected
7	OPEN_FLT_C	R	0h	Open load status on phase C 0h = No fault detected 1h = Fault detected
6	RESERVED	R	0h	Reserved
5	VGS_HA	R	0h	Gate driver fault status on the A High-side MOSFET. 0h = No fault detected 1h = Fault detected
4	VGS_LA	R	0h	Gate driver fault status on the A Low-side MOSFET. 0h = No fault detected 1h = Fault detected
3	VGS_HB	R	0h	Gate driver fault status on the B High-side MOSFET. 0h = No fault detected 1h = Fault detected
2	VGS_LB	R	0h	Gate driver fault status on the B Low-side MOSFET. 0h = No fault detected 1h = Fault detected
1	VGS_HC	R	0h	Gate driver fault status on the C High-side MOSFET. 0h = No fault detected 1h = Fault detected
0	VGS_LC	R	0h	Gate driver fault status on the C Low-side MOSFET. 0h = No fault detected 1h = Fault detected

6.7.1.4 IC_STAT4 Register (Offset = 3h) [Reset = 0000h]

IC_STAT4 is shown in Table 6-15.

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Table 6-15. IC_STAT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	RESERVED
14	DVDD_OV	R	0h	DVDD overvoltage detection 0h = No event is detected 1h = DVDD overvoltage event detected
13	VDRAIN_OV	R	0h	VDRAIN overvoltage status 0h = No fault detected 1h = Fault detected
12	VDRAIN_UVH	R	0h	VDRAIN undervoltage status, High threshold 0h = No fault detected 1h = Fault detected
11	VDRAIN_UVL	R	0h	VDRAIN undervoltage status, Low threshold 0h = No fault detected 1h = Fault detected
10	VCP_UV	R	0h	VCP undervoltage status 0h = No fault detected 1h = Fault detected
9	GVDD_OV	R	0h	GVDD overvoltage status 0h = No fault detected 1h = Fault detected
8	GVDD_UVH	R	0h	GVDD undervoltage status, high threshold 0h = No fault detected 1h = Fault detected
7	GVDD_UV_BST	R	0h	GVDD undervoltage status, BST 0h = No fault detected 1h = Fault detected
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	VREF_UV	R	0h	VREF undervoltage status 0h = No fault detected 1h = Fault detected
3	BST_TIMEOUT_FLT	R	0h	BST timeout fault during power-up (either BST_UV or VCP_UV remained high for longer than approximately 10ms during power-up sequence) 0h = No fault detected 1h = Fault detected
2	BSTA_UV	R	0h	BST undervoltage on the A High-side MOSFET 0h = No fault detected 1h = Fault detected
1	BSTB_UV	R	0h	BST undervoltage on the B High-side MOSFET 0h = No fault detected 1h = Fault detected
0	BSTC_UV	R	0h	BST undervoltage on the C High-side MOSFET 0h = No fault detected 1h = Fault detected

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6.7.1.5 IC_STAT5 Register (Offset = 4h) [Reset = 0000h]

IC_STAT5 is shown in Table 6-16.

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Table 6-16. IC_STAT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	RESERVED
14	RESERVED	R	0h	RESERVED
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	OTSD_TCP	R	0h	Overtemperature Shutdown TCP Status Bit 0h = No event is detected 1h = Overtemperature shutdown TCP event detected
10	OTSD	R	0h	Overtemperature Shutdown Status Bit 0h = No event is detected 1h = Overtemperature shutdown event detected
9	WDT_FLT	R	0h	Watchdog timer fault status 0h = No fault detected 1h = Fault detected
8	SPI_PAR_FLT	R	0h	SPI parity bit fault status 0h = No fault detected 1h = Fault detected
7	SPI_CRC_FLT	R	0h	SPI CRC fault status 0h = No fault detected 1h = Fault detected
6	SPI_ADDR_FLT	R	0h	SPI address fault status 0h = No fault detected 1h = Attempted access to invalid register address detected
5	SPI_CLK_FLT	R	0h	SPI clock fault status 0h = No fault detected 1h = Incorrect number of SCLK cycles detected
4	OTP_CRC_FLT	R	0h	OTP CRC fault status 0h = No fault detected
3	DEV_MODE_FLT	R	0h	Device mode fault status 0h = No fault detected 1h = Fault detected
2	RESERVED	R	0h	
1	STP_FLT	R	0h	Shoot-through protection fault status 0h = No fault detected 1h = Shoot-through input condition detected (INHx/INLx high simultaneously)
0	DEADT_FLT	R	0h	Deadtime protection fault status 0h = No fault detected 1h = Minimum dead time violation detected

6.7.1.6 IC_STAT6 Register (Offset = 5h) [Reset = 0000h]

IC_STAT6 is shown in Table 6-17.

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Table 6-17. IC_STAT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	VDRAIN_UVOV_RAW	R	0h	Un-latched status bit of VDRAIN OV/UV monitor output 0h = No fault detected 1h = Fault detected
6	GVDD_UVOV_RAW	R	0h	Un-latched status bit of GVDD OV/UV monitor output 0h = No fault detected 1h = Fault detected
5	BST_VCP_UV_RAW	R	0h	Un-latched status bit of BST UV and VCP UV monitor output 0h = No fault detected 1h = Fault detected
4	VREF_UV_RAW	R	0h	Un-latched status but of VREF UV monitor output 0h = No fault detected 1h = Fault detected
3	DVDD_OV_RAW	R	0h	Un-latched status bit of DVDD OV monitor output 0h = No fault detected 1h = Fault detected
2	OTSD_RAW	R	0h	Un-latched status bit of OTSD monitor output 0h = No fault detected 1h = Fault detected
1	RESERVED	R	0h	
0	RESERVED	R	0h	

6.7.2 CONTROL Registers

Table 6-18 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in Table 6-18 are considered as reserved locations and the register contents are not to be modified.

Table 6-18. CONTROL Registers

Offset	Acronym	Description	Section
9h	IC_CTRL1	IC Control Register 1	Section 6.7.2.1
Ah	IC_CTRL2	IC Control Register 2	Section 6.7.2.2
Bh	GD_CTRL1	Gate Drive Control Register 1	Section 6.7.2.3
Ch	GD_CTRL2	Gate Drive Control Register 2	Section 6.7.2.4
Dh	GD_CTRL3	Gate Drive Control Register 3	Section 6.7.2.5
Eh	GD_CTRL4	Gate Drive Control Register 4	Section 6.7.2.6
Fh	GD_CTRL5	Gate Drive Control Register 5	Section 6.7.2.7
13h	CSA_CTRL1	CSA Control Register 1	Section 6.7.2.8
14h	CSA_CTRL2	CSA Control Register 2	Section 6.7.2.9
15h	MON_CTRL1	Monitor Control Register 1	Section 6.7.2.10
16h	MON_CTRL2	Monitor Control Register 2	Section 6.7.2.11
17h	MON_CTRL3	Monitor Control Register 3	Section 6.7.2.12
18h	MON_CTRL4	Monitor Control Register 4	Section 6.7.2.13
19h	MON_CTRL5	Monitor Control Register 5	Section 6.7.2.14
1Ah	MON_CTRL6	Monitor Control Register 6	Section 6.7.2.15
1Bh	DIAG_CTRL1	Diagnostic Control Register 1	Section 6.7.2.16
1Ch	IC_CTRL_SP	IC Control Special Register	Section 6.7.2.17

Complex bit access types are encoded to fit into small table cells. Table 6-19 shows the codes that are used for access types in this section.

Table 6-19. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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6.7.2.1 IC_CTRL1 Register (Offset = 9h) [Reset = 0106h]

IC_CTRL1 is shown in Table 6-20.

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Table 6-20. IC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DIS_PWM_INPUT	R/W	0h	Disable PWM inputs 0h = Gate driver outputs are controlled by INHx and INL digital inputs. 1h = INHx and INLx digital inputs are ignored and the gate driver outputs are pulled low (active pull down) by default.
14	WARN_MODE	R/W	0h	Warning nFAULT mode; Control nFAULT response for warning events 0h = No nFAULT reporting for warning response. Status flags are set. 1h = nFAULT is driven low for warning response. Status flags are set.
13	DIS_SSC	R/W	0h	TI Internal design parameter: No change is required unless notified by TI. The bit disables Spread Spectrum Clocking feature of the device internal oscillator 0h = Normal operation. Spread Spectrum Clocking feature is enabled. 1h = Spread Spectrum Clock feature is disabled for TI debug purpose.
12	RESERVED	R	0h	Reserved
11	EBRAKE_LS_FORCE	R/W	0h	Force LS Emergency brake even under OCP_VDS_LS_x fault (if Ebrake is enabled 0h = LS Ebrake is not forced 1h = LS Ebrake is forced as described
10	EBRAKE_MODE	R/W	0h	Emergency brake on LS or HS 0h = Emergency brake by turning ON all LS FETs 1h = Emergency brake by turning ON all HS FETs
9	EBRAKE_EN	R/W	0h	Enable Emergency Brake (OR'ed with BRAKE pin) 0h = Normal mode 1h = Enable emergency brake
8	EBRAKE_PRIORITY	R/W	1h	Emergency brake priority over faults other than OTSD, GVDD_UVH, GVDDD_OV, and DRVOFF. These three listed faults have always priority over Ebrake. 0h = Brake has lower priority than all faults 1h = Brake has priority over faults other than OTSD, GVDD_UVH and DRVOFF (default)
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-1	LOCK	R/W	3h	Lock and unlock the register setting Bit settings not listed have no effect. 3h = Unlock all the registers 6h = Lock the settings by ignoring further register writes except to these bits.
0	CLR_FLT	R/W	0h	Clear fault. After fault event is detected and fault flag is set, TI recommends to issue CLR_FLT command first, then ENABLE_DRV command next in a separate SPI frame. If CLR_FLT and ENABLE_DRV commands are issued in the same SPI frame, CLR_FLT is higher priority and ENABLE_DRV is not set if fault flag is already latched and the device is waiting CLR_FLT. 0h = No action 1h = Clear faults. Self-clear to 0b.

6.7.2.2 IC_CTRL2 Register (Offset = Ah) [Reset = 0000h]

IC_CTRL2 is shown in Table 6-21.

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Table 6-21. IC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	TCP_SW_CURLIM	R/W	0h	TCP Switch current limit after TCP_EN_DLY 0h = 1.25mA (typ) 1h = 2.3mA (typ)
5-4	TCP_SW_HD_CURLIM	R/W	0h	TCP Switch HD current limit for High Duty cycle (TCP_HD_DIS=0) 0h = 7.7mA (typ) 1h = 6.4mA (typ) 2h = 10.5mA (typ) 3h = 9.2mA (typ)
3	TCP_SW_DLY	R/W	0h	Delay time to activate trickle charge pump after the device detects PWM inactive (INHx=INLx=Low) 0h = 100us (typ) 1h = 250us (typ)
2	TCP_HD_DIS	R/W	0h	VCP/TCP high-duty disabled 0h = TCP High-Duty cycle is enabled 1h = TCP High-Duty cycle is disabled
1-0	TCP_SW_MODE	R/W	0h	VCP/TCP mode control 0h = Normal VCP/TCP operation. VCP/TCP is enabled at power up. TCP SW responds to PWM inputs. TCP SW is enabled even if SPI DIS_PWM_INPUT is 1. When DRVOFF is high and if system expects the device to keep BST cap stay charged, TCP_SW_MODE must be 00b. 1h = VCP/CPTH-SHx switch is disabled. VCP/TCP charge pump clock is active. 2h = VCP/TCP shutdown. Both VCP/CPTH-SHx switch and VCP/TCP charge pump clock are disabled. 3h = Normal VCP/TCP operation. VCP/TCP is enabled at power up.

6.7.2.3 GD_CTRL1 Register (Offset = Bh) [Reset = 0038h]

GD_CTRL1 is shown in Table 6-22.

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Table 6-22. GD_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PWM1X_COM	R/W	0h	1x PWM Commutation Control 0h = 1x PWM mode uses synchronous rectification 1h = 1x PWM mode uses asynchronous rectification
14	PWM1X_DIR	R/W	0h	1x PWM Direction. In 1x PWM mode this bit is ORed with the INHC (DIR) input
13-12	PWM1X_BRAKE	R/W	0h	1x PWM output configuration 0h = Outputs follow commanded inputs 1h = Turn on all three low-side MOSFETs 2h = Turn on all three high-side MOSFETs 3h = Turn off all six MOSFETs (coast)
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-8	PWM_MODE	R/W	0h	PWM mode 0h = 6x PWM mode (INHx/INLx) 1h = 3x PWM mode with INLx enable control 2h = 1x PWM mode (INHx/INLx) 3h = Independent
7	STP_MODE_6X	R/W	0h	Control reporting for STP faults in 6xPWM mode 0h = Reporting enabled (outputs forced low) 1h = Reporting disabled (outputs forced low)
6-3	DEADT	R/W	7h	Gate driver dead time 0h = 70ns 1h = 120ns 2h = 180ns 3h = 300ns 4h = 400ns 5h = 500ns 6h = 600ns 7h = 750ns 8h = 1000ns 9h = 1.5us Ah = 2us Bh = 2.5us Ch = 3us Dh = 3.5us Eh = 5us Fh = 10us
2	DEADT_MODE	R/W	0h	Open Loop/Closed Loop 0h = Dead time is inserted when device input (INHx or INLx) goes low 1h = Dead time is inserted by monitoring gate driver outputs (GHx or GLx)

Table 6-22. GD_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	DEADT_MODE_6X	R/W	0h	Dead Time Violation Response Mode for 6 PWM mode only. NOTE: Other than 6 PWM mode, dead time is always inserted regardless of the DEADT_MODE bit and no fault is reported to the MCU. 0h = Dead-time protection is enabled. Reporting is performed. Gate driver control signals are enforced low during the dead time period. SPI fault flag is set and nFAULT pin is driven low when dead time condition is detected. 1h = Dead-time protection is enabled. Reporting is not performed. Gate driver control signals are enforced low during the dead time period. SPI fault flag is never set and nFAULT pin stays high when dead time condition is detected. 2h = Dead-time protection is disabled. No dead time is inserted. No SPI fault flag is set and the nFAULT1 pin stays high. This is applied to both cases when DEADT_MODE is 0b (monitoring INH or INL) and 1b (monitoring GHx or GLx). 3h = Dead-time protection is enabled and SPI fault is set but no nFAULT reporting is performed. Gate driver outputs are forced low during dead time period. nFAULT pin stays high when dead time condition is detected.

6.7.2.4 GD_CTRL2 Register (Offset = Ch) [Reset = 7700h]

GD_CTRL2 is shown in Table 6-23.

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Table 6-23. GD_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	TDRVP	R/W	7h	Peak source pull up drive timing 0h = 200ns 1h = 300ns 2h = 400ns 3h = 500ns 4h = 650ns 5h = 750ns 6h = 900ns 7h = 1000ns 8h = 1.4us 9h = 1.6us Ah = 2us Bh = 2.2us Ch = 2.6us Dh = 3us Eh = 3.5us Fh = 4us
11-8	TDRVN	R/W	7h	Peak sink pull down drive timing
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	IHOLD_SEL	R/W	0h	Select IHOLD pull-up and pull-down current. IHOLD_SEL bit must be configured while PWM is inactive (ENABLE_DRV is 0b). 0h = IHOLD pull-up/down 500mA/1000mA (typ) 1h = IHOLD pull-up/down 260mA/260mA (typ)
3-0	IDRVN_SD	R/W	0h	Smart shutdown drive current.

6.7.2.5 GD_CTRL3 Register (Offset = Dh) [Reset = 0000h]

GD_CTRL3 is shown in Table 6-24.

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Table 6-24. GD_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	IDRVP_HA	R/W	0h	High-side peak source pull up current.
11-8	IDRVN_HA	R/W	0h	High-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.
7-4	IDRVP_LA	R/W	0h	Low-side peak source pull up current.
3-0	IDRVN_LA	R/W	0h	Low-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.

6.7.2.6 GD_CTRL4 Register (Offset = Eh) [Reset = 0000h]

GD_CTRL4 is shown in Table 6-25.

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Table 6-25. GD_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	IDRVP_HB	R/W	0h	High-side peak source pull up current.
11-8	IDRVN_HB	R/W	0h	High-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.
7-4	IDRVP_LB	R/W	0h	Low-side peak source pull up current.
3-0	IDRVN_LB	R/W	0h	Low-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.

6.7.2.7 GD_CTRL5 Register (Offset = Fh) [Reset = 0000h]

GD_CTRL5 is shown in Table 6-26.

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Table 6-26. GD_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	IDRVP_HC	R/W	0h	High-side peak source pull up current.
11-8	IDRVN_HC	R/W	0h	High-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.
7-4	IDRVP_LC	R/W	0h	Low-side peak source pull up current.
3-0	IDRVN_LC	R/W	0h	Low-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.

6.7.2.8 CSA_CTRL1 Register (Offset = 13h) [Reset = 0000h]

CSA_CTRL1 is shown in Table 6-27.

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Table 6-27. CSA_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	CSA_AZ_TMAX	R/W	0h	Max delay to toggle CSA_CLK if no PWM input switching 0h = 250us 1h = 1ms 2h = 5ms 3h = No delay
3	CSA_AZ_DIS	R/W	0h	Current Sense Amplifier Auto Zero function disable (Note for Luis: force CSA clock low, bring this signal to top level) 0h = CSA Auto Zero function is enabled. This bit is 0b during normal PWM/CSA operation. 1h = CSA Auto Zero function is disabled. The purpose of this bit is to disable switching activity of current sense amplifier for auto zero function. Refer to timing requirements if this bit is used.
2	CSA_A_DIS	R/W	0h	Disable CSA channel A 0h = CSA channel A enabled 1h = CSA channel A disabled
1	CSA_B_DIS	R/W	0h	Disable CSA channel A 0h = CSA channel B enabled 1h = CSA channel B disabled
0	CSA_C_DIS	R/W	0h	Disable CSA channel C 0h = CSA channel C enabled 1h = CSA channel C disabled

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6.7.2.9 CSA_CTRL2 Register (Offset = 14h) [Reset = 0000h]

CSA_CTRL2 is shown in Table 6-28.

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Table 6-28. CSA_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AREF_DIV	R/W	0h	VREF dividing ratio 0h = 1/2 1h = 1/8
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-8	WDT_TEST	R/W	0h	SPI Test register for WDT. Write access to this register has no effect on device operation, but the watchdog timer is reset if accessed within the correct window.
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	CSA_GAIN_A	R/W	0h	CSA Gain of SOA. Gain can be updated during PWM operation. Undefined settings (1001b - 1111b) are 40. 0h = 5 1h = 10 2h = 20 3h = 40
3-2	CSA_GAIN_B	R/W	0h	CSA Gain of SOB. Gain can be updated during PWM operation. Undefined settings (1001b - 1111b) are 40. 0h = 5 1h = 10 2h = 20 3h = 40
1-0	CSA_GAIN_C	R/W	0h	CSA Gain of SOC. Gain can be updated during PWM operation. Undefined settings (1001b - 1111b) are 40. 0h = 5 1h = 10 2h = 20 3h = 40

6.7.2.10 MON_CTRL1 Register (Offset = 15h) [Reset = 4000h]

MON_CTRL1 is shown in Table 6-29.

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Table 6-29. MON_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	VDRAIN_OV_LVL	R/W	1h	VDRAIN Overvoltage threshold level 0h = 36V (typ) 1h = 54V (typ) 2h = 72V (typ) 3h = 84V (typ)
13-12	VDRAIN_UVH_LVL	R/W	0h	VDRAIN UV High threshold level 0h = 18V 1h = 20V 2h = 22V 3h = 24V
11	VDRAIN_UVL_LVL	R/W	0h	VDRAIN UV Low threshold level 0h = 10.5V 1h = 5.55V
10-8	VDRAIN_OV_MODE	R/W	0h	When set for Ebrake mode: HS or LS brake from SPI_BRAKE bit If VDRAIN_OV=1 while WPD on VDS response then Brake and LS APD (no WPD) regardless of SPI_BRAKE 0h = Warning mode (latched) 1h = Fault mode (latched) 2h = EBrake mode (latched, HS or LS based on SPI_EBRAKE_DIR or VDS fault) 3h = EBrake mode (autorecovery, HS or LS based on SPI_EBRAKE_DIR or VDS fault) 4h = Default mode 5h = Default mode 6h = Default mode 7h = No report. No shutdown.
7-6	VDRAIN_UVH_MODE	R/W	0h	VDRAIN monitor mode for under voltage monitor 0h = Warning mode (latched) 1h = Fault mode (latched) 2h = Warning mode (autorecovery) 3h = No report. No shutdown.
5-4	VDRAIN_UVL_MODE	R/W	0h	VDRAIN monitor mode for under voltage monitor 0h = Warning mode (latched) 1h = Fault mode (latched) 2h = Warning mode (autorecovery) VDS faults are disabled 3h = No report. No shutdown.
3	GVDD_UVH_MODE	R/W	0h	GVDD_UVH monitor mode 0h = Warning mode (latched) 1h = Fault mode (latched)
2-1	GVDD_UV_BST_MODE	R/W	0h	GVDD_UV_BST monitor mode. nFAULT remains high regardless of WARN_MODE. 0h = Warning mode (autorecovery), VCP_UV input remains enabled, BST_UV_LVL not forced 1h = Warning special mode (latched), VCP_UV input disabled, BST_UV_LVL is 1 2h = Warning special mode (autorecovery), VCP_UV input disabled, BST_UV_LVL is 1 3h = No report. No action.
0	GVDD_UV_BST_LVL	R/W	0h	GVDD_UV_BST monitor threshold level. 0h = 10.6V (typ) 1h = 9.6V (typ)

ADVANCE INFORMATION

6.7.2.11 MON_CTRL2 Register (Offset = 16h) [Reset = 8003h]

MON_CTRL2 is shown in Table 6-30.

Return to the Summary Table.

Table 6-30. MON_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GVDD_OV_MODE	R/W	1h	GVDD monitor mode of over voltage monitor 0h = Warning mode (latched) 1h = Fault mode (latched)
14	VDRAIN_UVL_MASK	R/W	0h	If active the bit` masks VDRAIN_UVL during first power-up sequence. 0h = Normal operation 1h = VDRAIN_UVL is masked during first power-up sequence
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	OCP_SNS_STD_SHD	R/W	0h	Shutdown type for OCP_SNS faults 0h = Soft shutdown sequence (fixed Tdrv) 1h = Standard shutdown sequence (follows TDRVN)
10	OCP_SNS_A_EN	R/W	0h	Shunt OCP enable for channel A 0h = Shunt OCP for channel A disabled 1h = Shunt OCP for channel A enabled
9	OCP_SNS_B_EN	R/W	0h	Shunt OCP enable for channel B 0h = Shunt OCP for channel B disabled 1h = Shunt OCP for channel B enabled
8	OCP_SNS_C_EN	R/W	0h	Shunt OCP enable for channel C 0h = Shunt OCP for channel C disabled 1h = Shunt OCP for channel C enabled
7	OCP_SNS_LVL	R/W	0h	Threshold voltage of V_{SENSE} overcurrent protection (shunt OCP). Threshold is represented as a % of VREF. 0h = 80%/20% of VREF-GND 1h = 90%/10% of VREF-GND
6	RESERVED	R	0h	Reserved
5	SNS_OCP_TRETRY	R/W	0h	Sense OCP retry time 0h = 1ms 1h = 9ms
4-2	SNS_OCP_MODE	R/W	0h	Monitor mode of V_{SENSE} overcurrent protection (Rshunt monitor) 0h = Warning mode (latched) 1h = Fault mode (latched) 2h = Warning mode (autorecovery) 3h = Fault mode (autorecovery) 4h = Limit mode (autorecovery CBC) 5h = Default mode 6h = Default mode 7h = No report. No shutdown.
1-0	SNS_OCP_DEG	R/W	3h	Deglitch time of V_{SENSE} overcurrent protection (Rshunt monitor) 0h = 3.0us (typ) 1h = 6.0us (typ) 2h = 9.0us (typ) 3h = 12.0us (typ)

ADVANCE INFORMATION

6.7.2.12 MON_CTRL3 Register (Offset = 17h) [Reset = 5101h]

MON_CTRL3 is shown in Table 6-31.

Return to the Summary Table.

Table 6-31. MON_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	VDS_MODE	R/W	1h	VDS overcurrent mode 0h = Warning mode (latched) 1h = Fault mode (latched) 2h = Default mode 3h = No report. No shutdown.
13-11	VDS_VGS_BLK	R/W	2h	VDS overcurrent and VGS blanking time 0h = 150ns 1h = 500ns 2h = 1us 3h = 2us 4h = 6us 5h = 8us 6h = 10us 7h = 12us
10-8	VDS_DEG	R/W	1h	VDS overcurrent deglitch time 0h = 500ns 1h = 1us 2h = 1.5us 3h = 2us 4h = 4us 5h = 6us 6h = 8us 7h = 8us
7-6	VGS_MODE	R/W	0h	VGS monitor mode 0h = Warning mode (latched) 1h = Fault mode (latched) 2h = Default mode 3h = No report. No shutdown.
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-0	VGS_DEG	R/W	1h	VGS monitor deglitch time 0h = 500ns 1h = 1us 2h = 1.5us 3h = 2us 4h = 2us 5h = 2us 6h = 2us 7h = 2us

ADVANCE INFORMATION

6.7.2.13 MON_CTRL4 Register (Offset = 18h) [Reset = 0000h]

MON_CTRL4 is shown in Table 6-32.

Return to the Summary Table.

Table 6-32. MON_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	WDT_FLT_MODE	R/W	0h	Watchdog Time Fault Mode 0h = Warning mode (latched) 1h = Fault mode (latched). Gate Driver shutdown.
4	WDT_CNT	R/W	0h	Watchdog Time Fault Count 0h = One time WDT fault reports status flag and asserts nFAULT1 pin low. 1h = Three consecutive faults report status flag and assert nFAULT pin low. Internal counter is cleared to 0 after the three consecutive faults are detected. Internal counter can also be cleared if WDT_EN is cleared to 0b.
3	WDT_MODE	R/W	0h	Watchdog Time MODE 0h = Any valid read access reset the watchdog timer 1h = A valid write access to CSA_CTRL2 resets the watchdog timer
2-1	WDT_W	R/W	0h	Watchdog Timer window tWDL (lower window) and tWDU (upper window) 0h = tWDL 0.5ms tWDU 10ms 1h = tWDL 1ms tWDU 20ms 2h = tWDL 2ms tWDU 40ms 3h = tWDL 2ms tWDU 40ms
0	WDT_EN	R/W	0h	Watchdog Time Enable 0h = Watchdog timer disabled 1h = Watchdog timer enabled

6.7.2.14 MON_CTRL5 Register (Offset = 19h) [Reset = 0000h]

MON_CTRL5 is shown in Table 6-33.

Return to the Summary Table.

Table 6-33. MON_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	SPARE_19h_7	R/W	0h	Spare
6	DVDD_OV_MODE	R/W	0h	DVDD monitor for overvoltage 0h = Warning mode (latched) 1h = Fault mode (latched)
5-4	VCP_UV_MODE	R/W	0h	VCP monitor mode of under voltage monitor 0h = Warning mode (latched) 1h = Fault mode (latched, TCP ON) 2h = Fault mode (latched, TCP OFF) 3h = No report. No shutdown.
3	BST_UV_LVL	R/W	0h	BST pin undervoltage threshold level V_{BST_UV} 0h = 6.0V (typ) 1h = 5.0V (typ)
2-0	BST_UV_MODE	R/W	0h	BST pin UV monitor mode. 0h = Warning mode (latched) 1h = Fault mode (real time) HS Active PD 2h = Fault mode (real time) HS Weak PD 3h = Fault mode (latched) HS Active PD 4h = Fault mode (latched) HS Weak PD 5h = Fault mode (latched) HS Weak PD, TCP_SW OFF 6h = Default mode 7h = No report. No action.

ADVANCE INFORMATION

6.7.2.15 MON_CTRL6 Register (Offset = 1Ah) [Reset = 2000h]

MON_CTRL6 is shown in Table 6-34.

Return to the Summary Table.

Table 6-34. MON_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	ALL_CH	R/W	1h	All channel shutdown enable 0h = Associated faulty half-bridge is shutdown (active pull down) in response to VDS, VGS and OCP_SNS. nFAULT goes low after all three channels have the faults. For a recovery sequence to re-start PWM, MCU uses CLR_FLT. 1h = All three half-bridges are shutdown (semi-active pull down) in response to VDS, VGS and OCP_SNS. nFAULT goes low if one or multiple channels have the faults.
12	RESERVED	R	0h	Reserved
11-8	VDS_LVL_A	R/W	0h	VDS overcurrent threshold for phase A 0h = 100mV 1h = 150mV 2h = 200mV 3h = 300mV 4h = 400mV 5h = 500mV 6h = 600mV 7h = 700mV 8h = 800mV 9h = 900mV Ah = 1.0V Bh = 1.5V Ch = 2.0V
7-4	VDS_LVL_B	R/W	0h	VDS overcurrent threshold for phase B
3-0	VDS_LVL_C	R/W	0h	VDS overcurrent threshold for phase C

6.7.2.16 DIAG_CTRL1 Register (Offset = 1Bh) [Reset = 0000h]

DIAG_CTRL1 is shown in Table 6-35.

Return to the Summary Table.

Table 6-35. DIAG_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	RESERVED
14	RESERVED	R	0h	RESERVED
13	RESERVED	R	0h	RESERVED
12	SPARE_1bh_12	R/W	0h	Spare
11	OPEN_DET_EN	R/W	0h	Automated offline open load detection. Runs second if short_en_det is enabled. Bit auto-clears when sequence complete. 0h = Normal operation 1h = Automated open-load detection is enabled
10	SHORT_DET_EN	R/W	0h	Automated offline short load detection. Runs first if open_en_det is enabled. Bit auto-clears when sequence complete. 0h = Normal operation 1h = Automated short-load detection is enabled
9-8	OFFLINE_DLY	R/W	0h	Automated offline detection delay 0h = 50us (typ) 1h = 250us (typ) 2h = 1ms (typ) 3h = 2.2ms (typ)
7	TCP_LL_MODE	R/W	0h	To reduce TCP_SWITCH current limit for phase diagnostics 0h = Normal TCP_SWITCH current limit 1h = Reduced TCP_SWITCH current limit (230uA, typical)
6	PH_DIAG_LL	R/W	0h	Phase diagnostic low leakage with predriver enabled/disable 0h = PWM'ing allowed during phase diagnostic 1h = No PWM'ing allowed during phase diagnostic
5	PH_DIAG_HA	R/W	0h	Phase diagnostic pull-up enable for phase A 0h = Diagnostic current source disabled 1h = Diagnostic current source enabled
4	PH_DIAG_LA	R/W	0h	Phase diagnostic pull-down enable for phase A 0h = Diagnostic current source disabled 1h = Diagnostic current source enabled
3	PH_DIAG_HB	R/W	0h	Phase diagnostic pull-up enable for phase B 0h = Diagnostic current source disabled 1h = Diagnostic current source enabled
2	PH_DIAG_LB	R/W	0h	Phase diagnostic pull-down enable for phase B 0h = Diagnostic current source disabled 1h = Diagnostic current source enabled
1	PH_DIAG_HC	R/W	0h	Phase diagnostic pull-up enable for phase C 0h = Diagnostic current source disabled 1h = Diagnostic current source enabled
0	PH_DIAG_LC	R/W	0h	Phase diagnostic pull-down enable for phase C 0h = Diagnostic current source disabled 1h = Diagnostic current source enabled

6.7.2.17 IC_CTRL_SP Register (Offset = 1Ch) [Reset = 0805h]

IC_CTRL_SP is shown in Table 6-36.

Return to the Summary Table.

Table 6-36. IC_CTRL_SP Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPARE_1ch_15	R/W	0h	Spare
14	SPARE_1ch_14	R/W	0h	Spare
13	SPI_CRC_EN	R/W	0h	Enable SPI CRC 0h = No CRC, 24-bit frame 1h = CRC enabled, 32-bit frame
12	DVDD_LVL	R/W	0h	Bit to control LDO output voltage 0h = 3.3V 1h = 5V
11	OTSD_MODE	R/W	1h	Overtemperature shutdown mode 0h = Warning mode (latched) 1h = Fault mode (latched)
10	RESERVED	R	0h	RESERVED
9	RESERVED	R	0h	RESERVED
8	RESERVED	R	0h	RESERVED
7	RESERVED	R	0h	RESERVED
6	RESERVED	R	0h	RESERVED
5	RESERVED	R	0h	RESERVED
4	RESERVED	R	0h	RESERVED
3	RESERVED	R	0h	RESERVED
2-0	LOCK2	R/W	5h	Unlock and lock this register Bit settings not listed have no effect. 2h = Unlock this register 5h = Lock the settings of this register by ignoring further writes except to these bits.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The DRV8363-Q1 is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *Section 7.2* section highlight how to use and configure the device.

7.2 Typical Application

7.2.1 Typical Application with 48-pin package

Figure shows a typical application diagram of DRV8363-Q1 48-pin package.

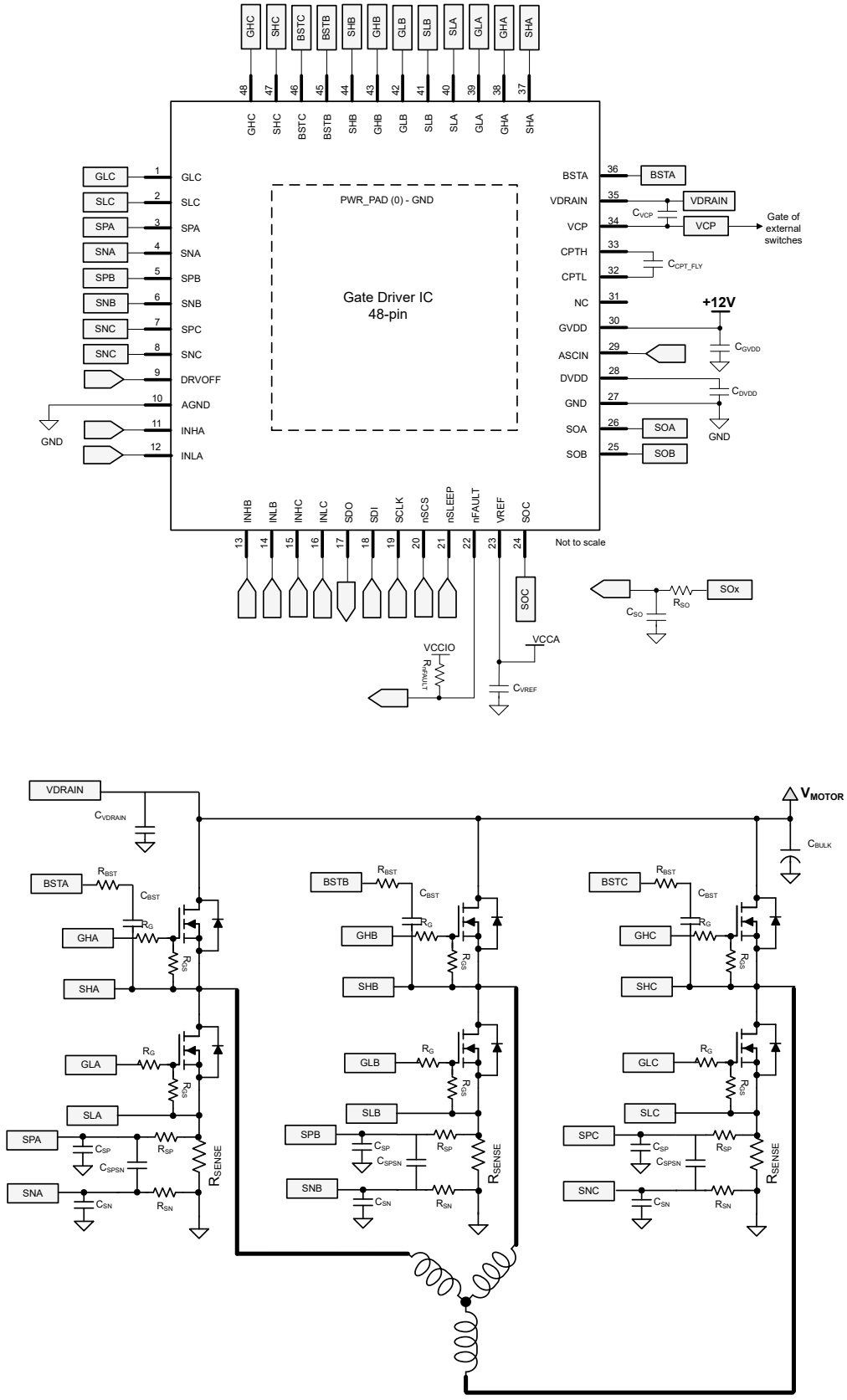

Figure 7-1. DRV8363-Q1 Typical Application Schematic

7.2.1.1 External Components

External components lists the recommended external components.

Table 7-1. External Components (48-pin Package)

COMPONENT	PIN1	PIN2	RECOMMENDED
C_{GVDD}	GVDD	GND	10-µF ceramic capacitor rated for GVDD.
C_{DVDD}	DVDD	GND	1.0-µF ceramic capacitor rated for DVDD voltage
C_{CPT_FLY}	CPTH	CPTL	1.0-µF ceramic capacitor rated for GVDD voltage
C_{VCP}	VCP	VDRAIN	1.0-µF ceramic capacitor rated for VCP voltage
R_{nFAULT}	VCCIO	nFAULT	10 kΩ pulled up the MCU I/O power supply or DVDD
C_{VREF}	VREF	GND	0.1-µF ceramic capacitor rated for VREF
C_{BULK}	V_{MOTOR}	GND	100-µF - 1000-µF rated for V_{MOTOR}; Depending on system configuration
C_{VDRAIN}	VDRAIN	GND	1-µF rated for VDRAIN
C_{BST}	BSTx	SHx	1.0-µF, 20-V ceramic capacitor between BSTx and SHx depending on the total gate charge of external MOSFET Q_g. $C_{BST} > 40 \times Q_g / (V_{GHX}-V_{SHx})$
R_{BST}	BSTx	SHx	OPTIONAL: 3-Ω series resistor between BSTx and SHx to help prevent C_{BST} from being overcharged if big negative transient voltage is observed on SHx pin.
R_G	GHx, GLx	Gate of external MOSFET	OPTIONAL: 2-Ω series resistor between GHx/GLx and Gate of external MOSFET.
R_{GS}	GHx, GLx	Source of external MOSFET	OPTIONAL: 100-kΩ pull down resistor between GHx/GLx and Source of external MOSFET.
R_{SENSE}	SPx	SNx	0.5-mΩ Shunt resistor for current sense amplifier. System design parameter.
R_{SO}	MCU ADC	SOx	160-Ω for current sense amplifier output filter
C_{SO}	MCU ADC	GND	470-pF ceramic capacitor rated for AREF for current sense amplifier output filter
R_{SP}, R_{SN}	SPx/SNx	R_{SENSE}	OPTIONAL: 10-Ω for current sense amplifier input filter.
C_{SPSN}	SPx	SNx	OPTIONAL: 1-nF ceramic capacitor for current sense amplifier input filter.
C_{SP}, C_{SN}	SPx/SNx	GND	OPTIONAL: 1-nF ceramic capacitor for current sense amplifier input filter.

7.2.2 Application Curves

Figure 7-2. Device Powerup

7.3 Layout

7.3.1 Layout Guidelines

- Minimize length and impedance of GHx, SHx, GLx, and SLx traces. Use as few vias as possible to minimize parasitic inductance. TI also recommends to increase these trace widths to 15-20mil shortly after routing away from the device pin to minimize parasitic resistance.
- Keep BSTx capacitors close to the respective pins. TI highly recommends to place this capacitor on the same side of the PCB to avoid parasitic via inductance.
- Keep CPTH/CPTL flying capacitor as close to the device pins as possible. TI highly recommends to place this capacitor on the same side of the PCB to avoid parasitic via inductance.
- Keep GVDD capacitor close to GVDD pin. TI highly recommends to place this capacitor on the same side of the PCB to avoid parasitic via inductance.
- Keep DVDD capacitor close to DVDD pin. TI highly recommends to place this capacitor on the same side of the PCB to avoid parasitic via inductance. Additionally, the GND-return connection of the DVDD capacitor is routed directly back to the adjacent GND pin to avoid adding parasitic inductance and resistance to the DVDD regulator loop.

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- VDRAIN connection is routed such that the connection observes an "average" of the three phases to help maintain VDS accuracy. TI also recommends to connect VDRAIN close to the high-side bulk capacitance to help stabilize the input to VDRAIN and avoid exceeding the pin abs max rating. Keep VDRAIN capacitor close to VDRAIN pin to supply steady switching current for the charge pump.
- Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance is placed such that the bulk capacitance minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces are as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.
- Connect SLx pins to individual MOSFET sources, not directly to GND, for accurate VDS detection and better transient resistance.
- Route SNx/SPx pins in parallel from the sense resistor to the device. Place filtering components close to the device pins to minimize post-filter noise coupling. Verify that SNx/SPx stay separated from GND plane to achieve best CSA accuracy.
- Place SO filtering components close to the MCU/ADC input to minimize post-filter noise coupling.
- The exposed pad is used for thermal dissipation, not electrical grounding, and has a high-impedance connection to the GND/AGND pins. Therefore, TI recommends to connect the exposed pad to the best thermal GND, and to connect the GND/AGND pins to the MCU-reference GND.

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

- Texas Instruments,*Understanding Smart Gate Drive (Rev. D)* application report
- Texas Instruments, *Brushless-DC Motor Driver Considerations and Selection Guide (Rev. A) application report*
- Texas Instruments, *Designing High-Side and 3-Phase Isolator MOSFET Circuits in Motor Apps* application note
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers (Rev. B)* application note
- Texas Instruments,*PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments,*PowerPAD™ Made Easy* application report
- Texas Instruments,*Sensored 3-Phase BLDC Motor Control Using MSP430* application report
- Texas Instruments, *Hardware Design Considerations for an Electric Bicycle Using a BLDC Motor* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

8.4 Trademarks

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial release.

ADVANCE INFORMATION

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

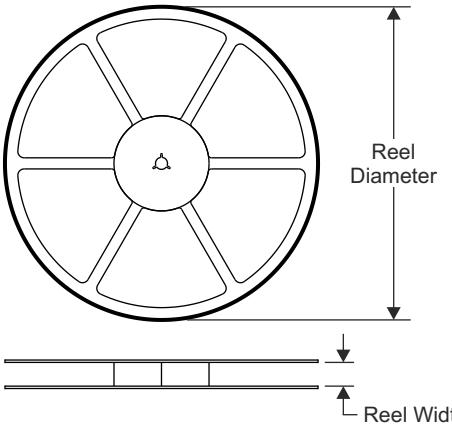
PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8363RGZR	Active	Preproduction	VQFN (RGZ) | 48	1000 | TRAY	Yes	NiPdAu	Level-3-260C-168 HR	-40 to 125	DRV8363

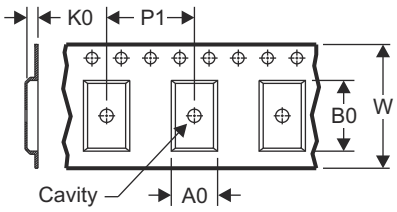
(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

10.1 Tape and Reel Information

REEL DIMENSIONS

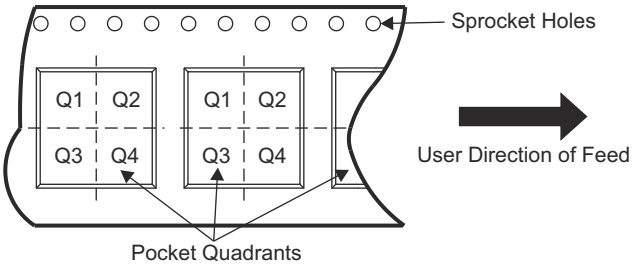


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

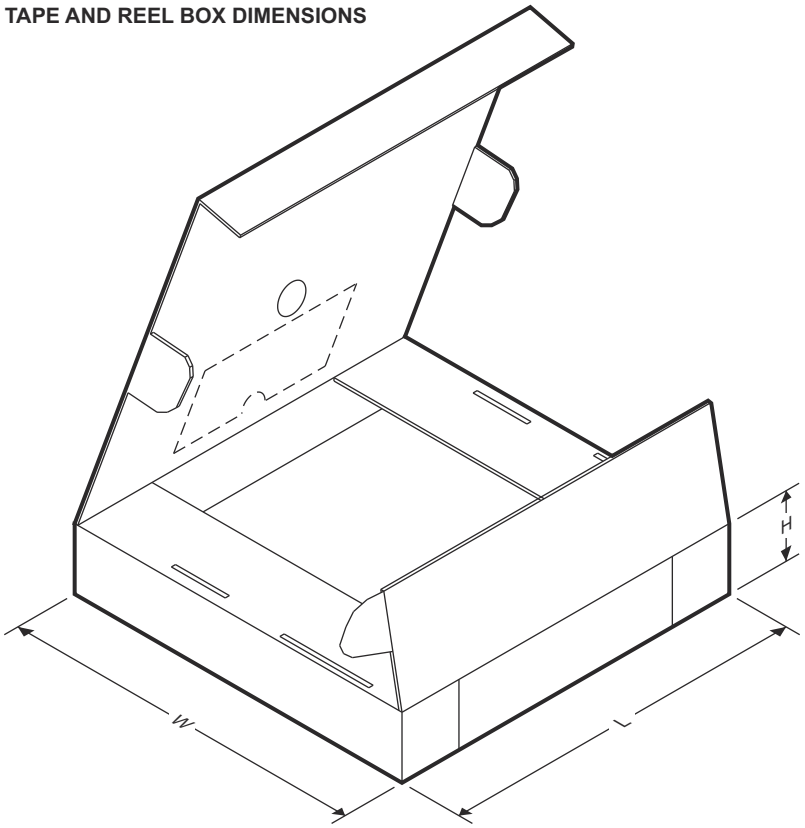
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8363RGZR	VQFN	RGZ	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PDRV8363QRGZRQ1	VQFN	RGZ	48	1000	336.6	336.6	31.8

ADVANCE INFORMATION

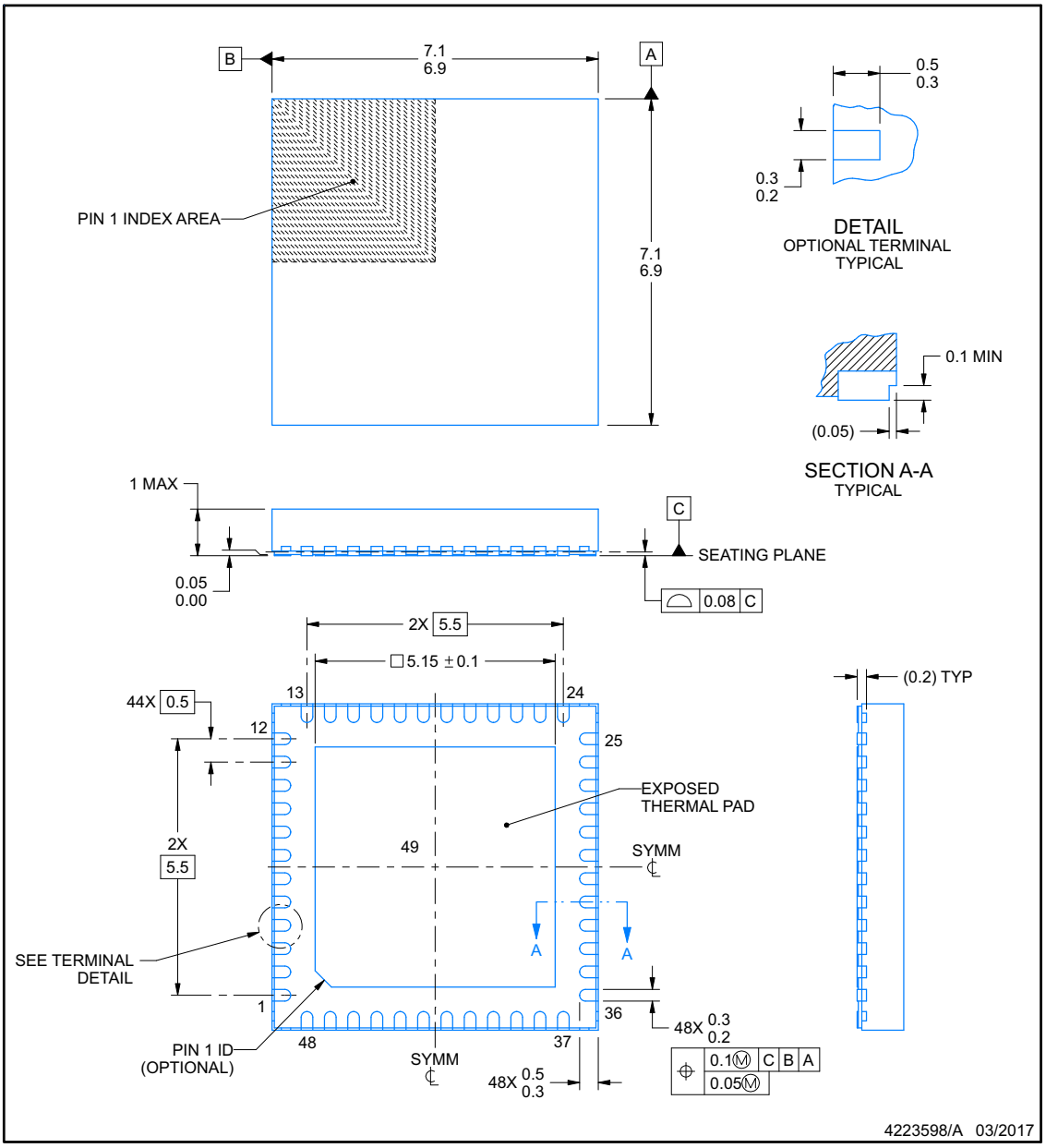
ADVANCE INFORMATION

PACKAGE OUTLINE

RGZ0048N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

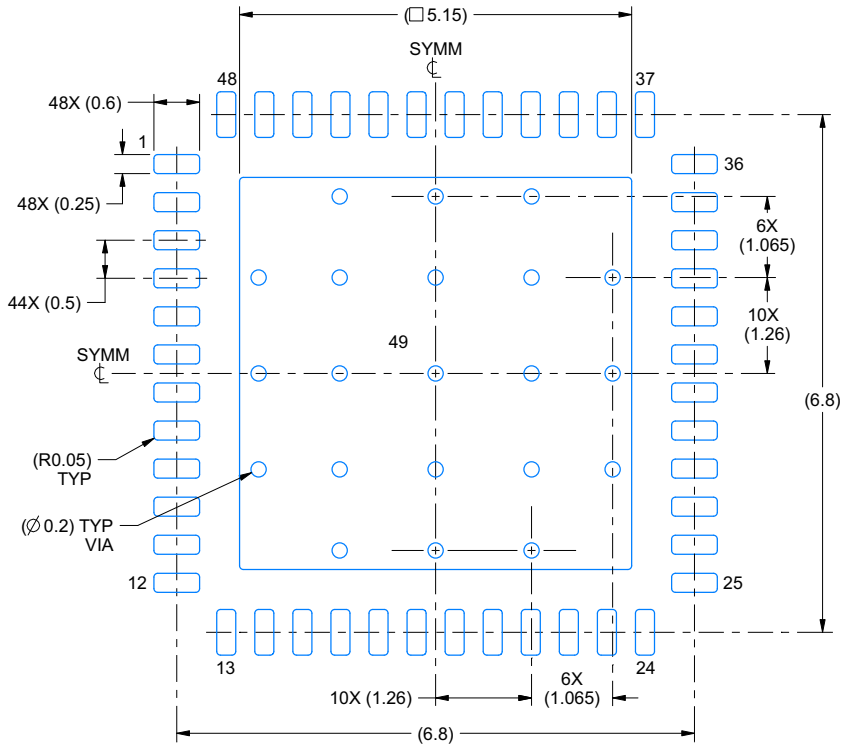
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

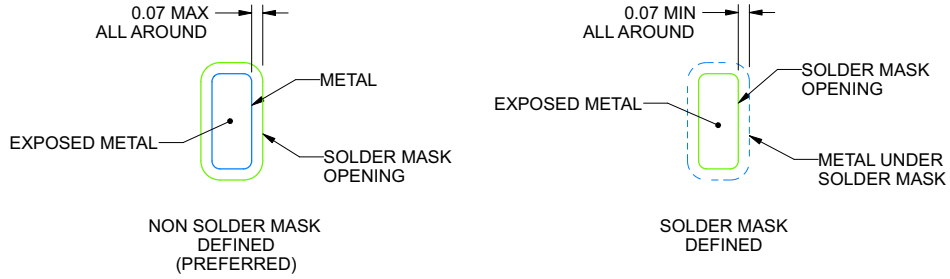
RGZ0048N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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NOTES: (continued)

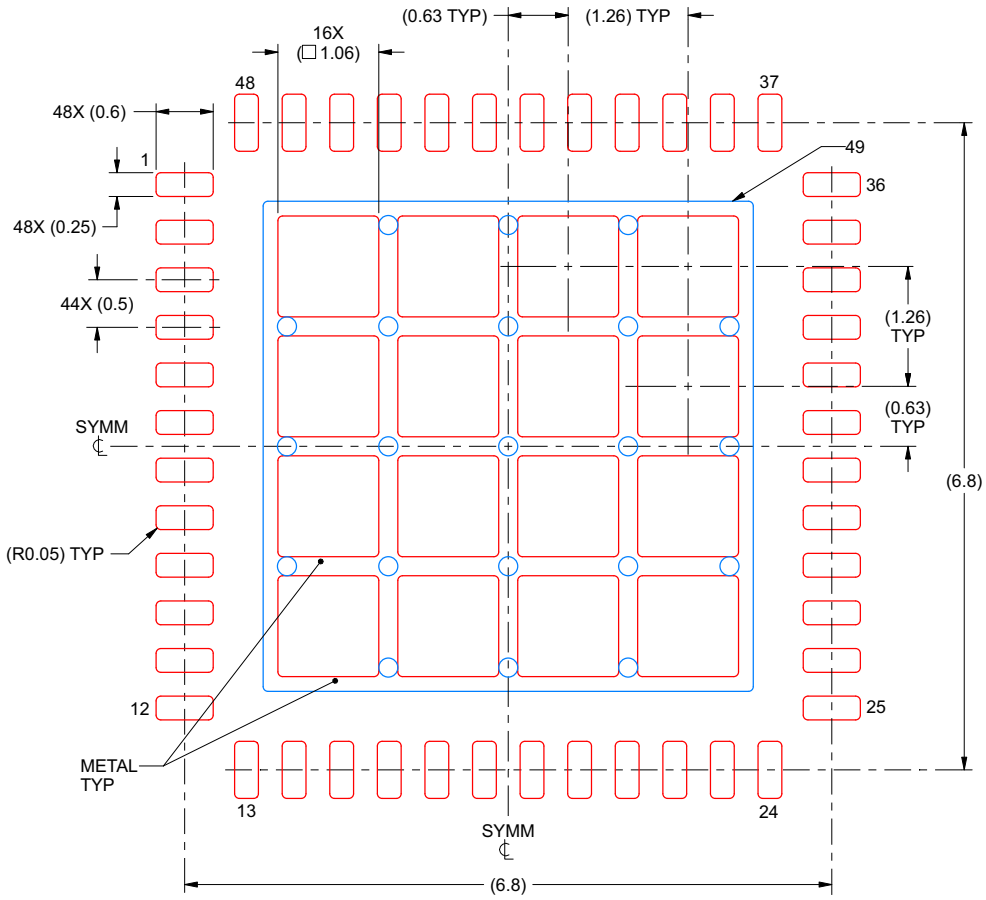
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGZ0048N — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDRV8363QRGZRQ1	Active	Preproduction	VQFN (RGZ) | 48	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

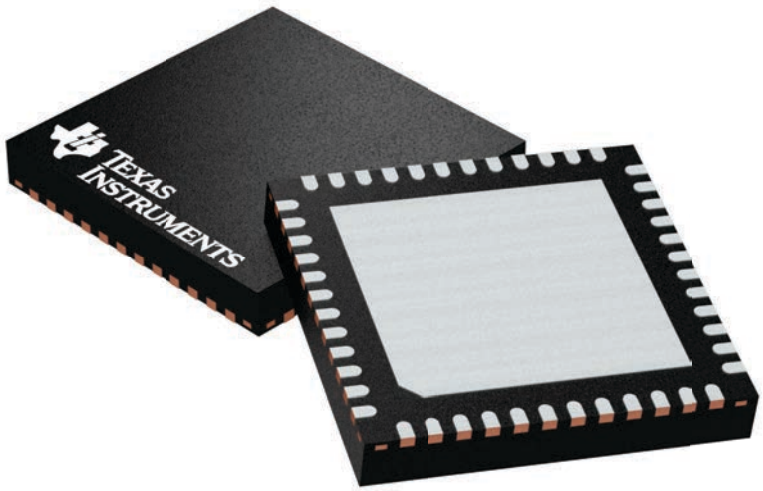
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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