DRV8000-Q1 Automotive Highly-Integrated, Multifunction Driver for Door Control

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Compliant Targeted
  - Developed for functional safety applications
  - Documentation to aid ISO26262 system design
  - Systematic integrity up to ASIL D
  - Hardware integrity up to ASIL B
- 5V to 35V (40V abs. max) operating range
- H-bridge or dual-channel half-bridge gate drivers
  - Smart gate drive architecture
  - Tripler charge pump for 100% PWM
  - Wide common mode current shunt amplifier
- 1 Integrated half-bridge with I_{OUT} max 8A (R_{DSON} HS +LS FET = 155mΩ)
- 1 Integrated half-bridge with I_{OUT} max 7A (R_{DSON} HS +LS FET = 185mΩ)
- 2 Integrated half-bridges with I_{OUT} max 4A (R_{DSON} HS +LS FET = 440mΩ)
- 2 Integrated half-bridges with I_{OUT} max 1.3A load (R_{DSON} HS +LS FET = 1540mΩ)
- 1 Configurable integrated high-side driver as lamp or LED driver with I_{OUT} Max 1.5/0.5A (R_{DSON} = 0.4/1.2Ω)
- 5 Configurable integrated high-side drivers for 0.5/0.25A load (R_{DSON} = 1.2Ω)
- 1 External MOSFET gate driver for charge of electrochromic glass
- 1 Integrated low-side FET for discharge of electrochromic glass
- Internal 10bit PWM generator for high-side drivers
- All high-side drivers support a low- or high- current threshold constant current mode to drive a wide range of LED modules
- 1 external MOSFET gate driver for heater
  - Offline open load detection
  - V_{DS} monitoring of low R_{DSON} MOSFET for short-circuit detection
- Integrated driver output features current regulation (ITRIP)
- Muxable sense output (IPROPI)
  - Internal current sensing with proportional current output (IPROPI)
  - Advanced die temperature monitoring with multiple thermal clusters
  - Motor supply voltage monitor
- Protection and diagnostic features with configurable fault behavior
  - Load diagnostics in both the off-state and on-state to detect open load and short-circuit
  - Overcurrent and over temperature protection
- Device Comparison Table

2 Applications

- Door module
- Body control modules
- Zonal module

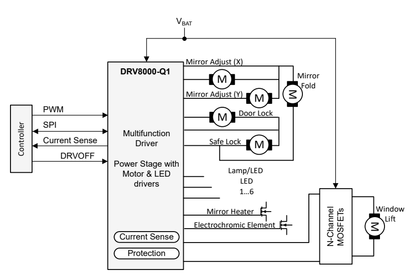
3 Description

The DRV8000-Q1 device integrates multiple door control specific functions: driving and diagnosing motor (inductive), resistive and capacitive loads, driving a lamp or LEDs, drive MOSFETs for special loads such as heating element or electrochromic elements. These drivers include protection features for offline and active diagnostics such as under and over voltage monitors, offline open load and short-circuit diagnostics, and zone-based thermal monitoring and shutdown protection. The device features two half-bridge gate drivers, 6 integrated half-bridges (2 high-side alternate modes), 6 integrated high-side drivers, one external high-side gate driver for heater, one external high-side gate driver for electrochromic charge and one integrated low-side driver for electrochromic load discharge. The half-bridge, high-side, heater and gate drivers have PWM input control configuration, sensing, diagnostics and device system protection. There is a dedicated internal programmable PWM generators for each high-side driver. Proportional current sense pin output is available for all integrated drivers, along with a robust and flexible current shunt amplifier for the gate driver.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)(2)
DRV8000-Q1	VQFN (48)	7.00mm × 7.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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4 Device Comparison

Table 4-1. Device Comparison

Device Name	H-Bridge Gate Driver	Half-bridge Driver	High-side Driver	Lamp/LED HS Driver	EC Gate Driver	Heater HS Gate Driver	Current Shunt Amp	Package
DRV8000-Q1	1x	6x	5x	1x	1x	1x	1x	7x7 QFN-48 Wettable Flank
DRV8001-Q1	X	6x	5x	1x	1x	1x	X	6x6 QFN-40 Wettable Flank
DRV8002-Q1	1x	6x	5x	1x	X	X	1x	7x7 QFN-48 Wettable Flank

Table 4-2. Device Orderable Information

Device	Pre-production Part Number	Orderable Part Number	EVM
DRV8000-Q1	PDRV8000QWRGZRQ1 P2DRV8000QWRGZRQ1	DRV8000QWRGZRQ1	DRV8000-Q1EVM
DRV8001-Q1	PDRV8001QWRHARQ1	DRV8001QWRHARQ1	DRV8001-Q1EVM
DRV8002-Q1	PDRV8002QRGZRQ1 P2DRV8002QWRGZRQ1	DRV8002QWRGZRQ1	DRV8000-Q1EVM

5 Pin Configuration and Functions

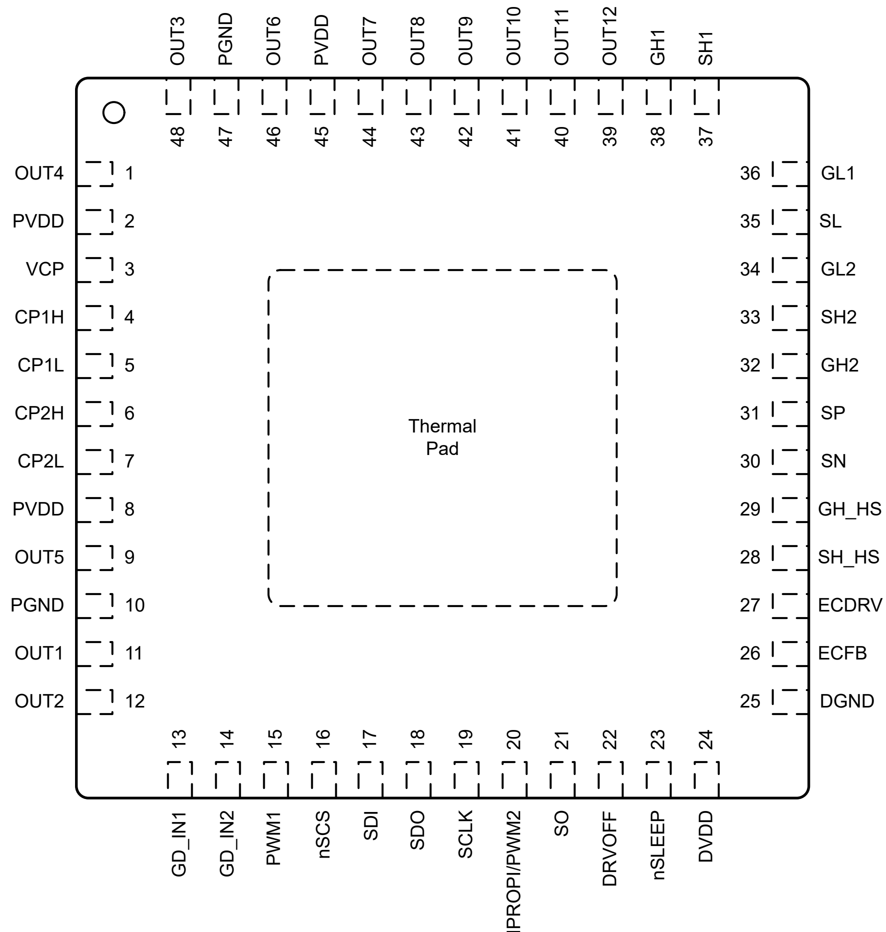

Figure 5-1. VQFN (RGZ) 48-Pin Package and Pin Functions

Table 5-1. Pin Functions

PIN		I/O[1]	TYPE	DESCRIPTION
NO.	NAME			
1	OUT4	O	Power	440mΩ half-bridge output 4.
2	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10µF between PVDD and GND pins.
3	VCP	I/O	Power	Charge pump output. Connect a 1µF, 16V ceramic capacitor between VCP and PVDD pins.
4	CP1H	I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP1H and CP1L pins.
5	CP1L	I/O	Power	
6	CP2H	I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP2H and CP2L pins.
7	CP2L	I/O	Power	
8	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10µF between PVDD and GND pins.
9	OUT5	O	Power	155mΩ half-bridge output 5.
10	PGND	I/O	Ground	Device ground. Connect to system ground.
11	OUT1	O	Power	1.54Ω half-bridge output 1.

Table 5-1. Pin Functions (continued)

PIN NO.	PIN NAME	I/O[(1)]	TYPE	DESCRIPTION
12	OUT2	O	Power	1.54Ω half-bridge output 2.
13	GD_IN1	I	Digital	Gate Driver Half-bridge and H-bridge control input 1.
14	GD_IN2	I	Digital	Gate Driver Half-bridge and H-bridge control input 2.
15	PWM1	I	Digital	PWM input 1 for regulation of all drivers except electrochrome and Gate Drivers.
16	nSCS	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor.
17	SDI	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.
18	SDO	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
19	SCLK	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.
20	IPROPI/PWM2	I/O	Analog	Sense output is multiplexed from any of driver load current feedback, PVDD voltage feedback, or thermal cluster temperature feedback. Can also be configured as second PWM pin input for half-bridge drivers.
21	SO	O	Analog	Shunt amplifier output.
22	DRVOFF	I	Analog	Gate driver shutdown pin. Logic high to pulldown both high-side and low-side gate driver outputs. Internal pulldown resistor.
23	nSLEEP	I	Analog	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.
24	DVDD	I	Power	Device logic and digital output power supply input. Recommended to connect a 1.0µF, 6.3V ceramic capacitor between the DVDD and GND pins.
25	DGND	I/O	Ground	Device ground. Connect to system ground.
26	ECFB	I/O	Power	For EC control, pin is used as voltage monitor input and fast discharge low-side switch. If the EC drive function is not used, connect this pin to GND through 10kΩ resistor.
27	ECDRV	O	Analog	For EC control, pin controls the gate of external MOSFET for EC voltage regulation
28	SH_HS	I	Analog	Source pin of high-side heater MOSFET and output to heater load. Connect to source of high-side MOSFET.
29	GH_HS	O	Analog	Gate driver output for heater MOSFET. Connect to gate of high-side MOSFET.
30	SN	I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor. Additional filtering is not recommended to the input of the Shunt Amplifier.
31	SP	I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor. Additional filtering is not recommended to the input of the Shunt Amplifier.
32	GH2	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET. Gate drive series resistance is not recommended as the impact crossover transition timing.
33	SH2	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
34	GL2	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
35	SL	I	Analog	Low-side MOSFET gate drive sense and power return. Connect to system ground with low impedance path to the low-side MOSFET ground return.
36	GL1	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
37	SH1	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
38	GH1	O	Power	High-side gate driver output. Connect to the gate of the high-side MOSFET. Gate drive series resistance is not recommended as the impact crossover transition timing.
39	OUT12	O	Power	1.2Ω high-side driver output 12. Connect to low-side load.

Table 5-1. Pin Functions (continued)

PIN NO.	PIN NAME	I/O[1]	TYPE	DESCRIPTION
40	OUT11	O	Power	1.2Ω high-side driver output 11. Configurable as SC protection switch for EC drive. Connect to low-side load.
41	OUT10	O	Power	1.2Ω high-side driver output 10. Connect to low-side load.
42	OUT9	O	Power	1.2Ω high-side driver output 9. Connect to low-side load.
43	OUT8	O	Power	1.2Ω high-side driver output 8. Connect to low-side load.
44	OUT7	O	Power	High-side driver output with configurable R_{DSON} (400mΩ/1200mΩ). Connect to low-side load.
45	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10µF between PVDD and GND pins.
46	OUT6	O	Power	185mΩ half-bridge output 6.
47	PGND	I/O	Ground	Device ground. Connect to system ground.
48	OUT3	O	Power	440mΩ half-bridge output 3.

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	–0.3	40	V
Power supply transient voltage ramp	PVDD		2	V/µs
Digital Logic power supply voltage ramp	DVDD		2	V/µs
Voltage difference between ground pins	GND, PGND	–0.3	0.3	V
Charge pump pin voltage	VCP	–0.3	PVDD + 15	V
Charge pump high-side pin voltage	CP1H	V_{PVDD} – 0.3	V_{VCP} + 0.3	V
Charge pump high-side pin voltage	CP2H	V_{PVDD} – 0.6	V_{VCP} + 0.3	V
Charge pump low-side pin voltage	CP1L, CP2L	–0.3	V_{PVDD} + 0.3	V
Digital regulator pin voltage	DVDD	–0.3	5.75	V
Logic pin voltage	GD_INx, PWM1, IPROPI/PWM2, DRVOFF, nSLEEP, SCLK, SDI, nSCS	–0.3	5.75	V
Output logic pin voltage	SDO	–0.3	V_{DVDD} + 0.3	V
Output pin voltage	OUT1-OUT12	–0.3	V_{PVDD} + 0.9	V
Output current	OUT1-OUT12, ECFB, ECDRV	Internally Limited	Internally Limited	A
Heater and Electrochromic MOSFET gate drive pin voltage	GH_HS	V_{SH_HS} – 0.3 to V_{SH_HS} + 13	V_{VCP} + 0.3	V
Heater and Electrochromic MOSFET source pin voltage	SH_HS, ECFB, ECDRV	–0.3	V_{PVDD} + 0.3	V
High-side driver and Heater MOSFET source pin maximum energy dissipation, T_J = 25°C, L_{LOAD} < 100 µH	OUT7-OUT12, SH_HS	-	1	mJ
High-side gate drive pin voltage	GHx (2)	–2	V_{VCP} + 0.3	V
Transient 1-µs high-side gate drive pin voltage	GHx (2)	–5	V_{VCP} + 0.3	V
High-side gate drive pin voltage with respect to SHx	GHx (2)	–0.3	13.5	V
High-side sense pin voltage	SHx (2)	–2	40	V
Transient 1-µs high-side sense pin voltage	SHx (2)	–5	40	V
Low-side gate drive pin voltage	GLx (2)	–2	13.5	V
Transient 1-µs low-side gate drive pin voltage	GLx (2)	–3	13.5	V
Low-side gate drive pin voltage with respect to SL	GLx (2)	–0.3	13.5	V
Low-side sense pin voltage	SL (2)	–2	2	V
Transient 1-µs low-side sense pin voltage	SL (2)	–3	3	V
Gate drive current	GHx, GLx	Internally Limited	Internally Limited	A
Amplifier input pin voltage	SN, SP	–2	V_{VCP} + 0.3	V
Transient 1-µs amplifier input pin voltage	SN, SP	–5	V_{VCP} + 0.3	V
Amplifier input differential voltage	SN, SP	–5.75	5.75	V
Amplifier output pin voltage	SO	–0.3	V_{DVDD} + 0.3	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) PVDD with respect to GHx, SHx, GLx, or SL should not exceed 40 V. When PVDD is greater than 35 V, negative voltage on GHx, SHx GLx, and SL should be limited to ensure this rating is not exceeded. When PVDD is less than 35 V, the full negative rating of GHx, SHx, GLx, and SL is available.

6.2 ESD Ratings Auto

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD[1] Classification Level 2	PVDD, OUT1 - OUT12, ECFB, GND	±4000	V
			All other pins	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Power supply voltage	PVDD	5		35	V
I_{HS} [1]	High-side average gate-drive current	GHx	0		15	mA
I_{LS} [1]	Low-side average gate-drive current	GLx	0		15	mA
V_{DVDD}	Logic input voltage	DVDD	3.1		5.5	V
V_{DIN}	Digital input voltage	GD_INx, PWM1, IPROPI/PWM2, DRVOFF, SO, SCLK, SDI	0		5.5	V
I_{DOUT}	Digital output current	SDO	0		5	mA
f_{PWM}	Input PWM frequency	PWM1, IPROPI/PWM2	0		25	kHz
V_{IPROPI}	Analog output voltage for V_{PVDD} > 7 V	IPROPI (IPROPI/PWM2 pin)	0		5.2	V
V_{IPROPI}	Analog output voltage for V_{PVDD} < 7 V	IPROPI (IPROPI/PWM2 pin)	0		V_{PVDD} - 1.8	V
I_{SO}	Shunt amplifier output current	SO	0		5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information RGZ package

THERMAL METRIC[1]		RGZ Package	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DVDD, VCP, PVDD)						
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} = 13.5 V, nSLEEP = 0 V -40 ≤ T_J ≤ 85˚C		3.5	5.5	µA
I_{DVDDQ}	DVDD sleep mode current	V_{PVDD} = 13.5 V, nSLEEP = 0 V -40 ≤ T_J ≤ 85˚C		3	4	µA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 13.5, nSLEEP = V_{DVDD}		8.7	14.5	mA
I_{PVDD}	PVDD active mode current, reduced options.	V_{PVDD} = 13.5, nSLEEP = V_{DVDD}; Charge pump in doubler mode.		7	11.5	mA
I_{DVDD}	DVDD active mode current	SDO = 0 V		5	8.5	mA
I_{DVDD}	DVDD active mode current, reduced options	SDO = 0 V; Charge pump in doubler mode.		3.3	7	mA
$I_{PVDD\_CP\_DIS}$	PVDD charge pump disabled mode current	V_{PVDD} = 13.5 V, DIS_CP = 1, EN_GD = 0, HEAT_EN = 0, EC_ON = 0, OUTx_EN = 0		1.2	4.5	mA
$I_{DVDD\_CP\_DIS}$	DVDD charge pump disabled mode current	V_{PVDD} = 13.5 V, DIS_CP = 1, EN_GD = 0, HEAT_EN = 0, EC_ON = 0, OUTx_EN = 0		3.4	8.5	mA
t_{WAKE}	Turnon time	nSLEEP = V_{DVDD} to active mode		670	850	µs
t_{SLEEP}	Turnoff time	nSLEEP = 0 V to sleep mode			1	ms
t_{DRVOFF_FLTR}	Filter time for DRVOFF signal asserted	DRVOFF = 0 V to V_{DVDD}		15		µs
f_{VDD}	Digital oscillator switching frequency	Primary frequency of spread spectrum	12.83	14.25	15.68	MHz
f_{VDD}	Digital oscillator spread spectrum range	Center spread on primary frequency	-7		7	%
V_{VCP}	Charge pump regulator voltage with respect to PVDD	V_{PVDD} ≥ 9 V, I_{VCP} ≤ 20 mA	9.5	10.5	12.5	V
V_{VCP}	Charge pump regulator voltage with respect to PVDD	V_{PVDD} = 7 V, I_{VCP} ≤ 15 mA	8.5	9	12	V
V_{VCP}	Charge pump regulator voltage with respect to PVDD	V_{PVDD} = 5 V, I_{VCP} ≤ 12 mA	6.8	7.5	11	V
t_{CP_tran}	Charge pump transition time between doubler and tripler mode				300	µs
t_{CP_EN}	Charge pump turn on time after enable command. Includes initialization.			500	550	µs
I_{VCP_LIM}	Charge pump output current limit	V_{PVDD} = 13.5 V, C_{FLY1} = C_{FLY2} = 100 nF, C_{VCP} = 1 µF, inrush during charge pump start-up			500	mA
f_{VCP}	Charge pump switching frequency	Primary frequency of spread spectrum		400		kHz
LOGIC-LEVEL INPUTS (INx, nSLEEP, SCLK, SDI, etc)						
V_{IL}	Input logic low voltage	DRVOFF, GD_INx, PWM1, IPROPI/PWM2, nSLEEP, SCLK, SDI	0.3		V_{DVDD} x 0.3	V
V_{IH}	Input logic high voltage	DRVOFF, GD_INx, PWM1, IPROPI/PWM2, nSLEEP, SCLK, SDI	V_{DVDD} x 0.7		5.5	V
V_{HYS}	Input hysteresis	DRVOFF, GD_INx, PWM1, IPROPI/PWM2, nSLEEP, SCLK, SDI		V_{DVDD} x 0.15		V
I_{IL}	Input logic low current	V_{DIN} = 0 V, DRVOFF, GD_INx, PWM1, IPROPI/PWM2, nSLEEP, SCLK, SDI	–5		5	µA
I_{IL}	Input logic low current	V_{DIN} = 0 V, nSCS		25	50	µA
I_{IH}	Input logic high current	V_{DIN} = V_{DVDD}, nSCS	–5		5	µA

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic high current	V_{DIN} = V_{DVDD}, DRVOFF, GD_INx, PWM1, IPROPI/PWM2, nSLEEP, SCLK, SDI		25	50	µA
R_{PD}	Input pulldown resistance	To GND, DRVOFF, GD_INx, PWM1, IPROPI/PWM2, nSLEEP, SCLK, SDI	140	200	260	kΩ
R_{PU}	Input pullup resistance	To DVDD, nSCS	140	200	265	kΩ
PUSH-PULL OUTPUT SDO						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.5	V
V_{OH}	Output logic high voltage	I_{OD} = –5 mA, SDO	DVDD x 0.8			V
GATE DRIVERS (GHx, GLx, SHx, SL)						
V_{GHx_L}	GHx low level output voltage	I_{DRVN_HS} = I_{STRONG}, I_{GHx} = 1mA, GHx to SHx	0		0.25	V
V_{GLx_L}	GLx low level output voltage	I_{DRVN_LS} = I_{STRONG}, I_{GLx} = 1mA, GLx to SL	0		0.25	V
V_{GHx_H}	GHx high level output voltage	I_{DRVP_HS} = I_{HOLD}, I_{GHx} = 1mA, VCP to GHx	0		0.25	V
V_{GLx_H}	GLx high level output voltage	I_{DRVP_LS} = I_{HOLD}, I_{GLx} = 1mA ,10.5 V ≤ V_{PVDD} ≤ V_{PVDD_OV} , GLx to SL. Gate driver turned off if V_{PVDD} > V_{PVDD_OV}	9.35	10.5	12.5	V
I_{DRVP}	Peak gate current (source)	IDRVP_x = 0000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.2	0.5	0.83	mA
		IDRVP_x = 0001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.5	1	1.6	mA
		IDRVP_x = 0010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	1.3	2	2.8	mA
		IDRVP_x = 0011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.1	3	4	mA
		IDRVP_x = 0100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.9	4	5.3	mA
		IDRVP_x = 0101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	3.7	5	6.45	mA
		IDRVP_x = 0110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	4.45	6	7.65	mA
		IDRVP_x = 0111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	5.5	7	9	mA
		IDRVP_x = 1000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	5.6	8	10.2	mA
		IDRVP_x = 1001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	8.8	12	15.2	mA
		IDRVP_x = 1010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	11.6	16	20.4	mA
		IDRVP_x = 1011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	16	20	25.4	mA
		IDRVP_x = 1100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	17.6	24	30.4	mA
		IDRVP_x = 1101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	24	31	40	mA
		IDRVP_x = 1110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	28	48	62	mA
		IDRVP_x = 1111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	46	62	78	mA

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRVN}	Peak gate current (sink)	IDRVN_x = 0000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.07	0.5	0.85	mA
		IDRVN_x = 0001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.23	1	1.7	mA
		IDRVN_x = 0010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.7	2	3.2	mA
		IDRVN_x = 0011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	1.2	3	4.6	mA
		IDRVN_x = 0100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	1.75	4	5.9	mA
		IDRVN_x = 0101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.4	5	7.2	mA
		IDRVN_x = 0110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	3	6	8.5	mA
		IDRVN_x = 0111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	3.6	7	9.8	mA
		IDRVN_x = 1000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	4.3	8	11	mA
		IDRVN_x = 1001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	7.3	12	16	mA
		IDRVN_x = 1010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	10.6	16	20.4	mA
		IDRVN_x = 1011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	14	20	25.3	mA
		IDRVN_x = 1100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	17.8	24	30.2	mA
		IDRVN_x = 1101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	23.8	31	40.2	mA
		IDRVN_x = 1110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	27	48	63	mA
		IDRVN_x = 1111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	45	62	79	mA
I_{HOLD}	Gate pullup hold current	Gate hold source current, V_{GSx} = 3 V	5	16	30	mA
I_{STRONG}	Gate pulldown strong current	V_{GSx} = 3 V I_{DRV} = 0.5 to 12 mA	30	62	100	mA
I_{STRONG}	Gate pulldown strong current	V_{GSx} = 3 V I_{DRV} = 16 to 62 mA	45	128	200	mA
R_{PDSA_LS}	Low-side semi-active gate pulldown	GLx to SL, V_{GSx} = 3 V		1.8		kΩ
R_{PDSA_LS}	Low-side semi-active gate pulldown	GLx to SL, V_{GSx} = 1 V		5		kΩ
R_{PD_HS}	High-side passive gate pulldown resistor	GHx to SHx		150		kΩ
R_{PD_LS}	Low-side passive gate pulldown resistor	GLx to SL		150		kΩ
I_{SHx}	Switch-node sense leakage current	Into SHx, SHx = PVDD < 28 V GHx - SHx = 0 V, nSLEEP = 0 V	–5	0	20	µA
GATE DRIVER TIMINGS (GHx, GLx)						
t_{PDR_LS}	Low-side rising propagation delay	Input to GLx rising		300	850	ns
t_{PDF_LS}	Low-side falling propagation delay	Input to GLx falling		300	600	ns
t_{PDR_HS}	High-side rising propagation delay	Input to GHx rising		300	600	ns
t_{PDF_HS}	High-side falling propagation delay	Input to GHx rising		300	600	ns
t_{DEAD}	Internal handshake dead-time	GLx/GHx falling 10% to GHx/GLx rising 10%		350		ns

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DEAD_D}	Insertable digital dead-time	VGS_TDEAD = 00b, Handshake only		0		µs
		VGS_TDEAD = 01b	1.6	2	2.4	µs
		VGS_TDEAD = 10b	3.4	4	4.6	µs
		VGS_TDEAD = 11b	6	8	10	µs
CURRENT SHUNT AMPLIFIERS (SN, SO, SP)						
V_{COM}	Common mode input range		–2		V_{PVDD} + 2	V
G_{CSA}	Sense amplifier gain	CSA_GAIN = 00b	9.75	10	10.25	V/V
		CSA_GAIN = 01b	19.5	20	20.5	V/V
		CSA_GAIN = 10b	38.8	40	41.2	V/V
		CSA_GAIN = 11b	77.6	80	82.4	V/V
t_{SET}	Sense amplifier settling time to 1%	V_{SO_STEP} = 1.5 V, G_{CSA} = 10 V/V C_{SO} = 60 pF		2.2		µs
		V_{SO_STEP} = 1.5 V, G_{CSA} = 20 V/V C_{SO} = 60 pF		2.2		µs
		V_{SO_STEP} = 1.5 V, G_{CSA} = 40 V/V C_{SO} = 60 pF		2.2		µs
		V_{SO_STEP} = 1.5 V, G_{CSA} = 80 V/V C_{SO} = 60 pF		3		µs
t_{BLK_CSA}	Sense amplifier output blanking time (% of Gate driver TDRIVE)	CSA_BLK = 000b		0		%
		CSA_BLK = 001b		25		%
		CSA_BLK = 010b		37.5		%
		CSA_BLK = 011b		50		%
		CSA_BLK = 100b		62.5		%
		CSA_BLK = 101b		75		%
		CSA_BLK = 110b		87.5		%
		CSA_BLK = 111b		100		%
t_{SLEW_CSA}	Output slew rate	C_{SO} = 60 pF		2.5		V/µs
V_{BIAS}	Output voltage bias	V_{SPx} = V_{SNx} = 0 V, CSA_DIV = 0b		V_{DVDD} / 2		V
		V_{SPx} = V_{SNx} = 0 V, CSA_DIV = 1b		V_{DVDD} / 8		V
V_{LINEAR}	Linear output voltage range	V_{DVDD} = 3.3 V = 5 V	0.25		V_{DVDD} – 0.25	V
V_{OFF}	Input offset voltage	V_{SPx} = V_{SNx} = 0V, T_J = 25˚C	–1		1	mV
V_{OFF_D}	Input offset voltage drift	V_{SPx} = V_{SNx} = 0 V		±10	±25	µV/˚C
I_{BIAS}	Input bias current	V_{SPx} = V_{SNx} = 0 V			100	µA
I_{BIAS_OFF}	Input bias current offset	I_{SPx} - I_{SNx}			100	µA
CMRR	Common mode rejection ratio	DC, –40 ≤ T_J ≤ 125˚C	72	90		dB
		DC, –40 ≤ T_J ≤ 150˚C	69	90		dB
		20kHz		80		dB
PSRR	Power supply rejection ratio	PVDD to SOx, DC		100		dB
		PVDD to SOx, 20kHz		90		dB
		PVDD to SOx, 400kHz		70		dB
GATE DRIVER PROTECTION CIRCUITS						
V_{CP_UV}	Charge pump undervoltage threshold	V_{VCP} - V_{PVDD}, V_{VCP} falling VCP_UV_MODE = 0b	4	4.75	5.5	V
		V_{VCP} - V_{PVDD}, V_{VCP} falling VCP_UV_MODE = 1b	5.5	6.25	7	V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CP\_UV\_DG}$	Charge pump undervoltage deglitch time		8	10	12.75	µs
V_{CP_SO}	Charge pump tripler to doubler switch over threshold	V_{PVDD} rising	17.75	18.75	19.75	V
V_{CP_SO}	Charge pump tripler to doubler switch over threshold	V_{PVDD} falling	16.75	17.75	18.75	V
$t_{CP\_SO\_HYS}$	Charge pump tripler to doubler switch over hysteresis			1.15		V
$t_{CP\_SO\_DG}$	Charge pump tripler to doubler switch over threshold deglitch		8	10	12.75	µs
V_{GS_CLP}	High-side driver VGS protection clamp		12.5	15	17	V
V_{GS_LVL}	Gate voltage monitor threshold	V_{GHx} – V_{SHx}, V_{GLx} – V_{PGND}, VGS_LVL = 0b	1.1	1.4	1.75	V
		V_{GHx} – V_{SHx}, V_{GLx} – V_{PGND}, VGS_LVL = 1b	0.75	1	1.2	V
$t_{GS\_FLT\_DG}$	V_{GS} fault monitor deglitch time		1.5	2	2.75	µs
$t_{GS\_HS\_DG}$	V_{GS} handshake monitor deglitch time			210		ns
t_{DRIVE}	V_{GS} and V_{DS} monitor blanking time	VGS_TDRV = 000b	1.5	2	2.5	µs
		VGS_TDRV = 001b	3.25	4	4.75	µs
		VGS_TDRV = 010b	6	8	10	µs
		VGS_TDRV = 011b	10	12	14	µs
		VGS_TDRV = 100b	14	16	18	µs
		VGS_TDRV = 101b	20	24	28	µs
		VGS_TDRV = 110b	28	32	36	µs
		VGS_TDRV = 111b	80	96	120	µs

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DS_LVL}	V_{DS} overcurrent protection threshold (DRV800x-Q1 Independent Half-bridge mode)	VDS_LVL_x = 0000b, BRG_MODE = 00b	0.050	0.062	0.074	V
		VDS_LVL_x = 0001b, BRG_MODE = 00b	0.070	0.084	0.098	V
		VDS_LVL_x = 0010b, BRG_MODE = 00b	0.089	0.105	0.123	V
		VDS_LVL_x = 0011b, BRG_MODE = 00b	0.108	0.127	0.147	V
		VDS_LVL_x = 0100b, BRG_MODE = 00b	0.128	0.148	0.170	V
		VDS_LVL_x = 0101b, BRG_MODE = 00b	0.147	0.169	0.195	V
		VDS_LVL_x = 0110b, BRG_MODE = 00b	0.166	0.191	0.218	V
		VDS_LVL_x = 0111b, BRG_MODE = 00b	0.185	0.212	0.243	V
		VDS_LVL_x = 1000b, BRG_MODE = 00b	0.278	0.318	0.363	V
		VDS_LVL_x = 1001b, BRG_MODE = 00b	0.372	0.425	0.483	V
		VDS_LVL_x = 1010b, BRG_MODE = 00b	0.466	0.532	0.605	V
		VDS_LVL_x = 1011b, BRG_MODE = 00b	0.562	0.638	0.725	V
		VDS_LVL_x = 1100b, BRG_MODE = 00b	0.655	0.745	0.847	V
		VDS_LVL_x = 1101b, BRG_MODE = 00b	0.942	1.066	1.208	V
		VDS_LVL_x = 1110b, BRG_MODE = 00b	1.322	1.494	1.692	V
		VDS_LVL_x = 1111b, BRG_MODE = 00b	1.890	2.132	2.411	V
V_{DS_LVL}	V_{DS} overcurrent protection threshold (DRV800x-Q1 H-bridge mode with matching VDS_LVLx setting, DRV800xE-Q1 all modes)	VDS_LVL_x = 0000b	0.051	0.06	0.069	V
		VDS_LVL_x = 0001b	0.068	0.08	0.092	V
		VDS_LVL_x = 0010b	0.085	0.10	0.115	V
		VDS_LVL_x = 0011b	0.102	0.12	0.138	V
		VDS_LVL_x = 0100b	0.119	0.14	0.161	V
		VDS_LVL_x = 0101b	0.136	0.16	0.184	V
		VDS_LVL_x = 0110b	0.153	0.18	0.207	V
		VDS_LVL_x = 0111b	0.17	0.2	0.23	V
		VDS_LVL_x = 1000b	0.255	0.3	0.345	V
		VDS_LVL_x = 1001b	0.35	0.4	0.45	V
		VDS_LVL_x = 1010b	0.44	0.5	0.56	V
		VDS_LVL_x = 1011b	0.52	0.6	0.68	V
		VDS_LVL_x = 1100b	0.61	0.7	0.79	V
		VDS_LVL_x = 1101b	0.88	1	1.12	V
		VDS_LVL_x = 1110b	1.2	1.4	1.6	V
		VDS_LVL_x = 1111b	1.75	2	2.25	V

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DS_DG}	V_{DS} overcurrent protection deglitch time	VDS_DG = 00b	0.75	1	1.5	µs
		VDS_DG = 01b	1.5	2	2.5	µs
		VDS_DG = 10b	3.25	4	4.75	µs
		VDS_DG = 11b	6	8	10	µs
I_{OLD_PU}	Offline diagnostic current source	Pullup current		3.5		mA
I_{OLD_PD}	Offline diagnostic current source	Pulldown current		4		mA
R_{OLD}	Offline open load resistance detection threshold	V_{DS_LVL} = 1.4 V, 5 V ≤ V_{PVDD} ≤ 18 V		22	50	kΩ
		V_{DS_LVL} = 1.4 V, 5 V ≤ V_{PVDD} ≤ 37 V		22	105	kΩ
		V_{DS_LVL} = 2 V, 5 V ≤ V_{PVDD} ≤ 18 V		10	25	kΩ
		V_{DS_LVL} = 2 V, 5 V ≤ V_{PVDD} ≤ 37 V		10	50	kΩ
HEATER MOSFET DRIVER						
$I_{GH\_HS\_HEAT}$	Average charge-current	T_J = 25 ˚C		50		mA
R_{GL_HEAT}	On-resistance (discharge stage)	T_J = 25 ˚C	15	20	25	Ω
R_{GL_HEAT}	On-resistance (discharge stage)	T_J = 125 ˚C		28	36	Ω
$V_{GH\_HS\_HIGH}$	GH_HS high level output voltage	V_{PVDD} = 5 V; I_{CP} = 15 mA	V_{SH_HS} + 6			V
$V_{GH\_HS\_HIGH}$	GH_HS high level output voltage	V_{PVDD} = 13.5 V; I_{CP} = 15 mA	V_{SH_HS} + 8	V_{SH_HS} + 10	V_{SH_HS} + 11.5	V
$I_{HEAT\_SH\_STBY\_LK}$	SH_HS leakage current standby				25	µA
R_{GS_HEAT}	Passive gate-clamp resistance			150		kΩ
$t_{PDR\_GH\_HS}$	GH_HS rising propagation delay	V_{PVDD} = 13.5 V; R_G = 0 Ω; C_G = 2.7 nF		0.6		µs
$t_{PDF\_GH\_HS}$	GH_HS falling propagation delay	V_{PVDD} = 13.5 V; V_{SH_HS} = 0 V; R_G = 0 Ω; C_G = 2.7 nF		0.5		µs
$t_{RISE\_GH\_HS}$	Rise time (switch mode)	V_{PVDD} = 13.5 V; V_{SH_HS} = 0 V; R_G = 0 Ω; C_G = 2.7 nF		300		ns
$t_{FALL\_GH\_HS}$	Fall time (switch mode)	V_{PVDD} = 13.5 V; V_{SH_HS} = 0 V; R_G = 0 Ω; C_G = 2.7 nF		170		ns
HEATER PROTECTION CIRCUITS						
$V_{DS\_LVL\_HEAT}$	V_{DS} overcurrent protection threshold for heater MOSFET	HEAT_VDS_LVL = 0000b	0.050	0.06	0.07	V
		HEAT_VDS_LVL = 0001b	0.067	0.08	0.093	V
		HEAT_VDS_LVL = 0010b	0.085	0.10	0.115	V
		HEAT_VDS_LVL = 0011b	0.102	0.12	0.138	V
		HEAT_VDS_LVL = 0100b	0.119	0.14	0.161	V
		HEAT_VDS_LVL = 0101b	0.136	0.16	0.184	V
		HEAT_VDS_LVL = 0110b	0.153	0.18	0.207	V
		HEAT_VDS_LVL = 0111b	0.17	0.2	0.23	V
		HEAT_VDS_LVL = 1000b	0.204	0.240	0.276	V
		HEAT_VDS_LVL = 1001b	0.238	0.280	0.322	V
		HEAT_VDS_LVL = 1010b	0.272	0.320	0.368	V
		HEAT_VDS_LVL = 1011b	0.306	0.360	0.414	V
		HEAT_VDS_LVL = 1100b	0.340	0.400	0.460	V
		HEAT_VDS_LVL = 1101b	0.374	0.440	0.506	V
		HEAT_VDS_LVL = 1110b	0.476	0.560	0.644	V
		HEAT_VDS_LVL = 1111b	0.85	1	1.15	V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DS\_HEAT\_DG}$	V_{DS} overcurrent protection deglitch time	HEAT_VDS_DG = 00b	0.75	1	1.5	μs
		HEAT_VDS_DG = 01b	1.5	2	2.5	μs
		HEAT_VDS_DG = 10b	3.25	4	4.75	μs
		HEAT_VDS_DG = 11b	6	8	10	μs
$t_{DS\_HEAT\_BLK}$	V_{DS} overcurrent protection blanking time	HEAT_VDS_BLK = 00b	3.25	4	4.75	μs
		HEAT_VDS_BLK = 01b	6	8	10	μs
		HEAT_VDS_BLK = 10b	13	16	19	μs
		HEAT_VDS_BLK = 11b	27	32	37	μs
V_{OL_HEAT}	Open load threshold voltage	V_{SH_HS} = 0 V	1.8	2	2.2	V
I_{OL_HEAT}	Pullup current source open-load diagnosis activated	V_{SH_HS} = 0 V; $V_{SHheater}$ = 4.5 V		1		mA
t_{OL_HEAT}	Open-load filter time for heater MOSFET			2		ms
ELECTROCHROMIC DRIVER						
R_{DSON} ECFB	Low-side MOSFET on resistance for EC discharge	V_{PVDD} = 13.5 V; T_J = 25 ˚C; I_{ECFB} = ±0.25 A ECFB_LS_EN = 1b		1375		mΩ
R_{DSON} ECFB	Low-side MOSFET on resistance for EC discharge	V_{PVDD} = 13.5 V; T_J = 150 ˚C; I_{ECFB} = ±0.125 A ECFB_LS_EN = 1b			2500	mΩ
I_{OC_ECFB}	Overcurrent threshold of low-side MOSFET	V_{PVDD} = 13.5 V; I_{ECFB} current sink	0.5		1	A
$t_{DG\_OC\_ECFB}$	Overcurrent shutdown deglitch time	V_{PVDD} <20 V; I_{ECFB} current sink		40		μs
		V_{PVDD} >20 V; I_{ECFB} current sink		15		μs
dV_{ECFB}/dt	Slew rate of ECFB, low-side MOSFET	V_{PVDD} = 13.5 V, Rload = 64 Ω to P_{VDD}		7		V/μs
$I_{OL\_ECFB\_LS}$	Open load detection threshold for EC during discharge	EC_OLEN = 1b, ECFB_LS_EN = 1b	10	20	32	mA
$t_{DG\_OL\_ECFB\_LS}$	Open load detection deglitch time	EC_OLEN = 1b, ECFB_LS_EN = 1b	400		600	μs
$V_{EC\_CTRLmax}$	Maximum EC-control voltage target for ECFB	ECFB_MAX = 1b	1.4		1.6	V
$V_{EC\_CTRLmax}$	Maximum EC-control voltage target for ECFB	ECFB_MAX = 0b	1.12		1.28	V
V_{EC_res}	Minimum resolution for adjustable voltage of ECFB	EC_ON = 1b		23.8		mV
DNL_{ECFB}	Differential Non Linearity	EC_ON = 1b	–2		2	LSB
$\lvert dV_{ECFB}\rvert$	Voltage deviation between target and ECFB	V_{target} = 23.8 mV, dV_{ECFB}=V_{target} - V_{ECFB}; $\lvert I_{ECDRV}\rvert$ < 1 μA	–5% (–1LSB)		+5% (+1LSB)	mV
$\lvert dV_{ECFB}\rvert$	Voltage deviation between target and ECFB	V_{target} = 1.5V, dV_{ECFB}=V_{target} - V_{ECFB}; $\lvert I_{ECDRV}\rvert$ < 1 μA	–5% (–1LSB)		+5% (+1LSB)	mV
V_{ECFB_HI}	Indicates voltage at ECFB is higher than target	EC_ON = 1b		V_{target} + 0.12		V
V_{ECFB_LO}	Indicates voltage at ECFB is lower than target	EC_ON = 1b		V_{target} – 0.12		V
t_{FT_ECFB}	Filter time of ECFB high/low flag	EC_ON = 1b		32		μs
t_{BLK_ECFB}	Blanking time of EC regulation flags	Any EC target voltage change	200	250	300	μs
$V_{ECFB\_OV\_TH}$	Threshold for overvoltage on ECFB	ECFB_OV_MODE = 01b or 10b, EC_ON = 1b		3		V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ECFB\_OV\_DG}$	Deglitch time for overvoltage flag on ECFB	ECFB_OV_MODE = 01b or 10b, ECFB_OV_DG = 00b	16	20	24	µs
		ECFB_OV_MODE = 01b or 10b, ECFB_OV_DG = 01b	40	50	60	µs
		ECFB_OV_MODE = 01b or 10b, ECFB_OV_DG = 10b	80	100	120	µs
		ECFB_OV_MODE = 01b or 10b, ECFB_OV_DG = 11b	160	200	240	µs
$V_{ECDRVminHIGH}$	Output voltage range of ECDRV when EC_ON = 1	I_{ECDRV} = -10µA	4.5		6.5	V
$V_{ECDRVmaxLOW}$	Output voltage range of ECDRV when EC_ON = 0	I_{ECDRV} = 10µA	0		0.7	V
I_{ECDRV}	Current into ECDRV	V_{target} > V_{ECFB} + 500 mV; V_{ECDRV} = 3.5 V	–730		–80	µA
I_{ECDRV}	Current into ECDRV	V_{target} < V_{ECFB} - 500 mV; V_{ECDRV} = 1.0 V; V_{target} = 1 LSB; V_{ECFB} = 0.5 V	150		350	µA
R_{ECDRV_DIS}	Pulldown resistance at ECDRV in fast discharge mode	V_{ECDRV} = 0.7 V; EC enabled, then EC<5:0> = 0 or EC disabled			11	kΩ
$t_{DISCHARGE}$	Auto-discharge pulse width	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	240	300	360	ms
$t_{ECFB\_DISC\_BLK}$	Auto-discharge blanking time	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	2.25	3	3.75	ms
V_{DISC_TH}	PWM discharge level V_{ECDRV}	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	335	400	465	mV
$V_{DISC\_TH\_DIFF}$	PWM discharge threshold level V_{ECDRV} - V_{ECFB}	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	–50	0	50	mV
$V_{ECFB\_OLP\_TH}$	Threshold for open load detection on ECFB	EC_EN = 0b, EC_DIAG = 10b		2		V
I_{ECFB_OLP}	Current into ECFB during open load detection	EC_EN = 0b, EC_DIAG = 10b		0.5		mA
t_{ECFB_OLP}	Open load filter time for ECFB	EC_ON=0b, ECFB_DIAG=10b	2	3	4	ms
$V_{ECFB\_SC\_TH}$	Threshold for short-circuit detection on ECFB	EC_EN = 0b, EC_DIAG = 01b, ECFB_SC_RSEL=00b		25		mV
		EC_EN = 0b, EC_DIAG = 01b, ECFB_SC_RSEL=01b		50		mV
		EC_EN = 0b, EC_DIAG = 01b, ECFB_SC_RSEL=10b		100		mV
		EC_EN = 0b, EC_DIAG = 01b, ECFB_SC_RSEL=11b		150		mV
I_{ECFB_SC}	Current into ECFB during short-circuit detection	EC_EN = 0b, EC_DIAG = 01b		50		mA
t_{ECFB_SC}	Short-circuit diagnostics filter time for ECFB	EC_ON=0b, ECFB_DIAG=01b	2	3	4	ms
HALF-BRIDGE DRIVERS						
$R_{ON\_OUT1,2\_HS}$	High-side MOSFET on resistance	I_{OUT} = 1 A, T_J = 25 ˚C		775		mΩ
		I_{OUT} = 0.5 A, T_J = 150 ˚C			1480	mΩ
$R_{ON\_OUT1,2\_LS}$	Low-side MOSFET on resistance	I_{OUT} = 1 A, T_J = 25 ˚C		765		mΩ
		I_{OUT} = 0.5 A, T_J = 150 ˚C			1460	mΩ
$R_{ON\_OUT3,4\_HS}$	High-side MOSFET on resistance	I_{OUT} = 4 A, T_J = 25 ˚C		220		mΩ
		I_{OUT} = 2 A, T_J = 150 ˚C			450	mΩ

$5\ V \le V_{PVDD} \le 35\ V$, $3.1\ V \le V_{DVDD} \le 5.5\ V$, $-40°C \le T_J \le 150°C$ (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ON\_OUT3,4\_LS}$	Low-side MOSFET on resistance	I_{OUT} = 4 A, T_J = 25 ˚C		220		mΩ
		I_{OUT} = 2 A, T_J = 150 ˚C			450	mΩ
$R_{ON\_OUT5\_HS}$	High-side MOSFET on resistance	I_{OUT} = 8 A, T_J = 25 ˚C		80		mΩ
		I_{OUT} = 4 A, T_J = 150 ˚C			160	mΩ
$R_{ON\_OUT5\_LS}$	Low-side MOSFET on resistance	I_{OUT} = 8 A, T_J = 25 ˚C		75		mΩ
		I_{OUT} = 4 A, T_J = 150 ˚C			150	mΩ
$R_{ON\_OUT6\_HS}$	High-side MOSFET on resistance	I_{OUT} = 7 A, T_J = 25 ˚C		90		mΩ
$R_{ON\_OUT6\_HS}$	High-side MOSFET on resistance	I_{OUT} = 3.5 A, T_J = 150 ˚C			180	mΩ
$R_{ON\_OUT6\_LS}$	Low-side MOSFET on resistance	I_{OUT} = 7 A, T_J = 25 ˚C		95		mΩ
$R_{ON\_OUT6\_LS}$	Low-side MOSFET on resistance	I_{OUT} = 3.5 A, T_J = 150 ˚C			190	mΩ
SR_{OUT_HB}	Output voltage rise/fall time for all half-bridge OUTx, 10% - 90%	PVDD = 13.5 V; OUTx_SR = 00b		1.6		V/µs
SR_{OUT_HB}	Output voltage rise/fall time for all half-bridge OUTx, 10% - 90%	PVDD = 13.5 V; OUTx_SR = 01b		13.5		V/µs
SR_{OUT_HB}	Output voltage rise/fall time for all half-bridge OUTx, 10% - 90%	PVDD = 13.5 V; OUTx_SR = 10b		24		V/µs
$t_{PD\_OUT\_HB\_HS\_R}$	Propagation time during output voltage rise for HS	ON command or INx (SPI last transition) to OUTx 10% voltage rise (any SR setting)	2		10	µs
$t_{PD\_OUT\_HB\_HS\_F}$	Propagation time during output voltage fall for HS	ON command or INx (SPI last transition) to OUTx 10% voltage fall (any SR setting)	1.5		11	µs
$t_{PD\_OUT\_HB\_LS\_R}$	Propagation time during output voltage rise for LS	ON command or INx (SPI last transition) to OUTx 10% voltage rise (any SR setting)	1.5		10	µs
$t_{PD\_OUT\_HB\_LS\_F}$	Propagation time during output voltage fall for LS	ON command or INx (SPI last transition) to OUTx 10% voltage fall (any SR setting)	1.5		10	µs
$t_{DEAD\_HS\_ON}$	Dead time during output voltage rise for HS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1		6	µs
$t_{DEAD\_HS\_OFF}$	Dead time during output voltage fall for HS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1		6	µs
$t_{DEAD\_LS\_ON}$	Dead time during output voltage rise for LS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1		7	µs
$t_{DEAD\_LS\_OFF}$	Dead time during output voltage fall for LS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1.7		14	µs
HALF-BRIDGE PROTECTION CIRCUITS						
$I_{OCP\_OUT1,2}$	Overcurrent protection threshold		1.2		2.2	A
$I_{OCP\_OUT3,4}$	Overcurrent protection threshold		4		8	A
I_{OCP_OUT5}	Overcurrent protection threshold		8		16	A
I_{OCP_OUT6}	Overcurrent protection threshold		7		13	A
$t_{DG\_OCP\_HB}$	Overcurrent protection deglitch time in half-bridge drivers	OUTX_OCP_DG = 00b	4.5	6	7.3	µs
		OUTX_OCP_DG = 01b	8	10	12	µs
		OUTX_OCP_DG = 10b	12	15	18	µs
		OUTX_OCP_DG = 11b	48	60	72	µs

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{ITRIP\_OUT1,2}$	Current threshold to trigger ITRIP regulation for OUT1 and OUT2	OUT1_ITRIP_LVL = 1b and OUT2_ITRIP_LVL = 1b	0.65		1.1	A
		OUT1_ITRIP_LVL = 0b and OUT2_ITRIP_LVL = 0b	0.5		0.9	A
$I_{ITRIP\_OUT3,4}$	Current threshold to trigger ITRIP regulation for OUT3 and OUT4	OUT3_ITRIP_LVL = 10b and OUT4_ITRIP_LVL = 10b	2.9		4.1	A
		OUT3_ITRIP_LVL = 01b and OUT4_ITRIP_LVL = 01b	1.6		3.25	A
		OUT3_ITRIP_LVL = 00b and OUT4_ITRIP_LVL = 00b	1		1.6	A
I_{ITRIP_OUT5}	Current threshold to trigger ITRIP regulation for OUT5	OUT5_ITRIP_LVL = 10b	6.65		8.95	A
		OUT5_ITRIP_LVL = 01b	5.65		7.8	A
		OUT5_ITRIP_LVL = 00b	2.5		3.4	A
I_{ITRIP_OUT6}	Current threshold to trigger ITRIP regulation for OUT6	OUT6_ITRIP_LVL = 10b	5.35		7.35	A
I_{ITRIP_OUT6}	Current threshold to trigger ITRIP regulation for OUT6	OUT6_ITRIP_LVL = 01b	4.65		6.4	A
I_{ITRIP_OUT6}	Current threshold to trigger ITRIP regulation for OUT6	OUT6_ITRIP_LVL = 00b	1.75		2.75	A
f_{ITRIP_HB}	Fixed frequency of ITRIP regulation for half-bridge drivers	OUTX_ITRIP_FREQ = 00b	17	20	23	kHz
		OUTX_ITRIP_FREQ = 01b	8	10	12	kHz
		OUTX_ITRIP_FREQ = 10b	4	5	6	kHz
		OUTX_ITRIP_FREQ = 11b	2	2.5	3	kHz
$t_{DG\_ITRIP\_HB}$	ITRIP regulation deglitch time for half-bridge drivers	OUTX_ITRIP_DG = 00b	1.5	2	2.5	µs
		OUTX_ITRIP_DG = 01b	4	5	6	µs
		OUTX_ITRIP_DG = 10b	8	10	12	µs
		OUTX_ITRIP_DG = 11b	16	20	24	µs
$I_{OLA\_OUT1,2}$	Under-current threshold for half-bridges 1 and 2		6	20	30	mA
$I_{OLA\_OUT3,4}$	Under-current threshold for half-bridges 3 and 4		15	50	90	mA
I_{OLA_OUT5}	Under-current threshold for half-bridges 5		40	150	300	mA
I_{OLA_OUT6}	Under-current threshold for half-bridges 6		30	120	240	mA
t_{OLA_HB}	Filter time of open-load signal for half-bridges	Duration of open-load condition to set the status bit		10		ms
$A_{IPROPI1,2}$	Current scaling factor for OUT1-2			650		A/A
$A_{IPROPI3,4}$	Current scaling factor for OUT3-4			1940		A/A
$A_{IPROPI5}$	Current scaling factor for OUT5			4000		A/A
$A_{IPROPI6}$	Current scaling factor for OUT6			3500		A/A
$I_{ACC\_1,2}$	Current sense output accuracy for OUT1-2	0.1 A < $I_{OUT1,2}$ < 0.25 A	-15		15	%
		0.25 A < $I_{OUT1,2}$ < 0.5 A	-10		10	%
		0.5 A < $I_{OUT1,2}$ < 1 A	-8		8	%
$I_{ACC\_3,4}$	Current sense output accuracy for OUT3-4	0.1 A < $I_{OUT3,4}$ < 0.5 A	-15		15	%
		0.5 A < $I_{OUT3,4}$ < 1 A	-12		12	%
		1 A < $I_{OUT3,4}$ < 2 A	-10		10	%
		2 A < $I_{OUT3,4}$ < 4 A	-8.5		8.5	%

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ACC_5}	Current sense output accuracy for OUT5	0.1 A < I_{OUT5} < 0.8 A	-40		40	%
I_{ACC_5}		0.8 A < I_{OUT5} < 2 A	-12		12	%
I_{ACC_5}		2 A < I_{OUT5} < 4 A	-10		10	%
I_{ACC_5}		4 A < I_{OUT5} < 8 A	-8		8	%
I_{ACC_6}	Current sense output error for OUT6	0.1 A < I_{OUT6} < 0.8 A	-40		40	%
I_{ACC_6}		0.8 A < I_{OUT6} < 2 A	-12		12	%
I_{ACC_6}		2 A < I_{OUT6} < 4 A	-10		10	%
I_{ACC_6}		4 A < I_{OUT6} < 8 A	-8		8	%
R_{S_GND}	Resistance threshold on OUTx to GND detected as a short during OLP	V_{DVDD} = 5 V, V_{OLP_REF} = 2.65 V, OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b	1		3	kΩ
R_{S_PVDD}	Resistance threshold on OUTx to PVDD detected as a short during OLP	V_{PVDD} = 13.5 V, V_{DVDD} = 5 V, V_{OLP_REF} = 2.65 V, OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b	3		15	kΩ
R_{S_PVDD}	Resistance threshold on OUTx to PVDD detected as a short during OLP	5 V ≤ V_{PVDD} ≤ 35 V, V_{DVDD} = 5 V, V_{OLP_REF} = 2.65 V, OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b	1		40	kΩ
R_{OPEN_HB}	Resistance threshold on OUTx detected as an open	V_{DVDD} = 5 V, V_{OLP_REF} = 2.65 V, OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b	35		1500	Ω
V_{OLP_REFH}	OLP comparator Reference High	OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b		2.65		V
V_{OLP_REFL}	OLP comparator Reference Low	OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b		2		V
R_{OLP_PU}	Internal pullup resistance on OUTx to VDD during OLP	OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b		1		kΩ
R_{OLP_PD}	Internal pulldown resistance on OUTx to VDD during OLP	OUTX_CNFG = 0b, HB_OLP_CNFG > 0b and HB_OLP_SEL > 0b		1		kΩ
HIGH-SIDE DRIVERS						
R_{DSON} OUT7 (low RDSON mode)	High-side MOSFET on resistance in low resistance mode	T_J = 25 ˚C; I_{OUT7} = ±0.5 A		400		mΩ
		T_J = 150 ˚C; I_{OUT7} = ±0.25 A			730	mΩ
R_{DSON} OUT7 (high RDSON mode)	High-side MOSFET on resistance in high resistance mode	T_J = 25 ˚C; I_{OUT8} = ±0.25 A		1200		mΩ
		T_J = 150 ˚C; I_{OUT8} = ±0.125 A			2200	mΩ
R_{DSON} OUT8	High-side MOSFET on resistance	T_J = 25 ˚C; I_{OUT8} = ±0.25 A		1200		mΩ
		T_J = 150 ˚C; I_{OUT8} = ±0.125 A			2200	mΩ
R_{DSON} OUT9	High-side MOSFET on resistance	T_J = 25 ˚C; I_{OUT9} = ±0.25 A		1200		mΩ
		T_J = 150 ˚C; I_{OUT9} = ±0.125 A			2200	mΩ
R_{DSON} OUT10	High-side MOSFET on resistance	T_J = 25 ˚C; I_{OUT10} = ±0.25 A		1200		mΩ
		T_J = 150 ˚C; I_{OUT10} = ±0.125 A			2200	mΩ
R_{DSON} OUT11	High-side MOSFET on resistance	T_J = 25 ˚C; I_{OUT11} = ±0.25 A		1200		mΩ
		T_J = 150 ˚C; I_{OUT11} = ±0.125 A			2200	mΩ

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON} OUT12	High-side MOSFET on resistance	T_J = 25 ˚C; I_{OUT12} = ±0.25 A		1200		mΩ
		T_J = 150 ˚C; I_{OUT12} = ±0.125 A			2200	mΩ
$SR_{HS\_OUT7\_HI}$	Slew rate for OUT7 High R_{DSON} mode (10 to 90% of the final OUT value)	OUT7_RDSON_MODE = 0b, PVDD = 13.5V, Rload = 64 Ω		0.35		V/µs
$SR_{HS\_OUT7\_LO}$	Slew rate for OUT7 Low R_{DSON} mode (10 to 90% of the final OUT value)	OUT7_RDSON_MODE = 1b, PVDD = 13.5V, Rload = 16 Ω		0.29		V/µs
SR_{HS}	Slew rate for OUT8 – OUT12 (10 to 90% of the final OUT value)	PVDD = 13.5V, Rload 64 Ω		1.6		V/µs
$t_{PD\_OUT7\_HI\_ON}$	Rise propagation delay time driver for OUT7 High R_{DSON} mode (Delay between High-side ON command (SPI last transition) to 10% of final OUT7 value)	OUT7_RDSON_MODE = 0b, PVDD=13.5V, Rload = 64 Ω		16		µs
$t_{PD\_OUT7\_HI\_OFF}$	Fall propagation delay time driver for OUT7 High R_{DSON} mode (Delay between High-side OFF command (SPI last transition) to 90% of final OUT7 value)	OUT7_RDSON_MODE = 0b, PVDD=13.5V, Rload = 64 Ω		16		µs
$t_{PD\_OUT7\_LO\_ON}$	Rise propagation delay time driver for OUT7 Low R_{DSON} mode (Delay between High-side ON command (SPI last transition) to 10% of final OUT7 value)	OUT7_RDSON_MODE = 1b, PVDD=13.5V, Rload =16 Ω		19		µs
$t_{PD\_OUT7\_LO\_OFF}$	Fall propagation delay time driver for OUT7 Low R_{DSON} mode (Delay between High-side OFF command (SPI last transition) to 90% of final OUT7 value)	OUT7_RDSON_MODE = 1b, PVDD=13.5V, Rload =16 Ω		19		µs
$t_{PD\_HS\_ON}$	Rising propagation delay time driver for high-side drivers OUT8 – OUT12 (Delay between High-side ON command (SPI last transition) to 10% of final OUTx value)	PVDD=13.5V, Rload = 64 Ω		4		µs
$t_{PD\_HS\_OFF}$	Falling propagation delay time driver for high-side drivers OUT8 – OUT12 (Delay between High-side OFF command (SPI last transition) to 90% of final OUTx value)	PVDD=13.5V, Rload = 64 Ω		4		µs
$f_{PWMx(00)}$	PWM switching frequency	PWM_OUTX_FREQ = 00b	78	108	138	Hz
$f_{PWMx(01)}$	PWM switching frequency	PWM_OUTX_FREQ = 01b	157	217	277	Hz
$f_{PWMx(10)}$	PWM switching frequency	PWM_OUTX_FREQ = 10b	229	289	359	Hz
$f_{PWMx(11)}$	PWM switching frequency	PWM_OUTX_FREQ = 11b	374	434	494	Hz
I_{LEAK_H}	Switched-off output current high-side drivers of OUT7-12	V_{OUT} = 0 V; standby mode	–10			µA
HIGH-SIDE DRIVER PROTECTION CIRCUITS						
I_{OC7}	Overcurrent threshold in high RDSON mode	OUT7_RDSON_MODE = 0b	500		1000	mA
	Overcurrent threshold in low RDSON mode	OUT7_RDSON_MODE = 1b	1500		3000	mA
I_{OC8}, I_{OC9}, I_{OC10}, I_{OC11},I_{OC12}	Overcurrent threshold OUT8 - OUT12	OUTX_OC_TH = 0b	250		500	mA
		OUTX_OC_TH = 1b	500		1000	mA

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCM_OUT7}	Constant current level for high-side driver OUT7 High R_{DSON}	OUT7_RDSON_MODE = 0b, OUT7_CCM_EN = 1b, OUT7_CCM_TO = 0b	180	250	330	mA
		OUT7_RDSON_MODE = 0b, OUT7_CCM_EN = 1b, OUT7_CCM_TO = 1b	240	330	420	mA
I_{CCM_OUT7}	Constant current level for high-side driver OUT7 Low R_{DSON}	OUT7_RDSON_MODE = 1b, OUT7_CCM_EN = 1b, OUT7_CCM_TO = 0b	210	360	530	mA
I_{CCM_OUT7}	Constant current level for high-side driver OUT7 Low R_{DSON}	OUT7_RDSON_MODE = 1b, OUT7_CCM_EN = 1b, OUT7_CCM_TO = 1b	250	450	650	mA
I_{CCM}	Constant current level for high-side drivers OUT8-12	OUTX_CCM_EN = 1b, OUTX_CCM_TO = 0b	240	350	450	mA
		OUTX_CCM_EN = 1b, OUTX_CCM_TO = 1b	320	450	580	mA
t_{CCMto}	Constant current mode time expiration	OUTX_CCM_EN = 1b	8	10	12	ms
V_{SC_DET}	Short-circuit detection Voltage on OUT7-12			2		V
t_{SC_BLK}	Blank time for short-circuit detection, ITRIP regulation and overcurrent protection in OUT7-12			40		µs
$t_{\_HS\_DG\_OUT7}$	Degltich time for short circuit detection , ITRIP regulation and overcurrent protection in OUT7	OUT7_ITRIP_DG = 00b , PVDD ≤ 20V	39	48	59	µs
		OUT7_ITRIP_DG = 01b , PVDD ≤ 20V	32	40	48	µs
		OUT7_ITRIP_DG = 10b , PVDD ≤ 20V	26	32	38	µs
		OUT7_ITRIP_DG = 11b , PVDD ≤ 20V	19	24	29	µs
		PVDD > 20V	8	10	13	µs
$f_{ITRIP\_HS\_OUT7}$	ITRIP frequency for high-side driver OUT7	OUT7_ITRIP_FREQ = 00b		1.7		kHz
		OUT7_ITRIP_FREQ = 01b		2.2		kHz
		OUT7_ITRIP_FREQ = 10b		3		kHz
		OUT7_ITRIP_FREQ = 11b		4.4		kHz
$t_{\_HS\_DG\_OUTx}$	Degltich time for short-circuit detection , ITRIP regulation and overcurrent protection in OUT8-12	OUTX_ITRIP_DG = 00b , PVDD ≤ 20V	39	48	59	µs
		OUTX_ITRIP_DG = 01b , PVDD ≤ 20V	32	40	48	µs
		OUTX_ITRIP_DG = 10b , PVDD ≤ 20V	26	32	38	µs
		OUTX_ITRIP_DG = 11b , PVDD ≤ 20V	19	24	29	µs
		PVDD > 20V	8	10	13	µs
$f_{ITRIP\_HS\_OUTX}$	ITRIP frequency for high-side driver OUT8-12	HS_OUT_ITRIP_FREQ=00b		1.7		kHz
		HS_OUT_ITRIP_FREQ=01b		2.2		kHz
		HS_OUT_ITRIP_FREQ=10b		3		kHz
		HS_OUT_ITRIP_FREQ=11b		4.4		kHz
I_{OLD7}	Open-load threshold for OUT7	OUT7_RDSON_MODE = 1b	15		30	mA
	Open-load threshold for OUT7	OUT7_RDSON_MODE = 0b	5		10	mA
I_{OLD8}, I_{OLD9}, I_{OLD10}, I_{OLD11}, I_{OLD12}	Open-load threshold for OUT8 - OUT12	OUTX_OLA_TH = 0b	1.3		3.3	mA
		OUTX_OLA_TH = 1b	4		12	mA
t_{OLD_HS}	Filter time of open-load signal for high-side drivers	Duration of open-load condition to set the status bit		200	250	µs
$A_{IPROPI7\_HI}$	Current scaling factor for OUT7 in high on-resistance mode	OUT7_RDSON_MODE = 0b		250		A/A

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{IPROPI7\_LO}$	Current scaling factor for OUT7 in low on-resistance mode	OUT7_RDSON_MODE = 1b		750		A/A
$A_{IPROPI8}$, $A_{IPROPI9}$, $A_{IPROPI10}$, $A_{IPROPI11}$, $A_{IPROPI12}$,	Current scaling factor for OUT8-12			250		A/A
$I_{ACC\_7\_HI\_RDSON}$	Current sense output accuracy for OUT7 in high RDSON mode	0.1 A < I_{OUT7} < 0.5 A	-18		18	%
$I_{ACC\_7\_HI\_RDSON}$	Current sense output accuracy for OUT7 in high RDSON mode	I_{OUT7} = 0.25 A	-10		10	%
$I_{ACC\_7\_HI\_RDSON}$	Current sense output accuracy for OUT7 in high RDSON mode	I_{OUT7} = 0.5 A	-9		9	%
$I_{ACC\_7\_LOW\_RDSON}$	Current sense output accuracy for OUT7 in low RDSON mode	0.5 A < I_{OUT7} < 1.5 A	-14		14	%
$I_{ACC\_7\_LOW\_RDSON}$	Current sense output accuracy for OUT7 in low RDSON mode	I_{OUT7} = 1 A	-8		8	%
$I_{ACC\_7\_LOW\_RDSON}$	Current sense output accuracy for OUT7 in low RDSON mode	I_{OUT7} = 1.5 A	-6		6	%
$I_{ACC\_8-12\_LO}$	Current sense output accuracy for low current OUT8-12	0.05 A < $I_{OUT8-12}$ < 0.1 A	-28		28	%
$I_{ACC\_8-12\_LO}$	Current sense output accuracy for low current OUT8-12	$I_{OUT8-12}$ < 0.075 A	-20		20	%
$I_{ACC\_8-12\_LO}$	Current sense output accuracy for low current OUT8-12	$I_{OUT8-12}$ < 0.1 A	-18		18	%
$I_{ACC\_8-12\_HI}$	Current sense output accuracy for high current OUT8-12	0.1 A < $I_{OUT8-12}$ < 0.5 A	-18		18	%
$I_{ACC\_8-12\_HI}$	Current sense output accuracy for high current OUT8-12	$I_{OUT8-12}$ = 0.25 A	-10		10	%
$I_{ACC\_8-12\_HI}$	Current sense output accuracy for high current OUT8-12	$I_{OUT8-12}$ = 0.5 A	-6		6	%
t_{IPROPI_BLK}	IPROPI blanking time	OUT7-12 goes high to IPROPI ready, only applicable when monitoring High-side driver current		60		µs
		IPROPI mux switching to IPROPI ready		5		µs
PROTECTION CIRCUITS						
V_{PVDD_UV}	PVDD undervoltage threshold	V_{PVDD} rising	4.425	4.725	5	V
		V_{PVDD} falling	4.225	4.525	4.8	V
$V_{PVDD\_UV\_HYS}$	PVDD undervoltage hysteresis	Rising to falling threshold		250		mV
$t_{PVDD\_UV\_DG}$	PVDD undervoltage deglitch time		8	10	12.75	µs
V_{PVDD_OV}	PVDD overvoltage threshold	V_{PVDD} rising, PVDD_OV_LVL = 0b	20	21	22	V
		V_{PVDD} falling, PVDD_OV_LVL = 0b	19	20	21	V
		V_{PVDD} rising, PVDD_OV_LVL = 1b	25.75	26.8	28	V
		V_{PVDD} falling, PVDD_OV_LVL = 1b	24.75	25.8	27	V
$V_{PVDD\_OV\_HYS}$	PVDD overvoltage hysteresis	Rising to falling threshold		1		V
$t_{PVDD\_OV\_DG}$	PVDD overvoltage deglitch time	PVDD_OV_DG = 00b	0.75	1	1.5	µs
		PVDD_OV_DG = 01b	1.5	2	2.5	µs
		PVDD_OV_DG = 10b	3.25	4	4.75	µs
		PVDD_OV_DG = 11b	7	8	9	µs

5 V ≤ V_{PVDD} ≤ 35 V, 3.1 V ≤ V_{DVDD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V, V_{DVDD} = 5 V and T_J = 25˚C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DVDD_POR}	DVDD supply POR threshold	DVDD falling	2.5	2.7	2.9	V
		DVDD rising	2.6	2.8	3	V
$V_{DVDD\_POR\_HYS}$	DVDD POR hysteresis	Rising to falling threshold		100		mV
$t_{DVDD\_POR\_DG}$	DVDD POR deglitch time		5	12	25	µs
t_{WD}	Watchdog window min	WD_WIN = 0b	3.4	4	4.6	ms
		WD_WIN = 1b	8.5	10	11.5	ms
	Watchdog window max	WD_WIN = 0b	10.5	12	13.5	ms
		WD_WIN = 1b	85	100	115	ms
$A_{IPROPI\_PVDD\_VOUT}$	IPROPI PVDD Voltage Sense Output Scaling Factor (V_{PVDD} / I_{IPROPI})	IPROPI_SEL = 10000b (5V-22V sense range)	9	11	13	V/mA
$A_{IPROPI\_PVDD\_VOUT}$	IPROPI PVDD Voltage Sense Output Scaling Factor (V_{PVDD} / I_{IPROPI})	IPROPI_SEL = 101010b (20V - 32V sense range)	13.5	16.5	19.5	V/mA
$V_{IPROPI\_TEMP\_VOUT}$	IPROPI Temperature Sense Output		–20		+20	°C
T_{OTW1}	Low Thermal warning temperature	T_J rising	110	125	140	°C
T_{OTW2}	High Thermal warning temperature	T_J rising	130	145	160	°C
T_{HYS}	Thermal warning hysteresis			20		°C
T_{OTSD}	Thermal shutdown temperature	T_J rising	160	175	190	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
t_{OTSD_DG}	Thermal shutdown deglitch time			10		µs

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
f_{SPI}	SPI supported clock frequency (1) (2)			5	MHz
t_{READY_SPI}	SPI ready after power up			1	ms
t_{CLK}	SCLK minimum period	200			ns
t_{CLKH}	SCLK minimum high time	100			ns
t_{CLKL}	SCLK minimum low time	100			ns
t_{HI_nSCS}	nSCS minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{H_nSCS}	nSCS input hold time	25			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{H_SDI}	SDI input data hold time	25			ns
t_{D_SDO}	SDO output data delay time, C_L = 20 pF (1)			60	ns
t_{EN_nSCS}	Enable delay time, nSCS low to SDO active			50	ns
t_{DIS_nSCS}	Disable delay time, nSCS high to SDO Hi-Z			50	ns

(1) SDO delay times are valid only with SDO external load (C_L) of 20 pF. Increasing load on SDO add an additional delay on SDO limiting the SCLK maximum.
(2) Refer to SPI Timing diagram for parameters.

7 Detailed Description

7.1 Overview

The DRV8000-Q1 device integrates multiple types of drivers intended for multiple functions: driving and diagnosing motor (inductive), resistive and capacitive loads. The devices features two half-bridge gate drivers, 6 integrated half-bridges, 6 integrated high-side drivers, one high-side external MOSFET gate driver for heater, one high-side gate driver for electrochromic charge and one integrated low-side driver for electrochromic load discharge. Each driver features current sensing, protection and diagnostics along with system protection and diagnostics, which increases system integration and reduces total system size and cost.

The device half-bridge external MOSFET gate driver architecture automatically manages dead time to prevent shoot-through, controls slew rate to decrease electromagnetic interference (EMI), and configurable propagation delay for optimized performance. These gate drivers support input modes for independent half-bridge or H-bridge control. Two PWM inputs can be configured as polarity and drive control. The external MOSFET gate driver protection circuits include charge pump monitoring, short-circuit protection (V_{DS} fault monitoring) and open load detection (V_{GS} fault monitoring).

The half-bridge drivers can be controlled through SPI register or PWM pins PWM1 and IPROPI/PWM2. The half-bridges have configurable current chopping scheme called ITRIP. Protection circuits include short-circuit protection, active and passive open load detection.

The high-side drivers can be controlled through SPI register, external PWM pin (PWM1), or with a dedicated PWM generator which enables load regulation during operation. All High-side drivers also have optional constant current mode, ITRIP regulation for LED or lamp module loads. One high-side driver is configurable to drive either a lamp or LED load. Protection circuits include short-circuit protection and open load detection.

The device also has an external MOSFET drivers for resistive heating element. The heater MOSFET driver can be controlled with SPI register or with PWM pin (PWM1) and feature both short-circuit and open load detection.

There is also an electrochromic (EC) mirror driver. The EC driver is controlled only through SPI register. For EC drive, the driver control loop regulates the EC voltage to a 6-bit target voltage. To discharge the EC element or change target voltage, there is an integrated low-side MOSFET to discharge the EC element in either two discharge modes, a PWM discharge and fast discharge options. The EC driver protection includes LS overcurrent and open load detection.

IPROPI (IPROPI/PWM2) pin is a multi-purpose output pin or input PWM pin (PWM) that can provide proportional current sense from any integrated driver with current sense. IPROPI can be also configured to output PVDD motor supply monitor, internal temperature cluster monitor, or can be configured as a second PWM input option for integrated half-bridges.

7.2 Functional Block Diagram

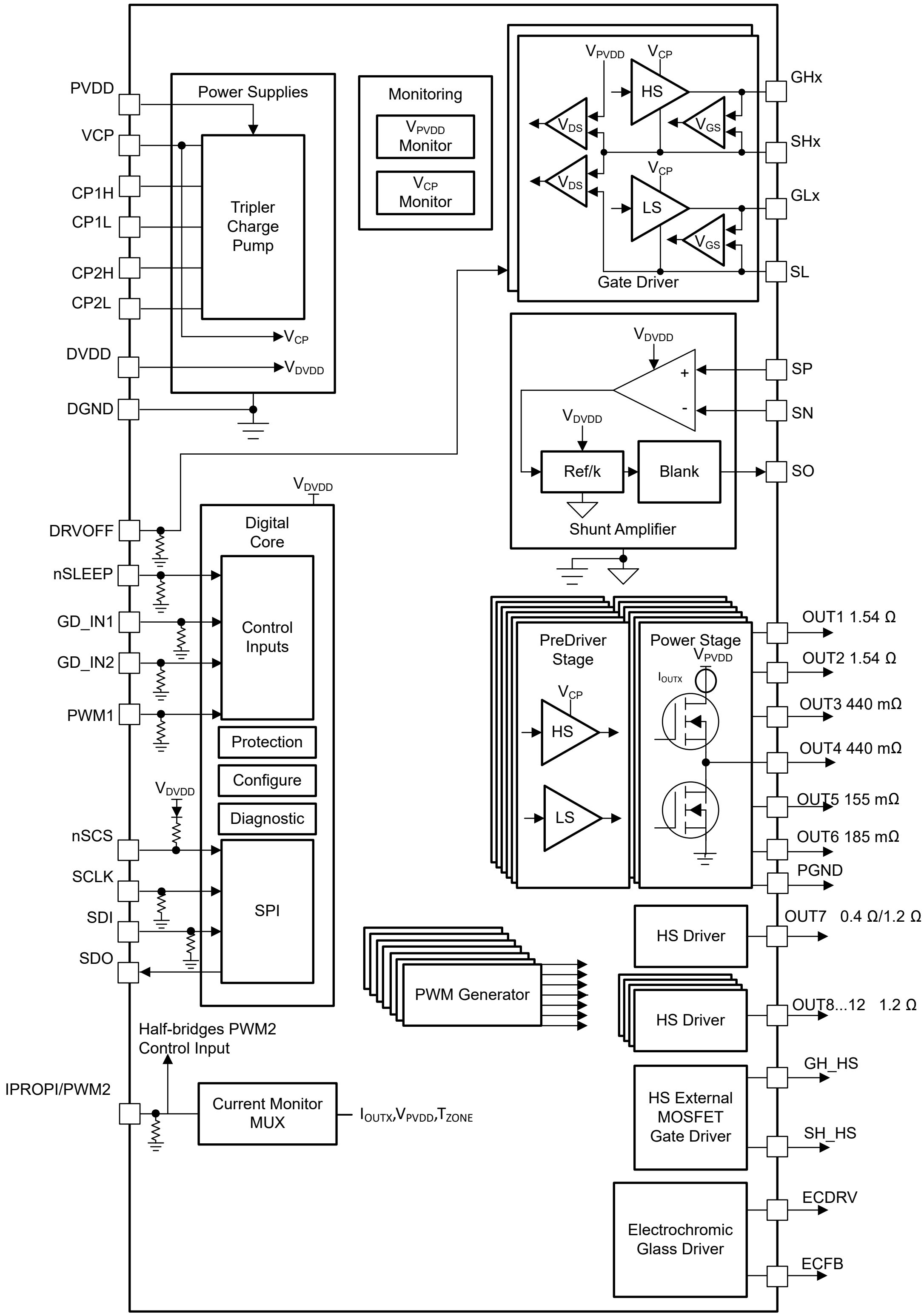


Figure 7-1. Block Diagram for DRV8000-Q1

7.3 External Components

Table 7-1 lists the recommended external components for the device. Refer to Section 9.2 for example of component placement.

Table 7-1. Recommended External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{PVDD1}	PVDD	GND	0.1µF, low ESR ceramic capacitor, PVDD-rated.
C_{PVDD2}	PVDD	GND	Local bulk capacitance greater than or equal to 10µF, PVDD-rated.
C_{DVDD}	DVDD	GND	1µF 6.3V, low ESR ceramic capacitor
C_{VCP}	VCP	PVDD	1µF 16V, low ESR ceramic capacitor
C_{FLY1}	CP1H	CP1L	0.1µF 100V, low ESR ceramic capacitor
C_{FLY2}	CP2H	CP2L	0.1µF 100V, low ESR ceramic capacitor
R_{IPROPI}	IPROPI	GND	Typically up to 2.35kΩ 0.063W resistor with 1% tolerance, depending on the controller supply voltage rail.
R_{FILT}	R_{IPROPI}	C_{FILT}	Optional resistor part of RC filter depending on the controller input.
C_{FILT}	R_{FILT}	GND	Optional low ESR ceramic capacitor part of RC filter depending on controller input.
R_{ECDRV}	ECDRV	GND	Typically 220Ω series resistance between ECDRV pin and gate of external MOSFET to stabilize control loop (only for ESD purposes). R_{ECDRV} is placed close to gate of external MOSFET after C_{ECDRV}.
C_{ECDRV}	ECDRV	GND	4.7nF, low ESR ceramic capacitor. C_{ECDRV} is placed on the ECDRV pin side of the series resistor R_{ECDRV}. **Note** Voltage rating for this capacitor is based on short to battery assumptions for ECFB.
C_{ECFB}	ECFB	GND	220nF, low ESR ceramic capacitor **Note** Voltage rating for this capacitor is based on short to battery assumptions for ECFB.
C_{SO1}	SO	GND	100nF 16V, low ESR ceramic capacitor. Part of Shunt Amplifier output filter.
C_{SO2}	SO	GND	0.01µF 16V, low ESR ceramic capacitor. Part of Shunt Amplifier output filter.
R_{SO}	C_{SO1}	C_{SO2}	Typically 0Ω, part of Shunt Amplifier output filter.
R_{GH_HS}	GH_SH	MOSFET Gate	Optional 0Ω, can be used for Heater slew rate control.
R_{SH_HS}	SH_SH	MOSFET Source	Optional 0Ω, can be used for Heater short to battery assumptions. **Note** External diode with appropriate current rating recommended in case of inductive shorts.

7.4 Feature Description

The table below provides links to all feature descriptions of key blocks of the device.

Table 7-2. Table of Device Features by Section

Device Block
Heater MOSFET Driver
Electrochromic Glass Driver
High-side Drivers
Half-bridge Drivers
Gate Drivers
IPROPI
Protection Circuits
Thermal Clusters
Fault Table

7.4.1 Heater MOSFET Driver

Table 7-3. Heater Driver Section Table of Contents

Heater Section	Link to Section
Back to Top of Feature Section	Section 7.4
Heater Driver Control	Section 7.4.1.1
Heater Driver Protection	Section 7.4.1.2

This is an external high-side MOSFET gate driver that can be used for driving resistive heating elements. The driver is controlled through SPI or PWM, and has programmable active short detection and off-state open-load detection.

7.4.1.1 Heater MOSFET Driver Control

The heater MOSFET driver control mode is configured with HEAT_CNFG bits in register HS_HEAT_OUT_CNFG. The heater configuration bits enable or disable control of the heater output, and configures the control source. For the heater driver, the control sources are SPI register control and PWM pin control.

When in SPI register control mode (HEAT_CNFG = 01b), the heater MOSFET gate drive is enabled and disabled by setting bit HEAT_EN in the register HS_EC_HEAT_CTRL.

When in PWM control mode (HEAT_CNFG = 10b), the gate driver is controlled with an external PWM signal on pin PWM1. If the heater driver is in PWM control mode, then HEAT_EN is ignored.

The table below summarizes the heater driver configuration and control options:

Table 7-4. Heater Configuration

HEAT_CNFG bits	Configuration	Description
00b	Disabled	Heater control disabled
01b	SPI register control	Heater SPI control enabled
10b	PWM1 control	Heater control by PWM1 pin
11b	Reserved	Reserved

Below is the block diagram for the heater driver block:

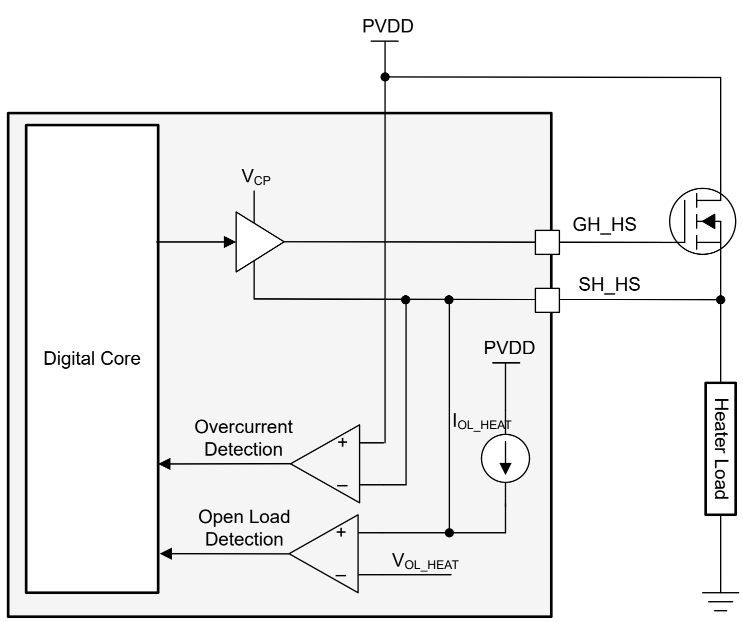


Figure 7-2. Heater MOSFET Driver Block Diagram

The timing waveform below shows the expected timing for the heater driver:

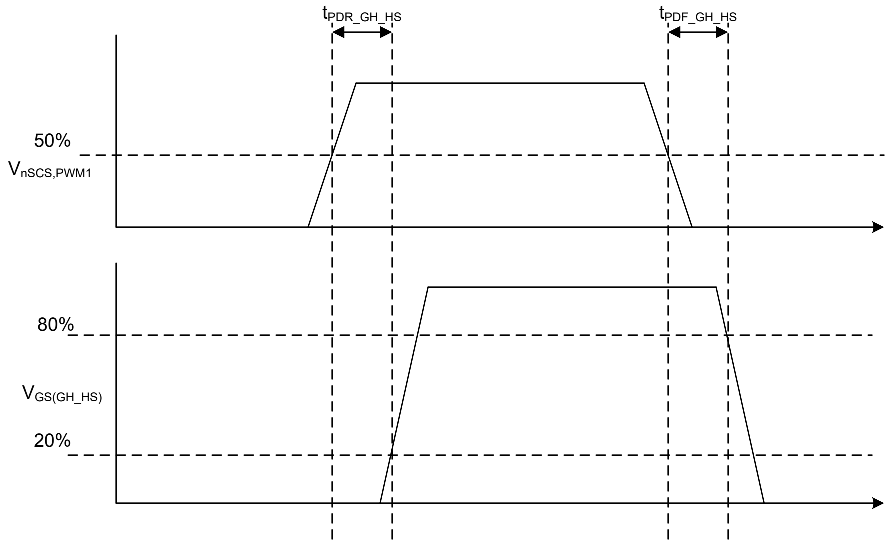


Figure 7-3. Heater Timing Diagram

7.4.1.2 Heater MOSFET Driver Protection

The heater driver has an active short-circuit detection and an off-state open-load detection.

7.4.1.2.1 Heater SH_HS Internal Diode

Only a limited amount of energy (<1mJ) can be dissipated by the internal ESD diodes on SH_HS pin. TI recommends adding an external diode from ground to SH_HS pin in case of a load short condition. During a heater load short condition, the current is limited only by the saturation current of the external heater MOSFET. If the heater output is configured to shut off due to short-circuit detection, this same current dissipates through the internal ESD diode from ground to SH_HS, which is larger than the what the internal ESD diode can dissipate.

7.4.1.2.2 Heater MOSFET V_{DS} Overcurrent Protection (HEAT_VDS)

If the voltage across the heater driver V_{DS} overcurrent comparator exceeds the $V_{DS\_LVL\_HEAT}$ for longer than the $t_{DS\_HEAT\_DG}$ time, a heater overcurrent condition is detected. The voltage threshold and deglitch time can be adjusted through the HEAT_CNFG register settings.

Table 7-5. Heater VDS Levels

HEAT_VDS_LVL	VDS Voltage Level
0000b	0.06V
0001b	0.08V
0010b	0.10V
0011b	0.12V
0100b	0.14V
0101b	0.16V
0110b	0.18V
0111b	0.2V
1000b	0.24V
1001b	0.28V
1010b	0.32V
1011b	0.36V
1100b	0.4V
1101b	0.44V

Table 7-5. Heater VDS Levels (continued)

HEAT_VDS_LVL	VDS Voltage Level
1110b	0.56V
1111b	1V

Table 7-6. Heater VDS Deglitch Times

HEAT_VDS_DG	Time
00b	1μs
01b	2μs
10b	4μs
11b	8μs

There is also a heater MOSFET V_{DS} monitor blanking period that is configured in bit HEAT_VDS_BLK in register HEAT_CNFG. There are four blanking time options:

Table 7-7. Heater VDS Blanking Times

HEAT_VDS_BLK	Time
00b	4μs
01b	8μs
10b	16μs
11b	32μs

The heater overcurrent monitor can respond and recover in four different modes set through the HEAT_VDS_MODE register setting.

- **Latched Fault Mode:** After detecting the overcurrent event, the gate driver pulldown is enabled, HEAT_VDS and EC_HEAT bits are asserted. After the overcurrent event is removed, the fault state remains latched until CLR_FLT is issued.
- **Cycle by Cycle Mode:** After detecting the overcurrent event, the gate driver pulldown is enabled and HEAT_VDS, EC_HEAT and FAULT bits are asserted. EC_HEAT and FAULT status bit in register IC_STAT1 remains asserted until driver control input changes (SPI or PWM). **To clear HEAT_VDS bit, a CLR_FLT command must be sent after an input change.** If CLR_FLT is issued before an input change, all the status bits remain asserted and driver pulldown stays enabled.
- **Warning Report Only Mode:** The heater overcurrent event is reported in the WARN and HEAT_VDS bits. The device takes no action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The heater V_{DS} overcurrent monitors are disabled and do not respond or report.

7.4.1.2.3 Heater MOSFET Open Load Detection

Off-state open-load monitoring is done by comparing the voltage difference SH_HS node when pulled up by current source against open-load threshold voltage V_{OL_HEAT}. If SH_HS voltage exceeds the open-load threshold V_{OL_HEAT} for longer than filter time t_{OL_HEAT}, the open-load bit HEAT_OL is set. Open-load monitor is controlled by bit HEAT_OLP_EN.

Note

The heater open load diagnostics only works when the heater configuration is disabled, where bits HEAT_CNFG must be 00b.

7.4.2 High-Side Drivers

Table 7-8. High-Side Driver Section Table of Contents

Half-Bridge Section	Link to Section
Back to Top of Feature Section	Section 7.4
High-side Driver Control	Section 7.4.2.1
High-side Driver Regulation	Section 7.4.2.1.3
High-side Driver Protection	Section 7.4.2.2

The device integrates 6 high-side drivers, OUT7 - OUT12, that can be programmed to drive several load types. Each high-side driver has selectable high or low overcurrent protection and open-load current thresholds. OUT7 can be configured to drive lamps, bulbs, or LEDs. All high-side drivers also have a fixed-time constant current mode intended for driving high capacitance LED modules.

Every high-side driver has open-load detection, overcurrent protection and short-circuit protection . OUT7 in both low R_{DSON} and high R_{DSON} mode has an optional ITRIP regulation for lamp or bulb loads. OUT8 - OUT12 also have optional ITRIP regulation which is activated if the respective overcurrent threshold (high or low) is exceeded. This feature can be used for driving larger LED modules or other load types with OUT8 - OUT12. If the electrochromic driver is used, OUT11 can be used to provide protected battery voltage for the EC element.

Below is a block diagram of the high-side drivers:

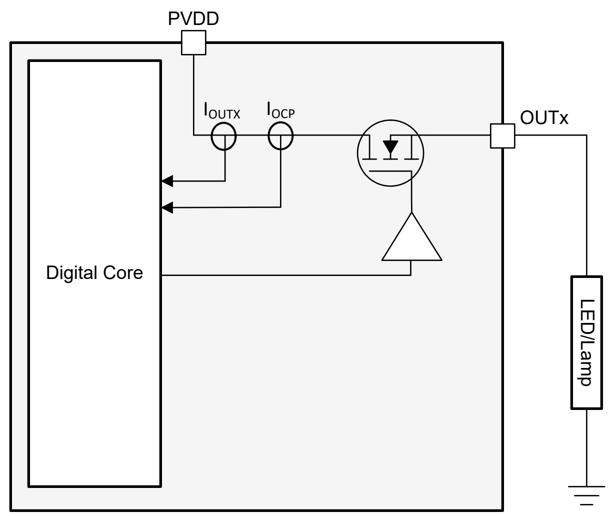


Figure 7-4. High-Side Driver Block Diagram

Table 7-9 summarizes all the device high-side drivers with the corresponding feature sets:

Table 7-9. High-Side Drivers and Features

High-Side Driver	RDSON (Ω)	OL Detect	Overcurrent/ Short-circuit Protection	ITRIP	CCM	Used for EC Supply
OUT7	0.4/1.2	Yes	Yes	Yes	Yes	No
OUT8	1.2	Yes	Yes	Yes	Yes	No
OUT9	1.2	Yes	Yes	Yes	Yes	No
OUT10	1.2	Yes	Yes	Yes	Yes	No
OUT11	1.2	Yes	Yes	Yes	Yes	Yes
OUT12	1.2	Yes	Yes	Yes	Yes	No

7.4.2.1 High-side Driver Control

The high-side drivers can be configured for control by SPI register, an internally generated PWM signal from 10-bit PWM generator or an external PWM signal from PWM1 pin. This configuration is done by setting OUTx_CNFG (OUT7-OUT12) bits in register HS_HEAT_OUT_CNFG.

In SPI register control mode, (OUTx_CNFG = 01b), the high-side output follows the enable bits for each output in HS_EC_HEAT_CTRL (ON/OFF).

The table below summarizes the high-side driver configuration options:

Table 7-10. High-side Driver Configuration

OUTx_CNFG bits	Configuration	Description
00	OFF	High-side driver control disabled
01	SPI register control	High-side driver SPI control enabled
10	PWM1 pin control	High-side driver control by PWM1 pin
11	PWM Generator	High-side driver control with dedicated internal PWM generator

7.4.2.1.1 High-side Driver PWM Generator

Each high-side driver has a dedicated PWM generator with 10-bit duty cycle resolution. The frequency and duty of each PWM generator can be controlled independently.

When configuring the high-side driver duty cycle a value up to 1022 (99.8%) can be selected.

Required Register Configuration Sequence:

1. Configure the high-side driver PWM frequency value in register HS_PWM_FREQ_CNFG
2. Set the duty cycle in register OUTx_DC with a value from 0 to 1022 (0% - 99.8% duty cycle)
3. Configure the driver mode of operation in register HS_HEAT_OUT_CNFG

The frequency of the PWM generator is controlled by bits PWM_OUTX_FREQ from register HS_PWM_FREQ_CNFG as shown in the table below:

Table 7-11. PWM Frequency

PWM_OUTX_FREQ	PWM Frequency (Hz)
00b	108
01b	217
10b	289
11b	434

7.4.2.1.2 Constant Current Mode

All high-side drivers have a timed Constant Current Mode feature (CCM), which can be used to provide a constant current for a short duration to the desired output. This mode is enabled with bit OUTx_CCM_EN in register HS_REG_CNFG2. When enabled, the current from the high-side driver is limited to the configured limit for a short duration of 10ms.

There are two current limit options for constant current mode. This is configured with bit OUTx_CCM_TO in register HS_REG_CNFG2, summarized in the table below:

Table 7-12. Constant Current Mode Options

High-side Output	OUTX_CCM_TO	Current Limit (I_{CCM})	Timeout (t_{CCMto})
OUT7 (RDSON High)	0b	250mA	10ms
	1b	330mA	10ms
OUT7 (RDSON Low)	0b	360mA	10ms
	1b	450mA	10ms

Table 7-12. Constant Current Mode Options (continued)

High-side Output	OUTX_CCM_TO	Current Limit (I_{CCM})	Timeout (t_{CCMto})
OUT8-12	0b	350mA	10ms
	1b	450mA	10ms

This constant current mode feature is enabled only if the OUTx_CCM_EN bit is configured prior to enabling the configured output and when the output is in the disabled state. CCM automatically expires after expiration time t_{CCMto}. After timeout, the driver remains enabled per bits OUTx_EN in register HS_HEAT_OUT_CNFG and configured based on OUTx_CNFG bits in register HS_HEAT_OUT_CNFG.

Required Register Configuration Sequence:

1. Configure the high-side driver CCM mode in register HS_REG_CNFG2
2. Configure the high-side driver operation in register HS_HEAT_OUT_CNFG

Once CCM mode is set and the driver configuration is done, the CCM timer begins when the corresponding OUTx_EN bits are set in register HS_HEAT_OUT_CNFG.

Only SPI control or external PWM generator control (OUTx_CNFG = 01b or 10b) is supported after CCM timer expires. Internal PWM generator control does not support CCM mode.

If constant current mode is configured after configuring the high-side driver, the CCM mode does not activate.

For OUTx_CCM_EN bit:

- If OUTx_CCM_EN is cleared by the controller before constant current mode timeout, the driver follows the command and is switched to the mode corresponding to OUTx_CNFG bits
- If OUTx_CCM_EN is set after the driver has already been enabled, the OUTx_CCM_EN bit is ignored; in this case OUTx_CCM_EN remains off

The short-circuit and overcurrent detection are active/enabled when the driver is ON, PWM driven, but NOT in constant current mode. Open load detection is always active.

7.4.2.1.3 OUTx HS ITRIP Behavior

For all high-side drivers, a fixed frequency current regulation feature called HS ITRIP is available. This function restarts the driver when an overcurrent condition occurs while driving certain loads. The overcurrent detection is based on sensed load current. This feature is intended to be used to drive loads with large inrush currents that exceed the overcurrent threshold of the driver, loads such as a lamp, bulb, or large LED module.

High side drivers can be configured to enable ITRIP regulation by setting the OUT7_ITRIP_EN in the HS_REG_CNFG1 register for OUT7 and the HS_OUTx_ITRIP_EN for OUT8-12 in HS_REG_CNFG3 register. By default, ITRIP regulation is disabled for all High-side drivers. If ITRIP regulation is disabled and after the blank time if the driver current exceeds overcurrent threshold (I_{OCx}) for deglitch time, the output is disabled.

ITRIP regulation enabled:

When ITRIP regulation is enabled and after blank time if driver current exceeds overcurrent threshold I_{OCx} for deglitch time, the output turns OFF. It automatically turns ON again after the end of ITRIP cycle. Overcurrent thresholds (high or low) are configured by setting OUT7_RDSON_MODE bit for OUT7 and OUTx_OC_TH bits for OUT8-12 in HS_OC_CNFG register.

Blank time for ITRIP regulation is 40µs for all high-side driver outputs. Blank time starts when OUTx is enabled. OUT7 has dedicated ITRIP frequency and deglitch time settings, configurable via bits OUT7_ITRIP_FREQ and OUT7_ITRIP_DG in the HS_REG_CNFG1 register. For OUT8-12, ITRIP frequency and deglitch time settings are shared, configurable via bits HS_OUT_ITRIP_FREQ and HS_OUT_ITRIP_DG in the HS_REG_CNFG3 register. For V_{PVDD} < 20V, all deglitch options (24, 32, 40, and 48µs) are available. For V_{PVDD} > 20V the deglitch time is automatically reduced to 10µs.

When ITRIP regulation is enabled and if an overcurrent detection is detected, OUT7_ITRIP_STAT bit in EC_HEAT_ITRIP_STAT register for OUT7 driver or OUTx_ITRIP_STAT bit in HS_ITRIP_STAT register for OUT8-12 drivers is set and latched. The fault bit remains set until the CLR_FLT bit is asserted.

Table 7-13. High-Side ITRIP Frequency Option Summary

Frequency (f_{ITRIP_HS})	HS_OUT_ITRIP_FREQ/OUT7_ITRIP_FREQ
1.7 kHz	00b
2.2 kHz	01b
3 kHz	10b
4.4 kHz	11b

Table 7-14. High-Side ITRIP Deglitch Option Summary

Deglitch Time ($t_{ITRIP\_HS\_DG}$)	HS_OUT_ITRIP_DG/OUT7_ITRIP_DG
48 µs	00b
40 µs	01b
32 µs	10b
24 µs	11b

The ITRIP deglitch timer starts when the OUTx ITRIP blank time expires. The minimum OUTx ITRIP ON time is the sum of blanking and deglitch times, and total period is determined by the OUTx ITRIP frequency. The diagram below shows the ITRIP behavior.

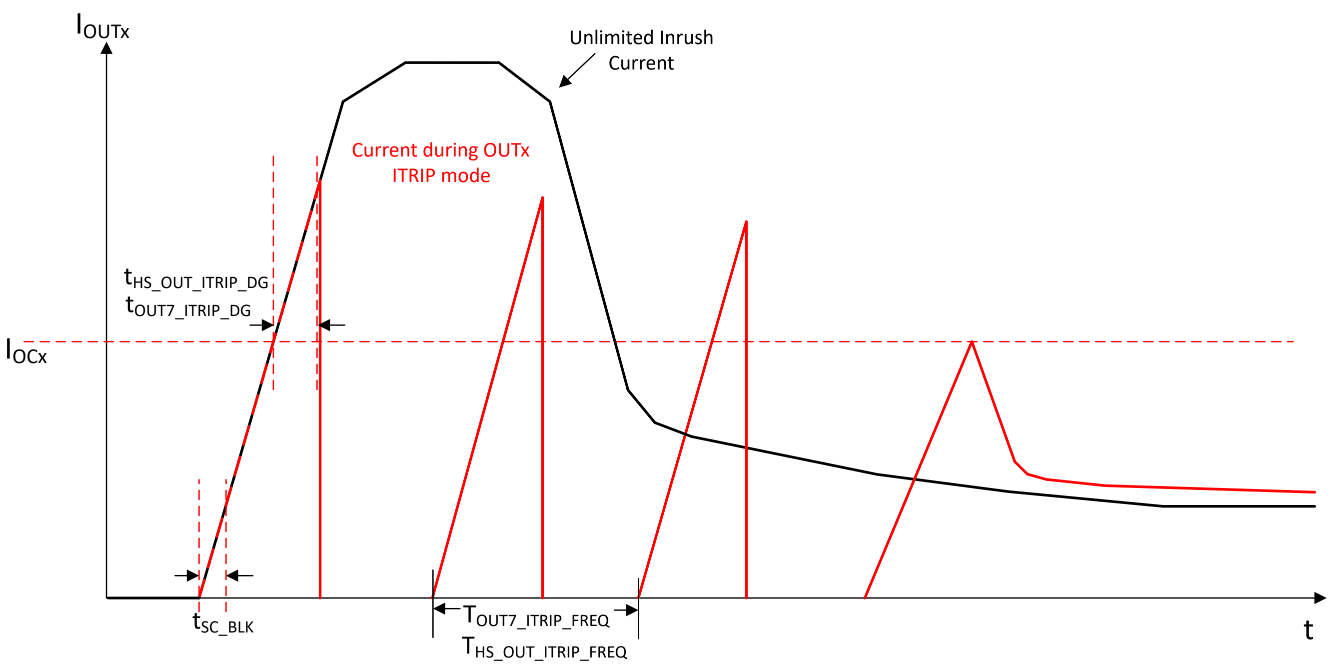


Figure 7-5. OUTx HS ITRIP Behavior with Incandescent Bulb

The blanking time t_{SC_BLK} is 40µs, after which the overcurrent condition can be detected. $t_{OUT7\_ITRIP\_DG}$ or $t_{HS\_OUT\_ITRIP\_DG}$ is the time OUTx remains on after overcurrent protection threshold is exceeded. $T_{OUT7\_ITRIP\_FREQ}$ or $T_{HS\_OUT\_ITRIP\_FREQ}$ is the time period of the ITRIP loop, inverse of $t_{OUT7\_ITRIP\_FREQ}$ or $t_{HS\_OUT\_ITRIP\_FREQ}$. ITRIP faults for OUT7-12 are reported in registers OUT7_ITRIP_STAT and OUTx_ITRIP_STAT.

7.4.2.1.4 High-side Drivers - Parallel Outputs

The high-side drivers OUT8 through OUT12 can be connected in parallel combinations to support even higher current loads. For example, OUT8 and OUT9 can be connected in parallel as a 600mΩ driver effectively, or OUT9, OUT10, and OUT12 can be connected in parallel as a 400mΩ driver effectively.

However, there are limitations with this mode of operation:

- Internal PWM control does not work for parallel high-side drivers and must not be configured for this mode of operation.
- Constant current mode is not be possible and must be disabled.
- ITRIP regulation is not supported.
- Overcurrent protection, short-circuit protection and active open load detection is supported.

If operating in parallel, the high-side drivers must be configured for ON/OFF SPI register control or external PWM signal control through pin.

7.4.2.2 High-side Driver Protection Circuits

7.4.2.2.1 High-side Drivers Internal Diode

Each high-side driver has an internal diode from ground to the high-side OUTx node for ESD protection. If either of the following occurs, this diode can be subjected to high energy dissipation:

- Both a loss of ground connection and short to ground on a high-side output.
- There is an inductive load on the high-side output.

Only a limited amount of energy (<1mJ) can be dissipated by the internal ESD diodes during freewheeling. For inductive loads greater than 100µH, a connection to an external freewheeling diode between PGND and the corresponding output is required

7.4.2.2.2 High-side Driver Short-circuit Protection

Short-circuit protection monitors each high-side output (OUT7-12) using a 2V comparator on the OUTx node. After the blank time If OUTx voltage does exceed the 2V short-circuit threshold for deglitch time, a short to ground fault is detected and the output is disabled.

The 2V comparator blank time (t_{SC_BLK}) is 40µs for all high side driver outputs. Blank time starts when OUTx is enabled. OUT7 has dedicated deglitch time settings, configurable via bits OUT7_ITRIP_DG in the HS_REG_CNFG1 register. For OUT8-12 deglitch time settings are shared, configurable via bits HS_OUT_ITRIP_DG in the HS_REG_CNFG3 register. For V_{PVDD} < 20V, all deglitch options (24, 32, 40, and 48µs) are available. For V_{PVDD} > 20V the deglitch time is automatically reduced to 10µs.

Upon short-circuit detection, the corresponding OUTx_OCP fault status bit in the HS_STAT register is latched and the corresponding output is shutoff. The fault bit remains set until the CLR_FLT bit is asserted. The diagram below shows the short circuit behavior for high-side drivers:

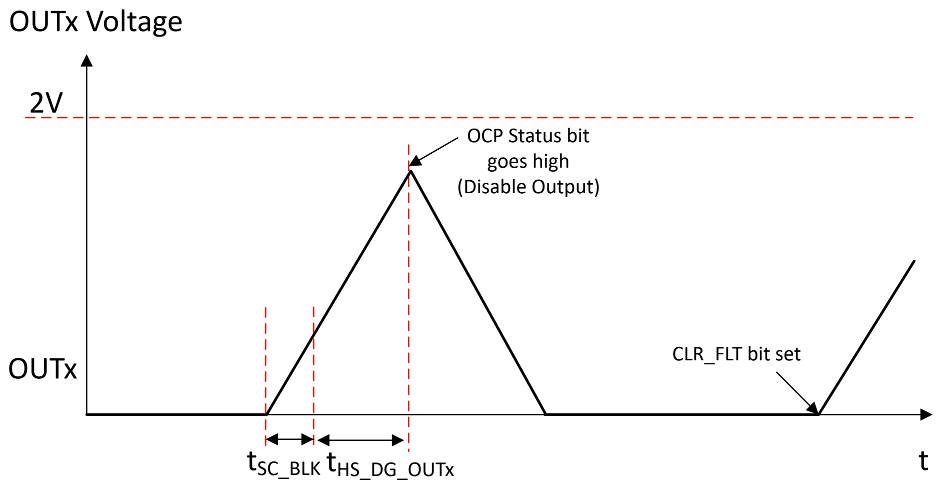


Figure 7-6. High-side Drivers Short-circuit Protection

7.4.2.2.3 High-side Driver Overcurrent Protection

Overcurrent protection is available when ITRIP regulation is disabled. The output current for all drivers (OUT7-OUT12) is monitored, and after the blank time if current exceed the overcurrent threshold after for deglitch time, the output is disabled.

Disable ITRIP for OUT7 by configuring OUT7_ITRIP_EN = 0b in HS_REG_CNFG1 and for OUT8-12 by configuring HS_OUTx_ITRIP_EN = 0b in HS_REG_CNFG3 register. Overcurrent thresholds are configured (high or low) by setting OUT7_RDSON_MODE bit for OUT7 and OUTx_OC_TH bits for OUT8-12 in HS_OC_CNFG register.

Blank time for overcurrent protection is 40µs for all high-side driver outputs. Blank time starts when OUTx is enabled. OUT7 has dedicated deglitch time settings, configurable via bits OUT7_ITRIP_DG in the HS_REG_CNFG1 register. For OUT8-12 deglitch time settings are shared, configurable via bits HS_OUT_ITRIP_DG in the HS_REG_CNFG3 register. For V_{PVDD} < 20V, all deglitch options (24, 32, 40, and 48µs) are available. For V_{PVDD} > 20V the deglitch time is automatically reduced to 10µs. When overcurrent detection is detected, OUT7_ITRIP_STAT bit in EC_HEAT_ITRIP_STAT register for OUT7 driver or OUTx_ITRIP_STAT bit in HS_ITRIP_STAT register for OUT8-12 drivers is latched and the corresponding output is shutoff. The fault bit remains set until the CLR_FLT bit is asserted.

7.4.2.2.4 High-side Driver Open Load Detection

The high-side drivers have open-load detection. Similar to the half-bridge drivers OLA detection scheme of the DRV800x-Q1, the high-side drivers open-load detection scheme sequences through each driver checking if the load current is below the open-load current threshold. The open-load current threshold I_{OLDx} is configurable between high and low-current thresholds with bits OUTx_OLA_TH in register HS_OL_CNFG for OUT8-12. The thresholds are automatically adjusted only for high-side driver OUT7 based on OUT7_RDSON_MODE.

Open-load detection must be enabled with bit OUTx_OLA_EN in register HS_OL_CNFG for OUT7-12 high-side drivers.

If the load current I_{OUTX} is below the open-load threshold (I_{OLD_HS}) for t > t_{OLD_HS}, then the corresponding high-side open load status bit OUTx_OLA is set in the status register. The driver detected with open-load is not switched off.

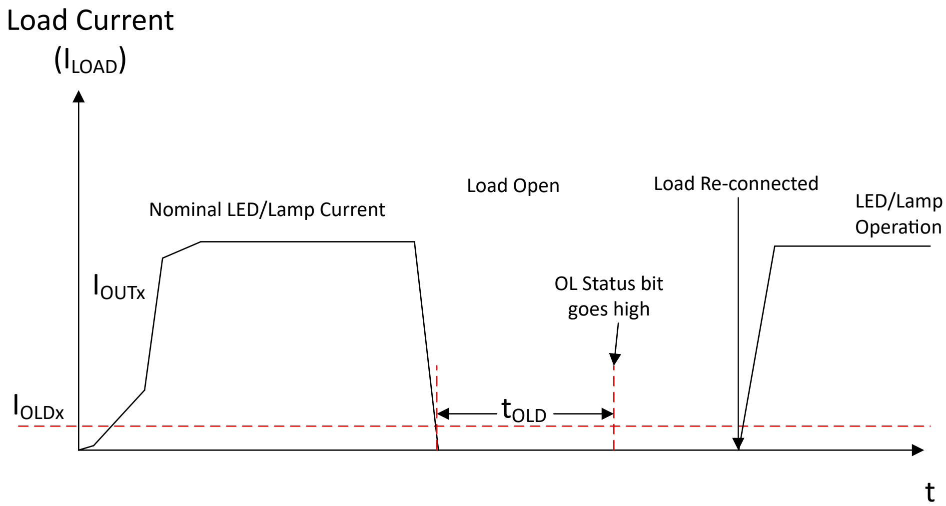


Figure 7-7. Open-Load Detection for High-side Drivers

The open-load detection test time for each high-side driver is 200μs. The timer does not start until the output is enabled. Once all enabled drivers have been cycled through, the detection cycle restarts. When the OLA bit is flagged for an OUTx, the status is latched and the OUTx is excluded from the detection cycle. CLR_FLT is required to restart the OLA check for the OUTx.

The high-side driver must be ON for minimum 200μs for the OLA detection to complete. Otherwise, the device waits until the next PWM cycle. The OFF counter for the OLA detection starts when the high-side driver turns OFF and ends OLA detection if the driver is detected OFF for more than 10ms.

7.4.3 Electrochromic Glass Driver

Table 7-15. EC Driver Section Table of Contents

EC Driver Section	Link to Section
Back to Top of Feature Section	Section 7.4
EC Driver Control	Section 7.4.3.1
EC Driver Protection	Section 7.4.3.2

The device features an integrated electrochromic driver block that can be used to charge or discharge an electrochromic element of a mirror. The electrochromic driver block charges an external MOSFET to control the charging and discharge voltage of the element. The driver configuration operates with either high-side driver OUT11 as protected supply to the element or without OUT11 (independent OUT11 control).

7.4.3.1 Electrochromic Driver Control

Below is the block diagram for the electrochromic driver:

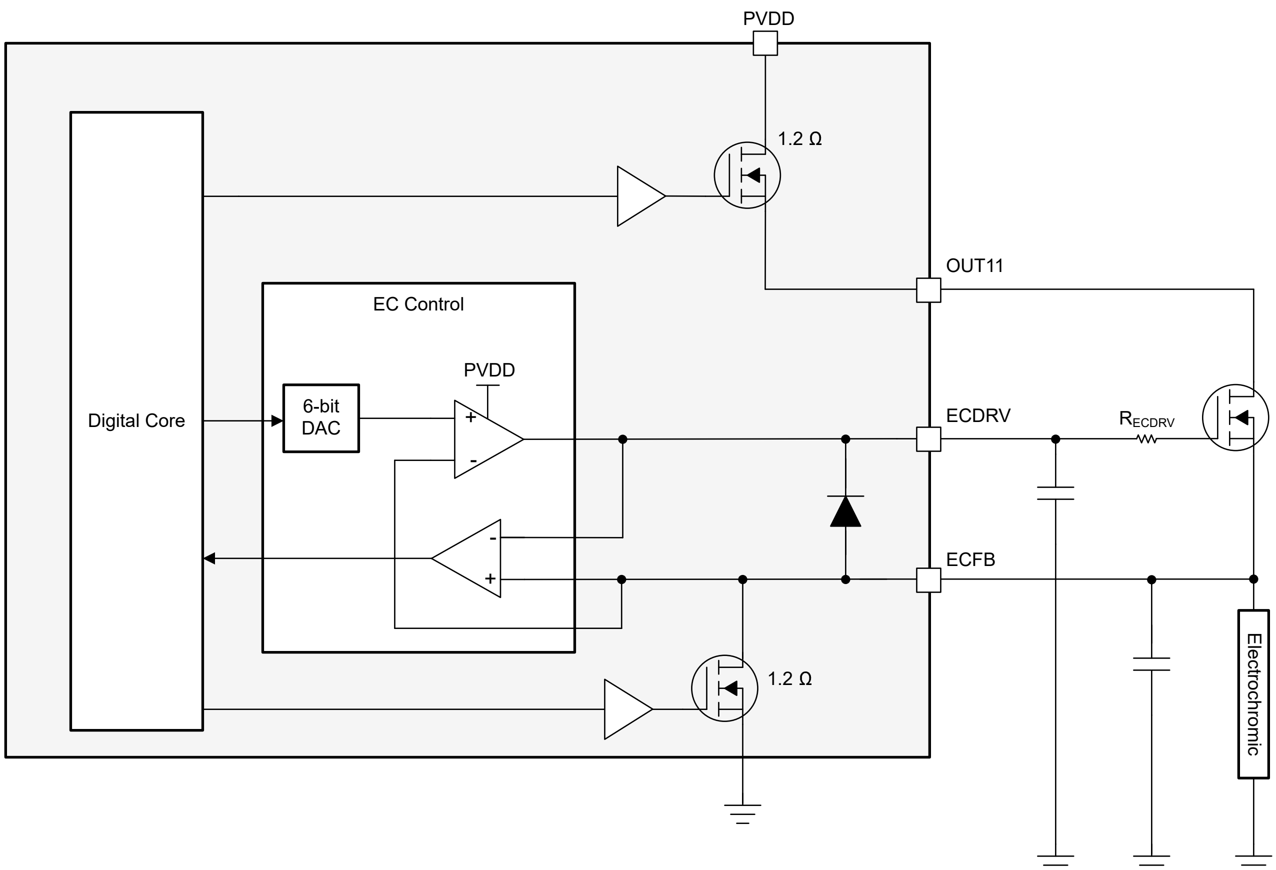


Figure 7-8. Electrochromic Driver Block Diagram - Default Configuration

Depending on the system implementation, the device electrochrome driver supports configuration where the drain of electrochrome high-side charge MOSFET can be supplied from either high-side driver OUT11, or directly from the supply voltage (PVDD). The EC control block can operate independently of the OUT11 or external FET supply (PVDD), with independent protection circuits in either configuration. This can be useful if an extra high-side driver is needed to drive another load. The main limitation in this configuration is that if the charge MOSFET fails short, the connection to supply cannot be shut off as when OUT11 is used as EC supply. A short, over voltage and open-load condition can still be detected when EC supplied with PVDD directly (OUT11 is configured as independent).

OUT11 for EC supply: This configuration is set in register HS_OC_CNFG, bit OUT11_EC_MODE. By default, OUT11_EC_MODE = 1b, which is configured as the supply for EC drive as shown in the block diagram Electrochromic Driver Block Diagram - Default Configuration. When in this configuration, bits OUT11_CNFG in register HS_HEAT_OUT_CNFG are ignored (ON/OFF, SPI/PWM). Both OUT11 and the 1.2Ω ECFB low-side discharge MOSFET have overcurrent, over voltage and passive open load detection active during EC charge and discharge states, respectfully.

PVDD for EC supply, independent OUT11: To use OUT11 as an independent high-side driver (independent of EC control) to drive a separate load, where the drain of the EC charge MOSFET is connected directly to supply voltage, set OUT11_EC_MODE = 0b in register HS_OC_CNFG.

Independent mode ITRIP regulation is valid for OUT11 when the pin is not used as EC. When OUT11 is in EC mode, no current regulation is performed even if the regulation mode is configured.

As before, the ECFB low-side discharge MOSFET protection circuits are active during EC discharge state. The diagram below shows this configuration:

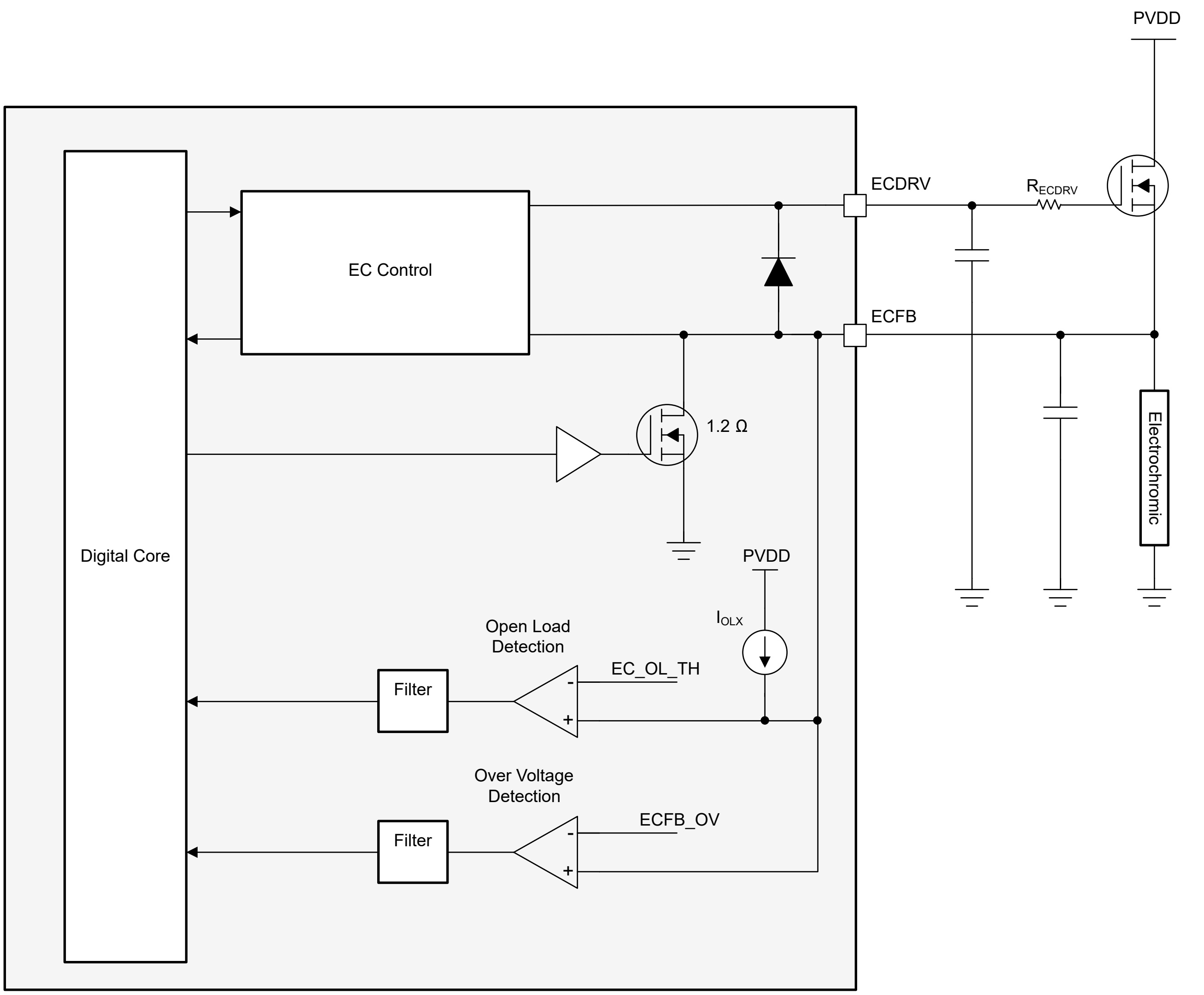


Figure 7-9. Electrochrome with direct PVDD supply (OUT11 independent)

To enable the EC driver: Set bits EC_ON and EC_V_TAR to the desired target voltage in register HS_EC_HEAT_CTRL to enable the EC driver control loop. Once these bits are set, EC driver control loop is enabled.

For EC element voltage control: Once the EC driver is enabled, the feedback loop of the driver is activated, and regulates ECFB pin voltage to the target voltage set in bits EC_V_TAR in register HS_EC_HEAT_CTRL. The target voltage on ECFB pin is binary coded with a full-scale range of either 1.5V or 1.2V, depending if bit ECFB_MAX in register EC_CNFG is set to 1 or 0, respectively. ECFB_MAX = 0b is the default value (1.2V).

Whenever a new value for the EC voltage is set, there is a blanking time t_{BLK_ECFB} of 250µs for ECFB_HI or ECFB_LO status indication of ECFB once the control loop begins regulation to the new target value.

The device provides two discharge modes: fast discharge and PWM discharge.

Fast discharge of the EC element: To fully discharge the EC element with fast discharge ECFB_LS_PWM must be set to 0b. The target output voltage EC_V_TAR must also be set to 0b, and bits ECFB_LS_EN, and EC_ON must be set to 1b in EC_CNFG. When these four conditions are met, the voltage at pin ECFB is discharged by pulling the internal 1.2Ω low-side MOSFET on ECFB pin to ground.

1. Configure ECFB_LS_PWM = 0b in register EC_CNFG
2. Set bits ECFB_LS_EN = 1b, EC_ON = 1b and EC_V_TAR = 0b in register HS_EC_HEAT_CTRL.
3. ECFB LS MOSFET is enabled and performs fast discharge of EC mirror.

PWM discharge of the EC element: The steps below outline the PWM discharge cycle of electrochrome driver:

1. Configure ECFB_LS_PWM = 1b in register EC_CNFG
2. Set bits ECFB_LS_EN = 1b, EC_ON = 1b in register HS_EC_HEAT_CTRL.
3. If the regulation loop detects V_{ECDRV} is less than V_{ECFB} and V_{ECDRV} is less than 400mV for longer than $t_{RECHARGE}$ or 3ms, the ECDRV regulator is switched off and the LS MOSFET on ECFB is activated for approximately 300ms ($t_{DISCHARGE}$). During this discharge, the ECDRV output is pulled low to prevent shoot-thru currents.
4. At the end of the discharge pulse $t_{DISCHARGE}$, the discharge MOSFET is switched off and the regulation loop is activated again with the new lower value. The regulation loop goes back to step 2, and out of regulation is again observed (V_{ECDRV} < 400mV or V_{ECDRV} < V_{ECFB}). If out of regulation condition is not met the loop goes back to normal operation state.

The diagram below shows the PWM discharge cycle of the electrochrome driver:

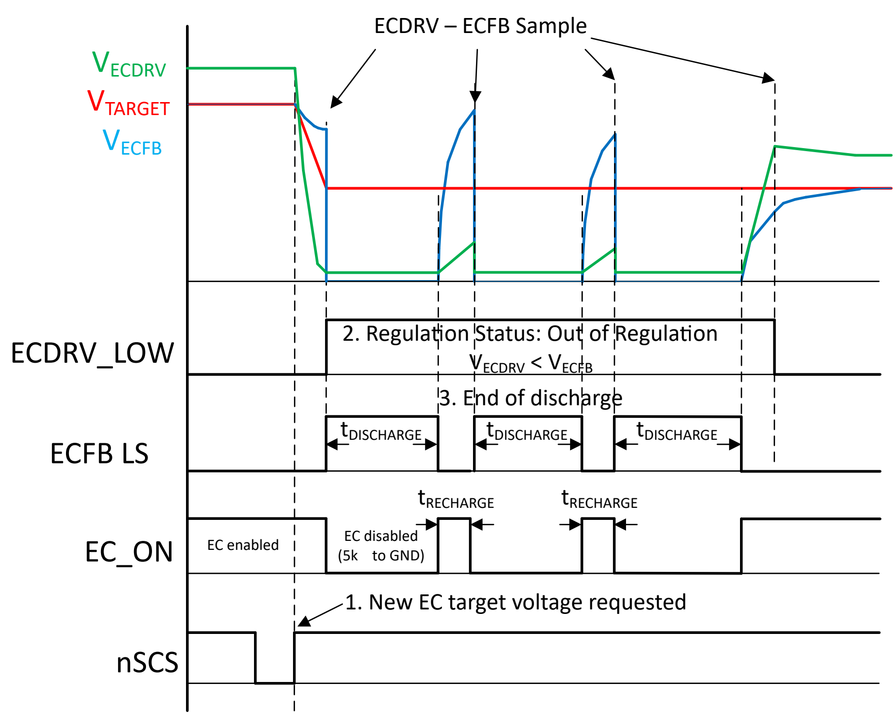


Figure 7-10. Electrochrome Discharge with PWM

The status of the voltage control loop is reported through SPI, and TI recommends to observe the report to determine the EC charge and discharge control timing. If the voltage at pin ECFB is higher than the target value by greater than 120mV, then bit ECFB_HI is set. If the voltage at pin ECFB is lower than the target value by 120mV , ECFB_LO is set. Both ECFB status bits ECFB_HI and ECFB_LO are valid if stable for at least the filter time t_{FT_ECFB}. The bits are not latched, and are not designated as global faults.

Exit discharge mode: To exit discharge mode set EC_V_TAR to a non-zero value. There is no need to change ECFB_LS_EN bit when a new target voltage is programmed, the control loop internal logic prevents both OUT11 and ECFB LS from being simultaneously on.

A capacitor of at least 4.7nF has to be added to pin ECDRV, and 220nF capacitor between ECFB and ground to increase control loop stability. For noise immunity reasons, TI recommends to place the loop capacitors as close as possible to the respective pins.

If the EC driver is not used, connect ECFB pin to ground.

7.4.3.2 Electrochromic Driver Protection

The electrochromic driver block has multiple protection and detection circuits for both charge and discharge states. There are the comparator-based detection circuits, protection circuits of OUT11 which are active during EC charge state (when configured with OUT11 as supply), and protection circuits on ECFB low-side discharge MOSFET.

EC supplied by OUT11: When the electrochrome drive is configured to be supplied by integrated high-side driver OUT11, the same protection and diagnostic functions as the other high-side drivers are available (e.g. during an overcurrent detection, the control loop is switched off). These high-side driver protections are active when the electrochrome is in the charge state (voltage ramp up). When in OUT11 EC mode (OUT11_EC_MODE = 1b), OUT11 cannot be controlled in PWM mode and EC_CNFG is used to configure diagnostics. For EC_OUT11_OCP_DG when V_{PVDD} < 20V, deglitch options (6µs, 10µs, 15µs, and 60µs) are available. For V_{PVDD} > 20V the deglitch time is automatically reduced to 10µs.

Fault on OUT11 during EC charge: In case of an overtemperature shutdown fault (zone 3 or 4) or overcurrent fault on OUT11 while EC_ON = 1b (EC control enabled):

- OUT11 is shut off (status register set)
- ECDRV pin is pulled to ground
- EC_ON remains '1'
- ECFB_LS_EN remains as programmed

To restart EC control after OUT11 failure, the controller must read and clear the corresponding fault. The driver reverts to the previous value of EC_V_TAR when restart occurs.

If an open load is detected on OUT11 during EC charge, the OUT11_OLA bit in register HS_STAT is set.

Discharge overcurrent protection LS FET: During discharge of ECFB via low-side FET(LSFET), overcurrent fault is detected if load current on ECFB pin exceeds the overcurrent threshold (I_{OC_ECFB}). Overcurrent fault response is configurable with EC_FLT_MODE bit in register EC_CNFG.

EC_FLT_MODE = 0b:

If the current through EC LSFET crosses the OCP threshold (I_{OC_ECFB}) after deglitch time, LSFET is disabled. The deglitch times for the EC LSFET depend on V_{PVDD}. For V_{PVDD} < 20V, the deglitch time is 40µs. For V_{PVDD} > 20V, the deglitch time is automatically reduced to 15µs.

EC_FLT_MODE = 1b:

If the current through EC LSFET after blank time crosses the OCP threshold (I_{OC_ECFB}) for deglitch time, the driver enters overcurrent recovery mode (OCR), similar to ITRIP regulation of HS drivers OUT7-12. Deglitch time and ITRIP frequency are taken from the OUT7 ITRIP settings.

When OCR mode is enabled and if ECFB_OV bit is high due to short from ECFB to V_{PVDD}, the driver is shutoff. The ECFB_OV deglitch time is 20µs regardless of the ECFB_OV_DG configuration settings.

Table 7-16. Discharge Overcurrent Protection

EC_FLT_MODE	Fault Response
0b	Latch (Hi-Z)
1b	Overcurrent Recovery (OUT7 ITRIP settings)

Discharge open load detection: While discharging the EC, open-load can also be detected. Bit EC_OLEN in register EC_CNFG must be set. If the load current on ECFB is below $I_{OL\_ECFB\_LS}$ for longer than $t_{DG\_OL\_ECFB\_LS}$, then the open load status bit ECFB_OL is set, and WARN bit is set in register IC_STAT1.

Short to battery/OV detection:

ECFB overvoltage or short to battery is detected when ECFB voltage exceeds threshold $V_{ECFB\_OV\_TH}$, for longer than the deglitch time $t_{ECFB\_OV\_DG}$ while EC_ON = 1. Bit ECFB_OV_MODE determines the driver ECFB overvoltage fault response. The EC overvoltage deglitch time is configured with bit ECFB_OV_DG in register EC_CNFG.

For over voltage fault response control, bit ECFB_OV_MODE can be configured in register EC_CNFG. If ECFB_OV_MODE = 00b, then no action is taken during this fault. For ECFB_OV_MODE = 01b, when ECFB voltage exceeds 3V for longer than programmed deglitch time $t_{ECFB\_OV\_DG}$, then the ECFB_OV bit is set in EC_HEAT_ITRIP_STAT register, and EC_HEAT fault bit is set in registeIC_STAT1r. For ECFB_OV_MODE = 10b, when OV on ECFB occurs, the ECDRV pin is pulled down, and the ECFB LS FET is Hi-Z. Faults are reported in the same registers as for when ECFB_OV_MODE = 01b.

The fault responses and bit values are summarized in the table below:

Table 7-17. Electrochrome Overvoltage Fault Response

ECFB_OV_MODE	Fault Response
00b	No action
01b	Report fault in register
10b	Pulldown ECDRV and ECFB LS FET, report fault in register
11b	No action

Table 7-18. EC Overvoltage Deglitch Times

ECFB_OV_DG	Deglitch Time
00b	20µs
01b	50µs
10b	100µs
11b	200µs

Short-circuit or open-load detection: The EC diagnostics can be configured to report either a short-circuit or an open load. This mode is selected by setting the ECFB_DIAG bits in the EC_CNFG register, with the requirement that the EC_ON bit must be 0b.

Table 7-19. ECFB Diagnostic Detection Options

ECFB_DIAG	Detection Setting
00b	Disabled
01b	Short-circuit
10b	Open Load

Short-circuit detection: The short-circuit detection can detect a low-impedance condition across ECFB to GND. The bits ECFB_SC_RSEL select the impedance under which a short-circuit is detected from 0.5Ω to 3Ω. The voltage $V_{ECFB\_SC\_TH}$ is compared to I_{ECFB_SC} * ECFB_SC_RSEL. The short-circuit detection below runs when the EC amplifier is off, ECFB_DIAG = 01b, and EC_ON = 0b:

- Run I_{ECFB_SC} current into the ECFB pin and wait an initial 3ms blanking time
- If the ECFB voltage is less than I_{ECFB_SC} * ECFB_SC_RSEL after enabling the short-circuit detection, register a short-circuit (ECFB_SC) by setting ECFB_DIAG_STAT = 1b.
- The I_{ECFB_SC} continues to run through ECFB pin as long as short-circuit detection is active.

Table 7-20. ECFB Diagnostic Detection Options

ECFB_SC_RSEL	Impedance Threshold
00b	0.5Ω
01b	1.0Ω
10b	2.0Ω
11b	3.0Ω

Open-load detection: The passive open load detection is active when ECFB_DIAG = 10b, EC_ON = 0b, the EC amplifier is off. An open load is detected when the output impedance is greater than 4kΩ, resulting in an ECFB voltage threshold of I_{ECFB_OLP} * 4kΩ which is $V_{ECFB\_OLP\_TH}$. The procedure for open load detection is:

- Run I_{ECFB_OLP} current into the ECFB pin and wait an initial 3ms blanking time
- If the ECFB voltage detected is greater than $V_{ECFB\_OLP\_TH}$, register an open-load condition (ECFB_OLP) by setting ECFB_DIAG_STAT = 1b.
- The I_{ECFB_OLP} continues to run through ECFB pin as long as open-load detection is active.

7.4.4 Half-bridge Drivers

Table 7-21. Half-bridge Section Table of Contents

Half-bridge Section	Link to Section
Back to Top of Feature Section	Section 7.4
Half-bridge Control	Section 7.4.4.1
Half-bridge Regulation	Section 7.4.4.4
Half-bridge Protection	Half-bridge Protection and Diagnostics

The device integrates six total half-bridge high-side and low-side FETs, supporting bidirectional drive for up to five motors; two 1.54Ω half-bridges, two 440mΩ half-bridges, one 185mΩ half-bridge, and one 155mΩ half-bridge. All of these drivers can be controlled with SPI register, PWM signal that can be sourced from the PWM1 pin or IPROPI/PWM2 pin. Each driver also has configurable current regulation feature called ITRIP. Half-bridge protection circuits include overcurrent protection, off-state and active open-load diagnostics.

The diagrams below show common configurations for the integrated half-bridges to support up to five mirror and lock motors, and all mirror motors:

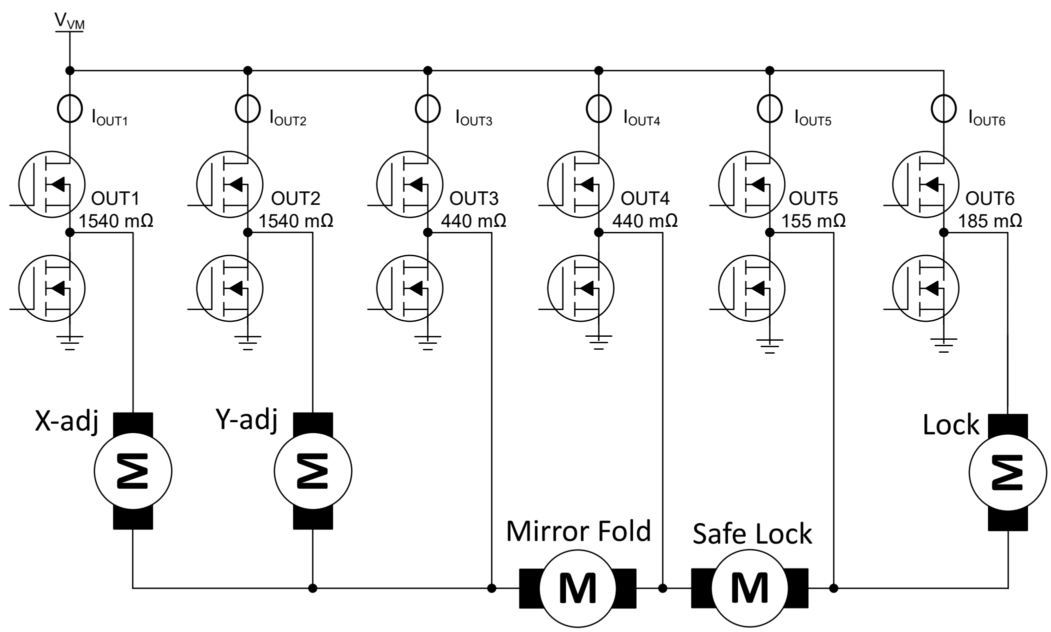


Figure 7-11. Half-bridge Configuration for up to Five Motors (Mirror and Lock)

The diagram below shows a configuration for mirror only loads:

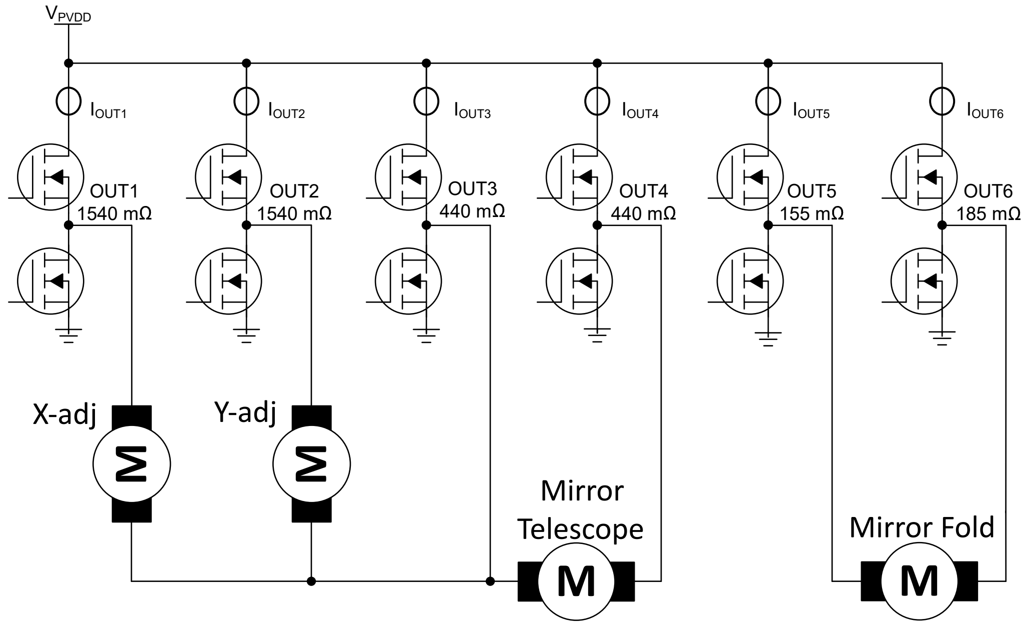


Figure 7-12. Half-bridge Configuration for up to Four Motors (Mirrors only)

7.4.4.1 Half-bridge Control

The half-bridge drivers can be controlled in two modes to support control schemes with either PWM input pins or SPI register control. The half-bridge drivers also have configuration registers (HB_OUT_CNFG1 and HB_OUT_CNFG2) to enable half-bridge control and to set up control mode (PWM or SPI).

The half-bridges can be configured for control by input signal from either PWM1 or IPROPI/PWM2 pins. The signal to PWM1 pin can be multiplexed internally to half-bridges, high-side drivers, and heater driver. IPROPI/PWM2 control from PWM2 pin is only available for half-bridges. When IPROPI/PWM2 pin is configured for PWM input, IPROPI sense output becomes unavailable. Each half-bridge driver's slew rate can be configured in the HB_SR_CNFG.

IPROPI/PWM2 is sense output by default. The configuration table is shown below. Note that OUT5 and OUT6 are configured in HB_OUT_CNFG1 and OUT1 through OUT4 are configured in HB_OUT_CNFG2:

Table 7-22. OUTX_CNFG Half-bridge Configuration

OUTX_CNFG[2]	OUTX_CNFG[1]	OUTX_CNFG[0]	OUTx	HS ON	LS ON
0	0	0	OFF	OFF	OFF
0	0	1	SPI Register Control	OUTX_CTRL	OUTX_CTRL
0	1	0	PWM 1 Complementary Control	~PWM1	PWM1
0	1	1	PWM 1 LS Control	OFF	PWM1
1	0	0	PWM 1 HS Control	PWM1	OFF
1	0	1	PWM 2 Complementary Control	~IPROPI/PWM2	IPROPI/PWM2
1	1	0	PWM 2 LS Control	OFF	IPROPI/PWM2
1	1	1	PWM 2 HS Control	IPROPI/PWM2	OFF

When the half-bridges are configured for SPI register control (OUTx_CNFG = 01b), the half-bridges high- and low-side MOSFETs can be individually controlled in register GD_HB_CTRL with bits OUTx_CTRL. The control truth table for the half-bridge outputs is shown below:

Table 7-23. Half-bridge Driver Controls

OUTx_CTRL (OUT1-6) bits	Configuration	Description
00	OFF	Half-bridge control OFF
01	HS ON	High-side MOSFET ON
10	LS ON	Low-side MOSFET ON
11	RSVD	Reserved.

The half-bridge control mode can be changed anytime SPI communication is available by writing to the bits. This change is immediately reflected.

When the half-bridges are configured for PWM operation (OUTx_CNFG = 01xb, 10xb or 11xb), the inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes.

The device automatically generates the dead-time needed during transitioning between the high-side and low-side FET on the switching half-bridge. This timing is based on internal FET gate-source voltage. No external timing is required. This scheme provides minimum dead time while preventing shoot-through current.

7.4.4.2 OUT1 and OUT2 High-side Driver Mode

OUT1 and OUT2 2 half bridges can be configured as high side drivers by setting the OUT1_MODE and OUT2_MODE bits in the HB_OUT_CNFG2 register. When OUTx_MODE is set to 1b the corresponding output operates in high-side mode.

In high side driver configuration, OUT1 and OUT2 outputs are controlled only by internal PWM generator. This control is enabled by configuring OUT1_CNFG and OUT2_CNFG to xx1b. Setting these bits to xx0b disables the outputs OUT1 and OUT2.

When configured in high-side mode, the PWM frequency for OUT1 and OUT2 can be programmed using PWM_OUT1_FREQ and PWM_OUT2_FREQ bits in the HB_ITRIP_FREQ register. The bits OUT1_DC and OUT2_DC configure the duty cycle control from internal PWM generator up to a value of 1022 (99.8% duty cycle).

Table 7-24. OUT1 or OUT2 PWM Frequency in High-side Driver Mode

PWM_OUTx_FREQ	PWM Frequency (Hz)
00b	108
01b	217
10b	289
11b	434

The same protections and diagnostic features as half-bridge mode apply to OUT1 and OUT2 in high-side mode.

7.4.4.3 Half-bridge Register Control

The half-bridges are disabled by default, once configured to operate in SPI register control mode any high-side or low-side can be enabled by configuring the individual enable bits for high-side (HS_ON) and low-side (LS_ON) in bits OUTx_CTRL in GD_HB_CTRL register.

An example can be used when connecting two half-bridges (OUT1/OUT2, OUT3/OUT4, OUT5/OUT6) as half-bridge X (OUTX) and half-bridge Y (OUTY). The high-side and low-side enable bits of a particular half-bridge are configured to drive the motor in forward mode, reverse mode, brake mode and coast mode as shown below:

Table 7-25. Motor Operation (Motor Connected between OUTX and OUTY)

nSLEEP	Half-Bridge X HS	Half-Bridge X LS	Half-Bridge Y HS	Half-Bridge Y LS	OUTX	OUTY	
0	X	X	X	X	Z	Z	Sleep
1	0	0	0	0	Z	Z	Coast
1	HS_ON = 1	LS_ON = 0	HS_ON = 0	LS_ON = 1	H	L	Forward

Table 7-25. Motor Operation (Motor Connected between OUTX and OUTY) (continued)

nSLEEP	Half-Bridge X HS	Half-Bridge X LS	Half-Bridge Y HS	Half-Bridge Y LS	OUTX	OUTY	
1	HS_ON = 0	LS_ON = 1	HS_ON = 1	LS_ON = 0	L	H	Reverse
1	HS_ON = 0	LS_ON = 1	HS_ON = 0	LS_ON = 1	L	L	Brake (low-side)
1	HS_ON = 1	LS_ON = 0	HS_ON = 1	LS_ON = 0	H	H	Brake (high-side)

7.4.4.4 Half-Bridge ITRIP Regulation

The device half-bridges have optional fixed-frequency load current regulation called ITRIP. This is done by comparing the active output current against configured current thresholds determined by OUTx_ITRIP_LVL. OUT1-2 has two possible ITRIP current thresholds, and OUT3-6 also have three current threshold options. ITRIP thresholds, enables, and timing settings are set individually for each half-bridge in the HB_ITRIP_CONFIG, HB_ITRIP_FREQ and HB_ITRIP_DG.

As this device has multiple integrated drivers which are enabled at any given time, there is freewheeling configuration intended to reduce power dissipation during ITRIP half-bridge regulation. Power dissipation is lower with synchronous rectification (MOSFETs) compared with asynchronous rectification (diodes). The half-bridge freewheeling is configurable between non-synchronous (passive freewheeling) and synchronous rectification (active freewheeling). The synchronous rectification for half-bridges during ITRIP regulation is enabled by setting bits NSR_OUTx_DIS in configuration register HB_OUT_CNFG1.

ITRIP detection is done on both high- and low-side MOSFETs of each half-bridge with blanking controlled internally.

The configurable ITRIP timing parameters are frequency and deglitch. The tables below summarize the ITRIP configuration options.

Table 7-26. Half-bridge ITRIP Synchronous Rectification Settings

NSR_OUTx_DIS	ITRIP Half-bridge Off-time Response
0b	Hi-Z
1b	complementary MOSFET ON

Table 7-27. ITRIP Current Thresholds for Half-bridges

Half-bridges	Typ ITRIP Current Thresholds	OUTx_ITRIP_LVL
OUT6	6.2 A	10b
	5.4 A	01b
	2.3 A	00b
OUT5	7.6 A	10b
	6.6 A	01b
	2.9 A	00b
OUT3 & OUT4	3.4 A	10b
	2.5 A	01b
	1.3 A	00b
OUT1 & OUT2	0.875 A	1b
	0.7 A	0b

Table 7-28. ITRIP Timing - Deglitch Options

Deglitch Time	OUTx_ITRIP_DG
2 µs	00b
5 µs	01b
10 µs	10b
20 µs	11b

Table 7-29. ITRIP Timing - Frequency Options

ITRIP Frequency	OUTx_ITRIP_FREQ
20 kHz	00b
10 kHz	01b
5 kHz	10b
2.5 kHz	11b

Note

If 20kHz ITRIP frequency is desired, the fastest deglitch time is recommended (2µs).

ITRIP regulation follows these steps:

- The low- or high-side of a half-bridge is enabled. The first ITRIP clock edge occurs when half-bridge enabled.
- If ITRIP limit is exceeded on either low- or high-side, the device waits for longer than deglitch time $t_{DG\_ITRIP\_HB}$.
- If ITRIP limit is still exceeded after the deglitch time, then either the half-bridge enters the Hi-Z state or turns on the opposite MOSFET for the remainder of the ITRIP cycle, depending on NSR_OUTx_DIS bit setting. ITRIP status bit is set, and the regulation loop restarts.
- If NSR_OUTx_DIS = 1b (synchronous rectification enabled), the current through the enabled MOSFET is monitored for current reversal. If current reversal is detected, the half-bridge output is Hi-Z for the remainder of the ITRIP cycle.

The synchronous rectification or freewheeling feature is enabled by setting bits NSR_OUTx_DIS in configuration register HB_OUT_CNFG1. When NSR_OUTx_DIS = 0b, if ITRIP occurs on either MOSFET, the half-bridge goes Hi-Z. If NSR_OUTx_DIS = 1b, if ITRIP occurs on either MOSFET, the opposite MOSFET is enabled.

For example, NSR_OUTx_DIS = 1b and OUTx_CNFG = 101b and 010b for complementary mode. If the PWM input sets HS MOSFET ON, and ITRIP is reached on HS MOSFET, the LS MOSFET turns on for the remainder of the ITRIP cycle. The HS MOSFET is turned ON at the end of the cycle. If the PWM input changes within the ITRIP period, the ITRIP counter is reset and ITRIP regulation is active while the LS MOSFET is ON.

If synchronous rectification is enabled and MOSFET turns on when ITRIP occurs, current is monitored for a current reversal, or zero-crossing detection. There is zero-crossing detection on both high-side and low-side MOSFETs. If the detected load current reaches 0A during ITRIP regulation for longer than the deglitch time, then the half-bridge output goes Hi-Z for the remainder of the ITRIP cycle. The zero-crossing deglitch time is the same ITRIP deglitch time.

The diagram below shows the ITRIP behavior for a half-bridge after configuring the OUTx_ITRIP_LVL, NSR_OUTx_DIS, HB_ITRIP_FREQ, HB_TOFF_SEL, and HB_ITRIP_DG:

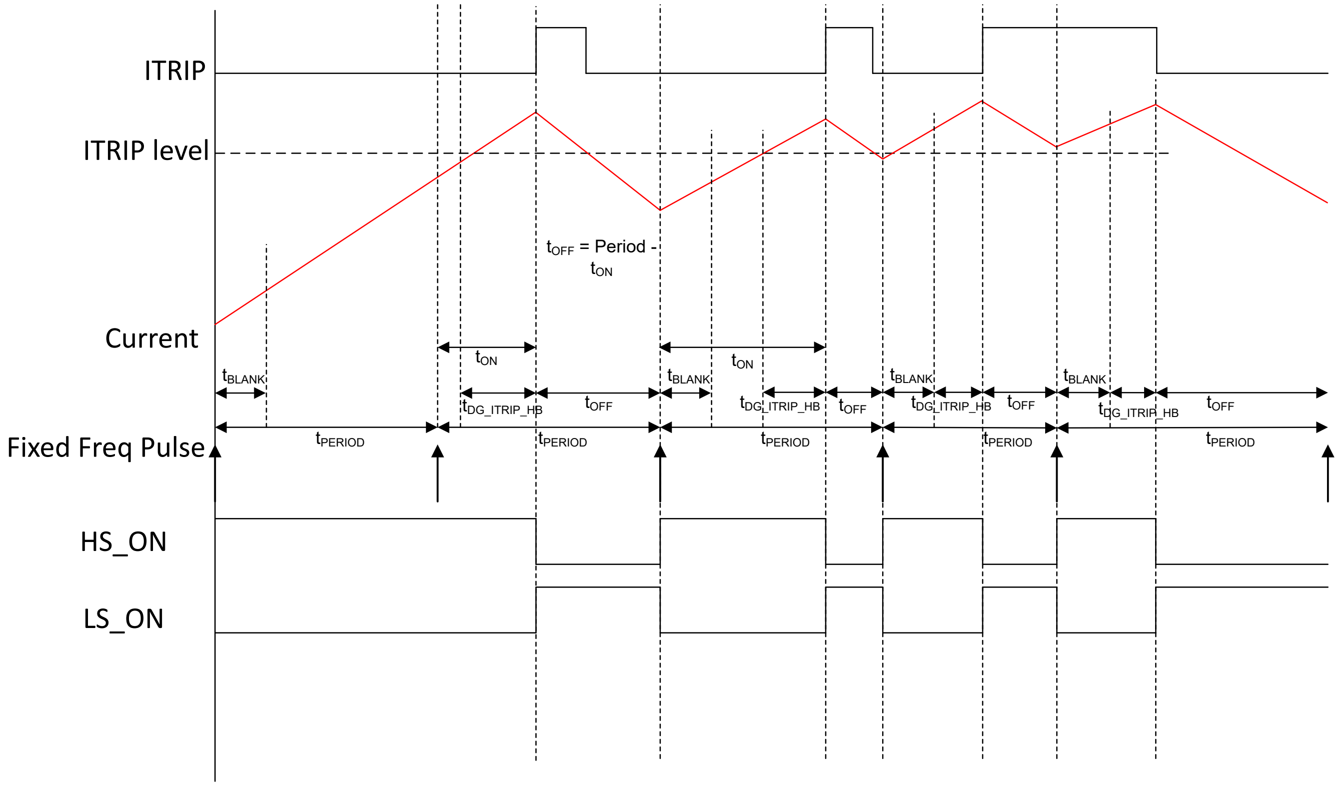


Figure 7-13. Fixed Frequency ITRIP Current Regulation for Half-bridges

The ITRIP setting can be changed at any time when SPI communication is available by writing to the OUTx_ITRIP_LVL bits. The change is immediately reflected in device behavior.

If a half-bridge is configured for PWM control and ITRIP, when ITRIP is reached, the behavior is the same as for SPI register control, but the input now comes from the configured PWM pin.

There is a minimum t_{OFF} time enforced based on the HB_TOFF_SEL bits in the HB_ITRIP_FREQ register. With this setting enabled,where Period = $1/f_{PWM}$, t_{OFF} = (Period - t_{ON}) if (Period - t_{ON}) > t_{OFF_MIN} or t_{OFF} = t_{OFF_MIN} if (Period - t_{ON}) < t_{OFF_MIN} .

For example, in the case of HB_TOFF_SEL = 01b and minimum t_{OFF} insertion of T/2.

1. If ITRIP occurs beyond 50% of duty cycle minimum fixed T/2 off time is inserted after ITRIP. The behavior is t_{OFF} = T/2.
2. If ITRIP occurs within 50% duty cycle then behavior is t_{OFF} = (Period - t_{ON}).

Table 7-30. Minimum t_{OFF} Time Options

HB_TOFF_SEL	Minimum t_{OFF} Enforced
00b	disabled, Zero
01b	T_{OFF}= T/2, 50% T
10b	T_{OFF}= T/4, 25% T
11b	T_{OFF}= T

7.4.4.5 Half-bridge Protection and Diagnostics

The half-bridge drivers are protected against overcurrent. The device also offers on-state and off-state load monitoring. Fault signaling is done through register HB_STATX.

7.4.4.5.1 Half-Bridge Off-State Diagnostics (OLP)

The user can determine the impedance on a pair of half-bridges using off-state diagnostics while the half-bridges are disabled in register HB_OUT_CNFGx. With this diagnostic, detecting the following fault conditions passively is possible:

- Output short to VM or GND < 1000 Ω
- Open load > 1.5K Ω for high-side load, VM = 13.5 V

Note

Detecting a **load short** with this diagnostic is NOT possible. However, the user can deduce this logically if an overcurrent fault (OCP) occurs when an output is actively driven, but OLP diagnostics do not report any fault when the output is disabled. Occurrence of both OCP when an output is actively drive and OLP when the output is disabled implies a terminal short (short on selected output node).

- The user can configure the following combinations
  - Internal pullup resistor (R_{OLP_PU}) on OUTx
  - Internal pulldown resistor (R_{OLP_PD}) on OUTx
  - Comparator reference level
- This combination is determined by the HB_OLP_CNFG bits in the HB_OL_CNFG1 register.
- The half-bridge pairs to be diagnosed are determined by the HB_OLP_SEL bits in the HB_OL_CNFG1 register.
- The off-state diagnostics comparator output is available on HB_OLP_STAT bit in HB_STAT2 register. The output is not latched.
- The user is expected to toggle through all the combinations and record the status bit output after the output is settled.
- Based on the input combinations and status register, the user can determine if there is a fault on the output.

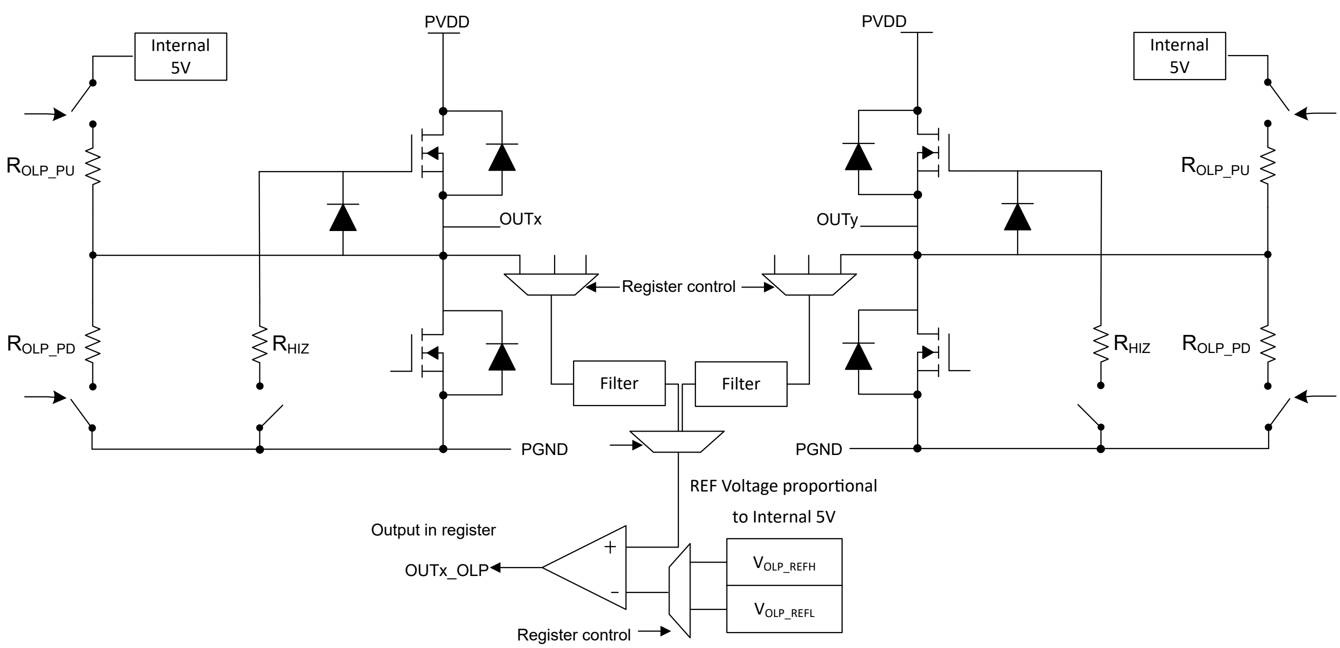


Figure 7-14. Off-State (Passive) Diagnostics

The following output, pulldown/pullup and VREF combinations are shown below:

Table 7-31. Off-state Output Pullup/pulldown and VREF Options

HB_OLP_CNFG	Description
00b	OLP Off

Table 7-31. Off-state Output Pullup/pulldown and VREF Options (continued)

HB_OLP_CNFG	Description
01b	Output X Pullup enabled, Output Y pulldown enabled, Output Y selected, VREF Low
10b	Output X Pullup enabled, Output Y pulldown enabled, Output X selected, VREF High
11b	Output X Pulldown enabled, Output Y pullup enabled, Output Y selected, VREF Low

The OLP combinations and truth table for a no fault scenario vs. fault scenario is shown in Table 7-32 For the diagnostics to be active and valid, all half-bridge configurations in bits OUTx_CNFG in registers HB_OUT_CNFGx must be zero (disabled).

Table 7-32. Off-State Diagnostics Control Table

User Inputs		OLP Set-Up				HB_OLP_STAT			
HB_OLP_CNFG	nSLEEP	OUTX	OUTY	CMP REF	Output Selected	Normal	Open	GND Short	VM Short
01b	1	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFL}	OUTY	**1b**	**0b**	**0b**	**1b**
10b	1	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFH}	OUTX	**0b**	**1b**	**0b**	**1b**
11b	1	R_{OLP_PD}	R_{OLP_PU}	V_{OLP_REFL}	OUTY	**1b**	**1b**	**0b**	**1b**

The following half-bridge pair off-state combinations and selection values are shown below.

Note

If any half-bridge is enabled, then all half-bridge OLP bits are automatically disabled and device ends off-state diagnostics.

Table 7-33. OUTx and OUTy Configurations

HB_OLP_SEL	OUTX & OUTY Pairs Selected
0000b	No output
0001b	OUT1 & OUT2
0010b	OUT1 & OUT3
0011b	OUT1 & OUT4
0100b	OUT1 & OUT5
0101b	OUT1 & OUT6
0110b	OUT2 & OUT3
0111b	OUT2 & OUT4
1000b	OUT2 & OUT5
1001b	OUT2 & OUT6
1010b	OUT3 & OUT4
1011b	OUT3 & OUT5
1100b	OUT3 & OUT6
1101b	OUT4 & OUT5
1110b	OUT4 & OUT6
1111b	OUT5 & OUT6

7.4.4.5.2 Half-bridge Open Load Detection

When the device is active and waiting for drive commands, there is an open-load detection loop for half-bridges OUT1 - OUT6. The detection scheme sequentially checks the open-load status for each high- and low-side of each half-bridge output and reports the status in bit OUTx_xx_OLA in register HB_STAT2 and WARN bit in register IC_STAT1.

From standby or sleep mode, starting with OUT1, the control loop begins checking the open-load status by comparing the current to the under-current threshold for that half-bridge after completing the open-load filter time. When running in PWM mode, this delay can be configured for 32, 128, 512, or 1024 PWM cycles with bit OUTx_OLA_TH in register HB_OL_CNFG2. The readback takes one extra cycle for example if OUTx_OLA_TH is configured for 32 cycles the value to read back is available at the end of the 33rd cycle. If an output is driven with EN/DIS only (no PWM switching) then the open-load detection delay is 10ms.

Table 7-34. Open Load Detection Cycle Delay

OUTx_OLA_TH	Delay Cycle Count
00b	32
01b	128
10b	512
11b	1024

If open-load is detected at the end of the cycle count threshold or 10ms timeout occurs, then bit OUTx_HS_OLA/ OUTx_LS_OLA is reported. If no open-load is detected after configured delay cycle count, then the loop moves to the next half-bridge. The loop continues checking each output through OUT6, then goes back to OUT1 to restart the OLA loop. For the open-load check to be valid, the half-bridge open-load detection must be enabled (OUTx_OLA = 1b) and the output OUTx_CNFG must not be disabled. The diagram below shows the OLA scheme:

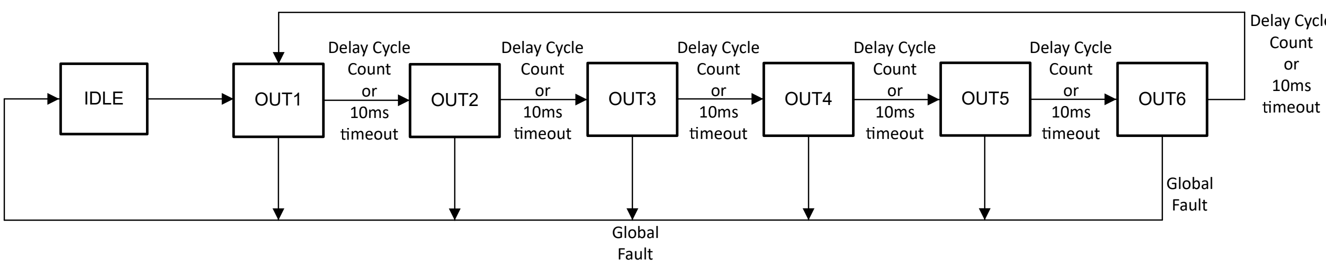


Figure 7-15. Half-bridge Open-Load Active Detection

Any given half-bridge is skipped if any of the following three conditions are met:

1. OUTx is disabled (OUTx_CNFG = 00b).
2. Open-load detect is not enabled (OUTx_OLA = 0b) for the half-bridge.
3. OUTx is OFF for more than 10ms
4. Both HS_OLA and LS_OLA have already been detected and flagged, or other fault condition on OUTx (overcurrent, over temperature)

With all half-bridge OUTx enabled without PWM, the total loop time can take up to 60ms to cycle through all half-bridges. When a half-bridge is driven individually or sequentially, the loop detects open load within 10ms or more (depending on EN or PWM control frequency). If a half-bridge is driven with a low frequency external PWM signal, the OFF time of the output can exceed the open-load detection window of 10ms, and so the half-bridge reports the status at end of timeout or number of PWM cycles less than 10ms and continue.

7.4.4.5.3 Half-Bridge Overcurrent Protection

When a half-bridge is active, an analog current protection circuit on each MOSFET shuts off the MOSFET during hard short-circuit events. If the output current exceeds the overcurrent threshold I_{OCP_OUTX} for longer than $t_{DG\_OCP\_HB}$, an overcurrent fault is detected. The corresponding output is Hi-Z (latch behavior) and the fault is latched in register (HB_STAT1). The half-bridge is disabled if V_{PVDD} > V_{PVDD_OV} configured in the PVDD_OV_MODE.

For overcurrent deglitch time $t_{DG\_OCP\_HB}$ of half-bridge drivers, there are four overcurrent deglitch options summarized in the table below.

Table 7-35. Half-bridge Overcurrent Deglitch

OUTx_OCP_DG	Voltage Limitation	Deglitch time
00b	$V_{PVDD} < V_{PVDD\_OV}$	6 µs
01b	$V_{PVDD} < V_{PVDD\_OV}$	10 µs
10b	$V_{PVDD} < V_{PVDD\_OV}$	15 µs
11b	V_{PVDD} < 20V	60 µs
	V_{PVDD} > 20V	15 µs

To re-activate the driver, the fault must first be cleared in register by the MCU by reading the status register. The diagram below shows the overcurrent behavior of a half-bridge:

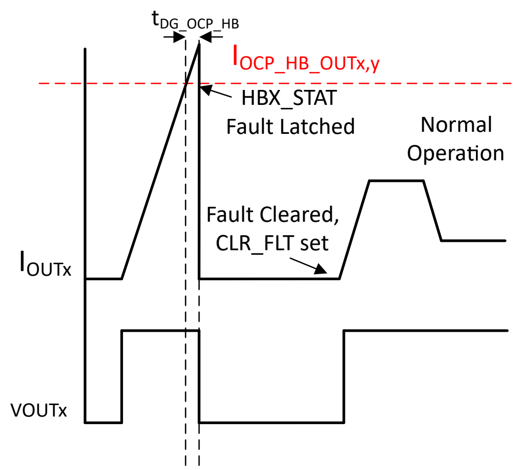


Figure 7-16. Overcurrent Behavior for Half-bridges

7.4.5 Gate Drivers

The device integrates two high-side and low-side external MOSFET gate drivers to drive one full H-bridge or two half-bridge loads. There is also an integrated current shunt amplifier which supports, high-side, low-side, and in-line current sensing.

7.4.5.1 Input PWM Modes

The DRV800x-Q1 has multiple input PWM modes to support different control schemes and output load configurations. The gate driver outputs can be controlled through the GD_IN1, GD_IN2, DRVOFF, and nSLEEP input pins. The outputs can also be controlled through the S_IN1, and S_IN2 register settings. The PWM mode is set through the SPI register setting BRG_MODE. The modes are listed below with additional details describing the functions.

Table 7-36. Input PWM Modes

Input Mode	BRG_MODE	
Section 7.4.5.1.1	00b	Independent half-bridge
Section 7.4.5.1.2	01b	(PH/EN)
	10b	(PWM)
Reserved	11b	Reserved

7.4.5.1.1 Half-Bridge Control

In half-bridge control mode, each half-bridge gate driver can be individually controlled through the corresponding IN1, IN2 pins or through register. The DRVOFF signal has priority over the IN1 and IN2 signals. For half-bridge control, INx designates half-bridges. The DRV800x-Q1 internally handles the dead-time generation between high-side and low-side switching so that a single PWM input can control each half-bridge.

The half-bridges can be configured for SPI control with INx_MODE bits. When INx_MODE = 1b, the half-bridges can be enabled with S_INx bits.

The half-bridges can be set to the Hi-Z state individually through the S_HIZx bits. Both half-bridges can be simultaneously set Hi-Z with DRVOFF pin.

Table 7-37. Half-Bridge Control (BRG_MODE = 00b)

S_HIZx	DRVOFF	INx	GHx	GLx	SHx
1	1	X	L	L	Z
0	0	0	L	H	L
0	0	1	H	L	H

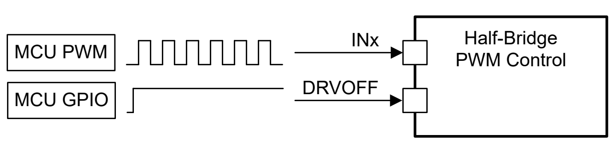


Figure 7-17. Half-Bridge Control

7.4.5.1.2 H-Bridge Control

In H-bridge control, both half-bridge gate drivers can be controlled as an H-bridge gate driver through a configurable combination of IN1 and IN2 input pins or the S_IN1 and S_IN2 bits in register GD_HB_CTRL.

To set the control mode for the half-bridge gate drivers, the SPI BRG_MODE bit can be configured to either PH/EN or PWM control modes. The PH/EN mode allows for the H-bridge to be controlled with a speed/direction type of interface commanded by one PWM signal and one GPIO signal. The PWM mode allows for the H-bridge to be controlled with a more advanced scheme typically requiring two PWM signals. This allows the H-bridge driver to enter four different output states for additional control flexibility if required.

In PH/EN mode, each half-bridge input control modes are configured with bits INx_MODE in register GD_CNFG. By default, INx_MODE = 0b and both half-bridge are controlled from pins. If INx_MODE = 1b, the half-bridge is controlled with SPI bit S_INx. If both INx_MODE = 1b, then S_IN1 becomes EN and S_IN2 becomes PH, following pins IN1 and IN2.

The H-bridge freewheeling state is configurable through the BRG_FW register setting. In both the PH/EN and PWM modes the default active freewheeling mode is active low-side. This setting can be utilized to modify the bridge between low-side or high-side active freewheeling.

The H-bridge can be set to the Hi-Z state through the PWM or PH/EN control mode, using DRVOFF pin or S_HIZx bits. The S_HIZx bits are an OR when the gate driver is in PH/EN control mode, and puts both outputs SHx into high impedance.

Table 7-38. H-Bridge PH/EN Control (BRG_MODE = 01b, INx_MODE = 0b)

DRVOFF	IN1 (EN)	IN2 (PH)	BRG_FW	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
1	X	X	X	L	L	L	L	Z	Z	High Impedance
0	0	X	0b	L	H	L	H	L	L	Low-Side Active Freewheel
0	0	X	1b	H	L	H	L	H	H	High-Side Active Freewheel
0	1	0	X	L	H	H	L	L	H	Drive SH2 → SH1 (Reverse)
0	1	1	X	H	L	L	H	H	L	Drive SH1 → SH2 (Forward)

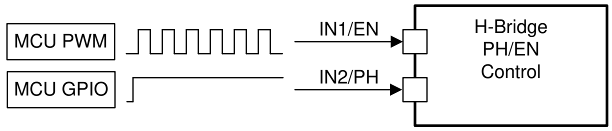


Figure 7-18. H-Bridge PH/EN Control

Table 7-39. H-Bridge PH/EN Control (BRG_MODE = 01b, IN2_MODE = 1b)

DRVOFF	IN1 (EN)	S_IN2 (PH)	BRG_FW	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
1	X	X	X	L	L	L	L	Z	Z	High Impedance
0	0	X	0b	L	H	L	H	L	L	Low-Side Active Freewheel
0	0	X	1b	H	L	H	L	H	H	High-Side Active Freewheel
0	1	0b	X	L	H	H	L	L	H	Drive SH2 → SH1 (Reverse)
0	1	1b	X	H	L	L	H	H	L	Drive SH1 → SH2 (Forward)

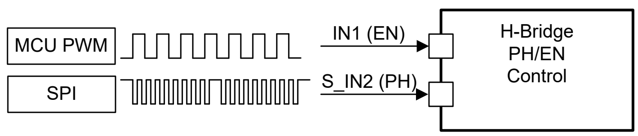


Figure 7-19. H-Bridge PH/EN Mixed Control

Table 7-40. H-Bridge PH/EN Control (BRG_MODE = 01b, IN1_MODE = 1b)

DRVOFF	S_IN1 (EN)	IN2 (PH)	BRG_FW	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
1	X	X	X	L	L	L	L	Z	Z	High Impedance
0	0b	X	0b	L	H	L	H	L	L	Low-Side Active Freewheel
0	0b	X	1b	H	L	H	L	H	H	High-Side Active Freewheel
0	1b	0	X	L	H	H	L	L	H	Drive SH2 → SH1 (Reverse)
0	1b	1	X	H	L	L	H	H	L	Drive SH1 → SH2 (Forward)

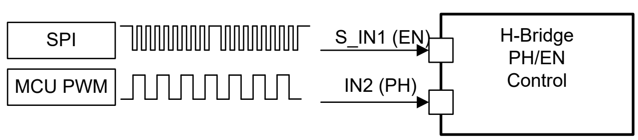


Figure 7-20. H-Bridge PH/EN Control (BRG_MODE = 01b, IN1_MODE = 1b)

Table 7-41. H-Bridge PWM Control (BRG_MODE = 10b)

DRVOFF	IN1	IN2	BRG_FW	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
1	X	X	X	L	L	L	L	Z	Z	High Impedance
0	0	0	X	L	L	L	L	Z	Z	Diode Freewheel (Coast)
0	0	1	X	L	H	H	L	L	H	Drive SH2 → SH1 (Reverse)
0	1	0	X	H	L	L	H	H	L	Drive SH1 → SH2 (Forward)
0	1	1	0b	L	H	L	H	L	L	Low-Side Active Freewheel
0	1	1	1b	H	L	H	L	H	H	High-Side Active Freewheel

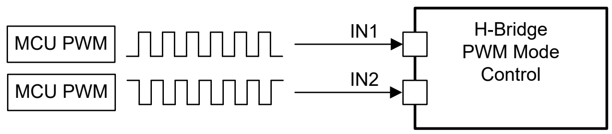


Figure 7-21. H-Bridge PWM Control

7.4.5.1.3 DRVOFF - Gate Driver Shutoff Pin

The DRV8000-Q1 provides dedicated H-bridge gate driver disable function with the DRVOFF pin. The DRVOFF pin provides a direct hardware pin to shutdown the gate driver without relying on an SPI command or PWM input change. When DRVOFF is asserted, both gate driver half-bridges are Hi-Z by enabling the gate driver pulldowns regardless of the other pin or SPI inputs. The integrated drivers and charge pump are independent from the DRVOFF pin.

The DRVOFF pin has a latched status bit DRVOFF_STAT in register GD_STAT that is continuously updated to reflect the status of the DRVOFF pin. This can be used to confirm that DRVOFF pin is either asserted or deasserted.

Note

The host controller must assert DRVOFF for more than 3ms to register a valid DRVOFF command. To properly clear the DRVOFF status latch, a CLR_FLT must be issued **after 3ms of DRVOFF going low.** TI recommends the host check DRVOFF status DRVOFF_STAT bit in register GD_STAT before and after issue a CLR_FLT to confirm that DRVOFF status has cleared. To recover from DRVOFF shutdown, wait until DRVOFF_STAT and DRVOFF_STAT_FB report HIGH after DRVOFF pin rising edge, then set DRVOFF pin to ZERO and issue CLR_FLT command.

While DRVOFF is asserted, SPI communication and logic inputs are still available as long as DVDD is present.

7.4.5.2 Smart Gate Driver - Functional Block Diagram

7.4.5.2.1 Smart Gate Driver

The DRV8000-Q1 provides an advanced, adjustable floating smart gate driver architecture to provide fine MOSFET control and robust switching performance. The smart gate driver architecture offers driver functions for slew rate control and a driver state machine for dead-time handshaking, parasitic dV/dt gate coupling prevention, and MOSFET gate fault detection.

Advanced adaptive drive functions are provided for reducing propagation delay, reducing duty cycle distortion, and closed loop programmable slew time. The advanced smart gate driver functions is available in any bridge mode, for a single half-bridge at a time. The advanced functions do not interfere with standard operation of the gate drivers and can be utilized as needed by system requirements.

The different functions of the smart gate drive architecture are summarized below with additional details in the following sections.

Smart Gate Driver Core Functions:

- Figure 7-22
- Section 7.4.5.2.3
- Section 7.4.5.2.4
- Advanced: Section 7.4.5.2.5
- Advanced: Section 7.4.5.2.9
- Advanced: Section 7.4.5.2.10

Note

The advanced, adaptive drive functions and registers are not required for normal operation of the device and intended for specific system requirements.

Table 7-42. Smart Gate Driver Terminology Descriptions

Core Function	Terminology	Description
IDRIVE / TDRIVE	I_{DRVP}	Programmable gate drive source current for adjustable MOSFET slew rate control. Configured with the IDRVP_x control register.
	I_{DRVN}	Programmable gate drive sink current for adjustable MOSFET slew rate control. Configured with the IDRVN_x control register.
	I_{HOLD}	Fixed gate driver hold pullup current during non-switching period.
	I_{STRONG}	Fixed gate driver strong pulldown current during non-switching period. This includes whenever the opposite MOSFET in the half-bridge is switching or Hi-Z.
	t_{DRIVE}	$I_{DRVP/N}$ drive current duration before I_{HOLD} or I_{STRONG}. Also provides V_{GS} and V_{DS} fault monitor blanking period. Configured with the VGS_TDRV control register.
	t_{PD}	Propagation delay from logic control signal to gate driver output change.
	t_{DEAD}	Body diode conduction period between high-side and low-side switch transition. Configured with the VGS_TDEAD control register.
PDR (Pre-charge)	I_{CHR_INIT}	Gate drive source current initial value for charge control loop. Configured with the PRE_CHR_INIT control register.
	I_{PRE_CHR}	Gate drive source current for pre-charge period after control loop lock. Adjustment rate configured with the KP_PDR control register. Max current clamp configured with the PRE_MAX control register.
	t_{PRE_CHR}	Gate drive source current pre-charge period duration. Configured with the T_PRE_CHR control register.
	t_{DON}	Delay time from start of pre-charge period to rising V_{SH} crossing V_{SH_L} threshold. Configure with T_DON_DOFF control register.
	I_{DCHR_INIT}	Gate drive sink current initial value for discharge period control loop. Configured with the PRE_DCHR_INIT control register.
	I_{PRE_DCHR}	Gate drive sink current for pre-discharge period after control loop lock. Adjustment rate configured with the KP_PDR control register. Max current clamp configured with the PRE_MAX control register.
	t_{PRE_DCHR}	Gate drive sink current pre-discharge period duration. Configured with the T_PRE_DCHR control register.
	t_{DOFF}	Delay time from start of pre-discharge period to falling V_{SH} crossing V_{SH_H} threshold. Configure with T_DON_DOFF control register.
	V_{SH_L}	Low voltage threshold for V_{SH} switch-node. Configured with the AGD_THR control register.
	V_{SH_H}	High voltage threshold for V_{SH} switch-node. Configured with the AGD_THR control register.
PDR (Post-charge)	I_{PST_CHR}	Gate drive source current for post-charge period. Adjustment rate configured with the KP_PST control register.
	t_{PST_CHR}	Gate drive source current post-charge period duration.
	I_{PST_DCHR}	Gate drive sink current for post-discharge period. Adjustment rate configured with the KP_PST control register.
	t_{PST_DCHR}	Gate drive source current post-charge period duration.
	I_{FW_CHR}	Freewheeling charge current. Configured with the FW_MAX control register.
	I_{FW_DCHR}	Freewheeling discharge current. Configured with the FW_MAX control register.

Table 7-42. Smart Gate Driver Terminology Descriptions (continued)

Core Function	Terminology	Description
STC	t_{RISE}	Time duration for V_{SHx} to cross from V_{SHx_L} to V_{SHx_H} threshold. Configured with the T_RISE_FALL control register.
	t_{FALL}	Time duration for V_{SHx} to cross from V_{SHx_H} to V_{SHx_L} threshold. Configured with the T_RISE_FALL control register.

7.4.5.2.2 Functional Block Diagram

Section 7.2 shows a high level function block diagram for the half-bridge gate driver architecture. The gate driver blocks provide a variety of functions for MOSFET control, feedback, and protection. This includes complimentary, push-pull high-side and low-side gate drivers with adjustable drive currents, control logic level shifters, V_{DS}, V_{GS}, and V_{SH} (switch-node) feedback comparators, a high-side Zener clamp, plus passive and active pulldown resistors.

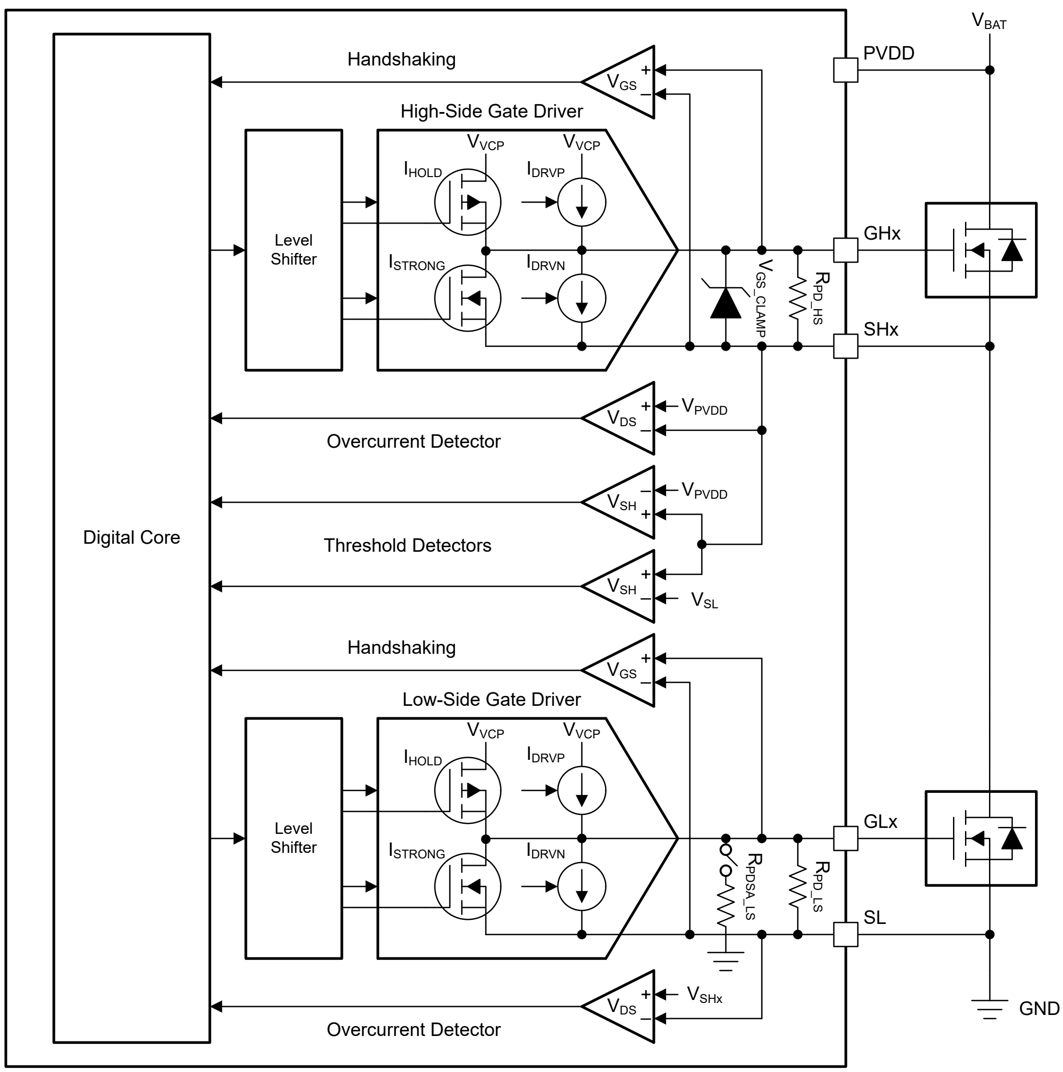


Figure 7-22. Gate Driver Functional Block Diagram

7.4.5.2.3 Slew Rate Control (IDRIVE)

The IDRIVE component of the smart gate drive architecture implements adjustable gate drive current control to adjust the external MOSFET V_{DS} slew rate. This is achieved by implementing adjustable pullup (I_{DRVP}) and pulldown (I_{DRVN}) current sources for the internal gate driver architecture.

The external MOSFET V_{DS} slew rates are a critical factor for optimizing radiated and conducted emissions, diode reverse recovery, dV/dt parasitic gate coupling, and overvoltage or undervoltage transients on the switch-node of the half-bridge. IDRIVE operates on the principle that the V_{DS} slew rates are predominantly determined by the rate of the gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By allowing the gate driver to adjust the gate current, the gate driver can effectively control the slew rate of the external power MOSFETs.

IDRIVE allows the DRV8000-Q1 to dynamically change the gate driver current setting through the IDRVP_x and IDRVN_x bits. The device provides 16 settings between the 0.5-mA and 62-mA range for the source and sink currents as shown in Table 7-43. The peak gate drive current is available for the t_{DRIVE} duration. After the MOSFET is switched and the t_{DRIVE} duration expires, the gate driver switches to a hold current (I_{HOLD}) for the pullup source current to limit the output current in case of a short-circuit condition and to improve the efficiency of the driver.

The IDRV_LOx bits allows for 16 settings <0.5mA if extremely low slew rate control is required.

Table 7-43. IDRIVE Source (I_{DRVP}) and Sink (I_{DRVN}) Current

IDRVP_x / IDRVN_x	Gate Source / Sink Current	
	IDRV_LOx = 0b	IDRV_LOx = 1b
0000b	0.5 mA	50 µA
0001b	1 mA	110 µA
0010b	2 mA	170 µA
0011b	3 mA	230 µA
0100b	4 mA	290 µA
0101b	5 mA	350 µA
0110b	6 mA	410 µA
0111b	7 mA	600 µA
1000b	8 mA	725 µA
1001b	12 mA	850 µA
1010b	16 mA	1 mA
1011b	20 mA	1.2 mA
1100b	24 mA	1.4 mA
1101b	31 mA	1.6 mA
1110b	48 mA	1.8 mA
1111b	62 mA	2.3 mA

7.4.5.2.4 Gate Driver State Machine (TDRIVE)

The TDRIVE component of the smart gate drive architecture is an integrated gate drive state machine that provides automatic dead time insertion, parasitic dV/dt gate coupling prevention, and MOSFET gate fault detection.

The first component of the TDRIVE state machine is an automatic dead time handshake. Dead time is the period of body diode conduction time between the switching of the external high-side and low-side MOSFET to prevent any cross conduction or shoot through. The gate drivers of DRV8000-Q1 use V_{GS} monitors to implement a break and then make dead time scheme by measuring the external MOSFET V_{GS} voltage to determine when to properly enable the external MOSFETs. This scheme allows the gate driver to adjust the dead time for variations in the system such as temperature drift, aging, voltage fluctuations, and variation in the external MOSFET parameters. An additional fixed digital dead time (t_{DEAD_D}) can be inserted if desired and is adjustable through the SPI registers.

The second component focuses on preventing parasitic dV/dt gate charge coupling. This is implemented by enabling a strong gate current pulldown (I_{STRONG}) whenever the opposite MOSFET in the half-bridge is switching or Hi-Z. This feature helps remove parasitic charge that couples into the external MOSFET gate when the half-bridge switch node is rapidly slewing.

The third component implements a gate fault detection scheme to detect an issue with the gate voltage. This is used to detect pin-to-pin solder defects, a MOSFET gate failure, or a gate stuck high or stuck low voltage condition. This is done by using the V_{GS} monitors to measure the gate voltage after the end of the t_{DRIVE} time. If the gate voltage has not reached the proper threshold, the gate driver reports the corresponding fault condition. To maintain a false fault is not detected, a t_{DRIVE} time is selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not impact the PWM minimum duration and terminates early if another PWM command is received.

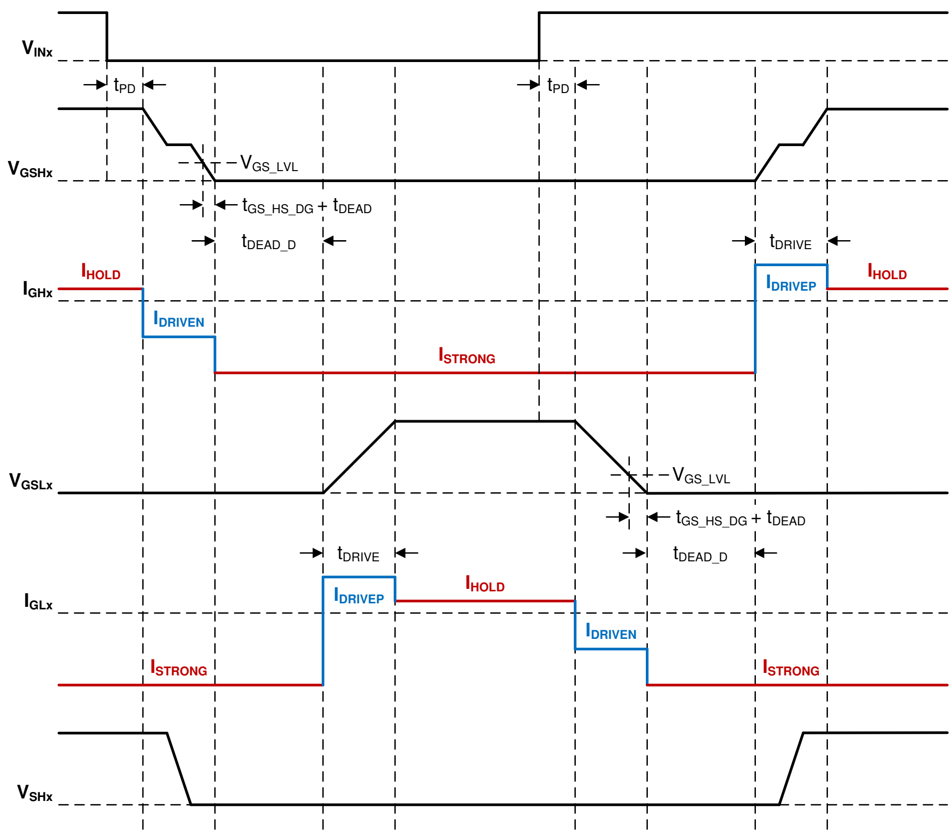


Figure 7-23. TDRIVE Turn On / Off

7.4.5.2.4.1 t_{DRIVE} Calculation Example

The driver gate to source monitor timeout (t_{DRIVE}) is configured to allow sufficient time for the external MOSFETs to charge and discharge for the selected I_{DRIVE} gate current. By default, the setting is 8us which is sufficient for many systems. The determine an appropriate t_{DRIVE} value, Equation 1 can be utilized.

$$t_{DRIVE} > Q_{G\_TOT} / I_{DRIVE} \quad (1)$$

Using the input design parameters as an example, we can calculate the approximate values for t_{DRIVE}.

$$t_{DRIVE} > 30nC / 6mA = 5us \quad (2)$$

Based on these calculations a value of 8us was chosen for t_{DRIVE}.

7.4.5.2.5 Propagation Delay Reduction (PDR)

Propagation delay reduction (PDR) control has two primary functions, a pre-charge propagation delay reduction function and a post-charge acceleration function.

The propagation delay reduction (PDR) primary goal is to reduce the turn on and turn off delay of the external MOSFET by using dynamic pre-charge and pre-discharge currents before the MOSFET Q_{GD} miller region. This can enable the driver to achieve higher and lower duty cycle resolution while still meeting difficult EMI requirements.

The post-charge acceleration function allows for the MOSFET to more quickly reach the low resistive or off state to minimize power losses by increasing the post-charge and post-discharge gate current after the MOSFET Q_{GD} miller region.

An example of the MOSFET pre-charge and post-charge current profiles are shown in PDR Charge Profile. The same control loop is repeated for the MOSFET pre-discharge and post-discharge as shown in PDR Discharge Profile. Several examples of the full control loop in different PWM and motor cases are shown in Section 7.4.5.2.8.

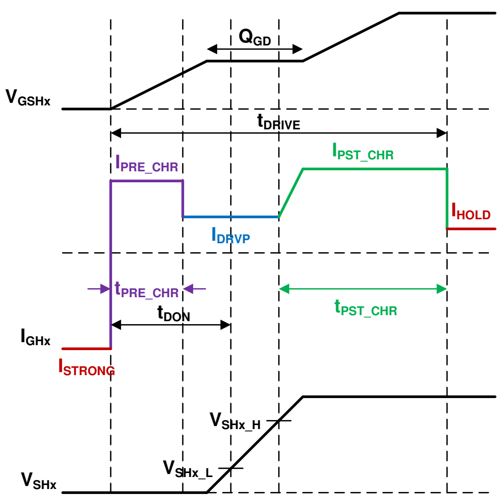


Figure 7-24. PDR Charge Profile

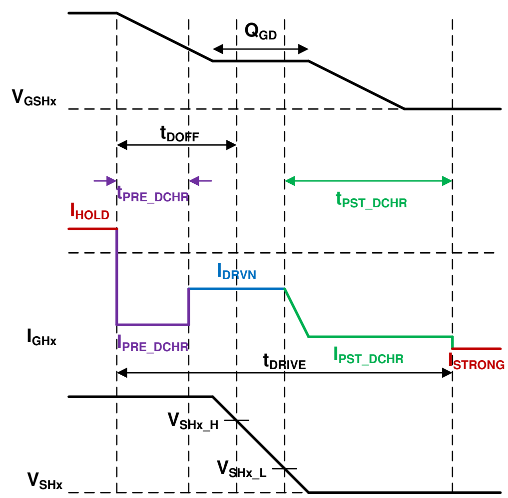


Figure 7-25. PDR Discharge Profile

7.4.5.2.6 PDR Pre-Charge/Pre-Discharge Control Loop Operation Details

The PDR pre-charge/pre-discharge control loop operates to achieve a user configured turn on and turn off propagation delay (T_DON_DOFF) by dynamically adjusting the driver pre-charge (I_{PRE_CHR}) and pre-discharge (I_{PRE_DCHR}) current levels through a proportional gain error controller (KP_PDR). The error controller measures the difference in the measured propagation delays (t_{ON}, t_{OFF}) compared to the configured propagation delay (T_DON_DOFF) and updates the pre-charge current level for the next switching cycle. The control loop can be operated with the default configuration settings of the device, but full flexibility is provided to configure the timing parameters, initial current levels, error controller strength, and other settings.

7.4.5.2.7 PDR Post-Charge/Post-Discharge Control Loop Operation Details

The PDR post charge/post-discharge control loop operates by increasing the driver gate current after the MOSFET switching region. This is done by measuring the switch-node voltage (V_{SHx}) and then increasing gate current after crossing the proper threshold. The control loop can be operated with the default configuration settings of the device, but full flexibility is provided to configure the timing parameters, controller strength, and other settings.

7.4.5.2.7.1 PDR Post-Charge/Post-Discharge Setup

- Enable the post-charge/post-discharge control loop. KP_PST register setting.
- **Optional Configuration Options:**
  - Add additional delay before post-charge/post-discharge starts. EN_PST_DLY register setting.
  - Adjust the proportional gain controller strength. KP_PST register setting.

7.4.5.2.8 Detecting Drive and Freewheel MOSFET

By default, the PDR loop automatically detects which MOSFET is the drive MOSFET and which MOSFET is the freewheel MOSFET by determining the polarity of the current out of the half-bridge. This is done by measuring the half-bridge V_{SHx} voltage during the dead-time period to determine if the high-side or low-side body diode is conducting. If the current polarity cannot be determined the IDIR_WARN is flagged in the GD_STAT register. The automatic freewheel detection can be disabled with the IDIR_MAN bit in register GD_AGD_CNFG. In the manual freewheel modes, the PDR loop relies on the IDIR_MAN_SEL bit in register GD_STC_CNFG to determine which MOSFET is the drive MOSFET and which MOSFET is the freewheel MOSFET. If = 0b, the high-side MOSFET is the drive MOSFET and the low-side MOSFET is the freewheel MOSFET. If = 1b, the low-side MOSFET is the drive MOSFET and high-side MOSFET is the freewheel MOSFET.

HS Drive PWM Turn On / Off Example shows the high-side MOSFET (HS1) controlling the V_{SHx} switch-node voltage transition and the low-side MOSFET (LS1) acting as the freewheeling MOSFET.

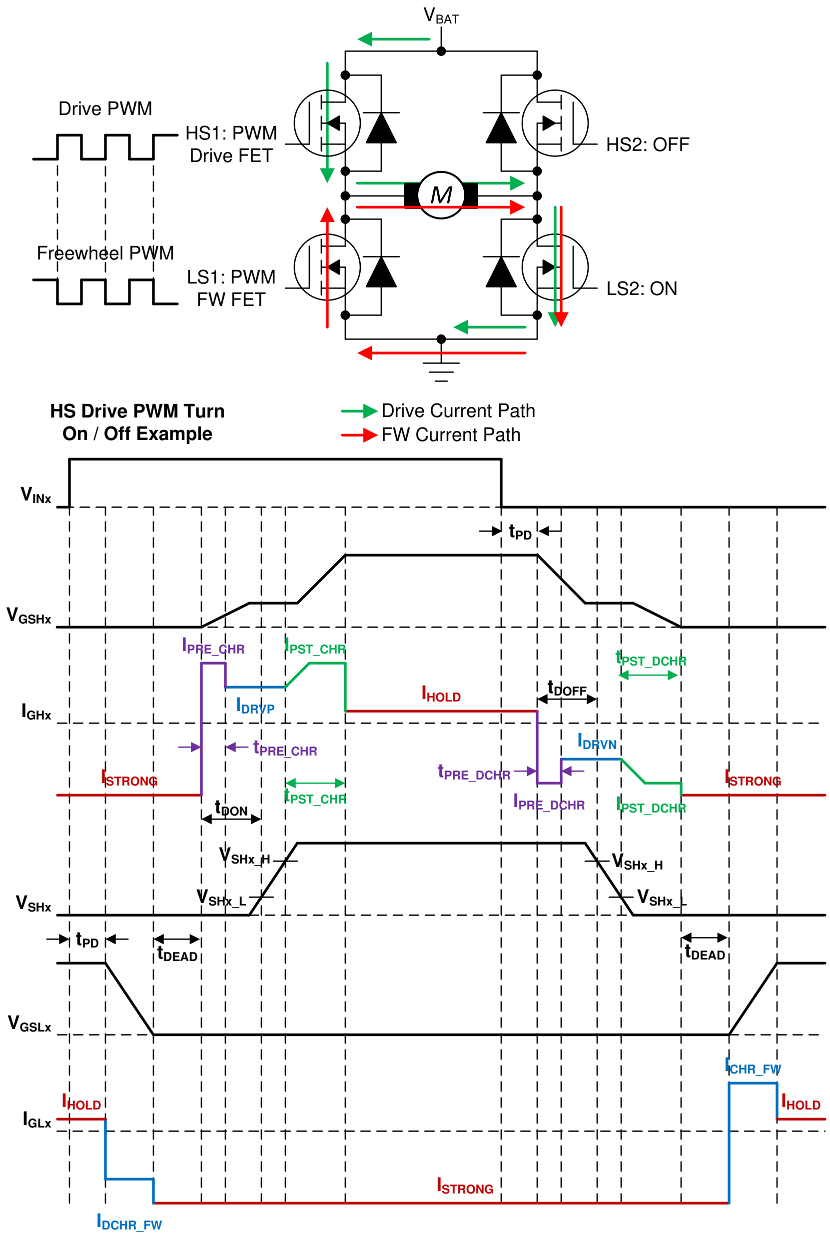


Figure 7-26. HS Drive PWM Turn On / Off Example

LS Drive PWM Turn On / Off Example shows the low-side MOSFET (LS2) controlling the V_{SHx} switch-node voltage transition and the high-side MOSFET (HS2) acting as the freewheeling MOSFET.

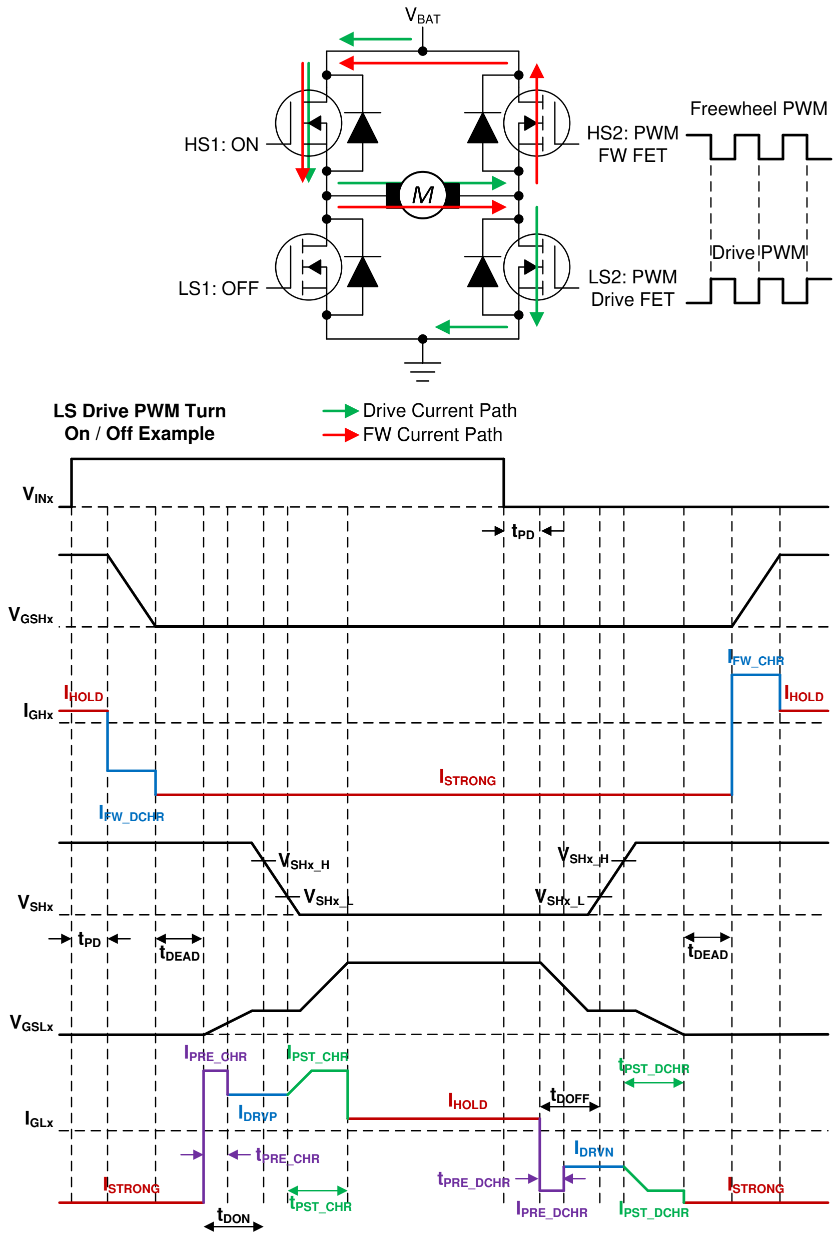


Figure 7-27. LS Drive PWM Turn On / Off Example

7.4.5.2.9 Automatic Duty Cycle Compensation (DCC)

The automatic duty cycle compensation (DCC) smart gate driver feature is a function to match the turn on and turn off signals to reduce duty cycle distortion that occurs due to different delays in the turn on and turn off sequences. The difference in turn on and turn off delay is introduced by a dependency on whether the freewheeling MOSFET must be charged or discharged before the V_{SHx} slew can occur. If the freewheeling MOSFET charges or discharges before the drive MOSFET this can introduce a mismatch causing duty cycle distortion. The DCC control loop adds an additional delay to match both the turn on and turn off delays. This function can be utilized in the standard drive modes or in combination with the PDR or STC control modes.

The DCC function is enabled through the EN_DCC bits. Set the active half-bridge receiving PWM control through the SET_AGD bits.

7.4.5.2.10 Closed Loop Slew Time Control (STC)

The slew time control (STC) loop provides the device the ability to configure a specific slew rise and fall time for the output switch-node. The device adjusts the gate drive output current (I_{DRVP} and I_{DRVN}) to meet the desired target settings. This function can be utilized in the standard drive modes or in combination with the PDR or DCC control modes.

7.4.5.2.10.1 STC Control Loop Setup

- Enable the STC control loop. EN_STC register setting
- Set the active PWM half-bridge. SET_AGD register setting. Note: The advance driver control settings are shared between each half-bridge pair.
- Set the target t_{RISE} and t_{FALL} time. T_RISE_FALL register setting.
- **Optional Configuration Options:**
- Adjust the proportional gain controller strength. KP_STC register setting.

7.4.5.3 Tripler (Double-Stage) Charge Pump

The high-side gate drive voltage for the external MOSFET is generated using a tripler (dual-stage) charge pump that operates from the PVDD voltage supply input. The charge pump allows the high-side and low-side gate drivers to properly bias the external N-channel MOSFETs with respect to the source voltage across a wide input supply voltage range. The charge pump output is regulated (VVCP) to maintain a fixed voltage respect to VPVDD. The charge pump is continuously monitored for an undervoltage (VCP_UV) event to prevent under driven MOSFET conditions or in case of a short-circuit condition.

The charge pump provides several configuration options. By default the charge pump automatically switches between tripler (dual-stage) mode and doubler (single-stage) mode after the PVDD pin voltage crosses the VCP_SO threshold to reduce power dissipation. The charge pump can also be configured to always remain in tripler or doubler mode through the SPI register setting CP_MODE.

The charge pumps requires a low ESR, 1µF, 16V ceramic capacitor (X7R recommended) between the PVDD and VCP pins to act as the storage capacitor. Additionally, a low ESR, 100nF, PVDD-rated ceramic capacitor (X7R recommended) is required between the CP1H to CP1L and CP2H to CP2L pins to act as the flying capacitors.

Note

Since the charge pump is regulated to the PVDD pin, verify that the voltage difference between the PVDD pin and MOSFET power supply is limited to a threshold that allows for proper VGS of the external MOSFET during switching operation.

7.4.5.4 Wide Common Mode Differential Current Shunt Amplifier

The device integrates a high-performance, wide common-mode, bidirectional, current-shunt amplifiers for current measurements using shunt resistors in the external half-bridges. Current measurements are commonly used to implement overcurrent protection, external torque control, or commutation with an external controller. Due to the high common-mode range of the shunt amplifier, the shunt amplifier can support low-side, high-side, or inline shunt configurations. The current shunt amplifiers include features such as programmable gain, unidirectional and bidirectional support, output blanking, and a programmable internal voltage reference to set a mid-point bias voltage for the amplifier output. A simplified block diagram is shown in Figure 7-28. SP is connected to the positive terminal of the shunt resistor and SN is connected to the negative terminal of the shunt resistor. An RC filter can be applied to the output of the amplifier as needed to the SO pin. If the amplifiers are not utilized, the SN, SP inputs can be tied to PCB GND and the SO output left floating.

Note

Note that in high-side sense configuration there exists a leakage path of approximately 600kΩ to GND when nSLEEP = 0V. TI does not recommend to add filtering to the input pins SP or SN of the Shunt Amplifier.

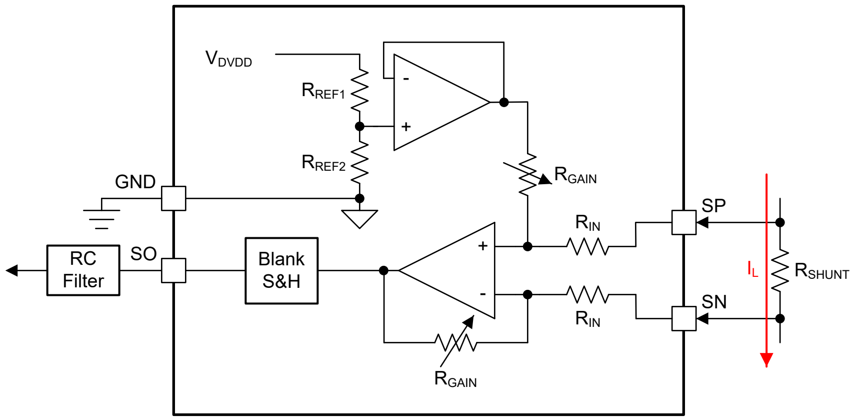


Figure 7-28. Amplifier Simplified Block Diagram

A detailed block diagram is shown in . The wide common mode amplifier is implemented with a two stage differential architecture. The 1st differential stage supports a wide common mode input, differential output, and has a fixed gain, G = 2. The 2nd differential stage supports a variable gain adjustment, G = 5, 10, 20, or 40. The total gain of the two stages are G = 10, 20, 40, or 80.

The internal reference voltage goes to a divider network, a buffer, and then sets the output voltage bias for the differential amplifier. The gain is configured through the register setting CSA_GAIN and the reference division ratio through CSA_DIV.

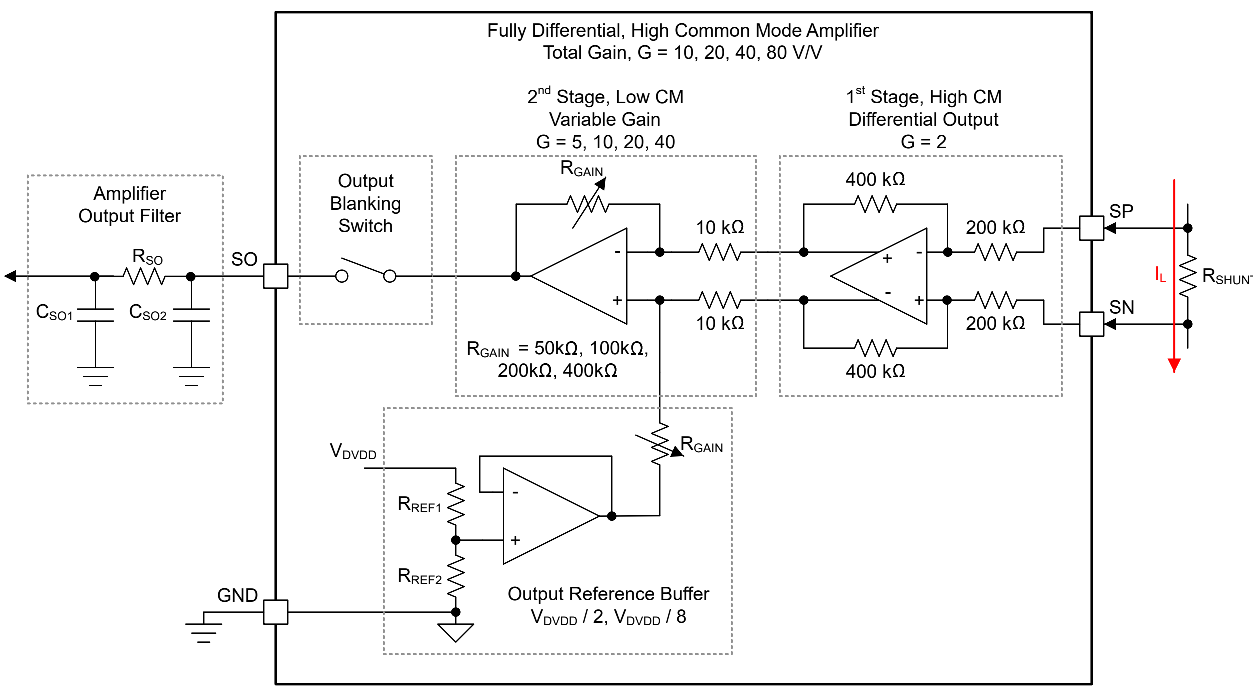


Figure 7-29. Amplifier Detailed Block Diagram

Lastly, the amplifier has an output blanking switch. The output switch can be used to disconnect the amplifier output during PWM switching to reduce output noise (blanking). The blanking circuit can be set to trigger on the active half-bridge through the CSA_BLK_SEL register setting. The blanking period can be configured through the CSA_BLK register setting. If the gate drivers are transitioning between high-side and low-side FET turn on and turn off or vice versa, the blanking time extends through the dead-time window to avoid amplifier signal noise if the output swings or noise couples during the dead-time period. An output hold up capacitor is recommended to stabilize the amplifier output C_{SO2} when the amplifier is disconnected during blanking. Typically this capacitor is after a series resistor in a RC filter configuration shown with R_{SO} and C_{SO1} to limit direct capacitance seen directly at the amplifier output. An example of the blanking function is shown in Figure 7-30.

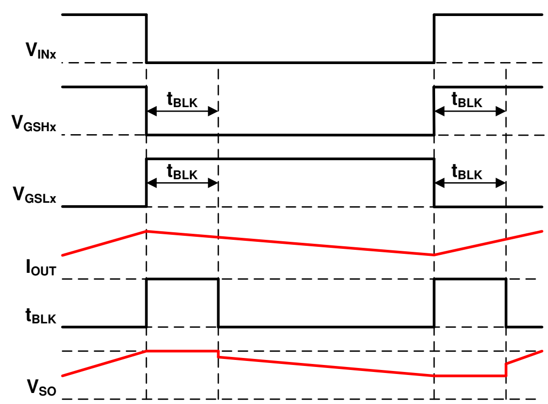


Figure 7-30. Amplifier Blanking Example

7.4.5.5 Gate Driver Protection Circuits

7.4.5.5.1 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

If the voltage across the V_{DS} overcurrent comparator exceeds the V_{DS_LVL} for longer than the t_{DS_DG} time, a V_{DS} overcurrent condition is detected. The voltage threshold and deglitch time can be adjusted through the VDS_xx_LVL and VDS_DG register settings.

The V_{DS} overcurrent monitor can respond and recover in four different modes set through the VDS_MODE register setting.

- **Latched Fault Mode:** After detecting the overcurrent event, the gate driver pulldowns are enabled and FAULT register bit, and associated VDS register bit are asserted. After the overcurrent event is removed, the fault state remains latched until CLR_FLT is issued.
- **Cycle by Cycle Mode:** After detecting the overcurrent event, the gate driver pulldowns are enabled and FAULT register bit, and associated VDS_XX register bit are asserted. The next PWM input clears the FAULT register bit and reenable the driver automatically. The associated VDS_XX register bit remains asserted until CLR_FLT is issued.
- **Warning Report Only Mode:** The overcurrent event is reported in the WARN and associated VDS_XX register bits. The device does not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The V_{DS} overcurrent monitors are disabled and does not respond or report.

When a V_{DS} overcurrent fault occurs, the gate pulldown current can be configured to increase or decrease the time to disable the external MOSFET. This can help to avoid a slow-turn off during high-current short-circuit conditions. This setting is configured through the VDS_IDRVN register setting.

7.4.5.5.2 Gate Driver Fault (VGS_GDF)

If the V_{GS} voltage does not cross the V_{GS_LVL} comparator level for longer than the t_{DRIVE} time, a V_{GS} gate fault condition is detected .

Additionally, in independent half-bridge split HS/LS PWM control (BRG_MODE = 00b) the device can be configured to disable all half-bridges or only the associated half-bridge in which the gate fault occurred through the VGS_IND register setting. In the DRV800x-Q1 PH/EN and PWM H-bridge control modes (BRG_MODE =

01b, 10b), the VGS_IND register setting can be used to disable all H-bridges or only the associated H-bridge in which the fault occurred.

The V_{GS} gate fault monitor can respond and recover in four different modes set through the VGS_MODE register setting.

- **Latched Fault Mode:** After detecting the gate fault event, the gate driver pulldowns are enabled and FAULT register bit, and associated VGS register bit asserted. After the gate fault event is removed, the fault state remains latched until CLR_FLT is issued.
- **Cycle by Cycle Mode:** After detecting the gate fault event, the gate driver pulldowns are enabled and FAULT register bit, GD and associated VGS_XX register bit asserted. The next PWM input clears the FAULT register bit and reenable the driver automatically. The VGS_XX and GD bits remains asserted until CLR_FLT is issued.
- **Warning Report Only Mode:** The overcurrent event is reported in the WARN and associated VGS_XX register bits. The device does not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The V_{GS} gate fault monitors are disabled and does not respond or report.

7.4.5.5.3 Offline Short-circuit and Open Load Detection (OOL and OSC)

The device provides the necessary hardware to conduct offline short-circuit and open load diagnostics of the external power MOSFETs and load. This is accomplished by an integrated pull up and pulldown current source on the SHx pin which connect to the external half-bridge switch-node. The offline diagnostics are controlled by the associated register bit EN_OLSC. First, the offline diagnostic mode needs to be enabled through the EN_OLSC register setting. Then the individual current sources can be enabled through the #none# and PU_SHx register settings.

The voltage on the SHx pin is continuously monitored through the internal V_{DS} comparators. During the diagnostic state the V_{DS} comparators report the real-time voltage feedback on the SHx pin node in the SPI registers in the associated VDS_XX register status bit. When in the V_{DS} comparators are in diagnostic mode, the global GD SPI register bits do not report faults or warnings.

Before enabling the offline diagnostics, TI recommends to place the external MOSFET half-bridges in the disabled state through the EN_GD register setting. Additionally, the V_{DS} comparator threshold (or) is adjusted to 1V or greater to maintain enough headroom for the internal blocking diode forward voltage drop.

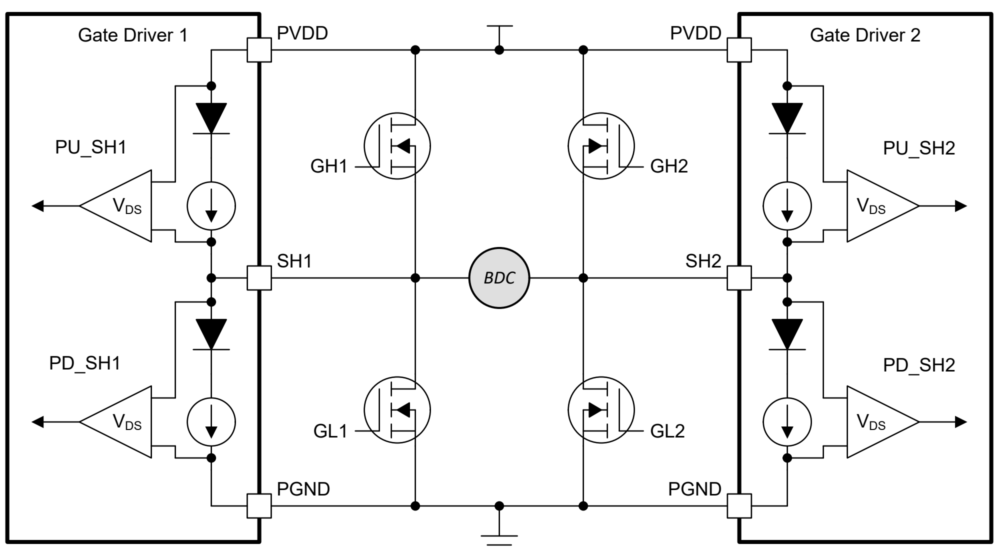


Figure 7-31. Offline Diagnostics

Note

The V_{DS} comparators start real-time voltage feedback immediately after EN_OLSC is set. Feedback is ignored until the proper pull up and pulldown configuration is set.

7.4.6 Sense Output (IPROPI)

The device features an output for current sensing, V_{PVDD} monitoring, and die temperature on the IPROPI pin. This information can be used for status or regulation of loads (on OUTx), check die temperature, or to provide local motor suppy voltage. These integrated features eliminate the need for multiple external sense resistors or sense circuitry, reducing system size, cost and complexity.

The load currents are sensed by using a shunt-less high-side current mirror topology. The IPROPI output current is a fixed ratio A_{IPROPI} of the instantaneous current of the enabled driver (OUTx). The thermal cluster outputs come from the corresponding zones temperature sensing circuits. The local motor supply PVDD sense and temperature sense is converted to a current output on IPROPI pin through the IPROPI resistor allowing scalable output voltage for 5V and 3.3V ADC pins.

For any IPROPI sense output, the maximum value of the selected scale (load current, voltage, or temperature) is represented by the maximum IPROPI output current of 2mA. For example, if OUT5 IPROPI is selected while driving an 8A load (the minimum driver OCP), the expected IPROPI output current is 2mA. If the load current is slightly higher than the minimum driver OCP, the IPROPI output current cannot be verified to follow the IPROPI current sense ratio, and in some cases OCP shutdown can occur.

Bit IPROPI_SEL defines which of the outputs is multiplexed to the IPROPI pin, the control values shown in the table below:

Table 7-44. IPROPI_SEL Options

IPROPI_SEL	Output
00000b	No output
00001b	OUT1 Current Sense
00010b	OUT2 Current Sense
00011b	OUT3 Current Sense
00100b	OUT4 Current Sense
00101b	OUT5 Current Sense
00110b	OUT6 Current Sense
00111b	OUT7 Current Sense
01000b	OUT8 Current Sense
01001b	OUT9 Current Sense
01010b	OUT10 Current Sense
01011b	OUT11 Current Sense
01100b	OUT12 Current Sense
01101b	RSVD
01110b	RSVD
01111b	RSVD
10000b	V_{PVDD} Sense Nominal Range (5V - 22V)
10001b	Thermal Cluster 1
10010	Thermal Cluster 2
10011	Thermal Cluster 3
10100	Thermal Cluster 4
10101	V_{PVDD} Sense High Range (20V - 32V)

The IPROPI pin is a multipurpose pin which can also be used as second PWM pin control input option for half-bridges, therefore the IPROPI/PWM2 pin mode is controlled with bit IPROPI_MODE in register IC_CTRL.

The diagram below shows the simple block diagram for the selectable IPROPI output:

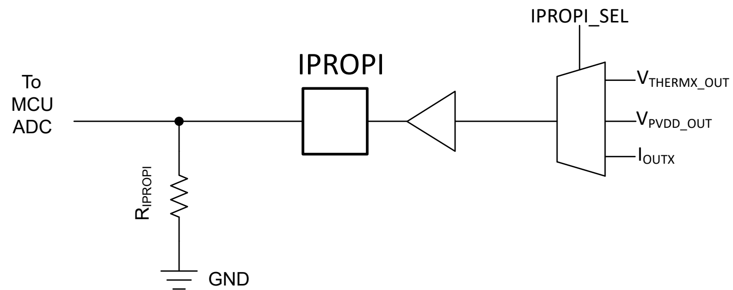


Figure 7-32. IPROPI Output Circuit

IPROPI Reset, Blank and Settling Times: When selecting between IPROPI output options from the above table, using the IPROPI_SEL bit, the IPROPI output first resets to 0V within 5.5μs. This reset occurs for any IPROPI output selection or transition. To prevent false readouts, the signal on IPROPI is blanked after switching on any driver or sense output until the circuitry settles, roughly 60μs for High-side driver.

Current (I_{OUTx}) Sense: For current output, the IPROPI output analog current is scaled by A_{IPROPI} as follows:

$$I_{IPROPI} = I_{OUTX} / A_{IPROPI} \quad (3)$$

PVDD Sense: For PVDD voltage sense output, there are two ranges:

- Nominal Range: 5V - 22V, where IPROPI output current is V_{PVDD}/11,000
- High Range: 20V - 32V, where IPROPI output current is V_{PVDD}/16,500

For example:

- IPROPI_SEL is selected for Nominal PVDD Range 1 (IPROPI_SEL = 10000b)
- V_{PVDD} is 13.5V
- I_{IPROPI} = 1.2mA

PVDD Sense Fault Behavior: The IPROPI PVDD voltage sense output is valid and available when V_{PVDD} is above the PVDD UV threshold, and when V_{DVDD} is above the minimum recommended operating voltage.

If V_{PVDD} is above the PVDD OV threshold, PVDD sense output is still supported. However, the nominal range (5V-22V) IPROPI PVDD sense output cannot be verified above V_{PVDD} > 22V. The High range IPROPI PVDD sense output ratio of 1/16,500 is valid within 20V to 32V, but cannot be verified above V_{PVDD} of 32V.

The faults where PVDD sense is unavailable:
- Charge Pump Undervoltage (VCP_UV)
- Thermal Shutdown when configured for global shutdown (default)

Temperature Sense Output: The IPROPI output also provides current representation of any single of the four thermal cluster temperature. This is intended for use in testing and evaluation, but not during device run-time.

The maximum internal temperature at which IPROPI output current is available is 195°C, at which point the IPROPI output current is 1.94mA. The IPROPI current output is scaled according to the temperature range -40°C to 195°C. The equation for the IPROPI output current is:

$I_{IPROPI} = \alpha + \beta \times t$

where α is offset roughly equal to 1.49mA, β is 2.32μA/°C, and 't' is temperature. To convert back to temperature, solving for temperature yields:

$t = (I_{IPROPI} - \alpha)/\beta$

In terms of the voltage generated on R_{IPROPI}:

$t = ([V_{IPROPI}/R_{IPROPI}] - \alpha)/\beta$

For example, when the cluster temperature is 0°C, the IPROPI output current is 1.49mA. At 145°C, the IPROPI output current is 1.83mA.

The IPROPI pin must connect to ground through an external resistor (R_{IPROPI}) generate the proportional voltage V_{IPROPI}. This allows for the IPROPI current to be measured as a voltage-drop across the R_{IPROPI} resistor in the application so that the full range of the controller ADC is utilized.

When selecting the IPROPI resistance value, note the maximum operating IPROPI output voltage of 4.7V. This value considers a 10% output error of IPROPI drives the IPROPI output voltage to 5.3V at a maximum sense value (maximum load current of a driver, for example). To stay below this voltage, use a resistance value of less than 2.35kΩ, as 2mA by 2.35kΩ is roughly 4.7V. If an MCU voltage of 3.3V is required, the resistance to stay below the MCU absolute maximum voltage, considering this 10% output error of IPROPI.

7.4.7 Protection Circuits

7.4.7.1 Fault Reset (CLR_FLT)

The DRV8000-Q1 provides a specific sequence to clear fault conditions from the driver and resume operation. This function is provided through the CLR_FLT register bit. To clear fault reporting the CLR_FLT register bit must be asserted after the fault condition is removed. After being asserted, the driver clears the fault and reset the CLR_FLT register bit.

7.4.7.2 DVDD Logic Supply Power on Reset (DVDD_POR)

If at any time the input logic supply voltage on the DVDD pin falls below the V_{DVDD_POR} threshold for longer than the $t_{DVDD\_POR\_DG}$ time or the nSLEEP pin is asserted low, the device enters the inactive state disabling the gate drivers, charge pump, OUTx outputs and protection monitors. Normal operation resumes when the DVDD undervoltage condition is removed or the nSLEEP pin is asserted high. After a DVDD power on reset (POR), the POR register bit is asserted until CLR_FLT is issued.

7.4.7.3 PVDD Supply Undervoltage Monitor (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD\_UV\_DG}$ time, the DRV8000-Q1 detects a PVDD undervoltage condition. After detecting the undervoltage condition, the gate driver pulldowns are enabled, charge pump disabled, all OUTx disabled, FAULT bit and PVDD_UV register bit are asserted.

The PVDD undervoltage monitor can recover in two different modes set through the PVDD_UV_MODE register setting.

- **Latched Fault Mode:** After the undervoltage condition is removed, the fault state remains latched and all outputs disabled until CLR_FLT is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the FAULT register bit is automatically cleared and the outputs are re-enabled. The PVDD_UV register bit remains latched until CLR_FLT is issued.

7.4.7.4 PVDD Supply Overvoltage Monitor (PVDD_OV)

In the DRV8000-Q1, there are two V_{PVDD_OV} thresholds, a low and high threshold. The overvoltage response options are dependent on the driver outputs configured (High-side, EC, Heater driver, Gate driver, Half-bridge drivers). There are two fault status bits available PVDD_OV_22V and PVDD_OV_28V in IC_STAT1.

The PVDD overvoltage monitor can respond and recover in two different modes set through the PVDD_OV_MODE register setting.

- **Latched Fault Mode (0b):** After detecting the overvoltage condition, all drivers are disabled and FAULT register bit, and PVDD_OV_22V or PVDD_OV_28V register bit are asserted. After the overvoltage condition is removed, the fault state remains latched until CLR_FLT is issued.

- **Automatic Recovery Mode (1b):** After detecting the overvoltage condition, all drivers are disabled and FAULT register bit, and PVDD_OV_22V or PVDD_OV_28V register bit asserted. After the overvoltage condition is removed, the FAULT register bit is automatically cleared and the driver automatically reenabled. The PVDD_OV_22V or PVDD_OV_28V register bit remains latched until CLR_FLT is issued.

High-side, EC and heater drivers overvoltage fault (PVDD_OV_22V):

- High-side, EC and heater drivers shutoff when V_{PVDD} > low V_{PVDD} threshold voltage (22V).
- PVDD_OV_22V fault status is defined in High-side, EC and heater drivers PVDD Overvoltage Behavior table.
- No PVDD_OV_LVL setting available for High-side, EC and heater drivers outputs
- PVDD_OV_MODE can be set to fault response Latched Fault or Automatic Recovery modes.

Table 7-45. High-side, EC and Heater Drivers PVDD Overvoltage Behavior

PVDD Voltage	High-side, EC and Heater Drivers	PVDD_OV_22V Status	PVDD_OV_28V	FAULT
V_{PVDD} < 22 V	Normal Operation	0b	Not Applicable	0b
V_{PVDD} > 22 V	Shutdown	1b	Not Applicable	1b

Half-bridges and gate driver overvoltage fault (PVDD_OV_22V or PVDD_OV_28V):

- Half-bridges and Gate drivers support warning or shutoff when V_{PVDD} > low V_{PVDD} threshold voltage (22V) or shutoff for high V_{PVDD} threshold voltage (28V).
- PVDD_OV_22V has a configurable warning or fault condition using register PVDD_OV_LVL setting available for these driver outputs as defined in Half-bridges and Gate driver PVDD Overvoltage Behavior table.
- The deglitch time for PVDD_OV_22V can be adjusted through the PVDD_OV_DG register settings.
- PVDD_OV_MODE can be set to fault response Latched Fault or Automatic Recovery modes.

Table 7-46. Half-Bridges and Gate Driver PVDD Overvoltage Behavior

PVDD_OV_LVL	PVDD Voltage	Half-Bridges and Gate Drivers	High-Side, EC and Heater Drivers	PVDD_OV_22V	PVDD_OV_28V	FAULT
0b	V_{PVDD} < 22 V	Normal Operation	Normal Operation	0b	0b	0b
0b	V_{PVDD} > 22 V	Shutdown	Shutdown	1b	0b	1b
1b	V_{PVDD} < 22 V	Normal Operation	Normal Operation	0b	0b	0b
1b	28 V> V_{PVDD} > 22 V	Normal Operation with Warning	Shutdown	1b	0b	1b
1b	V_{PVDD} > 28 V	Shutdown	Shutdown	1b	1b	1b

7.4.7.5 VCP Charge Pump Undervoltage Lockout (VCP_UV)

If at any time the voltage on the VCP pin falls below the V_{VCP_UV} threshold for longer than the $t_{VCP\_UV\_DG}$ time, the DRV8000-Q1 detects a VCP undervoltage condition. After detecting the undervoltage condition, all outputs are disabled, the gate driver pulldowns are enabled and FAULT register bit, and VCP_UV register bit is asserted. The undervoltage threshold can be adjusted through the VCP_UV_LVL register setting.

The VCP undervoltage monitor can recover in two different modes set through the VCP_UV_MODE register setting.

- **Latched Fault Mode:** Additionally the charge pump is disabled in latched fault mode. After the undervoltage condition is removed, the fault state remains latched and charge pump disabled until CLR_FLT is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the FAULT registerdfddfsdfsdfs bit is cleared and the driver automatically reenabled. The VCP_UV register bit remains latched until CLR_FLT is issued.

7.4.7.6 Thermal Clusters

As there are multiple drivers and types of drivers on this device, there are multiple dedicated thermal sensors located on chip to monitor key block temperatures on the chip. Each of these sensors, called thermal clusters, measure local die temperature for specific device blocks. These measurements are converted to a current for output on IPROPI pin, used to trigger temperature warnings or to shutdown a specific cluster which is exceeding acceptable temperature range or the entire device.

The device response to thermal cluster warnings can be configured with bit OTSD_MODE in the IC_CNFG1 register:

- Default mode (OTSD_MODE = 0b): if any cluster reaches thermal shutdown threshold for longer than t_{OTSD_DG}, the entire device is shutoff.
- Cluster mode (OTSD_MODE = 1b): if a cluster reaches thermal shutdown threshold for longer than t_{OTSD_DG}, only that cluster is shutoff.

There are four zones defined with thermal clusters, shown in the table and diagram below:

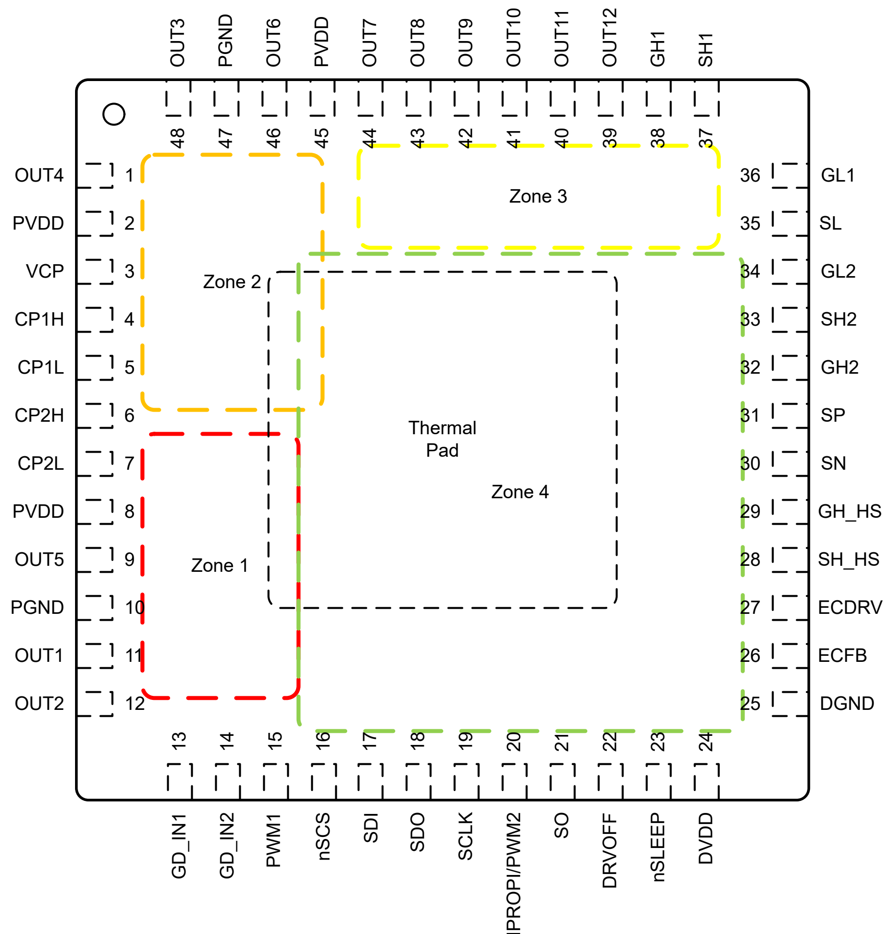


Figure 7-33. Thermal Sensor Zones

Table 7-47. Thermal Cluster Locations

Thermal Cluster 1	Thermal Cluster 2	Thermal Cluster 3	Thermal Cluster 4
OUT5, OUT1 and OUT2	OUT3, OUT4 and OUT6	High-side drivers	Global and remaining drivers

For each zone, there are comparator-based warnings for two temperature points, 125°C for low and 145°C for high. Bit ZONEX_OTW_X (L or H) is latched in register IC_STAT2. Each warning can be individually disabled with bit ZONEX_OTW_X_DIS in register IC_CNFG2. If overtemperature shutdown occurs, ZONEX_OTSD bit is latched in register IC_STAT2.

7.4.7.7 Watchdog Timer

The device integrates a programmable window type SPI watchdog timer to verify that the external controller is operating and the SPI bus integrity is monitored. The SPI watchdog timer can be enabled by through the WD_EN SPI register bit. The watchdog timer is disabled by default. When the watchdog timer is enabled, an internal timer starts to count up. The watchdog timer is reset by inverting the WD_RST SPI register. This WD_RST must be issued between the lower window time and the upper window time. If a watchdog timer fault is detected, the device response can be configured to either report only a warning or report a fault and disable all drivers. The watchdog fault can be cleared with a CLR_FLT command. If the watchdog is set to disable all drivers, the drivers are enabled after a CLR_FLT command is sent to remove the watchdog fault condition. To restart the watchdog after clear fault, disable and re-enable watchdog using WD_EN bit

7.4.7.8 Fault Detection and Response Summary Table

FAULT EVENT	CONDITION	MODE	DIGITAL CORE	CHARGE PUMP	DRIVERS	STATUS BIT	FAULT/ WARN	FUNCTIONAL RECOVERY	STATUS BIT RECOVERY
Disable Gate Driver	DRVOFF = High	N/A	Active	Active	Gate drivers are Pulldown	DRVOFF_STAT	NA	DRVOFF = Low and CLR_FLT	CLR_FLT
SPI Clock Fault	Invalid SPI Clock Frame	Latched	Active	Active	Active	SPI_OK, SCLK_FLT, Reject Frame SPI_ERR on SDO frame	NA	Valid SPI frame	CLR_FLT
SPI Address Fault	Address out of range	Latched	Active	Active	Active	SPI_ERR in SDO frame	NA	Valid SPI frame	NA
DVDD Power-on-Reset	DVDD < VDVDD_POR	NA	Reset	Disabled	Semi-Active Pulldown	POR	NA	DVDD > VDVDD_POR	CLR_FLT
PVDD Undervoltage	PVDD < VPVDD_UV	Latched	Active	Disabled	Pulldown	PVDD_UV OV/UV on SDO frame	FAULT	PVDD > VPVDD_UV and CLR_FLT	CLR_FLT
		Automatic	Active	Disabled	Pulldown	PVDD_UV OV/UV on SDO frame	FAULT	PVDD > VPVDD_UV	CLR_FLT
VCP Undervoltage	VCP < VVCP_UV	Latched	Active	Disabled	Pulldown	VCP_UV OV/UV on SDO frame	FAULT	VCP > VVCP_UV and CLR_FLT	CLR_FLT
		Automatic	Active	Active	Pulldown	VCP_UV OV/UV on SDO frame	FAULT	VCP > VVCP_UV	CLR_FLT
PVDD Overvoltage	PVDD_OV_LVL = 0 PVDD > 22V	Latched	Active	Active	Pulldown	PVDD_OV_22V OV/UV on SDO frame	FAULT	PVDD <VPVDD_OV_LO and CLR_FLT	CLR_FLT
		Automatic	Active	Active	Pulldown	PVDD_OV_22V OV/UV on SDO frame	FAULT	PVDD <VPVDD_OV_LO	CLR_FLT
	PVDD_OV_LVL = 1 28V > PVDD > 22V	Latched	Active	Active	EC, Heater and HS are Pulldown	PVDD_OV_22V OV/UV on SDO frame	FAULT	PVDD <VPVDD_OV_LO and CLR_FLT	CLR_FLT
		Automatic	Active	Active	EC, Heater and HS are Pulldown	PVDD_OV_22V OV/UV on SDO frame	FAULT	PVDD <VPVDD_OV_LO	CLR_FLT
	PVDD_OV_LVL = 1 PVDD > 28V	Latched	Active	Active	Pulldown	PVDD_OV_22V, PVDD_OV_28V OV/UV on SDO frame	FAULT	PVDD <VPVDD_OV_LO and CLR_FLT	CLR_FLT
		Automatic	Active	Active	Pulldown	PVDD_OV_22V, PVDD_OV_28V OV/UV on SDO frame	FAULT	PVDD <VPVDD_OV_LO	CLR_FLT

FAULT EVENT	CONDITION	MODE	DIGITAL CORE	CHARGE PUMP	DRIVERS	STATUS BIT	FAULT/ WARN	FUNCTIONAL RECOVERY	STATUS BIT RECOVERY
Gate Driver VDS Overcurrent	VDS > VVDS_LVL	Latched	Active	Active	Gate drivers are Pulldown	GD, VDS_Lx, VDS_Hx	FAULT	VDS<VDS_LVL and CLR_FLT	CLR_FLT
		Cycle	Active	Active	Gate drivers are Pulldown	GD, VDS_Lx, VDS_Hx	FAULT	VDS_VDS_LVL and (CLR_FLT or input cycling)	CLR_FLT
		Warning	Active	Active	Active	GD, VDS_Lx, VDS_Hx	WARN	NA	CLR_FLT
		Disabled	Active	Active	Active	NA	NA	NA	NA
VGS Gate Fault	FET OFF VGS > VVGS_LVL	Latched	Active	Active	Gate drivers are Pulldown	GD, VGS_Lx, VGS_Hx	FAULT	VGS<VVGS_LVL and CLR_FLT	CLR_FLT
		Cycle	Active	Active	Gate drivers are Pulldown	GD, VGS_Lx, VGS_Hx	FAULT	VGS<VGS_LVL and (CLR_FLT or input cycling)	CLR_FLT
		Warning	Active	Active	Active	GD, VGS_Lx, VGS_Hx	WARN	NA	CLR_FLT
		Disabled	Active	Active	Active	NA	NA	NA	NA
	FET ON VGS < VVGS_LVL	Latched	Active	Active	Gate drivers are Pulldown	GD, VGS_Lx, VGS_Hx	FAULT	VGS>VVGS_LVL and CLR_FLT	CLR_FLT
		Cycle	Active	Active	Gate drivers are Pulldown	GD, VGS_Lx, VGS_Hx	FAULT	VGS>VGS_LVL and (CLR_FLT or input cycling)	CLR_FLT
		Warning	Active	Active	Active	GD, VGS_Lx, VGS_Hx	WARN	NA	CLR_FLT
		Disabled	Active	Active	Active	NA	NA	NA	NA
Half-bridge Overcurrent Fault (OUT1-OUT6)	IOUTx > IOCPx	Latched	Active	Active	Affected driver Hi-Z	HB, OUTx_HS_OCP, OUTx_LS_OCP	FAULT	IOUTx < IOCPx and CLR_FLT	CLR_FLT
Half-bridge active open load Fault (OUT1-OUT6)	IOUTx < IOLA_OUTx	Latched	Active	Active	Active	HB, OUTx_HS_OLA,OUTx_LS_OLA	WARN	IOUTx > IOLA_OUTx and CLR_FLT	CLR_FLT
High-side Driver overcurrent Fault (OUT7-OUT12)	OUTx_ITRIP_EN =0 IOUTx > IOCx	Latched	Active	Active	Affected driver Hi-Z	HS, ITRIP, OUTx_ITRIP_STAT	FAULT	IOUTx < IOCx and CLR_FLT	CLR_FLT
High-side Driver OUTx ITRIP (OUT7-OUT12)	OUTx_ITRIP_EN =1 IOUTx > IOCx	Latched	Active	Active	Active	HS, ITRIP, OUTx_ITRIP_STAT	NA	IOUTx < IOCx	CLR_FLT
High Side driver short circuit fault (OUT7-12)	VOUTx<VSC_DET	Latched	Active	Active	Affected driver Hi-Z	HS, OUTx_OCP	FAULT	VOUTx > VSC_DET and CLR_FLT	CLR_FLT
High-side Driver open load Fault (OUT7-OUT12)	IOUTx < IOLDx	Latched	Active	Active	Active	HS, OUTx_OLA	WARN	IOUTx > IOLDx and CLR_FLT	CLR_FLT
ECFB Overvoltage	ECFB_OV_MODE=00b or 11b VECFB>VECFB_OV_TH	Disabled	Active	Active	Active	NA	NA	NA	NA
	ECFB_OV_MODE=01b VECFB>VECFB_OV_TH	Latched	Active	Active	Active	EC_HEAT, ECFB_OV	NA	NA	CLR_FLT
	ECFB_OV_MODE=10b VECFB>VECFB_OV_TH	Latched	Active	Active	EC driver Hiz	EC_HEAT, ECFB_OV	FAULT	VECFB<VECFB_OV_TH and CLR_FLT	CLR_FLT
ECFB short circuit (passive)	ECFB_DIAG=01b VECFB<VECFB_SC_TH	Automatic	Active	Active	NA	EC_HEAT, ECFB_DIAG_STAT	NA	VECFB > VECFB_SC_TH	NA
ECFB open load (passive)	ECFB_DIAG=10b VECFB >VECFB_OLP_TH	Automatic	Active	Active	NA	EC_HEAT, ECFB_DIAG_STAT	NA	VECFB <VECFB_OLP_TH	NA
ECFB Above Target Voltage	VECFB>VECFB_HI	Automatic	Active	Active	Active	EC_HEAT, ECFB_HI	NA	VECFB<VECFB_HI	NA

FAULT EVENT	CONDITION	MODE	DIGITAL CORE	CHARGE PUMP	DRIVERS	STATUS BIT	FAULT/ WARN	FUNCTIONAL RECOVERY	STATUS BIT RECOVERY
ECFB Below Target Voltage	VECFB<VECFB_LO	Automatic	Active	Active	Active	EC_HEAT, ECFB_LO	NA	VECFB>VECFB_LO	NA
ECFB Overcurrent (discharge)	EC_FLT_MODE= 0b IECFB> IOC_ECFB	Latched	Active	Active	ECFB Hi-Z	EC_HEAT, ECFB_OC	FAULT	IECFB< IOC_ECFB and CLR_FLT	CLR_FLT
ECFB Open load active (discharge)	IECFB< IOL_ECFB_LS	Latched	Active	Active	Active	EC_HEAT, ECFB_OL	WARN	IECFB> IOL_ECFB_LS and CLR_FLT	CLR_FLT
Heater VDS Overcurrent Fault	VHEAT_VDS > VDS_LVL_HEAT	Latched	Active	Active	Heater is Pulldown	EC_HEAT,HEAT_VDS	FAULT	VHEAT_VDS < VDS_LVL_HEAT and CLR_FLT	CLR_FLT
		Cycle	Active	Active	Heater is Pulldown	EC_HEAT,HEAT_VDS	FAULT	VHEAT_VDS < VDS_LVL_HEAT and (CLR_FLT or PWM)	CLR_FLT
		Warning	Active	Active	Active	EC_HEAT,HEAT_VDS	WARN	NA	CLR_FLT
		Disabled	Active	Active	Active	NA	NA	NA	NA
Heater VDS Open load Fault	VSH_HS > VOL_HEAT	Latched	Active	Active	Heater is Pulldown	EC_HEAT,HEAT_OL	FAULT	VSH_HS < VOL_HEAT and CLR_FLT	CLR_FLT
Zone X Thermal Warning	TJ > TOTW1,TOTW2	Automatic	Active	Active	Active	OTW, ZONEx_OTW_L, ZONEx_OTW_H	NA	TJ < TOTW1,TOTW2	NA
Zone X Thermal Shutdown	TJ > TOTSD	Latched	Active	Disabled	Semi-Active Pulldown, Hi-Z	OTSD, ZONEx_OTSD	FAULT	TJ < TOTSD and CLR_FLT	CLR_FLT
Watchdog	WD_FLT_M=0b , Invalid Access or Expiration	Warning	Active	Active	Active	WD_FLT	WARN	CLR_FLT and WD_EN disable and re-enable	CLR_FLT
Watchdog	WD_FLT_M=1b , Invalid Access or Expiration	Latched	Active	Active	Pulldown	WD_FLT	FAULT	CLR_FLT and WD_EN disable and re-enable	CLR_FLT

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI)

An SPI bus is used to set device configurations, operating parameters, and read out diagnostic information on the DRV8000-Q1 device. The SPI operates in peripheral mode and connects to a controller. The SPI input data (SDI) word consists of a 24 bit word, with an 8 bit command and 16 bits of data. The SPI output data (SDO) word for read commands consists of the fault status indication bits and then the register data being accessed for read commands. The SDO word for write commands consists of the fault status followed by the existing data in the written register. The data sequence between the MCU and the SPI peripheral driver is shown in Figure 7-34.

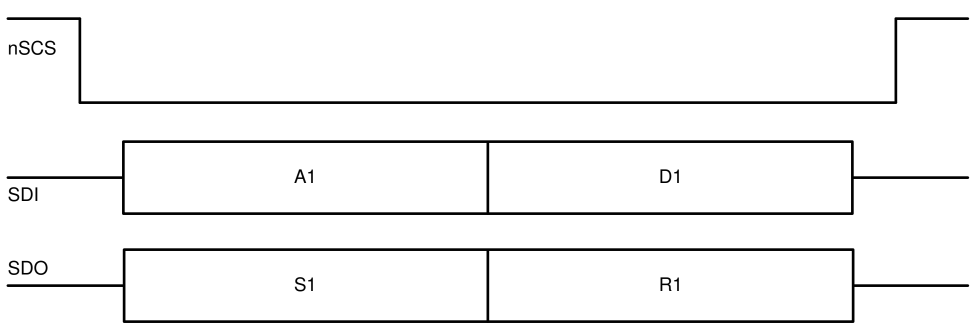


Figure 7-34. SPI Data Frame

A valid frame must meet the following conditions:

- The SCLK pin is pulled low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin is pulled high between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 24 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 24 bits, a frame error (SCLK_FLT) occurs and the data word is ignored.
- For a write command, following the 16-bit command data, the existing data in the register being written to is shifted out on the SDO pin starting with fault status byte then 16-bit data .

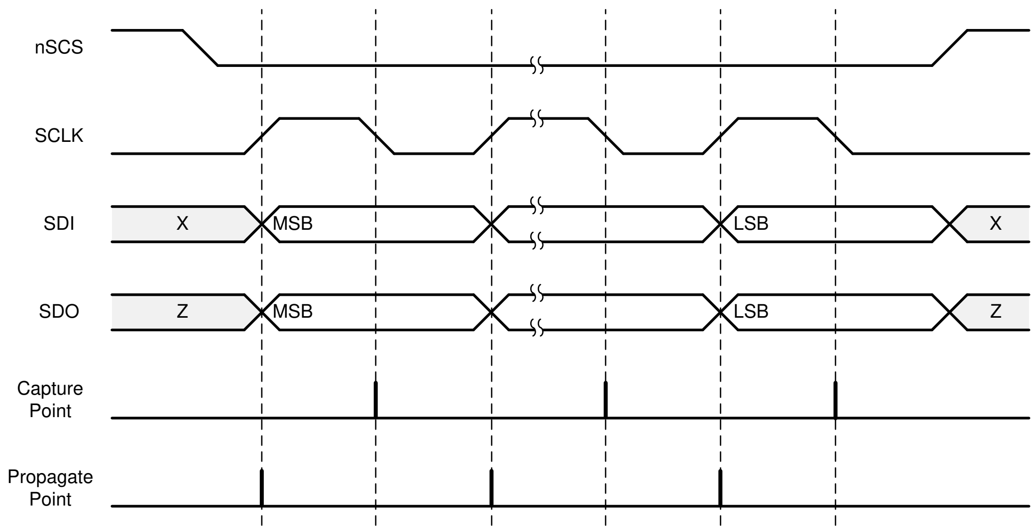


Figure 7-35. SPI peripheral Timing Diagram

7.5.2 SPI Format

The SDI input data word is 24 bits long and consists of the following format:

- MSB bit indicates frame type (bit B23 = 0 for standard frame)
- 1 read or write bit, W (bit B22, write = 0, read = 1)
- 6 address bits, A (bits B21 through B16)
- 16 data bits, D (bits B15 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

Table 7-48. SDI Input Data Word Format

		R/W	Address						Data															
Bit	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The SDO output data word is 24 bits long and the first 8 bits makes up the IC status register. The report word is the content of the register being accessed.

For a write command (W0 = 0), the response word consists of the fault status indication bits followed by the existing data in the register being written to.

For a read command (W0 = 1), the response word consists of the fault status indications bits followed by the data currently in the register being read.

Table 7-49. SDO Output Data Word Format

	IC Status								Report							
Bit	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8
									B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	FAULT	WARN	OV_UV	DRV	OTSD	SPI_ERR	D15	D14	D13	D12	D11	D10	D9	D8
									D7	D6	D5	D4	D3	D2	D1	D0

- FAULT - 'OR' of any device fault (global or driver)
- WARN - 'OR' of any device warnings
- OV_UV - 'OR' of PVDD, VCP overvoltage and undervoltage status
- DRV - 'OR' of any driver fault
- OTSD - Set when over temperature shutdown occurs
- SPI_ERR - Set when incorrect number of SCLKs received

7.5.3 Timing Diagrams

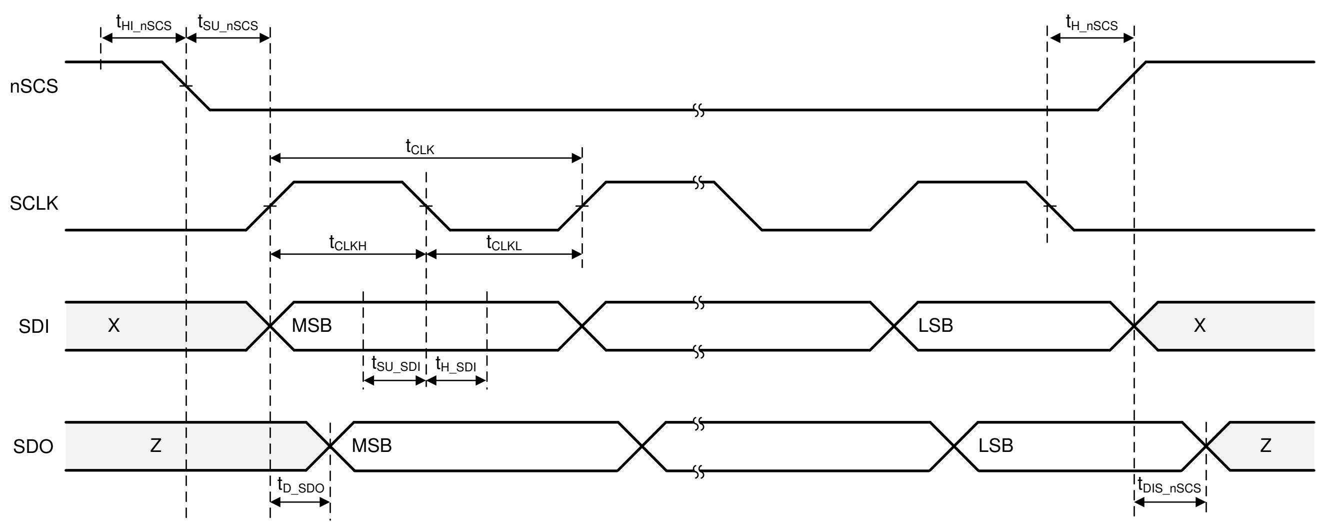


Figure 7-36. SPI Timing Diagram

8 DRV8000-Q1 Register Map

DRV8000-Q1 Register Map lists the memory-mapped registers for the DRV8000-Q1. All register addresses not listed are considered as reserved locations and the register contents are not modified. Descriptions of reserved locations are provided for reference only. The device ID table summarizes the device IDs for DRV800x devices.

Table 8-1. Device ID Summary

Device	Device ID
DRV8000-Q1	Reg Address 0x8h, DEVICE_ID=0x02
DRV8001-Q1	Reg Address 0x8h, DEVICE_ID=0x12
DRV8002-Q1	Reg Address 0x8h, DEVICE_ID=0x22

Table 8-2. DRV8000-Q1 Register Map

<table>
<tr><th rowspan="2">Name</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th rowspan="2">Type</th><th rowspan="2">Addr</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="2">IC_ STAT1</td><td>SPI_OK</td><td>POR</td><td>FAULT</td><td>WARN</td><td>GD</td><td>HB</td><td>EC_HEAT</td><td>HS</td><td rowspan="2">R</td><td rowspan="2">00h</td></tr>
<tr><td>PVDD_UV</td><td>PVDD_OV_22V</td><td>VCP_UV</td><td>OTW</td><td>OTSD</td><td>WD_FLT</td><td>ITRIP</td><td>PVDD_OV_28V</td></tr>
<tr><td rowspan="2">IC_STAT2</td><td>DEVICE_ERR</td><td>RSVD</td><td>SCLK_FLT</td><td>RSVD</td><td>ZONE4_OTSD</td><td>ZONE3_OTSD</td><td>ZONE2_OTSD</td><td>ZONE1_OTSD</td><td rowspan="2">R</td><td rowspan="2">01h</td></tr>
<tr><td>ZONE4_OTW_H</td><td>ZONE3_OTW_H</td><td>ZONE2_OTW_H</td><td>ZONE1_OTW_H</td><td>ZONE4_OTW_L</td><td>ZONE3_OTW_L</td><td>ZONE2_OTW_L</td><td>ZONE1_OTW_L</td></tr>
<tr><td rowspan="2">GD_STAT</td><td>DRVOFF_STAT_FB</td><td>DRVOFF_STAT</td><td>STC_WARN_R</td><td>STC_WARN_F</td><td>PCHR_WARN</td><td>PDCHR_WARN</td><td>IDIR</td><td>IDIR_WARN</td><td rowspan="2">R</td><td rowspan="2">02h</td></tr>
<tr><td>VGS_L2</td><td>VGS_H2</td><td>VGS_L1</td><td>VGS_H1</td><td>VDS_L2</td><td>VDS_H2</td><td>VDS_L1</td><td>VDS_H1</td></tr>
<tr><td rowspan="2">HB_STAT1</td><td colspan="2">RSVD</td><td>OUT6_LS_OCP</td><td>OUT5_LS_OCP</td><td>OUT4_LS_OCP</td><td>OUT3_LS_OCP</td><td>OUT2_LS_OCP</td><td>OUT1_LS_OCP</td><td rowspan="2">R</td><td rowspan="2">03h</td></tr>
<tr><td colspan="2">RSVD</td><td>OUT6_HS_OCP</td><td>OUT5_HS_OCP</td><td>OUT4_HS_OCP</td><td>OUT3_HS_OCP</td><td>OUT2_HS_OCP</td><td>OUT1_HS_OCP</td></tr>
<tr><td rowspan="2">HB_STAT2</td><td colspan="3">RSVD</td><td>HB_OLP_STAT</td><td>OUT6_LS_OLA</td><td>OUT5_LS_OLA</td><td>OUT4_LS_OLA</td><td>OUT3_LS_OLA</td><td rowspan="2">R</td><td rowspan="2">04h</td></tr>
<tr><td>OUT2_LS_OLA</td><td>OUT1_LS_OLA</td><td>OUT6_HS_OLA</td><td>OUT5_HS_OLA</td><td>OUT4_HS_OLA</td><td>OUT3_HS_OLA</td><td>OUT2_HS_OLA</td><td>OUT1_HS_OLA</td></tr>
<tr><td rowspan="2">EC_HEAT_ITRIP_STAT</td><td>ECFB_DIAG_STAT</td><td>ECFB_OV</td><td>ECFB_HI</td><td>ECFB_LO</td><td>ECFB_OC</td><td>ECFB_OL</td><td>HEAT_OL</td><td>HEAT_VDS</td><td rowspan="2">R</td><td rowspan="2">05h</td></tr>
<tr><td>RSVD</td><td>OUT7_ITRIP_STAT</td><td>OUT6_ITRIP_STAT</td><td>OUT5_ITRIP_STAT</td><td>OUT4_ITRIP_STAT</td><td>OUT3_ITRIP_STAT</td><td>OUT2_ITRIP_STAT</td><td>OUT1_ITRIP_STAT</td></tr>
<tr><td rowspan="2">HS_STAT</td><td colspan="2">RSVD</td><td>OUT12_OLA</td><td>OUT11_OLA</td><td>OUT10_OLA</td><td>OUT9_OLA</td><td>OUT8_OLA</td><td>OUT7_OLA</td><td rowspan="2">R</td><td rowspan="2">06h</td></tr>
<tr><td colspan="2">RSVD</td><td>OUT12_OCP</td><td>OUT11_OCP</td><td>OUT10_OCP</td><td>OUT9_OCP</td><td>OUT8_OCP</td><td>OUT7_OCP</td></tr>
<tr><td rowspan="2">HS_ITRIP_STAT</td><td colspan="8">RSVD</td><td rowspan="2">R</td><td rowspan="2">07h</td></tr>
<tr><td>RSVD</td><td>ECFB_LS_ITRIP_STAT</td><td>RSVD</td><td>OUT12_ITRIP_STAT</td><td>OUT11_ITRIP_STAT</td><td>OUT10_ITRIP_STAT</td><td>OUT9_ITRIP_STAT</td><td>OUT8_ITRIP_STAT</td></tr>
<tr><td rowspan="2">SPARE_STAT2</td><td colspan="8">RSVD</td><td rowspan="2">R</td><td rowspan="2">08h</td></tr>
<tr><td colspan="8">DEV_ID</td></tr>
<tr><td rowspan="2">IC_CNFG1</td><td>OTSD_MODE</td><td>DIS_CP</td><td>RSVD</td><td>PVDD_OV_MODE</td><td colspan="2">PVDD_OV_DG</td><td>PVDD_OV_LVL</td><td>VCP_UV_LVL</td><td rowspan="2">R/W</td><td rowspan="2">09h</td></tr>
<tr><td colspan="2">CP_MODE</td><td>VCP_UV_MODE</td><td>PVDD_UV_MODE</td><td>WD_EN</td><td>WD_FLT_M</td><td>WD_WIN</td><td>EN_SSC</td></tr>
<tr><td rowspan="2">IC_CNFG2</td><td colspan="8">RSVD</td><td rowspan="2">R/W</td><td rowspan="2">0Ah</td></tr>
<tr><td>ZONE4_OTW_H_DIS</td><td>ZONE3_OTW_H_DIS</td><td>ZONE2_OTW_H_DIS</td><td>ZONE1_OTW_H_DIS</td><td>ZONE4_OTW_L_DIS</td><td>ZONE3_OTW_L_DIS</td><td>ZONE2_OTW_L_DIS</td><td>ZONE1_OTW_L_DIS</td></tr>
<tr><td rowspan="2">GD_CNFG</td><td colspan="2">RSVD</td><td>IDRV_LO1</td><td>IDRV_LO2</td><td>PU_SH_1</td><td>PD_SH_1</td><td>PU_SH_2</td><td>PD_SH_2</td><td rowspan="2">R/W</td><td rowspan="2">0Bh</td></tr>
<tr><td>RSVD</td><td>IN2_MODE</td><td>IN1_MODE</td><td>BRG_FW</td><td colspan="2">BRG_MODE</td><td>EN_OLSC</td><td>EN_GD</td></tr>
<tr><td rowspan="2">GD_IDRV_CNFG</td><td colspan="4">IDRVP_1</td><td colspan="4">IDRVN_1</td><td rowspan="2">R/W</td><td rowspan="2">0Ch</td></tr>
<tr><td colspan="4">IDRVP_2</td><td colspan="4">IDRVN_2</td></tr>
<tr><td rowspan="2">GD_VGS_CNFG</td><td colspan="4">RSVD</td><td>VGS_IND</td><td colspan="2">VGS_TDEAD</td><td>RSVD</td><td rowspan="2">R/W</td><td rowspan="2">0Dh</td></tr>
<tr><td>RSVD</td><td colspan="3">VGS_TDRV</td><td>VGS_HS_DIS</td><td>VGS_LVL</td><td colspan="2">VGS_MODE</td></tr>
<tr><td rowspan="2">GD_VDS_CNFG</td><td>RSVD</td><td>VDS_IND</td><td colspan="2">VDS_IDRVN</td><td colspan="4">VDS_HS_LVL</td><td rowspan="2">R/W</td><td rowspan="2">0Eh</td></tr>
<tr><td colspan="2">VDS_MODE</td><td colspan="2">VDS_DG</td><td colspan="4">VDS_LS_LVL</td></tr>
<tr><td rowspan="2">GD_CSA_CNFG</td><td colspan="8">RSVD</td><td rowspan="2">R/W</td><td rowspan="2">0Fh</td></tr>
<tr><td colspan="3">CSA_BLK</td><td>CSA_BLK_SEL</td><td colspan="2">CSA_GAIN</td><td>CSA_DIV</td><td>CSA_EN</td></tr>
<tr><td rowspan="2">GD_AGD_CNFG</td><td>RVSD</td><td>PDR_ERR</td><td colspan="2">AGD_ISTRONG</td><td colspan="2">AGD_THR</td><td>SET_AGD</td><td>FW_MAX</td><td rowspan="2">R/W</td><td rowspan="2">10h</td></tr>
<tr><td>EN_DCC</td><td>IDIR_MAN</td><td colspan="2">KP_PST</td><td>EN_PST_DLY</td><td colspan="2">KP_PDR</td><td>EN_PDR</td></tr>
<tr><td rowspan="2">GD_PDR_CNFG</td><td colspan="2">PRE_MAX</td><td colspan="6">T_DON_DOFF</td><td rowspan="2">R/W</td><td rowspan="2">11h</td></tr>
<tr><td colspan="2">T_PRE_CHR</td><td colspan="2">T_PRE_DCHR</td><td colspan="2">PRE_CHR_INIT</td><td colspan="2">PRE_DCHR_INIT</td></tr>
</table>

Table 8-2. DRV8000-Q1 Register Map (continued)

Name	15	14	13	12	11	10	9	8	Type	Addr
	7	6	5	4	3	2	1	0		
GD_STC_CNFG	RSVD							IDIR_MAN_SEL	R/W	12h
	T_RISE_FALL				STC_ERR	KP_STC		EN_STC		
GD_SPARE_CNFG1	RSVD								R/W	13h
HB_ITRIP_DG	RSVD				OUT6_ITRIP_DG		OUT5_ITRIP_DG		R/W	14h
	OUT4_ITRIP_DG		OUT3_ITRIP_DG		OUT2_ITRIP_DG		OUT1_ITRIP_DG			
HB_OUT_CNFG1	RSVD	NSR_OUT6_DIS	NSR_OUT5_DIS	NSR_OUT4_DIS	NSR_OUT3_DIS	NSR_OUT2_DIS	NSR_OUT1_DIS	IPROPI_SH_EN	R/W	15h
	RSVD		OUT6_CNFG			OUT5_CNFG				
HB_OUT_CNFG2	RSVD		OUT4_CNFG			OUT3_CNFG			R/W	16h
	OUT2_MODE	OUT1_MODE	OUT2_CNFG			OUT1_CNFG				
HB_OCP_CNFG	RSVD				OUT6_OCP_DG		OUT5_OCP_DG		R/W	17h
	OUT4_OCP_DG		OUT3_OCP_DG		OUT2_OCP_DG		OUT1_OCP_DG			
HB_OL_CNFG1	RSVD		HB_OLP_CNFG		HB_OLP_SEL				R/W	18h
	RSVD		OUT6_OLA_EN	OUT5_OLA_EN	OUT4_OLA_EN	OUT3_OLA_EN	OUT2_OLA_EN	OUT1_OLA_EN		
HB_OL_CNFG2	RSVD				OUT6_OLA_TH		OUT5_OLA_TH		R/W	19h
	OUT4_OLA_TH		OUT3_OLA_TH		OUT2_OLA_TH		OUT1_OLA_TH			
HB_SR_CNFG	RSVD				OUT6_SR		OUT5_SR		R/W	1Ah
	OUT4_SR		OUT3_SR		OUT2_SR		OUT1_SR			
HB_ITRIP_CNFG	OUT6_ITRIP_EN	OUT5_ITRIP_EN	OUT4_ITRIP_EN	OUT3_ITRIP_EN	OUT2_ITRIP_EN	OUT1_ITRIP_EN	OUT6_ITRIP_LVL		R/W	1Bh
	OUT5_ITRIP_LVL		OUT4_ITRIP_LVL		OUT3_ITRIP_LVL		OUT2_ITRIP_LVL	OUT1_ITRIP_LVL		
HB_ITRIP_FREQ	RSVD		HB_TOFF_SEL		OUT6_ITRIP_FREQ		OUT5_ITRIP_FREQ		R/W	1Ch
	OUT4_ITRIP_FREQ		OUT3_ITRIP_FREQ		OUT2_ITRIP_PWM_FREQ/ PWM_OUT2_FREQ		OUT1_ITRIP_PWM_FREQ/ PWM_OUT1_FREQ			
HS_HEAT_OUT_CNFG	HEAT_CNFG		RSVD		OUT12_CNFG		OUT11_CNFG		R/W	1Dh
	OUT10_CNFG		OUT9_CNFG		OUT8_CNFG		OUT7_CNFG			
HS_OC_CNFG	RSVD			OUT11_EC_MODE	RSVD				R/W	1Eh
	RSVD		OUT12_OC_TH	OUT11_OC_TH	OUT10_OC_TH	OUT9_OC_TH	OUT8_OC_TH	OUT7_RDSON_MODE		
HS_OL_CNFG	RSVD		OUT12_OLA_TH	OUT11_OLA_TH	OUT10_OLA_TH	OUT9_OLA_TH	OUT8_OLA_TH	RSVD	R/W	1Fh
	RSVD		OUT12_OLA_EN	OUT11_OLA_EN	OUT10_OLA_EN	OUT9_OLA_EN	OUT8_OLA_EN	OUT7_OLA_EN		
HS_REG_CNFG1	RSVD								R/W	20h
	OUT7_ITRIP_EN	RSVD			OUT7_ITRIP_FREQ		OUT7_ITRIP_DG			
HS_REG_CNFG2	RSVD		OUT12_CCM_TO	OUT11_CCM_TO	OUT10_CCM_TO	OUT9_CCM_TO	OUT8_CCM_TO	OUT7_CCM_TO	R/W	21h
	RSVD		OUT12_CCM_EN	OUT11_CCM_EN	OUT10_CCM_EN	OUT9_CCM_EN	OUT8_CCM_EN	OUT7_CCM_EN		
HS_PWM_FREQ_CNFG	RSVD				PWM_OUT12_FREQ		PWM_OUT11_FREQ		R/W	22h
	PWM_OUT10_FREQ		PWM_OUT9_FREQ		PWM_OUT8_FREQ		PWM_OUT7_FREQ			
HEAT_CNFG	RSVD				HEAT_VDS_LVL				R/W	23h
	HEAT_VDS_MODE		HEAT_VDS_BLK		HEAT_VDS_DG		HEAT_OLP_EN	RSVD		
EC_CNFG	ECFB_DIAG		EC_OUT11_OCP_DG		ECFB_SC_RSEL		ECFB_OV_DG		R/W	24h
	RSVD		ECFB_OV_MODE		EC_FLT_MODE	ECFB_LS_PWM	EC_OLEN	ECFB_MAX		
HS_REG_CNFG3	RSVD				HS_OUT_ITRIP_FREQ		HS_OUT_ITRIP_DG		R/W	25h
	RSVD			HS_OUT12_ITRIP_EN	HS_OUT11_ITRIP_EN	HS_OUT10_ITRIP_EN	HS_OUT9_ITRIP_EN	HS_OUT8_ITRIP_EN		
SPARE_CNFG2	RSVD								R/W	26h
OUT1_HS_MODE_DC	RSVD						OUT1_DC		R/W	27h
	OUT1_DC									
OUT2_HS_MODE_DC	RSVD						OUT2_DC		R/W	28h
	OUT2_DC									
IC_CTRL	RSVD		IPROPI_MODE	IPROPI_SEL					R/W	29h
	CTRL_LOCK			CNFG_LOCK			WD_RST	CLR_FLT		

Table 8-2. DRV8000-Q1 Register Map (continued)

Name	15 / 7	14 / 6	13 / 5	12 / 4	11 / 3	10 / 2	9 / 1	8 / 0	Type	Addr
GD_HB_CTRL	S_HIZ2	S_HIZ1	S_IN2	S_IN1	OUT6_CTRL		OUT5_CTRL		R/W	2Ah
	OUT4_CTRL		OUT3_CTRL		OUT2_CTRL		OUT1_CTRL			
HS_EC_HEAT_CTRL	ECFB_LS_EN	EC_ON	EC_V_TAR						R/W	2Bh
	HEAT_EN	RSVD	OUT12_EN	OUT11_EN	OUT10_EN	OUT9_EN	OUT8_EN	OUT7_EN		
OUT7_PWM_DC	RSVD						OUT7_DC		R/W	2Ch
	OUT7_DC									
OUT8_PWM_DC	RSVD						OUT8_DC		R/W	2Dh
	OUT8_DC									
OUT9_PWM_DC	RSVD						OUT9_DC		R/W	2Eh
	OUT9_DC									
OUT10_PWM_DC	RSVD						OUT10_DC		R/W	2Fh
	OUT10_DC									
OUT11_PWM_DC	RSVD						OUT11_DC		R/W	30h
	OUT11_DC									
OUT12_PWM_DC	RSVD						OUT12_DC		R/W	31h
	OUT12_DC									

8.1 DRV8000-Q1_STATUS Registers

Table 8-3 lists the memory-mapped registers for the DRV8000-Q1_STATUS registers. All register offset addresses not listed in Table 8-3 should be considered as reserved locations and the register contents should not be modified.

Table 8-3. DRV8000-Q1_STATUS Registers

Offset	Acronym	Register Name	Section
0h	IC_STAT1	Device status summary 1.	Section 8.1.1
1h	IC_STAT2	Device status summary 2.	Section 8.1.2
2h	GD_STAT	Gate driver status.	Section 8.1.3
3h	HB_STAT1	Half-bridge overcurrent status.	Section 8.1.4
4h	HB_STAT2	Half-bridge open-load status.	Section 8.1.5
5h	EC_HEAT_ITRIP_STAT	Electrochrome, Heater, and ITRIP status.	Section 8.1.6
6h	HS_STAT	High-side driver status.	Section 8.1.7
7h	HS_ITRIP_STAT	Electrochrome and High-side ITRIP status	Section 8.1.8
8h	SPARE_STAT2	Spare status 2.	Section 8.1.9

Complex bit access types are encoded to fit into small table cells. Table 8-4 shows the codes that are used for access types in this section.

Table 8-4. DRV8000-Q1_STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 IC_STAT1 Register (Offset = 0h) [Reset = C000h]

IC_STAT1 is shown in Table 8-5.

Return to the Summary Table.

Main device status register for driver, supply and over temperature fault status. Also includes watchdog and ITRIP regulation fault status.

Table 8-5. IC_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_OK	R	1h	Indicates if a SPI communications fault has been detected. 0b = One or multiple of SCLK_FLT in the prior frames. 1b = No SPI fault has been detected.
14	POR	R	1h	Indicates power-on-reset condition. 0b = No power-on-reset condition detected. 1b = Power-on reset condition detected.
13	FAULT	R	0h	General Fault indicator. Indicates a device or driver fault has occurred. 0b = No fault. 1b = Fault detected.
12	WARN	R	0h	General warning indicator. Indicates a warning is present. 0b = No warning. 1b = Warning is present.
11	GD	R	0h	Logic OR of VDS and VGS fault indicators for gate driver.
10	HB	R	0h	Logic OR of overcurrent and open load fault indicators for half-bridges.
9	EC_HEAT	R	0h	Logic OR of EC OV, overcurrent, open load fault indicators for EC and heater.
8	HS	R	0h	Logic OR of overcurrent, short-circuit and open load fault indicators for integrated high-side drivers.
7	PVDD_UV	R	0h	Indicates undervoltage fault on PVDD pin.
6	PVDD_OV_22V	R	0h	Indicates overvoltage fault on PVDD pin greater than 22 V.
5	VCP_UV	R	0h	Indicates undervoltage fault on VCP pin.
4	OTW	R	0h	Indicates overtemperature warning.
3	OTSD	R	0h	Indicates overtemperature shutdown
2	WD_FLT	R	0h	Indicates watchdog timer fault.
1	ITRIP	R	0h	Indicates ITRIP regulation warning when any OUTx entered ITRIP.
0	PVDD_OV_28V	R	0h	Indicates overvoltage fault on PVDD pin greater than 28 V.

8.1.2 IC_STAT2 Register (Offset = 1h) [Reset = 0000h]

IC_STAT2 is shown in Table 8-6.

Return to the Summary Table.

Second device status register with SPI faults and specific thermal cluster fault/warning status.

Table 8-6. IC_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DEVICE_ERR	R	0h	Indicates device OTP memory error has occurred.
14	RESERVED	R	0h	Reserved
13	SCLK_FLT	R	0h	Indicates SPI clock (frame) fault when the number of SCLK pulses in a transaction frame are not equal to 24 bits, 1 byte address and two bytes data. Reported on bit SPI_ERR.
12	RESERVED	R	0h	Reserved
11	ZONE4_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 4.
10	ZONE3_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 3.
9	ZONE2_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 2.
8	ZONE1_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 1.
7	ZONE4_OTW_H	R	0h	Indicates high temperature warning (above 145°C) has occurred in zone 4.
6	ZONE3_OTW_H	R	0h	Indicates high temperature warning (above 145°C) has occurred in zone 3.
5	ZONE2_OTW_H	R	0h	Indicates high temperature warning (above 145°C) has occurred in zone 2.
4	ZONE1_OTW_H	R	0h	Indicates high temperature warning (above 145°C) has occurred in zone 1.
3	ZONE4_OTW_L	R	0h	Indicates low temperature warning (above 125°C) has occurred in zone 4.
2	ZONE3_OTW_L	R	0h	Indicates low temperature warning (above 125°C) has occurred in zone 3.
1	ZONE2_OTW_L	R	0h	Indicates low temperature warning (above 125°C) has occurred in zone 2.
0	ZONE1_OTW_L	R	0h	Indicates low temperature warning (above 125°C) has occurred in zone 1.

8.1.3 GD_STAT Register (Offset = 2h) [Reset = 0000h]

GD_STAT is shown in Table 8-7.

Return to the Summary Table.

Gate driver status register with all gate driver faults and warnings, including smart gate driver faults and warnings.

Table 8-7. GD_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DRVOFF_STAT_FB	R	0h	DRVOFF analog latched status for gate driver. User can clear status bit after releasing DRVOFF pin and issuing CLR_FLT command.
14	DRVOFF_STAT	R	0h	Indicates the latched status (high or low) of DRVOFF pin. If DRVOFF pin is asserted, DRVOFF_STAT = 1b. If DRVOFF pin is de-asserted, DRVOFF_STAT = 0b.
13	STC_WARN_R	R	0h	Indicates rising slew time TDRV overflow for gate driver half-bridge 1 and 2.
12	STC_WARN_F	R	0h	Indicates falling slew time TDRV overflow for gate driver half-bridge 1 and 2.
11	PCHR_WARN	R	0h	Indicates pre-charge underflow or overflow fault for gate driver half-bridge 1 and 2.
10	PDCHR_WARN	R	0h	Indicates pre-discharge underflow or overflow fault for gate driver half-bridge 1 and 2.
9	IDIR	R	0h	Indicates current direction for gate driver half-bridge 1 and 2.
8	IDIR_WARN	R	0h	Indicates unknown current direction for gate driver half-bridge 1 and 2
7	VGS_L2	R	0h	Indicates VGS gate fault on the low-side 2 MOSFET.
6	VGS_H2	R	0h	Indicates VGS gate fault on the high-side 2 MOSFET.
5	VGS_L1	R	0h	Indicates VGS gate fault on the low-side 1 MOSFET.
4	VGS_H1	R	0h	Indicates VGS gate fault on the high-side 1 MOSFET.
3	VDS_L2	R	0h	Indicates VDS overcurrent fault on the low-side 2 MOSFET.
2	VDS_H2	R	0h	Indicates VDS overcurrent fault on the high-side 2 MOSFET.
1	VDS_L1	R	0h	Indicates VDS overcurrent fault on the low-side 1 MOSFET.
0	VDS_H1	R	0h	Indicates VDS overcurrent fault on the high-side 1 MOSFET.

8.1.4 HB_STAT1 Register (Offset = 3h) [Reset = 0000h]

HB_STAT1 is shown in Table 8-8.

Return to the Summary Table.

Half-bridge overcurrent faults for either high- or low-side of each half-bridge.

Table 8-8. HB_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	OUT6_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT6.
12	OUT5_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT5.
11	OUT4_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT4.
10	OUT3_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT3.
9	OUT2_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT2.
8	OUT1_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT1.
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT6_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT6.
4	OUT5_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT5.
3	OUT4_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT4.
2	OUT3_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT3.
1	OUT2_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT2.
0	OUT1_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT1.

8.1.5 HB_STAT2 Register (Offset = 4h) [Reset = 0000h]

HB_STAT2 is shown in Table 8-9.

Return to the Summary Table.

Half-bridge active and off-state open load faults.

Table 8-9. HB_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	HB_OLP_STAT	R	0h	Indicates integrated half-bridge OLP status.
11	OUT6_LS_OLA	R	0h	Indicates active open load fault on low-side of half-bridge OUT6.
10	OUT5_LS_OLA	R	0h	Indicates active open load fault on low-side of half-bridge OUT5.
9	OUT4_LS_OLA	R	0h	Indicates active open load fault on low-side of half-bridge OUT4.
8	OUT3_LS_OLA	R	0h	Indicates active open load fault on low-side of half-bridge OUT3.
7	OUT2_LS_OLA	R	0h	Indicates active open load fault on low-side of half-bridge OUT2.
6	OUT1_LS_OLA	R	0h	Indicates active open load fault on low-side of half-bridge OUT1.
5	OUT6_HS_OLA	R	0h	Indicates active open load fault on high-side of half-bridge OUT6.
4	OUT5_HS_OLA	R	0h	Indicates active open load fault on high-side of half-bridge OUT5.
3	OUT4_HS_OLA	R	0h	Indicates active open load fault on high-side of half-bridge OUT4.
2	OUT3_HS_OLA	R	0h	Indicates active open load fault on high-side of half-bridge OUT3.
1	OUT2_HS_OLA	R	0h	Indicates active open load fault on high-side of half-bridge OUT2.
0	OUT1_HS_OLA	R	0h	Indicates active open load fault on high-side of half-bridge OUT1.

8.1.6 EC_HEAT_ITRIP_STAT Register (Offset = 5h) [Reset = 0000h]

EC_HEAT_ITRIP_STAT is shown in Table 8-10.

Return to the Summary Table.

Includes all electrochrome and heater driver faults and warnings. Also includes ITRIP regulation status warnings.

Table 8-10. EC_HEAT_ITRIP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECFB_DIAG_STAT	R	0h	Indicates ECFB_SC fault is present when ECFB_DIAG=0x01. Indicates ECFB OLP fault when ECFB_DIAG=10b.
14	ECFB_OV	R	0h	Indicates overvoltage (short to battery) fault on ECFB pin.
13	ECFB_HI	R	0h	Indicates regulation overvoltage fault on ECFB pin.
12	ECFB_LO	R	0h	Indicates regulation undervoltage fault on ECFB pin.
11	ECFB_OC	R	0h	Indicates overcurrent fault on ECFB pin.
10	ECFB_OL	R	0h	Indicates open load fault on ECFB pin.
9	HEAT_OL	R	0h	Indicates open load fault on SH_HS pin.
8	HEAT_VDS	R	0h	Indicates overcurrent fault on heater MOSFET.
7	RESERVED	R	0h	Reserved
6	OUT7_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT7.
5	OUT6_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT6.
4	OUT5_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT5.
3	OUT4_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT4.
2	OUT3_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT3.
1	OUT2_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT2.
0	OUT1_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT1.

8.1.7 HS_STAT Register (Offset = 6h) [Reset = 0000h]

HS_STAT is shown in Table 8-11.

Return to the Summary Table.

High-side driver overcurrent and open load fault status.

Table 8-11. HS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	OUT12_OLA	R	0h	Indicates open load fault on OUT12.
12	OUT11_OLA	R	0h	Indicates open load fault on OUT11.
11	OUT10_OLA	R	0h	Indicates open load fault on OUT10.
10	OUT9_OLA	R	0h	Indicates open load fault on OUT9.
9	OUT8_OLA	R	0h	Indicates open load fault on OUT8.
8	OUT7_OLA	R	0h	Indicates open load fault on OUT7.
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT12_OCP	R	0h	Indicates overcurrent fault on OUT12.
4	OUT11_OCP	R	0h	Indicates overcurrent fault on OUT11.
3	OUT10_OCP	R	0h	Indicates overcurrent fault on OUT10.
2	OUT9_OCP	R	0h	Indicates overcurrent fault on OUT9.
1	OUT8_OCP	R	0h	Indicates overcurrent fault on OUT8.
0	OUT7_OCP	R	0h	Indicates overcurrent fault on OUT7.

8.1.8 HS_ITRIP_STAT Register (Offset = 7h) [Reset = 0000h]

HS_ITRIP_STAT is shown in Table 8-12.

Return to the Summary Table.

Includes electrochrome and High-side ITRIP status register.

Table 8-12. HS_ITRIP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	ECFB_LS_ITRIP_STAT	R	0h	Indicates if ECFB_LS_ITRIP has occurred. Cleared only with CLR_FLT.
5	RESERVED	R	0h	Reserved
4	OUT12_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT12.
3	OUT11_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT11.
2	OUT10_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT10.
1	OUT9_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT9.
0	OUT8_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT8.

8.1.9 SPARE_STAT2 Register (Offset = 8h) [Reset = 0000h]

SPARE_STAT2 is shown in Table 8-13.

Return to the Summary Table.

Spare status register.

Table 8-13. SPARE_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-0	DEV_ID	R	0h	0x02= DRV8000 0x21= DRV8001 0x22= DRV8002

8.2 DRV8000-Q1_CNFG Registers

Table 8-14 lists the memory-mapped registers for the DRV8000-Q1_CNFG registers. All register offset addresses not listed in Table 8-14 should be considered as reserved locations and the register contents should not be modified.

Table 8-14. DRV8000-Q1_CNFG Registers

Offset	Acronym	Register Name	Section
9h	IC_CNFG1	IC configuration register 1.	Section 8.2.1
Ah	IC_CNFG2	IC configuration register 2.	Section 8.2.2
Bh	GD_CNFG	Gate driver configuration register.	Section 8.2.3
Ch	GD_IDRV_CNFG	IDRIVE setting configuration register.	Section 8.2.4
Dh	GD_VGS_CNFG	VGS detection configuration register.	Section 8.2.5
Eh	GD_VDS_CNFG	VDS monitoring configuration register.	Section 8.2.6
Fh	GD_CSA_CNFG	CSA configuration register.	Section 8.2.7
10h	GD_AGD_CNFG	Advanced smart gate driver configuration register.	Section 8.2.8
11h	GD_PDR_CNFG	Propagation Delay Reduction configuration register.	Section 8.2.9
12h	GD_STC_CNFG	Slew time control configuration register.	Section 8.2.10
13h	GD_SPARE_CNFG1	Spare gate driver configuration register 1.	Section 8.2.11
14h	HB_ITRIP_DG	Half-bridge ITRIP deglitch configuration register 2.	Section 8.2.12
15h	HB_OUT_CNFG1	Half-bridge output 5 and 6 configuration register.	Section 8.2.13
16h	HB_OUT_CNFG2	Half-bridge output 1-4 configuration register.	Section 8.2.14
17h	HB_OCP_CNFG	Half-bridge overcurrent deglitch configuration register.	Section 8.2.15
18h	HB_OL_CNFG1	Half-bridge active and passive open-load enable register	Section 8.2.16
19h	HB_OL_CNFG2	Half-bridge active open-load threshold select register.	Section 8.2.17
1Ah	HB_SR_CNFG	Half-bridge slew rate configuration register.	Section 8.2.18
1Bh	HB_ITRIP_CNFG	Half-bridge ITRIP configuration register 1.	Section 8.2.19
1Ch	HB_ITRIP_FREQ	Half-bridge ITRIP frequency configuration register 2.	Section 8.2.20
1Dh	HS_HEAT_OUT_CNFG	High-side and heater driver output configuration register.	Section 8.2.21
1Eh	HS_OC_CNFG	High-side driver overcurrent threshold configuration register.	Section 8.2.22
1Fh	HS_OL_CNFG	High-side driver open load threshold configuration register.	Section 8.2.23
20h	HS_REG_CNFG1	High-side driver regulation configuration register.	Section 8.2.24
21h	HS_REG_CNFG2	High-side driver regulation configuration register.	Section 8.2.25
22h	HS_PWM_FREQ_CNFG	High-side driver PWM generator frequency configuration register.	Section 8.2.26
23h	HEAT_CNFG	Heater configuration register.	Section 8.2.27
24h	EC_CNFG	Electrochrome configuration register.	Section 8.2.28
25h	HS_REG_CNFG3	High-side driver regulation configuration register.	Section 8.2.29
26h	SPARE_CNFG2	Spare configuration	Section 8.2.30
27h	OUT1_HS_MODE_DC	Duty cycle configuration for OUT1.	Section 8.2.31
28h	OUT2_HS_MODE_DC	Duty cycle configuration for OUT2.	Section 8.2.32

Complex bit access types are encoded to fit into small table cells. Table 8-15 shows the codes that are used for access types in this section.

Table 8-15. DRV8000-Q1_CNFG Access Type Codes

Access Type	Code	Description
Read Type		

Table 8-15. DRV8000-Q1_CNFG Access Type Codes (continued)

Access Type	Code	Description
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 IC_CNFG1 Register (Offset = 9h) [Reset = 0002h]

IC_CNFG1 is shown in Table 8-16.

Return to the Summary Table.

Includes configurations charge pump and watchdog, and fault levels and reactions for supply, charge pump, thermal, and watch dog faults.

Table 8-16. IC_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OTSD_MODE	R/W	0h	Sets overtemperature shutdown behavior. If any thermal cluster reaches OT, the device shuts down all drivers or affected drivers only (drivers in zone 3, for example). 0b = Global shutdown. 1b = Affected driver shutdown only.
14	DIS_CP	R/W	0h	When all output are off (OUTx_EN, EN_GD, HEAT_EN, EC_ON), the charge pump can be disabled, putting the device in a communication only mode. 0b = Charge pump enabled. 1b = Charge pump disabled.
13	RSVD	R	0h	Reserved.
12	PVDD_OV_MODE	R/W	0h	PVDD supply overvoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
11-10	PVDD_OV_DG	R/W	0h	PVDD supply overvoltage monitor deglitch time. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
9	PVDD_OV_LVL	R/W	0h	PVDD supply overvoltage monitor threshold. 0b = 22 V 1b = 28 V
8	VCP_UV_LVL	R/W	0h	VCP charge pump undervoltage monitor threshold. 0b = 4.75 V 1b = 6.25 V
7-6	CP_MODE	R/W	0h	Charge pump operating mode. 00b = Automatic switch between tripler and doubler mode. 01b = Always doubler mode. 10b = Always tripler mode. 11b = RSVD
5	VCP_UV_MODE	R/W	0h	VCP charge pump undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
4	PVDD_UV_MODE	R/W	0h	PVDD supply undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
3	WD_EN	R/W	0h	Watchdog timer enable. 0b = Watchdog timer disabled. 1b = Watchdog timer enabled.
2	WD_FLT_M	R/W	0h	Watchdog fault mode. Watchdog fault is cleared by CLR_FLT. 0b = Watchdog fault is reported to WD_FLT and WARN register bits. Drivers remain enabled and FAULT bit is not asserted. 1b = Watchdog fault is reported to WD_FLT and FAULT register bits. All drivers are disabled in response to watchdog fault.
1	WD_WIN	R/W	1h	Watchdog timer window. 0b = 4 to 12 ms 1b = 10 to 100 ms
0	EN_SSC	R/W	0h	Spread spectrum clocking. 0b = Disabled. 1b = Enabled.

8.2.2 IC_CNFG2 Register (Offset = Ah) [Reset = 0000h]

IC_CNFG2 is shown in Table 8-17.

Return to the Summary Table.

Includes thermal cluster warning disable bits.

Table 8-17. IC_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	ZONE4_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 4. Enabled = 0b Disabled = 1b
6	ZONE3_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 3. Enabled = 0b Disabled = 1b
5	ZONE2_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 2. Enabled = 0b Disabled = 1b
4	ZONE1_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 1. Enabled = 0b Disabled = 1b
3	ZONE4_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 4. Enabled = 0b Disabled = 1b
2	ZONE3_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 3. Enabled = 0b Disabled = 1b
1	ZONE2_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 2. Enabled = 0b Disabled = 1b
0	ZONE1_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 1. Enabled = 0b Disabled = 1b

8.2.3 GD_CNFG Register (Offset = Bh) [Reset = 0000h]

GD_CNFG is shown in Table 8-18.

Return to the Summary Table.

General gate driver controls. Includes gate driver enable, bridge configuration, input pin modes, and open load enable.

Table 8-18. GD_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	IDRV_LO1	R/W	0h	Enable low current IDRVN and IDRVP mode for half-bridge 1. 0b = IDRVP_1 and IDRVN_1 utilize standard values. 1b = IDRVP_1 and IDRVN_1 utilize low current values.
12	IDRV_LO2	R/W	0h	Enable low current IDRVN and IDRVP mode for half-bridge 2. 0b = IDRVP_2 and IDRVN_2 utilize standard values. 1b = IDRVP_2 and IDRVN_2 utilize low current values.
11	PU_SH_1	R/W	0h	Gate driver 1 pullup diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
10	PD_SH_1	R/W	0h	Gate driver 1 pulldown diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
9	PU_SH_2	R/W	0h	Gate driver 2 pullup diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
8	PD_SH_2	R/W	0h	Gate driver 2 pulldown diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
7	RESERVED	R/W	0h	Reserved
6	IN2_MODE	R/W	0h	Sets gate driver 2 control source. 0b = Input pin IN2. 1b = SPI control.
5	IN1_MODE	R/W	0h	Sets gate driver 1 control source. 0b = Input pin IN1. 1b = SPI control.
4	BRG_FW	R/W	0h	Gate driver 1 and 2 control freewheeling setting. Settings shared between half-bridges 1 and 2. 0b = Low-side freewheeling 1b = High-side freewheeling.
3-2	BRG_MODE	R/W	0h	Gate driver 1 and 2 input control mode. 00b = Independent half-bridge input control. 01b = PH/EN H-bridge input control. 10b = PWM H-bridge input control. 11b = Reserved.
1	EN_OLSC	R/W	0h	Offline open-load and short-circuit diagnostic enable. 0b = Disabled. 1b = VDS monitors set into real-time voltage monitor mode and diagnostics current sources enabled.
0	EN_GD	R/W	0h	Enable gate driver bit. 0b = Driver inputs are ignored and the gate driver passive pulldowns are enabled. 1b = Gate driver outputs are enabled and controlled by the digital inputs.

8.2.4 GD_IDRV_CNFG Register (Offset = Ch) [Reset = 4444h]

GD_IDRV_CNFG is shown in Table 8-19.

Return to the Summary Table.

Includes IDRIVE drive current levels for each half-bridge gate driver.

Table 8-19. GD_IDRV_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	IDRVP_1	R/W	4h	Gate driver 1 peak source pullup current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5 mA (50 μA) 0001b = 1 mA (110 μA) 0010b = 2 mA (170 μA) 0011b = 3 mA (230 μA) 0100b = 4 mA (290 μA) 0101b = 5 mA (350 μA) 0110b = 6 mA (410 μA) 0111b = 7 mA (600 μA) 1000b = 8 mA (725 μA) 1001b = 12 mA (850 μA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)
11-8	IDRVN_1	R/W	4h	Gate driver 1 peak sink pulldown current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5 mA (50 μA) 0001b = 1 mA (110 μA 0010b = 2 mA (170 μA 0011b = 3 mA (230 μA) 0100b = 4 mA (290 μA) 0101b = 5 mA (350 μA) 0110b = 6 mA (410 μA) 0111b = 7 mA (600 μA) 1000b = 8 mA (725 μA) 1001b = 12 mA (850 μA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)
7-4	IDRVP_2	R/W	4h	Gate driver 2 peak source pullup current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5 mA (50 μA) 0001b = 1 mA (110 μA) 0010b = 2 mA (170 μA) 0011b = 3 mA (230 μA) 0100b = 4 mA (290 μA) 0101b = 5 mA (350 μA) 0110b = 6 mA (410 μA) 0111b = 7 mA (600 μA) 1000b = 8 mA (725 μA) 1001b = 12 mA (850 μA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

Table 8-19. GD_IDRV_CNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_2	R/W	4h	Gate driver 2 peak sink pulldown current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.2.5 GD_VGS_CNFG Register (Offset = Dh) [Reset = 0030h]

GD_VGS_CNFG is shown in Table 8-20.

Return to the Summary Table.

VGS fault detection configurations.

Table 8-20. GD_VGS_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	VGS_IND	R/W	0h	VGS independent shutdown mode enable. Active for BRG_MODE = 00b. 0b = Disabled. 1b = Enabled. VGS gate fault only shuts down the associated half-bridge.
10-9	VGS_TDEAD	R/W	0h	Insertable digital dead-time. 00b = 0 ns 01b = 2 μs 10b = 4 μs 11b = 8 μs
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6-4	VGS_TDRV	R/W	3h	VGS drive time and VDS monitor blanking time. 000b = 2 μs 001b = 4 μs 010b = 8 μs 011b = 12 μs 100b = 16 μs 101b = 24 μs 110b = 32 μs 111b = 96 μs
3	VGS_HS_DIS	R/W	0h	VGS monitor based dead-time handshake. 0b = Enabled. 1b = Disabled. Gate drive transition based on tDRIVE and tDEAD time duration
2	VGS_LVL	R/W	0h	VGS monitor threshold for dead-time handshake and gate fault detection. 0b = 1.4 V 1b = 1.0 V
1-0	VGS_MODE	R/W	0h	VGS gate fault monitor mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.

8.2.6 GD_VDS_CNFG Register (Offset = Eh) [Reset = 0D2Dh]

GD_VDS_CNFG is shown in Table 8-21.

Return to the Summary Table.

VDS monitoring or short-circuit detection configuration register.

Table 8-21. GD_VDS_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD	R/W	0h	Reserved.
14	VDS_IND	R/W	0h	VDS fault independent shutdown mode configuration. 0b = Disabled. VDS fault shuts down all gate drivers. 1b = Enabled. VDS gate fault only shuts down the associated gate driver.
13-12	VDS_IDRVN	R/W	0h	IDRVN gate pulldown current after VDS_OCP fault for gate driver 1 and 2. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA
11-8	VDS_HS_LVL	R/W	Dh	High-side VDS overcurrent monitor threshold. 0000b = 0.06 V 00001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V
7-6	VDS_MODE	R/W	0h	VDS overcurrent monitor mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	VDS_DG	R/W	2h	VDS overcurrent monitor deglitch time. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs

Table 8-21. GD_VDS_CNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	VDS_LS_LVL	R/W	Dh	Low-side VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

8.2.7 GD_CSA_CNFG Register (Offset = Fh) [Reset = 0004h]

GD_CSA_CNFG is shown in Table 8-22.

Return to the Summary Table.

CSA configurations and controls.

Table 8-22. GD_CSA_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-5	CSA_BLK	R/W	0h	Current shunt amplifier blanking time. % of tDRV. 000b = 0 %, Disabled 001b = 25 % 010b = 37.5 % 011b = 50 % 100b = 62.5 % 101b = 75 % 110b = 87.5 % 111b = 100 %
4	CSA_BLK_SEL	R/W	0h	Current shunt amplifier blanking trigger source. 0b = Gate driver 1 1b = Gate driver 2
3-2	CSA_GAIN	R/W	1h	Current shunt amplifier gain setting. 00b = 10 V/V 01b = 20 V/V 10b = 40 V/V 11b = 80 V/V
1	CSA_DIV	R/W	0h	Current shunt amplifier internal reference voltage divider. 0b = VDVDD / 2 1b = VDVDD/ 8
0	CSA_EN	R/W	0h	Current sense amplifier enable. 0b = Disabled 1b = Enabled

8.2.8 GD_AGD_CNFG Register (Offset = 10h) [Reset = 0402h]

GD_AGD_CNFG is shown in Table 8-23.

Return to the Summary Table.

Includes Advanced smart gate driver configurations, enables for DCC and PDR, post-charge settings.

Table 8-23. GD_AGD_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	PDR_ERR	R/W	0h	PDR loop error limit for gate driver 1 and 2. 0b = 1-bit error 1b = Actual error
13-12	AGD_ISTRONG	R/W	0h	Adaptive gate driver ISTRONG configuration. 00b = ISTRONG pulldown decoded from initial IDRVP_x register setting. 01b = 62 mA 10b = 124 mA 11b = RSVD
11-10	AGD_THR	R/W	1h	Adaptive gate driver VSH threshold configuration. 00b = 0.5V, VDRAIN - 0.5V 01b = 1V, VDRAIN - 1V 10b = 1.5V, VDRAIN - 1.5V 11b = 2V, VDRAIN - 2V
9	SET_AGD	R/W	0h	Set active half-bridge for adaptive gate drive control loops. 0b = Gate driver 1 1b = Gate driver 2
8	FW_MAX	R/W	0h	Gate drive current used for freewheeling MOSFET for gate driver 1 and 2. 0b = PRE_CHR_MAX_12 1b = 64 mA
7	EN_DCC	R/W	0h	Enable duty cycle compensation for half-bridge 1 and 2.
6	IDIR_MAN	R/W	0h	Current polarity detection mode for half-bridge 1 and 2. 0b = Automatic 1b = Manual (Set by IDIR_MAN_SEL)
5-4	KP_PST	R/W	0h	Post charge proportional control gain setting for half-bridges 1 and 2. 00b = Disabled 01b = 2 10b = 4 11b = 15
3	EN_PST_DLY	R/W	0h	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_12 - T_PRE_CHR_12.
2-1	KP_PDR	R/W	1h	PDR proportional controller gain setting for half-bridge 1 and 2. 00b = 1 01b = 2 10b = 3 11b = 4
0	EN_PDR	R/W	0h	Enable PDR loop control for half-bridge 1 and 2.

8.2.9 GD_PDR_CNFG Register (Offset = 11h) [Reset = 0AF6h]

GD_PDR_CNFG is shown in Table 8-24.

Return to the Summary Table.

Includes remaining PDR controls, pre-charge settings and timing.

Table 8-24. GD_PDR_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	PRE_MAX	R/W	0h	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 1 and 2. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
13-8	T_DON_DOFF	R/W	Ah	On and off time delay for half-bridge 1 and 2. 140 ns x T_DON_DOFF [3:0] Default time: 001010b (1.4 μs)
7-6	T_PRE_CHR	R/W	3h	PDR control loop pre-charge time for half-bridge 1 and 2. Set as ratio of T_DON_DOFF_12 [5:0]. 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR	R/W	3h	PDR control loop pre-discharge time for half-bridge 1 and 2. Set as ratio of T_DON_DOFF_12 [5:0]. 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT	R/W	1h	PDR control loop initial pre-charge current setting for half-bridge 1 and 2. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT	R/W	2h	PDR control loop initial pre-discharge current setting for half-bridge 1 and 2. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.2.10 GD_STC_CNFG Register (Offset = 12h) [Reset = 0026h]

GD_STC_CNFG is shown in Table 8-25.

Return to the Summary Table.

Includes configurations and enable for slew time control.

Table 8-25. GD_STC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	IDIR_MAN_SEL	R/W	0h	Manual freewheel selection for Gate Drivers. 0b = High-side MOSFET drive, Low-side MOSFET freewheel. 1b = Low-side MOSFET drive, High-side MOSFET freewheel.
7-4	T_RISE_FALL	R/W	2h	Set switch-node VSH rise and fall time for half-bridge 1 and 2. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us
3	STC_ERR	R/W	0h	STC loop error limit for half-bridge 1 and 2. 0b = 1-bit error 1b = Actual error
2-1	KP_STC	R/W	3h	STC proportional controller gain setting for half-bridge 1 and 2. 00b = 1 01b = 2 10b = 3 11b = 4
0	EN_STC	R/W	0h	Enable STC loop control for half-bridge 1 and 2.

8.2.11 GD_SPARE_CNFG1 Register (Offset = 13h) [Reset = 0000h]

GD_SPARE_CNFG1 is shown in Table 8-26.

Return to the Summary Table.

Spare configuration register for gate driver.

Table 8-26. GD_SPARE_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

8.2.12 HB_ITRIP_DG Register (Offset = 14h) [Reset = 0000h]

HB_ITRIP_DG is shown in Table 8-27.

Return to the Summary Table.

Configures ITRIP deglitch for each half-bridge. ITRIP timing is shared between half-bridge pairs.

Table 8-27. HB_ITRIP_DG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	OUT6_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 6. 00b = 2 µs 01b = 5 µs 10b = 10 µs 11b = 20 µs
9-8	OUT5_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 5. 00b = 2 µs 01b = 5 µs 10b = 10 µs 11b = 20 µs
7-6	OUT4_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 4. 00b = 2 µs 01b = 5 µs 10b = 10 µs 11b = 20 µs
5-4	OUT3_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 3. 00b = 2 µs 01b = 5 µs 10b = 10 µs 11b = 20 µs
3-2	OUT2_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 2. 00b = 2 µs 01b = 5 µs 10b = 10 µs 11b = 20 µs
1-0	OUT1_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 1. 00b = 2 µs 01b = 5 µs 10b = 10 µs 11b = 20 µs

8.2.13 HB_OUT_CNFG1 Register (Offset = 15h) [Reset = 0000h]

HB_OUT_CNFG1 is shown in Table 8-28.

Return to the Summary Table.

Configures the output mode for each half-bridge, sets IPROPI sample and hold circuit, and half-bridge pair freewheeling.

Table 8-28. HB_OUT_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	NSR_OUT6_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 6. Passive freewheeling = 0b Active freewheeling = 1b
13	NSR_OUT5_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 5. Passive freewheeling = 0b Active freewheeling = 1b
12	NSR_OUT4_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 4. Passive freewheeling = 0b Active freewheeling = 1b
11	NSR_OUT3_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridges 3. Passive freewheeling = 0b Active freewheeling = 1b
10	NSR_OUT2_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 2. Passive freewheeling = 0b Active freewheeling = 1b
9	NSR_OUT1_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 1. Passive freewheeling = 0b Active freewheeling = 1b
8	IPROPI_SH_EN	R/W	0h	Enables IPROPI sample and hold circuit.
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5-3	OUT6_CNFG	R/W	0h	Configuration for half-bridge 6. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 LS Control 111b = PWM2 HS Control
2-0	OUT5_CNFG	R/W	0h	Configuration for half-bridge 5. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 LS Control 111b = PWM2 HS Control

8.2.14 HB_OUT_CNFG2 Register (Offset = 16h) [Reset = 0000h]

HB_OUT_CNFG2 is shown in Table 8-29.

Return to the Summary Table.

Configures the output mode for each half-bridge.

Table 8-29. HB_OUT_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13-11	OUT4_CNFG	R/W	0h	Configuration for half-bridge 4. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 LS Control 111b = PWM2 HS Control
10-8	OUT3_CNFG	R/W	0h	Configuration for half-bridge 3. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 LS Control 111b = PWM2 HS Control
7	OUT2_MODE	R/W	0h	Bit to enable OUT2 as High Side driver with internal PWM. OUT2_CNFG used for enabling and disabling the driver PWM settings - Freq: PWM_OUT2_FREQ, DC: OUT2_DC.
6	OUT1_MODE	R/W	0h	Bit to enable OUT1 as High Side driver with internal PWM. OUT1_CNFG used for enabling and disabling the driver PWM settings - Freq: PWM_OUT1_FREQ, DC: OUT1_DC.
5-3	OUT2_CNFG	R/W	0h	Configuration for half-bridge 2. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 LS Control 111b = PWM2 HS Control
2-0	OUT1_CNFG	R/W	0h	Configuration for half-bridge 1. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 LS Control 111b = PWM2 HS Control

8.2.15 HB_OCP_CNFG Register (Offset = 17h) [Reset = 0000h]

HB_OCP_CNFG is shown in Table 8-30.

Return to the Summary Table.

Overcurrent deglitch for half-bridges configuration register.

Table 8-30. HB_OCP_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	OUT6_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 6. 00b = 6 µs 01b = 10 µs 10b = 15 µs 11b = 60 µs
9-8	OUT5_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 5. 00b = 6 µs 01b = 10 µs 10b = 15 µs 11b = 60 µs
7-6	OUT4_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 4. 00b = 6 µs 01b = 10 µs 10b = 15 µs 11b = 60 µs
5-4	OUT3_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 3. 00b = 6 µs 01b = 10 µs 10b = 15 µs 11b = 60 µs
3-2	OUT2_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 2. 00b = 6 µs 01b = 10 µs 10b = 15 µs 11b = 60 µs
1-0	OUT1_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 1. 00b = 6 µs 01b = 10 µs 10b = 15 µs 11b = 60 µs

8.2.16 HB_OL_CNFG1 Register (Offset = 18h) [Reset = 0000h]

HB_OL_CNFG1 is shown in Table 8-31.

Return to the Summary Table.

Configures active and off-state open load detection circuits for half-bridges.

Table 8-31. HB_OL_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13-12	HB_OLP_CNFG	R/W	0h	Off-state diagnostics configuration. 00b = Off-state disabled 01b = OUT X Pullup enabled, OUT Y pulldown enabled, OUT Y selected, VREF Low 10b = OUT X Pullup enabled, OUT Y pulldown enabled, OUT X selected, VREF High 11b = OUT X Pulldown enabled, OUT Y pullup enabled, OUT Y selected, VREF Low
11-8	HB_OLP_SEL	R/W	0h	Off-state open load diagnostics enable for half-bridges. 0000b = Disabled 0001b = OUT1 and OUT2 0010b = OUT1 and OUT3 0011b = OUT1 and OUT4 0100b = OUT1 and OUT5 0101b = OUT1 and OUT6 0110b = OUT2 and OUT3 0111b = OUT2 and OUT4 1000b = OUT2 and OUT5 1001b = OUT2 and OUT6 1010b = OUT3 and OUT4 1011b = OUT3 and OUT5 1100b = OUT3 and OUT6 1101b = OUT4 and OUT5 1110b = OUT4 and OUT6 1111b = OUT5 and OUT6
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	OUT6_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 6. 0b = Disabled 1b = Enabled
4	OUT5_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 5. 0b = Disabled 1b = Enabled
3	OUT4_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 4. 0b = Disabled 1b = Enabled
2	OUT3_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 3. 0b = Disabled 1b = Enabled
1	OUT2_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 2. 0b = Disabled 1b = Enabled
0	OUT1_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 1. 0b = Disabled 1b = Enabled

8.2.17 HB_OL_CNFG2 Register (Offset = 19h) [Reset = 0000h]

HB_OL_CNFG2 is shown in Table 8-32.

Return to the Summary Table.

Configures cycle count threshold for active open load detection circuits of half-bridges.

Table 8-32. HB_OL_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	OUT6_OLA_TH	R/W	0h	Sets the half-bridge 6 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles 10b - 512 cycles 11b - 1024 cycles
9-8	OUT5_OLA_TH	R/W	0h	Sets the half-bridge 5 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles 10b - 512 cycles 11b - 1024 cycles
7-6	OUT4_OLA_TH	R/W	0h	Sets the half-bridge 4 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles 10b - 512 cycles 11b - 1024 cycles
5-4	OUT3_OLA_TH	R/W	0h	Sets the half-bridge 3 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles 10b - 512 cycles 11b - 1024 cycles
3-2	OUT2_OLA_TH	R/W	0h	Sets the half-bridge 2 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles 10b - 512 cycles 11b - 1024 cycles
1-0	OUT1_OLA_TH	R/W	0h	Sets the half-bridge 1 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles 10b - 512 cycles 11b - 1024 cycles

8.2.18 HB_SR_CNFG Register (Offset = 1Ah) [Reset = 0000h]

HB_SR_CNFG is shown in Table 8-33.

Return to the Summary Table.

Configures slew rate timing for each half-bridge.

Table 8-33. HB_SR_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	OUT6_SR	R/W	0h	Configures slew rate for half-bridge 6. 00b = 1.6 V/μs 01b = 13.5 V/μs 10b = 24 V/μs
9-8	OUT5_SR	R/W	0h	Configures slew rate for half-bridge 5. 00b = 1.6 V/μs 01b = 13.5 V/μs 10b = 24 V/μs
7-6	OUT4_SR	R/W	0h	Configures slew rate for half-bridge 4. 00b = 1.6 V/μs 01b = 13.5 V/μs 10b = 24 V/μs
5-4	OUT3_SR	R/W	0h	Configures slew rate for half-bridge 3. 00b = 1.6 V/μs 01b = 13.5 V/μs 10b = 24 V/μs
3-2	OUT2_SR	R/W	0h	Configures slew rate for half-bridge 2. 00b = 1.6 V/μs 01b = 13.5 V/μs 10b = 24 V/μs
1-0	OUT1_SR	R/W	0h	Configures slew rate for half-bridge 1. 00b = 1.6 V/μs 01b = 13.5 V/μs 10b = 24 V/μs

8.2.19 HB_ITRIP_CNFG Register (Offset = 1Bh) [Reset = 0000h]

HB_ITRIP_CNFG is shown in Table 8-34.

Return to the Summary Table.

Configures ITRIP levels and enables ITRIP for each half-bridge. ITRIP levels are shared between half-bridge pairs.

Table 8-34. HB_ITRIP_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT6_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 6.
14	OUT5_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 5.
13	OUT4_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 4.
12	OUT3_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 3.
11	OUT2_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 2.
10	OUT1_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 1.
9-8	OUT6_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold level for half-bridge 6. 00b = 2.3 A. 01b = 5.4 A 10b = 6.2 A 11b = Reserved.
7-6	OUT5_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold level for half-bridge 5. 00b = 2.9 A 01b = 6.6 A 10b = 7.6 A 11b = Reserved.
5-4	OUT4_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold level for half-bridge 4. 00b = 1.3 A 01b = 2.5 A 10b = 3.4 A 11b = Reserved.
3-2	OUT3_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold level for half-bridge 3. 00b = 1.3 A 01b = 2.5 A 10b = 3.4 A 11b = Reserved.
1	OUT2_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold level for half-bridge 2. 0b = 0.7 A 1b = 0.875 A
0	OUT1_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold level for half-bridge 1. 0b = 0.7 A 1b = 0.875 A

8.2.20 HB_ITRIP_FREQ Register (Offset = 1Ch) [Reset = 0000h]

HB_ITRIP_FREQ is shown in Table 8-35.

Return to the Summary Table.

Configures ITRIP frequency and deglitch for each half-bridge. ITRIP timing is shared between half-bridge pairs.

Table 8-35. HB_ITRIP_FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13-12	HB_TOFF_SEL	R/W	0h	Toff selection for OUT1-6 half bridge drivers. Here T is decided by OUTx_ITRIP_FREQ. 00b - Zero, disabled 01b - Toff = T/2 10b - Toff=T/4 11b - Toff=T
11-10	OUT6_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 6. 00b = 20 kHz 01b = 10 kHz 10b = 5 kHz 11b = 2.5 kHz
9-8	OUT5_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 5. 00b = 20 kHz 01b = 10 kHz 10b = 5 kHz 11b = 2.5 kHz
7-6	OUT4_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 4. 00b = 20 kHz 01b = 10 kHz 10b = 5 kHz 11b = 2.5 kHz
5-4	OUT3_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 3. 00b = 20 kHz 01b = 10 kHz 10b = 5 kHz 11b = 2.5 kHz
3-2	OUT2_ITRIP_FREQ/ PWM_OUT2_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 2. 00b = 20 kHz 01b = 10 kHz 10b = 5 kHz 11b = 2.5 kHz When OUT2_MODE = 1. Used for PWM FREQ settings PWM_OUT2_FREQ: 00b - 108Hz 01b - 217Hz 10b - 289Hz 11b - 434Hz
1-0	OUT1_ITRIP_FREQ/ PWM_OUT1_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 1. 00b = 20 kHz 01b = 10 kHz 10b = 5 kHz 11b = 2.5 kHz When OUT1_MODE = 1. Used for PWM FREQ settings PWM_OUT1_FREQ: 00b - 108Hz 01b - 217Hz 10b - 289Hz 11b - 434Hz

8.2.21 HS_HEAT_OUT_CNFG Register (Offset = 1Dh) [Reset = 0000h]

HS_HEAT_OUT_CNFG is shown in Table 8-36.

Return to the Summary Table.

Configures the output mode for each high-side driver and heater.

Table 8-36. HS_HEAT_OUT_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	HEAT_CNFG	R/W	0h	Configuration for heater driver. Enables or disables control of heater, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM1 pin control 11b = Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	OUT12_CNFG	R/W	0h	Configuration for high-side driver 12. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
9-8	OUT11_CNFG	R/W	0h	Configuration for high-side driver 11. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
7-6	OUT10_CNFG	R/W	0h	Configuration for high-side driver 10. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
5-4	OUT9_CNFG	R/W	0h	Configuration for high-side driver 9. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
3-2	OUT8_CNFG	R/W	0h	Configuration for high-side driver 8. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
1-0	OUT7_CNFG	R/W	0h	Configuration for high-side driver 7. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator

8.2.22 HS_OC_CNFG Register (Offset = 1Eh) [Reset = 1000h]

HS_OC_CNFG is shown in Table 8-37.

Return to the Summary Table.

Configures overcurrent threshold for each high-side driver.

Table 8-37. HS_OC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	OUT11_EC_MODE	R/W	1h	Bit sets high-side OUT11 for independent control through OUT11_CNFG bits or for supply for Electrochromic dirver. 0b = OUT11 is configured as independent high-side driver. Drain of EC FET is connected to PVDD 1b = OUT11 is configured as supply for EC FET
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	OUT12_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 12. 0b = Low current threshold 1b = High current threshold
4	OUT11_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 11. 0b = Low current threshold 1b = High current threshold
3	OUT10_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 10. 0b = Low current threshold 1b = High current threshold
2	OUT9_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 9. 0b = Low current threshold 1b = High current threshold
1	OUT8_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 8. 0b = Low current threshold 1b = High current threshold
0	OUT7_RDSON_MODE	R/W	0h	Configures high-side driver 7 between high RDSON mode and low RDSON mode (for bulb/lamp load). 0b = High RDSON mode (LED driver mode) 1b = Low RDSON mode (bulb/lamp driver mode)

8.2.23 HS_OL_CNFG Register (Offset = 1Fh) [Reset = 0000h]

HS_OL_CNFG is shown in Table 8-38.

Return to the Summary Table.

Configures open load threshold for each high-side driver.

Table 8-38. HS_OL_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	OUT12_OLA_TH	R/W	0h	Configures high-side driver 12 open load threshold. 0b = Low threshold 1b = High threshold
12	OUT11_OLA_TH	R/W	0h	Configures high-side driver 11 open load threshold. 0b = Low threshold 1b = High threshold
11	OUT10_OLA_TH	R/W	0h	Configures high-side driver 10 open load threshold. 0b = Low threshold 1b = High threshold
10	OUT9_OLA_TH	R/W	0h	Configures high-side driver 9 open load threshold. 0b = Low threshold 1b = High threshold
9	OUT8_OLA_TH	R/W	0h	Configures high-side driver 8 open load threshold. 0b = Low threshold 1b = High threshold
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	OUT12_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 12.
4	OUT11_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 11.
3	OUT10_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 10.
2	OUT9_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 9.
1	OUT8_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 8.
0	OUT7_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 7.

8.2.24 HS_REG_CNFG1 Register (Offset = 20h) [Reset = 0000h]

HS_REG_CNFG1 is shown in Table 8-39.

Return to the Summary Table.

Configures OUT7 ITRIP settings.

Table 8-39. HS_REG_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	OUT7_ITRIP_EN	R/W	0h	Enables ITRIP for high-side driver 7.
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3-2	OUT7_ITRIP_FREQ	R/W	0h	Configures OUT7 ITRIP regulation frequency. 00b = 1.7 kHz 01b = 2.2 kHz 10b = 3 kHz 11b = 4.4 kHz
1-0	OUT7_ITRIP_DG	R/W	0h	Configures OUT7 ITRIP deglitch time. 00b = 48 μs 01b = 40 μs 10b = 32 μs 11b = 24 μs

8.2.25 HS_REG_CNFG2 Register (Offset = 21h) [Reset = 0000h]

HS_REG_CNFG2 is shown in Table 8-40.

Return to the Summary Table.

Configures constant current mode for each high-side driver.

Table 8-40. HS_REG_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	OUT12_CCM_TO	R/W	0h	Configures the constant current mode current limit option of high-side output 12. 0b = 350 mA 1b = 450 mA
12	OUT11_CCM_TO	R/W	0h	Configures the constant current mode current limit option of high-side output 11. 0b = 350 mA 1b = 450 mA
11	OUT10_CCM_TO	R/W	0h	Configures the constant current mode current limit option of high-side output 10. 0b = 350 mA 1b = 450 mA
10	OUT9_CCM_TO	R/W	0h	Configures the constant current mode current limit option of high-side output 9. 0b = 350 mA 1b = 450 mA
9	OUT8_CCM_TO	R/W	0h	Configures the constant current mode current limit option of high-side output 8. 0b = 350 mA 1b = 450 mA
8	OUT7_CCM_TO	R/W	0h	Configures the constant current mode current limit option of high-side output 7. CCM values are based on OUT7_RDSON_MODE. If OUT7_RDSON_MODE = 0b: 0b = 250 mA 1b = 330 mA IF OUT7_RDSON_MODE = 1b: 0b = 360 mA 1b = 450 mA
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	OUT12_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 12.
4	OUT11_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 11.
3	OUT10_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 10.
2	OUT9_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 9.
1	OUT8_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 8.
0	OUT7_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 7.

8.2.26 HS_PWM_FREQ_CNFG Register (Offset = 22h) [Reset = 0000h]

HS_PWM_FREQ_CNFG is shown in Table 8-41.

Return to the Summary Table.

Configures the frequency for each dedicated PWM generator.

Table 8-41. HS_PWM_FREQ_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	PWM_OUT12_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 12. 00b = 108 Hz 01b = 217 Hz 10b = 289 Hz 11b = 434 Hz
9-8	PWM_OUT11_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 11. 00b = 108 Hz 01b = 217 Hz 10b = 289 Hz 11b = 434 Hz
7-6	PWM_OUT10_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 10. 00b = 108 Hz 01b = 217 Hz 10b = 289 Hz 11b = 434 Hz
5-4	PWM_OUT9_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 9. 00b = 108 Hz 01b = 217 Hz 10b = 289 Hz 11b = 434 Hz
3-2	PWM_OUT8_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 8. 00b = 108 Hz 01b = 217 Hz 10b = 289 Hz 11b = 434 Hz
1-0	PWM_OUT7_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 7. 00b = 108 Hz 01b = 217 Hz 10b = 289 Hz 11b = 434 Hz

8.2.27 HEAT_CNFG Register (Offset = 23h) [Reset = 0A3Ch]

HEAT_CNFG is shown in Table 8-42.

Return to the Summary Table.

Configures heater driver and fault responses.

Table 8-42. HEAT_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-8	HEAT_VDS_LVL	R/W	Ah	Heater MOSFET VDS monitor protection threshold. 0000b = 0.06 V 00001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.24 V 1001b = 0.28 V 1010b = 0.32 V 1011b = 0.36 V 1100b = 0.4 V 1101b = 0.44 V 1110b = 0.56 V 1111b = 1 V
7-6	HEAT_VDS_MODE	R/W	0h	Heater MOSFET VDS overcurrent monitor fault mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	HEAT_VDS_BLK	R/W	3h	Heater MOSFET VDS monitor blanking time. 00b = 4 µs 01b = 8 µs 10b = 16 µs 11b = 32 µs
3-2	HEAT_VDS_DG	R/W	3h	Heater MOSFET VDS overcurrent monitor deglitch time. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
1	HEAT_OLP_EN	R/W	0h	Enables heater offline open load detection circuit.
0	RESERVED	R/W	0h	Reserved

8.2.28 EC_CNFG Register (Offset = 24h) [Reset = 0000h]

EC_CNFG is shown in Table 8-43.

Return to the Summary Table.

Configures electrochrome driver and fault responses.

Table 8-43. EC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	ECFB_DIAG	R/W	0h	Enables open-load detection circuit on ECFB. 00b = disable 01b = SC 10b = OLP 11b = disable/reserved
13-12	EC_OUT11_OCP_DG	R/W	0h	OUT11 OCP Deglitch setting when EC_MODE=1 00b = 6 µs 01b = 10 µs 10b = 15 µs 11b = 60 µs
11-10	ECFB_SC_RSEL	R/W	0h	ECFB Diagnostic short-circuit detection options. 00b = 0.5 Ω 01b = 1.0 Ω 10b = 2.0 Ω 11b = 3.0 Ω
9-8	ECFB_OV_DG	R/W	0h	Configures overvoltage fault deglitch time. 00b = 20 µs 01b = 50 µs 10b = 100 µs 11b = 200 µs
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5-4	ECFB_OV_MODE	R/W	0h	Configures ECFB OV fault response for EC driver. 0b = No action 01b = Report ECFB_OV if voltage > 3V longer than EFB_OV_DG time. 10b = Report ECFB_OV if voltage > 3V longer than EFB_OV_DG time, drive ECDRV low with pulldown.
3	EC_FLT_MODE	R/W	0h	Configures overcurrent fault response for EC driver. 0b = Hi-Z EC Driver 1b = Retry with OUT7 ITRIP settings
2	ECFB_LS_PWM	R/W	0h	Enables LS PWM discharge for EC load. 0b = No PWM discharge (Fast discharge) 1b = PWM discharge enabled
1	EC_OLEN	R/W	0h	This bit enables the open load detection circuit during EC discharge. 0b = Open load detection disabled during EC discharge 1b = Open load detection enabled during EC discharge
0	ECFB_MAX	R/W	0h	Configures the maximum target voltage for EC. 0b = 1.2 V 1b = 1.5 V

8.2.29 HS_REG_CNFG3 Register (Offset = 25h) [Reset = 0000h]

HS_REG_CNFG3 is shown in Table 8-44.

Return to the Summary Table.

Configures HS ITRIP settings.

Table 8-44. HS_REG_CNFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	HS_OUT_ITRIP_FREQ	R/W	0h	ITRIP FREQ settings for OUT8-12 00b - 1.7KHz 01b - 2.2KHz 10b - 3KHz 11b - 4.4KHz
9-8	HS_OUT_ITRIP_DG	R/W	0h	Common ITRIP deglitch settings for OUT8-12 drivers 00b - 48 µs 01b - 40 µs 10b - 32 µs 11b - 24 µs
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	HS_OUT12_ITRIP_EN	R/W	0h	Enables ITRIP for high-side driver 12.
3	HS_OUT11_ITRIP_EN	R/W	0h	Enables ITRIP for high-side driver 11.
2	HS_OUT10_ITRIP_EN	R/W	0h	Enables ITRIP for high-side driver 10.
1	HS_OUT9_ITRIP_EN	R/W	0h	Enables ITRIP for high-side driver 9.
0	HS_OUT8_ITRIP_EN	R/W	0h	Enables ITRIP for high-side driver 8.

8.2.30 SPARE_CNFG2 Register (Offset = 26h) [Reset = 0000h]

SPARE_CNFG2 is shown in Table 8-45.

Return to the Summary Table.

Spare configuration register.

Table 8-45. SPARE_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

8.2.31 OUT1_HS_MODE_DC Register (Offset = 27h) [Reset = 0000h]

OUT1_HS_MODE_DC is shown in Table 8-46.

Return to the Summary Table.

Configures 10 bits for duty cycle

Table 8-46. OUT1_HS_MODE_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT1_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for OUT1 with max value of 1022 when OUT1_MODE=1.

8.2.32 OUT2_HS_MODE_DC Register (Offset = 28h) [Reset = 0000h]

OUT2_HS_MODE_DC is shown in Table 8-47.

Return to the Summary Table.

Configures 10 bits for duty cycle

Table 8-47. OUT2_HS_MODE_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT2_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for OUT2 with max value of 1022 when OUT2_MODE=1.

8.3 DRV8000-Q1_CTRL Registers

Table 8-48 lists the memory-mapped registers for the DRV8000-Q1_CTRL registers. All register offset addresses not listed in Table 8-48 should be considered as reserved locations and the register contents should not be modified.

Table 8-48. DRV8000-Q1_CTRL Registers

Offset	Acronym	Register Name	Section
29h	IC_CTRL	IC control register.	Section 8.3.1
2Ah	GD_HB_CTRL	Gate driver and half-bridge control register.	Section 8.3.2
2Bh	HS_EC_HEAT_CTRL	High-side driver, EC, and heater driver control register.	Section 8.3.3
2Ch	OUT7_PWM_DC	OUT7 PWM Duty cycle control register.	Section 8.3.4
2Dh	OUT8_PWM_DC	OUT8 PWM Duty cycle control register.	Section 8.3.5
2Eh	OUT9_PWM_DC	OUT9 PWM Duty cycle control register.	Section 8.3.6
2Fh	OUT10_PWM_DC	OUT10 PWM Duty cycle control register.	Section 8.3.7
30h	OUT11_PWM_DC	OUT11 PWM Duty cycle control register.	Section 8.3.8
31h	OUT12_PWM_DC	OUT12 PWM Duty cycle control register.	Section 8.3.9

Complex bit access types are encoded to fit into small table cells. Table 8-49 shows the codes that are used for access types in this section.

Table 8-49. DRV8000-Q1_CTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 IC_CTRL Register (Offset = 29h) [Reset = 006Ch]

IC_CTRL is shown in Table 8-50.

Return to the Summary Table.

Control register to lock and unlock configuration or control registers, and clear faults.

Table 8-50. IC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	IPROPI_MODE	R/W	0h	Selects IPROPI/PWM2 pin mode between input and output modes. 0b = Output (IPROPI mode) 1b = Input (PWM mode)
12-8	IPROPI_SEL	R/W	0h	Controls IPROPI MUX output between current, voltage, and temperature sense output. 00000b = No output 00001b = OUT1 current sense output 00010b = OUT2 current sense output 00011b = OUT3 current sense output 00100b = OUT4 current sense output 00101b = OUT5 current sense output 00110b = OUT6 current sense output 00111b = OUT7 current sense output 01000b = OUT8 current sense output 01001b = OUT9 current sense output 01010b = OUT10 current sense output 01011b = OUT11 current sense output 01100b = OUT12 current sense output 01101b = Reserved. 01110b = Reserved. 01111b = Reserved. 10000b = VPVDD Sense Nominal Range (5V -22V) 10001b = Thermal cluster 1 output 10010b = Thermal cluster 2 output 10011b = Thermal cluster 3 output 10100b = Thermal cluster 4 output 10101b = VPVDD Sense High Range (20V - 32V)
7-5	CTRL_LOCK	R/W	3h	Lock and unlock the control registers. Bit settings not listed have no effect. 011b = Unlock all control registers. 110b = Lock the control registers by ignoring further writes except to the IC_CTRL register.
4-2	CNFG_LOCK	R/W	3h	Lock and unlock the configuration registers. Bit settings not listed have no effect. 011b = Unlock all configuration registers. 110b = Lock the configuration registers by ignoring further writes.
1	WD_RST	R/W	0h	Watchdog restart. 0b by default after power up. Invert this bit to restart the watchdog timer. After written, the bit reflects the new inverted value.
0	CLR_FLT	R/W	0h	Clear latched fault status information. 0b = Default state. 1b = Clear latched fault bits, resets to 0b after completion. It also clears SPI fault and watchdog fault status.

8.3.2 GD_HB_CTRL Register (Offset = 2Ah) [Reset = 0000h]

GD_HB_CTRL is shown in Table 8-51.

Return to the Summary Table.

Gate driver and half-bridge output control register.

Table 8-51. GD_HB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	S_HIZ2	R/W	0h	Gate driver 2 Hi-Z control bit. Active only in half-bridge input control mode. 0b = Outputs follow GD_IN2 signal. 1b = Gate drivers ISTRONG pulldowns are enabled. Half-bridge 2 Hi-Z
14	S_HIZ1	R/W	0h	Gate driver 1 Hi-Z control bit. Active only in half-bridge input control mode. 0b = Outputs follow GD_IN1 signal. 1b = Gate drivers ISTRONG pulldowns are enabled. Half-bridge 1 Hi-Z
13	S_IN2	R/W	0h	Register control bit alternative to GD_IN2 input pin signal. Enabled through IN2_MODE bit.
12	S_IN1	R/W	0h	Register control bit alternative to GD_IN1 input pin signal. Enabled through IN1_MODE bit.
11-10	OUT6_CTRL	R/W	0h	Integrated half-bridge output 6 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
9-8	OUT5_CTRL	R/W	0h	Integrated half-bridge output 5 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
7-6	OUT4_CTRL	R/W	0h	Integrated half-bridge output 4 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
5-4	OUT3_CTRL	R/W	0h	Integrated half-bridge output 3 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
3-2	OUT2_CTRL	R/W	0h	Integrated half-bridge output 2 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
1-0	OUT1_CTRL	R/W	0h	Integrated half-bridge output 1 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD

8.3.3 HS_EC_HEAT_CTRL Register (Offset = 2Bh) [Reset = 0000h]

HS_EC_HEAT_CTRL is shown in Table 8-52.

Return to the Summary Table.

High-side driver, EC, and heater driver output control register.

Table 8-52. HS_EC_HEAT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECFB_LS_EN	R/W	0h	Enables EC discharge with LS MOSFET on ECFB while the EC regulation is active.
14	EC_ON	R/W	0h	Enables the EC output.
13-8	EC_V_TAR	R/W	0h	6-bits of resolution to control the target voltage on ECFB. 0 V to ECFB max (1.2 or 1.5V).
7	HEAT_EN	R/W	0h	Enables heater output.
6	RESERVED	R/W	0h	Reserved
5	OUT12_EN	R/W	0h	Enables high-side driver 12.
4	OUT11_EN	R/W	0h	Enables high-side driver 11.
3	OUT10_EN	R/W	0h	Enables high-side driver 10.
2	OUT9_EN	R/W	0h	Enables high-side driver 9.
1	OUT8_EN	R/W	0h	Enables high-side driver 8.
0	OUT7_EN	R/W	0h	Enables high-side driver 7.

8.3.4 OUT7_PWM_DC Register (Offset = 2Ch) [Reset = 0000h]

OUT7_PWM_DC is shown in Table 8-53.

Return to the Summary Table.

10-bit duty cycle control for high-side driver 7.

Table 8-53. OUT7_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT7_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 7 with max value of 1022.

8.3.5 OUT8_PWM_DC Register (Offset = 2Dh) [Reset = 0000h]

OUT8_PWM_DC is shown in Table 8-54.

Return to the Summary Table.

10-bit duty cycle control for high-side driver 8.

Table 8-54. OUT8_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT8_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 8 with max value of 1022.

8.3.6 OUT9_PWM_DC Register (Offset = 2Eh) [Reset = 0000h]

OUT9_PWM_DC is shown in Table 8-55.

Return to the Summary Table.

10-bit duty cycle control for high-side driver 9.

Table 8-55. OUT9_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT9_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 9 with max value of 1022.

8.3.7 OUT10_PWM_DC Register (Offset = 2Fh) [Reset = 0000h]

OUT10_PWM_DC is shown in Table 8-56.

Return to the Summary Table.

10-bit duty cycle control for high-side driver 10.

Table 8-56. OUT10_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT10_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 10 with max value of 1022.

8.3.8 OUT11_PWM_DC Register (Offset = 30h) [Reset = 0000h]

OUT11_PWM_DC is shown in Table 8-57.

Return to the Summary Table.

10-bit duty cycle control for high-side driver 11.

Table 8-57. OUT11_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT11_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 11 with max value of 1022.

8.3.9 OUT12_PWM_DC Register (Offset = 31h) [Reset = 0000h]

OUT12_PWM_DC is shown in Table 8-58.

Return to the Summary Table.

10-bit duty cycle control for high-side driver 12.

Table 8-58. OUT12_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT12_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 12 with max value of 1022.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DRV800x-Q1 is a highly configurable multichannel integrated half-bridge and half-bridge MOSFET gate driver than can be used to drive a variety of different output loads. The design examples below highlight how to use and configure the device for different application use cases.

9.2 Typical Application

The typical application for the DRV8000-Q1 is to control multiple loads in a typical automotive door. These include multiple integrated half-bridges and high-side drivers, an electrochromic mirror driver and external high-side MOSFET driver for a heating element, and an external MOSFET H-bridge driver with current shunt amplifier. A high-level schematic example is shown in DRV8000-Q1 Typical Application below.

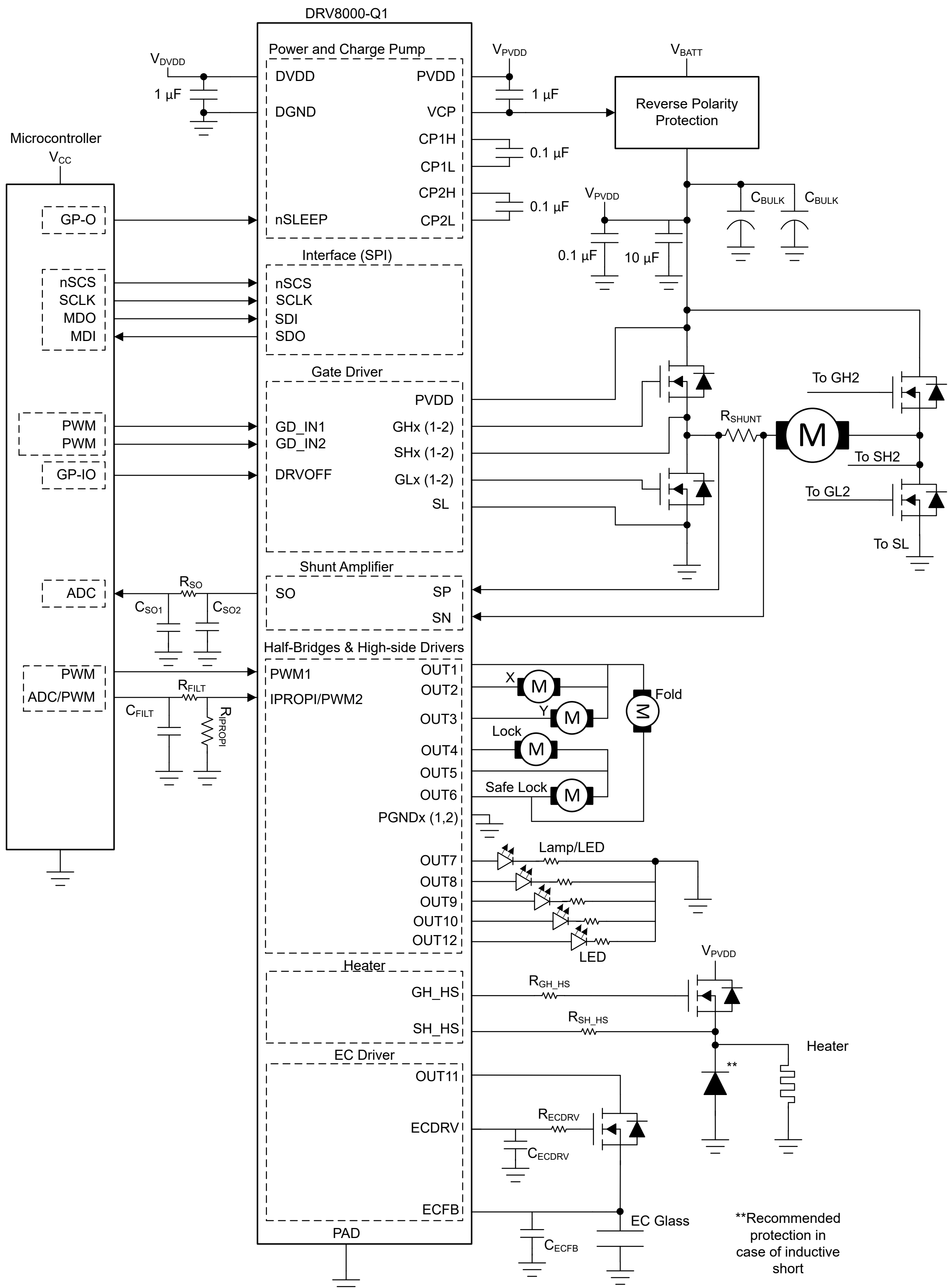


Figure 9-1. DRV8000-Q1 Typical Application

9.2.1 Design Requirements

Table 9-1 lists a set of example input parameters for the system design.

Table 9-1. Design Parameters

PARAMETER	VALUE
PVDD Supply Voltage Range	9 to 18V
PVDD Nominal Supply Voltage	13.5V
DVDD Logic Supply Voltage Range	3.3V
IPROPI Resistance	2.35kΩ
H-bridge MOSFET Total Gate Charge	30nC (typical) at V_{GS} = 10V
H-bridge MOSFET Gate to Drain Charge	5nC (typical)
H-bridge MOSFET On Resistance	4mΩ
Target Output Rise Time	750-1000ns
Target Output Fall Time	250-500ns
PWM Frequency	20kHz
Maximum H-bridge Motor Current	25A
Shunt Resistor Power Capability	3W

9.2.2 Detailed Design Procedure

9.2.2.1 I_{DRIVE} Calculation Example

The gate drive current strength, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the switch-node. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET can not turn on or off completely within the configured t_{DRIVE} time and a gate fault can be asserted. Additionally, slow rise and fall times leads to higher switching power losses in the external power MOSFETs. TI recommends to verify these values in system with the required external MOSFETs and load to determine the designed for settings.

The I_{DRIVEP} and I_{DRIVEN} for both the high-side and low-side external MOSFETs are configurable in register GD_IDRV_CNFG.

For MOSFETs with a known gate-to-drain charge (Q_{GD}), desired rise time (t_{rise}), and a desired fall time (t_{fall}), use Equation 4 and Equation 5 to calculate the approximate values of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} = Q_{GD} / t_{rise} \tag{4}$$

$$I_{DRIVEN} = Q_{GD} / t_{fall} \tag{5}$$

Using the input design parameters as an example, we can calculate the approximate values for I_{DRIVEP} and I_{DRIVEN}.

$$I_{DRIVEP\_HI} = 5nC / 750ns = 6.67mA \tag{6}$$

$$I_{DRIVEP\_LO} = 5nC / 1000ns = 5mA \tag{7}$$

Based on these calculations a value of 6mA was chosen for I_{DRIVEP}.

$$I_{DRIVEN\_HI} = 5nC / 250ns = 20mA \tag{8}$$

$$I_{DRIVEN\_LO} = 5nC / 500ns = 10mA \tag{9}$$

Based on these calculations, a value of 16 mA was chosen for I_{DRIVEN}.

9.2.2.2 t_{DRIVE} Calculation Example

The driver gate to source monitor timeout (t_{DRIVE}) is configured to allow sufficient time for the external MOSFETs to charge and discharge for the selected I_{DRIVE} gate current. By default, the setting is 8µs which is sufficient for many systems. Then determine an appropriate t_{DRIVE} value, the equation below can be utilized.

$$t_{DRIVE} > Q_{G\_TOT} / I_{DRIVE} \tag{10}$$

Using the input design parameters as an example, we can calculate the approximate values for t_{DRIVE}.

$$t_{DRIVE} > 30nC / 6mA = 5\mu s \tag{11}$$

Based on these calculations a value of 8 us was chosen for t_{DRIVE}.

9.2.2.3 Maximum PWM Switching Frequency

The maximum PWM frequency of the driver is typically determined by multiple factors in the system. While the DRV800x-Q1 device can support up to 100kHz, system parameters can limit this to a lower value.

These system parameters include:

- The rise and fall times of the external MOSFETs.
- The MOSFET Q_G and load on the charge pump.
- The minimum and maximum duty cycle requirements (Ex. 10% to 90%)

9.2.2.4 Current Shunt Amplifier Configuration

The DRV800x-Q1 differential shunt amplifier gain and shunt resistor value are selected based on the dynamic current range, reference voltage supply, shunt resistor power rating, and operating temperature range. In bidirectional operation of the shunt amplifier, the dynamic range at the output is approximately calculated as shown in the equation for Bidirectional SO Voltage. The output of the amplifier can swing from the midpoint reference (V_{DVDD} / 2) to either 0.25V or V_{DVDD} - 0.25V depending on the polarity of the input voltage to the amplifier.

$$V_{SO\_BI} = (V_{DVDD} - 0.25V) - (V_{DVDD} / 2) \tag{12}$$

If only unidirectional current sensing is required, the amplifier reference can be modified to expand the dynamic range at the output. The is modified through the CSA_DIV SPI register setting. In this mode, the dynamic range at the output is approximately calculated as shown in V_{SO_UNI}.

$$V_{SO\_UNI} = (V_{DVDD} - 0.25V) - (V_{DVDD} / 8) \tag{13}$$

Based on V_{DVDD} = 3.3V, the dynamic out range in both bidirectional or unidirectional sensing can be calculated as shown below:

$$V_{SO\_BI} = (3.3V - 0.25V) - (3.3V / 2) = 1.4V \tag{14}$$

$$V_{SO\_UNI} = (3.3V - 0.25V) - (3.3V / 8) = 2.6375V \tag{15}$$

The external shunt resistor value and shunt amplifier gain setting are selected based on the available dynamic output range, the shunt resistor power rating, and maximum motor current that needs to be measured. This exact values for the shunt resistance and amplifier gain are determine by both R_{SHUNT} calculation and Amplifier Gain calculation.

$$R_{SHUNT} < P_{SHUNT} / I_{MAX}{}^{2} \tag{16}$$

$$A_V < V_{SO} / (I_{MAX} \times R_{SHUNT}) \tag{17}$$

Based on V_{SO} = 1.4V, I_{MAX} = 25A and P_{SHUNT} = 3 W, the values for shunt resistance and amplifier gain can be calculated as shown below:

$$R_{SHUNT} < 3W / 25^2 A = 4.8m\Omega \tag{18}$$

$$A_V < 1.4V / (25A \times 4.8m\Omega) = 11.67V/V \tag{19}$$

Based on the results, a shunt resistance of 4mΩ and an amplifier gain of 10V/V can be selected.

9.3 Initialization Setup

9.4 Power Supply Recommendations

9.4.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The type of power supply, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor start-up and braking methods

The inductance between the power supply and motor drive system can limit the current rate from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

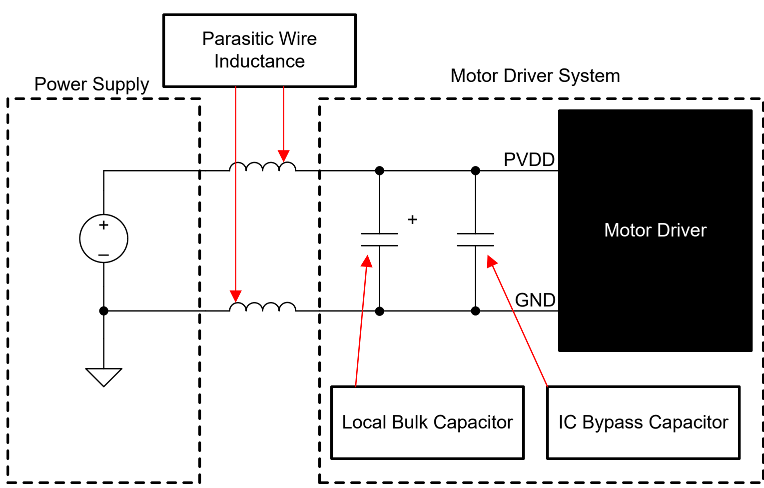


Figure 9-2. Motor Driver Supply Parasitics Example

9.5 Layout

9.5.1 Layout Guidelines

Bypass the PVDD pin to the GND pin using a low-ESR ceramic bypass capacitor C_{PVDD1}. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the GND pin. Additionally, bypass the PVDD pin using a bulk capacitor C_{PVDD2} rated for PVDD. This component can be electrolytic. This capacitance must be at least 10µF. Having the capacitance shared with the bulk capacitance for the external power MOSFETs is acceptable.

Place a low-ESR ceramic capacitor C_{FLY1} and C_{FLY2} between the CPL1 / CPH1 and CPL2 / CP2H pins. Additionally, place a low-ESR ceramic capacitor C_{VCP} between the VCP and PVDD pins.

Additional bulk capacitance is required to bypass the high current path on the external power MOSFETs of the H-bridge driver. Place this bulk capacitance such that the length of any high current paths is minimized through the external MOSFETs. Keep the connecting metal traces as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

For H-bridge driver external MOSFETs, bypass the drain pin to GND plane using a low-ESR ceramic bypass capacitor with appropriate voltage rating. Place this capacitor as close to the MOSFET drain and source pins as possible, with a thick trace or plane connection to GND plane. Place the series gate resistors as close to the MOSFET gate pins as possible.

For the current shunt amplifier, the placement of the sense resistor is in line with the components of the power stage to minimize trace impedance. If possible, the shunt resistor is also be placed close to the connection to the CSA to decrease the possibility of coupling on other traces on the board.

For high-side current sense, the shunt resistor is near the star point between the supply and the source of the high-side MOSFETs. For low-side current sense, the shunt resistor is between the source of the low-side MOSFET and the star point ground connection of the power stage. The remaining components is placed nearest to the device.

Routing of the sense signals is done using a differential pair. In a differential pair, both signals are tightly coupled in the layout and the traces must run parallel from the shunt or sense resistor to the CSA at the input of the IC.

Bypass the DVDD pin to the DGND pin with C_{DVDD}. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the DGND pin. If local bypass capacitors are already present on these power supplies in close proximity of the device to minimize noise, these additional components for DVDD are not required.

For the EC driver, place both the C_{ECDRV} and C_{ECFB} bypass capacitors to GND as close to the respective pins as possible.

Do not connect the SL pin directly to the GND plane. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations allow for more accurate VDS sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the SL pin.

9.5.2 Layout Example

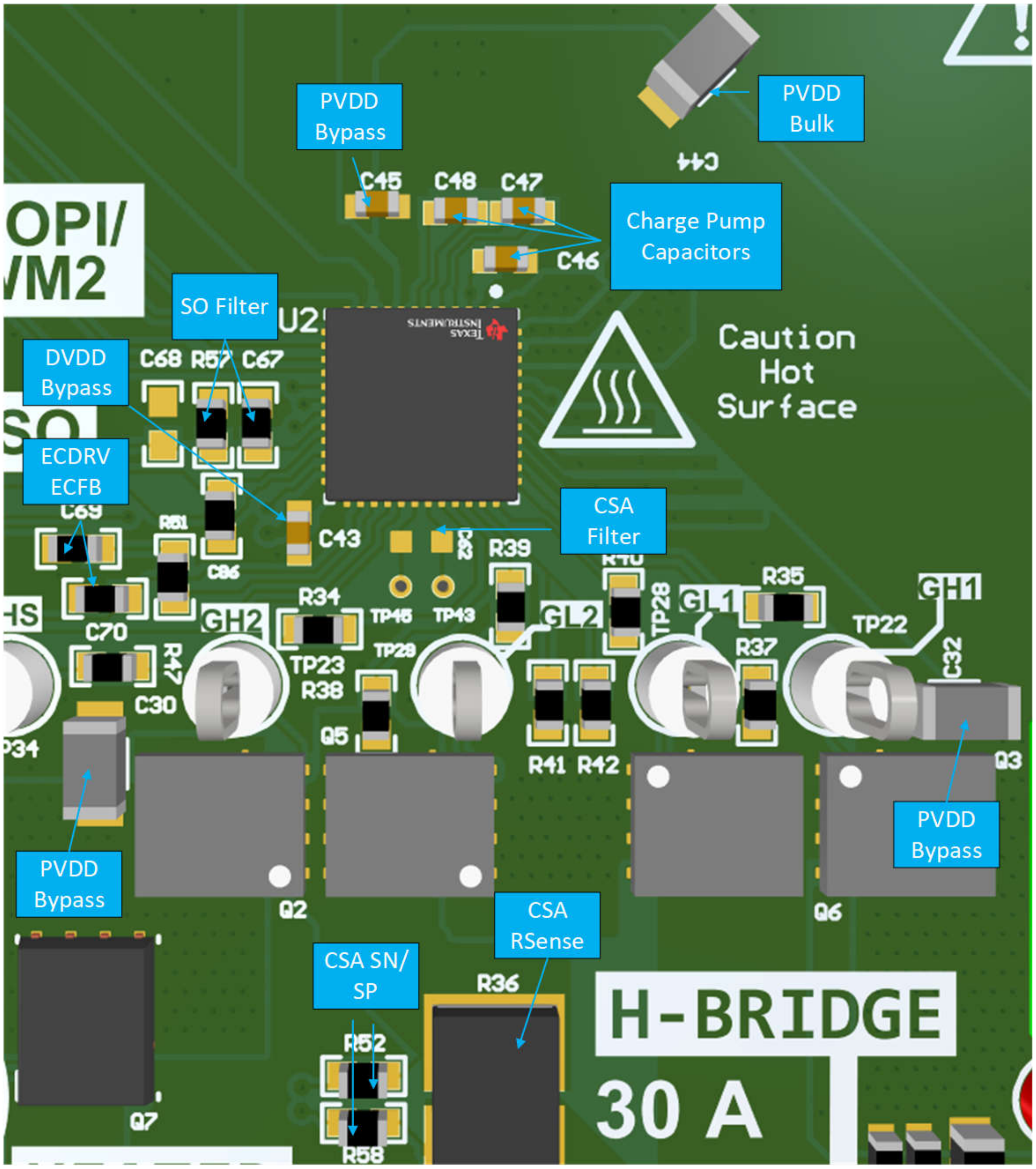


Figure 9-3. DRV8000-Q1 Component Placement and Layout

The layout screen shot above shows the device component and layout relative to the device. This layout screen shot comes from the device evaluation module. Note that all power supply decoupling capacitors, especially smaller values, and charge pump capacitors are placed as closed to the pins as possible and are placed on the same layer of the device. All general guidelines outlined in the previous section were followed in the evaluation module layout design when possible.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

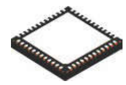
11 Pre-Production Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2024) to Revision A (October 2025)	Page

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

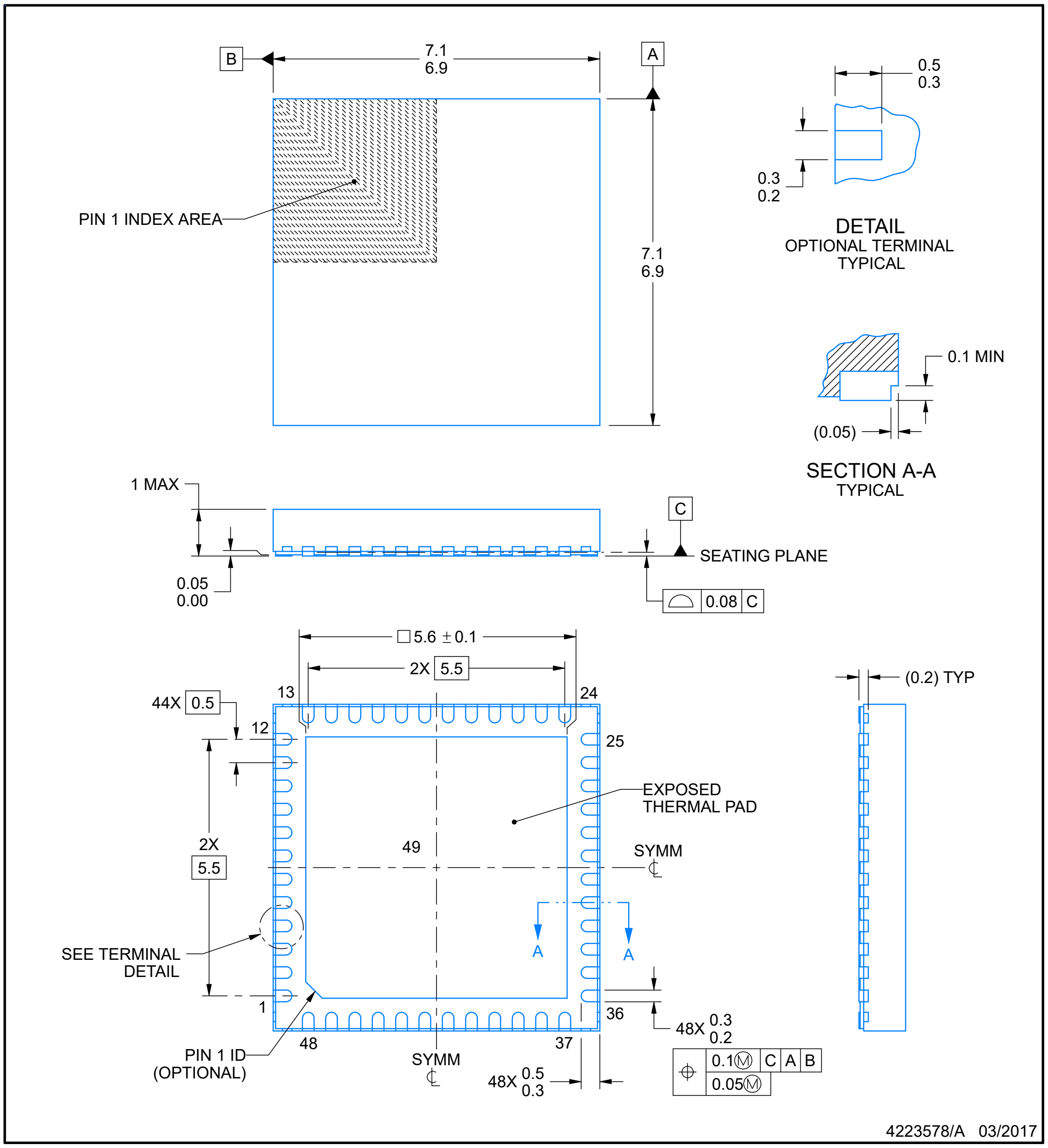


PACKAGE OUTLINE

RGZ0048M

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

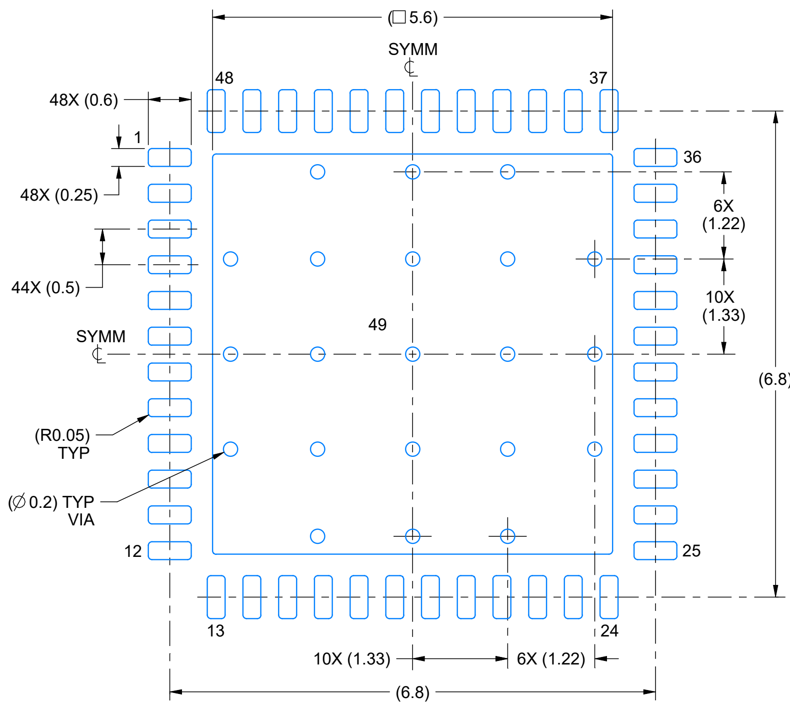
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

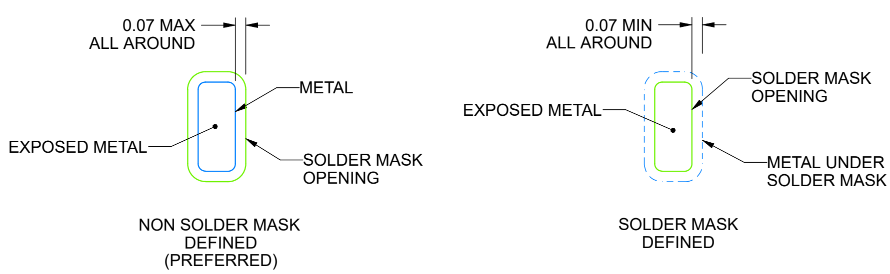
RGZ0048M

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4223578/A 03/2017

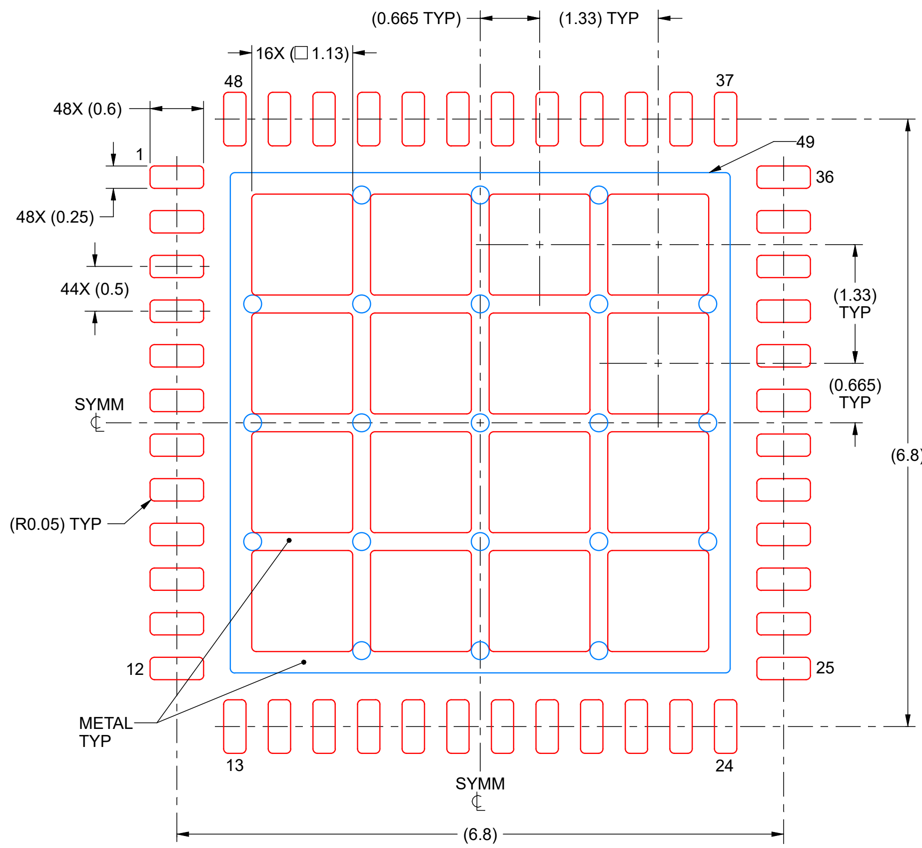
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048M **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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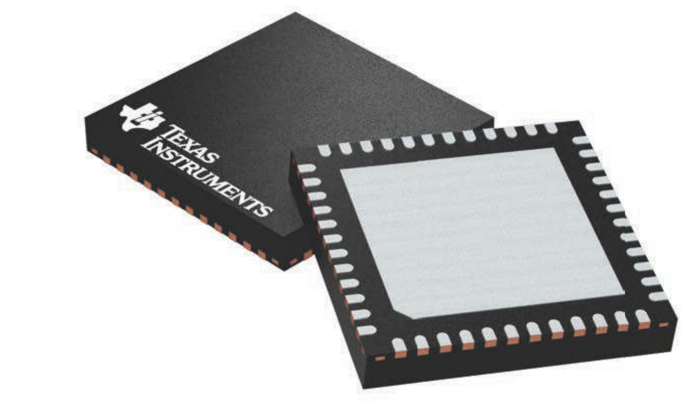
GENERIC PACKAGE VIEW

RGZ 48 **VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

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12.1 Package Option Addendum

Packaging Information

Orderable Device	Status	Package Type (1)	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PDRV8000QWRGZRQ1	PREVIEW	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	PDRV8000
DRV8000QWRGZRQ1	PRODUCTION	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

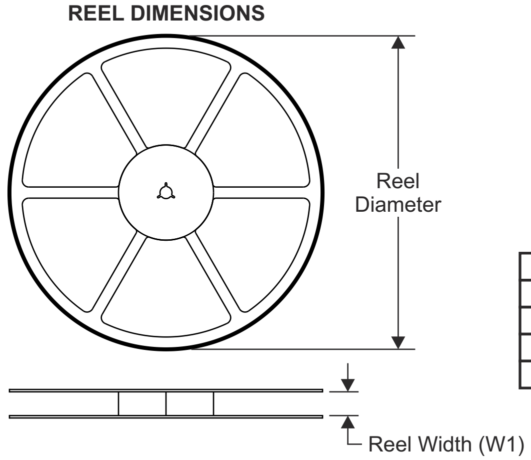
(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

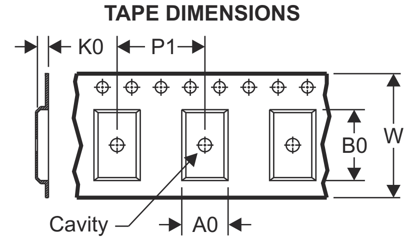
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

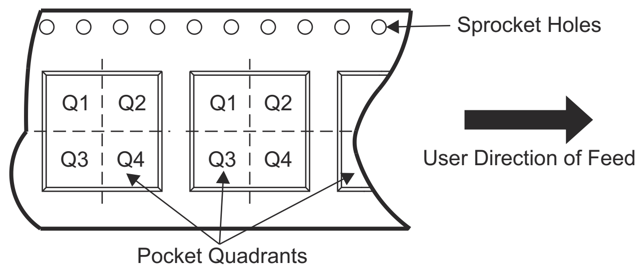
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

12.2 Tape and Reel Information



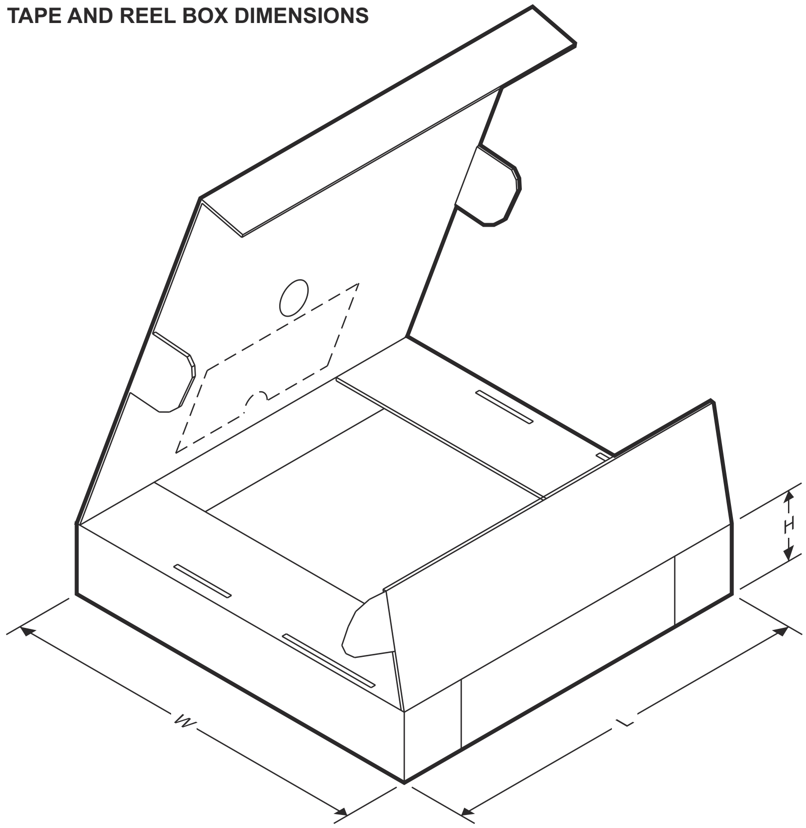


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8000QWRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12	16	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8000QWRGZRQ1	VQFN	RGZ	48	2500	367	367	35

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8000QWRGZRQ1	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8000

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

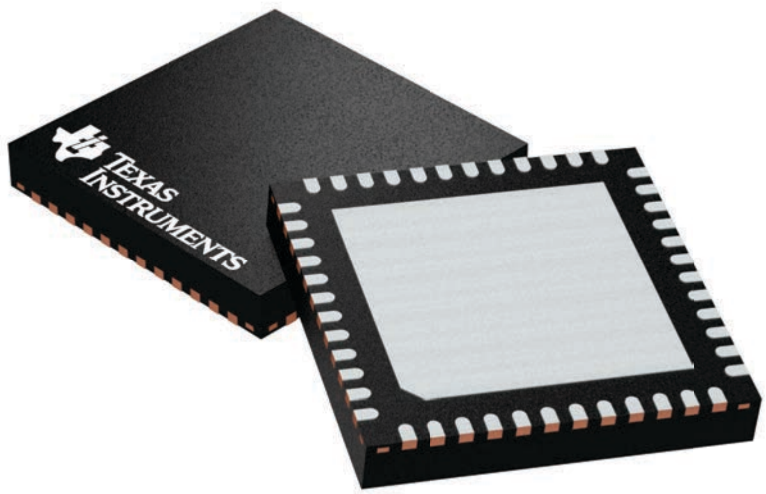
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGZ 48

VQFN - 1 mm max height

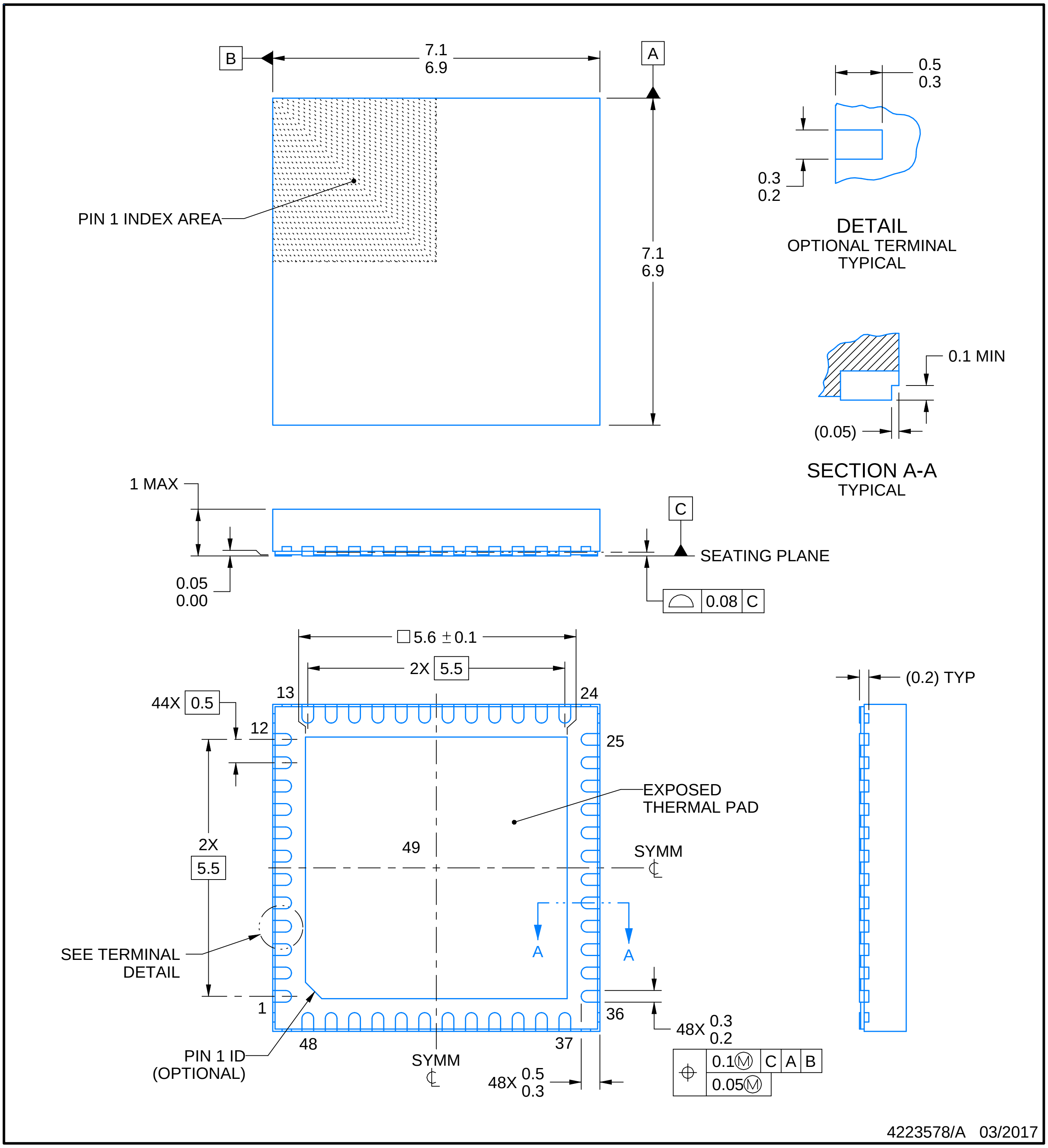
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



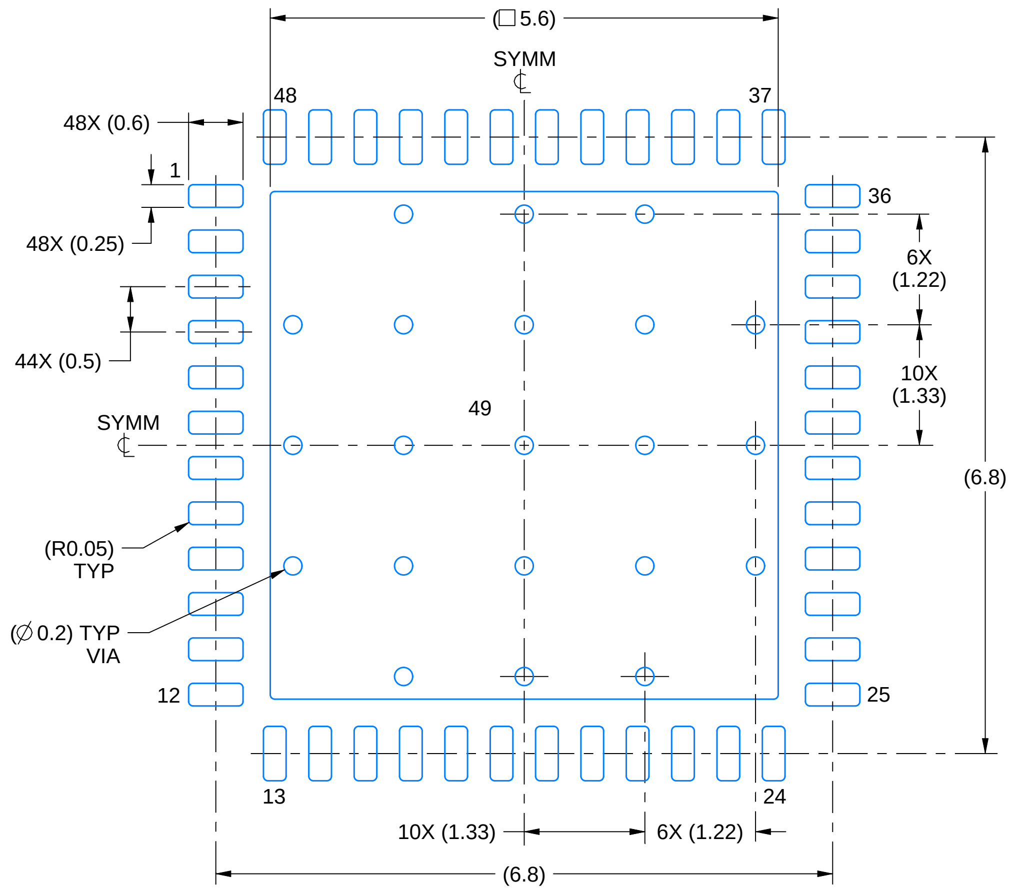
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

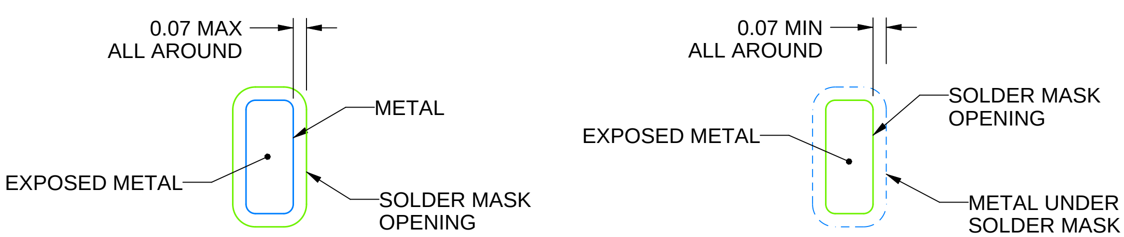


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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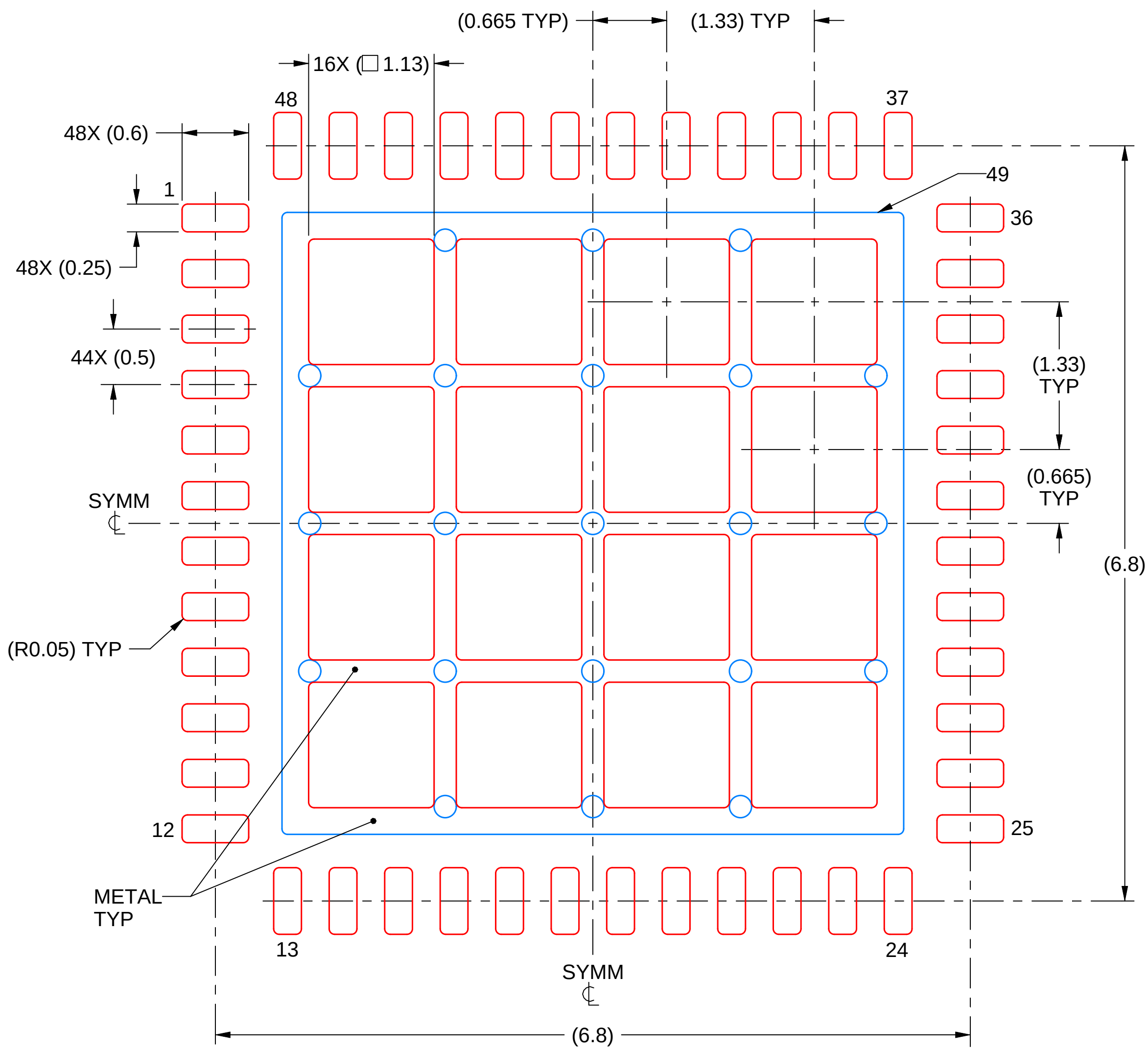
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.