DRV7308 Three Phase 650V, 5A, GaN Intelligent Power Module

1 Features

- Three-phase PWM motor driver with integrated 650V enhancement mode GaNFETs
- Up to 450V operating voltage
  - 650V absolute maximum voltage
- High output current capability: 5A Peak current
- Low conduction loss: Low on-state resistance per GaN FET: 205mΩ $R_{DS(ON)}$ at TA = 25°C
- Low switching loss: Zero reverse recovery, low output capacitance, slew rate control
- Low distortion: Ultra low propagation delay < 135ns, Ultra low adaptive dead time < 200ns
- Integrated gate drives with slew rate control of phase node voltage
  - Slew rate options from 5V/ns to 40V/ns
- 500ns minimum low side on time support with integrated fast bootstrap GaN rectifier
- Low-side GaN FET open source pins to support 1- or 2- or 3-shunt current sensing
- Supports up to 60kHz hard switching
- Integrates a 11MHz, 15V/µs amplifier for single shunt current sensing
- Supports 3.3V and 5V logic inputs
- Integrated BRAKE functionality to turn on all low side GaN FETs together
- Integrated temperature sensor
- >1.6mm clearance between OUTx and OUTx, VM and OUTx and OUTx and PGND.
- 2mm clearance between VM and PGND
- Integrated protection features
  - GVDD and bootstrap under voltage lockout
  - Over current protection for each GaN FET
  - Over temperature protection
  - PWM input dead time
  - Current limit protection using integrated comparators for all three phases
  - Fault condition indication pin (HV_nFAULT)

2 Applications

- Refrigerator & freezer
- Appliances and HVAC pumps and fans
- Dishwasher
- Small home appliances
- Residential air conditioners
- Cooker hood
- Brushless-DC motor modules

3 Description

The DRV7308 is a three-phase intelligent power module (IPM) that consists of 205mΩ, 650V e-mode Gallium-Nitride (GaN) for driving three-phase BLDC/ PMSM motors up to 450V DC rails. The applications include field-oriented control (FOC), sinusoidal current control, and trapezoidal (six step) current control of BLDC motors. The device helps to achieve more than 99% efficiency for a 3-phase modulated, FOC-driven, 250W motor drive application in a QFN 12mm x 12mm package at 20kHz switching frequency, eliminating the need for heat sink. The device helps to achieve ultra quiet operation, with very low dead time. The integrated bootstrap rectifier with bootstrap current limit, eliminates the need for an external bootstrap diode.

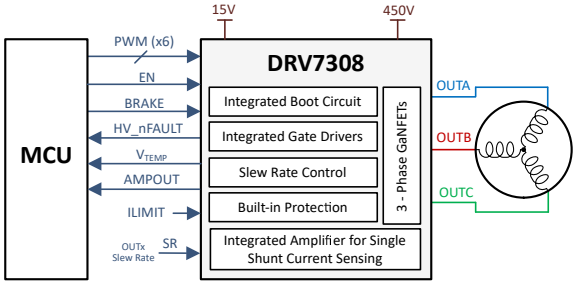
Note

For safety, TI recommends the use of isolated test equipment with overvoltage and overcurrent protection. TI recommends using a safety enclosure when operating the device.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)
DRV7308	REN (VQFN, 65)	12.00mm x 12.00mm

(1) For more information, see the Mechanical, Packaging, and Orderable Information .
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

ADVANCE INFORMATION

Table of Contents

ADVANCE INFORMATION

4 Pin Configuration and Functions

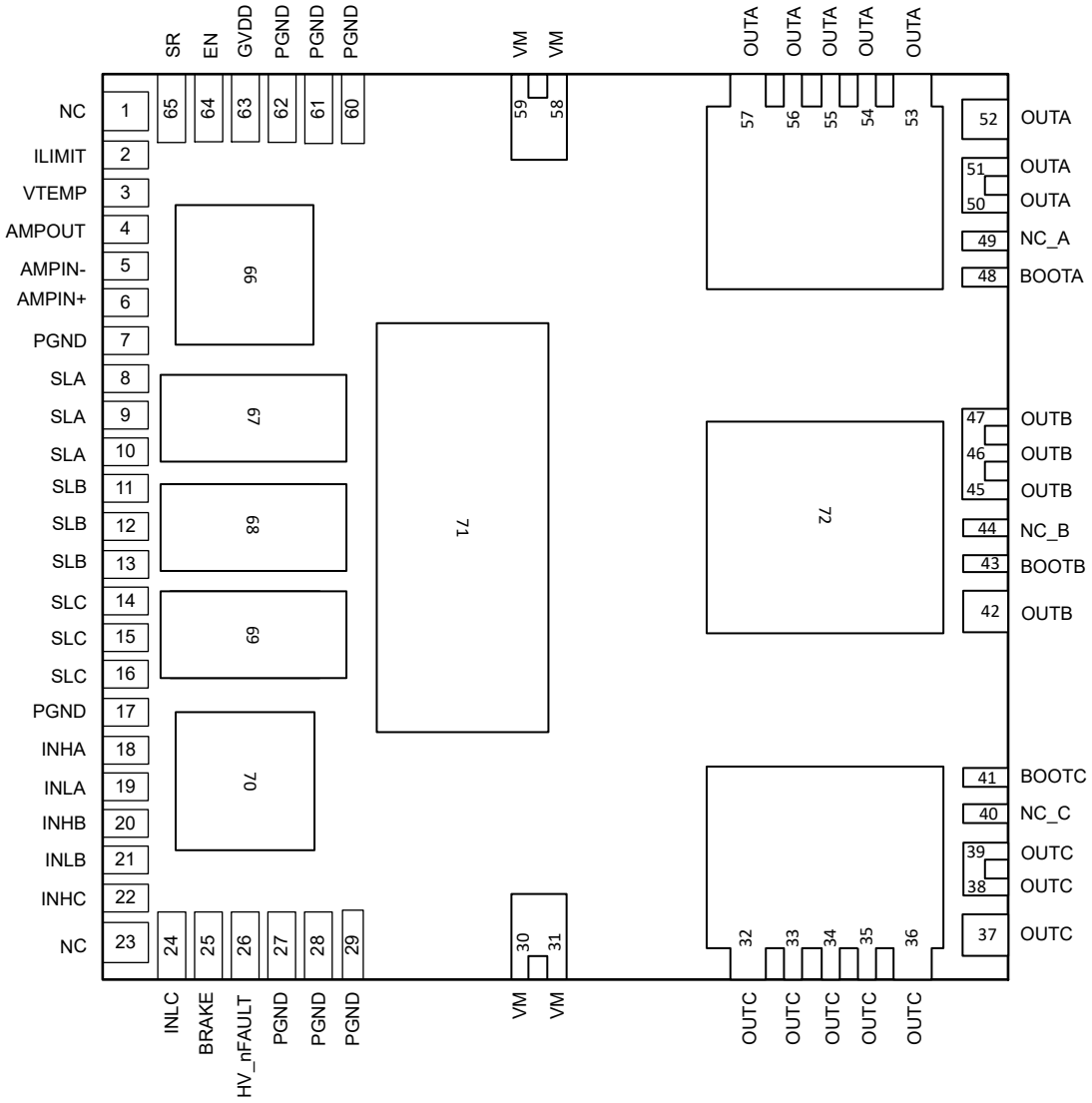


Figure 4-1. DRV7308 VQFN With Exposed Thermal Pad Top View

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AMPIN-	5	I	Inverting input of the operational amplifier
AMPIN+	6	I	Non-inverting input of the operational amplifier
AMPOUT	4	O	Output terminal of the operational amplifier
BOOTA	48	P	Bootstrap supply for phase A; bypass to OUTA with a GVDD rated capacitor
BOOTB	43	P	Bootstrap supply for phase B; bypass to OUTB with a GVDD rated capacitor
BOOTC	41	P	Bootstrap supply for phase C; bypass to OUTC with a GVDD rated capacitor
BRAKE	25	I	Motor Brake signal. Logic high on the pin turns on all the low side GaNFETs and turns off all the high side GaNFETs
EN	64	I	Driver enable pin. When this pin is logic low the device goes to shutdown mode and all the GaN FETs are turned off. A 20µs to 40µs low pulse can be used to reset fault conditions
HV_nFAULT	26	O	Fault indication pin. Pulled logic-low on fault condition; open-drain output requires an external pullup
ILIMIT	2	I	Reference voltage for over current limit for internal comparator
INHA	18	I	High-side driver control input for OUTA. This pin controls the output of the high-side GaNFET
INHB	20	I	High-side driver control input for OUTB. This pin controls the output of the high-side GaNFET
INHC	22	I	High-side driver control input for OUTC. This pin controls the output of the high-side GaNFET
INLA	19	I	Low-side driver control input for OUTA. This pin controls the output of the Low-side GaNFET
INLB	21	I	Low-side driver control input for OUTB. This pin controls the output of the Low-side GaNFET
INLC	24	I	Low-side driver control input for OUTC. This pin controls the output of the Low-side GaNFET
NC	1, 23		No connect, can be connected to PGND
NC_A	49	I	Can be connected to OUTA
NC_B	44	I	Can be connected to OUTB
NC_C	40	I	Can be connected to OUTC
OUTA	50-57	P	Half bridge output A
OUTB	42, 45-47, 72	P	Half bridge output B
OUTC	32-39	P	Half bridge output C
PGND	7, 17, 27,28,29, 60,61,62,66, 70, 71	G	Device power and signal ground. Connect to system ground
SLA	8, 9, 10, 67	P	Phase A half bridge low side source
SLB	11, 12, 13, 68	P	Phase B half bridge low side source
SLC	14, 15, 16, 69	P	Phase C half bridge low side source
SR	65	I	OUTx voltage slew rate control. Connect a resistor between SR pin and PGND or SR pin to GVDD to configure the slew rate
GVDD	63	P	Low voltage power supply; bypass to PGND with one 1µF, GVDD rated ceramic capacitor plus one bulk capacitor rated for GVDD
VM	30, 31, 58, 59	P	Power supply. Connect to motor supply voltage; bypass to PGND with a 0.1µF capacitor plus one bulk capacitor rated for VM
VTEMP	3	O	Temperature Sensor Output

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(2)

	MIN	MAX	UNIT
Drain-source blocking voltage (FET off) (V_{DS})		650	V
DC voltage applied between VM and PGND		450	V
Drain DC current (I_{DC}) @ TJ = 150ºC		4	A
Phase node pin voltage referred to PGND (OUTA, OUTB, OUTC)	-10	650	V
BOOTx pin voltage referred to OUTx (BOOTA, BOOTB, BOOTC) (1)	-0.5	20	V
Pin voltage - GVDD to PGND (1)	-0.5	20	V
Pin voltage - INx, EN, BRAKE, HV_nFAULT to PGND (1)	-0.5	20	V
Pin voltage - AMPIN+, AMPIN-, AMPOUT, ILIMIT, SR to PGND	-0.5	V_{GVDD}+0.3	V
Operational amlifier output current (AMPOUT)		20	mA
Operating ambiient temperature	-40	125	ºC
Operating junction temperature (T_J)	-40	150	ºC
Storage temperature (T_{stg})	-55	150	ºC

(1) For PDRV7308 devices limit the voltage to less than 16V
(2) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (All other pins - pin names)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge (VM, OUTx, BOOT, NCx)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	DC power supply voltage	VM	0		450	V
V_{GVDD}	Gate driver supply voltage (PDRV7308) (1)	GVDD	10.8		15	V
f_{PWM}	PWM frequency	OUTA, OUTB, OUTC		20	60	kHz
V_{IN}	Logic Input Voltage	INHx, INLx, EN, BRAKE	-0.1		5	V
V_{OD}	Open drain pull up voltage	HV_nFAULT	-0.1		5	V
I_{OD}	Open drain output sink current	HV_nFAULT	0		5	mA
V_{SR}	Slew rate pin voltage	SR			GVDD	V
V_{SLx}	SLx pin voltage	SLA, SLB, SLC	-1		1	V

ADVANCE INFORMATION

7 Recommended Operating Conditions (continued)

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{AMPINx}	Amplifier input pin voltage	AMPIN+, AMPIN-	-0.1		5	V
V_{ILIMIT}	Over current protection reference	ILIMIT	0.1		2	V
T_{ON_MIN}	Minimum low side on time @ Fsw = 20kHz/16kHz		0.5			µs
T_A			–40		100	°C
T_J			–40		125	°C

(1) Recommended maximum voltage at GVDD pin of PDRV7308 is 15V

8 Thermal Information

THERMAL METRIC(1)		DEVICE REN (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance per GaNFET	1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

9 Electrical Characteristics

T_J = –40°C to 150°C, V_{GVDD} = 15V, EN = High (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{GVDD} = 15V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GaN POWER TRANSISTOR						
$R_{DS(ON)}$	GaN transistor on resistance	V_{GVDD} = 15V, I_{OUTx} = 1A,T_J = 25ºC,		205	320	mΩ
$R_{DS(ON)}$	GaN transistor on resistance	V_{GVDD} = 15V, I_{OUTx} = 1A, T_J = 150ºC,		370		mΩ
V_{SD}	Third-quadrant mode source-drain voltage	INx = 0V, ISD = 0.1A, T_J = 25ºC		1.5		V
V_{SD}	Third-quadrant mode source-drain voltage	INx = 0V, ISD = 4A, T_J = 25ºC		2.8		V
Q_{RR}	Reverse recovery charge	V_R = 300 V, I_{SD} = 4 A, dI_{SD}/dt = 0.2 A/ns			0	nC
SWITCHING CHARACTERISTICS						
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM}= 300V, SR setting = 0		5		V/ns
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{VM}= 300V, SR setting = 0		5		V/ns
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM}= 300V, SR setting = 1		10		V/ns
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{VM}= 300V, SR setting = 1		10		V/ns
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM}= 300V, SR setting = 2		20		V/ns
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{VM}= 300V, SR setting = 2		20		V/ns

ADVANCE INFORMATION

9 Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{GVDD} = 15V, EN = High (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{GVDD} = 15V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM}= 300V, SR setting = 3		40		V/ns
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{VM}= 300V, SR setting = 3		40		V/ns
$t_{pd,on}$	Propagation delay, turn on	V_{INHx}, V_{INLx} = logic low to high, V_{VM} = 300V, I_D = 4A, SR = 0			125	ns
$t_{delay,on}$	Turn on delay time	V_{INHx}, V_{INLx} = logic low to high, V_{VM} = 300V, I_D = 4A, SR = 0		75		ns
$t_{pd,off}$	Propagation delay, turn off	V_{INHx}, V_{INLx} = logic high to low, V_{VM} = 300V, I_D = 4A, SR = 0			135	ns
$t_{delay,off}$	Turn off delay time	V_{INHx}, V_{INLx} = logic high to low, V_{VM} = 300V, I_D = 4A, SR = 0		75		ns
t_{DEAD}	Output dead time (high to low)	V_{VM} = 300V, I_{OUTx} = 4A, Current going out of phase node (OUTx)		40		ns
t_{DEAD}	Output dead time (high to low)	V_{VM} = 300V, I_{OUTx} = 4A, Current going in to phase node (OUTx), SR = 0		100		ns
t_{DEAD}	Output dead time (high to low)	V_{VM} = 300V, I_{OUTx} = 4A, Current going in to phase node (OUTx), SR = 1 or 2 or 3		100		ns
t_{DEAD}	Output dead time (low to high)	V_{VM} = 300V, I_{OUTx} = 4A, Current going in to phase node (OUTx)		40		ns
t_{MIN_PULSE}	Minimum input pulse width changing the output low-high-low	V_{GVDD} = 15V, V_{VM} = 300V		50		ns
t_{MIN_PULSE}	Minimum input pulse width changing the output high-low-high	V_{GVDD} = 15V, V_{VM} = 300V		50		ns
t_{start}	Start up time	V_{GVDD} > $V_{GVDD\_UV\_ON}$. EN = low to high, INLx = 1, low side GaNFET turns ON			2	ms
t_{off}	Device turn off time - to sleep	V_{GVDD} > $V_{GVDD\_UV\_ON}$. EN = high to low	40		80	us
tclr_flt	Time to clear any latched fault using EN	EN = low pulse witdth	20		40	us
t_{off}	Device turn off time- gate driver off	V_{GVDD} > $V_{GVDD\_UV\_ON}$. EN = high to low, INLx = 1, low side GaNFET turns OFF			500	ns
GVDD POWER SUPPLY						
$I_{GVDD,Q}$	GVDD operating curent, driver enabled, no switching	EN = High, V_{VM} = 300V, V_{GVDD} = 15V, INx = 0		4		mA
$I_{GVDD,3SW}$	GVDD average operating curent, driver enabled, GaN switching, No load at OUTx pins	EN = High, Fsw = 20kHz, 3-half bridge switching at 50% complimentary PWM, V_{VM} = 300V, V_{GVDD} = 15V, SR = 0		6		mA
$V_{GVDD\_UV\_ON}$	GVDD undervoltage turn on threshold	GVDD rising			10	V
$V_{GVDD\_UV\_OFF}$	GVDD undervoltage turn off threshold	GVDD falling	9			V
$V_{GVDD\_UV\_HYS}$	GVDD undervoltge detection hysterisis	GVDD rising to falling threshold		500		mV
t_{UVLO_GVDD}	GVDD undervoltage deglitch time				20	µs
BOOTSTRAP POWER SUPPLY						
R_{DS_BST}	Bootsrtap rectifier on resistance	V_{GVDD} = 15V, V_{VM} = 300V			30	Ω
I_{LMT_BST}	Bootstrap rectifier current limit	EN = High, V_{GVDD} = 15V, V_{VM} = 300V, INLx = High, INHx = Low, V_{BOOTx} - V_{OUTx} = 12V	150		250	mA
I_{BST_PK}	Bootstrap rectifier peak transient current	EN = High, V_{GVDD} = 15V, V_{VM} = 300V, INLx = High, INHx = Low, V_{BOOTx} - V_{OUTx} = 0 V		350		mA

ADVANCE INFORMATION

9 Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{GVDD} = 15V, EN = High (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{GVDD} = 15V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BST_Q}	Bootstrap quiescent current	EN = High, INHx = Low, INLx = Low, V_{GVDD} = 15V, V_{BOOTx} - V_{OUTx} = 12V		100		µA
I_{BST_Q}	Bootstrap quiescent current	EN = High, INHx = High, INLx = Low, V_{GVDD} = 15V, V_{BOOTx} - V_{OUTx} = 12V		350		µA
$V_{BST\_UV\_ON}$	Bootstrap supply undervoltage -turn on				9	V
$V_{BST\_UV\_OFF}$	Bootstrap supply undervoltage -turn off		8			V
$V_{BST\_UV\_HYS}$	Bootstrap supply undervoltage -hysterisis			500		mV
t_{BST_UV}	Bootstrap supply undervoltage deglitch time				20	µs
LOGIC-LEVEL INPUTS (EN, INHx, INLx, BRAKE)						
V_{IL}	Input logic low voltage	INHx, INLx, BRAKE, EN			0.8	V
V_{IH}	Input logic high voltage	INHx, INLx, BRAKE, EN	2.2			V
V_{HYS}	Input logic hysteresis	INHx, INLx, BRAKE, EN		400		mV
I_{IL}	Input logic low current (INHx, INLx, BRAKE, EN)	V_I = 0 V	-1		1	µA
I_{IL}	Input logic low current (BRAKE, EN)	V_I = 0 V	-1		1	µA
R_{PD}	Input pulldown resistance	INHx, INLx, EN	70	100	130	kΩ
R_{PD}	Input pulldown resistance	BRAKE	15	20	25	kΩ
t_{deg}	Input logic deglitch time	INHx, INLx	25		50	ns
t_{deg}	Input logic deglitch time	EN	150		400	ns
t_{deg}	Input logic deglitch time	BRAKE	1200		2000	ns
MULTI-LEVEL INPUT (SR)						
R_{L1}	SR setting = 0	Tied to PGND	0		1	kΩ
R_{L2}	SR setting = 1	Tied to GVDD	0		1	kΩ
R_{L3}	SR setting =2	R tied to PGND (R = 5 kΩ to 15 kΩ)	5		15	kΩ
R_{L4}	SR setting = 3	R tied to PGND (R = 40 kΩ to 100 kΩ)	40		100	kΩ
OPEN-DRAIN OUTPUTS (HV_nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	-1		1	µA
C_{OD}	Output capacitance				30	pF
GaN PREDRIVER PROTECTION						
I_{OCP_GaN}	Overcurrent detection threshold	V_{GVDD} = 15V, V_{VM} = 300V, T_J=25ºC	7.5			A
I_{OCP_GaN}	Overcurrent detection threshold	V_{GVDD} = 15V, V_{VM} = 300V, T_J=125ºC	5			A
$I_{OCP\_GaN\_BT}$	Blanking time (including deglitch)	V_{GVDD} = 15V, V_{VM} = 300V		150		ns
$I_{OCP\_GaN\_PD}$	Propagation delay (to FET turn off)	V_{GVDD} = 15V, V_{VM} = 300V		50		ns
T_{SD_RISE}	Thermal shutdown rising	Die temperature (T_J)	145	165	185	ºC
T_{SD_FALL}	Thermal shutdown falling	Die temperature (T_J)	125	145	165	ºC
T_{SD_HYST}	Thermal shutdown hysteresis	Die temperature (T_J)		20		ºC
CURRENT LIMIT COMPARATOR						
I_b	Input bias current (ILIMIT)	V_{ILIMIT} = 0.5V			1	µA
V_{off}	Input voltage offset			±2.5		mV
V_{ILIMIT_DIS}	ILIMIT to disable threshold minimum voltage		2.2		2.5	V
V_{ILIMIT}	Voltage range at ILIMIT				2	V

ADVANCE INFORMATION

9 Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{GVDD} = 15V, EN = High (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{GVDD} = 15V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{blank}	Over current detection blanking on all SLx inputs, from any INHx/INLx turn on/off		400		620	ns
$t_{deglitch}$	Overcurrent detection de-glitch time		190		330	ns
t_{filter}	Input RC filter time (SLx)	V_{SLx} = 0 to 1V step, VILIMIT = 0.63V	250		450	ns
t_{filter}	Input RC filter time (ILIMIT)	V_{ILIMIT} = 1 to 0V step, V_{SLx} = 0.37V	600	1000		ns
t_{pd_OFF}	Over current detection to all GaN turn off delay	V_{ILIMIT} = 0.63V, V_{SLx} = 0 to 1V step, INx = constant			1.2	µs
t_{pd_FAULT}	Over current detection to HV_nFAULT pin report delay	V_{ILIMIT} = 0.63V, V_{SLx} = 0 to 1V step, INx =constant			1	µs
t_{F_CLR}	Fault clear time after over current detection		40		65	µs
OPERATIONAL AMPLIFIER						
V_{LINEAR}	Output voltage swing	R_L = 10k to GND	0.02		4.9	V
GBW	Gain bandwidth product	RL= 10k, G = +1		11		MHz
V_{SR_opamp}	Output voltage slew rate	RL= 10k, G = +1		15		V/µs
t_{set}	Settling time to ±1%	2-V step , G = +1, CL = 130 pF, RL = 10k		0.4		µs
A_{OL}	Open-loop voltage gain	0.04 V < VAMPOUT < 4.8 V, RL = 10 kΩ to GND		106		dB
φ_m	Phase margin	G = +1, RL = 10k		60		°
V_{COM}	Common mode input range		0		5	V
V_{OFF}	Input offset voltage error	TA = –40°C to 125°C		±1		mV
V_{DRIFT}	Drift offset	TA = –40°C to 125°C		±0.5		µV/°C
I_{bias}	Input bias current	V_{AMPIN-} = V_{AMPIN+} = 2.5V		±100		nA
I_{bias_off}	Input bias offset current	V_{AMPIN-} = V_{AMPIN+} = 2.5V		±10		nA
CMRR	Common mode rejection ratio	– 0.1 V < VCM < 5 V, TA = –40°C to 125°C		96		dB
I_{SC_opamp}	Short-circuit current			±20		mA
Z_o	Open-loop output impedance	f = 5 MHz		250		Ω
C_L	Capacitive load drive				130	pF
TEMPERATURE SENSOR						
V_T	Temperature sense element output (VTEMP) voltage	TA = 25°C		1.98		V
R_T	Load resistance on VTEMP pin		90			kΩ
C_T	Maximum load capacitance at VTEMP pin				130	pF

ADVANCE INFORMATION

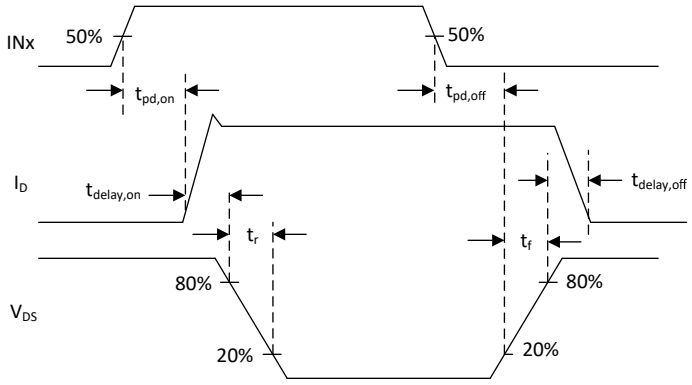


Figure 10-1. DRV7308 Turn On and Turn Off Switching Characteristics

11 Typical Characteristics

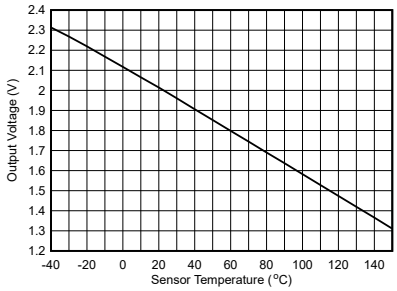


Figure 11-1. Temperature Sensor Output Across Sensor Temperature

ADVANCE INFORMATION

12 Detailed Description

12.1 Overview

The DRV7308 is a three-phase IPM, with three integrated half-H-bridge 205mΩ, 650V e-mode Gallium-Nitride (GaN) for driving three-phase BLDC/PMSM motors up to 450V DC rails. The device applications include field-oriented control (FOC), sinusoidal current control, and trapezoidal current control of BLDC motors. The device integrates pre-drivers for all GaNFETs with slew rate control of phase node voltages. The low R_{DS_ON}, slew rate control, zero reverse recovery, and low output capacitance help achieve more than 99% efficiency for a 3-phase modulated, FOC driven, 250W motor drive application, eliminating the need for heat sink.

The device integrates a suite of protections including overcurrent limit, overtemperature protection, overcurrent protection for all the GaN FETs, undervoltage protection for the GVDD and bootstrap power supplies, and adaptive dead time insertion to avoid shoot through conditions.

The device integrates a bootstrap rectifier with integrated GaN FET and a transient current limit, which eliminates the need for an external boot diode. The DRV7308 brings out all three low-side source pins of the GaN FETs to support 3-,2-, or 1-shunt current sensing. The device integrates an 11MHz, 15V/µs operational amplifier for single shunt current sensing in FOC and trapezoidal control of BLDC motors.

The low dead time helps achieve ultra quiet operations in BLDC/PMSM motors. The low propagation delay helps achieve lower distortion and accurate average current sensing.

The DRV7308 is available in a VQFN 12mm x 12mm package.

12.2 Functional Block Diagram

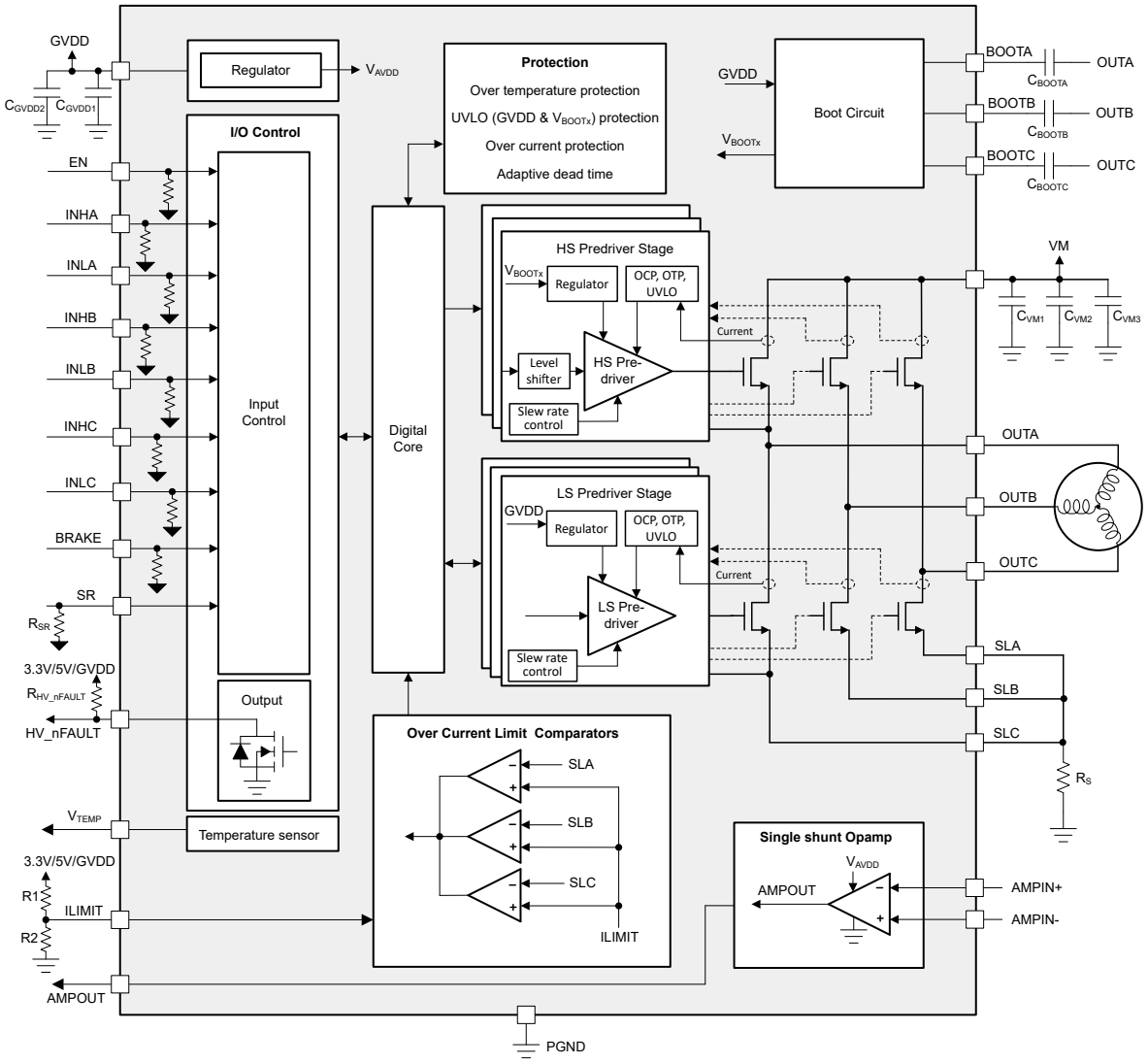


Figure 12-1. DRV7308 Block Diagram

12.3 Feature Description

Table 12-1 lists the recommended values of the external components for the driver.

Table 12-1. DRV7308 External Components

COMPONENTS	PIN1	PIN2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1µF, VM-rated capacitor
C_{VM2}	VM	PGND	X5R or X7R, 0.1µF, VM-rated capacitor (optional)
C_{VM3}	VM	PGND	≥ 10µF, VM-rated capacitor
C_{GVDD1}	GVDD	PGND	X5R or X7R, 0.1µF, GVDD-rated capacitor
C_{GVDD2}	GVDD	PGND	≥ 10µF, VM-rated capacitor
C_{BOOTA}	BOOTA	OUTA	X5R or X7R, 1µF to 220µF, GVDD-rated capacitor
C_{BOOTB}	BOOTB	OUTB	X5R or X7R, 1µF to 220µF, GVDD-rated capacitor
C_{BOOTC}	BOOTC	OUTC	X5R or X7R, 1µF to 220µF, GVDD-rated capacitor
R_{SR}	SR	PGND	Based on slew rate setting

Table 12-1. DRV7308 External Components (continued)

COMPONENTS	PIN1	PIN2	RECOMMENDED
R_{HV_nFAULT}	HV_nFAULT	3.3V/ 5.5V / GVDD	5.1kΩ, Pullup resistor
R1	ILIMIT	3.3V/ 5.5V / GVDD	Based on required ILIMIT threshold
R2	ILIMIT	PGND	Based on required ILIMIT threshold

Note

TI recommends to connect pull up on HV_nFAULT even if not used.

12.3.1 Output Stage

The DRV7308 device consists of integrated 205mΩ (one GaN FET on-state resistance) enhancement mode GaN (EGaN) FETs connected in a three-phase bridge configuration. The device integrates a pre-driver for low-side and high-side GaN FETs using an integrated bootstrap controller and rectifier using a low voltage external power supply at GVDD. An appropriately used external bootstrap capacitor offers 100% duty cycle support for a defined time.

12.3.2 Input Control Logic

The DRV7308 controls the state of the GaN FET based on the PWM input signals at the INHx and INLx pins. The device uses the BRAKE signal to apply brake to motor drive. A logic high at the BRAKE signal overrides the INHx and INLx pins and turns on all low side GaN transistors. The device enters shutoff mode (all the gate drivers and GaN FETs in off state) and ignores the status of the INHx, INLx, and BRAKE pins when a logic low on the EN pin occurs. A 20-40µs logic low pulse at the EN pin resets the device from OCP and OTP faults. The truth table for the input control logic is shown in Table 12-2.

Table 12-2. Input Control Logic

EN	BRAKE	INHx	INLx	HIGH SIDE GAN FET	LOW SIDE GAN FET	DESCRIPTION
0	X	X	X	OFF	OFF	Device in shutdown and all outputs in Hi-Z
1	1	X	X	OFF	ON	BRAKE. All low side GaN FETs are ON and all high-side GaN FETs are OFF
1	0	1	1	OFF	OFF	OUTx in Hi-Z
1	0	0	0	OFF	OFF	OUTx in Hi-Z
1	0	1	0	ON	OFF	OUTx connected to VM
1	0	0	1	OFF	ON	OUTx connected to SLx node

12.3.3 ENABLE (EN) Pin Function

When the EN pin is low, the device goes to a low-power sleep mode. In sleep mode, all GaNFETs are turned off—the Gan pre-drivers, integrated op amp, temperature sensor, GaN OCP, digital core LDO, and oscillators are all turned off. The t_{off} time must elapse after a falling edge on the EN pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the EN pin is pulled high. The t_{start} time must elapse before the device is ready for inputs.

Note

During power up and power down of the device through the EN pin, the HV_nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the HV_nFAULT pin is automatically released.

12.3.4 Temperature Sensor Output (VTEMP)

DRV7308 incorporates a temperature sensor that senses the device temperature. The output of the temperature sensor is an analog voltage that varies across temperature.

ADVANCE INFORMATION

12.3.5 Brake Function

The BRAKE pin provides a means to turn on all the low-side GaNFETs, independent of INHx and INLx pin status. The brake pin has an internal pull down. Connect the BRAKE pin to GND externally if not used. A logic high on the BRAKE pin places the device into brake by turning on all the low-side GaNFETs.

Note

Use caution while applying the BRAKE high command, as this can cause very high current driven by the motor back EMF. During BRAKE operation, the maximum current through the GaNFET must be a value that is within the operating limits of the GaNFET current and junction temperature .

12.3.6 Slew Rate Control (SR)

The DRV7308 can optionally control the slew rate of the voltage rise and fall at the OUTx pins through the configuration of the SR pin. The user can set slew rates of 5V/ns, 10V/ns, 20V/ns, or 40V/ns by configuring the SR pin. The slew rate is controlled by adjusting the gate current of GaNFETs.

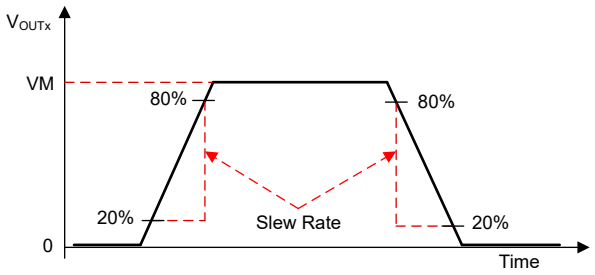


Figure 12-2. DRV7308 Slew Rate Control

Note

At higher slew rates of 20V/ns and 40V/ns, TI recommends adding a capacitor across the shunt resistors that have an RC time constant of 50ns.

Note

For PDRV7308, the high-side GaN FET slew rate is fixed at a 10V/ns setting, and the slew rate control feature is not available for high-side GaN FET. The low-side GaN FET slew rate is adjustable based on the SR pin setting.

12.3.7 Dead Time

The device is fully protected for any cross conduction of GaNFETs. In half-bridge configuration, the operation of the high-side and low-side GaNFETs are controlled to avoid any shoot-through currents by inserting dead time (t_{DEAD}). This process is implemented by using an adaptive dead time circuit that senses the gate-source voltage (VGS) of the low-side GaNFET and the phase node (OUTx) voltage of the same half-bridge.

12.3.8 Current Limit Functionaity (ILIMIT)

The DRV7308 incorporates a current limit functionality that monitors SLx voltages. DRV7308 has three integrated comparators, each monitoring voltage at SLA, SLB, and SLC pins separately. The reference voltage of all three comparators is fed externally using the ILIMIT pin. A voltage less than 2V at the ILIMIT pin enables the current limit circuitry and when the SLx voltage goes beyond the ILIMIT pin voltage, the device turns off all GaNFETs for a time t_{FCLR}. The GaNFETs turn on again after t_{FCLR} time elapses, depending on the status of input control signals. The ILIMIT functionality can be disabled by pulling up the ILIMIT pin voltage to more than V_{ILIMIT_DIS}.

The overcurrent comparator has a blacking time of t_{blank} on every edge of INHx and INLx. The comparator also has a deglitch time of $t_{deglitch}$, when the comparator output toggles from low to high.

Note

TI recommends an ILIMIT voltage of more than 0.1V to eliminate false trips due to noise. Use system-level design considerations by selecting an appropriate voltage at ILIMIT to eliminate any noise impact and select the shunt resistor value at SLx pins accordingly.

12.3.9 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

12.3.9.1 Four-Level Input Pin

Figure 12-3 shows the structure of the four-level SR pin.

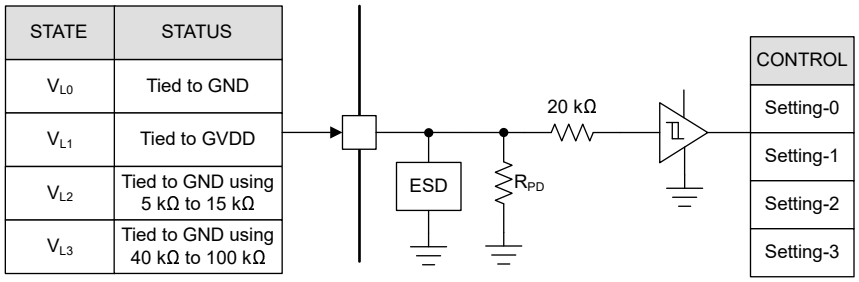


Figure 12-3. Four-Level Input Pin

12.3.9.2 Open-Drain Pin

Figure 12-4 shows the structure of the open-drain output pin, HV_nFAULT in open-drain mode. The open-drain output requires an external pullup resistor to function properly.

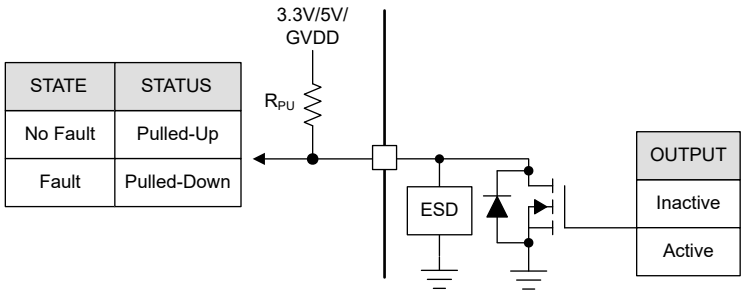


Figure 12-4. Open-Drain Pin Structure

12.3.9.3 Logic-Level Input Pin (Internal Pulldown)

Figure 12-5 shows the input structure for the logic level pins EN, INHx, INLx, ILIMIT, BRAKE. The input can be with a voltage or external resistor.

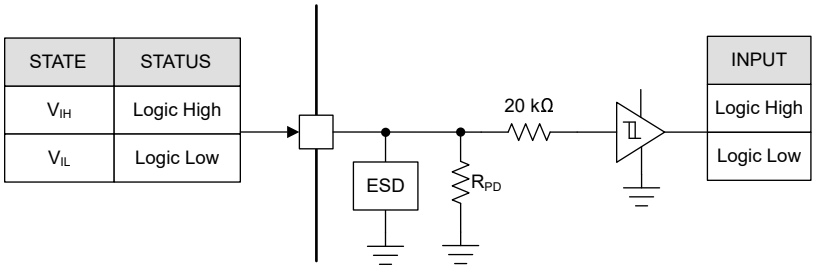


Figure 12-5. Logic-Level Input Pin Structure

ADVANCE INFORMATION

12.4 Protections

The DRV7308 integrates GaN FET overcurrent protection (GaN_OCP), overtemperature shutdown (OTSD), GVDD and bootstrap supply undervoltage protection (GVDD_UVLO and VBOOT_UVLO), and current limit (ILIMIT). Table 12-3 summarizes various faults details.

Table 12-3. Fault Action and Response

FAULT	CONDITION	REPORT	GAN BRIDGE	RECOVERY
GaN overcurrent protection (GaN_OCP)	GaN FET current > I_{OCP}	HV_nFAULT	All GaN pre-drivers turn off resulting Hi-Z (all three phases)	Latched. 20µs to 40µs toggling pulse on EN pin or GVDD power recycling
SLx overcurrent limit (OCL)	$V_{SLx} > V_{ILIMIT}$	HV_nFAULT	All GaN pre-drivers turn off resulting Hi-Z (all three phases)	Retry. After a fault clear time > t_{F_CLR}
GVDD undervoltage	$V_{GVDD} < V_{GVDD\_UV}$	HV_nFAULT	All GaN pre-drivers turn off resulting Hi-Z (all three phases)	Automatic: $V_{GVDD\_UVLO} > V_{GVDD\_UVLO\_ON}$
Boot supply undervoltage (voltage between BOOTx and OUTx pin)	$V_{BOOTx} < V_{BST\_UV}$	-	The impacted high-side GaN pre-drivers turn off. All other GaNFETs continue to operate.	Automatic: $V_{BOOTx} > V_{BST\_UV\_ON}$
Thermal shutdown (OTSD)	$T_J > T_{SD}$, for any GaNFET	HV_nFAULT	All GaN pre-drivers turns off resulting Hi-Z (all three phases)	Latched. 20µs to 40µs toggling pulse on EN pin or GVDD power recycling

12.4.1 GVDD Undervoltage Lockout

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold, all integrated GaNFETs are turned off by turning off the GaNFET pre-drivers. Normal operation starts again when the GVDD_UV condition clears. The GVDD_UV is reported by driving the HV_nFAULT pin low.

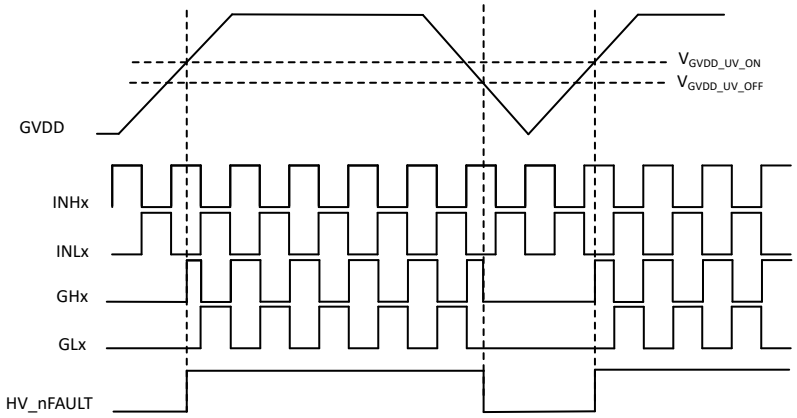


Figure 12-6. GVDD Under voltage Lockout

12.4.2 Bootstrap Undervoltage Lockout

If at any time the voltage across the bootstrap capacitor (BOOTx to OUTx voltage) pin falls lower than the V_{BST_UV} threshold, the corresponding high-side GaNFET is turned off by turning off the high-side pre-driver. All the other GaNFETs continue to work as commanded by the INx pin. Normal operation starts again at the next rising edge of INHx pulse after the BST_UV condition clears. The BOOTx undervoltage is not reported on HV_nFAULT pin.

ADVANCE INFORMATION

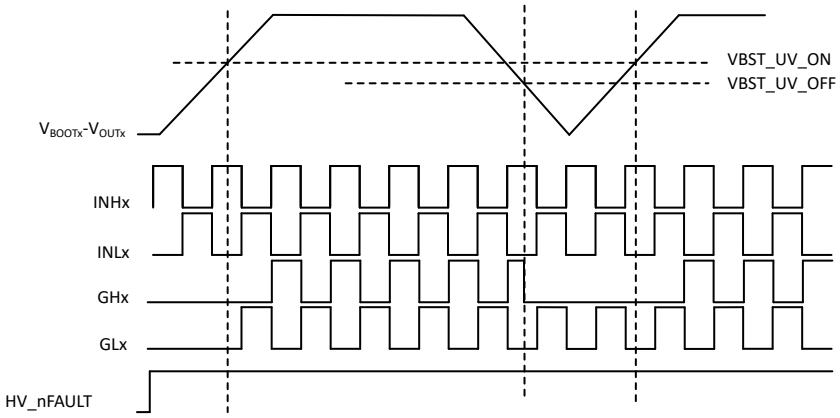


Figure 12-7. Bootstrap Undervoltage Lockout

12.4.3 Current Limit Protection

The DRV7308 integrates three comparators to protect the device, and external motor load, due to overload scenarios. DRV7308 has three integrated comparators, each monitoring voltage at SLA, SLB, and SLC pins separately. A voltage less than 2V at the ILIMIT pin enables the current limit circuitry and when the SLx voltage goes beyond the ILIMIT pin voltage, the device turns off all GaNFETs for a time t_{FCLR}. The GaNFETs turn on again after t_{FCLR} time elapses, depending on the status of input control signals. The current limit is reported by driving the HV_nFAULT pin low.

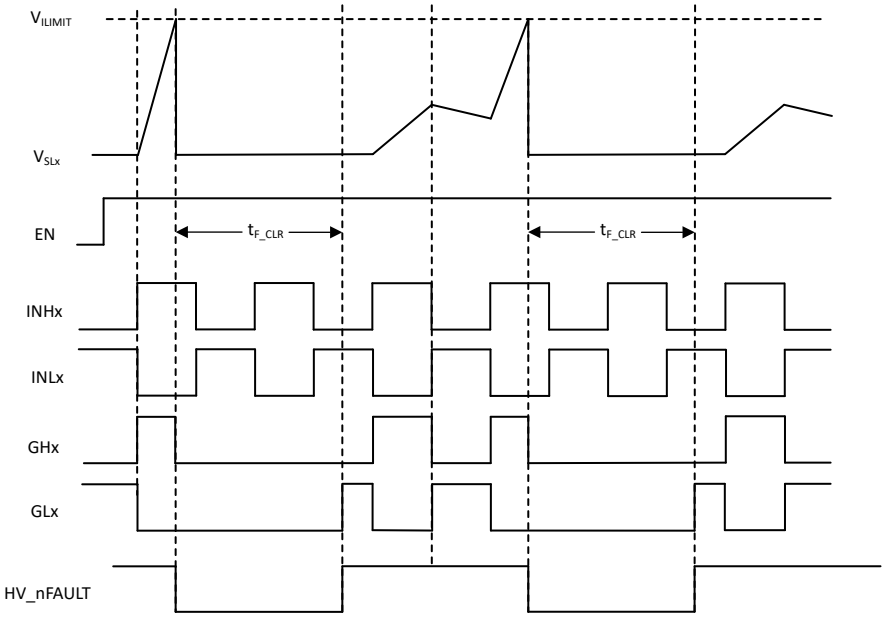


Figure 12-8. Current Limit Operation

12.4.4 GaNFET Overcurrent Protection

The DRV7308 integrates overcurrent protection for each high-side and low-side GaNFET by monitoring the VDS of the GaNFETs. If at any time, the GaNFET current goes more than I_{OCP_GaN}, all of the integrated GaNFETs are turned off by turning off the GaNFET pre-driver, and latched until cleared through a 20µs to 40µs toggling pulse on the EN pin or by a GVDD power recycling. The overcurrent event is reported by driving the HV_nFAULT pin low.

ADVANCE INFORMATION

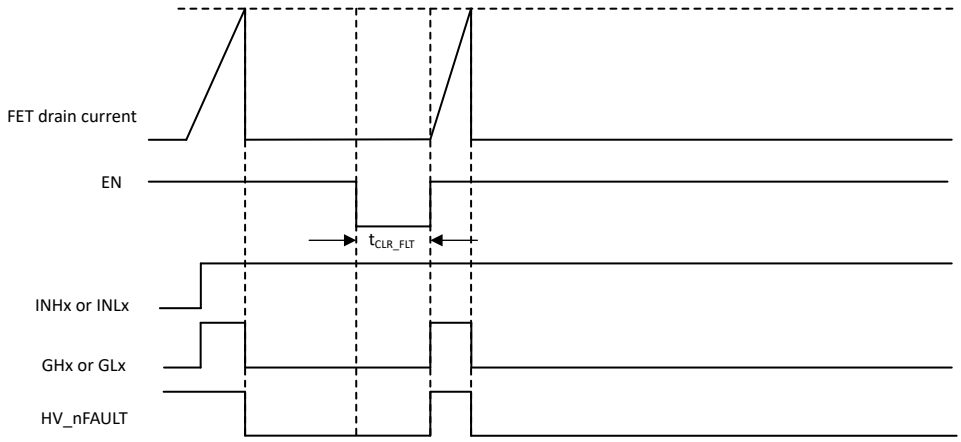


Figure 12-9. GaNFET Over current Protection

12.4.5 Thermal Shutdown (OTS)

If the die temperature near GaNFET exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the GaNFETs are disabled, and the HV_nFAULT pin is driven low. Normal operation starts again (driver operation and the HV_nFAULT pin is released) when the overtemperature condition clears and the fault is cleared through a 20µs to 40µs toggling pulse on the EN pin or by a GVDD power recycling.

ADVANCE INFORMATION

13 Layout

13.1 Layout Guidelines

The bulk capacitor must be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths must be as wide as possible and numerous vias must be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the GVDD decoupling capacitor, high frequency capacitor on VM pin to PGND, and the bootstrap capacitors must be placed close to device pins.

To minimize the power loop area, place the shunt resistors close to the device SLx pins and use copper polygon on the end of the shunt resistor, and return the current pack to the decoupling capacitor on the VM pin with a wider trace on the top layer, or through a copper polygon on the bottom layer with a sufficient number of stitching vias.

To improve thermal performance, maximize the copper planes on OUTx and PGND nets. To maximize the thermal performance, use multiple stitching vias on the OUTx pads and PGND pads and use larger copper planes on the top and bottom layers, as shown in the Figure 13-1.

The decoupling capacitor on the VM pin can be connected to any one side VM pin or to both the pins. The VM pins are internally shorted in the device and there is no need to short externally on the PCB.

13.2 Layout Example

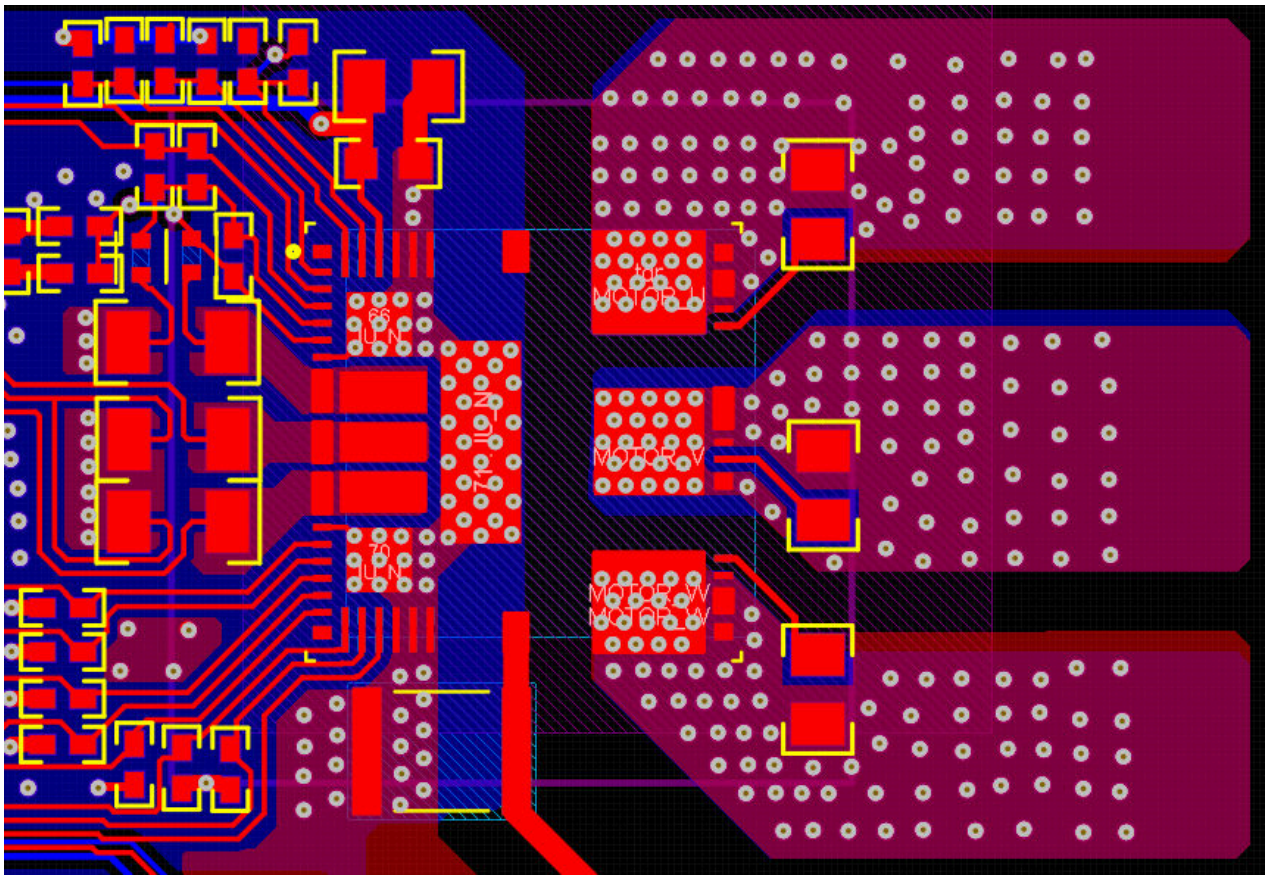


Figure 13-1. Recommended Layout for VQFN Package

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

ADVANCE INFORMATION

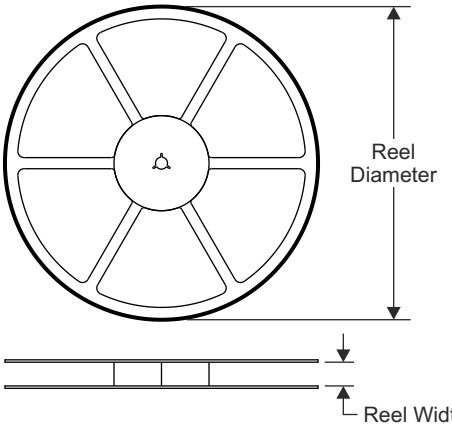
DATE	REVISION	NOTES
May 2024	*	Initial Release

15 Mechanical, Packaging, and Orderable Information

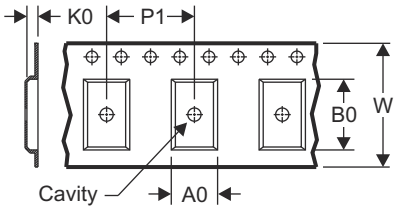
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

15.1 Tape and Reel Information

REEL DIMENSIONS

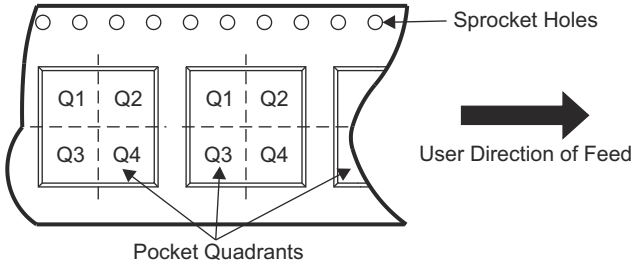


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

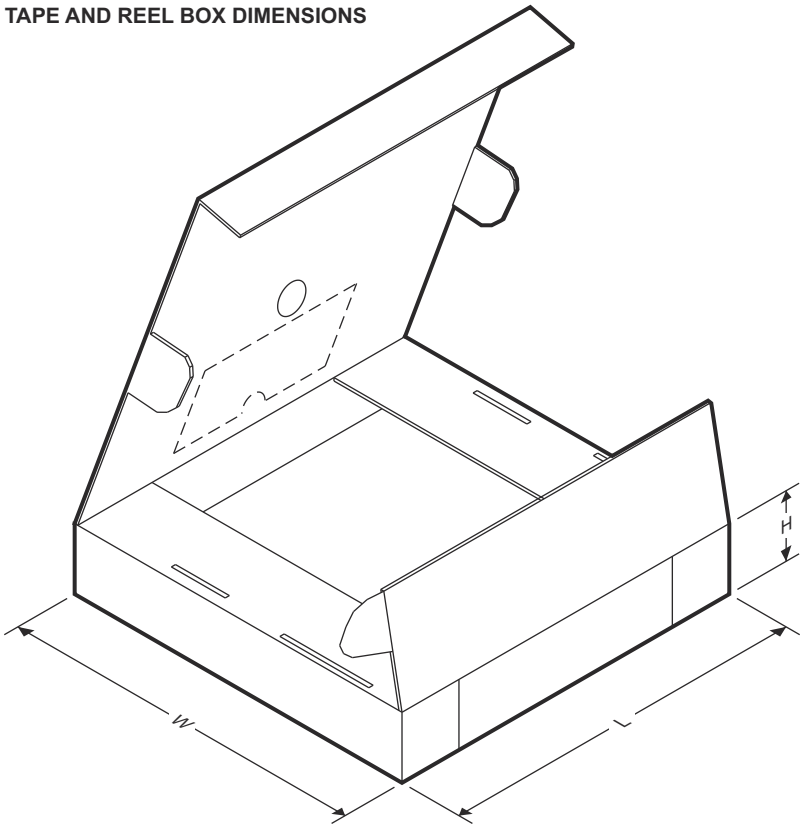
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV7308HRENR	VQFN	REN	65	2000	330.0	24.4	12.4	12.4	1.5	1.5	24.4	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV7308HRENR	VQFN	REN	65	2000	12.4	12.4	1.5

ADVANCE INFORMATION

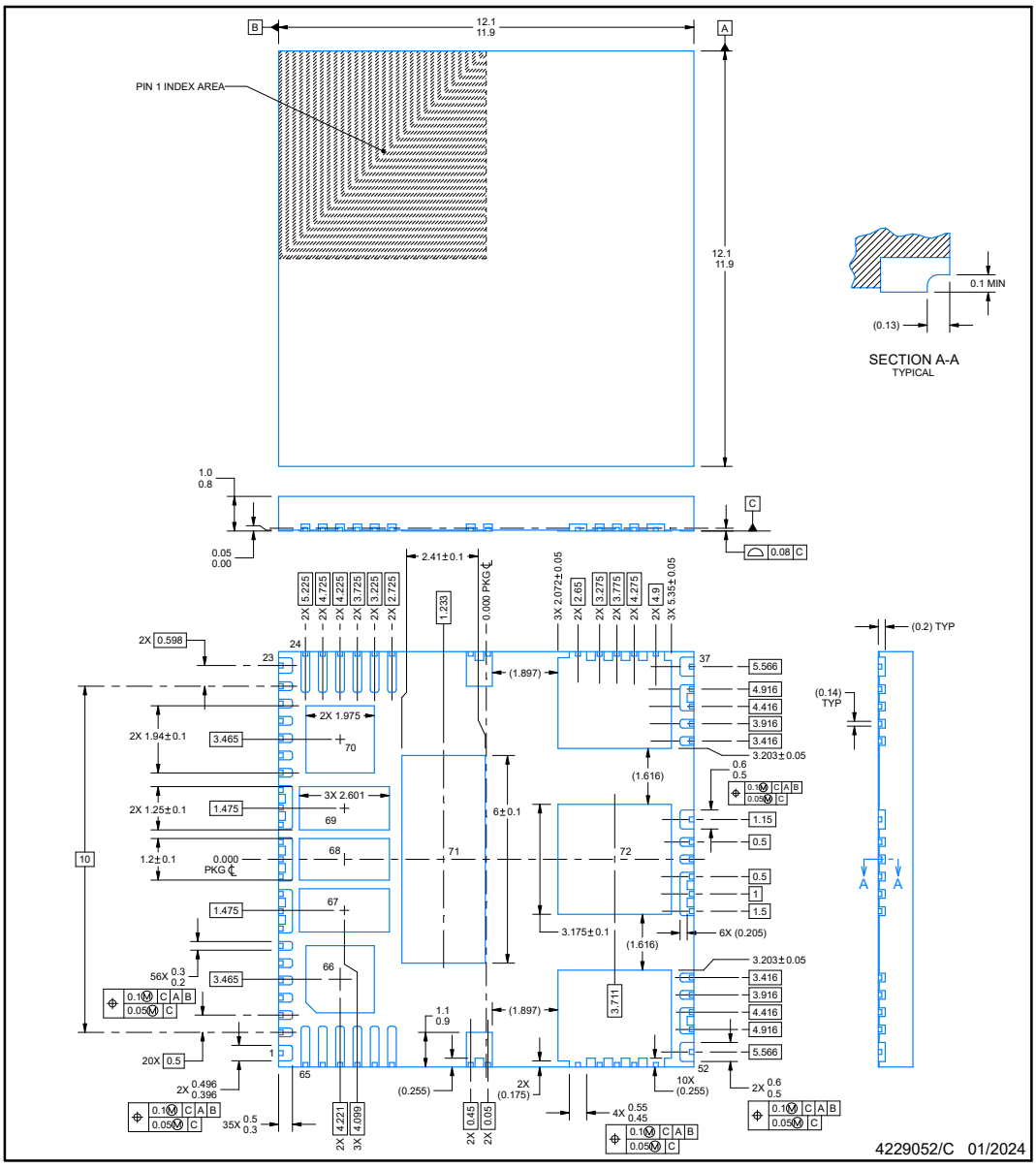
ADVANCE INFORMATION

PACKAGE OUTLINE

REN0065A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



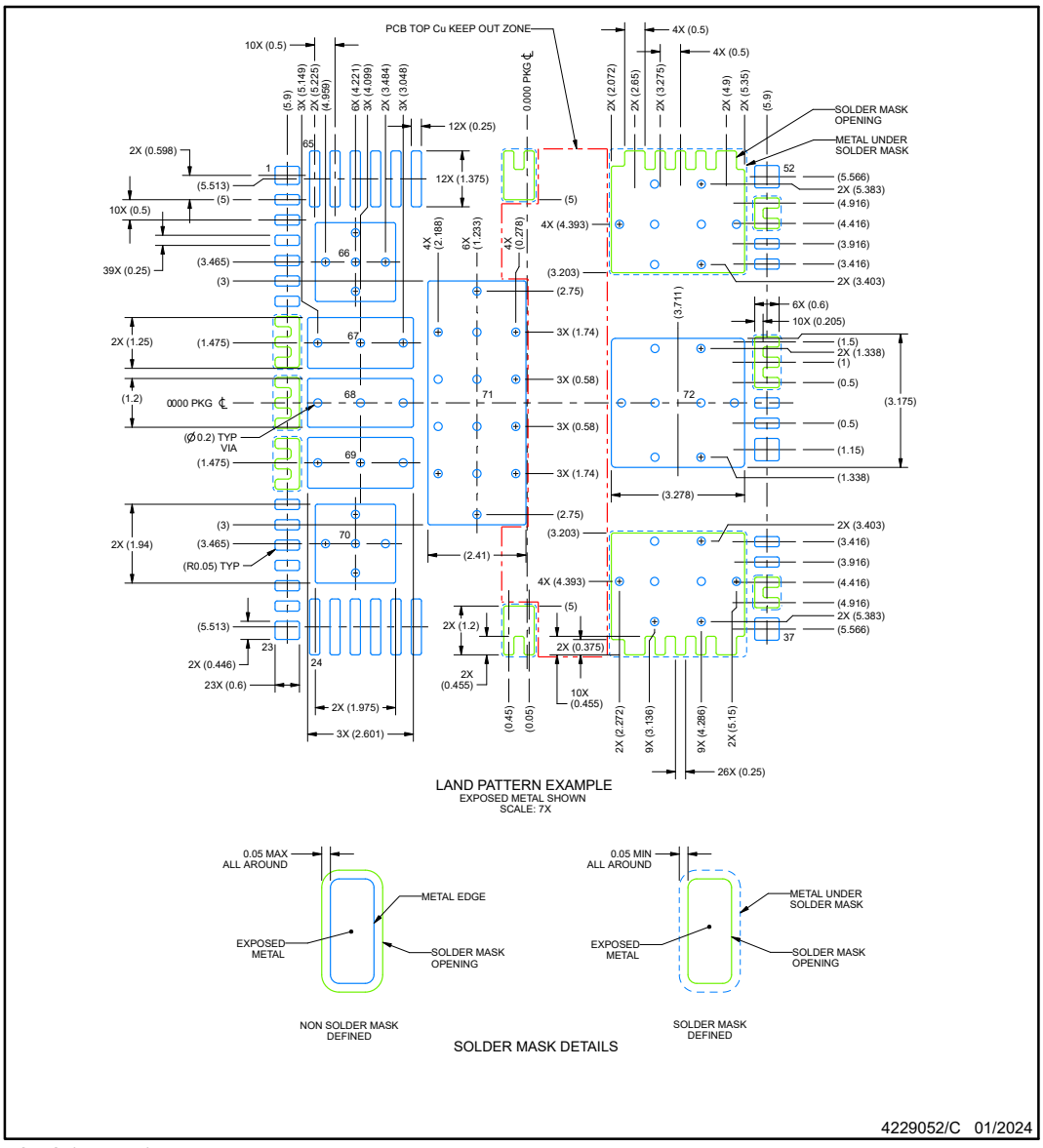
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad(s) must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REN0065A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

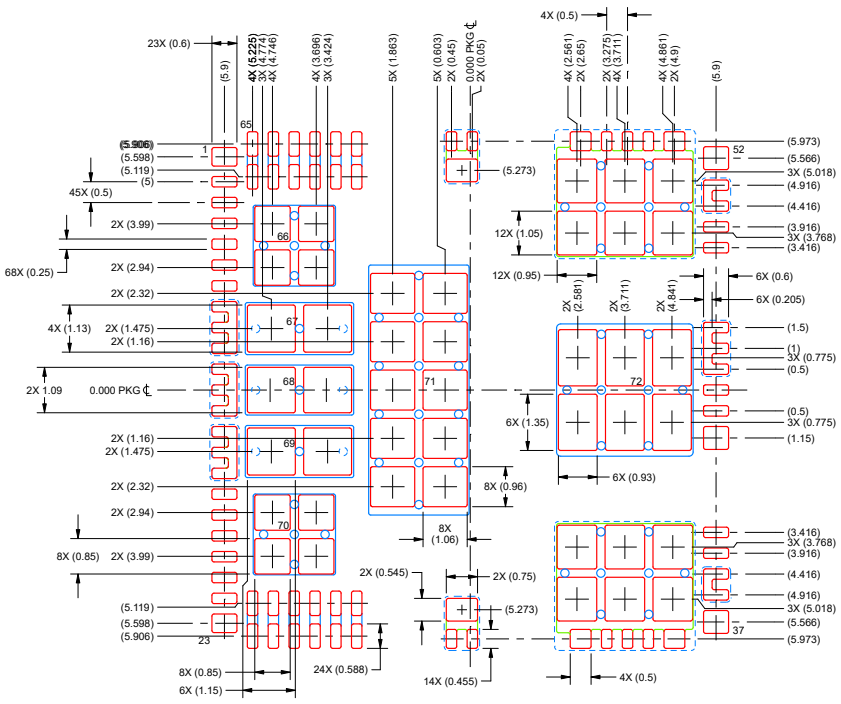
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

REN0065A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDRV7308HRENR	Active	Preproduction	VQFN (REN) | 68	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PDRV7308HRENR.A	Active	Preproduction	VQFN (REN) | 68	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PDRV7308HRENR.B	Active	Preproduction	VQFN (REN) | 68	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265