DRV3946-Q1 Dual Channel Automotive Solenoid Driver with Current Regulation, Clamping and Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation to aid ISO26262 system design is available
  - Systematic integrity up to ASIL D
  - Hardware integrity up to ASIL C
- Highly integrated solenoid driver targeted at automotive EV contactor relay and solenoid control applications
  - Integration of power supplies, current regulation, diagnostics, and safety functions
  - High-efficiency solenoid driving with configurable peak and hold current settings
  - Built-in-self-test and diagnostic functions for power supplies, interfaces, drivers, and monitors
  - Architecture for reliable operation with redundant power supplies, low-side and high-side drivers, and secondary monitoring logic
- Up to 28V (40V abs. max) operating voltage
- Integrated modified half-bridge
  - For charging, recirculation and clamping
  - Typical $R_{DS(ON)}$: 37mΩ (low-side), 57mΩ (high-side)
  - Quick Turn Off with integrated clamp circuits
  - High-side clamp with redundant low-side clamp
- Low-side load control by single wire connection
  - Allows external high-side switch for redundant shut-off
- ± 5% accurate Low and High-side current sense
  - Analog load current feedback pin (IPROPI)
- Internal control mode:
  - Closed loop PWM current regulation
  - Configurable peak time, peak and hold currents
- External control mode:
  - Vary duty cycle at fixed PWM frequency
  - Vary PWM frequency at fixed duty cycle
- 4-wire, addressable, 24-bit SPI with CRC
  - Allows multiple devices to operate on same SPI
  - All devices on shared SPI bus can receive broadcast commands
- Comprehensive protection and diagnostics:
  - Device built-in-self-test
  - Load monitoring for open/short detection
  - Sensing loss of control during driver ON and OFF
  - Forced relay open for undercurrent or undervoltage
  - Redundant pin shut-off
  - Fault notification on nFAULT pin

2 Applications

- EV Contactor relays
- Peak and hold solenoids
- On and off relays
- Proportional solenoids
- Battery Disconnect Units (BDUs)
- Battery Junction Boxes (BJBs)
- Power Distribution Boxes (PDBs)
- Active Suspension Systems
- Vehicle Control Units (VCUs)

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE (NOM)(2)
DRV3946-Q1	HTSSOP (28)	9.7mm X 4.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.

Device Information

KEY FEATURES
Can drive two solenoids with high-efficiency
Low on-resistance power stage
Integrated clamp circuits for quick turn off
Closed-loop PWM current regulation
Configurable peak and hold currents and timing parameters
Up to 20kHz PWM frequency options
Comprehensive on and off-state diagnostics
Addressable 24-bit SPI

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

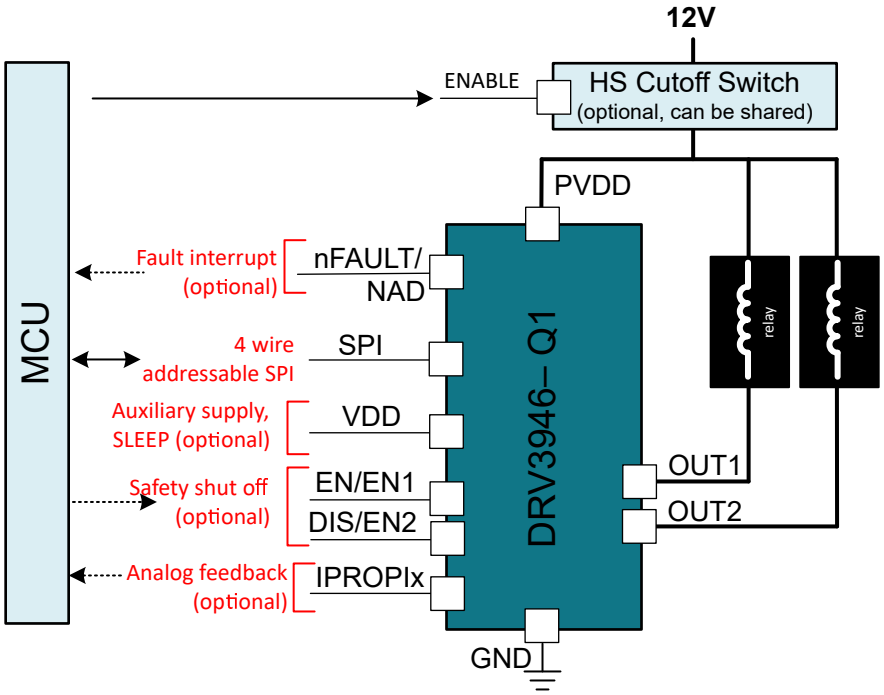
3 Description

The DRV3946-Q1 is a highly integrated solution to drive two solenoids for automotive applications such as contactor relays in EV battery management systems. It includes power supplies, current sensing and current regulation, configurable peak and hold currents and associated timings, and diagnostics and protection functions. It also incorporates several unique functions that enhance performance compared to traditional discrete solenoid drivers. These functions include integrated redundant clamp circuits to quickly discharge the load current, an addressable SPI, and modified half-bridge driver stage with low on-resistance switches.

The device controls solenoid loads through a single wire low-side connection and can pair with an external high-side switch (that can be shared) for redundant shut-off function. Integrated switches perform charging, recirculation and clamping. The device supports internal and external current control modes. The PWM frequency is configurable, with added low frequency dithering using automatic pseudo random frequencies generation and wave shaping. Internal PWM current control loop leads to reduced software development, since MCU current control loop is not needed. The DRV3946-Q1 supports flexible current control parameters to support wide range of solenoid types. Configurable peak and hold current and corresponding timing parameters allow system level power saving.

The DRV3946-Q1 is targeted to be functional safety-compliant, with ASIL-C rated functional safety goal for relay control and avoiding unintended operation. The device supports comprehensive protection and diagnostic features, such as continuous monitoring of load for open and short detection, on and off-state diagnostics, voltage monitors, short protection and high voltage rated IOs.

An addressable SPI allows multiple devices to be controlled on a shared SPI bus. In addition to reducing required MCU resources, the addressable SPI incorporates a broadcast command structure that can enable all devices on the shared addressed bus to take certain actions simultaneously. The SPI incorporates multiple robustness functions including a CRC, address readback capability, and various bus fault detection mechanisms.



Simplified Schematic

Copyright © 2026 Texas Instruments Incorporated

Table of Contents

Copyright © 2026 Texas Instruments Incorporated

4 Pin Configuration and Functions

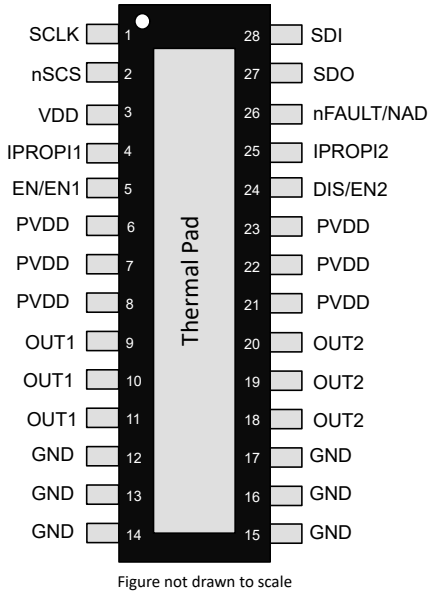


Figure not drawn to scale

Figure 4-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View

Table 4-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
SCLK	1	I	Digital	Serial clock input. Serial data is captured on the falling edge and shifted out on rising edge. Internal pulldown resistor to GND.
nSCS	2	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor to V5_S.
VDD	3	I	Power	Device low voltage and auxilary power supply.
IPROPI1(1)	4	O	Analog	Analog current feedback for output 1
EN/EN1(1)	5	I	Digital	Independent PIN input for shutting off output 1 or for shutting off both outputs
PVDD	6-8, 21-23	I	Power	Device primary power supply
OUT1(1)	9-11	O	Power	Driver output 1
GND	12-17	I	Power	Device ground. Connect to system ground.
OUT2(1)	18-20	O	Power	Driver output 2
DIS/EN2(1)	24	I	Digital	Independent PIN input for shutting off output 2 or for shutting off both outputs
IPROPI2(1)	25	O	Analog	Analog current feedback for output 2
nFAULT/NAD	26	O	Digital	Sets device address. Open-drain output to indicate fault during normal operation.
SDO	27	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
SDI	28	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor to GND.
TPAD	n/a	n/a	n/a	Device thermal pad. Connect to GND.

(1) Unused OUTx pin can be connected to PVDD, unused IPROPIx pin can be connected to GND, and unused EN/EN1 and DIS/EN2 pins can be connected to VDD or GND as needed.

Copyright © 2026 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	–0.3 (3)	40	V
Power supply transient voltage ramp	PVDD		2	V/µs
Low voltage supply pin	VDD	–0.3	40	V
Power supply transient voltage ramp	VDD		2	V/µs
Output pin voltage (with respect to GND)	OUT1, OUT2	Limited by internal clamps		V
Output pin voltage (with respect to PVDD)	OUT1, OUT2	Limited by internal clamps		V
Output pin current	OUT1, OUT2	Internally limited(2)		A
Inductive kick back energy on OUTx (current into pin)	OUT1, OUT2		250 (4)	mJ
Controller input pins voltage	ENABLE, DISABLE	–0.3	40	V
Controller output pins voltage	IPROPIx	–0.3	5.5	V
nFAULT pin voltage	nFAULT/NAD	-0.3	40	V
SPI input pin voltage	SDI, nSCS, SCLK	–0.3	40	V
SPI output pin voltage	SDO	–0.3	40	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Limited by the over current and over temperature protection functions of the device
(3) Can support negative transients up to 10 msec when protected with an external diode to limit PVDD pin current < 1 A
(4) Measured at T_{AMB} = 85 °C, Load current = 3 A, Single pulse.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	PVDD, OUT1, OUT2, GND	±4000	V
			All other pins	±2000	
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Power supply voltage	PVDD	4.5	13.5	35(1)	V
V_{VDD}	Logic supply voltage	VDD	4.5		5.5	V
V_{LOGIC}	Controller pins voltage	ENABLE, DISABLE, IPROPI1, IPROPI2, nFAULT/NAD	0		5.5	V
V_{SPI_IOS}	SPI pin voltage	SDI, SDO, nSCS, SCLK	0		5.5	V
T_A	Operating ambient temperature		–40		125	°C

Copyright © 2026 Texas Instruments Incorporated

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–40		150	°C

(1) The over current protection function does not support short inductance < 1 µH above 28 V supply voltage

5.4 Thermal Information

THERMAL METRIC(1)		HTSSOP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	13.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVDD and VDD Power Supplies						
V_{PVDD_REV}	Supply pin voltage during reverse current	I_{PVDD} = - 1 A, T_J = 25°C	-3		-0.1	V
		I_{PVDD} = - 1 A, T_J = 150°C	-2.8		-0.15	V
I_{PVDD_STBY}	PVDD current in STANDBY state	Drivers Hi-Z (using SPI and PINs), Off-state diagnostics enabled		7	12	mA
I_{VDD_STBY}	VDD current in STANDBY state	Drivers Hi-Z, PVDD = 0V (no SPI activity)		4.3	7.5	mA
I_{VDD_PEAK}	Peak VDD current in case of SDO bus contension (data collision) for one SCLK cycle	PVDD = 13.5 V		17	30	mA
t_{READY}	Power up time from POR till device is ready to accept commands	PVDD supply power up ramp			1	ms
I_{PVDD_VDD}	Leakage current from PVDD to VDD, measured at VDD pin	PVDD = 13.5 V, VDD = 0 V		5	12	µA
	Leakage current from PVDD to VDD, measured at PVDD pin	PVDD = 0 V, VDD = 5 V	-5			µA
I_{PVDD_GND}	Leakage current from PVDD, OUTx to GND	PVDD = OUTx = 1 V, VDD = 5 V in INIT1 state		50	250	µA
Reset (nPOR)						
$V_{PVDD\_RST\_FALL}$	PVDD falling level when reset occurs, with VDD in Hi-Z	VDD = 0V	2.6		3.1	V
$V_{PVDD\_RST\_RISE}$	PVDD rising level when reset is released, with VDD in Hi-Z	VDD = 0V	3.1		3.8	V
$V_{PVDD\_RST\_HYST}$	V5_S reset hysteresis with respect to PVDD, with VDD in HiZ	VDD = 0V		0.6		V
$V_{VDD\_RST\_FALL}$	VDD falling level when reset occurs, with VDD in Hi-Z	PVDD = 0V	2.6		3.1	V
$V_{VDD\_RST\_RISE}$	VDD rising level when reset is released, with VDD in Hi-Z	PVDD = 0V	3.1		3.8	V
$V_{VDD\_RST\_HYST}$	V5_S reset hysteresis with respect to VDD, with PVDD in HiZ	PVDD = 0V		0.6		V
PVDD monitor						

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PVDD\_UV\_BIAS\_FALL}$	PVDD BIAS Under voltage threshold when falling (LS 100% duty cycle)	VDD > 4.5 V	2.6		3.1	V
$V_{PVDD\_UV\_BIAS\_RISE}$	PVDD BIAS Under voltage threshold when rising	VDD > 4.5 V	2.8		3.3	V
$V_{PVDD\_UV\_BIAS\_HYST}$	PVDD BIAS Under voltage hysteresis	VDD > 4.5 V		0.21		V
$t_{PVDD5R\_UV\_BIAS}$	PVDD BIAS UV deglitch time		15		19	µs
$V_{PVDD\_UV\_FALL}$	PVDD Under voltage trigger threshold when falling		4.3	4.54	4.8	V
$V_{PVDD\_UV\_RISE}$	PVDD Under voltage recovery threshold when rising		4.5	4.75	5	V
$V_{PVDD\_UV\_HYST}$	PVDD UV hysteresis			0.21		V
$t_{PVDD\_UV\_W}$	PVDD UV deglitch time for warning		15		19	µs
t_{PVDD_UV}	PVDD UV deglitch time	PVDD_UV_FLTR = 0x0	240		315	µs
		PVDD_UV_FLTR = 0x1	475		600	µs
		PVDD_UV_FLTR = 0x2	700		890	µs
		PVDD_UV_FLTR = 0x3	940		1170	µs
$V_{PVDD\_OV\_RISE}$	PVDD Over voltage trigger threshold when rising		31.2	33	34.8	V
$V_{PVDD\_OV\_FALL}$	PVDD Over voltage recovery threshold when falling		30.2	31.9	33.8	V
$V_{PVDD\_OV\_HYST}$	PVDD Over voltage hysteresis			1.1		V
t_{PVDD_OV}	PVDD OV deglitch time	PVDD_OV_FLTR = 0x0	240		315	µs
		PVDD_OV_FLTR = 0x1	475		600	µs
		PVDD_OV_FLTR = 0x2	700		890	µs
		PVDD_OV_FLTR = 0x3	940		1170	µs
$V_{PVDD\_OV\_W\_RISE}$	PVDD Over voltage warning threshold when rising		19	19.7	20.5	V
$V_{PVDD\_OV\_W\_FALL}$	PVDD Over voltage warning threshold when falling		18.2	18.8	19.4	V
$V_{PVDD\_OV\_W\_HYST}$	PVDD Over voltage hysteresis			0.9		V
$t_{PVDD\_OV\_W}$	PVDD OV deglitch time for warning		15		19	µs
VDD monitor						
$V_{VDD\_UV\_FALL}$	VDD Under voltage trigger threshold when falling		4	4.2	4.4	V
$V_{VDD\_UV\_RISE}$	VDD Under voltage recovery threshold when rising		4.1	4.3	4.5	V
$V_{VDD\_UV\_HYST}$	VDD UV hysteresis			0.105		V
$t_{VDD\_UV\_W}$	VDD UV deglitch time for warning		15		19	µs
t_{VDD_UV}	VDD UV deglitch time	VDD_UV_FLTR = 0x0	240		315	µs
		VDD_UV_FLTR = 0x1	475		600	µs
		VDD_UV_FLTR = 0x2	700		890	µs
		VDD_UV_FLTR = 0x3	940		1170	µs
$V_{VDD\_OV\_RISE}$	VDD Over voltage trigger threshold when rising		5.9	6.2	6.5	V

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDD\_OV\_FALL}$	VDD Over voltage recovery threshold when falling		5.5	5.8	6.1	V
$V_{VDD\_OV\_HYST}$	VDD Over voltage hysteresis			0.4		V
$t_{VDD\_OV\_W}$	VDD OV deglitch time for warning(1)		15		19	µs
t_{VDD_OV}	VDD OV deglitch time	VDD_OV_FLTR = 0x0	240		315	µs
		VDD_OV_FLTR = 0x1	475		600	µs
		VDD_OV_FLTR = 0x2	700		890	µs
		VDD_OV_FLTR = 0x3	940		1170	µs
EN/EN1 and DIS/EN2 pins						
V_{IL}	Input logic low voltage				0.7	V
V_{IH}	Input logic high voltage		1.5			V
V_{IHYS}	Input hysteresis pin			0.11		V
R_{PD_ENABLE}	Input pull-down resistance on ENABLE pin to GND	Measured at min VIH level	100		200	kΩ
$R_{PD\_DISABLE}$	Input pull-down resistance on DISABLE pin to GND	Measured at min VIH level	100		200	kΩ
t_{FLTR_PIN}	Delay due to filtering at pin - falling edge		1		2.2	µs
t_{FLTR_PIN}	Delay due to filtering at pin - rising edge		0.15		0.6	µs
$t_{PIN\_TURNON\_DLY}$	Pin turn on delay	PIN_TURNON_DLYx = 0x0		0		ms
		PIN_TURNON_DLYx = 0x1	3.5		4.5	ms
		PIN_TURNON_DLYx = 0x2	7		9	ms
		PIN_TURNON_DLYx = 0x3	14		18	ms
		PIN_TURNON_DLYx = 0x4	21		27	ms
		PIN_TURNON_DLYx = 0x5	28		36	ms
		PIN_TURNON_DLYx = 0x6	35		45	ms
		PIN_TURNON_DLYx = 0x7	49		63	ms
$t_{PIN\_TURNOFF\_DLY}$	Pin turn off delay	PIN_TURNOFF_DLYx = 0x0		0		ms
		PIN_TURNOFF_DLYx = 0x1	3.5		4.5	ms
		PIN_TURNOFF_DLYx = 0x2	7		9	ms
		PIN_TURNOFF_DLYx = 0x3	14		18	ms
		PIN_TURNOFF_DLYx = 0x4	21		27	ms
		PIN_TURNOFF_DLYx = 0x5	28		36	ms
		PIN_TURNOFF_DLYx = 0x6	35		45	ms
		PIN_TURNOFF_DLYx = 0x7	49		63	ms
SPI I/Os						
R_{PU_nSCS}	Input pull-up resistance on nSCS to VDD	Measured at min VIH level	100		200	kΩ
R_{PD_SDI}	Input pull-down resistance on SDI to GND	Measured at max VIL level	200		400	kΩ
R_{PD_SCLK}	Input pull-down resistance on SCLK to GND	Measured at min VIH level	200		400	kΩ
V_{IL_SPI}	Input logic low voltage	SDI, nSCS, SCLK pins			0.7	V
V_{IH_SPI}	Input logic high voltage	SDI, nSCS, SCLK pins	1.5			V
V_{IHYS_SPI}	Input hysteresis	SDI, nSCS, SCLK pins		0.11		V
R_{PU_SDO}	Input pull-up resistance on SDO to VDD	Measured at max VIL level	500		1050	kΩ
V_{OL_SDO}	SDO Output logic low voltage	0.5 mA sink into the pin			0.3	V

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH_SDO}	SDO Output logic high voltage	0.5 mA source from the pin	VDD – 0.3			V
I_{OH_SDO}	SDO Output logic high current	Measured at 1V on SDO		15	35	mA
nFAULT/NAD pin						
R_{LVL_OORL}	Resistor to VDD - below minimum value				2.8	kΩ
R_{LVL1}	Resistor to VDD for NAD assignment = 2'b00	+/- 10% resistors	5.04	5.6	6.16	kΩ
R_{LVL2}	Resistor to VDD for NAD assignment = 2'b01	+/- 10% resistors	10.8	12	13.2	kΩ
R_{LVL3}	Resistor to VDD for NAD assignment = 2'b10	+/- 10% resistors	24.3	27	29.7	kΩ
R_{LVL4}	Resistor to VDD for NAD assignment = 2'b11	+/- 10% resistors	50.4	56	61.6	kΩ
R_{LVL_OORH}	Resistor to VDD - exceeds maximum value		100			kΩ
I_{nFAULT_PD}	Pull down current on nFAULT pin to indicate fault	V(nFAULT) = 0.3 V	5			mA
V_{IL_nFAULT}	Input logic low voltage for nFAULT feedback buffer	nFAULT pin			0.5	V
V_{IH_nFAULT}	Input logic high voltage for nFAULT feedback buffer	nFAULT pin	1.3			V
V_{IHYS_nFAULT}	Input hysteresis for nFAULT feedback buffer	nFAULT pin		0.11		V
t_{nFAULT}	Deglitch time for nFAULT feedback	nFAULT pin	15		19	µs
Output driver						
R_{ON_LS}	Low-side MOSFET on resistance	V_{VM} = 13.5 V, I_O = 3 A, T_J = 25°C		37	45	mΩ
		V_{VM} = 13.5 V, I_O = 3 A, T_J = 150°C		57	75	mΩ
R_{ON_RECIRC}	Total back to back High-side MOSFET on resistance	V_{VM} = 13.5 V, I_O = 3 A, T_J = 25°C		57	75	mΩ
		V_{VM} = 13.5 V, I_O = 3 A, T_J = 150°C		87	120	mΩ
V_{CLAMP_HS}	High-side clamp with respect to PVDD	I_{OUTx} = 3 A (Into pin), PVDD < 15 V	PVDD + 27	PVDD + 32	PVDD + 36	V
		I_{OUTx} = 3 A (Into pin), PVDD = 18 V	PVDD + 23.5	PVDD + 27	PVDD + 32	V
		I_{OUTx} = 3 A (Into pin), PVDD = 27 V	PVDD + 14	PVDD + 19	PVDD + 23	V
		I_{OUTx} = 3 A (Into pin), PVDD = 35 V	PVDD + 6.5	PVDD + 10	PVDD + 15	V
$V_{CLAMP\_LS\_ACTIVE}$	Low-side clamp (redundant) with respect to GND	I_{OUTx} = 3 A (Into pin), powered state, PVDD ≥ OV level	41.5	45	49.5	V
		I_{OUTx} = 3 A (Into pin), powered state, PVDD < OV level	VCLAMP_HS + 1	VCLAMP_HS + 2.5	VCLAMP_HS + 4	V
$V_{CLAMP\_LS\_PASSIVE}$	Low-side clamp (redundant) with respect to GND	I_{OUTx} = 3 A (Into pin), unpowered state	28	30	32	V
V_{SD_LS}	Body diode forward voltage	I_{OUTx} = -3 A (Out of pin)	-1.2		–0.5	V
I_{OCP_HS}	Over current protection threshold for HS FET		11		22	A
I_{OCP_LS}	Over current protection threshold for LS FET		11		22	A
t_{OCP}	Overcurrent protection deglitch time	OCP_FLTR = 0x0	3.8		4.7	µs
		OCP_FLTR = 0x1, PVDD < $V_{PVDD\_OV\_W\_RISE}$	7.1		9.2	µs

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current sense						
A_{IPROPI}	Current scaling factor (LS)	current range: 0.8 A to 6 A	19000	20000	21000	A/A
A_{IPROPI_LOW}	Current scaling factor (LS)	current range: 0.2 A to 0.8 A	18500	20000	21500	A/A
$Offset_{IPROPI}$	Offset current on IPROPI at zero load current (LS)	Measured in ACTIVE state with no load current			1	µA
A_{IPROPI_MATCH}	Current scaling factor matching (HS wrt LS)	current range: 0.8 A to 3 A	-8		8	%
A_{IPROPI_HS}	Current scaling factor (HS)	current range: 0.8 A to 3 A	18800	20000	21200	A/A
$A_{IPROPI\_LOW\_HS}$	Current scaling factor (HS)	current range: 0.2 A to 0.8 A	18000	20000	22000	A/A
$Offset_{IPROPI\_HS}$	Offset current on IPROPI at zero load current (High side sense)	Measured in ACTIVE state with no load current			1	µA
Internal current regulation						
V_{ITRIP_LVL}	Voltage threshold on IPROPIx pin to trigger current regulation	CHx_HC = 0x00	0.18	0.195	0.21	V
		CHx_HC = 0x01	0.19	0.205	0.22	V
		CHx_HC = 0x02	0.205	0.22	0.235	V
		CHx_HC = 0x04	0.225	0.24	0.255	V
		CHx_HC = 0x08	0.27	0.285	0.3	V
		CHx_HC = 0x10	0.36	0.375	0.39	V
		CHx_HC = 0x20	0.53	0.55	0.57	V
		CHx_HC = 0x40	0.85	0.9	0.95	V
		CHx_HC = 0x80	1.55	1.61	1.67	V
		CHx_HC = 0xFF	2.9	3.02	3.14	V
V_{QTO_START}	Voltage threshold with respect to PVDD on OUTx pin to detect QTO start	Load = 15 mH, 1.5Ω, 0.3A	1.75	2.00	2.25	V
V_{QTO_END}	Voltage threshold with respect to PVDD on OUTx pin to detect QTO end	Load = 15 mH, 1.5Ω, 0.3A	1.65	1.9	2.15	V
t_{QTO_DELAY}	Delay time for QTO start/stop detection(1)	Load = 15 mH, 1.5Ω, 0.3A		10		µs
t_{QTO_DETECT}	Deglitch time for QTO start/stop detection	Load = 15 mH, 1.5Ω, 0.3A	15		19	µs
$V_{IRIPPLE\_LVLH}$	Upper voltage threshold on internal IPROPI redundant node to trigger current ripple regulation, normalized to HC	CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x0	13.8	15	16.2	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x1	18.8	20	21.2	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x2	23.8	25	26.2	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x4	33.8	35	36.2	%
$V_{IRIPPLE\_LVLL}$	Lower voltage threshold on internal IPROPI redundant node to trigger current ripple regulation, normalized to HC	CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x0	-16.2	-15	-13.8	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x1	-21.2	-20	-18.8	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x2	-26.2	-25	-23.8	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x4	-36.2	-35	-33.8	%

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UCLO_LVL}	Voltage threshold on IPROPIx pin to trigger Under Current Lock Out (UCLO), normalized to HC	CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x4, CHx_UCLO_THRS = 0x0	–53.6	–52.2	–50.8	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x4, CHx_UCLO_THRS = 0x1	–50.3	–48.9	–47.5	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x4, CHx_UCLO_THRS = 0x2	–47.1	–45.7	–44.3	%
		CHx_HC = 0x80, CHx_RIPPLE_THRS = 0x4, CHx_UCLO_THRS = 0x3	–43.9	–42.5	–41.1	%
fc_{PWM}	PWM center frequency	CHx_fC_PWM = 0x04	4.3	5	5.7	KHz
		CHx_fC_PWM = 0x0B	8.6	10	11.4	KHz
		CHx_fC_PWM = 0x1F	17.2	20	22.8	KHz
fc_{PWM}	PWM frequency spread around center frequency	CHx_fC_PWM = 0x1F, CHx_fSS_SEL = 0x3		27		%
t_{PC}	Peak current timer	CHx_PT = 0x0	14		18	ms
		CHx_PT = 0x1	21		27	ms
		CHx_PT = 0x2	28		36	ms
		CHx_PT = 0x3	35		45	ms
		CHx_PT = 0x4	42		54	ms
		CHx_PT = 0x5	49		63	ms
		CHx_PT = 0x6	56		72	ms
		CHx_PT = 0x7	63		81	ms
		CHx_PT = 0x8	70		90	ms
		CHx_PT = 0x9	77		99	ms
		CHx_PT = 0xA	84		108	ms
		CHx_PT = 0xB	91		117	ms
		CHx_PT = 0xC	98		126	ms
		CHx_PT = 0xD	105		135	ms
		CHx_PT = 0xE	112		144	ms
		CHx_PT = 0xF	224		288	ms
Switching parameters						
SR_{LSOFF}	Output voltage rise time, 10% - 90%, , VM = 13.5 V, Load = 15 mH, 1.5Ω	SR = 0x0	1.3	2.9	4.5	V/µs
		SR = 0x1	2.2	4.5	6.8	V/µs
		SR = 0x2	4	7.4	10.8	V/µs
		SR = 0x3	6.2	12.6	19	V/µs
		SR = 0x4	8.1	16.3	24.5	V/µs
		SR = 0x5	13	24.1	35.2	V/µs
		SR = 0x6	16.5	31.2	45.9	V/µs
		SR = 0x7	22.2	41.8	61.4	V/µs
SR_{LSON}	Output voltage fall time, 90% - 10%, VM = 13.5 V, Load = 15 mH, 1.5Ω	SR = 0x0	1.3	2.9	4.5	V/µs
		SR = 0x1	2.2	4.5	6.8	V/µs
		SR = 0x2	4	7.4	10.8	V/µs
		SR = 0x3	6.2	12.6	19	V/µs
		SR = 0x4	8.1	16.3	24.5	V/µs
		SR = 0x5	13	24.1	35.2	V/µs
		SR = 0x6	16.5	31.2	45.9	V/µs
		SR = 0x7	22.2	41.8	61.4	V/µs

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON_MIN}	Minimum LS ON charge time (PWM = 1), , VM = 13.5V, Load = 15 mH, 1.5Ω, 3A	SR = 0x0	6	8.7	11.8	µs
		SR = 0x1	5.2	7.1	9.4	µs
		SR = 0x2	4.6	6	7.3	µs
		SR = 0x3	4.4	5.7	6.8	µs
		SR = 0x4	4.1	5.2	6.3	µs
		SR = 0x5	3.7	4.7	5.7	µs
		SR = 0x6	3.5	4.4	5.3	µs
		SR = 0x7	3.3	4.2	5.1	µs
t_{RECIRC_MIN}	Minimum recirculation time (PWM = 0), VM = 13.5V, Load = 15 mH, 1.5Ω, 3A	SR = 0x0	6.6	9.8	12.8	µs
		SR = 0x1	5.7	8.1	10.6	µs
		SR = 0x2	4.9	6.8	8.7	µs
		SR = 0x3	4.6	6.4	8	µs
		SR = 0x4	4.3	5.8	7.4	µs
		SR = 0x5	3.9	5.3	6.8	µs
		SR = 0x6	3.6	5	6.4	µs
		SR = 0x7	3.5	4.8	6.1	µs
Retry wait						
t_{RETRY_WAIT}	Forced retry delay time	RETRY_WAIT_SEL = 0x0	7		9	ms
		RETRY_WAIT_SEL = 0x1	14		18	ms
		RETRY_WAIT_SEL = 0x2	28		36	ms
		RETRY_WAIT_SEL = 0x3	56		72	ms
		RETRY_WAIT_SEL = 0x4	112		144	ms
		RETRY_WAIT_SEL = 0x5	224		288	ms
		RETRY_WAIT_SEL = 0x6	336		432	ms
		RETRY_WAIT_SEL = 0x7	448		576	ms
On-state diagnostics						
N_{PWM_FAULT}	Number of PWM fault cycles to detect current regulation abnormality including UCLO	PWM_FAULT_FLTR = 0x0		8		cycles
		PWM_FAULT_FLTR = 0x1		16		cycles
		PWM_FAULT_FLTR = 0x2		32		cycles
		PWM_FAULT_FLTR = 0x3		48		cycles
		PWM_FAULT_FLTR = 0x4		64		cycles
		PWM_FAULT_FLTR = 0x5		128		cycles
		PWM_FAULT_FLTR = 0x6		192		cycles
		PWM_FAULT_FLTR = 0x7		256		cycles
t_{PRT_MIN}	Peak current minimum ramp time threshold	PRT_MIN_THRSx = 0x0	28		48	µs
		PRT_MIN_THRSx = 0x1	56		84	µs
		PRT_MIN_THRSx = 0x2	112		156	µs
		PRT_MIN_THRSx = 0x3	224		300	µs
t_{HRT_MIN}	Hold current minimum ramp time threshold	HRT_MIN_THRSx = 0x0	28		36	µs
		HRT_MIN_THRSx = 0x1	56		72	µs
		HRT_MIN_THRSx = 0x2	112		144	µs
		HRT_MIN_THRSx = 0x3	224		288	µs

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HRT_MAX}	Hold current maximum ramp time threshold	HRT_MAX_THRSx = 0x0	224		288	ms
		HRT_MAX_THRSx = 0x1	448		576	ms
		HRT_MAX_THRSx = 0x2	896		1152	ms
		HRT_MAX_THRSx = 0x3	1792		2304	ms
t_{QTOT_MIN}	Quick Turn Off minimum ramp time threshold	QTOT_MIN_THRSx = 0x0	28		36	µs
		QTOT_MIN_THRSx = 0x1	56		72	µs
		QTOT_MIN_THRSx = 0x2	112		144	µs
		QTOT_MIN_THRSx = 0x3	224		288	µs
t_{QTOT_MAX}	Quick Turn Off maximum ramp time threshold	QTOT_MAX_THRSx = 0x0	3.5		4.5	ms
		QTOT_MAX_THRSx = 0x1	7		9	ms
		QTOT_MAX_THRSx = 0x2	14		18	ms
		QTOT_MAX_THRSx = 0x3	28		36	ms
t_{QTOST_MAX}	Quick Turn Off start time out		0.94		1.17	ms
Off-state diagnostics						
V_{OLP}	Voltage reference for comparator with respect to PVDD	OLP_SEL = 0x0	-0.32	-0.25	-0.18	V
		OLP_SEL = 0x1	-0.6	-0.5	-0.4	V
		OLP_SEL = 0x2	-0.85	-0.75	-0.65	V
		OLP_SEL = 0x3	-1.15	-1	-0.85	V
		OLP_SEL = 0x4	-1.4	-1.25	-1.1	V
		OLP_SEL = 0x5	-1.65	-1.5	-1.35	V
		OLP_SEL = 0x6	-1.95	-1.75	-1.55	V
		OLP_SEL = 0x7	-2.2	-2	-1.8	V
I_{OLP_PD}	Internal sink current on OUT to GND during Off-state diagnostics	VOUTx = PVDD	0.22	0.29	0.36	mA
t_{OLP_FLTR}	OLP Comparator deglitch time		250		350	µs
RIPROPI warning						
$R_{IPROPIL}$	R_IPROPIx lower threshold warning		3.2		4.4	kΩ
$R_{IPROPIH}$	R_IPROPIx upper threshold warning		22.7		30.5	kΩ
I_{IPROPI}	Pull up current on IPROPIx during initialization	V(IPROPIx) = 0 V	80		120	µA
R_{IPROPI_VAL}	CHx_RIPROPI value during initialization	IPROPIx resistor = 4.7 kΩ	237		255	code
		IPROPIx resistor = 6.8 kΩ	206		236	code
		IPROPIx resistor = 10 kΩ	165		205	code
		IPROPIx resistor = 15 kΩ	96		164	code
		IPROPIx resistor = 22 kΩ	1		95	code
V_{IPROPI_VAL}	CHx_VIPROPI value during initialization	IPROPIx resistor = 4.7 kΩ	12		40	code
		IPROPIx resistor = 6.8 kΩ	25		65	code
		IPROPIx resistor = 10 kΩ	45		103	code
		IPROPIx resistor = 15 kΩ	78		162	code
		IPROPIx resistor = 22 kΩ	123		245	code
SPI watchdog monitor						
t_{WD}	SPI valid transaction interval	SPI_WD_SEL = 0x0	56		72	ms
		SPI_WD_SEL = 0x1	224		288	ms
		SPI_WD_SEL = 0x2	896		1152	ms
		SPI_WD_SEL = 0x3	1792		2304	ms
Thermal protection						

Copyright © 2026 Texas Instruments Incorporated

4.5 V < V_{PVDD} < 35 V, 4.5 V < V_{VDD} < 5.5 V, - 40 °C < T_J < 150 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{TSD}	Thermal shutdown temperature		150	170	190	°C
T_{TSD_HYS}	Thermal shutdown hysteresis			20		°C
t_{TSD}	Thermal shutdown deglitch time		15		19	µs
T_{TSD_W}	Thermal shutdown warning temperature			150		°C
$T_{TSD\_W\_HYS}$	Thermal shutdown warning hysteresis			20		°C
t_{TSD_W}	Thermal shutdown warning deglitch time		15		19	µs
Device Safety Layer						
$V_{V5\_S\_UV\_FALL}$	V5_S Under voltage trigger threshold when falling		4.05	4.24	4.4	V
$V_{V5\_S\_UV\_RISE}$	V5_S Under voltage recovery threshold when rising		4.15	4.35	4.5	V
$V_{V5\_S\_UV\_HYST}$	V5_S UV hysteresis			0.11		V
$t_{V5\_S\_UV}$	V5_S UV deglitch time(1)		15		19	µs
$V_{V5\_S\_OV\_RISE}$	V5_S Over voltage trigger threshold when rising		5.9	6.2	6.5	V
$V_{V5\_S\_OV\_FALL}$	V5_S Over voltage recovery threshold when falling		5.5	5.8	6.1	V
$V_{V5\_S\_OV\_HYST}$	V5_S Over voltage hysteresis			0.4		V
$t_{V5\_S\_OV}$	V5_S OV deglitch time(1)		15		19	µs
f_{OSC}	Main oscillator frequency			20		MHz
t_{HEART_BEAT}	Heart beat interval from main logic		0.9		1.2	ms
t_{TIME_OUT}	Shut off timer time out duration		28		36	ms

(1) Guaranteed by design simulations.

5.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK minimum period(1)	125			ns
t_{SCLKH}	SCLK minimum high time	62.5			ns
t_{SCLKL}	SCLK minimum low time	62.5			ns
t_{HI_nSCS}	SDO minimum high time(2)	2000			ns
t_{SU_nSCS}	nSCS input setup time	40			ns
t_{H_nSCS}	nSCS input hold time	40			ns
t_{SU_SDI}	SDI input data setup time	20			ns
t_{H_SDI}	SDI input data hold time	20			ns
t_{EN}	SDO enable delay time			50	ns
t_{DIS}	SDO disable delay time			1000	ns

(1) SCLK minimum period is based on SDO external load of 20 pF. Additional load on SDO will further limit this minimum period.
(2) nSCS minimum high time is further limited in application by the pull up resistor SDO and capacitance on SDO.

Copyright © 2026 Texas Instruments Incorporated

5.7 Timing Diagrams

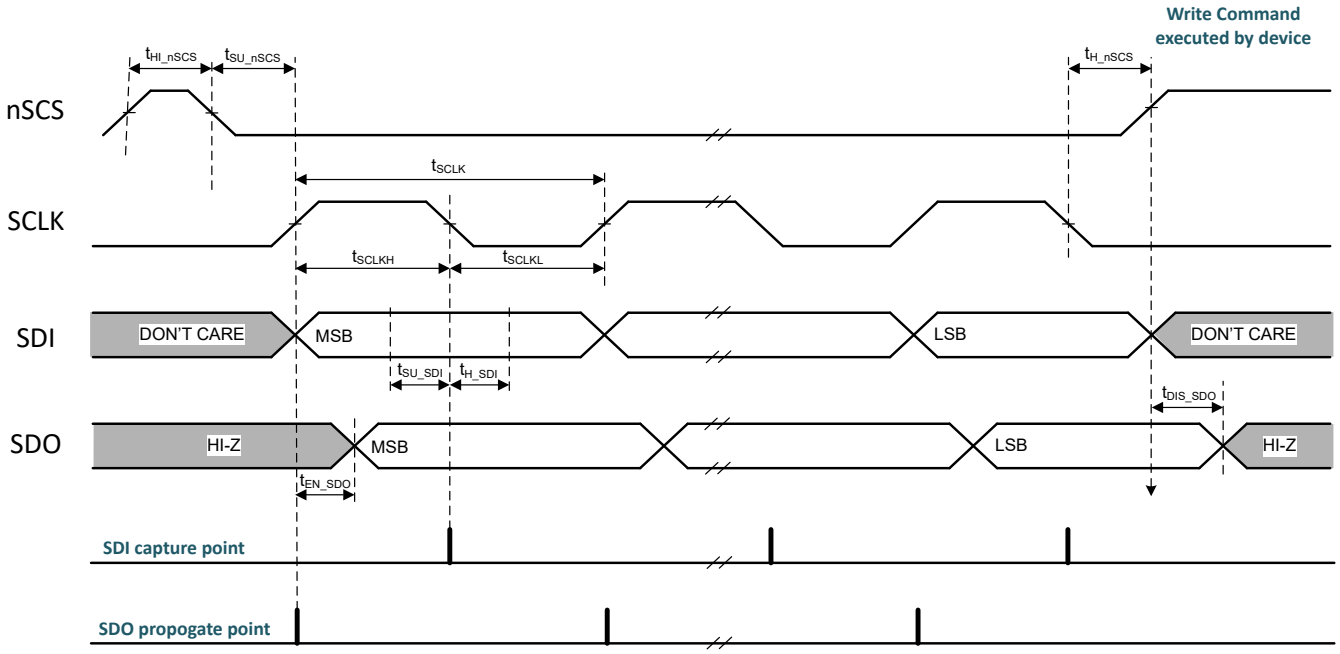


Figure 5-1. SPI Timing Diagram

5.8 Typical Characteristics

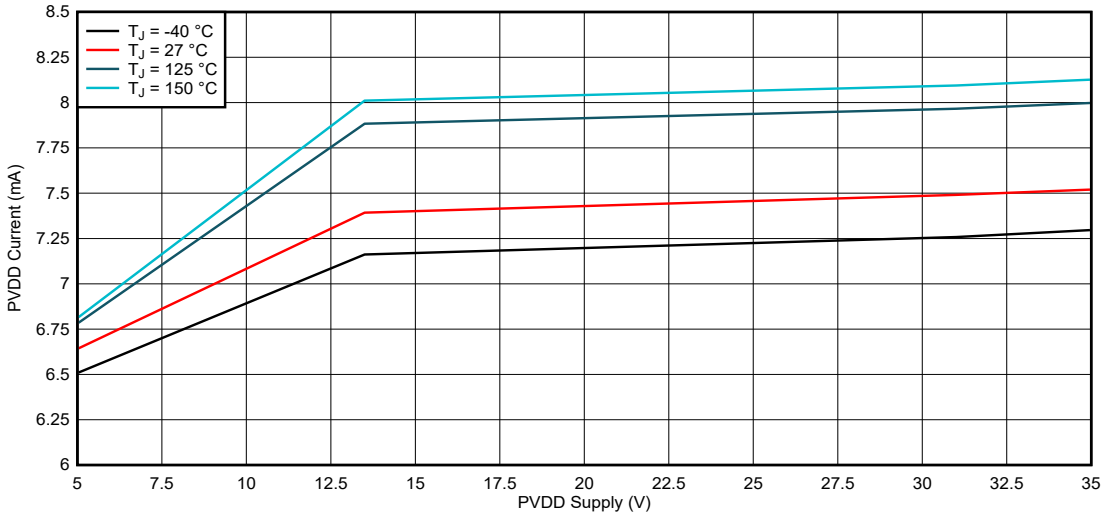


Figure 5-2. PVDD Current in Standby State, VDD = 5 V

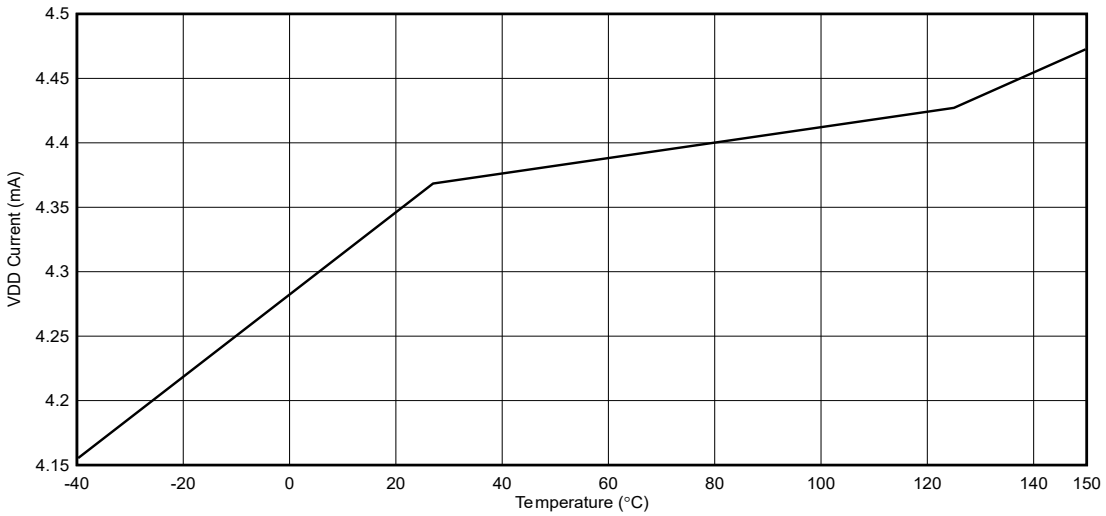


Figure 5-3. VDD Current in Standby State, PVDD = 0 V

Copyright © 2026 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

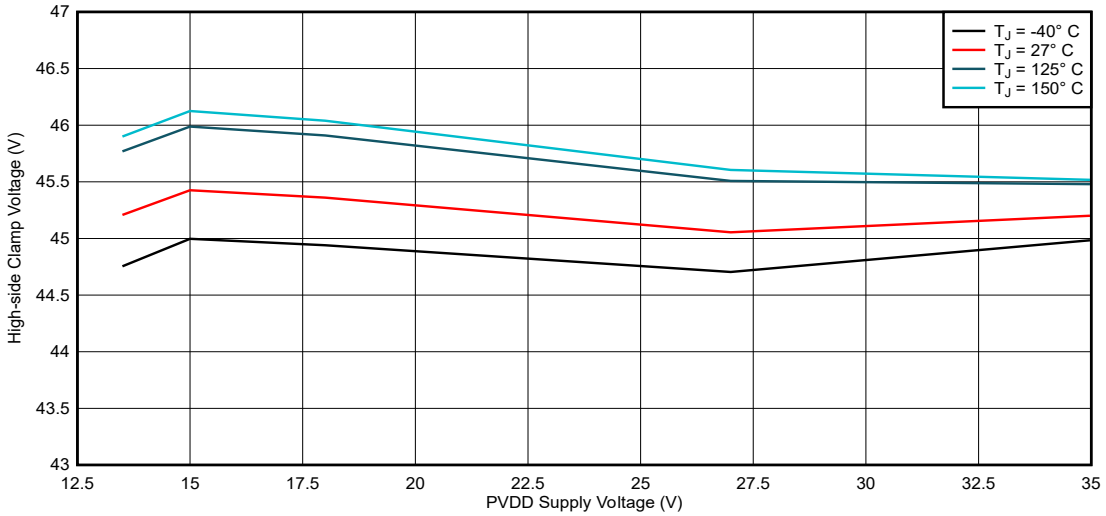


Figure 5-4. High-side Clamp Voltage, Active State

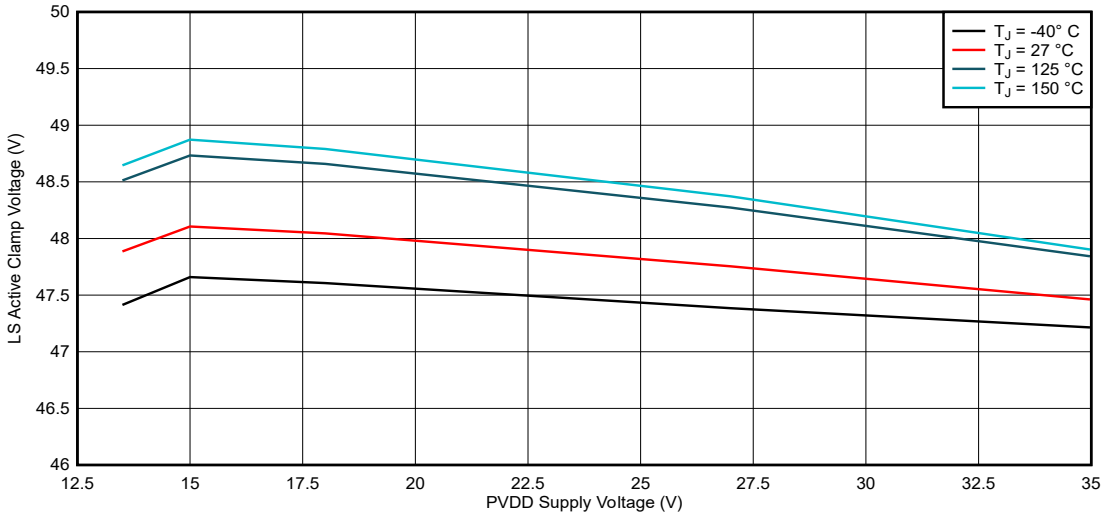


Figure 5-5. Low-side Active Clamp Voltage, Active State

Copyright © 2026 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

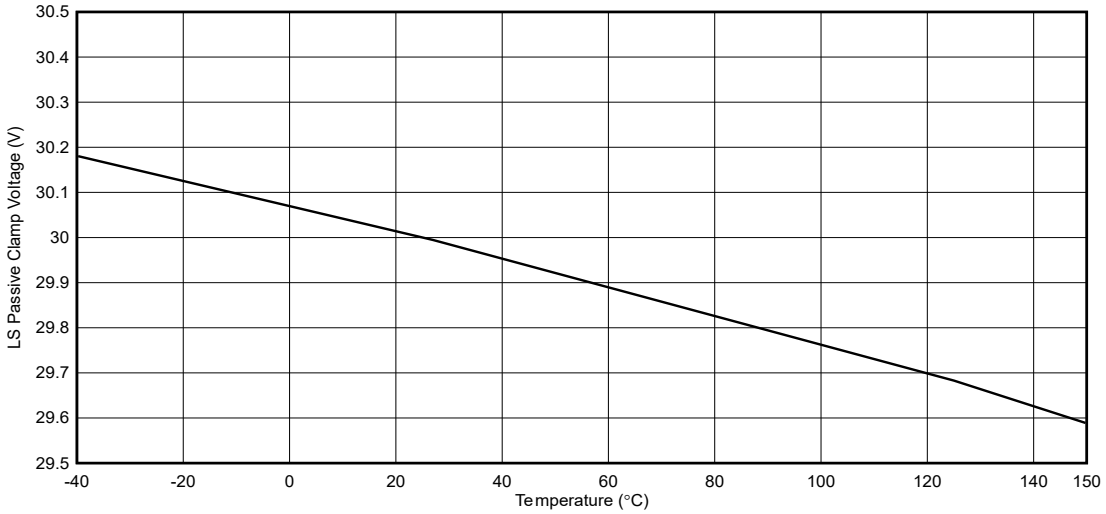


Figure 5-6. Low-side Passive Clamp Voltage in STANDBY state

Copyright © 2026 Texas Instruments Incorporated

6 Detailed Description

6.1 Overview

The table below outlines the various functions and their locations in this document. Detailed information on device initialization and software setup is provided in the Initialization Setup section.

Table 6-1. Function Overview

Category	Detailed Description Section	Electrical Characteristics Table
Power Supplies and Monitors	PVDD and VDD Power Supplies	PVDD and VDD Power Supplies
	PVDD Monitor	PVDD monitor
	VDD Monitor	VDD monitor
	Reset (nPOR)	Reset (nPOR)
	Device Safety Layer	Device Safety Layer
Output Driver	Output Driver	Output Driver
	Overcurrent Protection	
	Retry wait	Retry wait
	Thermal Protection	Thermal Protection
Start-up Sequencing	Start-up Sequencing	N/A
Current Control	Internal Regulation Mode	Internal current regulation, Switching parameters, Current Sense
	Fixed Frequency, Variable Duty Cycle Mode	
	Fixed Duty Cycle, Variable Frequency Mode	
	Quick Turn Off	
	PWM Frequency	
	Minimum and Maximum Duty Cycle	
Input pins	EN/EN1 and DIS/EN2 pins	EN/EN1 and DIS/EN2 pins
Diagnostics	On-state Diagnostics	On-state Diagnotics
	Off-state diagnostics	Off-state diagnostics
SPI Watchdog Monitor	SPI Watchdog Monitor	SPI Watchdog Monitor
nFAULT/NAD Pin	nFAULT/NAD Pin	nFAULT/NAD Pin
Fault Table	Fault Table	N/A
SPI Interface	Programming	SPI I/Os, SPI Timing Requirements

Copyright © 2026 Texas Instruments Incorporated

6.2 Functional Block Diagram

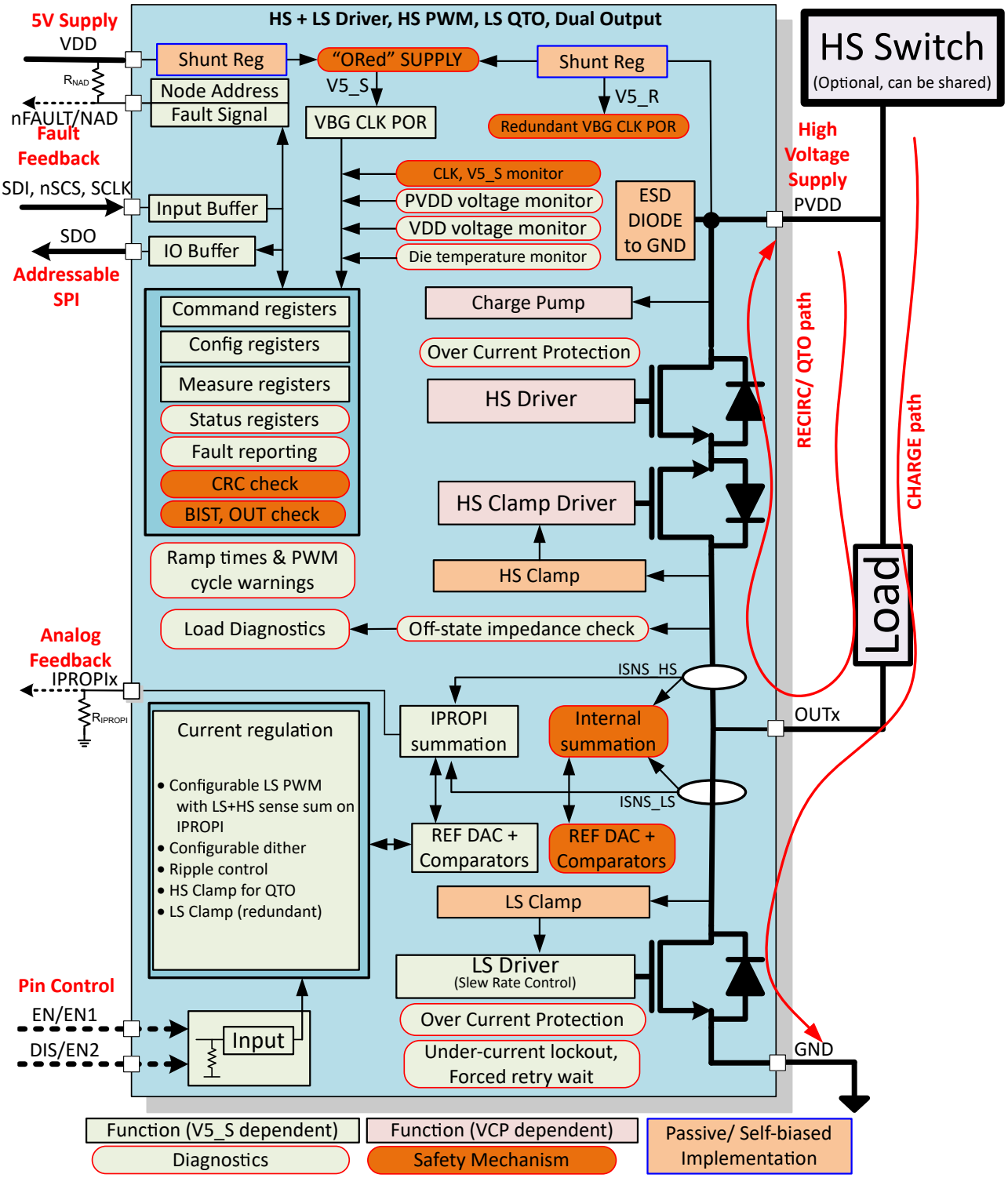


Figure 6-1. Functional Block Diagram

Copyright © 2026 Texas Instruments Incorporated

6.3 Feature Description

6.3.1 Recommended External Components

Table 6-2 lists the recommended external components for the DRV3946-Q1.

Table 6-2. External Components

Pin	Component	Purpose	Suggested Value
IPROPI1	Resistor to GND	Sets the range for the peak and hold current for output 1. This resistor needs to be in the specified range, else RIPROPI1_W warning flag will be set. Range allows for ~4X scaling of current based on relay type.	4.7kΩ to 20kΩ, 0.063W, **1%**
IPROPI1	Capacitor to GND	**Optional** - filter capacitor on IPROPI1 pin	10pF ceramic capacitor
IPROPI2	Resistor to GND	Sets the range for the peak and hold current for output 2. This resistor needs to be in the specified range, else RIPROPI2_W warning flag will be set. Range allows for ~4X scaling of current based on relay type.	4.7kΩ to 20kΩ,0.063W, **1%**
IPROPI2	Capacitor to GND	**Optional** - filter capacitor on IPROPI2 pin	10 pF ceramic capacitor
SDO	Resistor to VDD	Pull up resistor to ensure that SDO output is registered as high when not driven by the device.	10 kΩ, 0.063 W, 10%
nFAULT/NAD	Resistor to VDD	Sets the unique node address for SPI communication. This resistor needs to be one of the four resistor values allowed, else NAD_ERR flag will be set and SPI communication will be affected.	5.6kΩ/ 12kΩ/ 27kΩ/ 56kΩ, 0.063W, **1%**
PVDD	Bulk capacitor to GND	Local bulk capacitor on PVDD to handle transients	≥ 10µF, 35V
PVDD	Diode to GND	**Optional** – Diode to GND on PVDD to handle inductive current during load de-energization	35V, ≥ 1A
PVDD	Bypass capacitor to GND	Local high frequency bypass capacitor on PVDD	0.1µF, 35V, low ESR ceramic capacitor
VDD	Bypass cap to GND	**Optional** – Local high frequency bypass capacitor on VDD	0.1µF, 6.3V, low ESR ceramic capacitor
OUT1	EMC cap across load	**Optional** - High frequency EMC capacitor across load on output 1	≤ 0.1µF, low ESR ceramic capacitor
OUT2	EMC cap across load	**Optional** - High frequency EMC capacitor across load on output 2	≤ 0.1µF, low ESR ceramic capacitor

When a redundant High-Side (HS) switch is used to cut-off the 12V supply, the output of the HS switch (PVDD pin) needs to have sufficient capacitance to guarantee:

- dV/dt < 2V/µs on PVDD when HS switch is closed
- Ability to source the transient load current (inductive fly back) in case of:
  - Clamping function is NOT handled by DRV3946-Q1
  - Fault condition: When the HS switch is opened with the loads energized and one of the outputs shorted to GND (loss of clamping function for DRV3946-Q1).

The capacitance on PVDD is meant to prevent the violation of the ABS MIN on this pin during this transient. An optional diode from PVDD to GND is recommended to help with the inductive current sourced from PVDD during the clamping time to reduce the capacitor size. Depending on the current levels, half-bridge drivers could be an option to combine both the high-side switch cutoff function and discrete diode recirculation function to dissipate the inductive energy when the switch is opened.

Copyright © 2026 Texas Instruments Incorporated

6.3.2 Power Supplies and Monitors

This section describes the power supply architecture and associated safety features of the DRV3946-Q1.

6.3.2.1 PVDD and VDD Power Supplies

The DRV3946-Q1 is powered through the PVDD (12 V through an optional HS cut-off switch) and VDD (5 V) pins. While the drivers and the output stage are mainly supplied from PVDD, the logic, critical safety and diagnostic functions are driven from an internal 5V supply (safe 5V referred to as V5_S) that is derived from a power “OR” combination of PVDD and VDD. The power ORing ensures that the device maintains its intelligence and critical functions even if there is a loss of one of the supplies. Voltage references, current biases, oscillator and the digital block are powered by the V5_S. Redundant references and biases derived from PVDD are used to qualify V5_S and the oscillator.

Following a power-on-reset (POR) on V5_S, a power-up initialization is done that includes the address NAD determination, internal self-test (BIST) of the memory and diagnostics, R_{IPROPI} determination and settling time for internal blocks within t_{READY} time. A CLR_FAULT SPI command from the user to acknowledge wake-up will place the device in the STANDBY state, with drivers in the high-impedance (Hi-Z) state until commanded by the user. The current consumption of the device will be I_{PVDD_STBY} and I_{VDD_STBY} in STANDBY state. Since the device uses a power "OR" architecture, certain functions are available even in the event that one of the external power supplies is lost.

Table 6-3 shows key device functionality with varying VDD voltage levels, assuming PVDD is within undervoltage and overvoltage limits.

Table 6-3. Dependence on VDD Supply

VDD	Relay-on (Active state) function	Off-state Diagnostics	SPI Communication
> $V_{VDD\_OV\_RISE}$	Available (1)	Available (1)	SDI Ok, SDO will see VDD_ERR
Nominal	Available (1)	Available (1)	Available
< $V_{VDD\_UV\_FALL}$	Available (1)	Available (1)	SDI Ok, SDO will see VDD_ERR

(1) Limited by the overcurrent and over temperature protection functions of the device.

Table 6-4 shows key device functionality with varying PVDD voltage levels, assuming VDD is within undervoltage and overvoltage limits.

Table 6-4. Dependence on PVDD Supply

PVDD	Relay-on (Active state) function	Off-state Diagnostics	SPI Communication
> $V_{PVDD\_OV\_RISE}$	Configurable with PVDD_OV_SHUTOFF_EN	Available(1)	Available
Nominal	Available(1)	Available(1)	Available
< $V_{PVDD\_UV\_FALL}$	Device will go to STANDBY, outputs Hi-Z with QTO (passive) clamping, PVDD_UV flag will be set	Not Available	Available

(1) Limited by the overcurrent and over temperature protection functions of the device

When PVDD < $V_{PVDD\_UV\_FALL}$, transient behavior in the active-state during deglitch time is as follows:

- If PVDD > $V_{PVDD\_UV\_BIAS\_FALL}$ and internal regulation is enabled, device will switch to a 75% open loop regulation with fixed duty cycle and slew rate capped at SR = 0x2
- If PVDD < $V_{PVDD\_UV\_BIAS\_FALL}$ and internal regulation is enabled, device will switch to open loop regulation with 100% duty cycle

Table 6-5 shows key device functionality with loss of both PVDD and VDD power supplies.

Copyright © 2026 Texas Instruments Incorporated

Table 6-5. Loss of VDD and PVDD Supply

PVDD	VDD	Relay-on (Active state) function	Off-state diagnostics	SPI communication
< $V_{PVDD\_RST\_FALL}$	< $V_{VDD\_RST\_FALL}$	Not available	Not available	Not available

6.3.2.2 PVDD Monitor

The device has undervoltage (V_{PVDD_UV}) and overvoltage (V_{PVDD_OV}) fault monitors, as well as a warning level monitor ($V_{PVDD\_OV\_W}$) on the PVDD power supply. The voltage monitor results are recorded in the SPI STATUS registers.

In addition, there is a bias undervoltage monitor ($V_{PVDD\_UV\_BIAS}$) with a threshold level below PVDD undervoltage monitor. If the PVDD voltage drops below the bias under voltage level, the output drivers are disabled and forced Hi-Z.

6.3.2.3 VDD Monitor

The device has an under voltage (V_{VDD_UV}) and over voltage (V_{VDD_OV}) monitor on the VDD power supply. VDD undervoltage or overvoltage are indicated directly in the leading bit of the SDO SPI frame (VDD_ERR) response.

6.3.2.4 RESET (nPOR)

Power on reset (nPOR) for the device logic is based on the internal V5_S derived from the power “OR“ combination of PVDD (V_{PVDD_RST}) and VDD (V_{VDD_RST}).

In the event of an nPOR, all the registers are reset and a new start-up sequence should be followed.

6.3.2.5 Device Safety Layer

The device safety layer includes a voltage monitor on V5_S, frequency monitor on the main oscillator (f_{OSC}) with a secondary time out logic running on a seperate redundant oscillator (f_{OSC_R}). Any V5_S undervoltage or overvoltage or f_{OSC} underfrequency or overfrequency event for a time > t_{TIME_OUT} will result in output drivers disabled (Hi-Z) with device lock out fault, DEV_ERR.

Copyright © 2026 Texas Instruments Incorporated

6.3.3 Output Driver

The device has two independent drivers to drive two relays. Each driver is a modified half bridge for charge path to GND using low-side FET and back-to-back high-side FETs for recirculation and Quick Turn Off (clamping) for current decay. With the integrated power FETs, the device is capable of output wave shaping during PWM switching cycles to improve EMC performance. The device also supports programmable output voltage slew rate control.

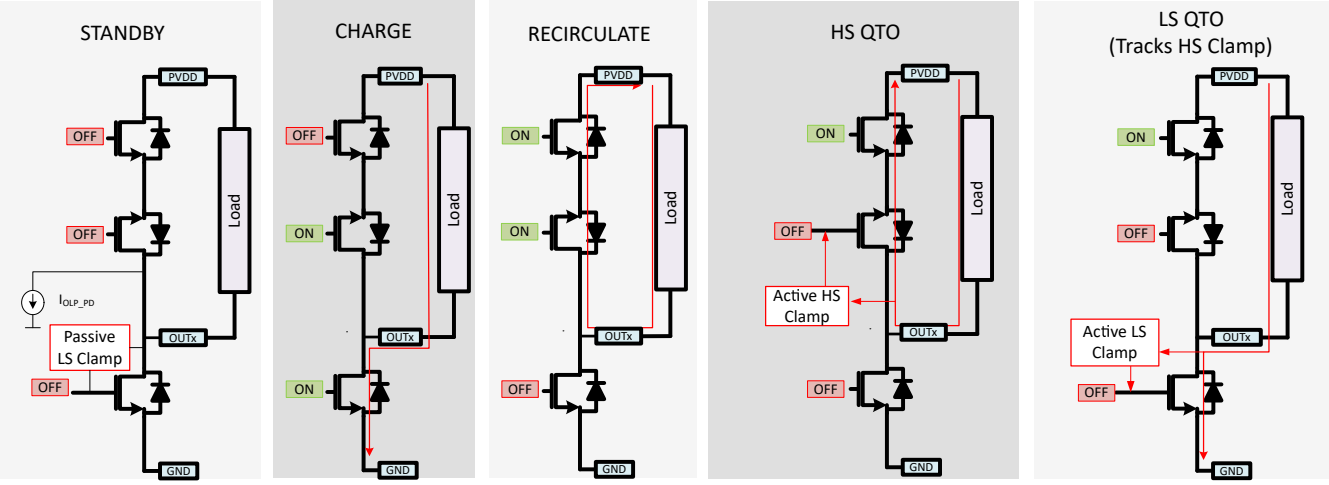


Figure 6-2. Output Driver

- **STANDBY state**: In this state, the drivers are OFF and OUTx is Hi-Z. OUTx is pulled down to GND with a current sink (I_{OLP_PD}).
- **ACTIVE state**: When the driver is commanded to turn on, the drivers are controlled by internal state machine to regulate the load current as configured (Peak current, Peak time, Hold current) along with the PWM parameters (PWM frequency, dither options).
  - The driver switches between CHARGE and RECIRCULATE phases to regulate the load current.
  - During CHARGE phase, current flows from load into the OUTx pin to the low-side FET to GND, while during RECIRCULATE, current recirculates between load into the OUTx pin to the two back to back high-side FETs to PVDD.
- **STANDBY state**: If the driver is commanded to turn off when the load is energized, the device forces a large voltage across the load in the opposite direction to decay the load current quickly. This is referred to as Quick Turn Off feature (QTO). During the QTO there are two possible current paths. High-side QTO is activated for all cases except PVDD overvoltage, in which case Low-side QTO is activated.
  - High-side (HS) QTO (Preferred): In this case, when the device is Hi-Z, the inductive current of the load pushes the voltage on the OUTx high to a point where the drain-to-gate clamp of the HS QTO FET breaks down and turns on the FET briefly till the inductive current has been decayed completely. This is the preferred clamping method as it limits the power dissipation inside the device and also pushes the inductive energy back to the PVDD supply capacitor.
  - Low-side (LS) QTO: In this case, when the device is Hi-Z, the inductive current of the load pushes the voltage on the OUTx high to a point where the low-side drain-to-gate clamp of the LS FET breaks down and turns on the FET briefly till the inductive current has been decayed completely. The LS clamp is a redundant structure and typically tracks to a voltage equal to HS Clamp voltage + 1 V. One exception is in case of PVDD OV fault, the LS clamp voltage is same as the HS clamp voltage.

6.3.3.1 Retry Wait

A configurable RETRY_WAIT timer (t_{RETRY_WAIT}) ensures a minimum off time for the relay. This can prevent inadvertant back-to-back quick turnon – turnoff – turnon events.

Copyright © 2026 Texas Instruments Incorporated

The RETRY_WAIT feature can be disabled with RETRY_WAIT_DIS bit.

6.3.3.2 Over Current Protection

The output driver MOSFETs are protected against pin shorts on both low-side (I_{OCP_LS}, short to battery) and high-side (I_{OCP_HS}, short to GND). Detection of an overcurrent event results in the affected output Hi-Z (driver shut off) with fault flagged in the CHx_STAT register.

6.3.3.3 Thermal Protection

The output driver MOSFETs are thermally protected in the event of an over temperature event. Detection of an over temperature event (T_{TSD}) results in the both outputs Hi-Z (driver shut off) with fault flagged in the CHx_STAT register. The device also issues an over temperature warning (T_{TSD_W}) which is set at a lower threshold than the thermal shut down. The device can be configured to switch at higher slew rates to reduce PWM switching losses in case of a thermal warning if the OT_W_ACTION bit is set.

Copyright © 2026 Texas Instruments Incorporated

6.3.4 Start-up Sequencing

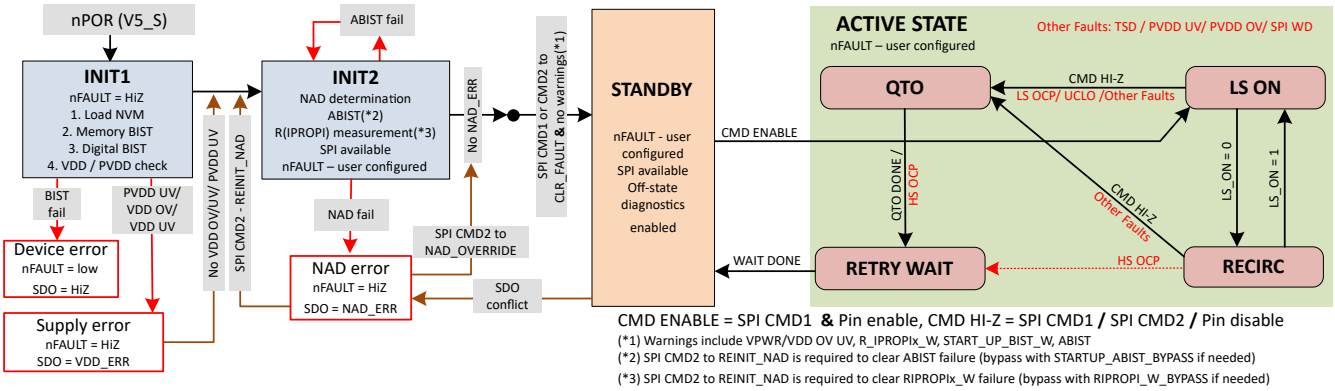


Figure 6-3. Simplified Start-up Sequencing Diagram

- Either PVDD or VDD will initiate power up of the device.
- A release of the internal power-on-reset (nPOR on V5_S) moves the device into the INIT1 state. In INIT1, the factory programmed NVM is loaded and a memory BIST (CRC check) and digital BIST is performed.
  - If there is a BIST failure, the device will enter a locked error state indicated by driving the nFAULT pin low and DEV_ERR fault on the SPI (SDO output Hi-Z). Only a power cycle can re-start this sequence.
- After entering the INIT1 STATE, the device waits until both VDD and PVDD are valid. For example, no VDD overvoltage, VDD undervoltage, or PVDD undervoltage before transitioning to the INIT2 state.
  - By default, the SPI SDO VDD_ERR is set. Only in case of no supply error, will VDD_ERR clear.
- In the INIT2 STATE, NAD_ERR is set by default. The device will start the node address (NAD) determination based on the pull-up resistor on the nFAULT/NAD pin. After a valid NAD determination, the NAD_ERR will clear.
  - After a successful NAD determination, the SPI POR bit in STATUS0 is set to indicate a device wake up from reset, SPI communication is available, and nFAULT indicators are configured for default settings.
- Next, an analog BIST (ABIST) is performed, whose failure is recorded in STARTUP_BIST_W bit in STATUS1.
- The resistance on IPROPI is determined by forcing a current $I_{RIPROPI}$ on both the IPROPIx pins, whose failure is recorded in CHx_RIPROPI_W bit in STATUS1 register.
  - An internal resistor R_{INT} used for secondary ripple loop current regulation is calibrated to match the resistance on the IPROPI pin, by forcing a current on the external resistor on the IPROPIx pin.
  - Voltage and resistance measured on IPROPIx pin are recorded in MEAS5 and MEAS6 resisters.
- EN/EN1_PIN_STAT and DIS/EN2_PIN_STAT will reflect the instantaneous pin level.
- If a NAD_ERR is detected after the automatic NAD determination, the microcontroller can either request a re-determination using the REINIT_NAD broadcast command or issue a NAD_OVERRIDE broadcast command with the ASSIGNED_NAD. Only the device(s) with the NAD_ERROR will process this command.
- While in INIT2, if VDD overvoltage or undervoltage occurs, NAD determination can be wrong and NAD_ERR is set. RE_INIT_NAD command has to be sent once VDD_ERR is cleared.
- VDD_ERR corresponds to VDD UV or OV or PVDD UV till device enters STANDBY.
- To enter the STANDBY STATE, the device now expects the microcontroller to perform a series of steps -
  - Write 14 bytes of CONFIG A and 10 bytes of CONFIG B registers along with their calculated CRCs
  - Issue a CLR_FAULT SPI command. If there are no wanrnings, this command puts the device in the STANDBY state with nFAULT de-asserted.
- Once in the STANDBY state, the device monitors the load with off-state diagnostics with nFAULT fault assertion as configured.
- **The EN/EN1 and DIS/EN2 pins must be driven AND the CHx_CTRL bits in CMD1 register must be programmed appropriately to turn ON the driver.** These pins can be configured as ENABLE and DISABLE for both outputs (default) or as ENABLE1 and ENABLE2 for each output seperately.

Copyright © 2026 Texas Instruments Incorporated

6.3.5 Current Control

Figure 6-4 illustrates current regulation and various modes of operation. The DRV3946-Q1 supports -

- SPI command or PINs to enable/disable the driver (shown in YELLOW) - minimum controller interaction required
- Ability to configure the load current profile and diagnostic monitoring using 20 bytes of CONFIG registers (highlighted in LIGHT ORANGE in Figure 6-4)
- 8 bytes of STATUS registers (highlighted in DARK ORANGE) for diagnostics / faults information with a summary byte
- 10 bytes of MEASUREMENT registers (highlighted in GREEN) for average duty cycle and ramp times for system S/W diagnostics

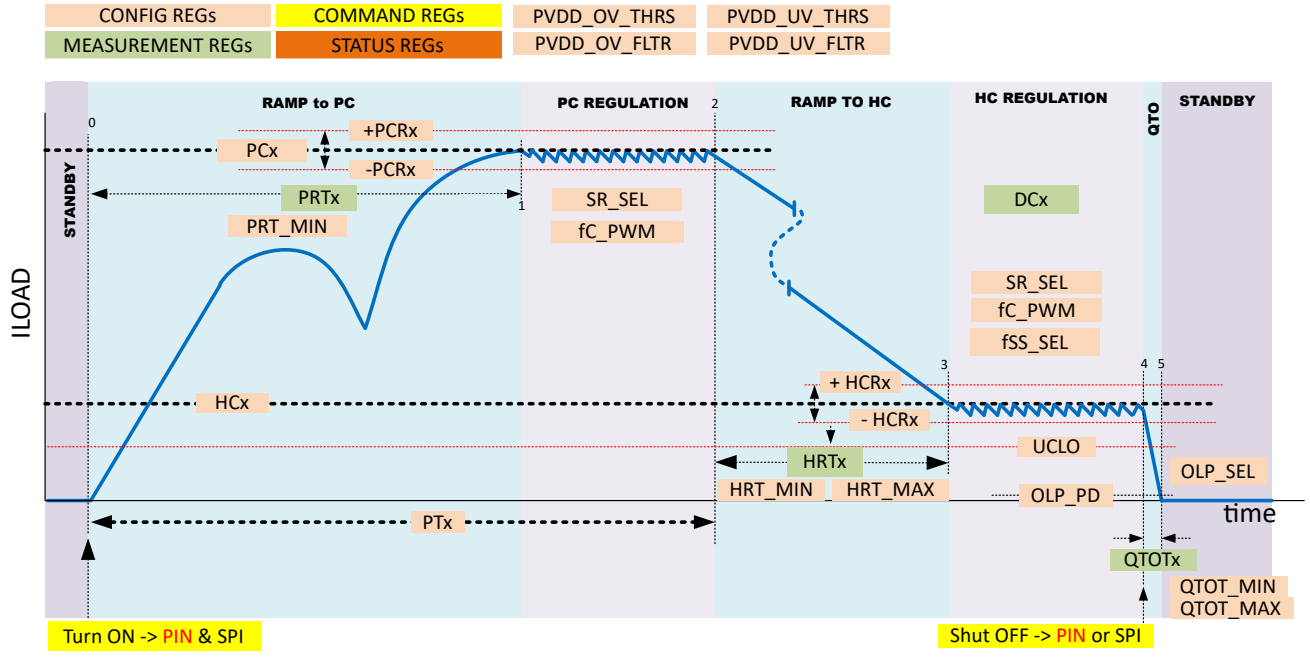


Figure 6-4. Current Control Illustration

Table 6-6. Glossary

PC	Peak Current	**UV**	Under voltage
PCR	Peak Current Ripple	**OV**	Over voltage
HC	Hold Current	**UCLO**	Under current lock out
HCR	Hold Current Ripple	**OLP_PD**	OUT to GND sink current during off-state diagnostics
PT	Peak Time	**DC**	Duty Cycle
PRT	Peak Ramp Time	**OLP_SEL**	Off-state diagnostics comapartor threshold
HRT	Hold Ramp Time	**SR_SEL**	Output slew rate
QTO	Quick Turn Off	**f_{C_PWM}**	Center frequency for PWM
QTOT	Quick Turn Off Time	**f_{SS_SEL}**	Spread Spectrum for PWM frequency

The user can command each driver ON independently with a SPI command either in an internal regulation mode or in a fixed frequency or fixed duty cycle mode, as explained in the following sections.

The device has shuntless current sense topology based on FET matching to sense the load current on both LS FET and HS FET. The current scaling factor is set by the ratio of the power FET to the sense FET.

Copyright © 2026 Texas Instruments Incorporated

6.3.5.1 Internal Regulation Mode

Internal regulation mode is selected by making CHx_CTRL_CONFIG = 0x0 and CHx_CTRL = 0x2. The internal regulation is a cycle-to-cycle peak current regulation algorithm mainly based on low-side current sense expressed on the IPROPIx pin with additional high-side sense information and ripple control based on redundant current sense experssed on internal R_{INT} resistor.

The device allows for peak cycle to be completely skipped (PC_DIS register bit). Internal regulation mode can be initiated with the following options -

- If PC_DIS = 0b and PC_REG_DIS = 0b, the load current is ramped up (100% LS ON) till load current > peak current target (PC) and lower peak ripple (PCR-) and then regulated at PC target for the duration of peak time. Then it is followed by ramp down in recirculation till load current < hold target (HC) or lower hold ripple (HCR-), thereafter maintaining regulation at HC target till commanded to shut off.

  If PC_DIS = 0b and PC_REG_DIS = 1b, the LS is turned on 100% for entire duration of the programmed peak time without regulation (100% LS ON) followed by ramp down to hold current target, thereafter maintaining regulation at HC target till commanded to shut off.

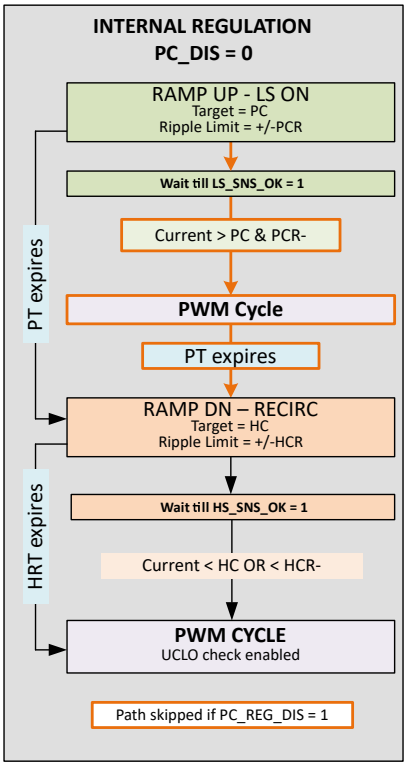


Figure 6-5. Internal Regulation, PC_DIS = 0b

-

Copyright © 2026 Texas Instruments Incorporated

If PC_DIS = 1b, peak regulation is completely skipped with a ramp up (or down) to hold current target, thereafter maintaining regulation (PWM CYCLE).

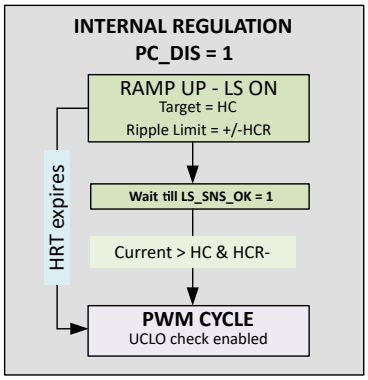


Figure 6-6. Internal Regulation, PC_DIS = 1

- Current targets and regulation parameters can be configured. Load current feedback through IPROPI pin as well as measured ramp times and average duty cycle information is available. PWM cycle warnings and other timing monitors are also available.

6.3.5.1.1 Current Thresholds

The device allows for a configurable peak time during internal current regulation set by register CHx_PT. The peak current and hold current targets are set by an internal 8-bit DAC with inputs from user registers (CHx_PC and CHx_HC) respectively. Current reference is ratiometric to the resistance on the IPROPIx pin ($R_{IPROPIx}$). This sets the threshold for the primary peak current regulation loop.

In addition, the device has a secondary ripple control loop set by an additional DAC and an internal resistor R_{INT} matched to $R_{IPROPIx}$ with inputs from CHx_RIPPLE_THRS register. Ripple+ and Ripple- are the respective high and low ripple current levels. This loop is completely independent of the primary loop for fail safe reasons. R_{INT} matching to $R_{IPROPIx}$ is done during device initialization (INIT2 state).

Also, as an anti-chatter prevention feature, the user can set a threshold for under current lock out (UCLO) valid during hold regulation, set by CHx_UCLO_THRS register. An UCLO event is detected if the driver is not able to sense current greater than this level for a duration of PWM cycles set by UCLO_FAULT_FLTR. The reaction to Hi-Z the driver or simply warn the user can be set by UCLO_EN bit.

Table 6-7 shows the derivations for peak current, hold current, current ripple and UCLO current:

Table 6-7. Peak, Hold, Ripple and UCLO Current Derivations

Register	Interpretation
CHx_HC	Hold current = (CHx_HC + 17)/272 x A_{IPROPI} x 3V / $R_{IPROPIx}$
CHx_PC	Peak current = (CHx_PC + 17)/272 x A_{IPROPI} x 3V / $R_{IPROPIx}$
CHx_RIPPLE_THRS	Ripple+ current = Hold / Peak current x [1 + 5% x (CHx_RIPPLE_THRS + 3)]
	Ripple- current = Hold / Peak current x [1 - 5% x (CHx_RIPPLE_THRS + 3)]
CHx_UCLO_THRS	UCLO current = Ripple- current x [1 - (5% x (CHx_UCLO_THRS + CHx_RIPPLE_THRS + 4))]

Copyright © 2026 Texas Instruments Incorporated

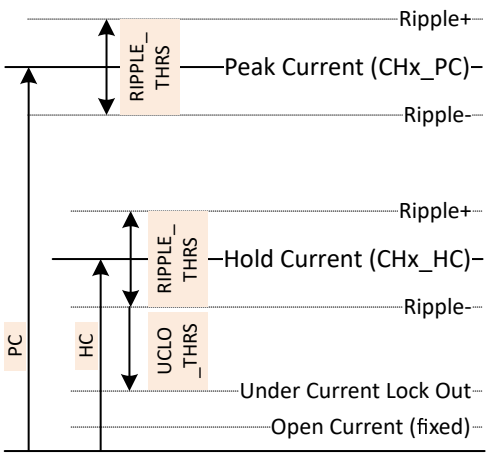


Figure 6-7. Current Thresholds

Note that UCLO_THRS is derived from the RIPPLE current threshold. Table 6-8 shows the RIPPLE and UCLO current threshold as a percentage of the Peak or Hold current.

Table 6-8. Ripple and UCLO current Derivations

RIPPLE_THRS	% of PC / HC		UCLO_THRS (% of HC)			
	RIPPLE+	RIPPLE-	0	1	2	3
0x0	115%	85%	68%	64%	60%	55%
0x1	120%	80%	64%	60%	56%	52%
0x2	125%	75%	60%	56%	53%	49%
0x3	130%	70%	56%	53%	49%	46%
0x4	135%	65%	52%	49%	46%	42%
0x5	140%	60%	48%	45%	42%	39%
0x6	145%	55%	44%	41%	39%	36%
0x7	150%	50%	40%	38%	35%	33%

Copyright © 2026 Texas Instruments Incorporated

6.3.5.1.2 PWM Cycle Control

When internal regulation is enabled, the device implements a cycle-to-cycle peak current regulation algorithm mainly based on low side current sense expressed on the IPROPIx pin with additional high side sense information and ripple control based on redundant current sense experssed on internal R_{INT} resistor. Also BIST and feedback time out features are implemented.

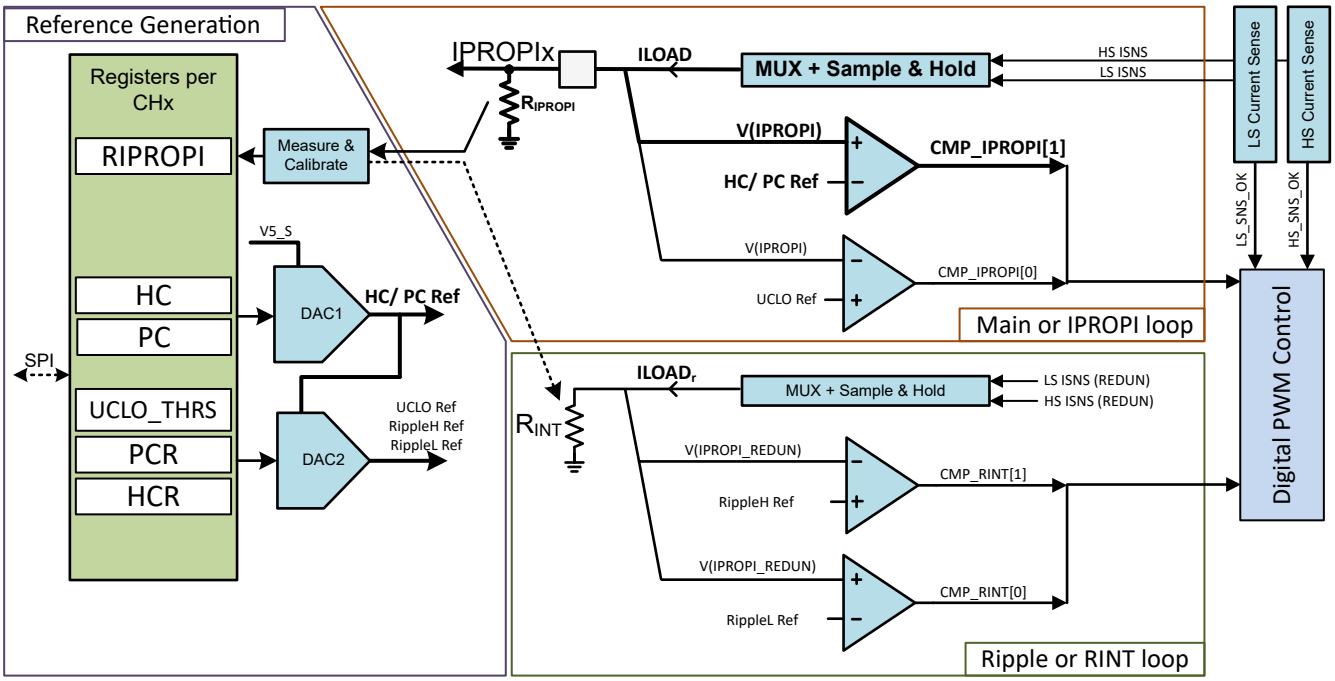


Figure 6-8. Regulation Block Diagram

- The reference generation block consists of DACs whose output voltages are set by the user-controlled register bits. The HC and PC reference is set based on an internal reference (V5_S) by DAC1. The DAC2 is ratiometric to the DAC1 output and sets the ripple levels and UCLO reference.
- The main loop (or IPROPI loop) is based on the comparison of IPROPI pin with the HC and PC reference. This comparison is shown by CMP[1] in the IPROPI regulation loop. The voltage on IPROPI is set by load current sense (LS + HS current sense) x R_{IPROPI}.
- The ripple control loop (or R_{INT} loop) is based on the comparison of an internal voltage set by (load current x R_{INT}) with +/- RippleH / RippleL reference. This is shown by the two comparators, CMP[1] and CMP[0] in the ripple control loop block.
- A fourth comparator is CMP[0] in the IPROPI regulation loop that enables under current lock out function.
- One comparator output from LS sense indicates whether the LS current sense is valid (reached the desired accuracy level following the OUTx slewing low following LS FET turned ON during charge operation)
- Another comparator output from HS sense indicates whether the HS sense is valid (reached the desired accuracy level following the OUTx slewing high following HS FET turned ON during recirculation operation)
- In case of loss of the pin function of the IPROPIx pin (short or open), the device can still regulate the current based on the ripple current limits, while warning the user about the loss of the pin function through the PWM cycle warnings.

Note

For this cycle-by-cycle peak current regulation loop, external capacitance on the IPROPIx pin should be avoided.

Flow charts for the PWM cycle with and without cycle skipping are shown below -

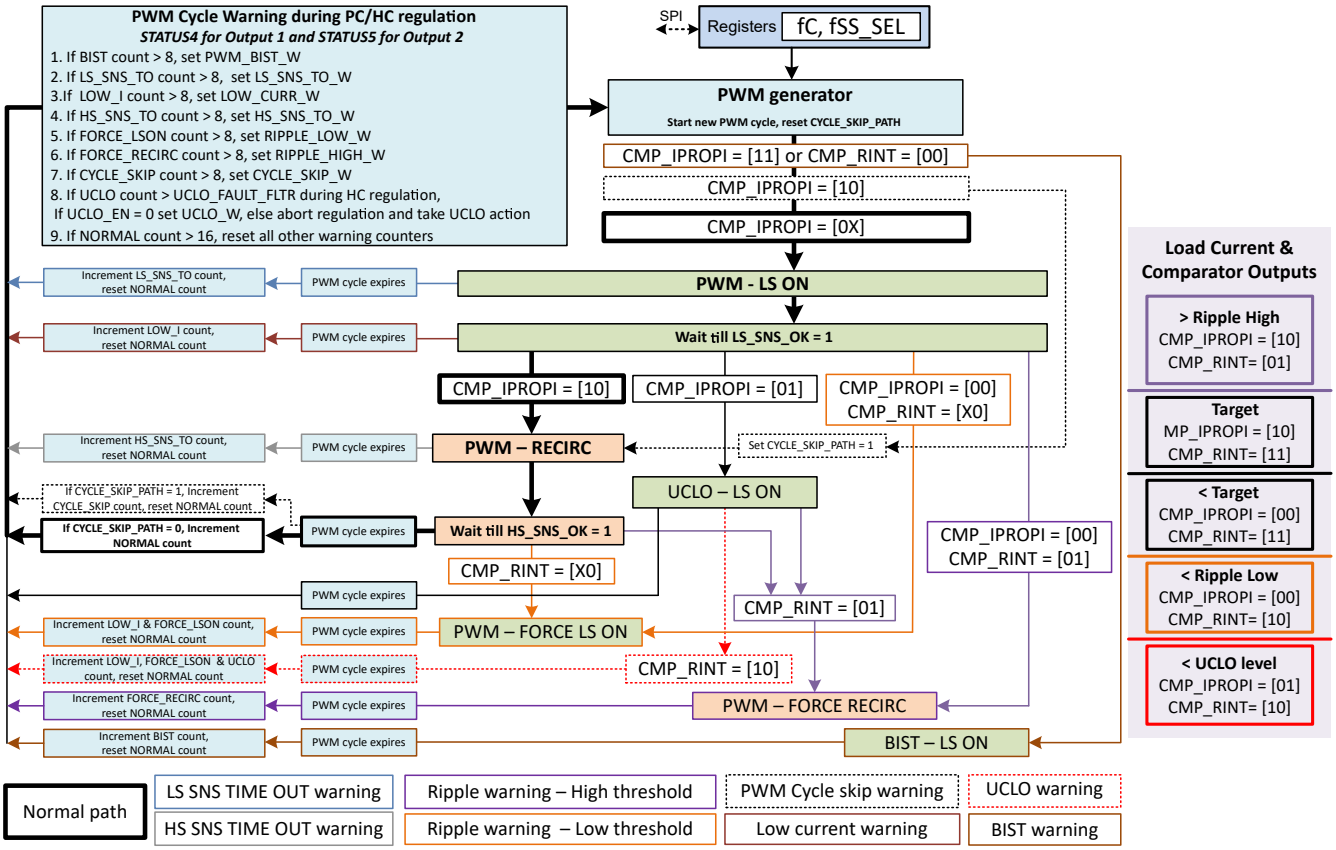


Figure 6-9. PWM CYCLE with cycle skip enabled [PWM_CYCLE_SKIP_DIS = 0]

Copyright © 2026 Texas Instruments Incorporated

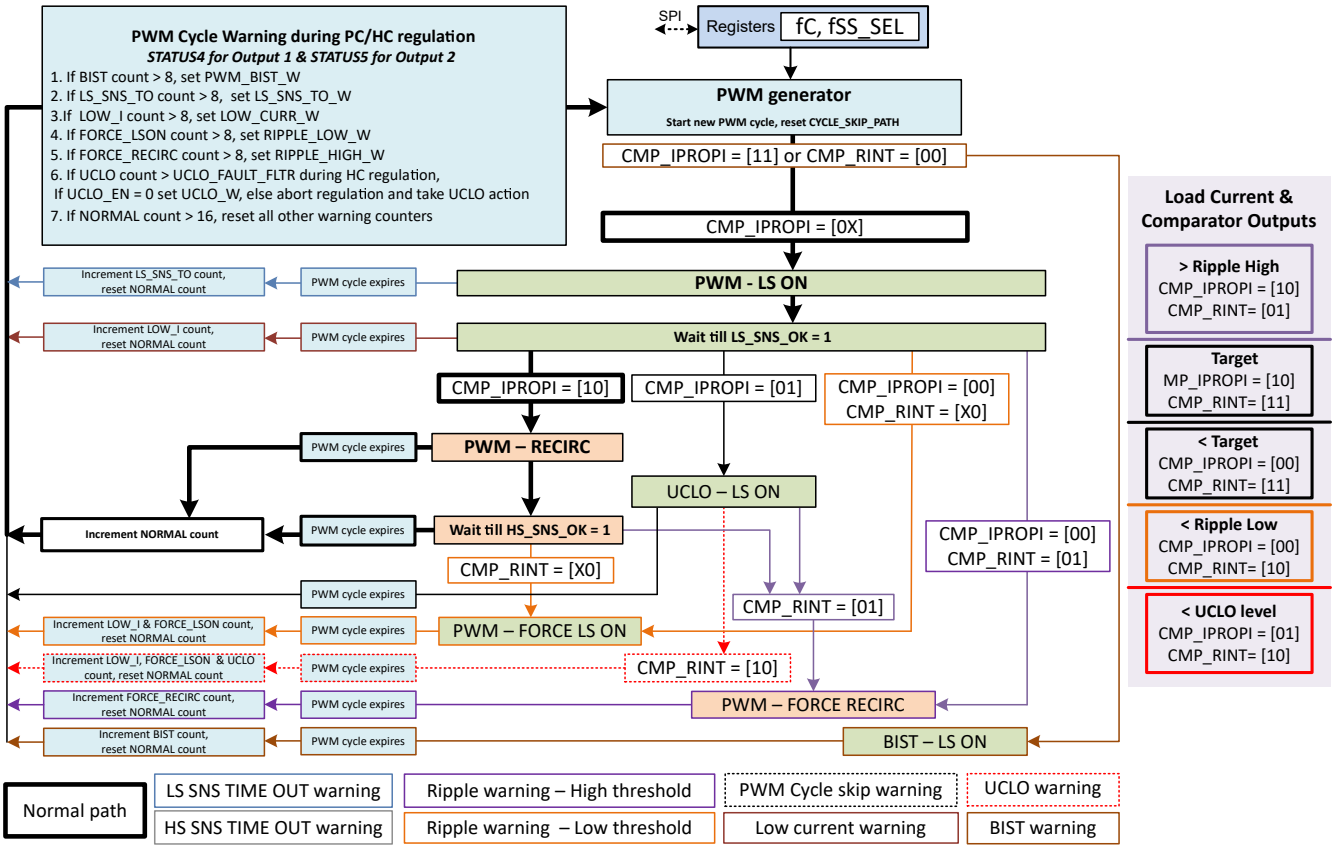


Figure 6-10. PWM CYCLE with cycle skip disabled [PWM_CYCLE_SKIP_DIS = 1]

A typical normal sequence (highlighted in bold) would be as follows:

- Start of new PWM cycle (PWM period set by fC, fSS_SEL)
- CMP_IPROPI = [0X] => Indicates that recirculation current sensed by high side is less than the target
- PWM - LS ON (charge)
- Wait for LS_SNS_OK
- CMP_IPROPI = [10] => Indicates that charge current sensed by low side is greater than the target
- PWM – RECIRC (recirculate)
- Wait for HS_SNS_OK
- PWM period expires to indicate end of cycle

The alternate paths show the PWM regulation behavior when the comparator outputs are NOT as expected. This could occur due to various reasons, such as -

- PVDD supply level (high side of the relay)
- Choice of PWM frequency
- Slew rates
- Load impedance
- Fault scenarios such as loss of IPROPI pin function, load impedance change as well as comparator failures.

The device tries to maintain the current level during these scenarios, while keeping a count of each abnormal regulation path. Warning flags are only raised if the abnormal behavior exceeds “8” PWM cycles. A normal consecutive “16” PWM cycle operation resets all the warning counters.

The warning flags include -

- LS / HS SNS time out
- Ripple warning – Low / High

Copyright © 2026 Texas Instruments Incorporated

- Low current warning (current < target, even though LS is 100% on)
- Cycle skip warning
- Under current lock out warning (if UCLO_EN = 0)
- Device BIST warning
- Under Current Lock Out is the only path that results in an action of Hi-Z the driver (optional – enabled by UCLO_EN bit). Filter time (based on PWM cycles) for UCLO can be configured by UCLO_FAULT_FLTR. When UCLO_EN bit is disabled, UCLO warning is issued.
- Refer to PWM cycle based warnings under On-state diagnostics for more details

6.3.5.2 Fixed Frequency, Variable Duty Cycle Mode

Fixed frequency, variable duty cycle mode is selected by making CHx_CTRL_CONFIG = 0x0 and CHx_CTRL between 0x3 to 0x7.

Each output can be individually configured to drive the load in open loop with internal current regulation disabled at fixed frequency, selectable duty cycle.

- User can choose one of the preset duty cycle levels (0%, 25%, 50%, 75% or 100%)
- The frequency will be set by the configured PWM frequency (CHx_fC_PWM), refer to Table 6-9 for details.
- Dither settings will be determined by CHx_fSS_SEL, refer to Table 7-40 for details.
- Load current feedback through IPROPI pin is available
- The device is capable of accepting run-time duty cycle changes or switch to internal regulation using SPI command CMD1
- Short circuit protection and thermal protection are maintained
- Timer and PWM warnings as well as timer and duty cycle measurements are not valid

6.3.5.3 Fixed Duty Cycle, Variable Frequency Mode

Fixed duty cycle, variable frequency mode is selected by making CHx_CTRL_CONFIG = 0x1 and CHx_CTRL between 0x2 to 0x7.

Each output can be individually configured to drive the load in open loop with internal current regulation disabled at fixed duty cycle, selectable frequency.

- User can choose one of the preset PWM frequencies (10, 12, 14, 16, 18 or 20 kHz).
- Duty cycle will be fixed at 25%
- Dither settings will be determined by CHx_fSS_SEL, refer to Table 7-40 for details.
- Load current feedback through IPROPI pin is available
- The device is capable of accepting run-time frequency changes using SPI command CMD1
- Short circuit protection and thermal protection are maintained
- Timer and PWM warnings as well as timer and duty cycle measurements are not valid

6.3.5.4 Quick Turn Off

At any time during active operation (with or without internal regulation), the user can issue a SPI Hi-Z command or drive the EN/IN2 and DIS/EN2 to turn OFF the drivers.

- Two types of SPI commands are supported for turn OFF – CMD1 for a specific node addressed device in the SPI bus or CMD2 for all devices in the SPI bus (Broadcast command).
- Following the command, the device will briefly recirlculate the current to ensure that the load current is less than the hold target (HC) or lower hold ripple target (HCR-) and then turn off (Hi-Z) the driver with QTO clamping.
- The clamping will ensure a large voltage acorss the load to rapidly decay the load current.
- QTO start and done is detected by comparing the voltage on the output with respect to PVDD.
- Following QTO_DONE detection, there is a 1 ms wait before going to the STANDBY state.
- Depending on the user configured RETRY WAIT, an additional wait period is enforced as minimum cool off period even if the driver is commanded ON by the user.

Copyright © 2026 Texas Instruments Incorporated

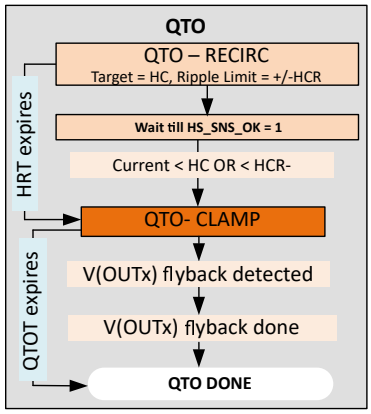


Figure 6-11. QTO

6.3.5.5 PWM Frequency

The device allows for a configurable PWM frequency set by register CHx_fC_PWM. In addition, it offers a spread spectrum feature (CHx_fSS_SEL) that adds a low frequency dither to the center PWM frequency. The spread percentage [0%, 5%, 10%, 20%] and type of dither (pseudo random vs triangular) is configurable.

Note

The PWM frequency set by CHx_fC_PWM is applicable in Internal Regulation Mode and Fixed Frequency, Variable Duty Cycle Mode.

Table 6-9. PWM Frequency Settings

CHx_fC_PWM	PWM center freq [Hz]	CHx_fC_PWM	PWM center freq [Hz]	CHx_fC_PWM	PWM center freq [Hz]	CHx_fC_PWM	PWM center freq [Hz]
0x0	500	0x8	8500	0x10	12500	0x18	16500
0x1	1000	0x9	9000	0x11	13000	0x19	17000
0x2	2000	0xA	9500	0x12	13500	0x1A	17500
0x3	4000	0xB	10000	0x13	14000	0x1B	18000
0x4	5000	0xC	10500	0x14	14500	0x1C	18500
0x5	6000	0xD	11000	0x15	15000	0x1D	19000
0x6	7000	0xE	11500	0x16	15500	0x1E	19500
0x7	8000	0xF	12000	0x17	16000	0x1F	20000

6.3.5.6 Minimum and Maximum Duty Cycle

The minimum and maximum PWM duty cycle depends on the slew settings, PWM frequency and PVDD voltage.

When duty cycle exceeds 50%, the device will maintain current regulation, but there might be sub-harmonic oscillations below the configured PWM fequency. This is especially valid while driving high resistance relay coils and low voltage supply. A simple estimation of the expected duty cycle is as follows:

Duty cycle = Hold current level / (Minimum PVDD level / Coil resitance)

If this estimation exceeds 43% and sub-harmonic oscillations are not desired, then slope compensation needs to be enabled (CHx_SLOPE_COMP_EN) with slope compensation time step size set by CHx_SLOPE_COMP.

During hold current regulation when slope compensation is enabled, once the duty cycle > 43%, the device will start reducing the target hold current by a count of 1 LSB of HC setting every CHx_SLOPE_COMP

Copyright © 2026 Texas Instruments Incorporated

count (assuming one PWM cycle ~1000 counts). While the device offers a wide range of this time step, it is recommended to start with a count of 50 and then emperically test to find the best setting.

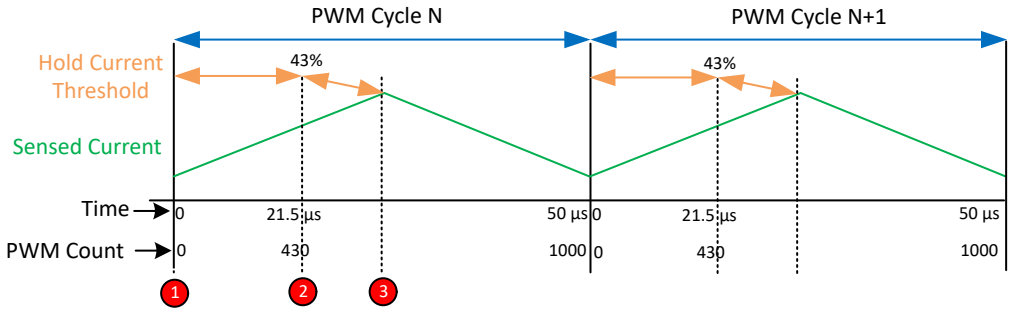


Figure 6-12. Slope Compensation

As shown in the diagram, starting at 43% duty, target hold current is reduced by an amount depending on the CHx_SLOPE_COMP count. For example, if the CHx_SLOPE_COMP is 50, the holding current threshold will be reduced by 1 code from 430 to 480 PWM count.

While slope compensation will help stabilizing load current at higher duty cycle operation, there are certain limitations of this implementation:

- Aggressive slope compensation (such as CHx_SLOPE_COMP < 16) leads to small time steps and large dI/dt for slope compensation, which causes a small error in the average load current. This needs to be corrected to raise the hold current value.
- Slope compensation may not be effective for hold current setting < 5 as there is not enough margin to reduce target current (dI is too small, so dI/dt for slope compensation is almost negligible).
- Slope compensation is disabled for hold current setting (CHx_HC) > 164.

6.3.6 EN/EN1 and DIS/EN2 pins

The device has two dedicated pins for secondary shut off to Hi-Z the driver. Both pins have an internal pull-down resistance to GND. PIN_CONFIG settings determines the function of the two pins as summarized below.

Table 6-10. EN/EN1 and DIS/EN2 Pin Settings

EN/EN1	DIS/EN2	PIN_CONFIG = 0x0	EN/EN1	DIS/EN2	PIN_CONFIG = 0x1
Lo	Lo	Both outputs Hi-Z	Lo	Lo	Both outputs Hi-Z
Lo	Hi	Both outputs Hi-Z	Lo	Hi	Output 1 Hi-Z, Output 2 controlled by SPI CMD
Hi	Lo	Both outputs controlled by SPI CMD	Hi	Lo	Output 1 controlled by SPI CMD, Output 2 Hi-Z
Hi	Hi	Both outputs Hi-Z	Hi	Hi	Both outputs controlled by SPI CMD

Note

- With PIN_CONFIG = 0b (default), EN/EN1 pin has to be driven high externally to turn ON the drivers, but DIS/EN2 pin can be left floating if not needed.
- For pin triggered turn-on or turn-off, the user can program a delay before the request is processed using the CHx_PIN_TURNON_DLY and CHx_PIN_TURNOFF_DLY.

6.3.7 Diagnostics Features

This section describes the On and Off state diagnostics features in the DRV3946-Q1.

6.3.7.1 On State Diagnostics

When internal regulation is enabled in the ACTIVE state, the device can detect abrupt changes in the load impedance or supply conditions or IPROPI resistor value that may result in loss of driver control.

Copyright © 2026 Texas Instruments Incorporated

6.3.7.1.1 PWM Cycle Warnings

During internal regulation, the device monitors the PWM cycle for the following:

- Low side sense time out warning
- High side sense time out (High duty cycle) warning
- Low current warning
- Upper ripple threshold warning (configurable CHx_RIPPLE_THRS)
- Lower ripple threshold warning
- PWM Cycle skip warning
- UCLO warning during hold regulation (configurable CHx_UCLO_THRS, UCLO_FAULT_FLTR)
- Internal PWM BIST warning

The warnings are issued on Section 7.1.5 and Section 7.1.6 registers for each output respectively with seperate record for peak and hold current regulation. The DRV3946-Q1 will continue to drive in the event of the warnings. Also the warnings can be individually disabled.

6.3.7.1.2 Timer Based Warnings

The device measures the following ramp times and issues warning for min/max time violation:

- Ramp up time to peak current (flag CHx_PRT_W)
- Ramp down time from peak to hold current (flag CHx_HRT_W)
- QTO (Clamping) time (flag CHx_QTOT_W)

The conditions for the time violation are described in Section 7.1.3 and Section 7.1.4 sections.

Note

The measured times are also recorded in the measurement registers. Average duty cycle measurement is also provided. Refer Measurement registers for details.

6.3.7.2 Off-state Diagnostics

In STANDBY state, the device asserts a current sink I_{OLP_PD} on OUTx to GND and compares the voltage drop on OUTx with respect to PVDD with an internal reference. This reference level is configurable. In case of a voltage drop greater than the reference is sensed, which can happen if the OUTx node is OPEN or shorted to GND, CHx_OFF_DIAG_STAT warning is set, indicating loss of relay control.

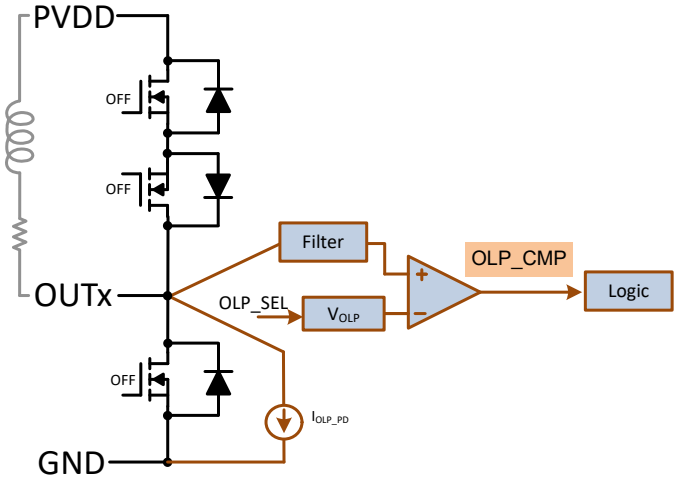


Figure 6-13. Off-state Diagnostics

Note

The device can't differentiate between short to GND and open on OUTx, as in both cases OLP_COMP = 0b. So only one bit is used for reporting as means to report loss of control. Also, the off-state diagnostics assumes that the external HS shut off switch on PVDD (if present) is enabled.

6.3.8 nFAULT/NAD Pin

The nFAULT/NAD pin is a dual purpose open-drain pin with an external pull up resistor. This pin is used for node address (NAD) determination during the device power-up initialization and then for fault or device STATE communication (asserted low) during operation.

The device node address (NAD) is set with an external pull up resistor. Four unique addresses can be set with 5.6, 12, 27, and 56 kΩ resistors (R_{LVL}).

The nFAULT/NAD pin can be setup to indicate different fault conditions. Refer to the nFAULT_CONFIG register for which faults are asserted on the nFAULT/NAD pin and how these can be configured.

6.3.9 Fault Table

This section describes the various device protection and diagnostic functions including the configuration options, response options, and recovery options. Detailed safety mechanism (SM) descriptions, classifications, and detection coverage can be found in the device safety manual.

Table 6-11. Fault Table

Fault Event	Safety Mechanism	Device State	CONFIG	nFAULT Assertion	SPI Indication	Driver function	Reaction	Recovery
SPI Watchdog Violation	SM_SPI_WD	Standby, Active	SPI_WD_DIS = 1	No	None	None	None	None
		Standby	SPI_WD_DIS = 0	Yes if nFAULT_CONFIG[1] = 1	SPI_WD_W	None	None	CLR FAULT command
		Active	SPI_WD_DIS = 0, SPI_WD_SHUTOFF_EN= 0	Yes if nFAULT_CONFIG[1] = 1	SPI_WD_W	None	None	CLR FAULT command
		Active	SPI_WD_DIS = 0, SPI_WD_SHUTOFF_EN= 1	Yes if nFAULT_CONFIG[1] = 1 or nFAULT_CONFIG[3] = 1	SPI_WD_W, CHx_STAT	Both outputs Hi-Z	None	CLR FAULT command. Driver is activated without CLR FAULT on changing SPI_WD_SHUTOFF_EN from 1 to 0, nFAULT remains low till CLR FAULT
VDD under voltage	SM_VDD_UV	Standby, Active	None	No	VDD_ERR on SDO	None	SDI is still valid	Auto recovery
VDD over voltage	SM_VDD_OV	Standby	None	No	VDD_ERR on SDO	None	SDI is still valid	Auto recovery
		Active	VDD_OV_SHUTOFF_EN = 0	No	VDD_ERR on SDO	None	SDI is still valid	Auto recovery
		Active	VDD_OV_SHUTOFF_EN = 1	Yes if nFAULT_CONFIG[3] = 1	VDD_ERR on SDOx, CHx_STAT (after VDD recovery)	Both outputs Hi-Z	SDI is still valid	CLR FAULT command

Copyright © 2026 Texas Instruments Incorporated

Table 6-11. Fault Table (continued)

Indeterminate node address due to NAD resistance out of range	SM_NAD_MON	INIT2	None	No	NAD_ERR on SDO	None	None	RE_INIT_NAD,NAD_OVERRIDE broadcast command. Connect proper NAD resistor and then issue RE_INIT_NAD command.
Indeterminate node address due to SDO conflict detection	SM_NAD_MON	Standby	None	No	NAD_ERR on SDO	None	None	RE_INIT_NAD,NAD_OVERRIDE broadcast command
		Active	None	No	NAD_ERR on SDO	None	None	RE_INIT_NAD,NAD_OVERRIDE broadcast command. From INIT2 state, device goes to active state without clear fault.
SPI Command CRC violation or incorrect frame length	SM_SPI_CMD_CRC, SM_SPI_ERR	Standby, Active	None	No	SPI_ERR	None	Ignored SPI frame	Proper write/read command
CRC violation of CONFIG registers	SM_CONFIG_CRC	Except INIT1	None	No	CONFIG_x_CRC_W	None	Register updates accepted	Write to checksum register with proper CRC
Power on reset	SM_V5_S_POR	Standby, Active	None	No	POR, CONFIG_x_CRC_W	Both outputs Hi-Z	None	CLR FAULT command
IPROPI resistor range violation	SM_IPROPI_MON	INIT2	None	No	CHx_RIPROPI_W	None	None	Make RIPROPI_W_BYPASS bit 1b, then CLR FAULT command
Off-state load impedance check	SM_OLP_MON	Standby	CHx_OLP_DIS = 0	Yes if nFAULT_CONFIG[3] = 1	CHx_OFF_DIAG_STAT	None	None	CLR FAULT command
		Standby	CHx_OLP_DIS = 1	No	None	None	None	None
Minimum peak ramp time violation	None	Active	PC_DIS = 0, PRT_MIN_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PRT_W	None	None	CLR FAULT command
		Active	PC_DIS = 0, PRT_MIN_W_DIS = 1	No	None	None	None	None

Copyright © 2026 Texas Instruments Incorporated

Table 6-11. Fault Table (continued)

Maximum peak ramp time violation	None	Active	PC_DIS = 0, PRT_MAX_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PRT_W	None	Device goes to next state after timeout. CHx_PRT register reads PT time.	CLR FAULT command
		Active	PC_DIS = 0, PRT_MAX_W_DIS = 1	No	None	None	None	None
Minimum hold ramp time violation	None	Active	HRT_MIN_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_HRT_W	None	None	CLR FAULT command
		Active	HRT_MIN_W_DIS = 1	No	None	None	None	None
Maximum hold ramp time violation	None	Active	HRT_MAX_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_HRT_W	None	Device goes to next state after timeout. CHx_HRT register reads maximum HRT threshold time.	CLR FAULT command
		Active	HRT_MAX_W_DIS = 1	No	None	None	None	None
Minimum QTO time violation	SM_MIN_QTO_MON	Active	QTOT_MIN_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_QTOT_W	None	None	CLR FAULT command
		Active	QTOT_MIN_W_DIS = 1	No	None	None	None	None
Maximum QTO time violation	SM_MAX_QTO_MON	Active	QTOT_MAX_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_QTOT_W	None	Device goes to next state after timeout. CHx_QTOT register reads maximum QTOT threshold time.	CLR FAULT command
		Active	QTOT_MAX_W_DIS = 1	No	None	None	None	None
Maximum QTO start time violation	None	Active	None	No	None	None	Device goes to next state after timeout. CHx_QTOST register reads maximum QTOST time.	None

Copyright © 2026 Texas Instruments Incorporated

Table 6-11. Fault Table (continued)

Ripple - Low threshold violation	SM_RIPPLE_MON_L	Active	RIPPLE_L_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PC_RIPPLE_LOW_W CHx_HC_RIPPLE_LOW_W	None	None	CLR FAULT command
		Active	RIPPLE_L_W_DIS = 1 or PC_PWM_W_DIS = 1 (peak regulation)	No	None	None	None	None
Ripple - High threshold violation	SM_RIPPLE_MON_H	Active	RIPPLE_H_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PC_RIPPLE_HIGH_W CHx_HC_RIPPLE_HIGH_W	None	None	CLR FAULT command
		Active	RIPPLE_H_W_DIS = 1 or PC_PWM_W_DIS = 1 (peak regulation)	No	None	None	None	None
Time out - HS SNS OK not registered before end of PWM period	SM_HS_SNS_OK	Active	HS_SNS_TO_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PC_HS_SNS_TO_W CHx_HC_HS_SNS_TO_W	None	None	CLR FAULT command
		Active	HS_SNS_TO_DIS = 1 or PC_PWM_W_DIS = 1 (peak regulation)	No	None	None	None	None
Time out - LS SNS OK not registered before end of PWM period	SM_LS_SNS_OK	Active	LS_SNS_TO_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PC_LS_SNS_TO_W CHx_HC_LS_SNS_TO_W	None	None	CLR FAULT command
		Active	LS_SNS_TO_DIS = 1 or PC_PWM_W_DIS = 1 (peak regulation)	No	None	None	None	None
Current less than target current though LS ON 100%	None	Active	LOW_CUR_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PC_LOW_CURR_W CHx_HC_LOW_CURR_W	None	None	CLR FAULT command
		Active	LOW_CUR_W_DIS = 1 or PC_PWM_W_DIS =1 (peak regulation)	No	None	None	None	None

Copyright © 2026 Texas Instruments Incorporated

Table 6-11. Fault Table (continued)

Cycle Skipping due to HS SNS current > target at start of PWM cycle	None	Active	CYCLE_SKIP_W_DIS = 0	Yes if nFAULT_CONFIG[0] = 1	CHx_PC_CYCLE_SKIP_W CHx_HC_CYCLE_SKIP_W	None	None	CLR FAULT command
		Active	PWM_CYCLE_SKIP_DIS = 1	No	None	None	None	None
		Active	CYCLE_SKIP_W_DIS = 1 or PC_PWM_W_DIS =1 (peak regulation)	No	None	None	None	None
PVDD under voltage - warning level	SM_PVDD_UV	Standby	PVDD_UV_W_DIS = 0	Yes if nFAULT_CONFIG[2] = 1	PVDD_UV	None	None	CLR FAULT command
		Standby	PVDD_UV_W_DIS = 1	No	None	None	None	None
		Active	PVDD_UV_W_DIS = 0	Yes if nFAULT_CONFIG[2] = 1	PVDD_UV	Fixed duty regulation	None	CLR FAULT command
		Active	PVDD_UV_W_DIS = 1	No	None	Fixed duty regulation	None	None
PVDD under voltage	SM_PVDD_UV	Standby	None	Yes if nFAULT_CONFIG[2] = 1	PVDD_UV	None	None	CLR FAULT command
	SM_PVDD_UV	INIT1, INIT2	None	No	SDO VDD_ERR	None	None	None
	SM_PVDD_UV_QTO	Active	None	Yes if nFAULT_CONFIG[2] = 1 or nFAULT_CONFIG[3] = 1	CHx_STAT, PVDD_UV	Both outputs Hi-Z	None	CLR FAULT command
PVDD over voltage - warning level	SM_PVDD_OV	Standby, Active	PVDD_OV_W_DIS = 0	Yes if nFAULT_CONFIG[2] = 1	PVDD_OV	None	t_{OCP} forced to lower setting	CLR FAULT command
		Standby, Active	PVDD_OV_W_DIS = 1	No	None	None	None	None
PVDD over voltage - shutdown level	SM_PVDD_OV	Standby	NA	Yes if nFAULT_CONFIG[2] = 1	PVDD_OV	None	None	CLR FAULT command
		INIT1, INIT2	None	No	SDO VDD_ERR	None	None	None
		Active	PVDD_OV_SHUTOFF_EN = 0	Yes if nFAULT_CONFIG[2] = 1	PVDD_OV	None	None	CLR FAULT command
		Active	PVDD_OV_SHUTOFF_EN = 1	Yes if nFAULT_CONFIG[2] = 1 or nFAULT_CONFIG[3] = 1	PVDD_OV, CHx_STAT	Both outputs Hi-Z	Low-side clamp for QTO	CLR FAULT command

Copyright © 2026 Texas Instruments Incorporated

Table 6-11. Fault Table (continued)

Over Current violation on Output x LS path (OCP_LS)	SM_LS_OCP	Active (LSON)	None	Yes if nFAULT_CONFIG[3] = 1	CHx_STAT	Affected output Hi-Z	None	CLR FAULT command
Over Current violation on Output x HS path (OCP_HS)	SM_HS_OCP	Active (RECIRC)	None	Yes if nFAULT_CONFIG[3] = 1	CHx_STAT	Affected output Hi-Z	None	CLR FAULT command
Under current violation (UCLO)	SM_UCLO	Active (LSON)	UCLO_EN = 0	No	CHx_UCLO_W	None	None	CLR FAULT command
		Active (LSON)	UCLO_EN = 1	Yes if nFAULT_CONFIG[3] = 1	CHx_STAT, CHx_UCLO_W	Affected output Hi-Z	None	CLR FAULT command
Over Temperature violation (TSD)	SM_TSD	Active	None	Yes if nFAULT_CONFIG[2] = 1 or nFAULT_CONFIG[3] = 1	CHx_STAT, OT	Both outputs Hi-Z	None	CLR FAULT command
Over Temperature warning (OTW)	SM_OTW	Standby, Active	OT_W_DIS = 0	Yes if nFAULT_CONFIG[2] = 1	OT	None	Switch to highest SR, if OT_W_ACTION = 1	CLR FAULT command
		Standby, Active	OT_W_DIS = 1	No	None	None	None	None
Safety layer - V5_S UV or OV	SM_V5_S_UV, SM_V5_S_OV	Standby, Active	None	Yes	SDO Hi-Z, DEV_ERR set, but cannot be read	Both outputs Hi-Z	Secondary logic timeout	Power cycle
Safety layer - f_{OSC} violation (high or low or stuck)	SM_OSC_MON	Standby, Active, INIT1, INIT2	None	Yes	SDO Hi-Z, DEV_ERR set, but cannot be read	Both outputs Hi-Z	Secondary logic timeout	Power cycle
Safety layer - Digital BIST failure	SM_LOGIC_BIST	INIT1	None	Yes	SDO Hi-Z, DEV_ERR set, but cannot be read	Both outputs Hi-Z	Secondary logic timeout	Power cycle
Safety layer - Memory BIST failure	SM_MEM_BIST	INIT1	None	Yes	SDO Hi-Z, DEV_ERR set, but cannot be read	Both outputs Hi-Z	Register updates accepted in TI factory test mode	Power cycle
Analog power-up BIST failure	SM_ABIST	INIT2	None	No	STARTUP_BIST_W	None	None	CLR FAULT command
PWM BIST violation	SM_PWM_BIST	Active	None	Yes if nFAULT_CONFIG[0] = 1	CHx_PC_PWM_BIST_W, CHx_HC_PWM_BIST_W	None	None	CLR FAULT command

Copyright © 2026 Texas Instruments Incorporated

6.3.10 Programming

6.3.10.1 SPI Interface

The device has a 4-wire, 24 bit SPI follower serial interface protocol. The SPI bus is used to set device configurations, operating parameters, and read out diagnostic information of the device. The device SPI operates in peripheral mode and connects to a central controller. The SPI input data (SDI) consists of 24 bits, with an 8-bit header and 16-bit data. The SPI output data (SDO) word consists of a read-back of the data received (SDI) and specific address data for a read command. Data on SDI is captured on the falling edge of SCLK and data on SDO is propagated on the rising edge of SCLK. For most typical MCUs this is mode 1 (CPOL = 0, CPHA = 1).

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low (to enable data transmission) and from low to high (to end data transmission).
- The nSCS pin should be pulled high inbetween each 24-bit frame transmission.
- Each frame must be exactly 24 SCLKs, else the frame will be discarded as an invalid frame and SPI_ERR will be flagged in the next frame transmission.
- Data on SDI is captured on the falling edge of SCLK and data on SDO is propagated on the rising edge of SCLK.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins will be ignored and the SDO pin will be placed in the Hi-Z state.
- The most significant bit (MSB) is shifted in and out first.

6.3.10.2 Addressable SPI

The device supports an optional addressable SPI format to enable up to four devices to operate off the same chip select pin (nSCS). This also allows the usage of special broadcast commands that can enable all devices on the shared addressed bus to take certain actions simultaneously and to minimize pins required to interact with multiple devices.

When using the CMD2 broadcast command, the SDI data is delivered to all devices on the same addressable SPI bus. The SDO response is limited to a single device and the responding device is set with the node address bits (A6, A5) in the SDI frame.

If not using the addressable SPI function, the nFAULT/NAD pin pullup resistor can be set to the default address (00) by using the 5.6 kΩ pull-up resistor value. The SPI then functions as a normal SPI by always setting the address bits A6 = 0b, and A5 = 0b.

During power up initialization, the device self assigns a node address (device address) that is based on the pull-up impedance on the nFAULT/NAD pin to VDD (see Table 6-12 for values). This address is mapped to the two MSBs of the 8 bit header (A6, B5) used in the SPI frame. This enables the user to assign an unique address to each driver (up to four drivers) using the node address feature on the nFAULT/NAD pin. Once initialized, the controller can access any specific register in any of the addressed devices with a single 24-bit frame. After initialization, this pin is then used for nFAULT assertion (open drain, active low) during normal device operation.

Table 6-12. nFAULT/NAD pin Pull-up Resistor

A6	A5	Resistor to VDD on nFAULT/NAD Pin
0	0	5.6 kΩ
0	1	12 kΩ
1	0	27 kΩ
1	1	56 kΩ

6.3.10.3 SPI Error Indicators

The SPI protocol provides a function to indicate certain SPI errors directly in the SDO response. Four different types of errors are provided and described below.

Copyright © 2026 Texas Instruments Incorporated

- **VDD_ERR:** The leading bit of the SDO response is used to signal VDD_ERR. The error could occur due to a VDD undervoltage (loss of VDD) or VDD overvoltage on any of the devices on the SPI bus. During power-up initialization (INIT1, INIT2), this field also indicates PVDD under voltage or PVDD over voltage.
- **NAD_ERR:** Failure to identify the node address (resistor out of range or device bias issues during initialization) or data conflict during SDO transmission results in a NAD_ERR condition. The second leading bit of the SDO response is used to signal NAD_ERR and for the remainder of the response SDO is disabled (Hi-Z). The error could occur due to NAD_ERR sensed by any of the devices on the SPI bus. Controller can resolve the NAD_ERR condition using the broadcast commands RE_INIT_NAD, NAD_OVERRIDE, or ASSIGNED_NAD. After power up, the NAD address is latched and does not change (unless commanded by the user).
- **SPI_ERR:** The device signals the rejection of an SPI frame by asserting the SPI_ERR bit (third leading bit on SDO response) high in the next SPI frame. This is also referred to as out-of-frame signaling. The remainder of the SDO response proceeds as normal. SPI_ERR could occur due to an incorrect number of SCLK edges when nSCS is low (device expects exactly 24) or a Command CRC mismatch.
- **DEV_ERR:** In the event of an error detected through the various device self-test (BIST) and power-up monitors the device signals a device error in the SDO response by keeping the SDI pin Hi-Z.

6.3.10.4 SPI Format

There are three different types of 24-bit SPI operations.

- **Read**: Read back register data from addressed location. The 8-bit header consists of a 2-bit device address, 5-bit register address, and 1-bit to indicate read (0x1 in B16). The 16-bit data is don't cares and can be set as "0"s.
- **Write**: Modify register contents at addressed location. The 8-bit header consists of a 2-bit device address, 5-bit register address, and 1-bit to indicate write (0x0 in B16). The 16-bit data consists of the data to write into the addressed register.
- **Command**: Special write commands with CRC8 protection. The 8-bit header consists of a 2-bit device address, 5-bit register address, and 1-bit to indicate write (0x0 in B16). This is followed by an 8-bit command byte and then an 8-bit CRC byte. The CRC is taken of the combined header plus command bytes (B23-B8). The CRC polynomial is 0x97, and initial value is 0xFF. The device accepts the command only when the CRC (lowest byte) matches the CRC calculated from the leading two bytes of the frame, else the frame is ignored and SPI_ERR bit is set.

The leading bits of SDO are used to indicated specific errors.

Table 6-13. SPI Read Format

SPI Read		Header Byte								Data Bye - MSB								Data Byte - LSB							
		B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SDI	Read	A6	A5	A4	A3	A2	A1	A0	1	All "0"s															
SDO	Normal	Hi-Z		0	A4	A3	A2	A1	A0	DATA[15:0] from addressed location															
	SPI_ERR	Hi-Z		1	A4	A3	A2	A1	A0	DATA[15:0] from addressed location															
	VDD_ERR	0	Hi-Z																						
	NAD_ERR	Hi-Z	0	Hi-Z																					
	DEV_ERR	Hi-Z																							

Table 6-14. SPI Write Format

SPI Write		Header Byte								Data Bye - MSB								Data Byte - LSB							
		B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SDI	Write	A6	A5	A4	A3	A2	A1	A0	0	New DATA[15:0] for addressed location															
SDO	Normal	Hi-Z		0	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	SPI_ERR	Hi-Z		1	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	VDD_ERR	0	Hi-Z																						
	NAD_ERR	Hi-Z	0	Hi-Z																					
	DEV_ERR	Hi-Z																							

Copyright © 2026 Texas Instruments Incorporated

Table 6-15. SPI Command Write Format

SPI Command		Header Byte								Data Bye - MSB								Data Byte - LSB							
		B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SDI	Command	A6	A5	A4	A3	A2	A1	A0	0	COMMAND[15:8]								CRC8[7:0] of bits B23-B8. Polynomial = 0x97							
SDO	Normal	Hi-Z		0	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	SPI_ERR	Hi-Z		1	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	VDD_ERR	0	Hi-Z																						
	NAD_ERR	Hi-Z	0	Hi-Z																					
	DEV_ERR	Hi-Z																							

Table 6-16. SPI Command Read Format

SPI Command		Header Byte								Data Bye - MSB								Data Byte - LSB							
		B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SDI	Command	A6	A5	A4	A3	A2	A1	A0	1	COMMAND[15:8]								CRC8[7:0] of bits B23-B8. Polynomial = 0x97							
SDO	Normal	Hi-Z		0	A4	A3	A2	A1	A0	DATA[15:0] from addressed location															
	SPI_ERR	Hi-Z		1	A4	A3	A2	A1	A0	DATA[15:0] from addressed location															
	VDD_ERR	0	Hi-Z																						
	NAD_ERR	Hi-Z	0	Hi-Z																					
	DEV_ERR	Hi-Z																							

The SPI_ERR corresponds to the SPI frame error from previous frame. The leading two bits on SDO are used to indicate SPI communcation failure on any of the devices. This includes VDD_ERR and NAD_ERR.

6.3.10.5 SPI Watchdog Monitor

The device has a SPI watchdog monitor which gets reset after any valid SPI frame. Reaction to a SPI watchdog violation is configurable between shut-off or inform only (SPI_WD_SHUTOFF_EN).

Copyright © 2026 Texas Instruments Incorporated

7 Register Maps

The device has five sets of register types: status (STATUS), measurement (MEAS), configuration A (CONFIG_A), configuration B (CONFIG_B) and command (CMD). The register maps for these are shown below with detailed register descriptions following.

Table 7-1. Status (STATUS) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
1h	STATUS0	NAD		POR	EN/ EN1_PIN_STAT	DIS/ EN2_PIN_STAT	nFAULT_PIN_STAT	DEVICE_ERR	WARNINGS
		CH1_OFF_DIAG_STAT	CH1_STAT			CH2_OFF_DIAG_STAT	CH2_STAT		
2h	STATUS1	NAD		EN/ EN1_PIN_STAT	EN/ EN1_PIN_STAT	DEVICE_ID		RSVD	PVDD_UV
		PVDD_OV	OT	SPI_WD_W	STARTUP_BIST_W	CH1_RIPROPI_W	CH2_RIPROPI_W	CONFIG_A_CRC_W	CONFIG_B_CRC_W
3h	STATUS2	NAD		CH1_PRT_W		CH1_QTOT_W		CH1_HRT_W	
		RSVD							
4h	STATUS3	NAD		CH2_PRT_W		CH2_QTOT_W		CH2_HRT_W	
		RSVD							
Ah	STATUS4	CH1_UCLO_W	CH1_PC_CYCLE_SKIP_W	CH1_PC_RIPPLE_HIGH_W	CH1_PC_RIPPLE_LOW_W	CH1_PC_HS_SNS_TO_W	CH1_PC_LOW_CURR_W	CH1_PC_LS_SNS_TO_W	RSVD
		RSVD	CH1_HC_CYCLE_SKIP_W	CH1_HC_RIPPLE_HIGH_W	CH1_HC_RIPPLE_LOW_W	CH1_HC_HS_SNS_TO_W	CH1_HC_LOW_CURR_W	CH1_HC_LS_SNS_TO_W	CH1_PWM_BIST_W
Bh	STATUS5	CH2_UCLO_W	CH2_PC_CYCLE_SKIP_W	CH2_PC_RIPPLE_HIGH_W	CH2_PC_RIPPLE_LOW_W	CH2_PC_HS_SNS_TO_W	CH2_PC_LOW_CURR_W	CH2_PC_LS_SNS_TO_W	RSVD
		RSVD	CH2_HC_CYCLE_SKIP_W	CH2_HC_RIPPLE_HIGH_W	CH2_HC_RIPPLE_LOW_W	CH2_HC_HS_SNS_TO_W	CH2_HC_LOW_CURR_W	CH2_HC_LS_SNS_TO_W	CH2_PWM_BIST_W

Table 7-2. Measurement (MEAS) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
5h	MEAS0	CH1_DC							
		CH2_DC							
6h	MEAS1	CH1_PRT							
		CH1_HRT							
7h	MEAS2	CH1_QTOST							
		CH1_QTOT							
8h	MEAS3	CH2_PRT							
		CH2_HRT							
9h	MEAS4	CH2_QTOST							
		CH2_QTOT							
Ch	MEAS5	CH1_RIPROPI							
		CH1_VIPROPI							
Dh	MEAS6	CH2_RIPROPI							
		CH2_VIPROPI							

Table 7-3. Configuration A (CONFIG_A) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
10h	CONFIG_A0	CH1_PC							
		CH1_HC							
11h	CONFIG_A1	CH2_PC							
		CH2_HC							
12h	CONFIG_A2	RSVD		CH1_UCLO_THRS		RSVD	CH1_RIPPLE_THRS		
		PWM_CYCLE_SKIP_DIS	RSVD	CH2_UCLO_THRS		CYCLE_SKIP_W_DIS	CH2_RIPPLE_THRS		
13h	CONFIG_A3	VDD_OV_FLTR		VDD_UV_FLTR		PVDD_OV_FLTR		PVDD_UV_FLTR	
		PT1				PT2			

Copyright © 2026 Texas Instruments Incorporated

Table 7-3. Configuration A (CONFIG_A) Register Map (continued)

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
14h	CONFIG_A4	CH1_SLOPE_COMP_EN	PIN_CONFIG	OCP_FLTR	UCLO_FAULT_FLTR			QTOT_MAX_THRS	
		QTOT_MIN_THRS		PRT_MIN_THRS		HRT_MAX_THRS		HRT_MIN_THRS	
15h	CONFIG_A5	nFAULT_CONFIG				CH1_PIN_TURNON_DLY			CH1_PIN_TURNOFF_DLY[2]
		CH1_PIN_TURNOFF_DLY[1:0]		CH2_PIN_TURNON_DLY			CH2_PIN_TURNOFF_DLY		
16h	CONFIG_A6	CH1_SLOPE_COMP							
		CONFIG_A_CRC8							

Table 7-4. Configuration B (CONFIG_B) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
17h	CONFIG_B0	VDD_OV_SHUTOFF_EN	RSVD	RETRY_WAIT_SEL			SPI_WD_SEL		PC_REG_DIS
		RSVD	UCLO_EN	PVDD_OV_SHUTOFF_EN	SPI_WD_SHUTOFF_EN	OT_W_ACTION	OLP_SEL		
18h	CONFIG_B1	PVDD_OV_W_DIS	OT_W_DIS	SPI_WD_DIS	QTOT_MAX_W_DIS	QTOT_MIN_W_DIS	PRT_MAX_W_DIS	PRT_MIN_W_DIS	HRT_MAX_W_DIS
		HRT_MIN_W_DIS	PC_PWM_W_DIS	LS_SNS_TO_DIS	HS_SNS_TO_DIS	RIPPLE_U_W_DIS	RIPPLE_L_W_DIS	LOW_CUR_W_DIS	PVDD_UV_W_DIS
19h	CONFIG_B2	CH1_fSS_SEL_TYPE	CH1_fSS_SEL		CH1_fC_PWM				
		CH2_fSS_SEL_TYPE	CH2_fSS_SEL		CH2_fC_PWM				
1Ah	CONFIG_B3	DIS_SSC	CP_SSC_CTRL	STARTUP_ABIST_BYPASS	CH1_OLP_DIS	CH2_OLP_DIS	RSVD	RIPROPI_W_BYPASS	CH2_SLOPE_COMP_EN
		CH2_SLOPE_COMP							
1Bh	CONFIG_B4	RSVD						CH1_CTRL_CONFIG	CH2_CTRL_CONFIG
		CONFIG_B_CRC8							

Table 7-5. Command (CMD) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
1Ch	CMD0	SR_SEL			RETRY_WAIT_DIS	PC_DIS1	PC_DIS2	FORCE_BIST	
1Dh	CMD1	CLR_FAULT	LOCK_CONFIG	CH1_CTRL			CH2_CTRL		
1Eh	CMD2 (Broadcast)	CLR_FAULT	RE_INIT	NAD_OVERRIDE	ASSIGNED_NAD		CHs_CTRL		

Copyright © 2026 Texas Instruments Incorporated

7.1 STATUS Registers

The device has 12 bytes of STATUS registers (Read only) at 6 address locations.

Table 7-6 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in Table 7-6 should be considered as reserved locations and the register contents should not be modified.

Table 7-6. STATUS Registers

Address	Acronym	Register Name	Section
1h	STATUS0	Summary of device, output, and input pin status.	Section 7.1.1
2h	STATUS1	Input pin, SPI, BIST, RIPROPI and power supply status.	Section 7.1.2
3h	STATUS2	Timing parameter warning status for output 1.	Section 7.1.3
4h	STATUS3	Timing parameter warning status for output 2.	Section 7.1.4
Ah	STATUS4	PWM cycle warnings for output 1.	Section 7.1.5
Bh	STATUS5	PWM cycle warnings for output 2.	Section 7.1.6

Complex bit access types are encoded to fit into small table cells. Table 7-7 shows the codes that are used for access types in this section.

Table 7-7. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 STATUS0 Register (Address = 1h) [Reset = 2500h]

STATUS0 is shown in Table 7-8.

Return to the Summary Table.

Global status register including fault and warning summary indicators for device and output status. Also includes input pin status.

Table 7-8. STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15-14	NAD	R	0x0	Device Node Address for SPI communication, determined based on pull-up resistor value on nFAULT/NAD pin	• 0x0: NAD Address = 0 • 0x1: NAD Address = 1 • 0x2: NAD Address = 2 • 0x3: NAD Address = 3
13	POR	R	0x1	Power-on Reset indicator. Bit is latched during power up till CLR_FAULT command.	• 0x0 = No POR • 0x1 = Prior POR event
12	EN/EN1_PIN_STAT	R	0x0	Transparent pin status indicator	• 0x0 = Pin low • 0x1 = Pin high
11	DIS/EN2_PIN_STAT	R	0x0	Transparent pin status indicator	• 0x0 = Pin low • 0x1 = Pin high
10	nFAULT_PIN_STAT	R	0x1	Transparent pin status indicator	• 0x0 = Pin low (nFAULT asserted) • 0x1 = Pin high

Copyright © 2026 Texas Instruments Incorporated

Table 7-8. STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
9	DEV_ERR	R	0x0	SDO response is Hi-Z in case of DEVICE_ERR. Device operation is disabled with outputs in Hi-Z. A power cycle (internal logic reset) is needed to clear this. This bit should always read low during operation.	
8	WARNINGS	R	0x1	Warning indicator (OR of warning bits in STATUS1 to STATUS5 registers). Read the other STATUS registers for the exact warning flag. Warnings flags are latched till CLR_FAULT command, but outputs are operational as commanded.	• 0x0 = No warning • 0x1 = Warning indication
7	CH1_OFF_DIAG_STAT	R	0x0	Output 1 off-state diagnostics status. In the event of a short to GND or OPEN detection, bit is latched till CLR_FAULT command.	• 0x0 = Normal load • 0x1 = Loss of control (Short to GND or Open)
6-4	CH1_STAT	R	0x0	Output 1 status. In the event of a shut off, output is locked out in Hi-Z and bit is latched till CLR_FAULT command.	• 0x0 = Commanded OFF • 0x1 = Commanded ON, Normal operation • 0x2 = Commanded ON, Shut OFF due to TSD • 0x3 = Commanded ON, Shut OFF due to OCP_LS • 0x4 = Commanded ON, Shut OFF due to OCP_HS • 0x5 = Commanded ON, Shut OFF due to PVDD UV • 0x6 = Commanded ON, Shut OFF due to UCLO (Enabled by UCLO_EN) • 0x7 = Commanded ON, Shut OFF due to PVDD OV (Enabled by PVDD_OV_SHUTOFF_EN) or VDD OV (Enabled by VDD_OV_SHUTOFF_EN) or due to SPI WD (Enabled by SPI_WD_SHUTOFF_EN)
3	CH2_OFF_DIAG_STAT	R	0x0	Output 2 off-state diagnostics status. In the event of a short to GND or OPEN detection, bit is latched till CLR_FAULT command.	• 0x0 = Normal load • 0x1 = Loss of control (Short to GND or Open)
2-0	CH2_STAT	R	0x0	Output 2 status. In the event of a shut off, output is locked out in Hi-Z and bit is latched till CLR_FAULT command.	• 0x0 = Commanded OFF • 0x1 = Commanded ON, Normal operation • 0x2 = Commanded ON, Shut OFF due to TSD • 0x3 = Commanded ON, Shut OFF due to OCP_LS • 0x4 = Commanded ON, Shut OFF due to OCP_HS • 0x5 = Commanded ON, Shut OFF due to PVDD UV • 0x6 = Commanded ON, Shut OFF due to UCLO (Enabled by UCLO_EN) • 0x7 = Commanded ON, Shut OFF due to PVDD OV (Enabled by PVDD_OV_SHUTOFF_EN) or VDD OV (Enabled by VDD_OV_SHUTOFF_EN) or due to SPI WD (Enabled by SPI_WD_SHUTOFF_EN)

Copyright © 2026 Texas Instruments Incorporated

7.1.2 STATUS1 Register (Address = 2h) [Reset = 0803h]

STATUS1 is shown in Table 7-9.

Return to the Summary Table.

Status register including EN/EN1 pin status, SPI CRC error, device ID, PVDD OV and UV monitors, and RIPROPI monitor.

Table 7-9. STATUS1 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15-14	NAD	R	0x0	Device Node Address for SPI communication, determined based on pull-up resistor value on nFAULT/NAD pin	• 0x0: NAD Address = 0 • 0x1: NAD Address = 1 • 0x2: NAD Address = 2 • 0x3: NAD Address = 3
13	EN/EN1_PIN_STAT	R	0x0	Copy of STATUS0, bit 12	• 0x0 = Pin low • 0x1 = Pin high
12	EN/EN1_PIN_STAT	R	0x0	Copy of STATUS0, bit 12	• 0x0 = Pin low • 0x1 = Pin high
11-10	DEVICE_ID	R	0x2	Unique device identity. 0x2 for production samples	
9	RSVD	R	0x0	Reserved	
8	PVDD_UV	R	0x0	PVDD undervoltage flag (If warning is enabled, bit will be set at the warning threshold). Bit is latched till CLR_FAULT command.	• 0x0 = No PVDD undervoltage flag • 0x1 = PVDD undervoltage flag
7	PVDD_OV	R	0x0	PVDD overvoltage flag (If warning is enabled, bit will be set at the warning threshold). Bit is latched till CLR_FAULT command.	• 0x0 = No PVDD overvoltage flag • 0x1 = PVDD overvoltage flag
6	OT	R	0x0	Over temperature flag (If warning is enabled, bit will be set at the warning threshold). Bit is latched till CLR_FAULT command.	• 0x0 = No OT flag • 0x1 = OT flag
5	SPI_WD_W	R	0x0	SPI watchdog warning. Bit is latched till CLR_FAULT command.	• 0x0 = No watchdog warning • 0x1 = Watchdog warning
4	STARTUP_BIST_W	R	0x0	Device start up ABIST failure warning. Bit is latched till fault exists. In case of a fault, user needs to issue REINIT_NAD command to re-trigger test (bypass with STARTUP_ABIST_BYPASS if needed). During the first power-up, device will NOT exit INIT2 state till fault is cleared.	• 0x0 = No ABIST failure warning • 0x1 = ABIST failure warning
3	CH1_RIPROPI_W	R	0x0	Resistor on IPROPI1 pin used for output 1 Out-of-Range warning or indeterministic due to PVDD UV. Bit is latched till fault exists. In case of a fault, user needs to issue REINIT_NAD command to re-trigger test (bypass with RIPROPI_W_BYPASS if needed). Device will NOT exit INIT2 state till fault is cleared.	• 0x0 = No RIPROPI out-of-range warning • 0x1 = RIPROPI out-of-range warning
2	CH2_RIPROPI_W	R	0x0	Resistor on IPROPI2 pin used for output 2 Out-of-Range warning or indeterministic due to PVDD UV. Bit is latched till fault exists. In case of a fault, user needs to issue REINIT_NAD command to re-trigger test (bypass with RIPROPI_W_BYPASS if needed). Device will NOT exit INIT2 state till fault is cleared.	• 0x0 = No RIPROPI out-of-range warning • 0x1 = RIPROPI out-of-range warning
1	CONFIG_A_CRC_W	R	0x1	CRC mismatch warning for CONFIG_A space. Bit is latched till next CONFIG_A CRC register write.	

Copyright © 2026 Texas Instruments Incorporated

Table 7-9. STATUS1 Register Description (continued)

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
0	CONFIG_B_CRC_W	R	0x1	CRC mismatch warning for CONFIG_B space. Bit is latched till next CONFIG_B CRC register write.	

7.1.3 STATUS2 Register (Address = 3h) [Reset = 0000h]

STATUS2 is shown in Table 7-10.

Return to the Summary Table.

Status register including timing parameter warning status for output 1.

Table 7-10. STATUS2 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15-14	NAD	R	0x0	Device Node Address for SPI communication, determined based on pull-up resistor value on nFAULT/NAD pin	• 0x0: NAD Address = 0 • 0x1: NAD Address = 1 • 0x2: NAD Address = 2 • 0x3: NAD Address = 3
13-12	CH1_PRT_W	R	0x0	Peak ramp duration warning for output 1. Bit is latched till CLR_FAULT command.	• 0x0 = Within threshold • 0x1 = Minimum threshold violation set by PRT_MIN_THRS • 0x2 = Maximum threshold violation set by CH1_PT • 0x3 = Not used
11-10	CH1_QTOT_W	R	0x0	Quick Turn Off (Clamping) duration warning for output 1. Bit is latched till CLR_FAULT command.	• 0x0 = Within threshold • 0x1 = Minimum threshold violation set by QTOT_MIN_THRS • 0x2 = Maximum threshold violation set by QTOT_MAX_THRS • 0x3 = Not used
9-8	CH1_HRT_W	R	0x0	Hold ramp duration warning for output 1. Bit is latched till CLR_FAULT command.	• 0x0 = Within threshold • 0x1 = Minimum threshold violation set by HRT_MIN_THRS • 0x2 = Maximum threshold violation set by HRT_MAX_THRS • 0x3 = Not used
7-0	RSVD	R	0x0	Reserved	Reserved

Copyright © 2026 Texas Instruments Incorporated

7.1.4 STATUS3 Register (Address = 4h) [Reset = 0000h]

STATUS3 is shown in Table 7-11.

Return to the Summary Table.

Status register including timing parameter warning status for output 2.

Table 7-11. STATUS3 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15-14	NAD	R	0x0	Device Node Address for SPI communication, determined based on pull-up resistor value on nFAULT/NAD pin	• 0x0: NAD Address = 0 • 0x1: NAD Address = 1 • 0x2: NAD Address = 2 • 0x3: NAD Address = 3
13-12	CH2_PRT_W	R	0x0	Peak ramp duration warning for output 2. Bit is latched till CLR_FAULT command.	• 0x0 = Within threshold • 0x1 = Minimum threshold violation set by PRT_MIN_THRS • 0x2 = Maximum threshold violation set by CH2_PT • 0x3 = Not used
11-10	CH2_QTOT_W	R	0x0	Quick Turn Off (Clamping) duration warning for output 2. Bit is latched till CLR_FAULT command.	• 0x0 = Within threshold • 0x1 = Minimum threshold violation set by QTOT_MIN_THRS • 0x2 = Maximum threshold violation set by QTOT_MAX_THRS • 0x3 = Not used
9-8	CH2_HRT_W	R	0x0	Hold ramp duration warning for output 2. Bit is latched till CLR_FAULT command.	• 0x0 = Within threshold • 0x1 = Minimum threshold violation set by HRT_MIN_THRS • 0x2 = Maximum threshold violation set by HRT_MAX_THRS • 0x3 = Not used
7-0	RSVD	R	0x0	Reserved	Reserved

Copyright © 2026 Texas Instruments Incorporated

7.1.5 STATUS4 Register (Address = Ah) [Reset = 0000h]

STATUS4 is shown in Table 7-12.

Return to the Summary Table.

STATUS4 register includes PWM cycle warning status for output 1.

Table 7-12. STATUS4 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15	CH1_UCLO_W	R	0x0	Under current lock out warning	• 0x0 = No UCLO warning • 0x1 = UCLO warning
14	CH1_PC_CYCLE_SKIP_W	R	0x0	Cycle skip warning during peak current regulation	• 0x0 = No PC Cycle skip warning • 0x1 = PC Cycle skip warning
13	CH1_PC_RIPPLE_HIGH_W	R	0x0	Ripple high warning during peak current regulation	• 0x0 = No PC Ripple high warning • 0x1 = PC Ripple high warning
12	CH1_PC_RIPPLE_LOW_W	R	0x0	Ripple low warning during peak current regulation	• 0x0 = No PC Ripple low warning • 0x1 = PC Ripple low warning
11	CH1_PC_HS_SNS_TO_W	R	0x0	High side sense time out warning during peak current regulation	• 0x0 = No PC HS sense time out warning • 0x1 = PC HS sense time out warning
10	CH1_PC_LOW_CURR_W	R	0x0	Low current warning during peak current regulation	• 0x0 = No PC low current warning • 0x1 = PC Low current warning
9	CH1_PC_LS_SNS_TO_W	R	0x0	Low side sense time out warning during peak current regulation	• 0x0 = No PC LS sense time out warning • 0x1 = PC LS sense time out warning
8	CH1_PWM_BIST_W	R	0x0	PWM comparator BIST warning during peak current regulation	• 0x0 = No PC PWM BIST warning • 0x1 = PC PWM BIST warning
7	RSVD	R	0x0	Reserved	
6	CH1_HC_CYCLE_SKIP_W	R	0x0	Cycle skip warning during hold current regulation	• 0x0 = No HC Cycle skip warning • 0x1 = HC Cycle skip warning
5	CH1_HC_RIPPLE_HIGH_W	R	0x0	Ripple high warning during hold current regulation	• 0x0 = No HC Ripple high warning • 0x1 = HC Ripple high warning
4	CH1_HC_RIPPLE_LOW_W	R	0x0	Ripple low warning during hold current regulation	• 0x0 = No HC Ripple low warning • 0x1 = HC Ripple low warning
3	CH1_HC_HS_SNS_TO_W	R	0x0	High side sense time out warning during hold current regulation	• 0x0 = No HC HS sense time out warning • 0x1 = HC HS sense time out warning
2	CH1_HC_LOW_CURR_W	R	0x0	Low current warning during hold current regulation	• 0x0 = No HC low current warning • 0x1 = HC Low current warning
1	CH1_HC_LS_SNS_TO_W	R	0x0	Low side sense time out warning during hold current regulation	• 0x0 = No HC LS sense time out warning • 0x1 = HC LS sense time out warning
0	CH1_PWM_BIST_W	R	0x0	PWM comparator BIST warning during hold current regulation	• 0x0 = No HC PWM BIST warning • 0x1 = HC PWM BIST warning

Copyright © 2026 Texas Instruments Incorporated

7.1.6 STATUS5 Register (Address = Bh) [Reset = 0000h]

STATUS5 is shown in Table 7-13.

Return to the Summary Table.

STATUS5 register includes PWM cycle warning status for output 2.

Table 7-13. STATUS5 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15	CH2_UCLO_W	R	0x0	Under current lock out warning	• 0x0 = No UCLO warning • 0x1 = UCLO warning
14	CH2_PC_CYCLE_SKIP_W	R	0x0	Cycle skip warning during peak current regulation	• 0x0 = No PC Cycle skip warning • 0x1 = PC Cycle skip warning
13	CH2_PC_RIPPLE_HIGH_W	R	0x0	Ripple high warning during peak current regulation	• 0x0 = No PC Ripple high warning • 0x1 = PC Ripple high warning
12	CH2_PC_RIPPLE_LOW_W	R	0x0	Ripple low warning during peak current regulation	• 0x0 = No PC Ripple low warning • 0x1 = PC Ripple low warning
11	CH2_PC_HS_SNS_TO_W	R	0x0	High side sense time out warning during peak current regulation	• 0x0 = No PC HS sense time out warning • 0x1 = PC HS sense time out warning
10	CH2_PC_LOW_CURR_W	R	0x0	Low current warning during peak current regulation	• 0x0 = No PC low current warning • 0x1 = PC Low current warning
9	CH2_PC_LS_SNS_TO_W	R	0x0	Low side sense time out warning during peak current regulation	• 0x0 = No PC LS sense time out warning • 0x1 = PC LS sense time out warning
8	CH2_PWM_BIST_W	R	0x0	PWM comparator BIST warning during peak current regulation	• 0x0 = No PC PWM BIST warning • 0x1 = PC PWM BIST warning
7	RSVD	R	0x0	Reserved	
6	CH2_HC_CYCLE_SKIP_W	R	0x0	Cycle skip warning during hold current regulation	• 0x0 = No HC Cycle skip warning • 0x1 = HC Cycle skip warning
5	CH2_HC_RIPPLE_HIGH_W	R	0x0	Ripple high warning during hold current regulation	• 0x0 = No HC Ripple high warning • 0x1 = HC Ripple high warning
4	CH2_HC_RIPPLE_LOW_W	R	0x0	Ripple low warning during hold current regulation	• 0x0 = No HC Ripple low warning • 0x1 = HC Ripple low warning
3	CH2_HC_HS_SNS_TO_W	R	0x0	High side sense time out warning during hold current regulation	• 0x0 = No HC HS sense time out warning • 0x1 = HC HS sense time out warning
2	CH2_HC_LOW_CURR_W	R	0x0	Low current warning during hold current regulation	• 0x0 = No HC low current warning • 0x1 = HC Low current warning
1	CH2_HC_LS_SNS_TO_W	R	0x0	Low side sense time out warning during hold current regulation	• 0x0 = No HC LS sense time out warning • 0x1 = HC LS sense time out warning
0	CH2_PWM_BIST_W	R	0x0	PWM comparator BIST warning during hold current regulation	• 0x0 = No HC PWM BIST warning • 0x1 = HC PWM BIST warning

Copyright © 2026 Texas Instruments Incorporated

7.2 MEAS Registers

The device has 14 read only bytes of measurement registers at 7 address locations.

Table 7-14 lists the memory-mapped registers for the MEAS registers. All register offset addresses not listed in Table 7-14 should be considered as reserved locations and the register contents should not be modified.

Table 7-14. MEAS Registers

Offset	Acronym	Register Name	Section
5h	MEAS0	Average duty cycle measurement for both outputs.	Section 7.2.1
6h	MEAS1	Peak and hold ramp time measurement for output 1.	Section 7.2.2
7h	MEAS2	QTO start time and QTO time measurement for output 1.	Section 7.2.3
8h	MEAS3	Peak and hold ramp time measurement for output 2.	Section 7.2.4
9h	MEAS4	QTO start time and QTO time measurement for output 2.	Section 7.2.5
Ch	MEAS5	Resistance and voltage on IPROPI1 pin measurement.	Section 7.2.6
Dh	MEAS6	Resistance and voltage on IPROPI2 pin measurement.	Section 7.2.7

Complex bit access types are encoded to fit into small table cells. Table 7-15 shows the codes that are used for access types in this section.

Table 7-15. MEAS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2026 Texas Instruments Incorporated

7.2.1 MEAS0 Register (Address = 5h) [Reset = 0000h]

MEAS0 is shown in Table 7-16.

Return to the Summary Table.

Measurement register that provides average duty cycle measurement for both outputs.

Table 7-16. MEAS0 Register Description

Bit	Field	Type	Reset	Bit Description
15-8	CH1_DUTY_CYCLE	R	0x0	Measured 16-cycle average duty cycle for output 1. Auto-updated when data is requested. Cleared on the next ACTIVE cycle. % Average duty cycle = [Reg Value] x DC Scaling Factor. Scaling factor is set by CHx_fC_PWM, as shown in Table 7-17.
7-0	CH2_DUTY_CYCLE	R	0x0	Measured 16-cycle average duty cycle for output 2. Auto-updated when data is requested. Cleared on the next ACTIVE cycle. % Average duty cycle = [Reg Value] x DC Scaling Factor. Scaling factor is set by CHx_fC_PWM, as shown in Table 7-17.

Table 7-17. DC Scaling Factor

CHx_fC_PWM	DC Scaling Factor
0x5	0.48
0x10	0.50
0x11	0.52
0x12	0.54
0x6, 0x13	0.56
0x14	0.58
0x15	0.60
0x16	0.62
0x0, 0x1, 0x2, 0x3, 0x7, 0x17	0.64
0x18	0.66
0x8c, 0x19	0.68
0x1A	0.70
0x9, 0x1B	0.72
0x1C	0.74
0xA, 0x1D	0.76
0x1E	0.78
0x4, 0xB, 0x1F	0.80
0xC	0.84
0xD	0.88
0xE	0.92
0xF	0.96

Copyright © 2026 Texas Instruments Incorporated

7.2.2 MEAS1 Register (Address = 6h) [Reset = 0000h]

MEAS1 is shown in Table 7-18.

Return to the Summary Table.

Measurement register that provides peak and hold ramp time measurements for output 1.

Table 7-18. MEAS1 Register Description

Bit Field	Bit Field Name	Reset Value	Bit Description
15-8	CH1_PRT	0x0	Measured peak ramp time for output 1. Latched at the end of peak cycle. Cleared on the next ACTIVE cycle. Timer resolution is set by CHx_PT setting, as shown in Table 7-19 .
7-0	CH1_HRT	0x0	Measured hold ramp time for output 1. Latched at the end of hold ramp cycle. Cleared on the next ACTIVE cycle. Timer resolution is set by HRT_MAX_THRS setting, as shown in Table 7-20.

Table 7-19. CHx_PRT Timer Resolution

CHx_PT	PRT timer resolution (µs)	Maximum Count	Maximum Peak Ramp Time (ms)
0x0	102.4	156	16
0x1	102.4	234	24
0x2	204.8	156	32
0x3	204.8	195	40
0x4	204.8	234	48
0x5	409.6	136	56
0x6	409.6	156	64
0x7	409.6	175	72
0x8	409.6	195	80
0x9	409.6	214	88
0xA	409.6	234	96
0xB	409.6	253	104
0xC	819.2	136	112
0xD	819.2	146	120
0xE	819.2	156	128
0xF	1638.4	156	256

Table 7-20. HRT Timer Resolution

HRT_MAX_THRS	HRT timer resolution (ms)	Maximum Count	Maximum Hold Ramp Time (ms)
0x0	1.64	156	256
0x1	3.28	156	512
0x2	6.55	156	1024
0x3	13.11	156	2048

Copyright © 2026 Texas Instruments Incorporated

7.2.3 MEAS2 Register (Address = 7h) [Reset = 0000h]

MEAS2 is shown in Table 7-21.

Return to the Summary Table.

Measurement register that provides QTO start time and QTO time measurements for output 1.

Table 7-21. MEAS2 Register Description

Bit Field	Bit Field Name	Reset Value	Bit Description
15-8	CH1_QTOST	0x0	Measured QTO (Clamping) start time for output 1. Timer resolution = 6.4 µs. Maximum count is 156.
7-0	CH1_QTOT	0x0	Measured QTO (Clamping) time for output 1. Latched at the end of QTO event. Cleared on the next ACTIVE cycle. Timer resolution is set by QTOT_MAX_THRS setting, as shown in Table 7-22.

Table 7-22. QTOT Timer Resolution

QTOT_MAX_THRS	QTOT timer resolution (µs)	Maximum count	Maximum QTO time (ms)
0x0	25.6	156	4
0x1	51.2	156	8
0x2	102.4	156	16
0x3	204.8	156	32

7.2.4 MEAS3 Register (Address = 8h) [Reset = 0000h]

MEAS3 is shown in Table 7-23.

Return to the Summary Table.

Measurement register that provides peak and hold ramp time measurements for output 2.

Table 7-23. MEAS3 Register Description

Bit Field	Bit Field Name	Reset Value	Bit Description
15-8	CH2_PRT	0x0	Measured peak ramp time for output 2. Latched at the end of peak cycle. Cleared on the next ACTIVE cycle. Timer resolution is set by CHx_PT setting, as shown in Table 7-19.
7-0	CH2_HRT	0x0	Measured hold ramp time for output 2. Latched at the end of hold ramp cycle. Cleared on the next ACTIVE cycle. Timer resolution is set by HRT_MAX_THRS setting, as shown in Table 7-20.

7.2.5 MEAS4 Register (Address = 9h) [Reset = 0000h]

MEAS4 is shown in Table 7-24.

Return to the Summary Table.

Measurement register that provides QTO start time and QTO time measurements for output 2.

Table 7-24. MEAS4 Register Description

Bit Field	Bit Field Name	Reset Value	Bit Description
15-8	CH2_QTOST	0x0	Measured QTO (Clamping) start time for output 2. Timer resolution = 6.4 µs.
7-0	CH2_QTOT	0x0	Measured QTO (Clamping) time for output 2. Latched at the end of QTO event. Cleared on the next ACTIVE cycle. Timer resolution is set by QTOT_MAX_THRS setting, as shown in Table 7-22.

Copyright © 2026 Texas Instruments Incorporated

7.2.6 MEAS5 Register (Address = Ch) [Reset = 0000h]

MEAS5 is shown in Table 7-25.

Return to the Summary Table.

Measurement register that provides resistance and voltage on IPROPI1 pin.

Table 7-25. MEAS5 Register Description

Bit Field	Bit Field Name	Reset Value	Bit Description
15-8	CH1_RIPROPI	0x0	Resistance on IPROPI1 pin measured during initialization.
7-0	CH1_VIPROPI	0x0	Voltage on IPROPI1 pin measured during initialization based on forced I_{IPROPI}. Value = (Reg Value+17)/272 x 3V

7.2.7 MEAS6 Register (Address = Dh) [Reset = 0000h]

MEAS6 is shown in Table 7-26.

Return to the Summary Table.

Measurement register that provides resistance and voltage on IPROPI2 pin.

Table 7-26. MEAS6 Register Description

Bit Field	Bit Field Name	Reset Value	Bit Description
15-8	CH2_RIPROPI	0x0	Resistance on IPROPI2 pin measured during initialization.
7-0	CH2_VIPROPI	0x0	Voltage on IPROPI2 pin measured during initialization based on forced I_{IPROPI}. Value = (Reg Value+17)/272 x 3V

Copyright © 2026 Texas Instruments Incorporated

7.3 CONFIG A Registers

CONFIG A is set of 14 R/W bytes of configuration registers at 7 address locations, including a 8-bit CRC protection in the last location.

Table 7-27 lists the memory-mapped registers for the CONFIG A registers. All register offset addresses not listed in Table 7-27 should be considered as reserved locations and the register contents should not be modified.

Table 7-27. CONFIG A Registers

Address	Acronym	Register Name	Section
10h	CONFIG_A0	Peak and hold current setting for output 1.	Section 7.3.1
11h	CONFIG_A1	Peak and hold current setting for output 2.	Section 7.3.2
12h	CONFIG_A2	UCLO and ripple current setting for both outputs.	Section 7.3.3
13h	CONFIG_A3	OV and UV deglitch time setting and peak time setting for both outputs.	Section 7.3.4
14h	CONFIG_A4	Slope compensation configuration, input pin configuration, OCP and UCLO filter time, limits for peak and hold ramp time and QTO time.	Section 7.3.5
15h	CONFIG_A5	nFAULT configuration, pin turn on and off delays.	Section 7.3.6
16h	CONFIG_A6	Slope compensation for output 1 and CRC for CONFIG A.	Section 7.3.7

Complex bit access types are encoded to fit into small table cells. Table 7-28 shows the codes that are used for access types in this section.

Table 7-28. CONFIG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.3.1 CONFIG_A0 Register (Address = 10h) [Reset = C040h]

CONFIG_A0 is shown in Table 7-29.

Return to the Summary Table.

Configuration register to setup the peak and hold current settings for output 1.

Table 7-29. CONFIG_A0 Register Description

Bit	Field	Type	Reset	Bit Description
15-8	CH1_PC	R/W	0xC0	Peak current setting for output 1, set by (Reg Value + 17) / 272 x A_{IPROPI} x 3V / $R_{IPROPI1}$
7-0	CH1_HC	R/W	0x40	Hold current setting for output 1, set by (Reg Value + 17) / 272 x A_{IPROPI} x 3V / $R_{IPROPI1}$

7.3.2 CONFIG_A1 Register (Address = 11h) [Reset = C040h]

CONFIG_A1 is shown in Table 7-30.

Return to the Summary Table.

Configuration register to setup the peak and hold current settings for output 2.

Table 7-30. CONFIG_A1 Register Description

Bit	Field	Type	Reset	Bit Description
15-8	CH2_PC	R/W	0xC0	Peak current setting for output 2, set by (Reg Value + 17) / 272 x A_{IPROPI} x 3V / $R_{IPROPI2}$
7-0	CH2_HC	R/W	0x40	Hold current setting for output 2, set by (Reg Value + 17) / 272 x A_{IPROPI} x 3V / $R_{IPROPI2}$

7.3.3 CONFIG_A2 Register (Address = 12h) [Reset = 2424h]

CONFIG_A2 is shown in Table 7-31.

Return to the Summary Table.

Configuration register to setup the UCLO and ripple current setting for both outputs.

Table 7-31. CONFIG_A2 Register Description

Bit	Field	Type	Reset	Bit Description
15-14	RSVD	R	0x0	Reserved
13-12	CH1_UCLO_THRS	R/W	0x2	Under current lock out (UCLO) threshold for output 1 with respect to lower ripple threshold during hold current regulation. Refer Current Threshold section for setting values.
11	RSVD	R	0x0	Reserved
10-8	CH1_RIPPLE_THRS	R/W	0x4	Ripple current setting for output 1. Sets both the upper and lower ripple threshold with respect to the peak or hold current. Refer Current Threshold section for setting values.
7	PWM_CYCLE_SKIP_DIS	R/W	0x0	Internal regulation PWM cycle – Cycle skip path is ignored
6	RSVD	R	0x0	Reserved
5-4	CH2_UCLO_THRS	R/W	0x2	Under current lock out (UCLO) threshold for output 2 with respect to lower ripple threshold during hold current regulation. Refer Current Threshold section for setting values.
3	CYCLE_SKIP_W_DIS	R/W	0x0	Internal regulation PWM cycle – Reporting of cycle skip warning is disabled
2-0	CH2_RIPPLE_THRS	R/W	0x4	Ripple current setting for output 2. Sets both the upper and lower ripple threshold with respect to the peak or hold current. Refer Current Threshold section for setting values.

7.3.4 CONFIG_A3 Register (Address = 13h) [Reset = 0088h]

CONFIG_A3 is shown in Table 7-32.

Copyright © 2026 Texas Instruments Incorporated

Return to the Summary Table.

Configuration register to setup the OV and UV deglitch time setting and peak time setting for both outputs.

Table 7-32. CONFIG_A3 Register Description

Bit	Field	Type	Reset	Bit Description
15-14	VDD_OV_FLTR	R/W	0x0	VDD over voltage deglitch filter
13-12	VDD_UV_FLTR	R/W	0x0	VDD under voltage deglitch filter
11-10	PVDD_OV_FLTR	R/W	0x0	PVDD over voltage deglitch filter
9-8	PVDD_UV_FLTR	R/W	0x0	PVDD under voltage deglitch filter
7-4	CH1_PT	R/W	0x8	Peak time setting for output 1
3-0	CH2_PT	R/W	0x8	Peak time setting for output 2

7.3.5 CONFIG_A4 Register (Address = 14h) [Reset = 130Ch]

CONFIG_A4 is shown in Table 7-33.

Return to the Summary Table.

Register for slope compensation configuration, input pin configuration, OCP and UCLO filter time, limits for peak and hold ramp time and QTO time.

Table 7-33. CONFIG_A4 Register Description

Bit	Field	Type	Reset	Bit Description
15	CH1_SLOPE_COMP_EN	R/W	0x0	Enables slope compensation for output 1
14	PIN_CONFIG	R/W	0x0	EN/EN1 and DIS/EN2 pin configuration
13	OCP_FLTR	R/W	0x0	Over Current Protection (OCP) filter time, common for both outputs. In case of a PVDD over voltage event (> PVDDD_OV_W threshold), OCP filter time is forced to the smaller setting.
12-10	UCLO_FAULT_FLTR	R/W	0x4	Filter for UCLO detection, common for both outputs • 0x0 = 8 PWM cycles • 0x1 = 16 PWM cycles • 0x2 = 32 PWM cycles • 0x3 = 48 PWM cycles • 0x4 = 64 PWM cycles • 0x5 = 128 PWM cycles • 0x6 = 192 PWM cycles • 0x7 = 256 PWM cycles
9-8	QTOT_MAX_THRS	R/W	0x3	QTO (Clamping) time - maximum duration threshold, common for both outputs
7-6	QTOT_MIN_THRS	R/W	0x0	QTO (Clamping) time - minimum duration threshold, common for both outputs
5-4	PRT_MIN_THRS	R/W	0x0	Peak ramp time - minimum duration threshold, common for both outputs
3-2	HRT_MAX_THRS	R/W	0x3	Hold ramp time - maximum duration threshold, common for both outputs
1-0	HRT_MIN_THRS	R/W	0x0	Hold ramp time - minimum duration threshold, common for both outputs

Copyright © 2026 Texas Instruments Incorporated

7.3.6 CONFIG_A5 Register (Address = 15h) [Reset = 8000h]

CONFIG_A5 is shown in Table 7-34.

Return to the Summary Table.

Register for nFAULT configuration and pin turn on and off delays.

Table 7-34. CONFIG_A5 Register Description

Bit	Field	Type	Reset	Bit Description
15	nFAULT_CONFIG[3]	R/W	0x1	Enable assertion (nFAULT = low) if CHx_STAT > 0x1 when commanded ON or CHx_OFF_DIAG_STAT = 1 when commanded OFF. nFAULT is de-asserted by CLR_FLT command. DEV_ERR always causes assertion.
14	nFAULT_CONFIG[2]	R/W	0x0	Enable assertion (nFAULT = low) if PVDD or temperature warnings occur. nFAULT is de-asserted by CLR_FLT command. DEV_ERR always causes assertion.
13	nFAULT_CONFIG[1]	R/W	0x0	Enable assertion (nFAULT = low) if SPI_WD_W = 0x1. nFAULT is de-asserted by CLR_FLT command. DEV_ERR always causes assertion.
12	nFAULT_CONFIG[0]	R/W	0x0	Enable assertion (nFAULT = low) if there are PWM or timer warnings during internal current regulation. nFAULT is de-asserted by CLR_FLT command. DEV_ERR always causes assertion.
11-9	CH1_PIN_TURNON_DLY	R/W	0x0	Driver turn-on delay for output 1 when enabled by the pin
8-6	CH1_PIN_TURNOFF_DLY	R/W	0x0	Driver turn-off delay for output 1 when disabled by the pin
5-3	CH2_PIN_TURNON_DLY	R/W	0x0	Driver turn-on delay for output 2 when enabled by the pin
2-0	CH2_PIN_TURNOFF_DLY	R/W	0x0	Driver turn-off delay for output 2 when disabled by the pin

7.3.7 CONFIG_A6 Register (Address = 16h) [Reset = 0000h]

CONFIG_A6 is shown in Table 7-35.

Return to the Summary Table.

Register for configuring slope compensation for output 1 and CRC for CONFIG A.

Table 7-35. CONFIG_A6 Register Description

Bit	Field	Type	Reset	Bit Description
15-8	CH1_SLOPE_COMP	R/W	0x0	Slope compensation for CH1 – Count value (time) to reduce target current value by 1 code after 43% duty cycle. Number of steps (slope) ~ 570 / CHx_SLOPE_COMP value. 0x0 => Slope compensation disabled
7-0	CONFIG_A_CRC	R/W	0x0	Programmed CRC for CONFIG A space. Writing to this register triggers CRC check for CONFIG A space. CRC check takes 100 ns x no of bits (for flagging after CRC bits are incorrectly written or clearing after CRC bits are correctly written). The CRC polynomial is 0x97, and initial value is 0xFF.

Copyright © 2026 Texas Instruments Incorporated

7.4 CONFIG B Registers

CONFIG B is set of 10 R/W bytes of configuration registers at 5 address locations, including a 8-bit CRC protection in the last location.

Table 7-36 lists the memory-mapped registers for the CONFIG B registers. All register offset addresses not listed in Table 7-36 should be considered as reserved locations and the register contents should not be modified.

Table 7-36. CONFIG B Registers

Address	Acronym	Register Name	Section
17h	CONFIG_B0	Response to power supply overvoltage and undercurrent, forced wait duration, watchdog duration for SPI, off-state diagnostic comparator threshold setting.	Section 7.4.1
18h	CONFIG_B1	Disables reporting of various warnings.	Section 7.4.2
19h	CONFIG_B2	Type and amount of frequency dither and PWM center frequency setting.	Section 7.4.3
1Ah	CONFIG_B3	Spread spectrum setting, off-state diagnostic setting and slope compensation configuration for output 2.	Section 7.4.4
1Bh	CONFIG_B4	Configures CHx_CTRL bits.	Section 7.4.5

Complex bit access types are encoded to fit into small table cells. Table 7-37 shows the codes that are used for access types in this section.

Table 7-37. CONFIG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.4.1 CONFIG_B0 Register (Address = 17h) [Reset = 2623h]

CONFIG_B0 is shown in Table 7-38.

Return to the Summary Table.

Configuration register to setup the response to power supply overvoltage and undercurrent, forced wait duration, watchdog duration for SPI and off-state diagnostic comparator threshold setting.

Table 7-38. CONFIG_B0 Register Description

Bit	Field	Type	Reset	Bit Description
15	VDD_OV_SHUTOFF_EN	R/W	0x0	Hi-Z driver when a VDD OV condition is detected
14	RSVD	R	0x0	Reserved
13-11	RETRY_WAIT_SEL	R/W	0x4	Forced wait duration between driver turn-off and turn-on retry, common for both outputs
10-9	SPI_WD_SEL	R/W	0x3	Watchdog duration to detect any valid SPI read or write frames
8	PC_REG_DIS	R/W	0x0	Disable current regulation during peak time (LS ON 100%)
7	RSVD	R	0x0	Reserved
6	UCLO_EN	R/W	0x0	Hi-Z driver when load under current condition is detected
5	PVDD_OV_SHUTOFF_EN	R/W	0x1	Hi-Z driver when a PVDD OV condition is detected
4	SPI_WD_SHUTOFF_EN	R/W	0x0	Hi-Z driver for a SPI watchdog violation
3	OT_W_ACTION	R/W	0x0	Force SR_SEL = 0xF (max setting) when an OT_W is detected
2-0	OLP_SEL	R/W	0x3	Off-state diagnostic (OLP) comparator threshold setting

7.4.2 CONFIG_B1 Register (Address = 18h) [Reset = 0040h]

CONFIG_B1 is shown in Table 7-39.

Return to the Summary Table.

Configuration register to disable reporting of various warnings.

Table 7-39. CONFIG_B1 Register Description

Bit	Field	Type	Reset	Bit Description
15	PVDD_OV_W_DIS	R/W	0x0	Disable reporting of PVDD over voltage warning
14	OT_W_DIS	R/W	0x0	Disable reporting of over temperature warning
13	SPI_WD_DIS	R/W	0x0	Disable reporting of SPI watchdog warning
12	QTOT_MAX_W_DIS	R/W	0x0	Disable reporting of QTOT (clamping) maximum duration violation warning
11	QTOT_MIN_W_DIS	R/W	0x0	Disable reporting of QTOT (clamping) minimum duration violation warning
10	PRT_MAX_W_DIS	R/W	0x0	Disable reporting of Peak Ramp Time maximum duration violation warning
9	PRT_MIN_W_DIS	R/W	0x0	Disable reporting of Peak Ramp Time minimum duration violation warning
8	HRT_MAX_W_DIS	R/W	0x0	Disable reporting of Hold Ramp Time maximum duration violation warning
7	HRT_MIN_W_DIS	R/W	0x0	Disable reporting of Hold Ramp Time minimum duration violation warning
6	PC_PWM_W_DIS	R/W	0x1	Disable reporting of all PWM cycle warnings reporting for both outputs during peak cycle
5	LS_SNS_TO_DIS	R/W	0x0	Disable reporting of low side sense time out warning for both outputs during both peak and hold cycle
4	HS_SNS_TO_DIS	R/W	0x0	Disable reporting of high side sense time out warning for both outputs during both peak and hold cycle
3	RIPPLE_U_W_DIS	R/W	0x0	Disable reporting of ripple warning - upper threshold for both outputs during both peak and hold cycle
2	RIPPLE_L_W_DIS	R/W	0x0	Disable reporting of ripple warning - lower threshold for both outputs during both peak and hold cycle
1	LOW_CUR_W_DIS	R/W	0x0	Disable reporting of low current warning for both outputs during both peak and hold cycle
0	PVDD_UV_W_DIS	R/W	0x0	Disable reporting of PVDD under voltage warning

7.4.3 CONFIG_B2 Register (Address = 19h) [Reset = 0B0Bh]

CONFIG_B2 is shown in Table 7-40.

Return to the Summary Table.

Copyright © 2026 Texas Instruments Incorporated

Configuration register to set type and amount of frequency dither and PWM center frequency.

Table 7-40. CONFIG_B2 Register Description

Bit	Field	Type	Reset	Bit Description
15	CH1_fSS_SEL_TYPE	R/W	0x0	PWM frequency dither type selection for output 1 • 0x0 = Pseudo random dither • 0x1 = Triangular (512) dither
14-13	CH1_fSS_SEL	R/W	0x0	PWM frequency dither setting for spread spectrum for output 1 • 0x0 = No dither • 0x1 = Band of +/- 5% around fC_PWM • 0x2 = Band of +/- 10% around fC_PWM • 0x3 = Band of +/- 20% around fC_PWM
12-8	CH1_fC_PWM	R/W	0x0B	PWM center frequency setting for output 1
7	CH2_fSS_SEL_TYPE	R/W	0x0	PWM frequency dither type selection for output 2 • 0x0 = Pseudo random dither • 0x1 = Triangular (512) dither
6-5	CH2_fSS_SEL	R/W	0x0	PWM frequency dither setting for spread spectrum for output 2 • 0x0 = No dither • 0x1 = Band of +/- 5% around fC_PWM • 0x2 = Band of +/- 10% around fC_PWM • 0x3 = Band of +/- 20% around fC_PWM
4-0	CH2_fC_PWM	R/W	0x0B	PWM center frequency setting for output 2

7.4.4 CONFIG_B3 Register (Address = 1Ah) [Reset = 8000h]

CONFIG_B3 is shown in Table 7-41.

Return to the Summary Table.

Configuration register for spread spectrum setting, off-state diagnostic setting and slope compensation configuration for output 2.

Table 7-41. CONFIG_B3 Register Description

Bit	Field	Type	Reset	Bit Description
15	DIS_SSC	R/W	0x1	Disable SSC for the internal oscillators
14	CP_SSC_CTRL	R/W	0x0	Increase charge pump spread spectrum
13	STARTUP_ABIST_BYPASS	R/W	0x0	Bypass Startup ABIST failure from INIT2 to STANDBY state during powerup
12	CH1_OLP_DIS	R/W	0x0	Disable off-state diagnostics for output 1
11	CH2_OLP_DIS	R/W	0x0	Disable off-state diagnostics for output 2
10	RSVD	R	0x0	Reserved
9	RIPROPI_W_BYPASS	R/W	0x0	Bypass RIPROPIx_W failure from INIT2 to STANDBY state during powerup
8	CH2_SLOPE_COMP_EN	R/W	0x0	Enables slope compensation for output 2
7-0	CH2_SLOPE_COMP	R/W	0x0	Slope compensation for output 2 – Count value (time) to reduce target current value by 1 code after 43% duty cycle. Number of steps (slope) ~ 570 / CHx_SLOPE_COMP value. 0x0 => Slope compensation disabled

7.4.5 CONFIG_B4 Register (Address = 1Bh) [Reset = 0000h]

CONFIG_B4 is shown in Table 7-42.

Return to the Summary Table.

Copyright © 2026 Texas Instruments Incorporated

Configures CHx_CTRL bits.

Table 7-42. CONFIG_B4 Register Description

Bit	Field	Type	Reset	Bit Description
15-10	RSVD	R	0x0	Reserved
9	CH1_CTRL_CONFIG	R/W	0x0	Configures CH1_CTRL in CMD1 for run-time control using CH1_CTRL bits • 0x0 = Internal regulation/ vary duty cycle • 0x1 = Vary PWM frequency
8	CH2_CTRL_CONFIG	R/W	0x0	Configures CH2_CTRL in CMD1 for run-time control using CH2_CTRL bits • 0x0 = Internal regulation/ vary duty cycle • 0x1 = Vary PWM frequency
7-0	CONFIG_B_CRC	R/W	0x0	Programmed CRC for CONFIG B space. Writing to this register triggers CRC check for CONFIG B space. CRC check takes 100 ns x no of bits (for flagging after CRC bits are incorrectly written or clearing after CRC bits are correctly written). The CRC polynomial is 0x97, and initial value is 0xFF.

Copyright © 2026 Texas Instruments Incorporated

7.5 CMD Registers

Command registers are set of 3 special R/W bytes referred as commands. Write to these registers is protected with 8-bit CRC (bits 7 – 0). The device accepts the command ONLY when the transmitted CRC (lowest byte) matches the CRC calculated from the leading two bytes of the frame, else the frame is ignored and SPI_ERR bit is set.

The FORCE_BIST command is accepted only during device STANDBY state. The RE_INIT, NAD_OVERRIDE and ASSIGNED_NAD commands are accepted only during device INIT2 state.

Table 7-43 lists the memory-mapped registers for the CMD registers. All register offset addresses not listed in Table 7-43 should be considered as reserved locations and the register contents should not be modified.

Table 7-43. CMD Registers

Address	Acronym	Register Name	Section
1Ch	CMD0	General command.	Section 7.5.1
1Dh	CMD1	Action command.	Section 7.5.2
1Eh	CMD2	Broadcast command.	Section 7.5.3

Complex bit access types are encoded to fit into small table cells. Table 7-44 shows the codes that are used for access types in this section.

Table 7-44. CMD Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2026 Texas Instruments Incorporated

7.5.1 CMD0 Register (Address = 1Ch) [Reset = 8000h]

CMD0 is shown in Table 7-45.

Return to the Summary Table.

CMD0 register contains the general commands.

Table 7-45. CMD0 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15-13	SR_SEL	R/W	0x4	Slew rate setting for both outputs	• 0x0 = 3.25 V/µsec • 0x1 = 4.75 V/µsec • 0x2 = 7.75 V/µsec • 0x3 = 13 V/µsec • 0x4 = 18 V/µsec • 0x5 = 25 V/µsec • 0x6 = 34 V/µsec • 0x7 = 46 V/µsec
12	RETRY_WAIT_DIS	R/W	0x0	Disable RETRY wait time	
11	CH1_PC_DIS	R/W	0x0	Skip peak cycle regulation and go direct to hold cycle for output 1	
10	CH2_PC_DIS	R/W	0x0	Skip peak cycle regulation and go direct to hold cycle for output 2	
9-8	FORCE_BIST	R/W	0x0	System BIST features. Command is accepted ONLY during STANDBY state of operation, else ignored.	• 0x0 = No action • 0x1 = Assert nFAULT pin low till CLR_FAULT command • 0x2 = Force secondary logic time out till CLR_FAULT command • 0x3 = 10K Hz clock based on internal oscillator fOSC

Copyright © 2026 Texas Instruments Incorporated

7.5.2 CMD1 Register (Address = 1Dh) [Reset = 0000h]

CMD1 is shown in Table 7-46.

Return to the Summary Table.

CMD1 register contains the action commands.

Table 7-46. CMD1 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15	CLR_FAULT	R/W	0x0	Broadcast command to clear faults on all devices. Bit is auto cleared after the command has been registered.	
14	LOCK_CONFIG	R/W	0x0	Locks the user CONFIG (both A and B) space for device configuration	
13-11	CH1_CTRL	R/W	0x0	Output 1 control (*Valid only if CHs_CTRL in CMD2 register is not 0x4)	• CH1_CTRL_CONFIG = 0x0 – 0x0 = Shut off 0x1 = Shut off – 0x2* = Turn ON with internal current regulation – 0x3* = Force 100% duty cycle (internal regulation disabled) – 0x4*= Force 75% duty cycle (internal regulation disabled) – 0x5* = Force 50% duty cycle (internal regulation disabled) – 0x6* = Force 25% duty cycle (internal regulation disabled) – 0x7* = Force 0% duty cycle (internal regulation disabled) • CH1_CTRL_CONFIG = 0x1 (internal regulation disabled) – 0x0 = Shut off 0x1 = Shut off – 0x2* = Force fC_PWM to 20 KHz at 25% duty cycle – 0x3* = Force fC_PWM to 18 KHz at 25% duty cycle – 0x4* = Force fC_PWM to 16 KHz at 25% duty cycle – 0x5* = Force fC_PWM to 14 KHz at 25% duty cycle – 0x6* = Force fC_PWM to 12 KHz at 25% duty cycle – 0x7* = Force fC_PWM to 10 KHz at 25% duty cycle
10-8	CH2_CTRL	R/W	0x0	Output 2 control (*Valid only if CHs_CTRL in CMD2 register is not 0x4)	• CH2_CTRL_CONFIG = 0x0 – 0x0 = Shut off 0x1 = Shut off – 0x2* = Turn ON with internal current regulation – 0x3* = Force 100% duty cycle (internal regulation disabled) – 0x4*= Force 75% duty cycle (internal regulation disabled) – 0x5* = Force 50% duty cycle (internal regulation disabled) – 0x6* = Force 25% duty cycle (internal regulation disabled) – 0x7* = Force 0% duty cycle (internal regulation disabled) • CH2_CTRL_CONFIG = 0x1 (internal regulation disabled) – 0x0 = Shut off 0x1 = Shut off – 0x2* = Force fC_PWM to 20 KHz at 25% duty cycle – 0x3* = Force fC_PWM to 18 KHz at 25% duty cycle – 0x4* = Force fC_PWM to 16 KHz at 25% duty cycle – 0x5* = Force fC_PWM to 14 KHz at 25% duty cycle – 0x6* = Force fC_PWM to 12 KHz at 25% duty cycle – 0x7* = Force fC_PWM to 10 KHz at 25% duty cycle

Copyright © 2026 Texas Instruments Incorporated

7.5.3 CMD2 Register (Address = 1Eh) [Reset = 0000h]

CMD2 is shown in Table 7-47.

Return to the Summary Table.

CMD2 register contains the Broadcast commands. SDI message is applicable to all devices on the SPI bus. SDO is driven by the device addressed in the NAD Address bits [A6, A5] in the SDI frame.

Table 7-47. CMD2 Register Description

Bit	Field	Type	Reset	Bit Description	Bit Enumerations
15	CLR_FAULT	R/W	0x0	Broadcast command to clear faults on all devices. Bit is auto cleared after the command has been registered.	
14	RE_INIT	R/W	0x0	Broadcast command to re-initialize NAD on all devices. Write is accepted ONLY in the device INIT2 state, else command is ignored.	
13	NAD_OVERRIDE	R/W	0x0	When set, any device having a NAD error, clears NAD_ERR and picks up the address in the next two bits as their assigned NAD for SPI communication. Write is accepted ONLY during INIT2 state when NAD_ERR is detected and RE_INIT_NAD = 0.	
12-11	ASSIGNED_NAD	R/W	0x0	Assigned NAD for device with NAD error when NAD_OVERRIDE = 1	
10-8	CHs_CTRL	R/W	0x0	Peak current and hold current target update for both outputs (on-the fly current change) * Valid only when CHx_CTRL in CMD1 register = 0x2 (Internal regulation) ** Valid for any value in CHx_CTRL in CMD1 register	• 0x0 = No change • 0x1* = Add 16 codes to PC & HC register value, cap at 255 • 0x2* = Add 32 codes to PC & HC register value, cap at 255 • 0x3* = Add 64 codes to PC & HC register value, cap at 255 • 0x4** = Shut off • 0x5* = Subtract 16 codes to PC & HC register value, cap at 0 • 0x6* = Subtract 32 codes to PC & HC register value, cap at 0 • 0x7* = Subtract 64 codes to PC & HC register value, cap at 0

Copyright © 2026 Texas Instruments Incorporated

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV3946-Q1 is an integrated solenoid driver targeted at automotive EV contactor relay and solenoid control applications. The sections below will give some design guidelines on using the device.

8.2 Typical Application

The DRV3946-Q1 is intended to interact with an external controller directly or through a device serving as a communications bridge.

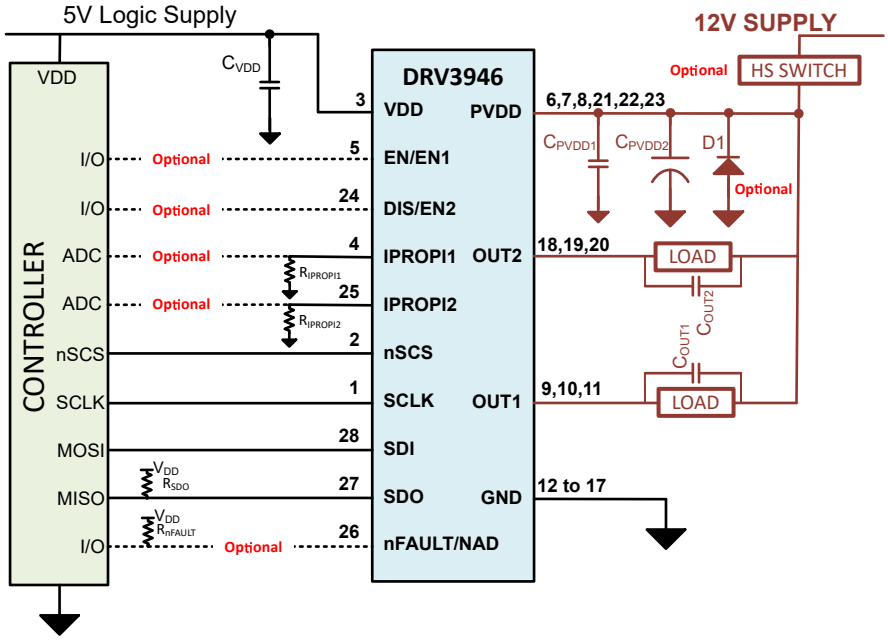


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
PVDD Power Supply	12 V (typical), but can utilize higher boosted supply voltages. Power dissipation and thermal limits should be observed.
VDD Power Supply	5 V, only supports 5 V input, external conversion to 3.3 V required for 3.3 V controller SDO interface.
nFAULT/NAD Pin	Refer to nFAULT/NAD Pin section

8.2.2 Transient Thermal Impedance and Current Capability

The following table summarizes the transient thermal resistance (Junction-to-ambient) for a sample 4 layer, 4cm x 4cm x 1.6mm PCB design with no additional heat sinking. The 4 layers uses 2oz copper on top and bottom

signal layers and 1 oz copper on internal supply layers, with 0.3mm thermal via drill diameter, 0.025mm Cu plating and 1mm via pitch.

Table 8-2. Transient Thermal Resistance

$R_{\theta JA}$ at 0.1 s (°C/W)	$R_{\theta JA}$ at 1 s (°C/W)	$R_{\theta JA}$ at 10 s (°C/W)	$R_{\theta JA}$ at DC (°C/W)
3.3	7.2	12.2	29.0

The transient current carrying capability per channel (assuming both channels are operating simultaneously) is summarized below, based on ambient temperature of 85 deg C (thermal GND). It is assumed that the waiting time between two successive QTO events is large, so that there is no residual temperature rise due to a previous QTO event. Switching losses have been estimated at PVDD = 13.5 V, PWM frequency = 20 kHz, Duty Cycle = 25% and Slew Rate = 12.6 V/µsec, using an approximation of PVDD x I x PVDD / SR x f_{PWM}.

Table 8-3. Transient Current Carrying Capability

I at 0.1 sec (A)	**I at 1 sec** (A)	**I at 10 sec** (A)	**I at DC** (A)
8.03	5.08	3.67	2.07

Note:

- Switching losses will limit the hold current at slower slew rates and higher PWM frequencies
- Peak current regulation is optional and can be disabled to avoid switching at higher currents that could cause thermal challenges

The following formula explains in detail the above example at DC or steady state condition:

At 85 deg C thermal ground, junction temperature rise budget = 65 deg C, to restrict junction temperature below 150 deg C.

Power Dissipation per channel on LS FET during charge

*= I^2 x LS RON**max** x DutyCycle*

= 2.07 ^{2} x 75 mohm x 25%

= 80.3 mW

Power Dissipation per channel on HS FET during recirc

*= I^2 x RECIRC RON**max** x (1-DutyCycle)*

= 2.07 ^{2} x 120 mohm x 75%

= 385.6 mW

Power Dissipation per channel on LS FET during PWM switching

= PVDD x I x PVDD/SlewRate x f_{PWM}

= 13.5 V x 2.07 x 13.5 V/ (12.6 V/µsec) x 20 kHz

= 598.8 mW

Total power dissipation per channel = 1064.7 mW

Switching loss / Total = 598.8 mW/ 1064.7 mW = 56%

Total power dissipation for both channels = 2 x 1064.7 mW = 2129.4 mW

At 29 deg C/W, this translate to junction heating of (29 deg C/W x 2.129 W) = 62 deg C.

Copyright © 2026 Texas Instruments Incorporated

8.2.3 Application Performance Plots

CH1 - nFAULT, CH5 - EN/EN1, CH2 - OUT1, CH4 - IPROPI1, CH8 - Load Current

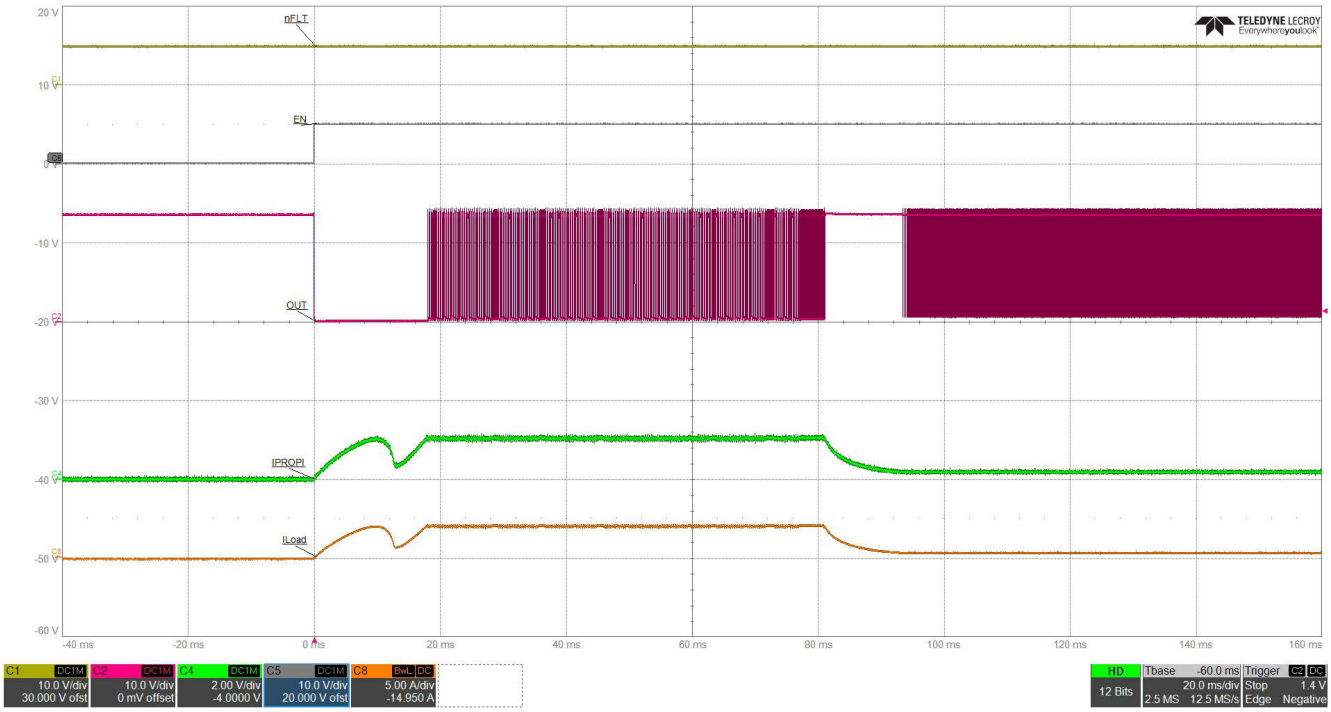


Figure 8-2. Relay turn-on, Peak and Hold current Regulation

CH1 - nFAULT, CH5 - EN/EN1, CH2 - OUT1, CH4 - IPROPI1, CH8 - Load Current

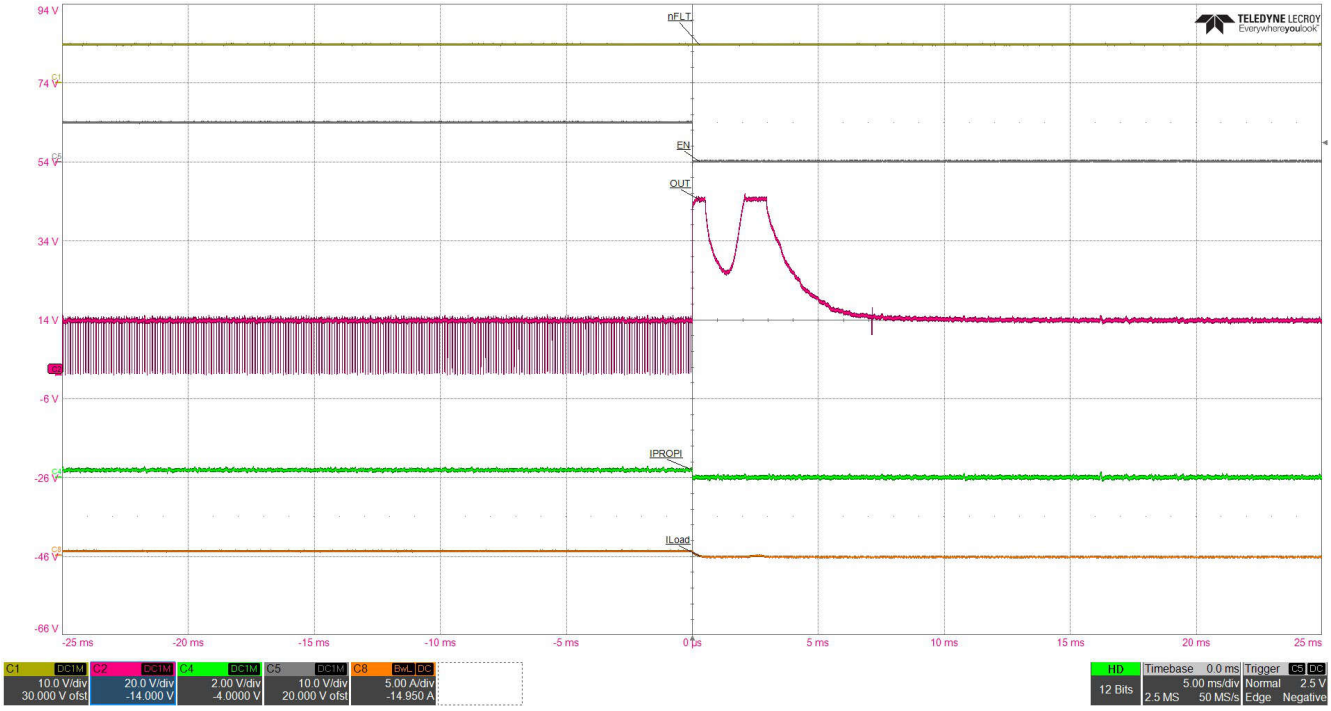


Figure 8-3. Quick Turn-off

8.2.4 PVDD Capacitance Value Estimation

Let us assume -

- Total 8 loads connected to four DRV3946-Q1 devices, with all loads energized together
- Load: L = 400 mH, R = 4 Ω
- Peak current I_{PC} = 1 A, Hold current I_{HC} = 0.5 A
- HS switch is shut off
- PVDD UV threshold = 5 V
- PVDD voltage clamp limit = - 1V
- OUTx LS passive clamp = 29 V

With these assumptions, we can derive the following -

- Voltage across load during clamp V_{CLAMP}= 29 – (-1) V = 30 V
- Clamping duration t_{CLAMP} = I x L / V_{CLAMP}
- For peak current, clamping duration t_{CLAMP} = 1 A x 0.4 H / 30 V = 13.3 ms
- For hold current, clamping duration t_{CLAMP} = 0.5 A x 0.4 H / 30 V = 6.67 ms
- Charge sourced from PVDD cap (Q_{PVDD}) = I X t_{CLAMP} / 2
  - For peak current, charge sourced from PVDD cap = 1 A x 13.3 ms / 2 = 6.67 mC
  - For hold, charge sourced from PVDD cap = 0.5 A x 6.67 ms / 2 = 1.67 mC
- Allowed delta voltage on PVDD cap = PVDD UV threshold – PVDD voltage clamp limit = 5 – (-1) = 6 V
- Cap on PVDD = N x QPVDD / ΔV
  - For peak , cap on PVDD = 8 x 6.67 mC / 6 V = 8.9 mF
  - For hold, cap on PVDD = 8 x 1.67 mC / 6 V = 2.2 mF

In this case, using a diode parallel to the PVDD cap of ~47 µF is more practical than a large capacitor. Diode current capability and thermal constraints should be considered. Alternate solution would be to replace the HS switch and the diode with a half-bridge driver device.

Copyright © 2026 Texas Instruments Incorporated

8.3 Initialization Setup

Recommended procedures for software development are listed below.

8.3.1 Device Initialization – NAD

1. WAIT - After PVDD and VDD ramp up, wait t_{READY} time
2. STATUS0_READ - Read STATUS0 of each one of the devices on the addressed SPI bus. A normal response would include
    a. Correct address and NAD values
    b. POR bit set
    c. WARNINGS bit set (due to CONFIG_CRC_W)
    d. Status of the EN/EN1 and DIS/EN2 pins = 0x0 (No data yet)
3. VDD_ERR - If the response indicates VDD_ERR, this indicates a power supply issue with any of the devices on the addressed SPI bus. Check the condition of VDD and PVDD supplies and repeat STATUS0_READ. The power-up initialization of the device is gated till supply monitor flags, PVDD_UV, VDD_OV and VDD_UV, are clear.
4. NAD_ERR - If the response indicates NAD_ERR, this indicates a NAD address determination issue with any of the devices on the addressed SPI bus. Check the pull-up resistor on nFAULT/NAD pin to VDD, followed by:
    a. Issue a broadcast command with INITIALIZE bit set
    b. Wait t_{READY} time
    c. Follow up with a broadcast command with INITIALIZE bit cleared. Response will include NAD_ERR and previous command content (command confirmation). If response still indicates a NAD_ERR, then refer to NAD_RECOVERY.
    d. Cycle back to SATUS0_READ
5. NO_RESPONSE – This would indicate one of the following:
    a. Device Error – nFAULT pin will be asserted low. A power cycle is needed to proceed.
    b. No device found on the addressed NAD. This indicates the NAD determination on this specific NAD is incorrectly mapped to the different NAD. In this case, refer to SDO_CONFLICT_CREATION below.
6. NAD_RECOVERY – Issue the following commands to force the NAD address
    a. Issue a broadcast command with FORCE_NAD bit set with intended NAD address. The device with NAD_ERR picks up this command and assigns itself the commanded NAD address.
    b. Follow up with a broadcast command with FORCE_NAD bit cleared. Response will include NAD_ERR and previous command content (command confirmation). NAD_ERR should be cleared.
    c. Cycle back to STATUS0_READ.
7. SDO_CONFLICT_CREATION – This procedure assumes that the hardware has the ability to assert EN/EN1 pin high or low individually to each device on the addressed SPI -
    a. Assert EN/EN1 pin high on device which is not responding, while asserting EN/EN1 pin low on all other devices on the addressed SPI.
    b. Read STATUS1 of the devices on the addressed SPI bus one by one.
    c. Since STATUS1 reads EN/EN1_PIN_STAT, the device with EN/EN1 high will detect an SDO conflict with the other device and back off transmitting on SDO with a NAD_ERR.
    d. Follow the NAD_RECOVERY steps to correct the NAD_ERR of the device which is not responding.

8.3.2 Device Initialization – Configuration

1. Calculate the CRC8 for the 13 bytes of CONFIG A and 9 bytes of CONFIG B
2. Write CONFIG_A0 to CONFIG_A6 to configure the device as needed along with the calculated CRC8 in CONFIG_A6 lower byte.

Copyright © 2026 Texas Instruments Incorporated

3. Similarly, write CONFIG_B0 top CONFIG_B4 to configure the device as needed along with the calculated CRC8 in CONFIG_B4 lower byte.
4. Read registers MEAS5 and MEAS6 to record the measured value of resistance on IPROPIx pin and voltage on IPROPIx pin observed with a forced current during INIT2
5. Issue a CLR_FAULT command and read STATUS0
6. A normal response would include
    a. Correct address and NAD values
    b. POR bit cleared
    c. WARNINGS bit cleared
    d. Correct status of the EN/EN1 and DIS/EN2 pins
7. The device will be in STANDBY state with the off-state diagnostics enabled.
8. It is recommended to issue CMD1 = 0x40 to set LOCK_CONFIG to prevent any inadvertent configuration register SPI write during operation.
9. Poll STATUS0 periodically to ensure CHx_OFF_DIAG_STAT = 0x0 (0x1 indicates loss of control)

8.3.3 System Initialization

Perform all the system initialization checks as needed at this point. Note that these tests are ONLY meant to be performed in the device STANDBY state. These include -

1. EN/EN1 and DIS/EN2 function check
2. Device timing check
3. nFAULT signaling check
4. Secondary logic check

8.3.3.1 EN/EN1 and DIS/EN2 Function Check

Assuming that PIN_CONFIG = 0x1 -

1. Assert EN/EN1 pin high
2. Read EN/EN1_PIN_STAT in the STATUS0 register. It should read 0x1 to align with the pin.
3. Read CH1_STAT in the SATUS0 register. It should read 0x0 since it is commanded OFF (Needs SPI command in addition to pin to turn the driver ON).
4. De-assert EN/EN1 pin low
5. Read EN/EN1_PIN_STAT in the STATUS0 register. It should read 0x0 to align with the pin.
6. Read CH1_STAT in the SATUS0 register. It should still read 0x0 since it is commanded OFF.
7. Steps 1-6 can be repeated for DIS/EN2 pin.

8.3.3.2 nFAULT Signalling Check

1. Write CMD0 = 0x01 - request nFAULT assert
2. Write CMD1 = 0x80 – CLR_FAULT so that request is processed
3. nFAULT pin will be asserted low. This can be confirmed by reading back nFAULT_PIN_STAT in STATUS0 register
4. Write CMD0 = 0x0 - request nFAULT de-assert
5. Write CMD1 = 0x80 – CLR_FAULT so that request is processed
6. nFAULT pin will be controlled by nFAULT_CONFIG settings at this point

8.3.3.3 Device Timing Check

1. Write CMD0 = 0x03 - request timing signal assert on nFAULT
2. Write CMD1 = 0x80 – CLR_FAULT so that request is processed
3. nFAULT pin will be driven with a 50% 10 kHz output
4. Write CMD0 = 0x0 - request timing signal de-assert
5. Write CMD1 = 0x80 – CLR_FAULT so that request is processed
6. nFAULT pin will be controlled by nFAULT_CONFIG settings at this point

Copyright © 2026 Texas Instruments Incorporated

8.3.3.4 Secondary Logic Check

1. Write CMD0 = 0x02 - force secondary logic time out assert
2. Within 40 msec, nFAULT pin will be asserted low to indicate time out
3. Write CMD0 = 0x0 - request secondary logic time out de-assert
4. Write CMD1 = 0x80 – CLR_FAULT so that request is processed
5. nFAULT pin will be controlled by nFAULT_CONFIG settings at this point

8.3.4 Turn On Relay

1. Drive the EN/EN1 and DIS/EN2 pins as configured for single output or combined outputs control
2. Internal regulation - Write CMD1 = 0x50, to enable output 1 in internal regulation mode, followed by CMD1 = 0x40. Response will include previous command content (command confirmation).
3. Write CMD1 = 42 to enable output 2 in internal regulation mode, followed by CMD1 = 0x40. Response will include previous command content (command confirmation). Typically peak ramp time of both channels will be staggered.
4. After the peak ramp time, read the STATUSx and MEASx registers
5. A normal response should indicate -
    a. CHx_STAT = 0x1 with no warnings
    b. Peak ramp up time measurement – CHx_PRT
    c. Peak to hold ramp down time measurement – CHx_HRT
    d. Average duty cycle measurement – CHx_DC
6. Poll STATUS0 periodically to ensure there are no warnings.
7. For External control – Similar procedure as (2), but CMD1 values should be updated based on CHx_CTRL selection. Measurements are not valid.
8. Broadcast command (CMD2) is available to change the target current on the all the relays controlled by drivers on the same SPI bus simultaneously.

8.3.5 Turn Off Relay

8.3.5.1 Using Target Device Command

1. Write CMD1 = 0x08 to turn off output 1, 0x01 to turn off output 2 or 0x09 to turn off both outputs, followed by CMD1 = 0x40. Response will include previous command content (command confirmation).
2. Off-state diagnostics will automatically start once the drivers are shut-off.
3. After ~100 msec, read the STATUSx and MEASx registers
4. A normal response should indicate
    a. CHx_STAT = 0x0 with no warnings
    b. CHx_OFF_DIAG_STAT = 0x0
    c. QTO time measurement – CHx_QTOT
    d. QTO start time measurement – CHx_QTOST

8.3.5.2 Using Broadcast Command

1. To turn off all the relays controlled by drivers on the same SPI bus, write CMD2 = 0x04 to immediately quench the currents in all the loads.
2. Follow this with individual device CMD1 = 0x09 to ensure that all the devices remain shut off.
3. Write CMD2 = 0x00 to reset the broadcast command bit
4. After ~100 msec, read the STATUSx and MEASx registers
5. A normal response should indicate
    a. CHx_STAT = 0x0 with no warnings
    b. CHx_OFF_DIAG_STAT = 0x0
    c. QTO time measurement – CHx_QTOT

Copyright © 2026 Texas Instruments Incorporated

d. QTO start time measurement – CHx_QTOST

Copyright © 2026 Texas Instruments Incorporated

8.4 Power Supply Recommendations

- **PVDD:** PVDD is the high voltage power supply from the system and should be connected to all the PVDD pins of the DRV3946-Q1.
- **VDD**: The device requires a 5V low voltage supply to function as both the logic supply and as a redundant power supply for several safety monitoring functions.

8.4.1 PVDD Supply Requirements

The PVDD (12 V) supply should be reverse battery protected with filtering (based on the total loads) before HS switch. The output of the HS switch going to PVDD should have sufficient capacitance (30V, > 10µF) to ensure:

- dV/dt < 2 V/µsec on PVDD when HS switch is closed
- Ability to source the transient load current (inductive energy)
  - When the HS switch is opened with the loads energized, without commanding the DRV3946-Q1 to shut off simultaneously .
  - Fault condition: When the HS switch is opened with the loads energized with commanding DRV3946-Q1 to shut off simultaneously, however one of the loads is shorted to GND.

The capacitance on PVDD is meant to prevent the violation of the ABS MIN on this pin [- 2 V for 10 msec] during this transient. An optional diode from PVDD to GND can be added to help with the inductive current sourced from PVDD during the clamping time to reduce the capacitor size.

If the HS switch is opened with the loads energized, clamping will occur on OUTx (QTO) to rapidly dissipate the inductive energy and de-energize the load in a controlled manner. Two clamping scenarios occur depending on whether the DRV3946-Q1 is commanded to simultaneously shut off the drivers as well.

- Simultaneous shut off (typical & recommended use-case): The device will de-energize or decay the current through the HS clamp. Current path will be PVDD -> Load -> HS clamp triggered HS FET -> PVDD. Capacitance on PVDD does not play a role, other than providing some delay of a few µs for the DRV3946-Q1 to be commanded off after the HS switch has been shut off.
- Only HS switch shut off (not typical): DRV3946-Q1 will continue to maintain regulation as long as possible as PVDD voltage drops and eventually detects PVDD under voltage and decay the current through LS clamp triggered LS FET. Capacitance on PVDD supports the transient load current as current is sourced out of PVDD. Voltage on OUTx pin increases to trigger the passive LS clamp inside the device, which sinks the current from the load into the device. Current path will be GND -> PVDD Capacitor to GND -> Load -> OUTx -> LS FET triggered by LS passive clamp -> GND.

8.4.2 PVDD Undervoltage Transients - Contactor Chatter or Weld Prevention

- There are two features in the DRV3946-Q1 that will handle this depending on the duration of the pulses on PVDD pin and the inductance of the load:
  - UCLO (Under current lock out) – Load current drops below configured level for a configured duration
  - PVDD UV - Voltage on PVDD drops below configured level for a configured duration
- In both these cases, the device can be configured to Hi-Z the driver with internal device clamping through the HS FET. Status register will be updated with the corresponding warnings.
- Once the driver has turned off, the device will NOT turn on the driver till a user CLR FAULT (SPI command) is issued, even if the voltage on PVDD has recovered to normal level.
- There is an additional “RETRY_WAIT” feature that can be enabled to ensure that the relay has a minimum time to cool off before turned on again. This is again to prevent quick unintended turn on – off - on cycles.

Copyright © 2026 Texas Instruments Incorporated

8.5 Layout

8.5.1 Layout Guidelines

- PVDD and VDD pins must be bypassed to ground using low-ESR ceramic capacitors with recommended values. These capacitors should be placed as close to the pins as possible with a thick trace or ground plane connection to the device GND pin.
- Additional bulk capacitance may be required to on PVDD pin. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.
- All PVDD, OUTx and GND pins must be shorted externally with sufficiently wide traces.
- The following figure shows a layout example for a 4cm X 4cm x 1.6mm, 4-layer PCB for the leaded HTSSOP package device. The 4 layers uses 2oz copper on top/ bottom signal layers and 1oz copper on internal supply layers, with 0.3mm thermal via drill diameter, 0.025mm Cu plating, 1mm minimum via pitch.

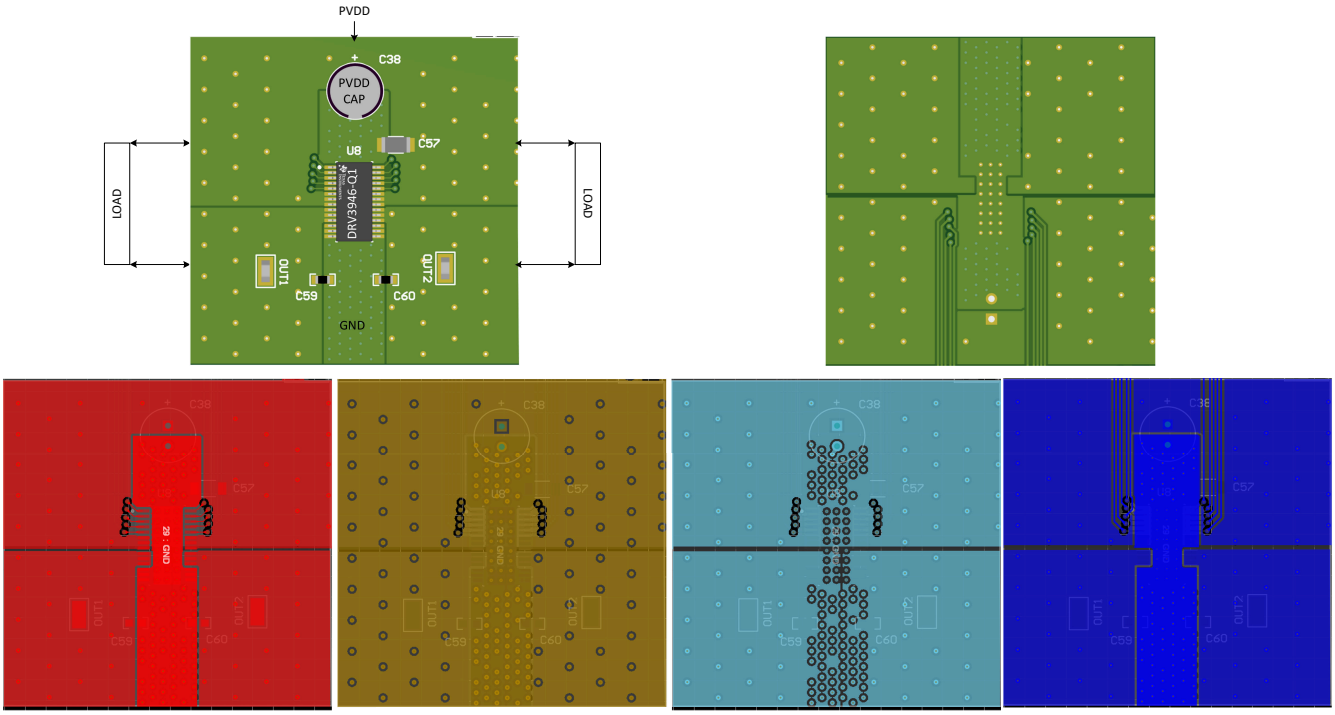


Figure 8-4. Layout Example

Copyright © 2026 Texas Instruments Incorporated

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2023) to Revision A (June 2024)	Page
• Updated Functional Safety text	1
• Updated text on broadcast command	1
• Increased VDD current in standby state from max 5.5mA to max 7.5mA	5
• Added typical and maximum values for all clamp voltages in EC table	5
• Added 10pF filter cap from IPROPI to GND in External Components table	21
• Added Slope Compensation diagram and current reduction paragraph.	35
• Updated Fault Table states	38
• Updated STATUS4 and STATUS5 register names	47
• Updated CONFIG_A6 and CONFIG_B4 registers	61
• Added *Transient Thermal Impedance and Current Capability* section	73

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2026 Texas Instruments Incorporated

11.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
DRV3946QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	3946

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

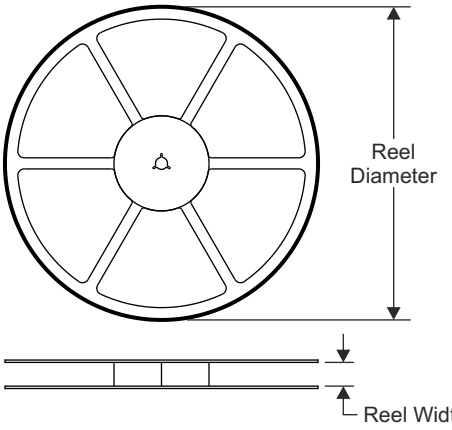
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

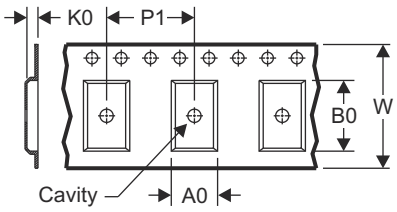
Copyright © 2026 Texas Instruments Incorporated

11.2 Tape and Reel Information

REEL DIMENSIONS

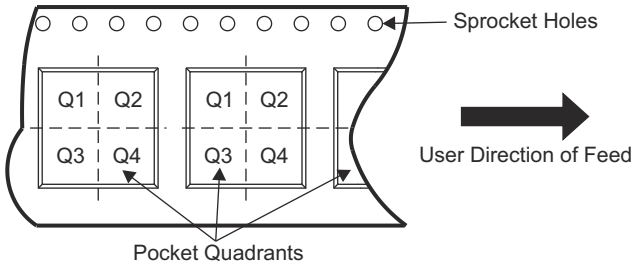


TAPE DIMENSIONS



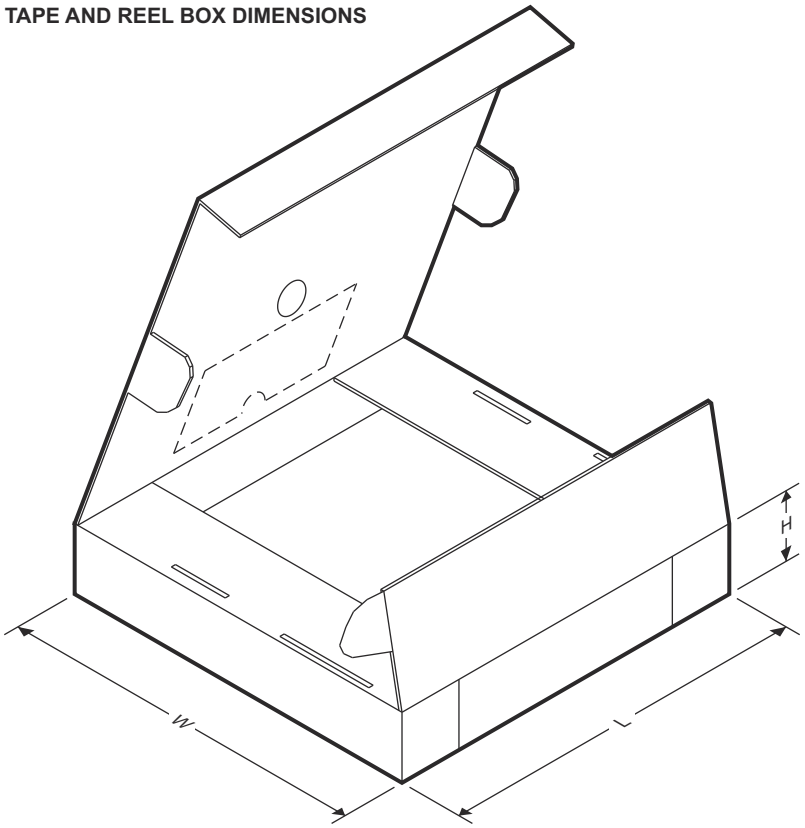
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3946QPWPRQ1	HTSSOP	PWP	28	2500	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

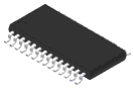


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3946QPWPRQ1	HTSSOP	PWP	28	2500	356.0	356.0	35.0

Copyright © 2026 Texas Instruments Incorporated

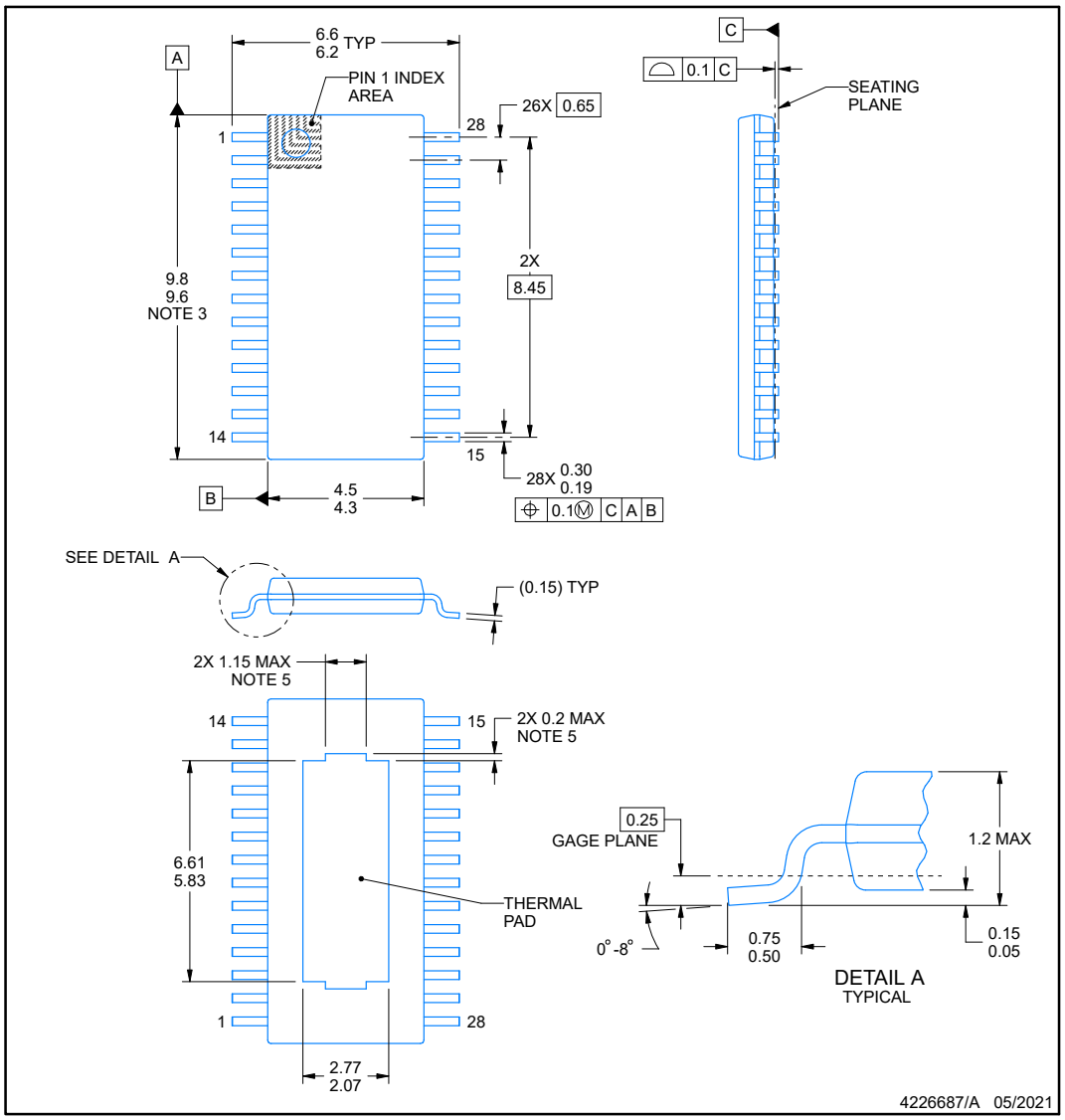
PACKAGE OUTLINE

PWP0028T



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

Copyright © 2026 Texas Instruments Incorporated

PWP0028T

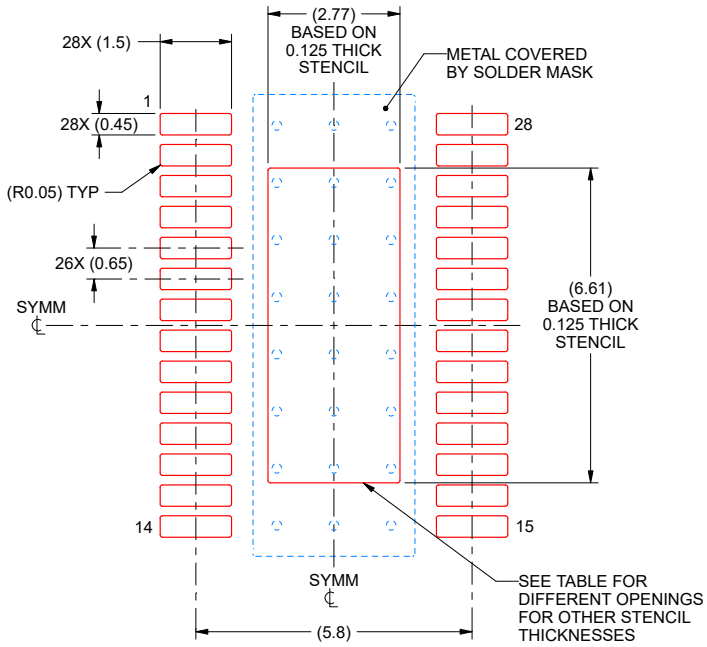
PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

EXAMPLE STENCIL DESIGN

PWP0028T — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

4226687/A 05/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV3946QPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3946
DRV3946QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	3946

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

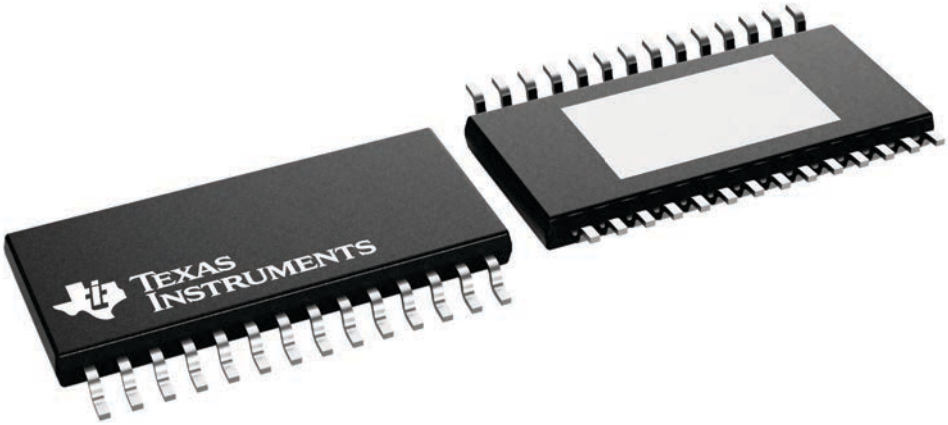
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

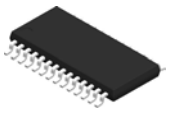
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

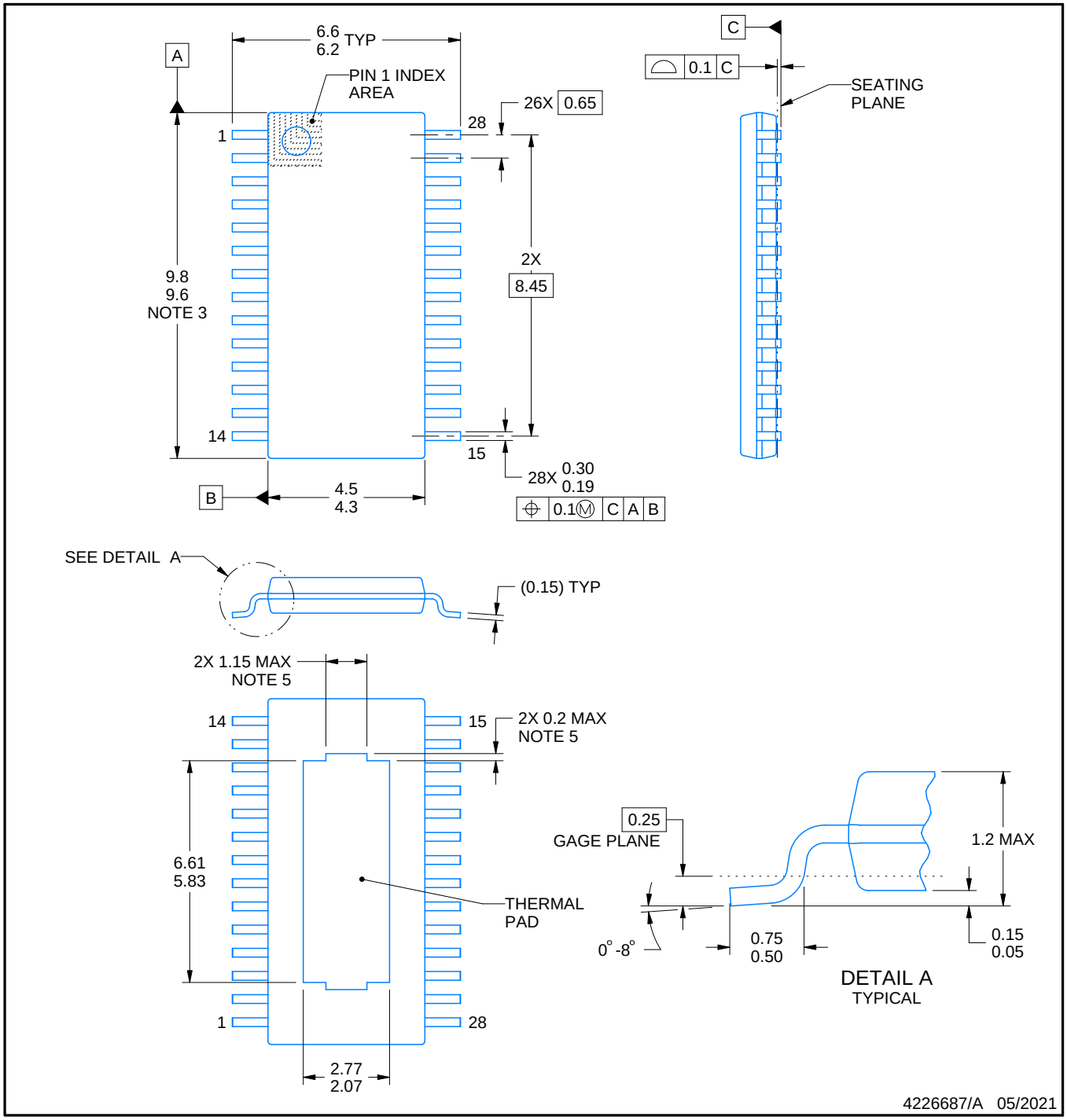
PACKAGE OUTLINE

PWP0028T



PowerPAD™ TSSOP - 1.2 mm max height

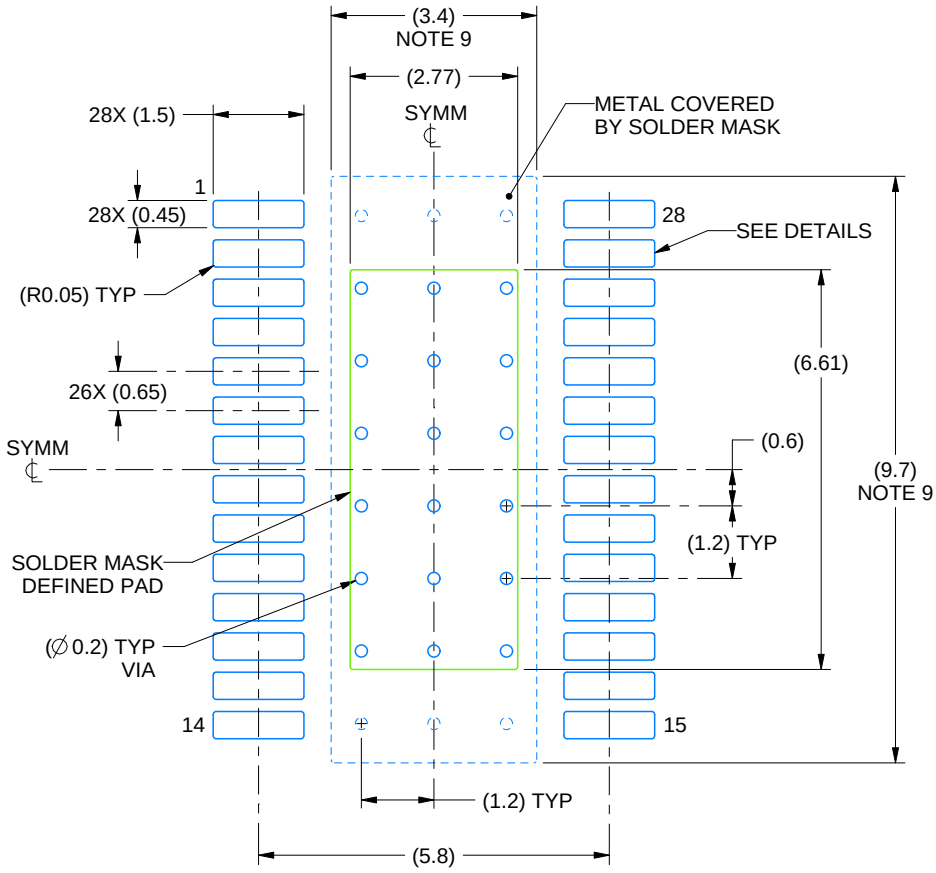
SMALL OUTLINE PACKAGE



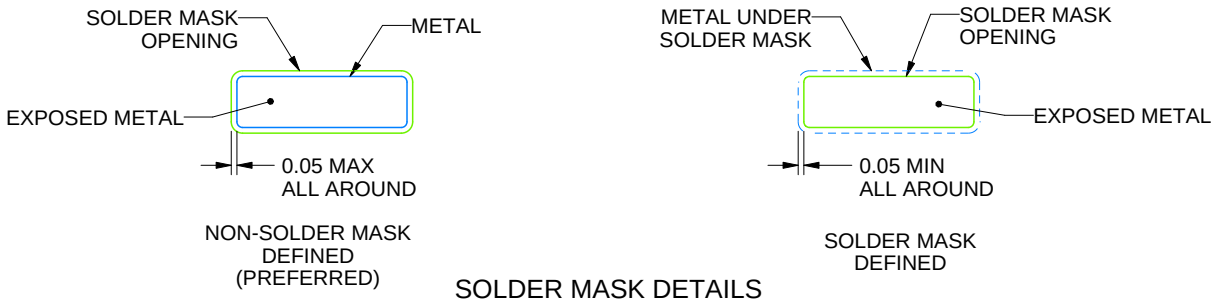
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

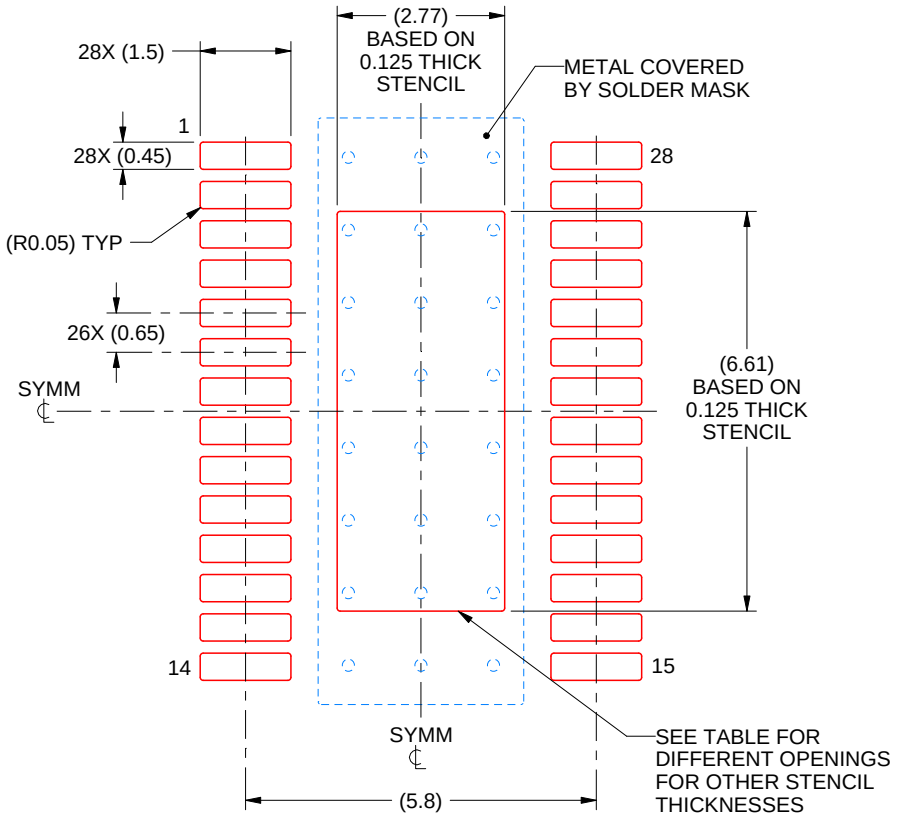


SOLDER MASK DETAILS

4226687/A 05/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

4226687/A 05/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025