DRV3901-Q1 Single Channel Squib Driver For Automotive EV Pyro-Fuse

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation to aid ISO26262 system design up to ASIL C
- Highly integrated squib driver solution targeted at automotive EV pyro-fuse application
  - Integration of power supplies, current regulation, diagnostics, and safety functions
  - SPI or HW pin-based triggering for flexible interface options and rapid firing reaction
  - Diagnostic functions for system energy reservoir capacitor and squib health monitoring
  - Built-in-self-test and diagnostic functions for power supplies, interfaces, drivers, and monitors
  - Architecture for reliable operation with redundant power supplies, low-side and high-driver drivers, and secondary monitoring logic
- Up to 28-V (40-V abs. max) operating voltage
- Compact HVSSOP-28 (DGQ) leaded package
- Two-wire load interface with protected, current controlled high-side and protected secondary low-side switches
- Integrated charge pump for minimal MOSFET drop out voltage
- 4-wire, addressable, 24-bit SPI with CRC protection
  - Allows multiple device to operate on the same SPI
  - Allows for broadcast commands to multiple devices.
- Configurable deployment currents (1.2 A / 2 ms, 1.75 A / 0.5 ms, up to 3.4 A / 0.5 ms)
- Configurable deployment interface options
  - 2-pin HW trigger with PWM or level signaling
  - Protected SPI command with CRC
- Comprehensive off-state diagnostics
  - Device built-in-self-test
  - Driver output and switch test
  - Interface test
  - Energy reservoir capacitor test
  - Squib resistance test
- Configurable fault indicator (nFAULT)

2 Applications

- Squib driver
- Automotive EV pyro-fuse
- Battery disconnect unit
- Battery junction box

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE (NOM)(2)
DRV3901-Q1	HVSSOP (28)	7.3 mm X 4.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.

Device Information

KEY FEATURES
Protected High-Side and Low-Side Architecture
Configurable Deploy Current Options
Direct Hardware Pin Trigger Interface
Energy Reservoir Capacitor Diagnostic
Comprehensive Off-State Diagnostics
Addressable 24-Bit SPI

3 Description

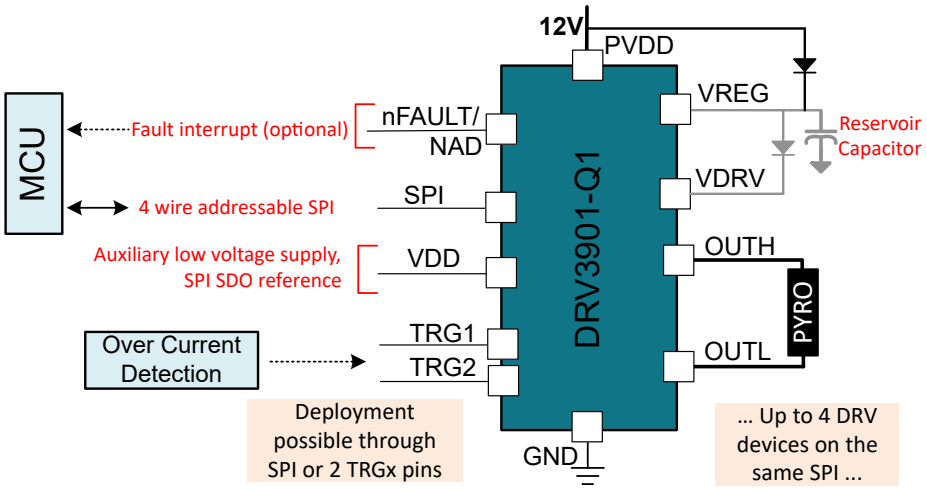
The DRV3901-Q1 is a highly integrated squib driver intended for automotive EV pyro-fuse applications. It includes the power supplies, current sensing and regulation, and diagnostics and protection functions needed to drive a squib load. It incorporates several key functions unique to the device that are different from traditional squib drivers. These functions include a hardware pin trigger interface, an energy reservoir capacitor diagnostic, an addressable SPI, and optimized driver stage with integrated charge pump and additional deployment current options.

The hardware pin trigger (TRGx) interface allows for a deployment command to be issued directly in hardware to the DRV3901-Q1. This allows the flexiblity to either trigger the deployment with MCU hardware pins, directly with an overcurrent sensor, or through other external hardware circuit monitors. The hardware trigger pins support a 2-pin interface with both threshold or PWM based options to ensure robustness against miss deployment while still providing flexiblity to support a variety of interface options. Additionally, CRC protected deployment commands can be sent through the SPI bus as a secondary method.

To support a diagnostic for the system energy reservoir capacitor, the DRV3901-Q1 integrates a switch and monitor circuit to be able to bias and monitor the discharge voltage of the reservoir capacitor. This enables the device and the external MCU to detect a loss/failure of the reservoir capacitor or its approximate value in normal operation.

An addressable SPI, allow multiple devices to be controlled on a shared SPI bus. In addition to reducing required MCU resources, the addressable SPI incorporates a broadcast command structure that allows multiple drivers to be coordinated to trigger simultaneously or with staggered delays. The SPI incorporate multiple robustness functions including a CRC, address readback capability, and various bus fault detection mechanisms.

The power stage utilizes a protected high-side and low-side switch to ensure robustness against unintended driving due to a variety of fault conditions. An integrated charge pump ensures minimal drop out voltage across the switches during deployment to enable operation down to low supply voltages. A wide variety of deployment options are available to optimize for different types of squib loads or for specific application requirements.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2023	*	Initial Release

5 Pin Configuration and Functions

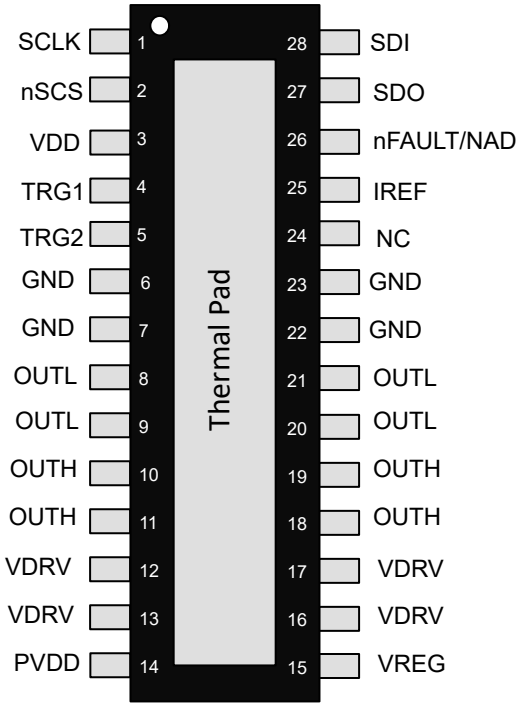


Figure not drawn to scale

Figure 5-1. DRV3901-Q1 HVSSOP 28-Pin (DGQ) Package Pin Diagram

Table 5-1. DRV3901-Q1 HVSSOP 28-Pin (DGQ) Package Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	SCLK	I	Digital	Serial clock input. Serial data is captured on the falling edge and shifted out on rising edge. Internal pulldown resistor to GND.
2	nSCS	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor to V5_S.
3	VDD	I	Power	Device low voltage and auxilary power supply. See section Section 7.3.2 for additional details.
4	TRG1	I	Digital	Direct hardware trigger interface pin. See section Section 7.3.4 for additonal details.
5	TRG2	I	Digital	Direct hardware trigger interface pin. See section Section 7.3.4 for additonal details.
6, 7 22, 23	GND	I	Power	Device ground. Connect to system ground.
8, 9, 20, 21	OUTL	O	Power	Driver low-side output. Connect to negative side of load.
10, 11, 18, 19	OUTH	O	Power	Driver high-side output. Connect to positive side of load.
12, 13, 16, 17	VDRV	I	Power	Device primary power supply. See section Section 7.3.2 for additional details.
14	PVDD	I	Analog	Device connection for optional reservoir capacitor diagnostic. See section Section 7.3.2 for additional details.
15	VREG	O	Analog	Device connection for optional reservoir capacitor diagnostic. See section Section 7.3.2 for additional details.
24	NC	NC	NC	Internal no connect. Connect to GND.
25	IREF	O	Analog	Reference resistor for internal current diagnostic.
26	nFAULT/NAD	O	Digital	Sets device address through external resistor. Open-drain output to indicate fault during normal operation. See section Section 7.3.8 for additional details.
27	SDO	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
28	SDI	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor to GND.
n/a	TPAD	n/a	n/a	Device thermal pad. Connect to GND.

Note

See section Section 7.3.1 for details on required and optional external component connections.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VDRV, VREG, PVDD	–0.3	40	V
Power supply transient voltage ramp	VDRV, VREG, PVDD		1	V/µs
Low voltage supply pin	VDD	–0.3	40	V
Power supply transient voltage ramp	VDD		2	V/µs
Output pin voltage (with respect to GND)	OUTH, OUTL(3)	–0.9	40	V
Output pin current	OUTH, OUTL	Internally limited(2)		A
Trigger pins voltage	TRG1, TRG2	–0.3	40	V
nFAULT/NAD pin voltage	nFAULT/NAD	–0.3	40	V
SPI input pin voltage	SDI, nSCS, SCLK	–0.3	40	V
SPI output pin voltage	SDO	–0.3	40	V
IREF pin voltage	IREF	–0.3	5.5	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Limited by the over current and over temperature protection functions of the device
(3) OUTL pin voltage assumes a resistive load (squib) between OUTH and OUTL.

6.2 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{SUPPLY}	Power supply voltage(2)	PVDD, VREG, VDRV	5		28(1)	V
V_{VDD}	Logic supply voltage(2)	VDD	4.5		5.5	V
V_{LOGIC}	Controller pins voltage	TRG1, TRG2, nFAULT/NAD	0		5.5	V
V_{SPI_IOS}	SPI pins voltage	SDI, SDO, nSCS, SCLK	0		5.5	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Limited by the over current and over temperature protection functions of the device.
(2) Refer to the Power Supplies and Monitors section for specific information on power supply ranges.

6.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	PVDD, VDRV, VREG, OUTH, OUTL, GND	±4000	V
			All other pins	±2000	
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Thermal Information

THERMAL METRIC(1)		HVSSOP (28)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	29.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDRV and VDD Power Supplies						
V_{VDRV_REV}	Supply pin voltage during reverse current	I(VDRV) = - 1 A, device in unpowered state		-2		V
I_{VDRV_STBY}	VDRV current in STANDBY state	Drivers Hi-Z, Off-state diagnostics disabled			2.5	mA
I_{VDD_STBY}	VDD current in STANDBY state	Drivers Hi-Z, VDRV = 0V (no SPI activity)			2.5	mA
I_{VDD_PEAK}	Peak VDD current in case of SDO bus contension (data collision) for one SCLK cycle				40	mA
t_{READY}	Power up time from POR till device is ready to accept commands	VDRV supply power up ramp			1	ms
I_{VDRV_VDD}	Leakage current from VDRV to VDD	VDRV = 13.5 V, VDD = 0 V			25	µA
I_{VDRV_VDD}	Leakage current from VDRV to VDD	VDRV = 0 V, VDD = 5 V	–3			µA
Reset (nPOR)						
$V_{VDRV\_RST\_FALL}$	VDRV falling level when reset occurs, with VDD in HiZ	VDD = 0V	2.5		3.5	V
$V_{VDRV\_RST\_RISE}$	VDRV rising level when reset is released, with VDD in HiZ	VDD = 0V	3		4	V
$V_{VDD\_RST\_FALL}$	VDD falling level when reset occurs, with VDD in HiZ	VDRV = 0V	2.5		3.5	V
$V_{VDD\_RST\_RISE}$	VDD rising level when reset is released, with VDD in HiZ	VDRV = 0V	3		4	V
t_{RST}	Analog filter time on reset	Valid during power-up		13		µs
VDRV Monitor						
$V_{VDRV\_UV\_BIAS\_FALL}$	VDRV BIAS Under voltage threshold when falling	VDD > 4.5 V	2.5		3.4	V
$V_{VDRV\_UV\_BIAS\_RISE}$	VDRV BIAS Under voltage threshold when rising	VDD > 4.5 V	2.7		3.6	V
$V_{VDRV\_UV\_BIAS\_HYST}$	VDRV BIAS Under voltage hysteresis	VDD > 4.5 V		0.2		V
$t_{VDRV\_UV\_BIAS}$	VDRV BIAS UV deglitch time		14.1		18.9	µs
$V_{VDRV\_UV\_FALL}$	VDRV Under voltage trigger threshold when falling		4.3	4.55	4.8	V
$V_{VDRV\_UV\_RISE}$	VDRV Under voltage recovery threshold when rising		4.5	4.75	5	V

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDRV\_UV\_HYST}$	VDRV UV hysteresis			0.2		V
$t_{VDRV\_UV\_W}$	VDRV UV deglitch time for warning		14.1		18.9	µs
t_{VDRV_UV}	VDRV UV deglitch time	VDRV_UV_FLTR = 0x0	233.1		294.5	µs
t_{VDRV_UV}	VDRV UV deglitch time	VDRV_UV_FLTR = 0x1	465.9		578.9	µs
t_{VDRV_UV}	VDRV UV deglitch time	VDRV_UV_FLTR = 0x2	698.6		863.4	µs
t_{VDRV_UV}	VDRV UV deglitch time	VDRV_UV_FLTR = 0x3	931.3		1147.8	µs
$V_{VDRV\_OV\_RISE}$	VDRV Over voltage trigger threshold when rising		26	27	28	V
$V_{VDRV\_OV\_FALL}$	VDRV Over voltage recovery threshold when falling		25.5	26.5	27.5	V
$V_{VDRV\_OV\_HYST}$	VDRV Over voltage hysteresis			0.55		V
t_{VDRV_OV}	VDRV OV deglitch time	VDRV_OV_FLTR = 0x0	233.1		294.5	µs
t_{VDRV_OV}	VDRV OV deglitch time	VDRV_OV_FLTR = 0x1	465.9		578.9	µs
t_{VDRV_OV}	VDRV OV deglitch time	VDRV_OV_FLTR = 0x2	698.6		863.4	µs
t_{VDRV_OV}	VDRV OV deglitch time	VDRV_OV_FLTR = 0x3	931.3		1147.8	µs
$V_{VDRV\_OV\_W\_RISE}$	VDRV Over voltage warning threshold when rising		26	27	28	V
$V_{VDRV\_OV\_W\_FALL}$	VDRV Over voltage warning threshold when falling		25.5	26.5	27.5	V
$V_{VDRV\_OV\_W\_HYST}$	VDRV Over voltage hysteresis			0.55		V
$t_{VDRV\_OV\_W}$	VDRV OV deglitch time for warning		14.1		18.9	µs
VDD Monitor						
$V_{VDD\_UV\_FALL}$	VDD Under voltage trigger threshold when falling		4	4.2	4.4	V
$V_{VDD\_UV\_RISE}$	VDD Under voltage recovery threshold when rising		4.1	4.3	4.5	V
$V_{VDD\_UV\_HYST}$	VDD UV hysteresis			0.1		V
$t_{VDD\_UV\_W}$	VDD UV deglitch time for warning		14.1		18.9	µs
t_{VDD_UV}	VDD UV deglitch time	VDD_UV_FLTR = 0x0	233.1		294.5	µs
t_{VDD_UV}	VDD UV deglitch time	VDD_UV_FLTR = 0x1	465.9		578.9	µs
t_{VDD_UV}	VDD UV deglitch time	VDD_UV_FLTR = 0x2	698.6		863.4	µs
t_{VDD_UV}	VDD UV deglitch time	VDD_UV_FLTR = 0x3	931.3		1147.8	µs
$V_{VDD\_OV\_RISE}$	VDD Over voltage trigger threshold when rising		5.9	6.2	6.5	V
$V_{VDD\_OV\_FALL}$	VDD Over voltage recovery threshold when falling		5.5	5.8	6.1	V
$V_{VDD\_OV\_HYST}$	VDD Over voltage hysteresis			0.4		V
t_{VDD_OV}	VDD OV deglitch time	VDD_OV_FLTR = 0x0	233.1		294.5	µs
t_{VDD_OV}	VDD OV deglitch time	VDD_OV_FLTR = 0x1	465.9		578.9	µs
t_{VDD_OV}	VDD OV deglitch time	VDD_OV_FLTR = 0x2	698.6		863.4	µs
t_{VDD_OV}	VDD OV deglitch time	VDD_OV_FLTR = 0x3	931.3		1147.8	µs
VREG Switch						
V_{PVDD_REV}	Supply pin voltage during reverse current	I(PVDD) = - 0.1 A, device in unpowered state		-1.1		V

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREG_THRS1}	Under voltage threshold below PVDD when VREG switch is disabled		1.7		2.3	V
V_{VREG_THRS1R}	Under voltage recovery threshold below PVDD when VREG switch is re-enabled			1.9		V
V_{VREG_THRS2}	Over voltage threshold above PVDD when VREG switch is disabled		12		32	mV
V_{VREG_THRS2R}	Over voltage threshold above PVDD when VREG switch is re-enabled on recovery			-100		mV
$R_{VREG\_SW\_ON}$	Resistance between PVDD and VREG when switch is enabled		10		35	Ω
$R_{VREG\_SW\_OFF}$	Resistance between PVDD and VREG when switch is disabled		800			KΩ
$t_{VREG\_SW\_W}$	Deglitch time for VREG_SW warnings		204.8	256	307.2	µs
TRG1, TRG2 Pins						
V_{IL}	Input logic low voltage				0.7	V
V_{IH}	Input logic high voltage		1.5			V
V_{IHYS}	Input hysteresis			0.5		V
R_{PD_TRG}	Input pull-down resistance on ENABLE pin to GND	Measured at min VIH level	100		200	kΩ
t_{FLTR_TRG}	Filtering time at pin input		1		3	µs
t_{PWM_TRG}	Acceptable PWM frequency tolerance on TRGx pin to accept as a deploy signal (TRGx_STAT=0x2), valid for PWM based trigger only	PWM_FLTR_SEL = 0, 16 KHz, 75%	-18		32	%
t_{PWM_TRG}	Acceptable PWM frequency tolerance on TRGx pin to accept as a deploy signal (TRGx_STAT=0x2), valid for PWM based trigger only	PWM_FLTR_SEL = 1, 16 KHz, 75%	-15		24	%
t_{PWM_TRG}	Acceptable PWM frequency tolerance on TRGx pin to accept as a deploy signal (TRGx_STAT=0x2), valid for PWM based trigger only	PWM_FLTR_SEL = 2, 16 KHz, 75%	-12		16	%
t_{PWM_TRG}	Acceptable PWM frequency tolerance on TRGx pin to accept as a deploy signal (TRGx_STAT=0x2), valid for PWM based trigger only	PWM_FLTR_SEL = 3, 16 KHz, 75%	-9		12	%
$t_{PWM\_TRG\_TO}$	Time out to detect TRGx pin stuck at low or high (TRGx_STAT = 0x3), valid for PWM based trigger only		85		170	µs
t_{LVL_TRG}	Deglitch time for TRGx pin for level trigger		14.1		18.9	µs
SPI I/Os						
R_{PU_nSCS}	Input pull-up resistance on nSCS to VDD	Measured at min VIH level	100		200	kΩ
R_{PD_SDI}	Input pull-down resistance on SDI to GND	Measured at max VIL level	200		400	kΩ
R_{PD_SCLK}	Input pull-down resistance on SCLK to GND	Measured at min VIH level	200		400	kΩ
V_{IL_SPI}	Input logic low voltage	SDI, nSCS, SCLK pins			0.7	V
V_{IH_SPI}	Input logic high voltage	SDI, nSCS, SCLK pins	1.5			V
V_{IHYS_SPI}	Input hysteresis	SDI, nSCS, SCLK pins		0.1		V
R_{PU_SDO}	Input pull-up resistance on SDO to VDD	Measured at max VIL level	500		1000	kΩ
V_{OL_SDO}	SDO Output logic low voltage	0.5 mA sink into the pin			0.35	V

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH_SDO}	SDO Output logic high voltage	0.5 mA source from the pin	VDD - 0.35			V
I_{OH_SDO}	SDO Output logic high current	Measured at 1V on SDO			30	mA
nFAULT/NAD Pin						
R_{LVL_OORL}	Resistor value out of range – lower threshold				2.6	kΩ
R_{LVL1}	Acceptable resistance for NAD = 00b		5.04	5.6	6.16	kΩ
R_{LVL2}	Acceptable resistance for NAD = 01b		10.8	12	13.2	kΩ
R_{LVL3}	Acceptable resistance for NAD = 10b		24.3	27	29.7	kΩ
R_{LVL4}	Acceptable resistance for NAD = 11b		50.4	56	61.6	kΩ
R_{LVL_OORH}	Resistor value out of range – upper threshold		100			kΩ
I_{nFAULT_PD}	Pull down current on nFAULT pin to indicate fault	V(nFAULT) = 0.3 V	5			mA
V_{IL_nFAULT}	Input logic low voltage for nFAULT feedback buffer	nFAULT pin			0.5	V
V_{IH_nFAULT}	Input logic high voltage for nFAULT feedback buffer	nFAULT pin	1.3			V
V_{IHYS_nFAULT}	Input hysteresis for nFAULT feedback buffer	nFAULT pin		0.1		V
t_{nFAULT_FB}	Deglitch time for nFAULT feedback		14.1		18.9	µs
Output Driver						
R_{ON_LS}	Low-side MOSFET on resistance	V_{VM} = 13.5 V, I_O = 3 A, T_J = 25°C		55		mΩ
R_{ON_LS}	Low-side MOSFET on resistance	V_{VM} = 13.5 V, I_O = 3 A, T_J = 150°C			110	mΩ
R_{ON_HS}	High-side MOSFET on resistance	V_{VM} = 13.5 V, I_O = 3 A, T_J = 25°C		55		mΩ
R_{ON_HS}	High-side MOSFET on resistance	V_{VM} = 13.5 V, I_O = 3 A, T_J = 150°C			110	mΩ
E_{CLAMP}	Inductive energy kick-back	ILOAD = 3.5 A, L = 100µH			1	mJ
I_{OCP_HS}	Over current protection threshold for HS FET		12		20	A
I_{OCP_LS}	Over current protection threshold for HS FET		11.75		20	A
$I_{OCP\_HS\_RDSON}$	Over current protection threshold for HS FET during HS RDSON test				0.45	A
$I_{OCP\_HS\_MEAS}$	Over current protection threshold for HS FET during LOAD resistance measurement test				0.45	A
$I_{OCP\_LS\_RDSON}$	Over current protection threshold for LS FET during LS RDSON test				0.4	A
$I_{OCP\_LS\_MEAS}$	Over current protection threshold for LS FET during IREF resistance & LOAD resistance measurement test				0.4	A
t_{HS_OCP}	Overcurrent protection deglitch time for HS FET		3.2		5	µs
t_{LS_OCP}	Overcurrent protection deglitch time for LS FET		3.2		5	µs
R_{HIZ_OUTL}	Resistance on OUTL to GND in STANDBY state	V_{OUTL} = 1 V	2		6.5	KΩ
I_{HIZ_OUTH}	Pull down current on OUTH to GND in STANDBY state	V_{OUTH} = 3 V	0.4		1.5	mA
I_{HIZ_LOAD}	Load current in STANDBY state	V_{VDRV} = 40 V, load = 2Ω			0.1	mA

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HIZ_LOAD}	Load current in STANDBY state during OUTH short to VDRV	V_{VDRV} = 28 V, load = 2Ω			10	mA
I_{HIZ_LOAD}	Load current in STANDBY state during OUTL short to GND	V_{VDRV} = 28 V, load = 2Ω			0.11	mA
I_{HIZ_LOAD}	Load current in STANDBY state during OUTL short to VDRV	V_{VDRV} = 28 V, load = 2Ω			7	mA
Deploy Parameters						
t_{DLY_SPI}	Time to start deployment after a valid SPI command	DEPLOY_IRATE = 0x0			50	µs
t_{DLY_SPI}	Time to start deployment after a valid SPI command	DEPLOY_IRATE = 0x1			60	µs
t_{DLY_TRG}	Time to start deployment after a valid TRGx pin command	DEPLOY_IRATE = 0x0			50	µs
t_{DLY_TRG}	Time to start deployment after a valid TRGx pin command	DEPLOY_IRATE = 0x1			60	µs
I_{DEPLOY}	Deploy current	Load = 2Ω, DEPLOY_ISEL = 0x0	1.2	1.3	1.41	A
I_{DEPLOY}	Deploy current	Load = 2Ω, DEPLOY_ISEL = 0x1 or 0x2	1.65	1.85	2.01	A
I_{DEPLOY}	Deploy current	Load = 0Ω, DEPLOY_ISEL = 0x3	1.75	1.93	2.09	A
I_{DEPLOY}	Deploy current	Load = 2Ω, DEPLOY_ISEL = 0x3	1.75	1.93	2.09	A
I_{DEPLOY}	Deploy current	Load = 2Ω, DEPLOY_ISEL = 0x4 or 0x6	2.19	2.39	2.59	A
I_{DEPLOY}	Deploy current	Load = 2Ω, DEPLOY_ISEL = 0x5 or 0x7	3.40	3.72	4.04	A
I_{SNS_THRS}	Deploy current sense threshold	With respect to typical value	60		90	%
t_{DEPLOY}	Deploy time	Load = 2Ω, DEPLOY_ISEL ≤ 0x2	2.09		2.56	ms
t_{DEPLOY}	Deploy time	Load = 2Ω, DEPLOY_ISEL > 0x2	0.52		0.64	ms
I_{RISE0}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_IRATE = 0x0		1.6		µs/A
I_{RISE0}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x1 or 0x2, DEPLOY_IRATE = 0x0		1.3		µs/A
I_{RISE0}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x3, DEPLOY_IRATE = 0x0		1		µs/A
I_{RISE0}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x4 or 0x6, DEPLOY_IRATE = 0x0		1		µs/A
I_{RISE0}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x5 or 0x7, DEPLOY_IRATE = 0x0		1		µs/A
I_{RISE1}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x0, DEPLOY_IRATE = 0x1		16		µs/A
I_{RISE1}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x1 or 0x2, DEPLOY_IRATE = 0x1		12		µs/A
I_{RISE1}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x3, DEPLOY_IRATE = 0x1		11		µs/A
I_{RISE1}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x4 or 0x6, DEPLOY_IRATE = 0x1		9		µs/A
I_{RISE1}	Rising current slope (20% - 80%)	Load = 2Ω, DEPLOY_ISEL = 0x5 or 0x7, DEPLOY_IRATE = 0x1		6		µs/A
t_{START_TO}	Time out for TMEAS_START timer	TMEAS_START_TO = 0x0	71.36		87.78	µs
t_{START_TO}	Time out for TMEAS_START timer	TMEAS_START_TO = 0x1	129.55		158.89	µs
t_{START_TO}	Time out for TMEAS_START timer	TMEAS_START_TO = 0x2	187.73		230	µs
t_{START_TO}	Time out for TMEAS_START timer	TMEAS_START_TO = 0x3	245.45		300.56	µs
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x0	0.09		0.111	ms
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x1	0.181		0.222	ms
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x2	0.363		0.444	ms

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x3	0.726		0.888	ms
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x4	1.454		1.777	ms
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x5	2.181		2.666	ms
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x6	2.908		3.555	ms
t_{DEPLOY_DLY}	Programmed delay to start deployment	DEPLOY_DLY = 0x7	3.635		4.444	ms
Off-State Diagnostics						
t_{BIST}	Device BIST time		0.13		0.17	ms
$t_{CMP\_FLTR\_WK\_PU}$	Comparator deglitch time for weak pull up test		14.1		18.9	µs
$V_{REF\_WK\_PU}$	Voltage reference for comparator on OUTL for weak pull up test	OFF_DIAG_WK_PU_VSEL = 0	1.89	2.1	2.31	V
$V_{REF\_WK\_PU}$	Voltage reference for comparator on OUTL for weak pull up test	OFF_DIAG_WK_PU_VSEL = 1	2.16	2.4	2.64	V
$I_{REF\_WK\_PU}$	Pull up current on OUTL for weak pull up test	OFF_DIAG_WK_PU_ISEL = 0, V_{OUTL}= 2.4 V	0.75	1	1.25	mA
$I_{REF\_WK\_PU}$	Pull up current on OUTL for weak pull up test	OFF_DIAG_WK_PU_ISEL = 1, V_{OUTL}= 2.4 V	1.5	2	2.5	mA
t_{WK_PU}	Time out for weak pull up test	OFF_DIAG_WK_PU_TSEL = 0	0.22		0.29	ms
t_{WK_PU}	Time out for weak pull up test	OFF_DIAG_WK_PU_TSEL = 1	0.45		0.56	ms
t_{WK_PU}	Time out for weak pull up test	OFF_DIAG_WK_PU_TSEL = 2	0.9		1.12	ms
t_{WK_PU}	Time out for weak pull up test	OFF_DIAG_WK_PU_TSEL = 3	1.81		2.24	ms
$t_{CMP\_FLTR\_WK\_PD}$	Comparator deglitch time for weak pull down test		14.1		18.9	µs
$V_{REF\_WK\_PD}$	Voltage reference for comparator on OUTL for weak pull down test	OFF_DIAG_WK_PD_VSEL = 0	1.35	1.5	1.65	V
$V_{REF\_WK\_PD}$	Voltage reference for comparator on OUTL for weak pull down test	OFF_DIAG_WK_PD_VSEL = 1	1.62	1.8	1.98	V
$I_{REF\_WK\_PD}$	Pull down current on OUTH for weak pull down test	OFF_DIAG_WK_PD_ISEL = 0, V_{OUTH}= 1.5 V	0.7	1	1.3	mA
$I_{REF\_WK\_PD}$	Pull down current on OUTH for weak pull down test	OFF_DIAG_WK_PD_ISEL = 1, V_{OUTH}= 1.5 V	1.4	2	2.6	mA
t_{WK_PD}	Time out for weak pull down test	OFF_DIAG_WK_PD_TSEL = 0	0.22		0.29	ms
t_{WK_PD}	Time out for weak pull down test	OFF_DIAG_WK_PD_TSEL = 1	0.45		0.56	ms
t_{WK_PD}	Time out for weak pull down test	OFF_DIAG_WK_PD_TSEL = 2	0.9		1.12	ms
t_{WK_PD}	Time out for weak pull down test	OFF_DIAG_WK_PD_TSEL = 3	1.81		2.24	ms
$t_{CMP\_FLTR\_HSRDSON}$	Comparator deglitch time for HS RDSON test		14.1		18.9	µs
$V_{REF\_PC\_HSRDSON}$	Pre-charge voltage reference for comparator on OUTH with respect to VDRV for HS RDSON test		-1.65	-1.5	-1.35	V
$V_{REF\_HSRDSON}$	Voltage reference for comparator on OUTH with respect to VDRV for HS RDSON test	OFF_DIAG_HSRDSON_VSEL = 0	-90	-75	-60	mV
$V_{REF\_HSRDSON}$	Voltage reference for comparator on OUTH with respect to VDRV for HS RDSON test	OFF_DIAG_HSRDSON_VSEL = 1	-180	-150	-120	mV
$I_{REF\_PC\_HSRDSON}$	Pre-charge pull up current on OUTH for HS RDSON test	V_{OUTH} = V_{VDRV} - 3.5 V	32	40	48	mA
$I_{REF\_HSRDSON}$	Pull down current on OUTH for HS RDSON test	OFF_DIAG_HS_RDSON_ISEL = 0, V_{OUTH} = V_{VDRV} - 0.75 V	16	20	24	mA

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{REF\_HSRDSON}$	Pull down current on OUTH for HS RDSON test	OFF_DIAG_HS_RDSON_ISEL = 1, V_{OUTH} = V_{VDRV} - 0.75 V	32	40	48	mA
$t_{HSRDSON}$	Time out for HS RDSON test	OFF_DIAG_HS_RDSON_TSEL = 0	0.22		0.29	ms
$t_{HSRDSON}$	Time out for HS RDSON test	OFF_DIAG_HS_RDSON_TSEL = 1	0.45		0.56	ms
$t_{HSRDSON}$	Time out for HS RDSON test	OFF_DIAG_HS_RDSON_TSEL = 2	0.9		1.12	ms
$t_{HSRDSON}$	Time out for HS RDSON test	OFF_DIAG_HS_RDSON_TSEL = 3	1.81		2.24	ms
$t_{CMP\_FLTR\_LSRDSON}$	Comparator deglitch time for LS RDSON test		14.1		18.9	µs
$V_{REF\_PC\_LSRDSON}$	Pre-charge voltage reference for comparator on OUTL for LS RDSON test		1.350	1.500	1.650	V
$V_{REF\_LSRDSON}$	Voltage reference for comparator on OUTL for LS RDSON test	OFF_DIAG_LSRDSON_VSEL = 0	60	75	90	mV
$V_{REF\_LSRDSON}$	Voltage reference for comparator on OUTL for LS RDSON test	OFF_DIAG_LSRDSON_VSEL = 1	120	150	180	mV
$I_{REF\_PC\_LSRDSON}$	Pre-charge pull down current on OUTL for LS RDSON test	V_{OUTL} = 3.5 V	32	40	48	mA
$I_{REF\_LSRDSON}$	Pull up current on OUTL for LS RDSON test	OFF_DIAG_LS_RDSON_ISEL = 0, V_{OUTL} = 0.75 V	16.0	20	24.0	mA
$I_{REF\_LSRDSON}$	Pull up current on OUTL for LS RDSON test	OFF_DIAG_LS_RDSON_ISEL = 1, V_{OUTL} = 0.75 V	32	40	48	mA
$t_{LSRDSON}$	Time out for LS RDSON test	OFF_DIAG_LS_RDSON_TSEL = 0	0.22		0.29	ms
$t_{LSRDSON}$	Time out for LS RDSON test	OFF_DIAG_LS_RDSON_TSEL = 1	0.45		0.56	ms
$t_{LSRDSON}$	Time out for LS RDSON test	OFF_DIAG_LS_RDSON_TSEL = 2	0.9		1.12	ms
$t_{LSRDSON}$	Time out for LS RDSON test	OFF_DIAG_LS_RDSON_TSEL = 3	1.81		2.24	ms
I_{IREF}	Pull-up current forced on IREF pin	V_{IREF} = 0.1 V	9	10	11	µA
$t_{CMP\_FLTR\_MEAS}$	Comparator deglitch time for IREF & RLOAD measurements		14.1		18.9	µs
t_{MBIST}	Time for IREF resistance monitor test		0.9		1.12	ms
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL = 0	-36	-25	-14	mV
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL = 1	-60	-40	-20	mV
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL = 2	-90	-60	-30	mV
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL =3	-120	-80	-40	mV
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL = 4	-150	-100	-50	mV
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL = 5	-180	-120	-60	mV
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL = 6	-210	-140	-70	mV
V_{DAC_VREG}	Comparator reference below PVDD	OFF_DIAG_CMEAS_THRS_SEL = 7	-240	-160	-80	mV
V_{DIFF}	Stop threshold for comparator reference with respect to start threshold		-44	-40	-36	mV
V_{OFFSET}	Threshold for CMP_R below CMP			-50		mV
t_{VREG_MEAS}	Comparator deglitch time for OUTH & OUTL comparators		1.8		3.4	µs
t_{VREG_VMEAS}	Time for VREG voltage measurement		3.9		4.9	ms
t_{CMEAS_SETUP}	Set up time for VREG capacitor measurement		14.1		18.9	µs
I_{VDRV_DIAG}	Pull down current on VDRV (Includes I_{VDRV_STBY})		38	46.5	56	mA
t_{CMEAS}	Total discharge time for VREG capacitor measurement	OFF_DIAG_CMEAS_TSEL = 0	0.43		0.54	ms

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CMEAS}	Total discharge time for VREG capacitor measurement	OFF_DIAG_CMEAS_TSEL = 1	0.9		1.11	ms
t_{CMEAS}	Total discharge time for VREG capacitor measurement	OFF_DIAG_CMEAS_TSEL = 2	1.8		2.21	ms
t_{CMEAS}	Total discharge time for VREG capacitor measurement	OFF_DIAG_CMEAS_TSEL = 3	3.63		4.45	ms
I_{RMEAS}	Load current during RLOAD test		32	40	48	mA
t_{RMEAS}	Time for RLOAD test	OFF_DIAG_RMEAS_TSEL = 0	0.27		0.34	ms
t_{RMEAS}	Time for RLOAD test	OFF_DIAG_RMEAS_TSEL = 1	0.5		0.61	ms
t_{RMEAS}	Time for RLOAD test	OFF_DIAG_RMEAS_TSEL = 2	0.95		1.17	ms
t_{RMEAS}	Time for RLOAD test	OFF_DIAG_RMEAS_TSEL = 3	1.86		2.29	ms
R_{MEASL}	Load resistor range for low resistance detection	OFF_DIAG_RMEAS_THRS_L = 0	1.3		1.7	Ω
R_{MEASL}	Load resistor range for low resistance detection	OFF_DIAG_RMEAS_THRS_L = 1	1		1.5	Ω
R_{MEASH}	Load resistor range for high resistance detection	OFF_DIAG_RMEAS_THRS_H = 0	2.5		3.15	Ω
R_{MEASH}	Load resistor range for high resistance detection	OFF_DIAG_RMEAS_THRS_H = 1	2.9		3.65	Ω
R_{MEASH}	Load resistor range for high resistance detection	OFF_DIAG_RMEAS_THRS_H = 2	3.3		4.2	Ω
R_{MEASH}	Load resistor range for high resistance detection – used for post-deployment resistance check	OFF_DIAG_RMEAS_THRS_H = 3	50		70	Ω
SPI Watchdog Monitor						
t_{WD}	SPI valid transaction interval	SPI_WD_SEL = 0x0	57.7		71.7	ms
t_{WD}	SPI valid transaction interval	SPI_WD_SEL = 0x1	227.1		278.8	ms
t_{WD}	SPI valid transaction interval	SPI_WD_SEL = 0x2	908.5		1111.7	ms
t_{WD}	SPI valid transaction interval	SPI_WD_SEL = 0x3	1818		2223.3	ms
Thermal Protection						
T_{TSD}	Thermal shutdown during ACTIVE		150	170	190	°C
T_{TSD_HYS}	Thermal shutdown hysteresis			20		°C
t_{TSD}	Thermal shutdown deglitch time		14.1		18.9	µs
$T_{TSD\_W\_OFF}$	Thermal warning during off-state diagnostics			140		°C
T_{TSD_W}	Thermal warning during ACTIVE/ STANDBY			150		°C
$T_{TSD\_W\_HYS}$	Thermal warning hysteresis			20		°C
t_{TSD_W}	Thermal warning deglitch time		14.1		18.9	µs
Safety Layer						
$V_{V5\_S\_UV\_FALL}$	V5_S Under voltage trigger threshold when falling		4	4.2	4.4	V
$V_{V5\_S\_UV\_RISE}$	V5_S Under voltage recovery threshold when rising		4.1	4.3	4.5	V
$V_{V5\_S\_UV\_HYST}$	V5_S UV hysteresis			0.1		V
$t_{V5\_S\_UV}$	V5_S UV deglitch time		15		20	µs
$V_{V5\_S\_OV\_RISE}$	V5_S Over voltage trigger threshold when rising		5.9	6.2	6.5	V

5 V < V_{VDRV} < 28 V, 4.5V < V_{VDD} < 5.5 V, -40 °C < T_J < 125 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{V5\_S\_OV\_FALL}$	V5_S Over voltage recovery threshold when falling		5.5	5.8	6.1	V
$V_{V5\_S\_OV\_HYST}$	V5_S Over voltage hysteresis			0.4		V
$t_{V5\_S\_OV}$	V5_S OV deglitch time		15		20	µs
f_{OSC}, f_{OSC_R}	Main and redundant oscillator frequency			2		MHz
t_{HEART_BEAT}	Heart beat interval from main logic		0.69		1.324	ms
$t_{HEART\_BEAT\_L}$	Heart beat interval - lower threshold		0.945		1.155	ms
$t_{HEART\_BEAT\_H}$	Heart beat interval - upper threshold		1.41		1.724	ms
t_{TIME_OUT}	Shut off timer time out duration		29.03		35.55	ms

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK minimum period	125			ns
t_{SCLKH}	SCLK minimum high time	62.5			ns
t_{SCLKL}	SCLK minimum low time	62.5			ns
t_{HI_nSCS}	SDO minimum high time	2000			ns
t_{SU_nSCS}	nSCS input setup time	40			ns
t_{H_nSCS}	nSCS input hold time	40			ns
t_{SU_SDI}	SDI input data setup time	20			ns
t_{H_SDI}	SDI input data hold time	20			ns
t_{EN}	SDO enable delay time			50	ns
t_{DIS}	SDO disable delay time			1000	ns

6.7 Timing Diagrams

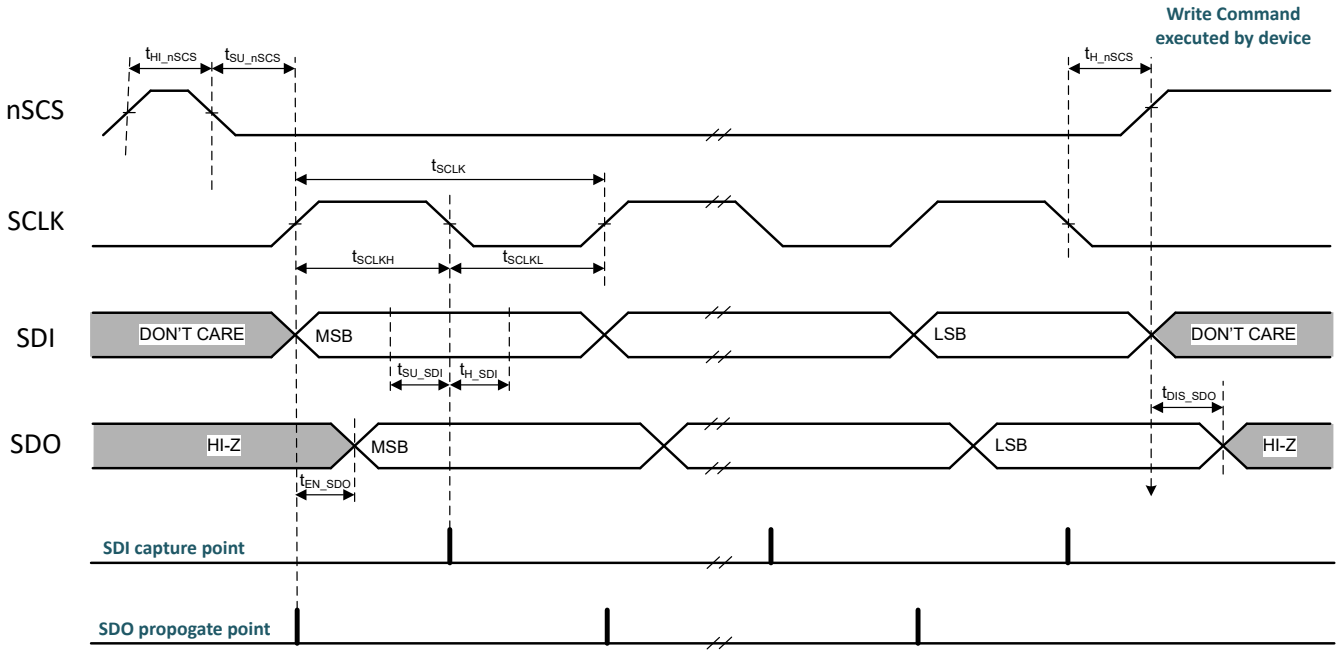


Figure 6-1. SPI Timing Diagram

6.8 Typical Characteristics

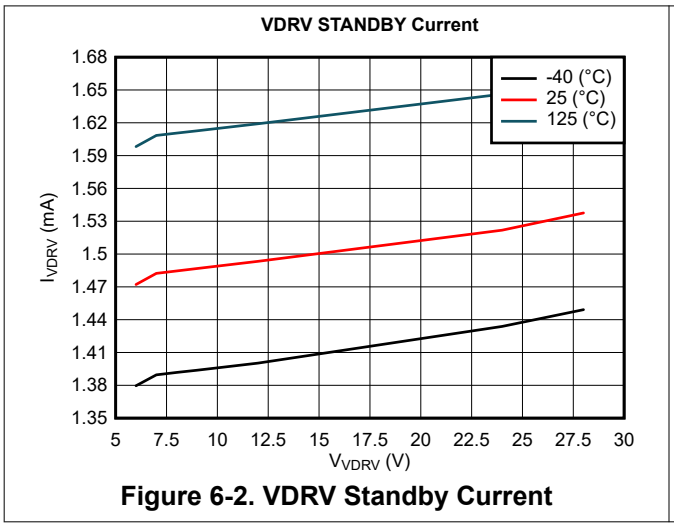


Figure 6-2. VDRV Standby Current

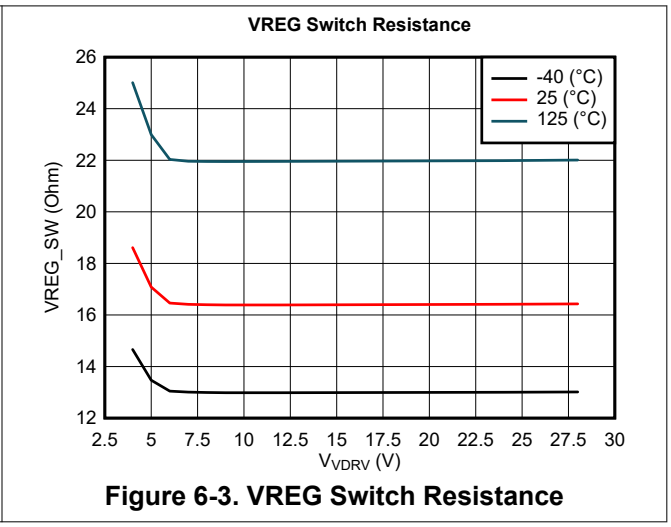


Figure 6-3. VREG Switch Resistance

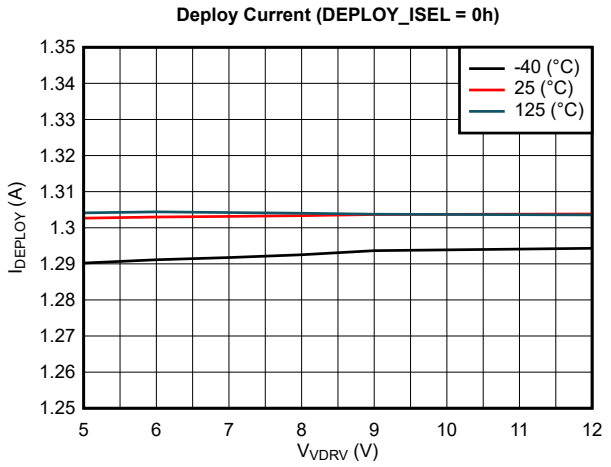


Figure 6-4. Deploy Current (DEPLOY_ISEL = 0h)

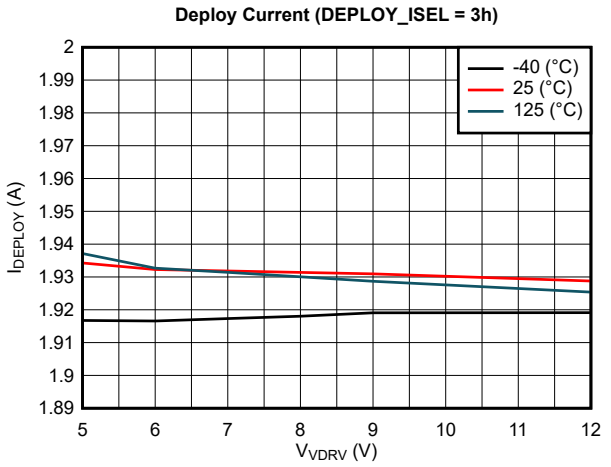


Figure 6-5. Deploy Current (DEPLOY_ISEL = 3h)

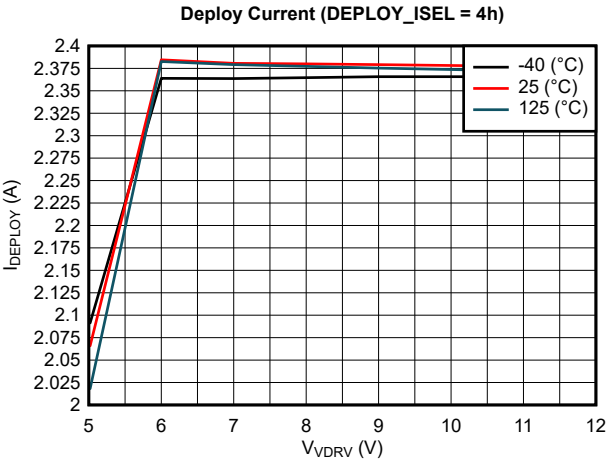


Figure 6-6. Deploy Current (DEPLOY_ISEL = 4h)

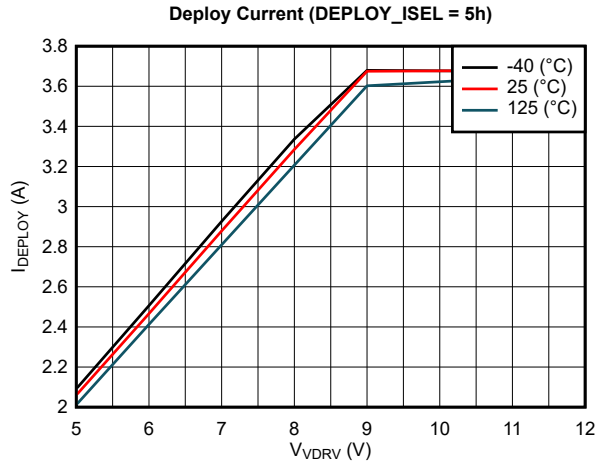


Figure 6-7. Deploy Current (DEPLOY_ISEL = 5h)

7 Detailed Description

7.1 Overview

The table below outlines the various functions and their locations in this document. Detailed information on device initialization and software setup is provided in the Initialization Setup section.

Table 7-1. Function Overview

Category	Detailed Description Section	Electrical Characteristics Table
Power Supplies and Monitors	VDRV and VDD Power Supplies	VDRV and VDD Power Supplies
	VREG Switch	VREG Switch
	VDRV Monitor	Reset (nPOR)
	VDD Monitor	VDD Monitor
	Reset (nPOR)	Reset (nPOR)
	Device Safety Layer	Safety Layer
State Diagram	State Diagram	N/A
Output Driver	Output Driver	Output Driver
	STANDBY State	
	ACTIVE State	
	Overcurrent Protection	
	Thermal Protection	Thermal Protection
Trigger (TRGx) Pins	Trigger (TRGx) Pins	TRG1, TRG2 Pins
	PWM Based Trigger	
	Trigger Monitors	
Deploy Parameters	Deploy Parameters	Deploy Parameters
	Deploy Delay	
Off-State Diagnostics	Off-State Diagnostics	Off-state Diagnotics
	Device BIST	
	Weak Pull-Up Test	
	Weak Pull-Down Test	
	High-Side MOSFET RDSON Test	
	Low-Side MOSFET RDSON Test	
	IREF Resistance Monitor	
	VREG Voltage and Capacitance Measurement	
	Output Load Resistance Monitor	
SPI Watchdog Monitor	SPI Watchdog Monitor	SPI Watchdog Monitor
nFAULT/NAD Pin	nFAULT/NAD Pin	nFAULT/NAD Pin
Fault Tables	Fault Tables	N/A
SPI Interface	SPI Interface	SPI I/Os

7.2 Functional Block Diagram

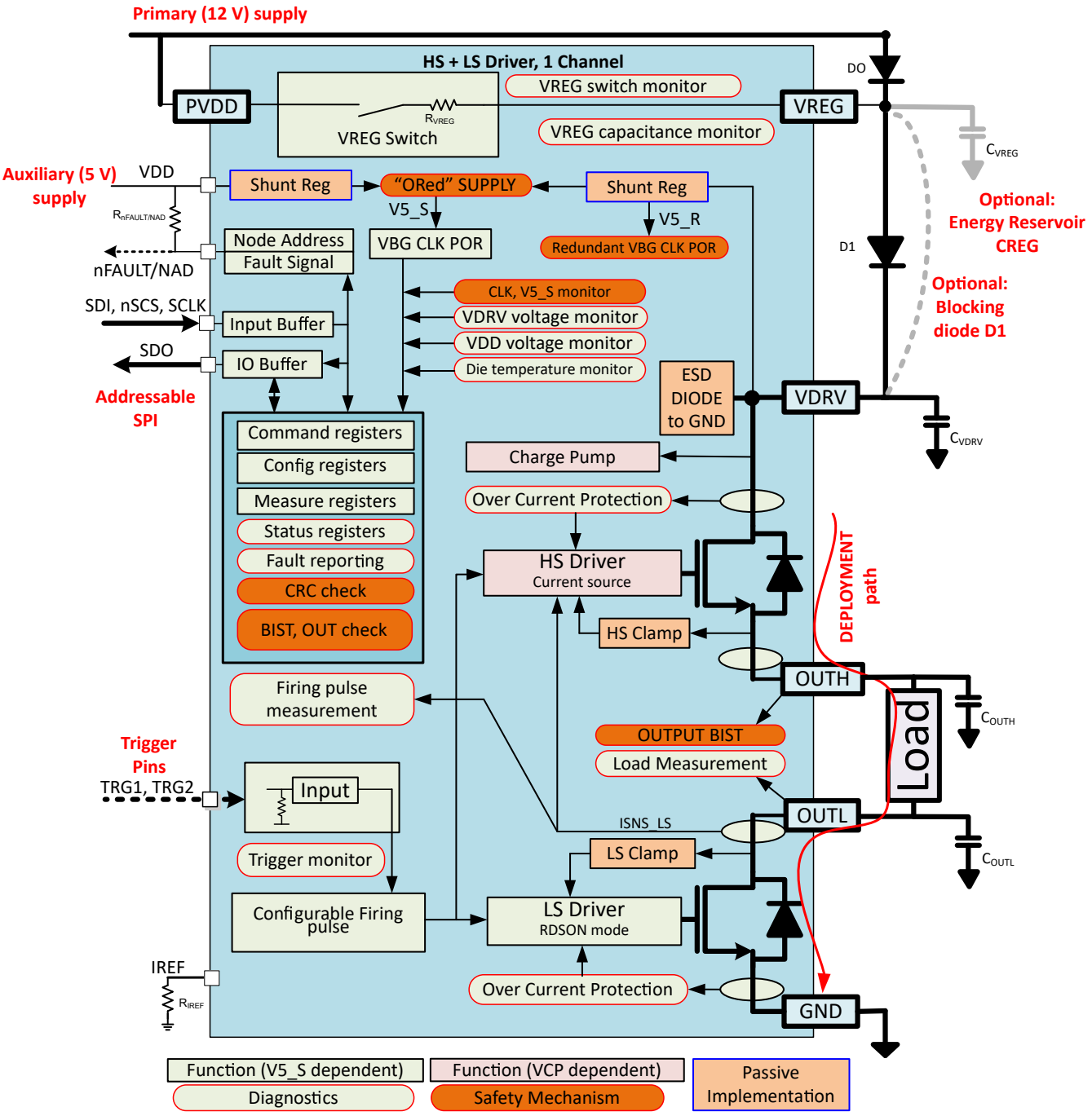


Figure 7-1. DRV3901-Q1 Block Diagram

7.3 Feature Description

7.3.1 External Components

Table 7-2. Recommended External Components

PIN 1	PIN 2	Component	Name	Function	Value
IREF	GND	Resistor	R_{IREF}	Used during off-state diagnostics for the measurement BIST to qualify the load measurement.	0.063W, 10K Ω, 10%
SDO	VDD	Resistor	R_{SDO}	Pull up resistor on SDO to ensure that SDO output is registered as high when not driven by the device.	0.063W, 10K Ω, 10%
nFAULT/NAD	VDD	Resistor	$R_{NFAULT/NAD}$	Sets the unique node address for SPI communication. This needs to be one of the four resistor values allowed, else NAD_ERROR flag will be set.	0.0603W, 5.6K / 12K / 27K / 56K Ω, 1%
VREG	GND	Bulk Capacitor	C_{VREG}	Optional - Local energy reservoir capacitor on VREG to supply driver in loss of PVDD power supply fault condition.	Supply-rated, 100 µF or higher, application dependent
VDRV	GND	Bypass Capacitor	C_{VDRV}	Local high frequency bypass capacitor on VDRV.	Supply-rated, 0.1 µF, low ESR ceramic capacitor
VDD	GND	Bypass Capacitor	C_{VDD}	Optional – Local high frequency bypass capacitor on VDD.	Supply-rated, 0.1 µF, low ESR ceramic capacitor
PVDD	VREG	Diode	D0	Blocks current flow from VREG to PVDD in case of loss of PVDD.	
PVDD	GND	Bypass Capacitor	C_{PVDD}	Optional – Local high frequency bypass capacitor on PVDD.	Supply-rated, 0.1 µF or higher, low ESR ceramic capacitor
VREG	VDRV	Diode	D1	Optional – False deployment prevention for fault condition when OUTL is shorted to high voltage with VREG at low voltage.	
OUTH	OUTH	Filter Inductor	L_{OUTH}	Optional – The device itself limits the di/dt during operation. This series inductor may be used to reduce this further if needed by the squib requirements.	≤ 22 µH
OUTL	OUTL	Filter Inductor	L_{OUTL}	Optional – The device itself limits the di/dt during operation. This series inductor may be used to reduce this further if needed by the squib requirements.	≤ 22 µH
OUTH	GND	Bypass Capacitor	C_{OUTH}	ESD capacitor close to the load	Supply-rated, ≤ 47 nF, low ESR ceramic capacitor
OUTL	GND	Bypass Capacitor	C_{OUTL}	ESD capacitor close to the load	Supply-rated, ≤ 47 nF, low ESR ceramic capacitor

7.3.2 Power Supplies and Monitors

7.3.2.1 VDRV and VDD Power Supplies

The DRV3901-Q1 is powered through VDRV (12 V typical) and VDD (5 V typical) pins. While the drivers and the output stage are mainly supplied from VDRV, the logic and critical safety / diagnostic functions are driven from an internal 5V supply (safe 5V referred to as V5_S) that is derived from a power "OR" combination of VDRV and VDD. The power ORing ensures that the device maintains its intelligence and critical functions even if there is a loss of one of the external supplies. Voltage references, current biases, oscillator and the digital block are powered by V5_S. Redundant references and biases derived from PVDD are used to qualify V5_S and the oscillator.

Following a power-on-reset (POR) on V5_S, a power up initialization is done that includes the address NAD determination, internal self-test (BIST) of the memory and diagnostics, and settling time for internal blocks within t_{READY} time. A CLR_FAULT SPI command from the user to acknowledge wake-up will place the device in the STANDBY state, with I_{VDRV_STBY} and I_{VDD_STBY} with drivers in the high-impedance (Hi-Z) state until commanded by the user. Since the device uses a power "OR" architecture, certain functions are available even in the event that one of the external power supplies (VDD or VDRV) is lost.

Table 7-3 below shows key device functionality with varying VDD voltage levels, assuming VDRV is within undervoltage and overvoltage limits.

Table 7-3. VDD Power Supply Dependency

VDD	Deploy Function	Off-state Diagnostics	SPI Communication
> $V_{VDD\_OV\_RISE}$	Available (1)	Available (1)	SDI Ok, SDO will see VDD_ERR
Nominal	Available (1)	Available (1)	Available
< $V_{VDD\_UV\_FALL}$	Available (1)	Available (1)	SDI Ok, SDO will see VDD_ERR

(1) Limited by the overcurrent and over temperature protection functions of the device.

Table 7-4 and Figure 7-2 below shows key device functionality with varying VDRV voltage levels, assuming VDD is within undervoltage and overvoltage limits.

Table 7-4. VDRV Power Supply Dependency

VDRV	Deploy Function	Off-state Diagnostics	SPI Communication
> $V_{VDRV\_OV\_RISE}$	Not available (1)	Not available	Available
Nominal	Available	Available	Available
< $V_{VDRV\_UV\_FALL}$ & > $V_{VDRV\_UV\_BIAS\_FALL}$	Available (2)	Not available	Available
< $V_{DRV\_UV\_BIAS\_FALL}$	Not available	Not available	Available

(1) Disabled due to VDRV overvoltage detection.
(2) Available, but operates without current control. Drivers will operate in RDSON mode.

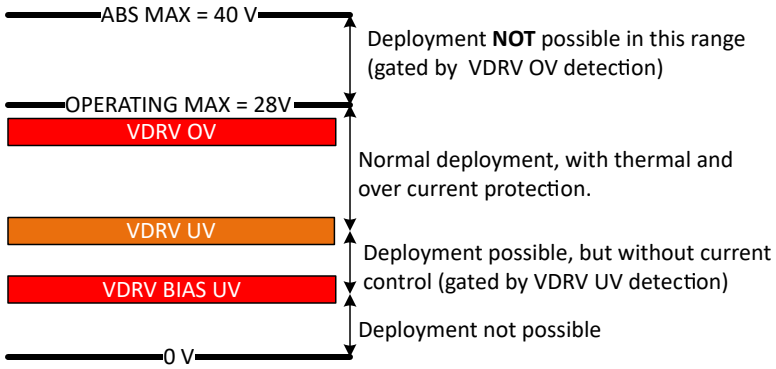


Figure 7-2. VDRV Deploment Operating Regions

Table 7-5 below shows key device functionality with loss of both VDRV and VDD power supplies.

Table 7-5. Loss of VDRV and VDD Power Supply

VDRV	VDD	Deploy Function	Off-state Diagnostics	SPI Communication
< $V_{VDRV\_RST\_FALL}$	< $V_{VDD\_RST\_FALL}$	Not available	Not available	Not available

7.3.2.2 VREG Switch

Certain applications may require the use of a reservoir capacitor in order to ensure deployment of the squib load even in the case of a loss of power (PVDD) event. This can be achieved with an external capacitor connected to the VREG pin with an external diode between PVDD and VREG pins to prevent reverse current flow into the PVDD power supply.

The internal VREG switch of the DRV3901-Q1 helps reduce the voltage drop to the external capacitor due to the blocking diode by having a current limited pull up to PVDD. The VREG switch also enables the monitoring of the external capacitance of the energy reservoir during off-state diagnostics. This functions by opening the switch for a limited time duration and observing the voltage discharge rate of the external capacitor.

The VREG switch is normally closed during operation, but the switch is automatically turned off in two scenarios.

1. Excessive forward voltage bias: VREG < PVDD - V_{VREG_THRS1}
2. Excessive reverse voltage bias: VREG > PVDD + V_{VREG_THRS2}

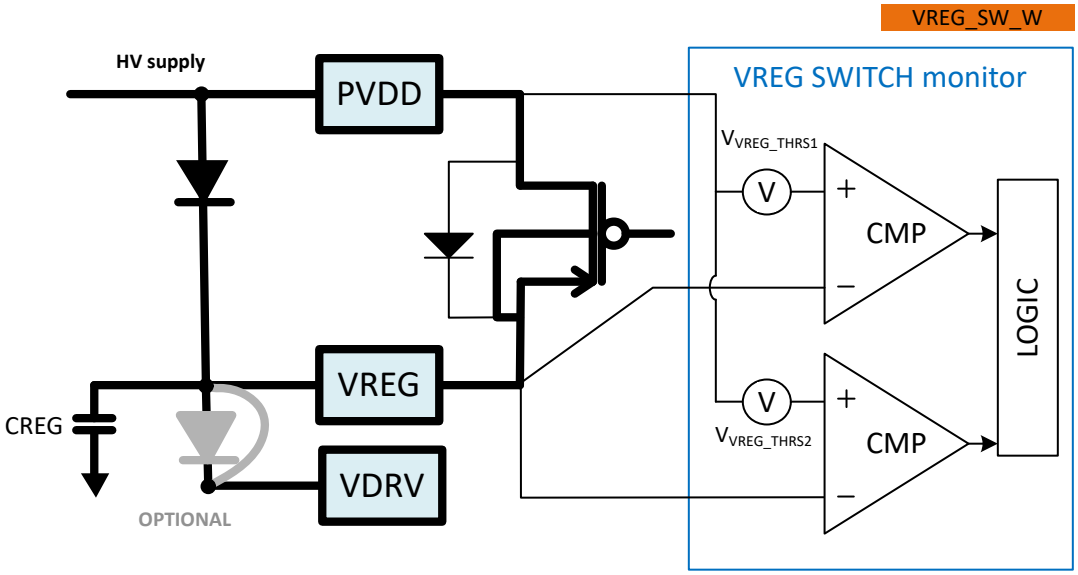


Figure 7-3. VREG Switch and Monitor Diagram

Turning off the switch in the STANDBY state is reported in the SPI warning flag (VREG_SW_W). Note that the VREG switch cannot be used to limit the inrush current during PVDD ramp up and an external diode connection between PVDD and VREG is required.

Note

If VREG_SW_W_DIS = 1b to disable VREG switch warnings (not typical use-case), the off-state diagnostic ABIST should also be disabled (OFF_DIAG_ABIST_DIS = 1b) to avoid a false warning during off-state diagnostics.

7.3.2.3 VDRV Monitor

The device has undervoltage (V_{DRV_UV}) and overvoltage (V_{DRV_OV}) fault monitors, as well as a warning level monitor on the VDRV power supply. The voltage monitor results are recorded in the SPI STATUS registers. In the event of an VDRV overvoltage warning or VDRV undervoltage, the off-state diagnostics are not available. Additionally, there is a bias under voltage monitor ($V_{DRV\_UV\_BIAS}$) with a threshold level below the VDRV

undervoltage monitor. If the VDRV pin voltage drops below $V_{VDRV\_UV\_BIAS\_FALL}$ during deployment, the output drivers are disabled and forced Hi-Z.

7.3.2.4 VDD Monitor

The device has an undervoltage and overvoltage monitor on the VDD power supply. VDD undervoltage or overvoltage are indicated directly in the leading bit of the SDO SPI frame (VDD_ERR) response.

7.3.2.5 Reset (nPOR)

Power on reset (nPOR) for the device logic is based on the internal V5_S derived from the power “OR“ combination of VDRV and VDD. The voltage at which the nPOR reset occurs are described with the V_{DRV_RST} and V_{VDD_RST} parameters.

7.3.2.6 Device Safety Layer

The device safety layer includes a voltage monitor on V5_S, frequency monitor on the main oscillator (f_{OSC}) with a secondary time out logic running on a seperate redundant oscillator (f_{OSC_R}). Any V5_S undervoltage ($V_{5\_S\_UV}$), V5_S overvoltage ($V_{5\_S\_OV}$), f_{OSC} under frequency ($t_{HEART\_BEAT\_H}$), or f_{OSC} overfrequency ($t_{HEART\_BEAT\_L}$) event for a time greater than t_{TIME_OUT} will result in output drivers disabled (Hi-Z) with device lock out fault, DEV_ERR.

7.3.3 Output Driver

The output driver consists of a LS FET between OUTL pin and GND along with a HS FET between OUTH pin and VDRV. On a valid trigger pin (TRGx) or SPI command, the device enters the ACTIVE state for deployment. During this deployment, the HS FET is operated as a current source with the LS FET in RDSON mode. Current sensed from LS FET (shuntless current mirror architecture) is used as feedback to control the HS FET. Current sensed on the LS side is also used to measure the trigger pulse duration. Between the PVDD and VREG pins is an integrated switch to enable a reservoir capacitor diagnostic function.

The device provides several different power supply connections (PVDD, VREG, VDRV) to enable the connection of an optional external reservoir capacitor and / or reverse current blocking diode. To utilize an external reservoir capacitor, a diode should be connected between the PVDD and VREG pins and the reservoir capacitor connected to the VREG pin.

To utilize an external reverse current blocking diode, a diode should be connected between the VREG and VDRV pins. Else the two pins can be tied / shorted together on the PCB.

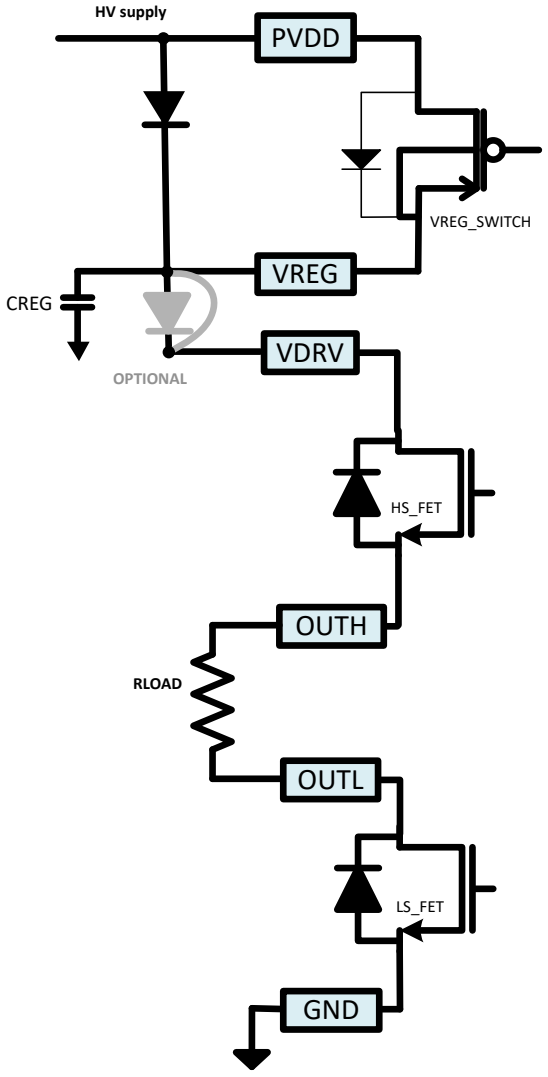


Figure 7-4. Output Driver Diagram

7.3.3.1 STANDBY State

The STANDBY state is the default state of the device with the equivalent driver output state shown below. The device is ready to accept SPI commands to either deploy or to perform off-state diagnostics. The device is also

ready to accept pin triggers (TRGx) commands to deploy. The device current consumption is at minimum in this state. SPI communication, pin triggers, and critical monitoring functions are available. All other functions are disabled to save current consumption.

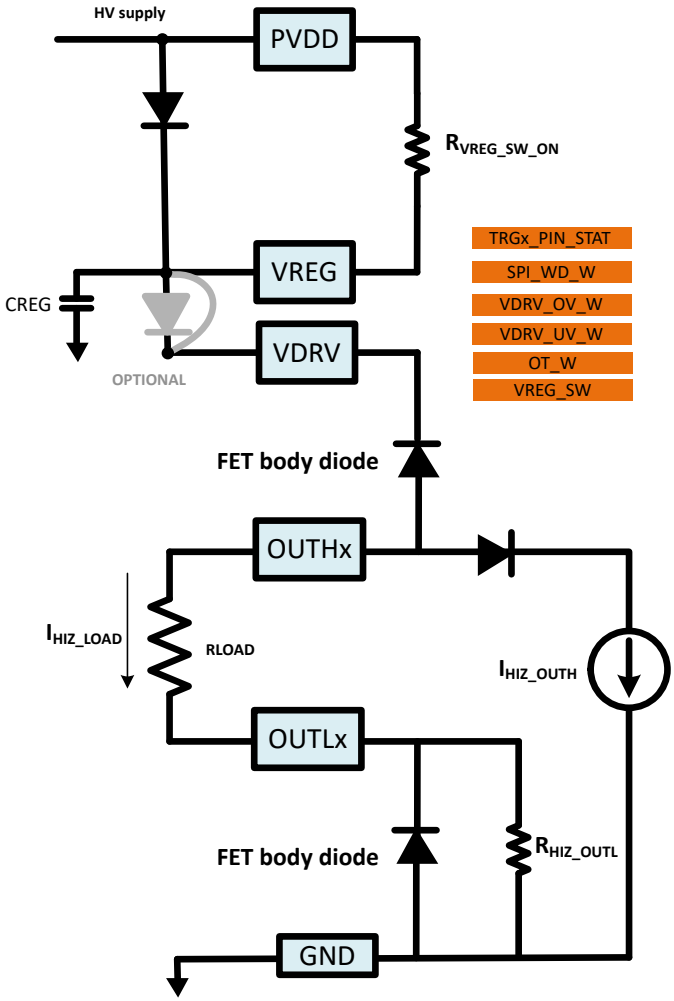


Figure 7-5. Output Driver STANDBY State

7.3.3.2 ACTIVE State

In this state, the device drives the load with the user-configured deploy current profile and time with the equivalent output driver state shown below. In the event of an undervoltage event (VDRV < $V_{VDRV\_UV\_FALL}$, but > $V_{VDRV\_UV\_BIAS\_FALL}$ level), the HS FET will be driven in the RDSON mode (current regulation not possible due to lack of voltage headroom). Below $V_{VDRV\_UV\_BIAS\_FALL}$, outputs are disabled. Additionally, when enabled, the output driver MOSFETs are protected by I_{OCP_LS} and I_{OCP_HS}, as well as thermal shut down.

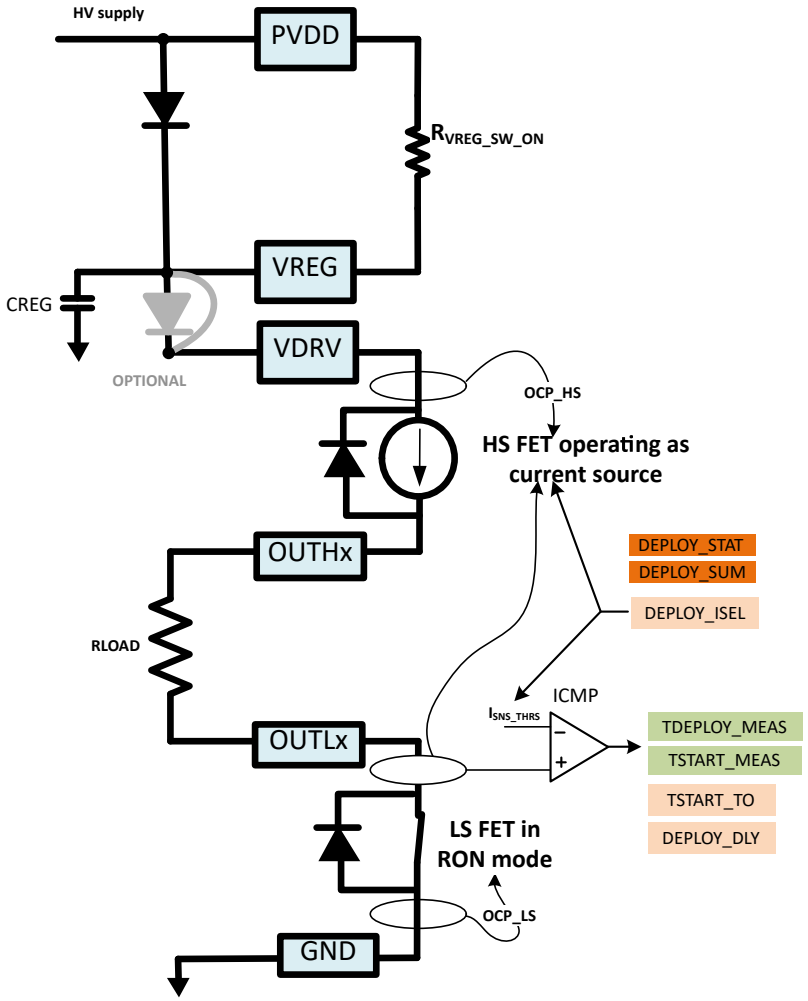


Figure 7-6. Output Driver ACTIVE State

7.3.3.3 Overcurrent Protection

The output driver MOSFETs are protected against pin short circuits on both low-side (I_{OCP_LS}, short to battery) and high-side (I_{OCP_HS}, short to GND) during both active state and off-state diagnostics (FET RDSON and measurement tests) when the MOSFETs are the turned on. Note that the overcurrent threshold levels during off-state diagnostics ($I_{OCP\_HS\_MEAS}$, $I_{OCP\_LS\_MEAS}$, $I_{OCP\_HS\_RDSON}$, $I_{OCP\_LS\_RDSON}$) are significantly lowered to reduce any risks of mis-triggering. Detection of an overcurrent event results in the output driver shut off (Hi-Z) with corresponding fault flagged in the DEPLOY_STAT or OFF_DIAG_STAT STATUS registers.

7.3.3.4 Thermal Protection

The output driver MOSFETs are thermally protected in the event of an over temperature event (T_{TSD}) during active state. Detection of an over temperature event results in disabling the output drivers (Hi-Z) with a fault flagged in the DEPLOY_STAT STATUS register. The device also issues an over temperature warning (T_{TSD_W} and $T_{TSD\_W\_OFF}$) which is set at a lower threshold than thermal shut down. The device can be configured to

switch to lower deploy currents in case of a thermal warning. In the event of an over temperature warning, the off-state diagnostics are not available.

7.3.4 Trigger (TRGx) Pins

The device has two dedicated hardware pins to trigger deployment. The pins have an internal pull-down resistance to GND with filtering. Pin triggering is disabled by default, but can be enabled through a SPI configuration. Both level and PWM based triggering are supported by the device. Triggering options are configured by the TRG_SEL SPI register. All level triggering options are combinational by design (TRG1 + TRG2) to avoid mis-triggering. PWM based triggering enables reliable deployment with a single pin. A dual PWM frequency of 16 KHz and 125 KHz is supported.

SPI based deployment is always available along with the pin-based triggers as an “OR” option unless specifically configured as an “AND” option for additional protection against inadvertent deployment. The different deployment trigger methods are shown below.

Table 7-6. TRG1 + TRG2 Pin Trigger Options (Configured by TRG_SEL)

TRG_SEL	Deployment Trigger Method
0h	Deploy only with SPI command (Trigger pins not used)
1h	Deploy if (TRG1 = Hi **AND** TRG2 = Hi) **OR** SPI command
2h	Deploy if (TRG1 = Hi **AND** TRG2 = Hi) **AND** SPI command
3h	Deploy if (TRG1 = Hi **AND** TRG2 = Lo) **OR** SPI command
4h	Deploy if (TRG1 = Hi **AND** TRG2 = Lo) **AND** SPI command
5h	Deploy only with SPI command (Trigger pins not used)
6h	Deploy only with SPI command (Trigger pins not used)
7h	Deploy only with SPI command (Trigger pins not used)
8h	Deploy if [(TRG1 75% **OR** TRG2 75%) duty cycle @ 16K Hz PWM] **OR** SPI command
9h	Deploy if [(TRG1 25% **OR** TRG2 25%) duty cycle @ 16K Hz PWM] **OR** SPI command
Ah	Deploy if [(TRG1 75% **AND** TRG2 75%) duty cycle @ 16K Hz PWM] **OR** SPI command
Bh	Deploy if [(TRG1 25% **AND** TRG2 25%) duty cycle @ 16K Hz PWM] **OR** SPI command
Ch	Deploy if [(TRG1 75% **OR** TRG2 75%) duty cycle @ 125K Hz PWM] **OR** SPI command
Dh	Deploy if [(TRG1 25% **OR** TRG2 25%) duty cycle @ 125K Hz PWM] **OR** SPI command
Eh	Deploy if [(TRG1 75% **AND** TRG2 75%) duty cycle @ 125K Hz PWM] **OR** SPI command
Fh	Deploy if [(TRG1 25% **AND** TRG2 25%) duty cycle @ 125K Hz PWM] **OR** SPI command

7.3.4.1 PWM Based Trigger

The device can be configured to support a PWM pattern-based trigger for deployment on each TRGx pin individually. PWM frequencies of 16 kHz and 125 kHz are supported.

Two duty cycle configurations are supported:

1. 75% duty cycle – valid deployment trigger, 25% duty cycle - valid no action trigger
2. 25% duty cycle – valid deployment trigger, 75% duty cycle - valid no action trigger

The selection of 75% duty cycle with 16 kHz PWM is recommended for the best compromise between response time and filtering to avoid inadvertent triggering.

The device measures the ON time and OFF time for the pulse of the TRGx pin by using the internal f_{OSC} clock. If two successive cycles match the selected pattern, a valid trigger is registered. Any other type of pulse is considered either a normal operation pulse or a stuck at fault. TRGx_PIN_STAT is updated continuously to indicate trigger pin status.

The figure below is for 75% duty cycle, where the valid cycle check starts on the positive edge of the TRGx pin. The ON time is compared to configured window threshold set by PWM_FLTR_SEL. The OFF time is compared to a dynamic limit set by the ON time measurement.

For the 25% duty cycle, the input to this logic is inverted to maintain the same implementation, so the valid cycle check starts on the negative edge of the TRGx pin in this case.

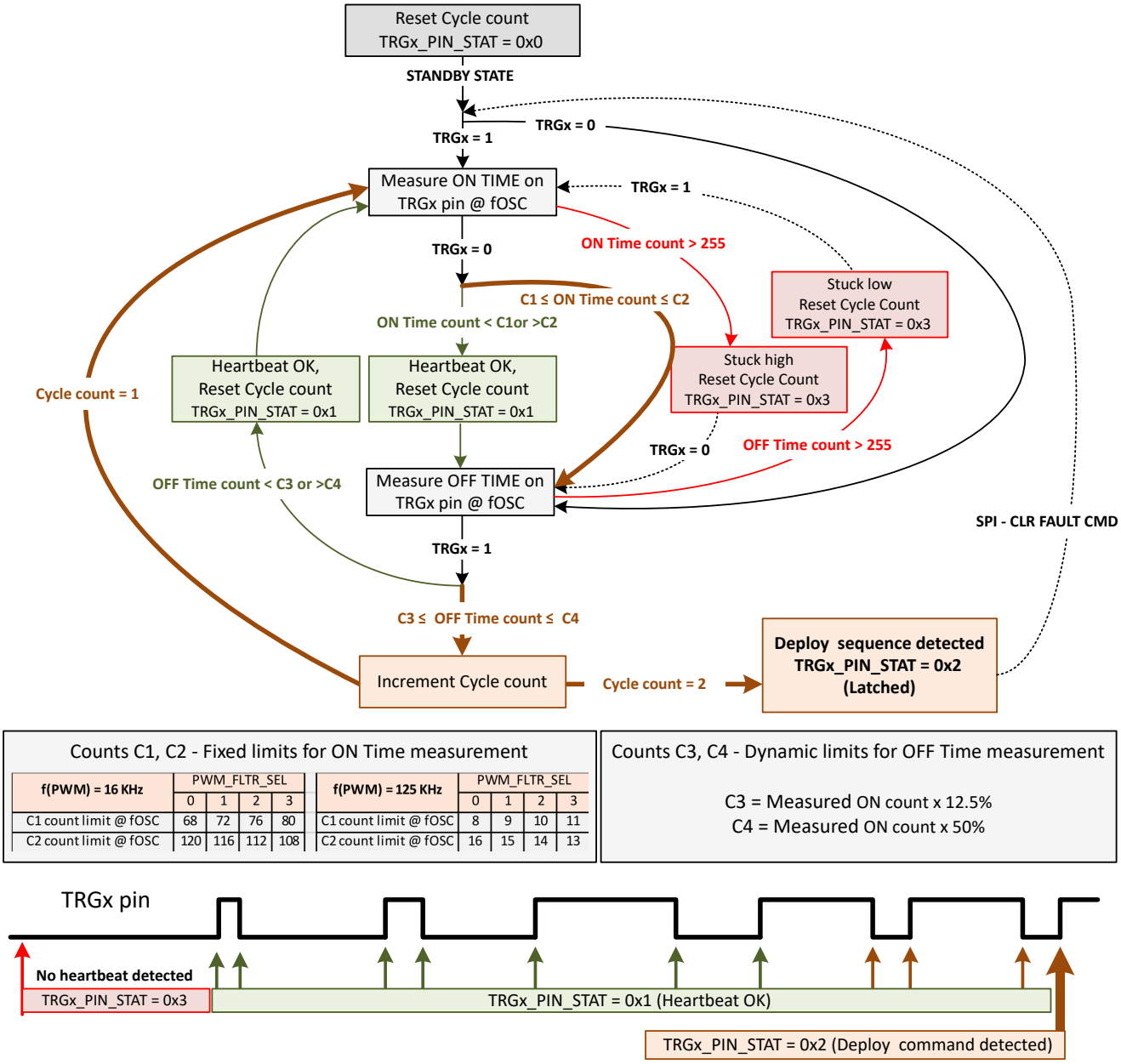


Figure 7-7. PWM Based Triggering

7.3.4.2 Trigger Monitors

The device provides several monitoring options of the TRG1 and TRG2 pins to verify the health of the input trigger signals to the device. This information is displayed in the STATUS registers, in register fields TRG1_PIN_STAT, TRG2_PIN_STAT, TRG1_PIN_LVL1, and TRG1_PIN_LVL2. These status registers are for feedback only and the device takes no action based on them.

The TRGx_PIN_STAT registers display a status based on the selection of the trigger interface mode (TRG_SEL). The feedback of the TRGx_PIN_STAT register is defined in the table below.

The TRG1_PIN_LVL1 and TRG1_PIN_LVL2 are a simple real time level status of the TRG1 pin.

Table 7-7. TRG1_PIN_STAT and TRG2_PIN_STAT Modes

TRG_SEL	TRG1_PIN_STAT	TRG2_PIN_STAT
0h	3h (SPI Trigger)	3h (SPI Trigger)
1h	0h = No data available yet 1h = Pin high 2h = Pin low 3h = Reserved	0h = No data available yet 1h = Pin high 2h = Pin low 3h = Reserved
2h		
3h		
4h		
5h	3h (SPI Trigger)	3h (SPI Trigger)
6h	3h (SPI Trigger)	3h (SPI Trigger)
7h	3h (SPI Trigger)	3h (SPI Trigger)
8h - Fh	0h = No data available 1h = PWM heartbeat signal detected 2h = PWM valid deploy signal detected (pattern match) 3h = PWM heartbeart signal missing (stuck high or low)	0h = No data available 1h = PWM heartbeat signal detected 2h = PWM valid deploy signal detected (pattern match) 3h = PWM heartbeart signal missing (stuck high or low)

7.3.5 Deploy Parameters

The deployment current pulse duration (t_{DEPLOY}) and level (I_{DEPLOY}) can be configured by the user in the SPI CONFIG registers. The rate of rise of the current pulse (I_{RISE}) is controlled internally. It can be slowed down further if needed with an external series inductor.

There are two internal timers with 500 ns time resolution that are triggered when deployment occurs. The timer values are recorded in the MEAS registers at the end of the deployment.

1. **TSTART_MEAS** - This is a measure of the time from the deploy command until the load current crosses the sense threshold (I_{SNS_THRS}) or expiration of the user configured TSTART_TO timer. User configured DEPLOY_DLY time is not included in this measurement. The deploy duration timer t_{DEPLOY} is started at the end of TSTART_MEAS. The TSTART_TO sets the timeout for the TSTART_MEAS timer, in the case that I_{SNS_THRS} is not detected within the timeout window.
2. **TDEPLOY_MEAS** - This is a measure of the time when the deploy current is ≥ I_{SNS_THRS} during t_{DEPLOY}

Figure 7-8 below demonstrates a normal deployment scenario along with the measurement timers.

1. Based on TRG_SEL register configuration, SPI deployment command registered and validated with nSCS rising or PWM / voltage level on the TRGx pins.
2. This is followed by the user configurable delay set by DEPLOY_DLY register.
3. The output driver MOSFETs are enabled (LS FET is turned on, followed by the HS FET).
4. DEPLOY_ISEL sets the deploy current level (I_{DEPLOY}) and deploy duration (t_{DEPLOY}), while the rise (di/dt) time of the load current (I_{RISE}) is set by the DEPLOY_IRATE register.

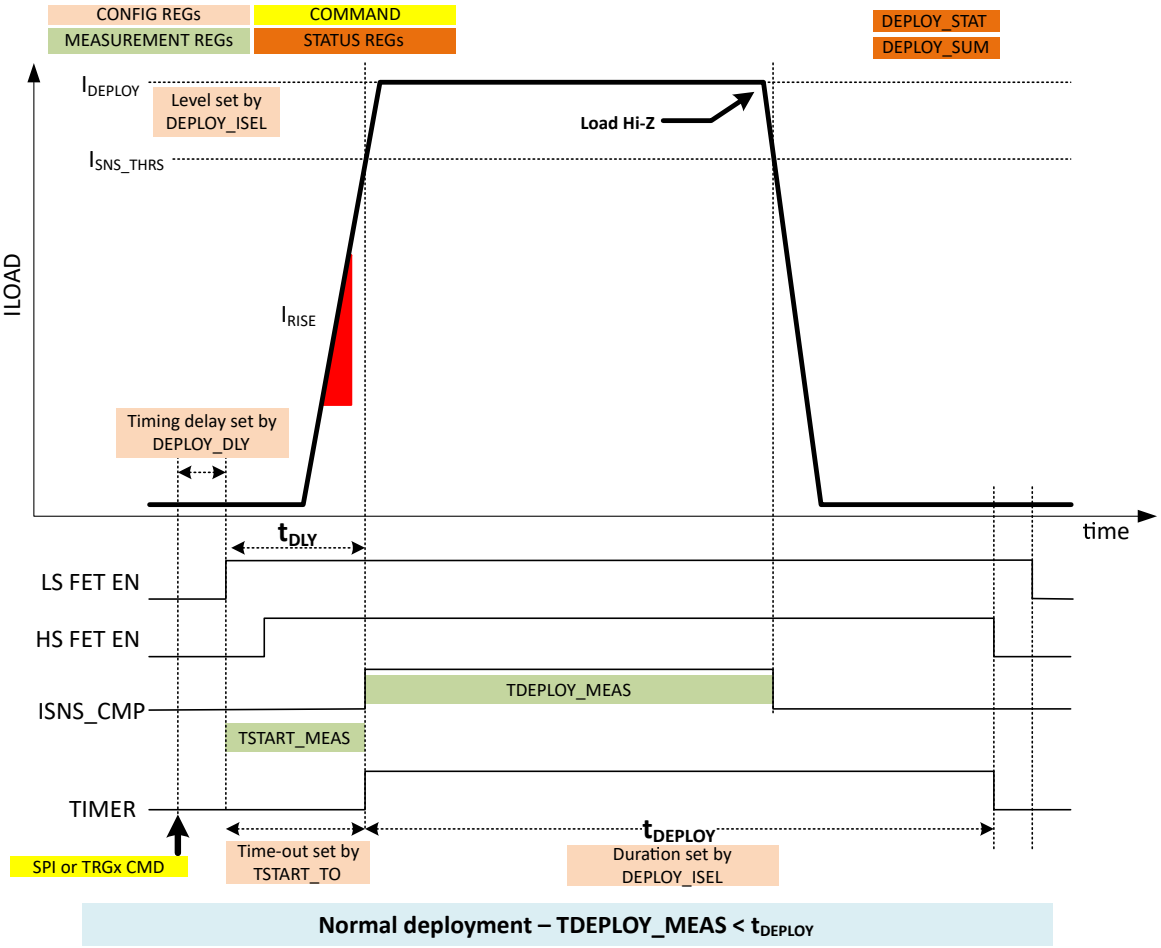


Figure 7-8. Typical Deployment with TDEPLOY_MEAS < t_{DEPLOY}

Behavior of the measurement timers for some of the example abnormal deployment cases are shown below.

TDEPLOY_MEAS is a measure of the time when the deploy current (I_{DEPLOY}) is ≥ ISNS_THRS. In Figure 7-9 below, the timer is paused whenever the deploy current drops below the I_{SNS_THRS} level during deployment.

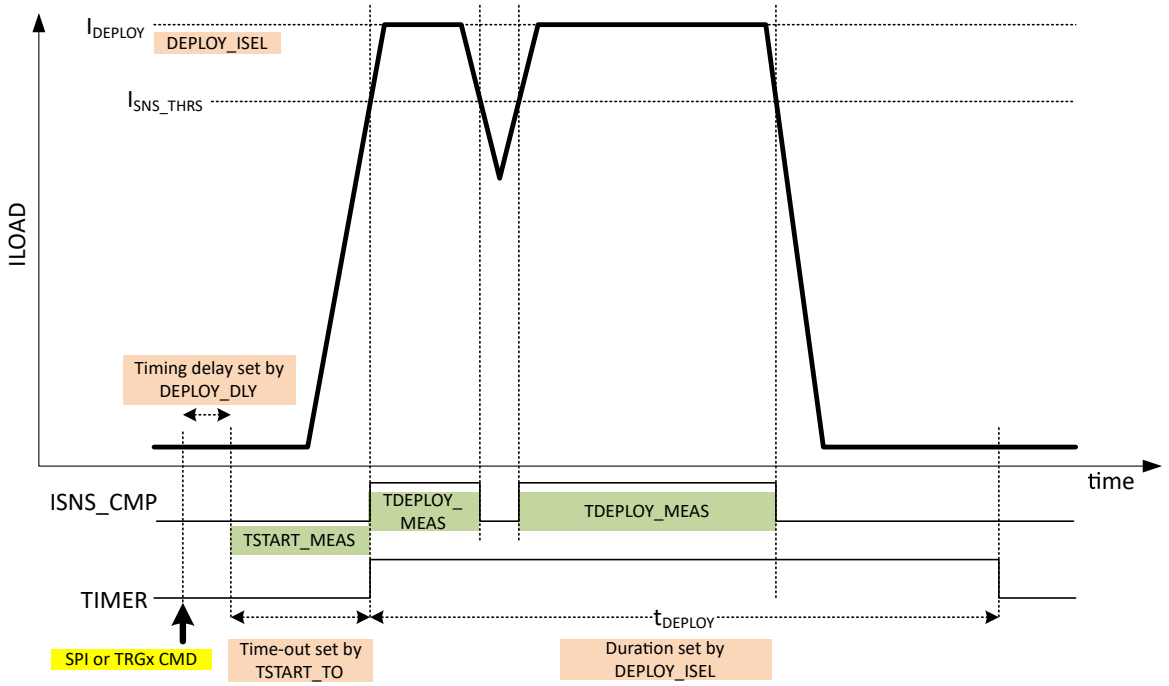


Figure 7-9. Abnormal Deployment Example (Deploy Current Drop)

At the end of the t_{DEPLOY} duration, the deployment is stopped even if the load current has not dropped below the I_{SNS_THRS} threshold. This is shown in Figure 7-10, where the TDEPLOY_MEAS is almost the value of t_{DEPLOY}.

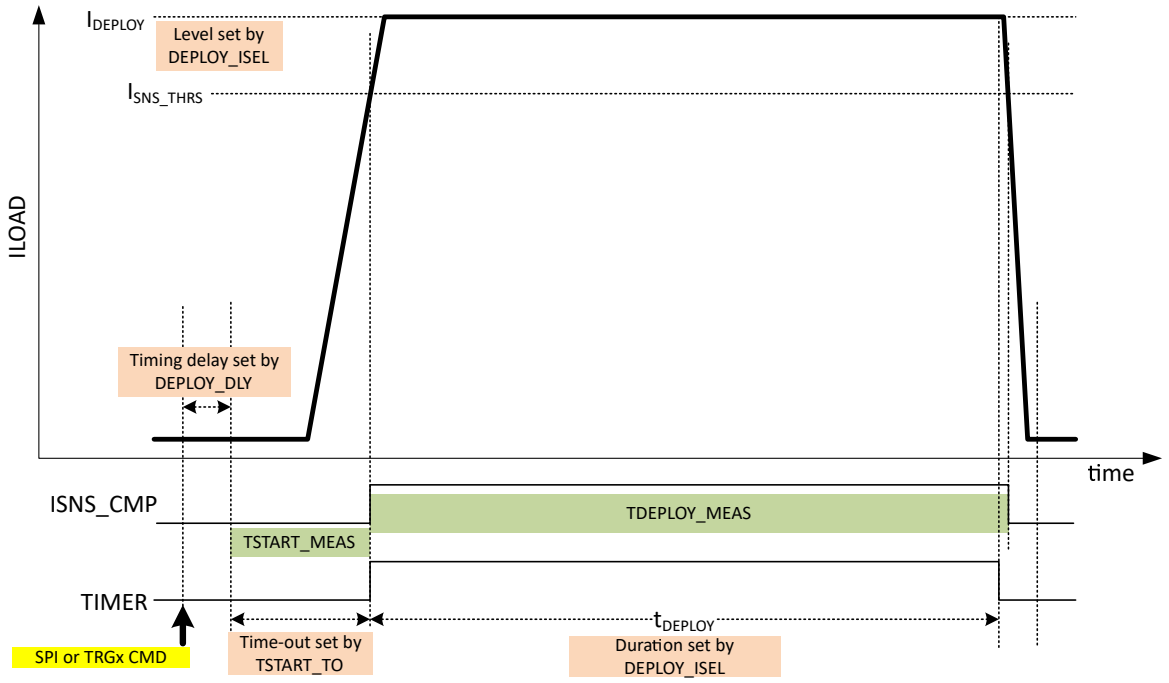


Figure 7-10. Abnormal Deployment Example (Deploy Time Expires)

In the event I_{SNS_THRS} does not occur, within the time set by TSTART_TO register once the output driver MOSFETs are enabled, a time out event is recorded in the DEPLOY_STAT STATUS register. In this event, the TSTART_MEAS register will measure the same as TSTART_TO register value. The TDEPLOY_MEAS register value is still valid.

7.3.5.1 Deploy Delay

On a valid SPI command (CMD1 or broadcast CMD2), pin trigger (TRGx), or a combination of the two (set by TRG_SEL), the device will initiate deployment with the t_{DLY0} or t_{DLY1} duration. This time is measured from the time the command has been registered (rising edge of nSCS pin) to the time when the load current > I_{SNS_THRS}, without any additional user configured delay.

Additionally, the device offers a programmable delay (t_{DEPLOY_DLY}) to synchronize deployment of multiple drivers on the same addressed SPI bus. The delay time (DEPLOY_DLY register) can be configured as follows and can be independently enabled for SPI based deployment (ACTIVITY_CTRL register for normal SPI and DEPLOY_DLY_EN register for broadcast SPI) and for pin based trigger (PIN_DEPLOY_DLY_EN register).

Table 7-8. Deployment Delay for Different Trigger Selections

Trigger Selection	Pin Delay	SPI Delay	Deployment Delay
Only SPI (TRG_SEL = 0h, 5h-7h)	Don't care	Disabled	No delay
		Enable	Delay as per DEPLOY_DLY register setting
SPI **OR** TRGx pin (TRG_SEL = 1h, 3h, 8h-Fh)	Disabled	Disabled	No delay
	Disabled	Enable	Delay as per DEPLOY_DLY setting only if SPI command is received first
	Enable	Disabled	Delay as per DEPLOY_DLY setting only if TRGx pin trigger is received first
	Enable	Enable	Delay as per DEPLOY_DLY setting
SPI **AND** TRGx pin (TRG_SEL = 2h, 4h)	Disabled	Disabled	No delay
	Disabled	Enable	No delay
	Enable	Disabled	No delay
	Enable	Enable	Delay as per DEPLOY_DLY setting after both SPI command and TRG pin trigger

7.3.6 Off-State Diagnostics

From the STANDBY state, the device can be commanded to perform off-state diagnostics with a valid SPI command. The diagnostics include a series of sequenced, self-timed tests that check the availability of the deployment function without creating a risk of inadvertent deployment.

Failure in any of the first six tests results in aborting the off-state diagnostics at the instant of the failure. Off-state diagnostics function is not available in case of VDRV undervoltage, VDRV overvoltage warning, or over temperature warning. The results are captured in the STATUS registers, OFF_DIAG_STAT and OFF_DIAG_SUM.

At any time during off-state diagnostics, the device can accept a valid pin TRG or SPI command to deploy. At this point, the device will abort the diagnostics instantly in controlled manner and transition to ACTIVE state for deployment. The deployment delay parameters t_{DLY0} and t_{DLY1} times are still maintained.

The sequence of tests and their objective is as follows:

1. Device BIST: Device BIST to qualify the monitors.
2. Weak Pull-Up Test: Detect an impedance to ground.
3. Weak Pull-Down Test: Detect an impedance to supply.
4. HS RDSON Test (disabled by default): Device high-side MOSFET check
5. LS RDSON Test (disabled by default): Device low-side MOSFET check.
6. IREF Resistance Monitor: Resistance measurement check for external IREF pin resistor.
7. VREG Voltage and Capacitance Measurement: Measures the voltage on VREG (BIST included) with respect to PVDD and reports the discharge rate of the capacitor on VREG with a controlled current sink in order to estimate the capacitance on the pin.
8. Load Resistance Monitor: Check the resistance of the output squib load. (typically 2 Ω).

The sequence of the tests cannot be changed, but individual tests can be disabled through the CONFIG registers.

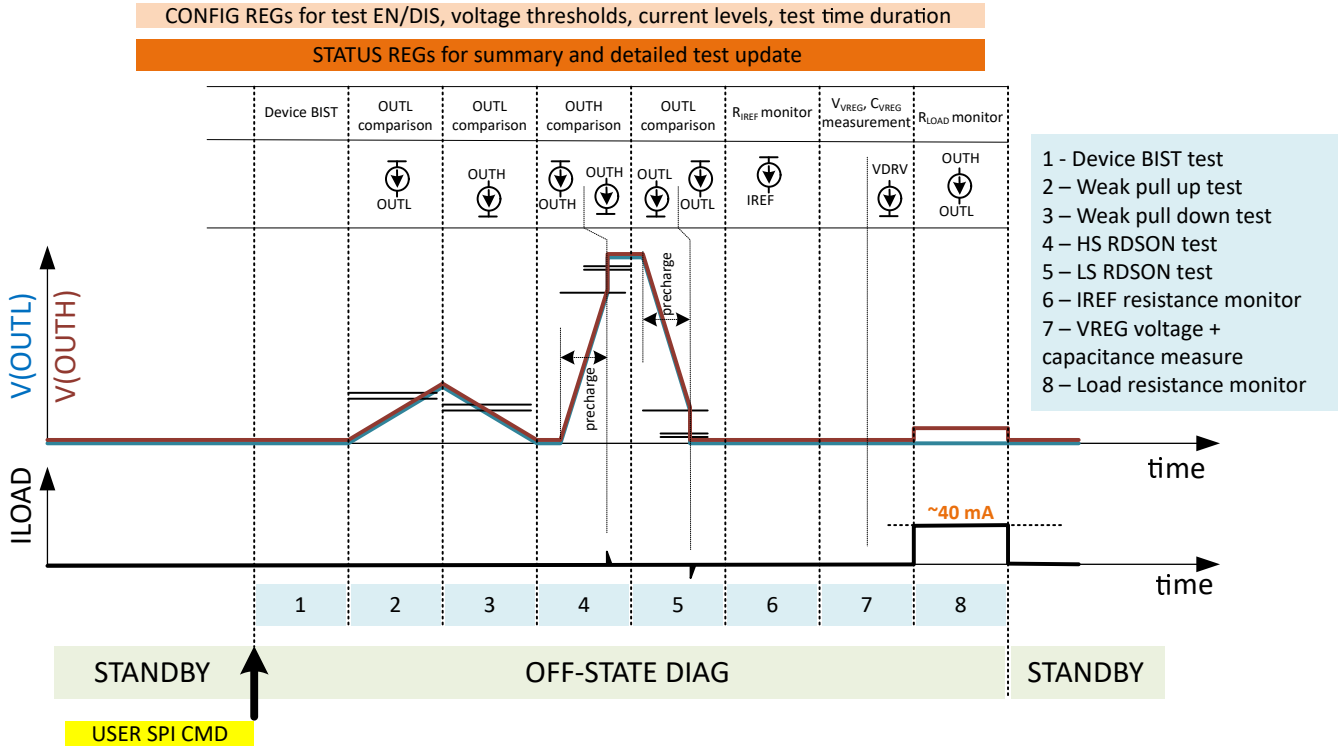


Figure 7-11. Off-State Diagnostic Sequence

During device operation, the following 3 combinations are recommended to conduct the off-state diagnostics:

1. **Startup check:** All tests to validate the health of the device, load, and qualify the monitors.
2. **Periodic check:** Weak pull up, weak pull down, VREG voltage & capacitance measurements, and load resistance monitor to validate the availability of the deployment function.
3. **Post deployment check:** Load resistance monitor only to validate that initiator has been deployed.

7.3.6.1 Device BIST

This built-in-self-test checks the integrity of the comparators used for power supplies, diagnostics, and current sense.This is a self timed test completed with t_{BIST} duration. User can skip this test with register OFF_DIAG_ABIST_DIS = 0x1.

A failure within this test results in abortion of the off-state diagnostics sequence and is reported as OFF_DIAG_STAT = 0x8 in the STATUS registers.

7.3.6.2 Weak Pull-Up Test

With the driver disabled (Hi-Z), this test forces a user-configured pull up current ($I_{REF\_WK\_PU}$) on OUTL and compares the voltage on OUTL with an internal reference ($V_{REF\_WK\_PU}$) with a user configured time out (t_{WK_PU}). The intent is to detect to any signficant, unintended impedance to ground on the output that may impede the deployment function. A test failure results in abortion of off-state diagnostics and is reported as OFF_DIAG_STAT = 0x9 in the STATUS registers.

User can skip this test with register OFF_DIAG_WK_PU_DIS = 0x1.

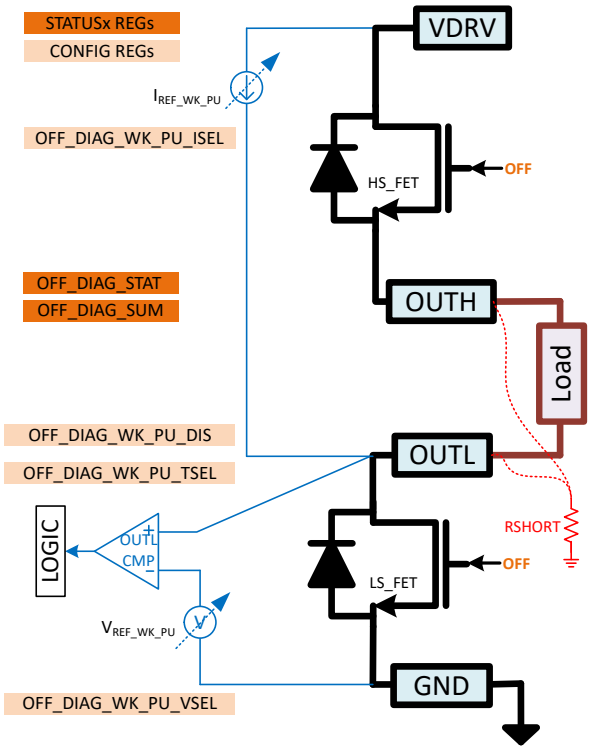


Figure 7-12. Weak Pull-Up Test Diagram

7.3.6.3 Weak Pull-Down Test

With the driver disabled (Hi-Z), this test forces a user-configured pull down current ($I_{REF\_WK\_PD}$) on OUTH and compares the voltage on OUTL with an internal reference ($V_{REF\_WK\_PD}$) with a user configured time out (t_{WK_PD}). The intent is to detect any significant unintended impedance to the high voltage supply on the output that may impede the deployment function. A test failure results in abortion of off-state diagnostics and is reported as OFF_DIAG_STAT = 0xA in the STATUS registers.

User can skip this test with register OFF_DIAG_WK_PD_DIS = 0x1.

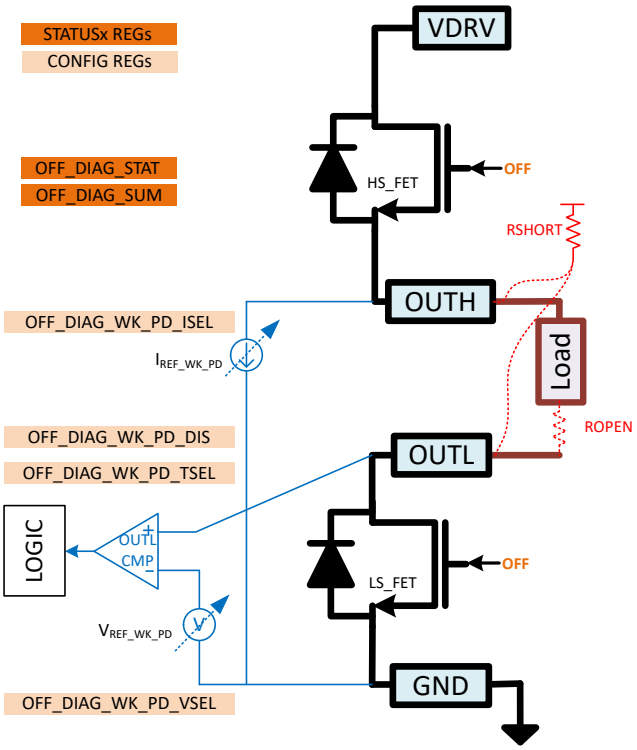


Figure 7-13. Weak Pull-Down Test Diagram

7.3.6.4 High-Side MOSFET RDSON Test

There are two parts to this test. First, with the driver disabled (Hi-Z), this test forces a pull up current ($I_{REF\_PC\_HSRDSON}$) on OUTH until the output has reached a voltage close to VDRV pre-charge ($V_{REF\_PC\_HSRDSON}$). After this, only the high-side (HS) MOSFET switch is turned on with an user configured pull down current ($I_{REF\_HSRDSON}$) on OUTH and the drain to source voltage of the HS MOSFET switch is compared to an internal reference ($V_{REF\_HSRDSON}$). The test has a user configured time out ($t_{HSRDSON}$). The HS MOSFET is protected by $I_{OCP\_HS\_RDSON}$ to ensure the MOSFET is switched off in the case of a short-circuit on the output.

A test failure results in abortion of off-state diagnostics and is reported as OFF_DIAG_STAT = 0xB in the STATUS registers with additional information in the OFF_DIAG_STAT_MISC register to differentiate between a pre-charge time out or RDSON failure.

While the user can skip this test with register OFF_DIAG_HS_RDSON_DIS = 0x1, it is recommended to skip both the LS and HS MOSFET switch tests together, and not skip only the LS or HS test.

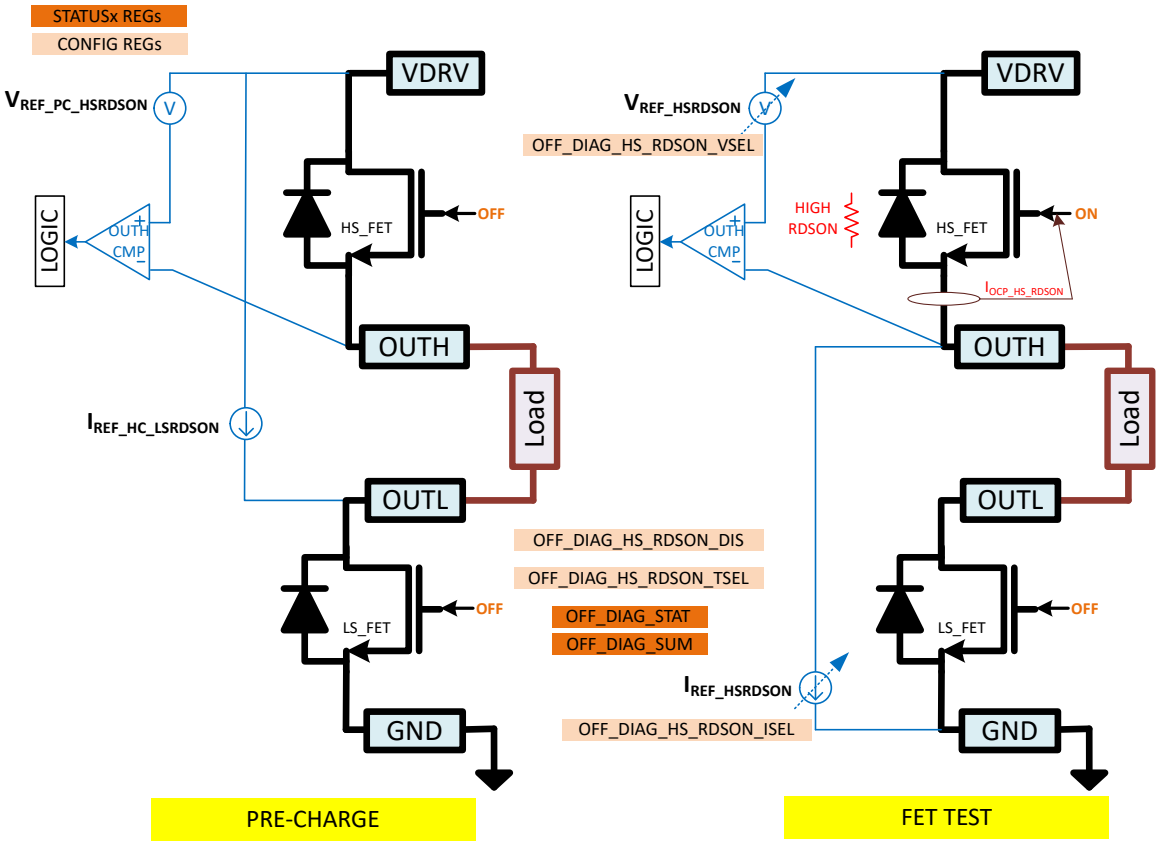


Figure 7-14. HS MOSFET RDSON Test Diagram

7.3.6.5 Low-Side MOSFET RDSON Test

There are two parts to this test. First, with the driver disabled (Hi-Z), this test forces a pull down current ($I_{REF\_PC\_LSRDSON}$) on OUTL until the output has reached a voltage close to GND pre-charge ($V_{REF\_PC\_LSRDSON}$). After this, only the low-side (LS) switch is turned on with an user configured pull up current ($I_{REF\_LSRDSON}$) on OUTL and the drain-source voltage of the LS switch is compared to an internal reference ($V_{REF\_LSRDSON}$). The test has a user configured time out ($t_{LSRDSON}$). The LS MOSFET is protected by $I_{OCP\_LS\_RDSON}$ to ensure the MOSFET is switched off in case of a short-circuit on the output.

A test failure results in abortion of off-state diagnostics and is reported as OFF_DIAG_STAT = 0xC in the STATUS registers with additional information in the OFF_DIAG_STAT_MISC register to differentiate between pre-charge time out or RDSON failure.

While the user can skip this test with register OFF_DIAG_LS_RDSON_DIS = 0x1, it is recommended to skip both the LS & HS MOSFET switch tests together, and not skip only the LS or HS test.

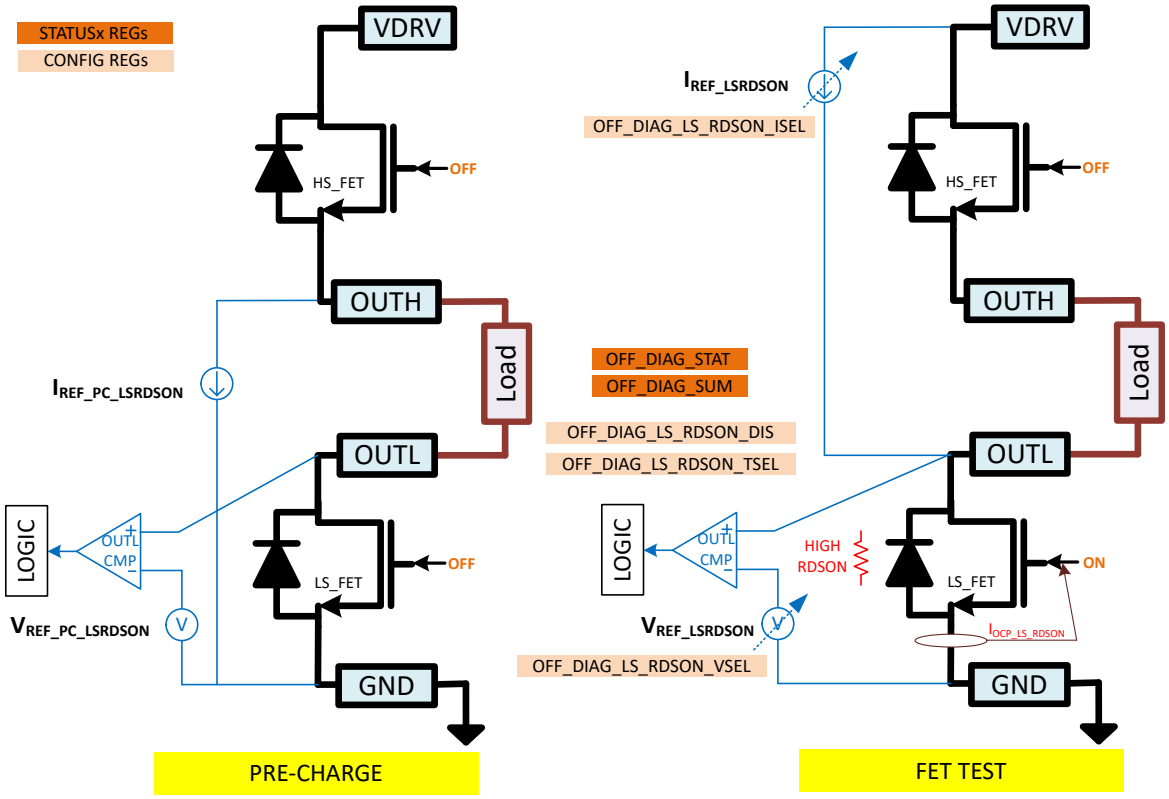


Figure 7-15. LS MOSFET RDSON Test Diagram

7.3.6.6 IREF Resistance Monitor

The intent of this test is to qualify the resistance measurement circuitry with a pass/fail criteria based on the assumption of a 10 kOhm resistor on the IREF pin. With the driver disabled (Hi-Z), this self-timed (t_{IREF_MEAS}) test forces a current (I_{REF}) on the external IREF pin to generate a voltage input to an internal resistance measurement block, which consists of a gain buffer, 5-bit voltage DAC and comparator. The DAC is swept through all the codes and the trip point is recorded in RIREF_MEAS in MEAS2 register. If the measured code falls outside the range for a 10 kOhm resistor, the test is recorded as a fail. This results in abortion of the off-state diagnostics and gets reported in the STATUS registers as OFF_DIAG_STAT = 0xD.

Additionally, the LS MOSFET is protected by overcurrent protection $I_{OCP\_LS\_MEAS}$ to ensure the MOSFET is switched off in case of a short-circuit on the output. Occurance of a LS overcurrent results in abortion of the off-state diagnostics and gets reported in the STATUS register as OFF_DIAG_STAT = 0xE.

User can skip this test with register OFF_DIAG_IREF_DIS = 0x1.

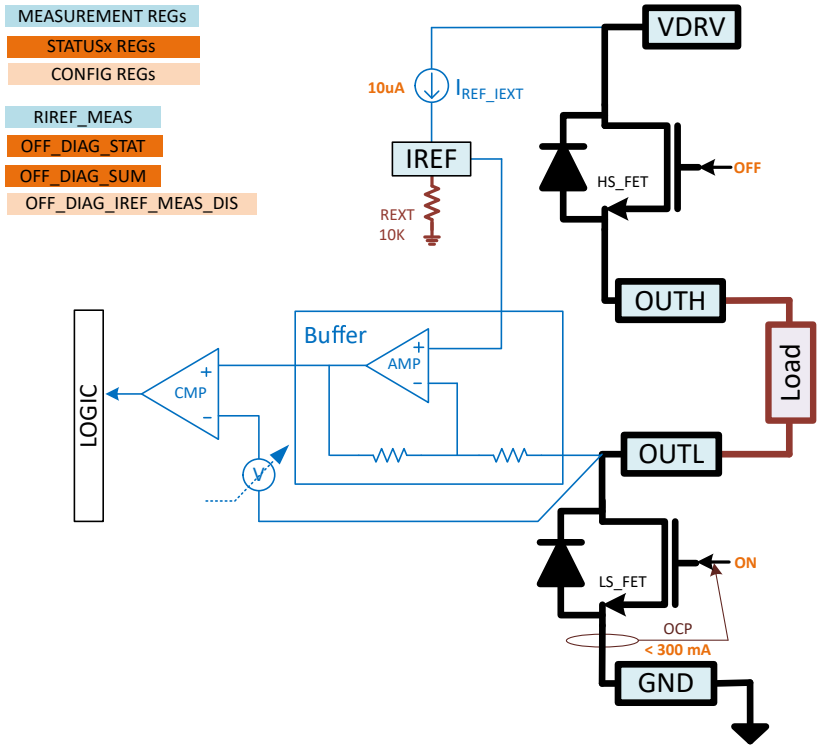


Figure 7-16. IREF Resistance Monitor Diagram

7.3.6.7 VREG Voltage and Capacitance Measurement

There are two parts to this test. First a voltage measurement on the VREG pin, which is then followed is then followed by a capacitance measurement on the VREG pin.

Voltage measurement: With the driver disabled (Hi-Z) and the VREG_SW closed, there is a 4 ms settling time to allow for the voltage on the VREG pin to settle from the prior tests. This is followed by a voltage measurement sequence involving a 3-bit DAC, comparator (CMP) and logic that sweeps the DAC codes (V_{DAC_VREG}) to estimate the voltage on the VREG pin. The result is reported in STATUS register OFF_DIAG_STAT either as normal, with the voltage value recorded in VREG_MEAS in STATUS3 register, or a voltage low failure, with the subsequent capacitor measurement skipped. This is a self-timed test (t_{VREG_VMEAS}). A second comparator (CMP_R) with a fixed offset to the CMP comparator is used for additional confirmation measures. An invalid comparator output combination results in abortion of the off-state diagnostics and gets reported as OFF_DIAG_STAT = 0xD in the STATUS registers.

Capacitance measurement: With the driver disabled (Hi-Z) and VREG_SW opened, a controlled pull down current (I_{VDRV_DIAG}) is forced on VDRV pin causing VREG to discharge slowly. The start reference of CMP comparator is set by user configured threshold (V_{DAC_VREG}), set by registers OFF_DIAG_CMEAS_THRS_SEL or OFF_DIAG_CMEAS_THRS_AUTO. When this comparator trips, a timer is started and the comparator reference is switched to a fixed lower value V_{DIFF}. The timer is stopped when the comparator trips again. This discharge time is recorded in T_VREG_CAP in STATUS3 register. The duration, t_{CMEAS}, is set by the OFF_DIAG_CMEAS_TSEL register, with an additional set up time t_{CMEAS_SETUP} for opening time of the VREG switch and settling time for the pull down current. The user can estimate the capacitance on VREG pin based on the difference in the comparator tripping time, along with the fixed voltage threshold (V_{DIFF}) and pull down current (I_{VDRV_DIAG}).

User can skip this test (both parts) with register OFF_DIAG_VREG_MEAS_DIS = 0x1.

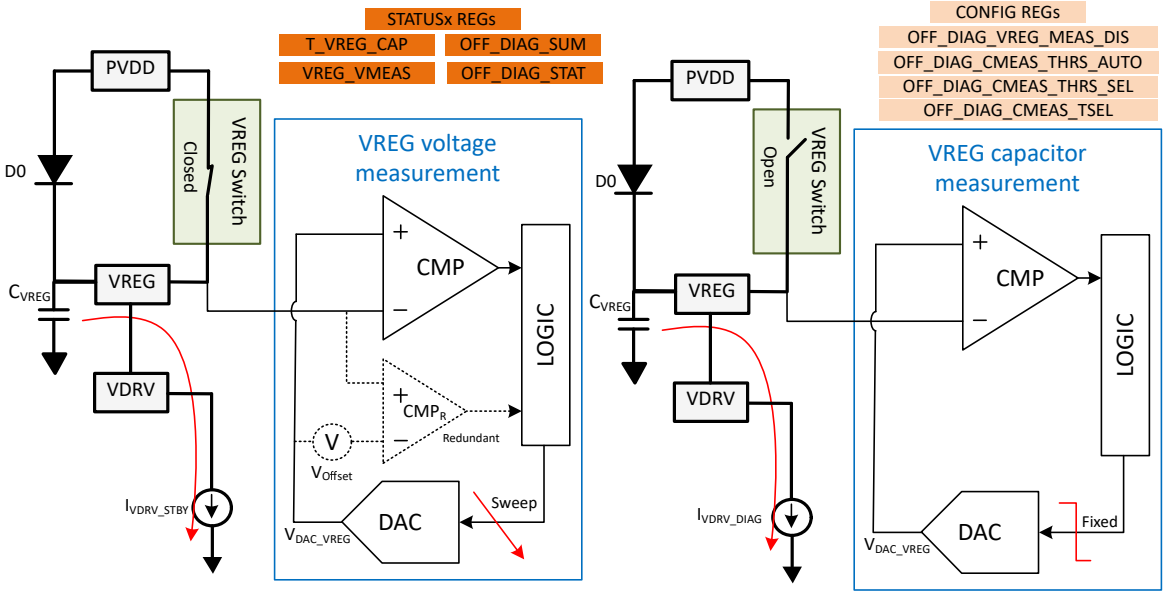


Figure 7-17. VREG Voltage and Capacitance Measurement Diagram

Table 7-9. Reservoir Capacitor T_VREG_CAP Calculations

T_VREG_CAP	Result	Calculation
00h	Timer start did not occur, value not determined.	N/A
01h - 31h	Timer start and stop occurred	Cap value = T_VREG_CAP (register value decimal) x timer resolution x 1.16
31h - 3Fh	Timer start occurred but stop did not occur.	Cap value (Farad) > T_VREG_CAP (register value decimal) x timer resolution x 1.16

Timer resolution = OFF_DIAG_CMEAS_TSEL (0.5ms, 1ms, 2ms, 4ms) / 32. Can also refer to T_VREG_CAP register description in the STATUS3 section to understand how different start-stop timer scenarios can be inferred.

Note

In the case of a result of T_VREG_CAP > 31h (timer start occurred by stop did not occur), the device will register VREG_SW_W = 2h. This can be reset by issuing a clear fault command (CLR_FAULT) after the diagnostic.

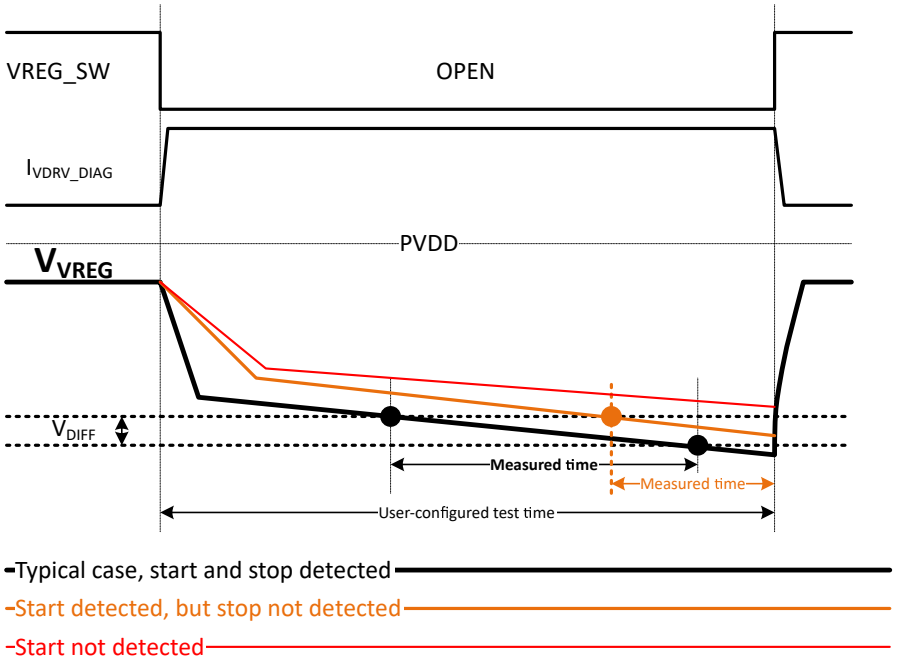


Figure 7-18. VREG Voltage and Capacitance Measurement Example

7.3.6.8 Output Load Resistance Monitor

This user-timed test monitors the output load resistance across the OUTx pins and issues either a normal or fail high / fail low warning, reported in the OFF_DIAG_STAT register. For measuring the load resistance, the HS FET is configured as a current source (I_{RMEAS}) with the LS FET in RDSON mode with a lowered overcurrent limit. The voltage is amplified with a buffer and is compared with two different thresholds, one configured by OFF_DIAG_RMEAS_THRS_L_SEL register for low threshold check (R_{MEASL}) and other configured by OFF_DIAG_RMEAS_THRS_H_SEL register for high threshold check (R_{MEASH}). The duration of this test, t_{RMEAS}, is set by OFF_DIAG_RMEAS_TSEL register.

The output driver MOSFETs are protected by overcurrent protection, $I_{OCP\_LS\_MEAS}$ and $I_{OCP\_HS\_MEAS}$ to ensure the MOSFETs are switched off in case of a short-circuit on the output. Occurance of a LS or HS overcurrent results in abortion of off-state diagnostics and gets reported in the STATUS registers as OFF_DIAG_STAT = 0xE / 0xF respectively.

Additionally, an invalid comparator output combination results in abortion of off-state diagnostics and gets reported in the STATUS registers as OFF_DIAG_STAT = 0xD. Users can skip this test with register OFF_DIAG_RMEAS_DIS = 0x1.

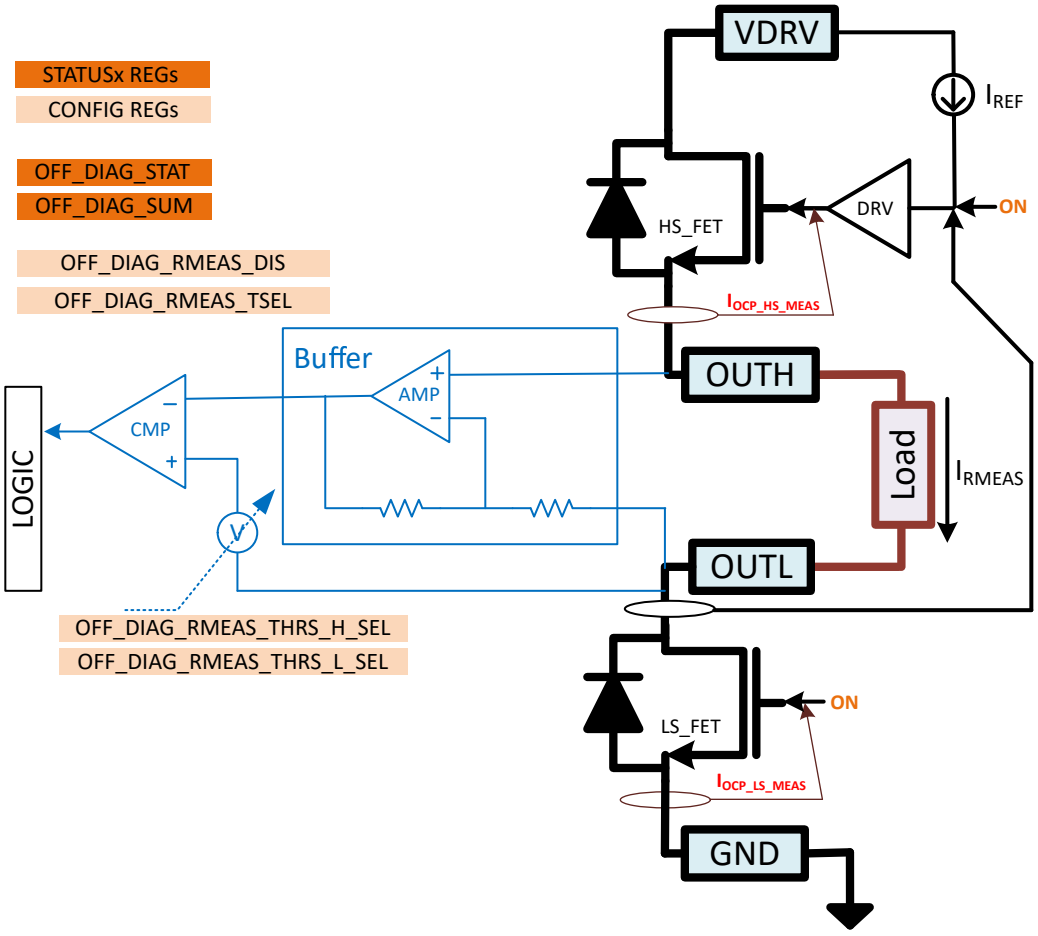


Figure 7-19. Output Load Resistance Monitor Diagram

7.3.7 SPI Watchdog Monitor

The device has an integrated SPI watchdog monitor which gets reset after any valid SPI (read or write) frame within the watchdog timer window (t_{WD}). The watchdog timer window can be configured with the SPI_WD_SEL CONFIG register. The warning can be disabled through the SPI_WD_W_DIS register.

7.3.8 nFAULT/NAD Pin

The nFAULT/NAD pin is a dual purpose open-drain pin with an external pull up resistor is used for node address (NAD) determination during the device power-up initialization and then for fault or device STATE communication (asserted low) during operation.

The device node address (NAD) is set with an external pull up resistor. Four unique addresses can be set with 5.6, 12, 27, and 56 kOhm resistors (R_{LVL}).

The nFAULT/NAD pin can be setup to indicate different fault conditions. Refer to the nFAULT_CONFIG register for which faults are asserted on the nFAULT/NAD pin and how these can be configured.

7.3.9 Fault Tables

The next sections describe the various device protection and diagnostic functions including the configuration options, response options, and recovery options. Detailed safety mechanism (SM) descriptions, classifications, and detection coverage can be found in the device safety manual.

7.3.9.1 General Device Faults

This table summarizes the faults and fault responses during the power up initialization (INIT1 and INIT2) states and STANDBY state.

Table 7-10. General Device Fault Table

Fault	Safety Mechanism	Configure	Device State	Enable / Disable	nFAULT Assertion	SPI Status	Deploy Function	Recovery
SPI Watchdog Violation	SM_SPI_WD	SPI_WD_SEL	Except INITx	Disable, SPI_WD_W_DIS = 0x1	No	N/A	Available	N/A
				Enable, SPI_WD_W_DIS = 0x0	Yes, if NFAULT_CONFIG1 = 0x1	SPI_WD_W	Available	CLR_FAULT command
VDD Undervoltage	SM_VDD_UV	VDD_UV_FILTER	All	Always enabled	No	SDO VDD_ERR	Available	Auto recover
VDD Overvoltage	SM_VDD_OV	VDD_OV_FILTER	All	Always enabled	No	SDO VDD_ERR	Available	Auto recover
Node Address Resistance Out of Range	SM_NAD_MON	N/A	INIT2	Always enabled	No	SDO NAD_ERR	Not available	RE_INIT_NAD broadcast command
Node Address SDO Bus Conflict	SM_NAD_MON	N/A	Except INIT1	Always enabled	No	SDO NAD_ERR	Not available	NAD_OVERRIDE broadcast command
SPI Command CRC or Frame Length Violation	SM_SPI_CMD_CRC	N/A	Except INIT1	Always enabled	No	SPI_ERR	Available	Next valid SPI frame
CRC Violation of CONFIG Registers	SM_CONFIG_CRC	N/A	Except INIT1	Always enabled	No	CONFIG_CRC_W	Available	Correct CRC entered
Power On Reset	SM_V5_S_POR	N/A	All	Always enabled	No	POR	Not available	CLR_FAULT command
Safety Layer V5_S UV or OV	SM_V5S_UV or SM_V5S_OV	N/A	All	Always enabled	Yes	SDO DEV_ERR (SDO pin Hi-Z)	Not available	Power cycle
Safety Layer f_{OSC} Low or High	SM_OSC_MON	N/A	All	Always enabled	Yes	SDO DEV_ERR (SDO pin Hi-Z)	Not available	Power cycle
Safety Layer Digital BIST Failure	SM_LOGIC_BIST	N/A	INIT1	Always enabled	Yes	SDO DEV_ERR (SDO pin Hi-Z)	Not available	Power cycle
Safety Layer Memory BIST Failure	SM_MEM_BIST	N/A	INIT1	Always enabled	Yes	SDO DEV_ERR (SDO pin Hi-Z)	Not available	Power cycle
Analog BIST Failure	SM_ABIST	N/A	INIT2	Always enabled	No	STARTUP_BIST_W	Not available	Power cycle, REINIT_NAD
VDRV Undervoltage	SM_VDRV_UV	VDRV_UV_FLTR	INIT1, INIT2	Always enabled	No	SDO VDD_ERR	Not available	CLR_FAULT command
			STANDBY	Always enabled	No	VDRV_UV	Available in STANDBY	CLR_FAULT command

Table 7-10. General Device Fault Table (continued)

Fault	Safety Mechanism	Configure	Device State	Enable / Disable	nFAULT Assertion	SPI Status	Deploy Function	Recovery
VDRV Overvoltage	SM_VDRV_OV	VDRV_OV_FLTR	STANDBY	Disable, VDRV_OV_W_DIS = 0x1	No	N/A	Available	N/A
				Enable, VDRV_OV_W_DIS = 0x0	No	VDRV_OV	Available	CLR_FAULT command
VREG Switch Monitors	SM_VREG_SW_MONITOR	N/A	STANDBY	Disable, VREG_SW_W_DIS = 0x1	No	N/A	Available	N/A
				Enable, VREG_SW_W_DIS = 0x0	No	VREG_SW_W	Available	CLR_FAULT command
Over Temperature Warning	SM_OTW	N/A	STANDBY	Disable, OT_W_DIS = 0x1	No	N/A	Available	N/A
				Enable, OT_W_DIS = 0x0	No	OT_W	Available	CLR_FAULT command

7.3.9.2 Off-State Diagnostic Faults

This table summarizes the faults and fault responses that can occur during off-state diagnostics.

Table 7-11. Off-State Diagnostics Fault Table

Fault	Safety Mechanism	Configure	Enable / Disable	nFAULT Assertion	SPI Status	Reaction	Recovery
VDRV Undervoltage	SM_VDRV_UV	VDRV_UV_FLTR	Always enabled	Yes, if NFAULT_CONFIG2 = 0x1	VDRV_UV,OFF_DIAG_SUM, OFF_DIAG_STAT	Diagnostics aborted	CLR_FAULT command
VDRV Overvoltage Warning	SM_VDRV_OV	N/A	Disabled, VDRV_OV_W = 0x1	No	None	None	N/A
			Enabled, VDRV_OV_W = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	VDRV_OV, OFF_DIAG_SUM, OFF_DIAG_STAT	Diagnostics aborted	CLR_FAULT command
Over Temperature Warning	SM_OTW	N/A	Disabled, OT_W_DIS = 0x1	No	None	Diagnostics aborted only at TSD level	N/A
			Enabled, OT_W_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM, OT_W	Diagnostics aborted	CLR_FAULT command

Table 7-11. Off-State Diagnostics Fault Table (continued)

Fault	Safety Mechanism	Configure	Enable / Disable	nFAULT Assertion	SPI Status	Reaction	Recovery
Device BIST Failure Warning	SM_DIAG_BIST	N/A	Disabled, OFF_DIAG_ABIST_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_ABIST_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM	Diagnostics aborted	CLR_FAULT command
Weak Pull-Up Failure	SM_WK_PU	OFF_DIAG_WK_PU_TSEL, OFF_DIAG_WK_PU_VSEL, OFF_DIAG_WK_PU_ISEL,	Disabled, OFF_DIAG_WK_PU_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_WK_PU_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM	Diagnostics aborted	CLR_FAULT command
Weak Pull-Down Failure	SM_WK_PD	OFF_DIAG_WK_PD_TSEL, OFF_DIAG_WK_PD_VSEL,OFF_DIAG_WK_PD_ISEL,	Disabled, OFF_DIAG_WK_PD_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_WK_PD_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM	Diagnostics aborted	CLR_FAULT command
High-Side FET RDSON Failure	SM_HS_RDSON	OFF_DIAG_HS_RDSON_TSEL, OFF_DIAG_HS_RDSON_VSEL, OFF_DIAG_HS_RDSON_ISEL,	Disabled, OFF_DIAG_HS_RDSON_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_HS_RDSON_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM, OFF_DIAG_STAT_MISC	Diagnostics aborted	CLR_FAULT command
Low-Side FET RDSON Failure	SM_LS_RDSON	OFF_DIAG_LS_RDSON_TSEL, OFF_DIAG_LS_RDSON_VSEL, OFF_DIAG_LS_RDSON_ISEL,	Disabled, OFF_DIAG_LS_RDSON_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_LS_RDSON_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM, OFF_DIAG_STAT_MISC	Diagnostics aborted	CLR_FAULT command
LS FET Overcurrent	SM_LS_OCP	N/A	Always enabled	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM	Diagnostics aborted	CLR_FAULT command
HS FET Overcurrent	SM_HS_OCP	N/A	Always enabled	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM	Diagnostics aborted	CLR_FAULT command

Table 7-11. Off-State Diagnostics Fault Table (continued)

Fault	Safety Mechanism	Configure	Enable / Disable	nFAULT Assertion	SPI Status	Reaction	Recovery
IREF Resistance Monitor Failure	SM_IREF_MON	N/A	Disabled, OFF_DIAG_IREF_MEAS_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_IREF_MEAS_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM	Diagnostics aborted	CLR_FAULT command
VREG Voltage Measurement Failure	SM_VREG_V_MONITOR	N/A	Disabled, OFF_DIAG_VREG_MEAS_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_VREG_MEAS_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM, OFF_DIAG_STAT_MISC	None	N/A
RMEAS Out-of-Range- Warning	SM_RLOAD_MEAS	OFF_DIAG_RMEAS_THRS_H_SEL OFF_DIAG_RMEAS_THRS_L_SEL OFF_DIAG_RMEAS_TSEL	Disabled, OFF_DIAG_RMEAS_DIS = 0x1	No	None	None	N/A
			Enabled, OFF_DIAG_RMEAS_DIS = 0x0	Yes, if NFAULT_CONFIG2 = 0x1	OFF_DIAG_STAT, OFF_DIAG_SUM	None	N/A

7.3.9.3 Deployment Faults

This table summarizes the faults and fault responses that can occur during deployment (ACTIVE state).

Table 7-12. Deployment Fault Table

Fault	Safety Mechanism	Configure	nFAULT Assertion	SPI Status	Reaction	Recovery
Deploy Current Timeout Violation	SM_PULSE_MEAS	TSTART_TO	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM	Deployment continues	CLR_FAULT command
Over Temperature Warning	SM_OTW	N/A	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM, OT_W	Deployment continues, see DEPLOY_ISEL	CLR_FAULT command
Over Temperature Shutdown	SM_TSD	N/A	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM	Deployment aborted	CLR_FAULT command
LS FET Overcurrent	SM_LS_OCP	N/A	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM	Deployment aborted	CLR_FAULT command
HS FET Overcurrent	SM_HS_OCP	N/A	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM	Deployment aborted	CLR_FAULT command
VDRV Undervoltage	SM_VDRV_UV	VDRV_UV_FLTR	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM, VDRV_UV	Deployment continues, but in RDSON mode	CLR_FAULT command
VDRV Bias Undervoltage	SM_VDRV_UV	N/A	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM	Deployment aborted	CLR_FAULT command

Table 7-12. Deployment Fault Table (continued)

Fault	Safety Mechanism	Configure	nFAULT Assertion	SPI Status	Reaction	Recovery
VDRV Overvoltage	SM_VDRV_OV	VDRV_OV_FLTR	Yes, if NFAULT_CONFIG3 = 0x1	DEPLOY_STAT, DEPLOY_SUM, VDRV_OV	Deployment aborted	CLR_FAULT command

7.4 Device Functional Modes

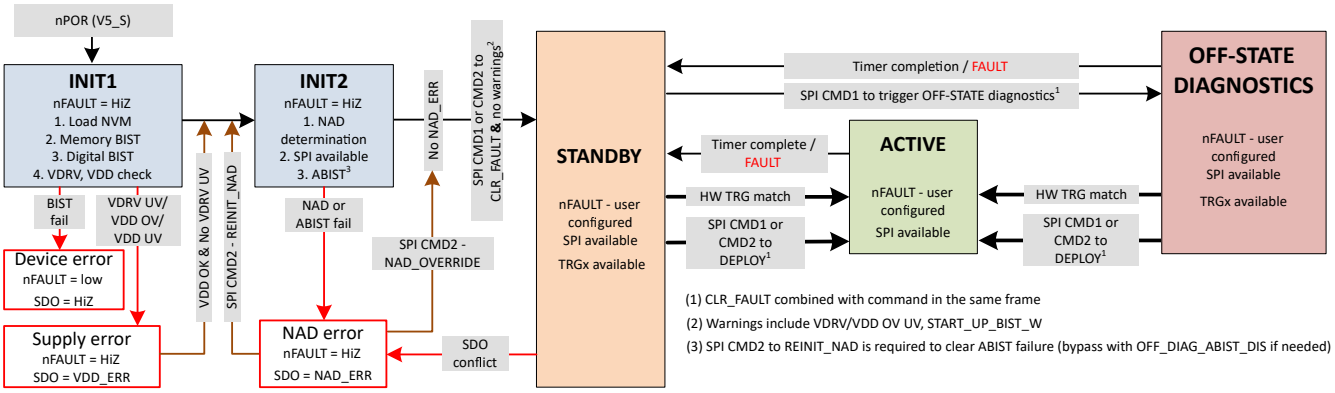


Figure 7-20. DRV3901-Q1 State Diagram

The various states and state transitions are described below.

1. Either VDRV or VDD will initiate power up of the device. A release of the internal power-on-reset (shown as nPOR on V5_S supply) will move the device into the INIT1 state. In the INIT1 state, the factory programmed NVM is loaded and additionally a memory BIST (CRC check) and digital BIST are performed. If there is a BIST failure, the device will enter a locked error state indicated by driving the nFAULT pin low and DEV_ERR fault on the SPI (SDO output Hi-Z). Only a power cycle can re-start this sequence.
2. After entering the **INIT1 STATE**, the device waits until both power supplies, VDD and VDRV are valid. For example, no VDD overvoltage, VDD undervoltage, or VDRV undervoltage before transitioning to the INIT2 state. By default, the SPI SDO VDD_ERR is set. Only in case of no supply error, will VDD_ERR clear.
3. In the **INIT2 STATE**, NAD_ERR is set by default. The device will start the node address (NAD) determination for SPI communcation based on the external pull-up resistor on the nFAULT/NAD pin. Only in the case of a valid NAD determination will the SPI SDO NAD_ERR clear. After a successful NAD determination, the SPI POR bit in STATUS0 is set to indicate a device wake up from reset, SPI communication is available, and nFAULT indicators are configured for default settings. Following this, an analog BIST (ABIST) is performed, whose failure is recorded in the STARTUP_BIST_W bit in STATUS1. The TRGx_PIN_STAT bits will read 0x0 (No data yet) and the TRG1_PIN_LVL bit will reflect the instantaneous pin level.

Note

If a NAD_ERR is detected after the automatic NAD determination, the external microcontroller can either request a re-determination using the REINIT_NAD SPI broadcast command or issue a NAD_OVERRIDE SPI broadcast command with the ASSIGNED_NAD. Only the device(s) with the NAD_ERROR will process this command.

4. To enter the **STANDBY STATE**, the device now expects the external microcontroller to perform a series of steps.
   a. Write the 10 bytes of CONFIG registers along with the calculated CRC.
   b. Issue a CLR_FAULT SPI command.
   c. This puts the device in the STANDBY state with nFAULT de-asserted and TRGx_PIN_STAT will now reflect the pin status. Note that the hardware deploy trigger pins (TRGx) are disabled by default to ensure no accidental deployment.

Note

In this case that an SDO conflict occurs in the STANDBY state, the SPI CMD - REINIT_NAD will automatically take the device through the INIT2 state to STANDBY.

5. Based on the TRG_SEL configuration, the device can be commanded to the **ACTIVE STATE** for deployment. The above diagram is shown for the TRG_SEL option where deployment is possible with either an SPI command "OR" the trigger (TRGx) pin interface. Deployment options are also available for "AND" combination of SPI command and trigger pins. Two types of SPI commands are supported for deployment. CMD1 for a specific node addressed device in the SPI bus or CMD2 for all devices in the SPI bus (broadcast

command). On completion of the deployment (timer completion or abortion due to fault), the device updates the STATUS registers. Further deployment commands are not serviced until a CLR_FAULT command is issued.

6. Additionally, the device can be commanded to perform **OFF-STATE DIAGNOSTICS** with a SPI command. The device can be commanded to deploy any time during off-state diagnostics. A CLR_FAULT command can also be combined with either a deploy or off-state diagnostic command in the same frame.

Note

Refer to the Application and Implementation, Initialization Setup section for recommendations on device interface and control.

7.5 Programming

7.5.1 SPI Interface

The device has a 4-wire, 24 bit SPI follower serial interface protocol. The SPI bus is used to set device configurations, operating parameters, and read out diagnostic information of the device. The device SPI operates in peripheral mode and connects to a central controller. The SPI input data (SDI) consists of 24 bits, with an 8-bit header and 16-bit data. The SPI output data (SDO) word consists of a read-back of the data received (SDI) and specific address data for a read command. Data on SDI is captured on the falling edge of SCLK and data on SDO is propagated on the rising edge of SCLK. For most typical MCUs this is mode 1 (CPOL = 0, CPHA = 1).

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low (to enable data transmission) and from low to high (to end data transmission).
- The nSCS pin should be pulled high inbetween each 24-bit frame transmission.
- Each frame must be exactly 24 SCLKs, else the frame will be discarded as an invalid frame and SPI_ERR will be flagged in the next frame transmission.
- Data on SDI is captured on the falling edge of SCLK and data on SDO is propagated on the rising edge of SCLK.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins will be ignored and the SDO pin will be placed in the Hi-Z state
- The most significant bit (MSB) is shifted in and out first

7.5.2 Addressable SPI

The device supports an optional addressable SPI format to enable up to four devices to operate off the same chip select pin (nSCS). This also allows the usage of special broadcast commands that can enable all devices on the shared addressed bus to take certain actions simultaneously and to minimize pins required to interace with multiple devices.

When using the CMD2 broadcast command, the SDI data is delivered to all devices on the same addressable SPI bus. The SDO response is limited to a single device and the responding device is set with the node address bits (A6, A5) in the SDI frame.

If not using the addressable SPI function, the nFAULT/NAD pin pullup resistor can be set to the default address (00) by using the 5.6k Ohm pullup resistor value. The SPI then functions as a normal SPI by always setting the address bits A6 = 0b, and A5 = 0b.

During power up initialization, the device self assigns a node address (device address) that is based on the pull-up impedance on the nFAULT/NAD pin to VDD (see table below for values). This address is mapped to the two MSBs of the 8 bit header (A6, B5) used in the SPI frame. This enables the user to assign an unique address to each driver (up to four drivers) using the node address feature on the nFAULT/NAD pin. Once initialized, the controller can access any specific register in any of the addressed devices with a single 24-bit frame. After initialization, this pin is then used for nFAULT assertion (open drain, active low) during normal device operation.

Table 7-13.

A6	A5	Resistor to VDD on nFAULT/NAD Pin
0	0	5.6 kOhm
0	1	12 kOhm
1	0	27 kOhm
1	1	56 kOhm

7.5.3 SPI Error Indicators

The SPI protocol provides a function to indicate certain SPI errors directly in the SDO response. Four different types of errors are provided and described below. You can also find an example of the SPI error format in the prior section.

VDD_ERR: The leading bit of the SDO response is used to signal VDD_ERR. The error could occur due to a VDD undervoltage (loss of VDD) or VDD overvoltage on any of the devices on the SPI bus. During power-up initialization (INIT1, INIT2), this field also indicates VDRV under voltage.

NAD_ERR: Failure to identify the node address (resistor out of range or device bias issues during initialization) or data conflict during SDO transmission results in a NAD_ERR condition. The second leading bit of the SDO response is used to signal NAD_ERR and for the remainder of the response SDO is disabled (Hi-Z). The error could occur due to NAD_ERR sensed by any of the devices on the SPI bus. Controller can resolve the NAD_ERR condition using the broadcast commands RE_INIT_NAD, NAD_OVERRIDE, or ASSIGNED NAD. After power up, the NAD address is latched and does not change (unless commanded by the user).

SPI_ERR: The device signals the rejection of an SPI frame by asserting the SPI_ERR bit (third leading bit on SDO response) high in the next SPI frame. This is also referred to as out-of-frame signaling. The remainder of the SDO response proceeds as normal. SPI_ERR could occur due to an incorrect number of SCLK edges when nSCS is low (device expects exactly 24) or a Command CRC mismatch.

DEV_ERR: In the event of an error detected through the various device self-test (BIST) and power-up monitors the device signals a device error in the SDO response by keeping the SDI pin Hi-Z.

7.5.4 SPI Format

There are three different types of 24-bit SPI operations.

- Read: Read back register data from addressed location. The 8-bit header consists of a 2-bit device address, 5-bit register address, and 1-bit to indicate read (0x1 in B16). The 16-bit data is don't cares and can be set as "0"s/
- Write: Modify register contents at addressed location. The 8-bit header consists of a 2-bit device address, 5-bit register address, and 1-bit to indicate write (0x0 in B16). The 16-bit data consists of the data to write into the addressed register.
- Command: Special write commands with CRC8 protection. The 8-bit header consists of a 2-bit device address, 5-bit register address, and 1-bit to indicate write (0x0 in B16). This is followed by an 8-bit command byte and then an 8-bit CRC byte. The CRC is taken of the combined header plus command bytes (B23-B8). The CRC polynomial = 0x97. The device accepts the command only when the CRC (lowest byte) matches the CRC calculated from the leading two bytes of the frame, else the frame is ignored and SPI_ERR bit is set.

The leading bits of SDO are used to indicated specific errors. Additional details can be found in the Section 7.5.3 for additional details.

Table 7-14. SPI Read Format

SPI Read		Header Byte								Data Bye - MSB								Data Byte - LSB							
		B23	B22	B21	B20	B19	B18	B17	B16	B5	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SDI	Read	A6	A5	A4	A3	A2	A1	A0	1	All "0"s															
SDO	Normal	Hi-Z		0	A4	A3	A2	A1	A0	DATA[15:0] from addressed location															
	SPI_ERR	Hi-Z		1	A4	A3	A2	A1	A0	DATA[15:0] from addressed location															
	VDD_ERR	0	Hi-Z																						
	NAD_ERR	Hi-Z	0	Hi-Z																					
	DEV_ERR	Hi-Z																							

Table 7-15. SPI Write Format

SPI Write		Header Byte								Data Bye - MSB								Data Byte - LSB							
		B23	B22	B21	B20	B19	B18	B17	B16	B5	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SDI	Write	A6	A5	A4	A3	A2	A1	A0	0	New DATA[15:0] from addressed location															
SDO	Normal	Hi-Z		0	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	SPI_ERR	Hi-Z		1	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	VDD_ERR	0	Hi-Z																						
	NAD_ERR	Hi-Z	0	Hi-Z																					
	DEV_ERR	Hi-Z																							

Table 7-16. SPI Command Format

SPI Command		Header Byte								Data Bye - MSB								Data Byte - LSB							
		B23	B22	B21	B20	B19	B18	B17	B16	B5	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SDI	Command	A6	A5	A4	A3	A2	A1	A0	0	COMMAND[15:8]								CRC8[7:0] of bits B23-B8. Polynomial = 0x97							
SDO	Normal	Hi-Z		0	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	SPI_ERR	Hi-Z		1	A4	A3	A2	A1	A0	Prior DATA[15:0] from addressed location															
	VDD_ERR	0	Hi-Z																						
	NAD_ERR	Hi-Z	0	Hi-Z																					
	DEV_ERR	Hi-Z																							

7.6 Register Maps

The device has four sets of register types, status (STATUS), measurement (MEAS), configuration (CONFIG), and command (CMD). The register maps for these are shown below with detailed register descriptions following.

Table 7-17. Status (STATUS) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
1h	STATUS0	NAD		POR	TRG1_PIN_STAT				WARNINGS
		DEPLOY_SUM		OFF_DIAG_SUM		RSVD	RSVD	NFAULT_PIN_STAT	DEV_ERR
2h	STATUS1	NAD		TRG1_PIN_LVL	TRG1_PIN_LVL	DEVICE_ID		RSVD	RSVD
		VDRV_OV	OT_W	SPI_WD_W	STARTUP_BIST_W	VDRV_UV	VREG_SW_W		CONFIG_CRC_W
3h	STATUS2	NAD		RSVD					
		OFF_DIAG_STAT				DEPLOY_STAT			
4h	STATUS3	NAD		T_VREG_CAP					
		OFF_DIAG_STAT				OFF_DIAG_STAT_MISC	VREG_VMEAS		

Table 7-18. Measurement (MEAS) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
5h	MEAS0	NAD		RSVD					TSTART_MEAS								
6h	MEAS1	NAD		RSVD	TDEPLOY_MEAS												
7h	MEAS2	NAD		RSVD								RIREF_MEAS					

Table 7-19. Configuration (CONFIG) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
10h	CONFIG0	OFF_DIAG_WK_PU_TSEL		OFF_DIAG_WK_PU_VSEL	OFF_DIAG_WK_PU_ISEL	OFF_DIAG_WK_PD_TSEL		OFF_DIAG_WK_PD_VSEL	OFF_DIAG_WK_PD_ISEL
		OFF_DIAG_HS_RDSON_TSEL		OFF_DIAG_HS_RDSON_VSEL	OFF_DIAG_HS_RDSON_ISEL	OFF_DIAG_LS_RDSON_TSEL		OFF_DIAG_LS_RDSON_VSEL	OFF_DIAG_LS_RDSON_ISEL
11h	CONFIG1	OFF_DIAG_RMEAS_THRS_L_SEL	OFF_DIAG_RMEAS_THRS_H_SEL		OFF_DIAG_RMEAS_TSEL		OFF_DIAG_CMEAS_THRS_SEL		
		OFF_DIAG_ABIST_DIS	OFF_DIAG_WK_PU_DIS	OFF_DIAG_WK_PD_DIS	OFF_DIAG_HS_RDSON_DIS	OFF_DIAG_LS_RDSON_DIS	OFF_DIAG_IREF_MEAS_DIS	OFF_DIAG_RMEAS_DIS	OFF_DIAG_VREG_MEAS_DIS
12h	CONFIG2	VDD_OV_FLTR		VDD_UV_FLTR		VDRV_OV_FLTR		VDRV_UV_FLTR	
		OFF_DIAG_CMEAS_AUTO	RSVD	RSVD	VDRV_OV_W_DIS	OT_W_DIS	SPI_WD_W_DIS	VREG_SW_W_DIS	VREG_SW_DIS
13h	CONFIG3	NFAULT_CONFIG3	NFAULT_CONFIG2	NFAULT_CONFIG1	NFAULT_CONFIG0	TRG_SEL			
		PIN_DEPLOY_DLY_EN	DEPLOY_DLY			SPI_WD_SEL		OFF_DIAG_CMEAS_TSEL	

Table 7-19. Configuration (CONFIG) Register Map (continued)

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
14h	CONFIG4	TSTART_TO		PWM_FLTR_SEL		DEPLOY_ISEL			DEPLOY_IRATE
		CONFIG_CRC							

Table 7-20. Command (CMD) Register Map

ADDR	NAME	B15	B14	B13	B12	B11	B10	B9	B8
		B7	B6	B5	B4	B3	B2	B1	B0
1Ch	CMD0	Force "0"			TRG1_DIS	TRG2_DIS	RSVD	FORCE_BIST	
		CRC8							
1Dh	CMD1	CLR_FAULT	LOCK_CONFIG	RSVD	ACTIVATE	ACTIVITY_CTRL		RSVD	
		CRC8							
1Eh	CMD2	BCST_CLR_FAULT	RE_INIT_NAD	NAD_OVERRIDE	ASSIGNED_NAD		DEPLOY	DEPLOY_DLY_EN	RSVD
		CRC8							

7.6.1 STATUS Registers

Table 7-21 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in Table 7-21 should be considered as reserved locations and the register contents should not be modified.

Table 7-21. STATUS Registers

Offset	Acronym	Register Name	Section
1h	STATUS0	Summary of device, output, and trigger pin (TRG) status.	Section 7.6.1.1
2h	STATUS1	Trigger pin (TRG), SPI, BIST, and power supply status.	Section 7.6.1.2
3h	STATUS2	Off-state and deploy status.	Section 7.6.1.3
4h	STATUS3	Off-state and reservoir cap status.	Section 7.6.1.4

Complex bit access types are encoded to fit into small table cells. Table 7-22 shows the codes that are used for access types in this section.

Table 7-22. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 STATUS0 Register (Offset = 1h) [Reset = 2102h]

STATUS0 is shown in Table 7-23.

Return to the Summary Table.

Global status register including fault and warning summary indicators for device and output status. Also includes trigger pin (TRG) status.

Table 7-23. STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	NAD	R	0h	Device node address for SPI communication. Determined based on pullup resistor value on nFAULT/NAD pin. Mirrored in all registers as bits 15-14. 0h = 5.6 kOhm 1h = 12 kOhm 2h = 27 kOhm 3h = 56 kOhm
13	POR	R	1h	Power-on reset indicator. Bit is latched until CLR_FAULT command is issued.
12-11	TRG1_PIN_STAT	R	0h	Trigger pin 1 (TRG1) status indicator. Status is latched, until CLR_FAULT command is issued, if TRG1 causes deployment. Deployment action can be disabled with TRGx_DIS, but TRG1 pin status will continue to be shown to allow option of pin inteface diagnostic. Feedback based on TRG_SEL mode. For additional details refer to the Pin Monitors section.
10-9	TRG2_PIN_STAT	R	0h	Trigger pin 2 (TRG2) status indicator. Status is latched, until CLR_FAULT command is issued, if TRG1 causes deployment. Deployment action can be disabled with TRGx_DIS, but TRG1 pin status will continue to be shown to allow option of pin inteface diagnostic. Feedback based on TRG_SEL mode. For additional details refer to the Pin Monitors section.
8	WARNINGS	R	1h	Warning indicator (summary). This indicator is set if any of the warnings in STATUS1 register are high. Read STATUS1 register for detailed warning information. Warnings are latched until CLR_FAULT command is issued, but outputs remain operational.
7-6	DEPLOY_SUM	R	0h	Deployment summary indicator. Read DEPLOY_STAT in STATUS2 register for detailed information. Latched after deployment until CLR_FAULT command. 0h = No data available yet 1h = Deployment in progress 2h = Deployment successful 3h = Deplyoment completed with warning or aborted with error.
5-4	OFF_DIAG_SUM	R	0h	Off-state diagnostics summary indicator. Read OFF_DIAT_STAT in STATUS2 and OFF_DIAT_STAT_MISC in STATUS3 register for detailed information. Latched after diagnostic until CLR_FAULT command. 0h = No data available yet 1h = Off-state diagnostic in progress 2h = Off-state diagnostic successful 3h = Off-state diagnostic completed with warning or aborted with error.
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	FLT_PIN_STAT	R	1h	nFAULT/NAD pin status indicator. 0h = Pin low (fault asserted) 1h = Pin high (normal operation)

Table 7-23. STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DEV_ERR	R	0h	DEV_ERR fault is communicated by holding SDO pin in Hi-Z state. Refer to SPI section details. If DEV_ERR fault is present, device operation is disabled with outputs in Hi-Z state and a power cycle (internal logic reset) is required to clear this fault. This bit should always read low during normal device operation. 0h = Device normal operation 1h = Device fault, SDO pin asserted Hi-Z

7.6.1.2 STATUS1 Register (Offset = 2h) [Reset = 0801h]

STATUS1 is shown in Table 7-24.

Return to the Summary Table.

Status register including trigger pin 1 (TRG1) level status, SPI CRC error, device ID, VDRV OV and UV monitors, and VREG switch monitor.

Table 7-24. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	NAD	R	0h	Mirror of NAD address in STATUS0 register.
13	TRG1_PIN_LVL1	R	0h	Trigger 1 pin (TRG1) level status. 0h = Pin low 1h = Pin high
12	TRG1_PIN_LVL2	R	0h	Trigger 1 pin (TRG1) level status. Mirror of TRG1_PIN_LVL1 0h = Pin low 1h = Pin high
11-10	DEVICE_ID	R	2h	Device ID. Production silicon revision fixed to 2h.
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	VDRV_OV	R	0h	VDRV overvoltage fault indication when VDRV_OV_W_DIS = 1b. VDRV overvoltage warning when VDRV_OV_W_DIS = 0b. Latched until CLR_FLT command is issued.
6	OT_W	R	0h	Over temperature warning. Latched until CLR_FAULT command is issued.
5	SPI_WD_W	R	0h	SPI watchdog warning. Latched until CLR_FAULT command is issued.
4	STARTUP_BIST_W	R	0h	Device start up ABIST failure indictor. If an ABIST fault occurs, user needs to issue REINIT_NAD in CMD2 register to restart ABIST test. The ABIST test can be bypassed with OFF_DIAG_ABIST_DIS in CONFIG1 register. The device will not exit INIT2 device state until this fault is cleared.
3	VDRV_UV	R	0h	VDRV undervoltage. Latched until CLR_FAULT command is issued.
2-1	VREG_SW_W	R	0h	VREG switch warning (Valid only VDRV > $V_{DRV\_UV\_BIAS}$). Latched until CLR_FAULT command issued. 0h = No data available yet. 1h = VREG switch disabled due to VREG < PVDD - VREG_THRS1 2h = VREG switch disabled due to VREG > PVDD + VREG_THRS2 3h = No warning
0	CONFIG_CRC_W	R	1h	CRC mismatch warning for CONFIG register space. Cleared with update of CONFIG_CRC register with correct check sum.

7.6.1.3 STATUS2 Register (Offset = 3h) [Reset = 0000h]

STATUS2 is shown in Table 7-25.

Return to the Summary Table.

Status register including off-state diagnostic and output deployment status.

Table 7-25. STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	NAD	R	0h	Mirror of NAD address in STATUS0 register.
13-8	RESERVED	R	0h	Reserved
7-4	OFF_DIAG_STAT	R	0h	Off-state diagnostic status. Latched until next off-state diagnostic test sequence is commanded. 0h = Diagnostics complete, no error or warning. 1h = Diagnostics complete, Load resistance ok, VREG voltage low (< PVDD - 160mV). 2h = Diagnostics complete, Load resistance low, VREG voltage ok. 3h = Diagnostics complete, Load resistance low, VREG voltage low (< PVDD - 160mV). 4h = Diagnostics complete, Load resistance high, VREG voltage ok. 5h = Diagnostics complete, Load resistance high, VREG voltage low (< PVDD - 160mV). 6h = Diagnostic aborted due to VDRV_OV, VDRV_UV or OT_W. Corresponding detailed status bit will be set. 7h = Diagnostic aborted due to deployment (DEPLOY) command. 8h = Diagnostic aborted due to device ABIST failure. 9h = Diagnostic aborted due to weak pull up failure. Ah = Diagnostic aborted due to weak pull down failure. Bh = Diagnostic aborted due to HS RDSON failure or VDRV_OV_W. Detailed information in the OFF_DIAG_STAT_MISC or VDRV_OV status bits. Ch = Diagnostic aborted due to LS RDSON failure or VDRV_OV_W. Detailed information in the OFF_DIAG_STAT_MISC or VDRV_OV status bits. Dh = Diagnostic aborted due to IREF resistance out of range or incorrect comparator output combination during load resistance monitor / VREG voltage measurement. Detailed information in the OFF_DIAG_STAT_MISC status bits. Eh = Diagnostic aborted due to low side over current violation. Violation can occur during RDSON test or IREF / load resistance measurement. Fh = Diagnostic aborted due to high side over current violation. Violation can occur during RDSON test or IREF / load resistance measurement.
3-0	DEPLOY_STAT	R	0h	Deployment status. Latched until the next deployment, SPI or pin triggered (TRGx) is commanded. 0h = Deployment complete, no error or warning. 1h = Deployment complete, but TSTART_TO enforced. 2h = Deployment complete, but OT_W detected. 3h = Deployment complete, but OT_W detected and TSTART_TO enforced. 4h = Deployment complete, but VDRV_UV detected. 5h = Deployment complete, but VDRV_UV and TSTART_MEAS time out detected. 6h = Deployment complete, but VDRV_UV and OT_W detected. 7h = Deployment complete, but VDRV_UV, OT_W and TSTART_MEAS time out detected. 8h = Deployment aborted due to thermal shutdown. 9h = Deployment aborted due to low side over current violation. Ah = Deployment aborted due to high side over current violation. Bh = Deployment aborted due to VDRV overvoltage violation. Ch = Deployment aborted due to VDRV bias undervoltage violation. Dh = Reserved. Eh = Reserved. Fh = Reserved.

7.6.1.4 STATUS3 Register (Offset = 4h) [Reset = 0000h]

STATUS3 is shown in Table 7-26.

Return to the Summary Table.

Status register including off-state diagnostic and VREG reservoir capacitor diagnostics status.

Table 7-26. STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	NAD	R	0h	Mirror of NAD address in STATUS0 register.
13-8	T_VREG_CAP	R	0h	VREG reservoir cap value. 00h = Timer start did not occur, value not determined. 01h - 31h = Timer start and stop occurred. Cap value (Farad) = T_VREG_CAP (register value decimal) x timer resolution x 1.16 31h - 3Fh = Timer start occurred but stop did not occur. Cap value (Farad) > T_VREG_CAP (register value decimal) x timer resolution x 1.16 Timer resolution = OFF_DIAG_CMEAS_TSEL (0.5ms, 1ms, 2ms, 4ms) / 32. Ex. If T_VREG_CAP = 0x08 and OFF_DIAG_CMEAS_TSEL = 1 ms, VREG cap value = 8 x (1m/32) x 1.16 = 290 uF.
7-4	OFF_DIAG_STAT	R	0h	Mirror of OFF_DIAG_STAT in STATUS2 register.
3	OFF_DIAG_STAT_MISC	R	0h	Additional information for aborted diagnostics due to failures. 0h = Diagnostic aborted due to RDSON precharge failure (if OFF_DIAG_STAT is Bh or Ch), else Diagnostic aborted due to IREF resistance monitor failure (if IOFF_DIAG_STAT is Dh). 1h = Diagnostic aborted due to RDSON FET test failure (if OFF_DIAG_STAT is Bh or Ch), else Diagnostic aborted due to RLOAD monitor or VREG voltage measurement failure (if IOFF_DIAG_STAT is Dh).
2-0	VREG_VMEAS	R	0h	VREG voltage measurement during off-state diagnostics. Measurement valid only if OFF_DIAG_STAT = 0x0 / 0x2 / 0x4 after diagnostics. 0h = No data available yet or VREG ≥ PVDD-20mV 1h = PVDD-20mV > VREG ≥ PVDD-40mV 2h = PVDD-40mV > VREG ≥ PVDD-60mV 3h = PVDD-60mV > VREG ≥ PVDD-80mV 4h = PVDD-80mV > VREG ≥ PVDD-100mV 5h = PVDD-100mV > VREG ≥ PVDD-120mV 6h = PVDD-120mV > VREG ≥ PVDD-140mV 7h = PVDD-140mV > VREG ≥ PVDD-160mV

7.6.2 MEAS Registers

Table 7-27 lists the memory-mapped registers for the MEAS registers. All register offset addresses not listed in Table 7-27 should be considered as reserved locations and the register contents should not be modified.

Table 7-27. MEAS Registers

Offset	Acronym	Register Name	Section
5h	MEAS0	Deployment delay measurement.	Section 7.6.2.1
6h	MEAS1	Deployment duration measurement.	Section 7.6.2.2
7h	MEAS2	Reference resistance measurement.	Section 7.6.2.3

Complex bit access types are encoded to fit into small table cells. Table 7-28 shows the codes that are used for access types in this section.

Table 7-28. MEAS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.1 MEAS0 Register (Offset = 5h) [Reset = 0000h]

MEAS0 is shown in Table 7-29.

Return to the Summary Table.

Measurement register that provides time to reach deploy current levels after activation.

Table 7-29. MEAS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	NAD	R	0h	Mirror of NAD address in STATUS0 register.
13-9	RESERVED	R	0h	Reserved
8-0	TSTART_MEAS	R	0h	Measured time to reach deployment current level once commanded to deploy. Timer resolution is 500 ns. Measured time (ns) = (TSTART_MEAS register value in decimal + 30) x 500 ns.

7.6.2.2 MEAS1 Register (Offset = 6h) [Reset = 0000h]

MEAS1 is shown in Table 7-30.

Return to the Summary Table.

Measurement register that provides deployment current duration.

Table 7-30. MEAS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	NAD	R	0h	Mirror of NAD address in STATUS0 register.
13	RESERVED	R	0h	Reserved
12-0	DEPLOY_MEAS	R	0h	Measured time that deploy current is sensed during deployment. Timer resolution is 500 ns. Measured time (ns) = (DEPLOY_MEAS register value in decimal) X 500 ns.

7.6.2.3 MEAS2 Register (Offset = 7h) [Reset = 0000h]

MEAS2 is shown in Table 7-31.

Return to the Summary Table.

Measurement register that provides reference resistance measurement.

Table 7-31. MEAS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	NAD	R	0h	Mirror of NAD address in STATUS0 register.
13-5	RESERVED	R	0h	Reserved
4-0	RIREF_MEAS	R	0h	IREF resistance measurement when measurement is in range (8-24 in decimal), else reported as 0h.

7.6.3 CONFIG Registers

Table 7-32 lists the memory-mapped registers for the CONFIG registers. All register offset addresses not listed in Table 7-32 should be considered as reserved locations and the register contents should not be modified.

Table 7-32. CONFIG Registers

Offset	Acronym	Register Name	Section
10h	CONFIG0	Off-state diagnostic configuration 1.	Section 7.6.3.1
11h	CONFIG1	Off-state diagnostic configuration 2.	Section 7.6.3.2
12h	CONFIG2	Overvoltage, undervoltage, watchdog, reservoir cap configuration.	Section 7.6.3.3
13h	CONFIG3	Fault, deploy delay and mode, trigger pin mode, watchdog, and reservoir cap configuration.	Section 7.6.3.4
14h	CONFIG4	Tstart, input PWM, deploy pulse and rate, and CRC configuration.	Section 7.6.3.5

Complex bit access types are encoded to fit into small table cells. Table 7-33 shows the codes that are used for access types in this section.

Table 7-33. CONFIG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.3.1 CONFIG0 Register (Offset = 10h) [Reset = 0011h]

CONFIG0 is shown in Table 7-34.

Return to the Summary Table.

Configuration register to setup the output weak pull up and pull down, and rdson off-state diagnostics.

Table 7-34. CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	OFF_DIAG_WK_PU_TSEL	R/W	0h	Test time selection (t_{WK_PU}) for output settling during off-state diagnostics, weak pull up test. 0h = 0.25 ms 1h = 0.5 ms 2h = 1 ms 3h = 2 ms
13	OFF_DIAG_WK_PU_VSEL	R/W	0h	Voltage reference selection ($V_{REF\_WK\_PU}$) for off-state diagnostics, weak pull up test. 0h = 2.1 V 1h = 2.4 V
12	OFF_DIAG_WK_PU_ISEL	R/W	0h	Current selection ($I_{REF\_WK\_PU}$) for off-state diagnostics, weak pull up test 0h = 1 mA 1h = 2 mA
11-10	OFF_DIAG_WK_PD_TSEL	R/W	0h	Test time selection (t_{WK_PD}) for output settling during off-state diagnostics, weak pull down test. 0h = 0.25 ms 1h = 0.5 ms 2h = 1 ms 3h = 2 ms
9	OFF_DIAG_WK_PD_VSEL	R/W	0h	Voltage reference selection ($V_{REF\_WK\_PD}$) for off-state diagnostics, weak pull down test. 0h = 1.5 V 1h = 1.8 V
8	OFF_DIAG_WK_PD_ISEL	R/W	0h	Current selection ($I_{REF\_WK\_PD}$) for off-state diagnostics, weak pull down test. 0h = 1 mA 1h = 2 mA
7-6	OFF_DIAG_HS_RDSON_TSEL	R/W	0h	Test time selection ($t_{HSRDSON}$) for output settling during off-state diagnostics, HS RDSON test. 0h = 0.25 ms 1h = 0.5 ms 2h = 1 ms 3h = 2 ms
5	OFF_DIAG_HS_RDSON_VSEL	R/W	0h	Voltage reference selection ($V_{REF\_HSRDSON}$) for off-state diagnostics, HS RDSON test. 0h = -75 mV 1h = -150 mV
4	OFF_DIAG_HS_RDSON_ISEL	R/W	1h	Current selection ($I_{REF\_HSRDSON}$) for off-state diagnostics, HS RDSON test. 0h = 20 mA 1h = 40 mA
3-2	OFF_DIAG_LS_RDSON_TSEL	R/W	0h	Test time selection ($t_{LSRDSON}$) for output settling during off-state diagnostics, LS RDSON test. 0h = 0.25 ms 1h = 0.5 ms 2h = 1 ms 3h = 2 ms
1	OFF_DIAG_LS_RDSON_VSEL	R/W	0h	Voltage reference selection ($V_{REF\_LSRDSON}$) for off-state diagnostics, LS RDSON test. 0h = 75 mV 1h = 150 mV

Table 7-34. CONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OFF_DIAG_LS_RDSON_ISEL	R/W	1h	Current selection ($I_{REF\_LSRDSON}$) for off-state diagnostics, LS RDSON test. 0h = 20 mA 1h = 40 mA

7.6.3.2 CONFIG1 Register (Offset = 11h) [Reset = 0018h]

CONFIG1 is shown in Table 7-35.

Return to the Summary Table.

Configuration register to setup the output load resistance measurement, reservoir capacitor measurement, and enable/disable each output diagnostic.

Table 7-35. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OFF_DIAG_RMEAS_THRS_L_SEL	R/W	0h	Low RLOAD (R_{MEASL}) threshold selection. 0h = 1.5 Ohm 1h = 1.25 Ohm
14-13	OFF_DIAG_RMEAS_THRS_H_SEL	R/W	0h	High RLOAD (R_{MEASH}) threshold selection. 0h = 2.8 Ohm 1h = 3.3 Ohm 2h = 3.8 Ohm 3h = 60 Ohm
12-11	OFF_DIAG_RMEAS_TSEL	R/W	0h	Test time selection (t_{RMEAS}) for output settling during off-state diagnostics, RMEAS test. 0h = 0.25 ms 1h = 0.5 ms 2h = 1 ms 3h = 2 ms
10-8	OFF_DIAG_CMEAS_THRS_SEL	R/W	0h	Voltage threshold (V_{DAC_VREG}) for CMPH during discharge cycle for VREG CAP measurement, off-state diagnostics (used only when OFF_DIAG_CMEAS_THRS_AUTO = 0x0). Voltage threshold for CMPL is fixed at 20 mV below this threshold. 0h = -25 mV 1h = -40 mV 2h = -60 mV 3h = -80 mV 4h = -100 mV 5h = -120 mV 6h = -140 mV 7h = -160 mV
7	OFF_DIAG_ABIST_DIS	R/W	0h	Disable ABIST during off-state diagnostics and INIT2 state. 0h = Enabled 1h = Disabled
6	OFF_DIAG_WK_PU_DIS	R/W	0h	Disable weak pull up test during off-state diagnostics. 0h = Enabled 1h = Disabled
5	OFF_DIAG_WK_PD_DIS	R/W	0h	Disable weak pull-down test during off-state diagnostics. 0h = Enabled 1h = Disabled
4	OFF_DIAG_HS_RDSON_DIS	R/W	1h	Disable HS RDSON test during off-state diagnostics. 0h = Enabled 1h = Disabled
3	OFF_DIAG_LS_RDSON_DIS	R/W	1h	Disable LS RDSON test during off-state diagnostics. 0h = Enabled 1h = Disabled
2	OFF_DIAG_IREF_MEAS_DIS	R/W	0h	Disable IREF pin resistance measurement during off-state diagnostics. 0h = Enabled 1h = Disabled
1	OFF_DIAG_RMEAS_DIS	R/W	0h	Disable RMEAS test during off-state diagnostics. 0h = Enabled 1h = Disabled

Table 7-35. CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OFF_DIAG_VREG_MEAS_DIS	R/W	0h	Disable VREG voltage and capacitor measurement test during off-state diagnostics. 0h = Enabled 1h = Disabled

7.6.3.3 CONFIG2 Register (Offset = 12h) [Reset = 0000h]

CONFIG2 is shown in Table 7-36.

Return to the Summary Table.

Configuration register to setup the VDD, VDRV under and overvoltage monitors. Also provides option for reservoir capacitor diagnostic, overtemperature, and watchdog modes.

Table 7-36. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	VDD_OV_FLTR	R/W	0h	VDD overvoltage deglitch filter (t_{VDD_OV}). 0h = 250 us 1h = 500 us 2h = 750 us 3h = 1000 us
13-12	VDD_UV_FLTR	R/W	0h	VDD undervoltage deglitch filter (t_{VDD_UV}). 0h = 250 us 1h = 500 us 2h = 750 us 3h = 1000 us
11-10	VDRV_OV_FLTR	R/W	0h	VDRV overvoltage deglitch filter (t_{VDRV_OV}). 0h = 250 us 1h = 500 us 2h = 750 us 3h = 1000 us
9-8	VDRV_UV_FLTR	R/W	0h	VDRV undervoltage deglitch filter (t_{VDRV_UV}). 0h = 250 us 1h = 500 us 2h = 750 us 3h = 1000 us
7	OFF_DIAG_CMEAS_AUTO	R/W	0h	Off-state diagnostic VREG capacitor measurement auto thresholding. 0h = Disabled, user defined value in OFF_DIAG_CMEAS_THRS_SEL 1h = Enabled, automatically set as one code above VREG_MEAS value. If VREG_MEAS is 7h, then set at 7h.
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	VDRV_OV_W_DIS	R/W	0h	Disable reporting of VDRV overvoltage warning. 0h = Enabled 1h = Disabled
3	OT_W_DIS	R/W	0h	Disable reporting of over temperature warning. Off-state diagnostics are also not aborted when over temperature warning levels are reached. 0h = Enabled 1h = Disabled
2	SPI_WD_W_DIS	R/W	0h	Disable reporting of SPI watchdog warning. 0h = Enabled 1h = Disabled
1	VREG_SW_W_DIS	R/W	0h	Disable reporting of VREG switching warnings. 0h = Enabled 1h = Disabled
0	VREG_SW_DIS	R/W	0h	Disable VREG switch. User should also disable VREG switch warnings by setting VREG_SW_W_DIS = 1b if VREG_SW_DIS = 1b. 0h = Enabled 1h = Disabled. User should also set VREG_SW_W_DIS is 1b

7.6.3.4 CONFIG3 Register (Offset = 13h) [Reset = 8000h]

CONFIG3 is shown in Table 7-37.

Return to the Summary Table.

Configuration register to setup the fault mode, deployment current delay, and trigger pin (TRG) mode. Also provides options for reservoir capacitor diagnostic and watchdog modes.

Table 7-37. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NFAULT_CONFIG3	R/W	1h	Enable nFAULT pin reporting (drive low) if DEPLOY_SUM = 3h. nFAULT pin is cleared by CLR_FAULT command. A DEV_ERR fault will always report on nFAULT pin.
14	NFAULT_CONFIG2	R/W	0h	Enable nFAULT pin reporting (drive low) if OFF_DIAG_SUM = 3h, except when off-state diagnostics are aborted due to a deployment command. nFAULT pin is cleared by CLR_FAULT command. A DEV_ERR fault will always report on nFAULT pin.
13	NFAULT_CONFIG1	R/W	0h	Enable nFAULT pin reporting (drive low) if SPI_WD_W = 1h. nFAULT pin is cleared by CLR_FAULT command. A DEV_ERR fault will always report on nFAULT pin.
12	NFAULT_CONFIG0	R/W	0h	Enable nFAULT pin reporting (drive low) during deployment (ACTIVE state). nFAULT pin is cleared by CLR_FAULT command. A DEV_ERR fault will always report on nFAULT pin.
11-8	TRG_SEL	R/W	0h	Trigger pin configuration. Refer to the Trigger (TRGx) Pins section for details on configuration options.
7	PIN_DEPLOY_DLY_EN	R/W	0h	Enables delayed deployment triggered through TRGx pins. 0h = Disabled 1h = Enabled
6-4	DEPLOY_DLY	R/W	0h	Deployment delay (t_{DEPLOY_DLY}) selection (valid for both PIN and SPI deployment triggers when enabled). 0h = 0.1 ms 1h = 0.2 ms 2h = 0.4 ms 3h = 0.8 ms 4h = 1.5 ms 5h = 2.5 ms 6h = 3.25 ms 7h = 4 ms
3-2	SPI_WD_SEL	R/W	0h	Watchdog duration (t_{WD}) to detect valid SPI read or write frame. 0h = 65 ms 1h = 250 ms 2h = 1000 ms 3h = 2000 ms
1-0	OFF_DIAG_CMEAS_TSEL	R/W	0h	Test time selection (t_{CMEAS}) for VREG capacitor measurement test during off-state diagnostics. 0h = 0.5 ms 1h = 1 ms 2h = 2 ms 3h = 4 ms

7.6.3.5 CONFIG4 Register (Offset = 14h) [Reset = 0600h]

CONFIG4 is shown in Table 7-38.

Return to the Summary Table.

Configuration register to setup the tstart delay timeout, trigger pin (TRG) filtering, deployment current pulse and edge rate, and configuration CRC.

Table 7-38. CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TSTART_TO	R/W	0h	Time out duration (t_{START_TO}) for TSTART_MEAS. 0h = 75 us 1h = 150 us 2h = 200 us 3h = 275 us
13-12	PWM_FLTR_SEL	R/W	0h	TRGx pin PWM filtering selection (t_{PWM_TRG}). Valid only when PWM triggering (16kHz) is selected. For TRGx pin level (LVL) signaling, device uses deglitch time of 16 us. 0h = -18 to 32 % 1h = -15 to 24 % 2h = -12 to 16 % 3h = -9 to 12 %
11-9	DEPLOY_ISEL	R/W	3h	Deployment current pulse selection. For 2h, in the event of OT_W, the device will automatically drop to lower setting of DEPLOY_ISEL = 0h. For 6h and 7h, in the event of OT_W, the device will automatically drop to the lower setting of DEPLOY_ISEL = 3h. 0h = 1.2 A (Min) 1h = 1.65 A (Min) 2h = 1.65 A* (Min) 3h = 1.75 A (Min) 4h = 2.19 A (Min) 5h = 3.4 A (Min) 6h = 2.19 A* (Min) 7h = 3.4 A* (Min)
8	DEPLOY_IRATE	R/W	0h	Deployment current di/dt selection. 0h = Fast (1 us/A) 1h = Slow (4 us/A)
7-0	CONFIG_CRC	R/W	0h	Programmed CRC for CONFIG register space. Writing to this register triggers CRC check for CONFIG register space. Polynomial = 97h. The CRC is applied to the 16 bit data of all CONFIG registers, not including the CONFIG_CRC itself (9 bytes total). Starting from CONFIG0, up to CONFIG4, MSB to LSB.

7.6.4 CMD Registers

Table 7-39 lists the memory-mapped registers for the CMD registers. All register offset addresses not listed in Table 7-39 should be considered as reserved locations and the register contents should not be modified.

Table 7-39. CMD Registers

Offset	Acronym	Register Name	Section
1Ch	CMD0	General command.	Section 7.6.4.1
1Dh	CMD1	Action command.	Section 7.6.4.2
1Eh	CMD2	Broadcast command.	Section 7.6.4.3

Complex bit access types are encoded to fit into small table cells. Table 7-40 shows the codes that are used for access types in this section.

Table 7-40. CMD Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.4.1 CMD0 Register (Offset = 1Ch) [Reset = 1800h]

CMD0 is shown in Table 7-41.

Return to the Summary Table.

General command for disabling trigger pin deployment and enabling system BIST functions.

Table 7-41. CMD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	TRG1_DIS	R/W	1h	Disable TRG1 deployment. Feedback through TRG1_PIN_STAT is still valid. 0h = Enabled 1h = Disabled
11	TRG2_DIS	R/W	1h	Disable TRG2 deployment. Feedback through TRG2_PIN_STAT is still valid. 0h = Enabled 1h = Disabled
10	RESERVED	R	0h	Reserved
9-8	FORCE_BIST	R/W	0h	Enable system BIST feature. Command is only accepted during STANDBY state of operation. 0h = No action 1h = Assert nFAULT pin low until CLR_FAULT command is issued. 2h = Force secondary logic time out until CLR_FAULT command is issued. 3h = Assert 75% duty cycle PWM @ 16K Hz on nFAULT
7-0	CRC	R/W	0h	Embedded CRC field. Write command only accepted when valid CRC is provided to this value. Polynomial = 97h. CRC is applied to the 8 bits of command data.

7.6.4.2 CMD1 Register (Offset = 1Dh) [Reset = 0000h]

CMD1 is shown in Table 7-42.

Return to the Summary Table.

Action command for clearing faults, locking registers, and taking driver action.

Table 7-42. CMD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR_FAULT	R/W	0h	Clear fault command. Auto cleared after the command has been registered. 0h = Default 1h = Clear fault
14	LOCK_CONFIG	R/W	0h	Lock the CONFIG register space for device configuration. Unlock to make additional CONFIG register changes. 0h = Unlock 1h = Lock
13	RESERVED	R	0h	Reserved
12	ACTIVATE	R/W	0h	Configurable action command based on ACTIVITY_CTRL. 0h = No action 1h = Take action based on ACTIVITY_CTRL
11-10	ACTIVITY_CTRL	R/W	0h	Action command selection for ACTIVATE command. 0h = No action 1h = Perform off-state diagnostics if ACTIVATE is 1b 2h = Perform deployment if ACTIVATE is 1b 3h = Perform deployment with delay (DEPLOY_DLY) if ACTIVATE is 1b
9-8	RESERVED	R	0h	Reserved
7-0	CRC	R/W	0h	Embedded CRC field. Write command only accepted when valid CRC is provided to this value. Polynomial = 97h. CRC is applied to the 8 bits of command data.

7.6.4.3 CMD2 Register (Offset = 1Eh) [Reset = 0000h]

CMD2 is shown in Table 7-43.

Return to the Summary Table.

Broadcast command for clearing faults, managing SPI addressing, and driver deployment.

Table 7-43. CMD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BCST_CLR_FAULT	R/W	0h	Broadcast clear fault command to all connected devices. Auto cleared after the command has been registered.
14	RE_INIT_NAD	R/W	0h	Broadcast command to re-initialize NAD on all connected devices. Write command is only accepted in the device INIT2 state.
13	NAD_OVERRIDE	R/W	0h	When set, any device having a NAD error, clears NAD_ERR and picks up the address in the next two bits as their assigned NAD for SPI communication. Write is accepted ONLY during INIT2 state when NAD_ERR is detected and RE_INIT_NAD = 0b.
12-11	ASSIGNED_NAD	R/W	0h	Assigned NAD for device with NAD error when NAD_OVERRIDE = 1b.
10	DEPLOY	R/W	0h	Broadcast deployment command.
9	DEPLOY_DLY_EN	R/W	0h	Enable broadcast deployment with delay (DEPLOY_DLY) if DEPLOY = 1b. 0h = Disabled 1h = Enabled
8	RSVD	R/W	0h	Reserved. Write 0x0 to this field.
7-0	CRC	R/W	0h	Embedded CRC field. Write command only accepted when valid CRC is provided to this value. Polynomial = 97h. CRC is applied to the 8 bits of command data.

8 Application and Implementation

8.1 Application Information

The DRV3901-Q1 is a high integrated driver for resistive squib loads. The sections below will give some design guidelines on using the device.

8.2 Typical Application

While the DRV3901-Q1 can be used as a general purpose squib load driver, the device was specifically developed to support driving squibs used for automotive EV pyro-fuse applications. The device is intended to interact with an external controller directly or through a device serving as a communications bridge to the DRV3901-Q1.

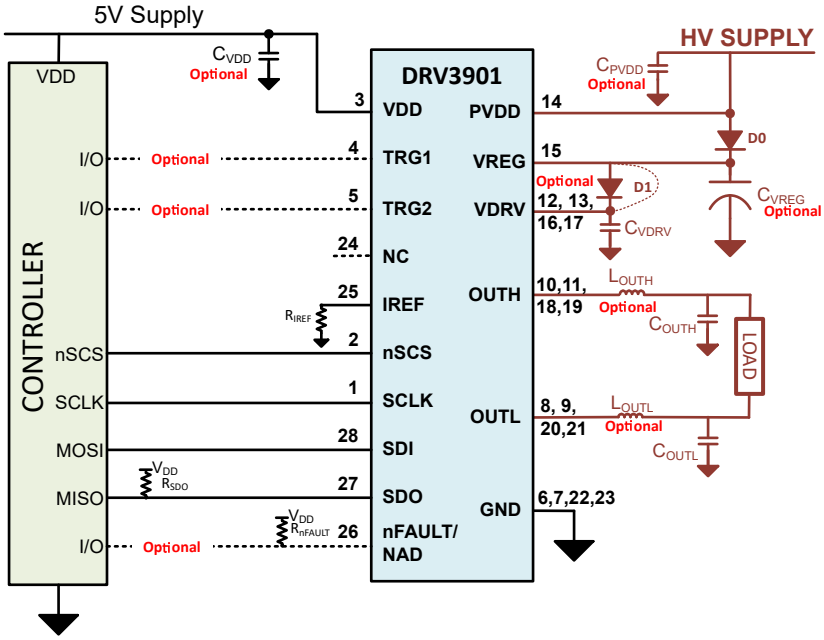


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
PVDD / VDRV Power Supply	12 V (typical), but can utilize higher boosted supply voltages. Power dissipation and thermal limits should be observed.
VDD Power Supply	5 V, only supports 5 V input, external conversion to 3.3 V required for 3.3 V controller SDO interface.
nFAULT/NAD Pin	Refer to nFAULT/NAD Pin section
Energy Reservoir Capacitor	Refer to VREG Voltage and Capacitance Measurement section

8.2.2 Detailed Design Procedure

Transient Thermal Information

Since the device drives a fast transient pulse, transient thermal information is important for proper thermal design. The table below summarizes the transient thermal resistance (Junction-to-ambient) for a sample 4 layer, 2 cm x 2 cm x 1.6 mm PCB design with no additional heat sinking. The 4 layers uses 2 oz copper on top/ bottom signal layers and 1 oz copper on internal supply layers,with 0.3 mm thermal via drill diameter, 0.025 mm Cu plating, 1 minimum mm via pitch.

Table 8-2. Transient Thermal Impedance

$R_{\theta JA}$	$R_{\theta JA}$	$R_{\theta JA}$
1.2 C/W	2.3 C/W	70.1 C/W

8.2.3 Application Performance Plots

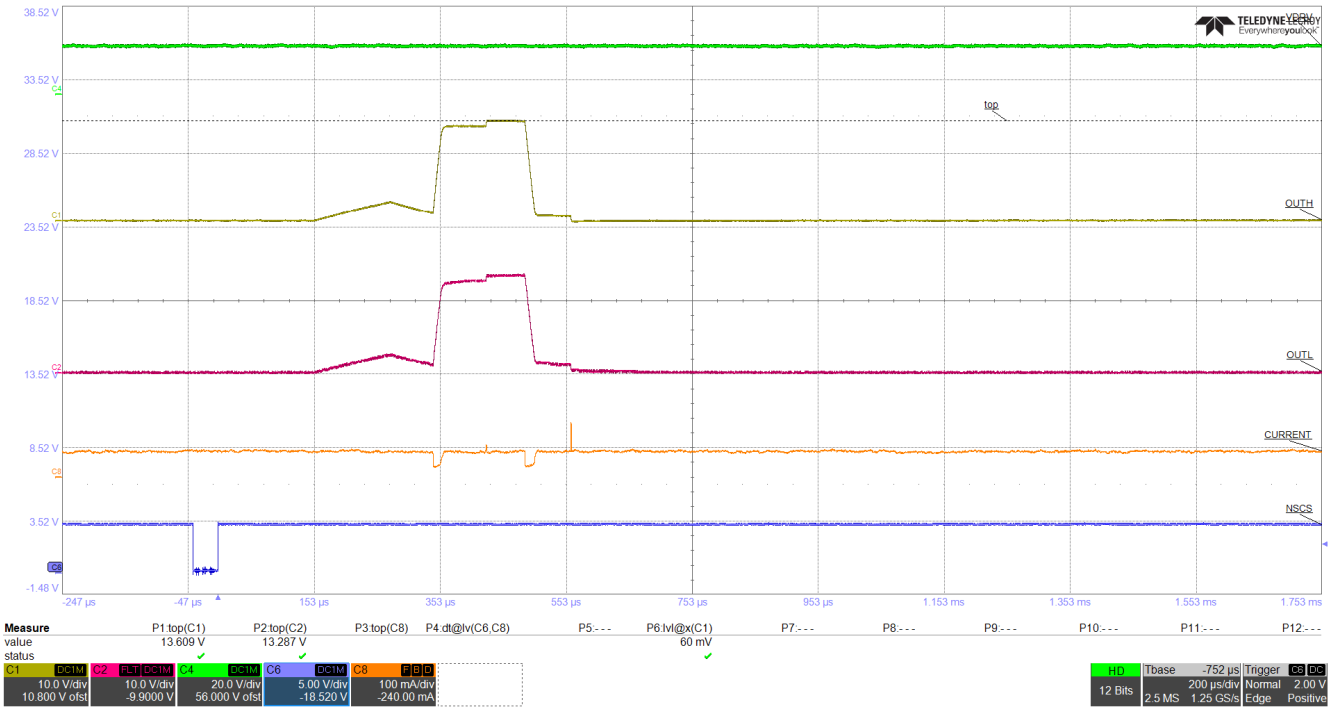


Figure 8-2. Off-State Diagnostics Sequence Example

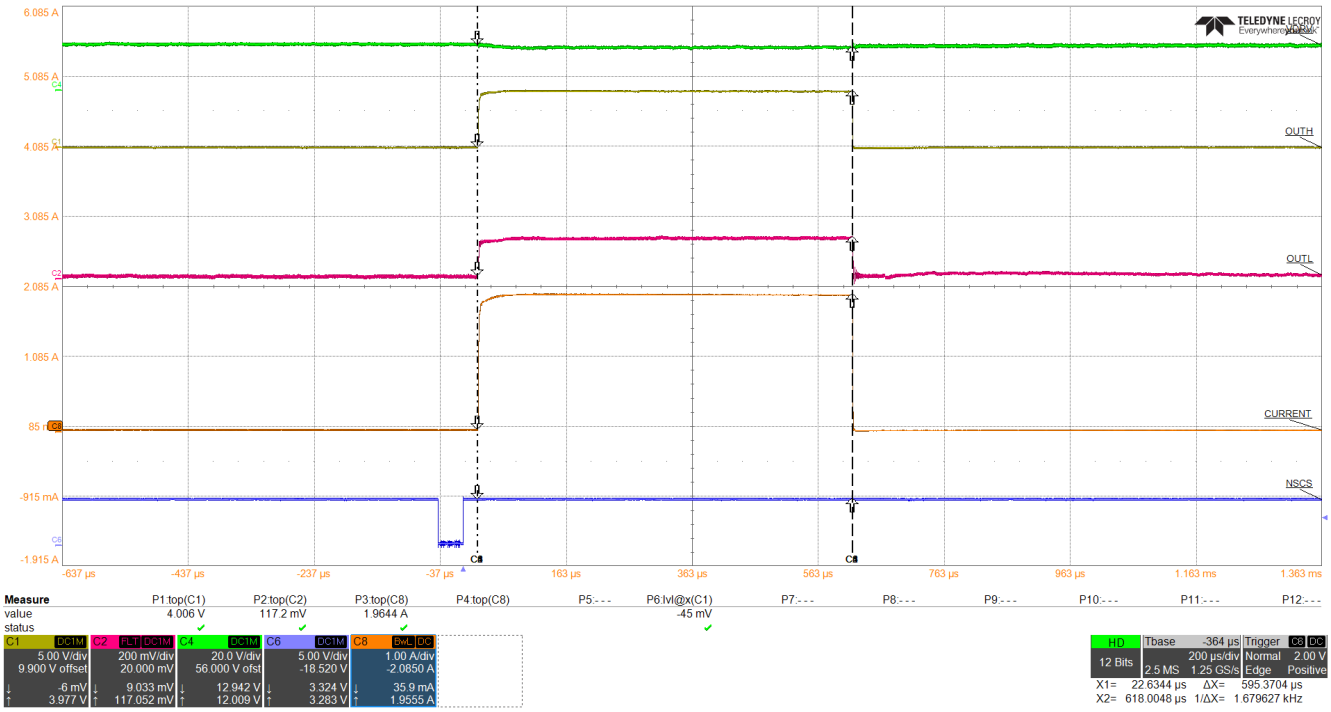


Figure 8-3. Typical Deployment Sequence with ISEL = 2h

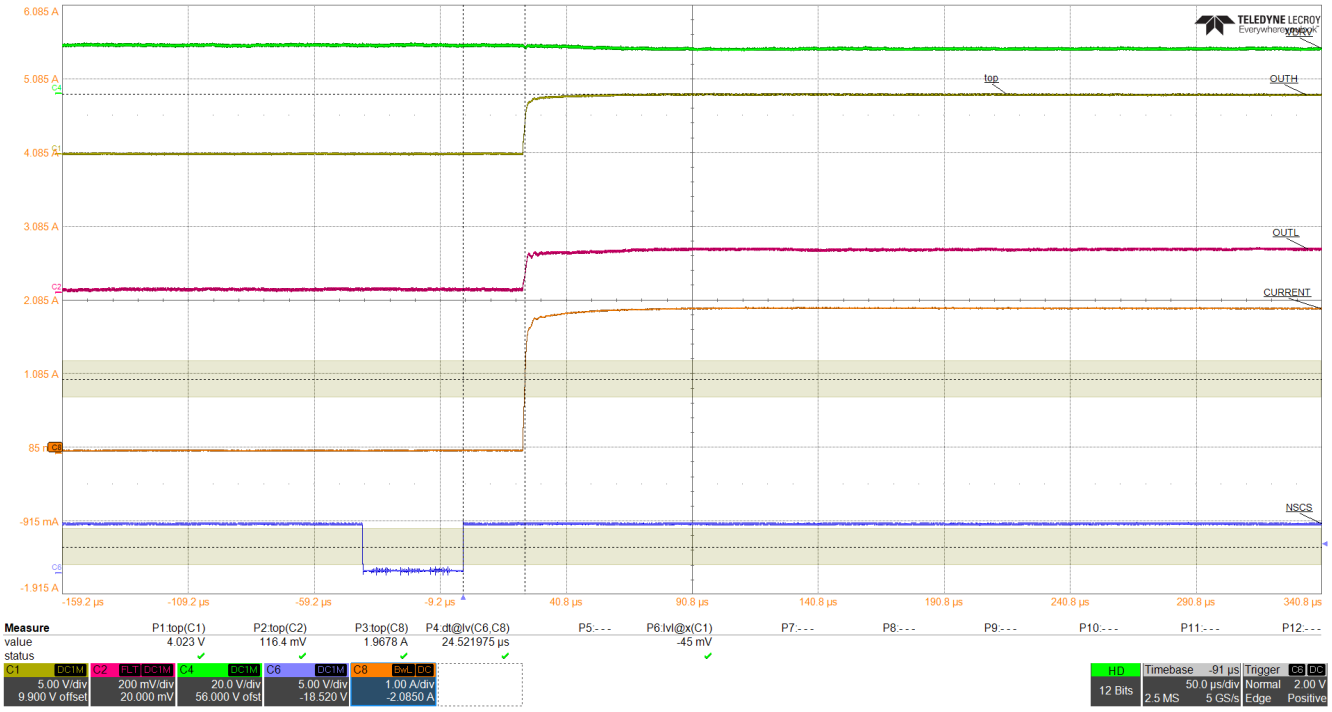


Figure 8-4. Typical Deployment Sequence with ISEL = 2h (Zoom)

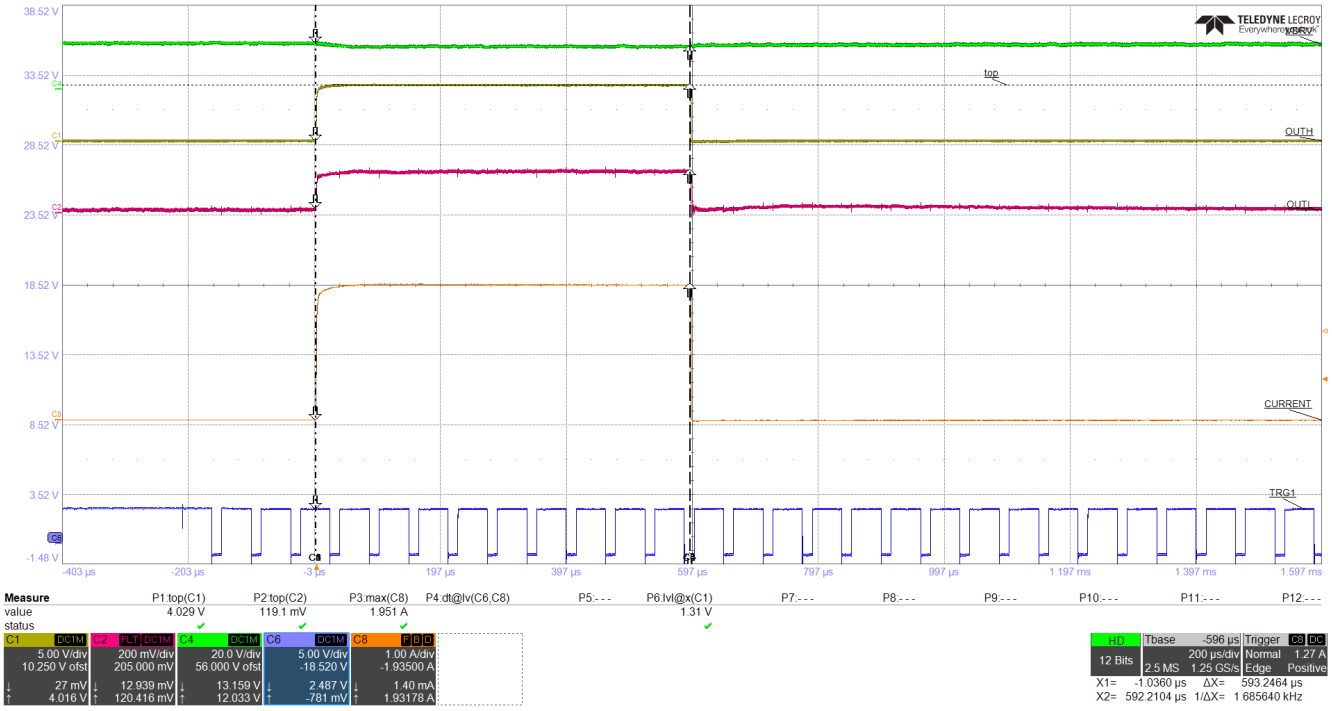


Figure 8-5. Trigger Pin (TRGx) Deployment With PWM Encoding (TRG_SEL = 8h)

8.2.4 Initialization Setup

Listed below are the **recommended** device initialization and application setup procedures for software development.

8.2.4.1 Device Initialization - NAD

The steps below describe the procedure for initial device startup and the node address NAD initialization.

1. WAIT- After PVDD and VDD ramp up, wait t_{READY} time.
2. STATUS0_READ - Read STATUS0 of each device on the same addressed SPI bus. A normal response would include:
   a. Confirm correct device address (NAD) values.
   b. Device reset (POR) bit is asserted.
   c. Device warning (WARNINGS) bit is asserted (due to CONFIG_CRC_W).
   d. The status of the trigger pins (TRGx_PIN_STAT) = 0h (No data yet).
3. VDD_ERR - If the SDO response indicates VDD_ERR, this indicates a supply issue with any of the devices on the addressed SPI bus. Check the condition of VDD and PVDD power supplies and repeat STATUS0_READ. The power-up initialization of the device is gated till supply monitor flags, VDRV_UV, VDD_OV and VDD_UV, are clear.
4. NAD_ERR - If the SDO response indicates NAD_ERR, this indicates a NAD address determination issue with any of the devices on the addressed SPI bus. Check the pull-up resistor on nFAULT/NAD pin to VDD, followed by:
   a. Issue a broadcast command with the RE_INIT_NAD bit asserted.
   b. Wait t_{READY} time.
   c. Follow up with a broadcast command with RE_INIT_NAD bit cleared. The SDO response will include NAD_ERR and previous command content (command confirmation). If response still indicates a NAD_ERR, then refer to NAD_RECOVERY.
   d. Cycle back to STATUS0_READ
5. NO_RESPONSE – This would indicate one of the following:
   a. Device Error (DEV_ERR) – nFAULT pin will be asserted low. A power cycle is needed to proceed.
   b. No device found on the addressed NAD. This indicates the NAD determination on this specific NAD is incorrectly mapped to a different NAD. In this case, refer to NAD_CONFLICT_CREATION.
6. NAD_RECOVERY – Issue the following commands to force the NAD address:
   a. Issue a broadcast command with NAD_OVERRIDE bit set with intended NAD address. The device with NAD_ERR picks up this command and assigns itself the commanded NAD address.
   b. Follow up with a broadcast command with NAD_OVERRIDE bit cleared. Response will include NAD_ERR and previous command content (command confirmation). NAD_ERR should be cleared.
   c. Cycle back to STATUS0_READ.
7. NAD_CONFLICT_CREATION – This procedure assumes that the hardware has the ability to assert TRG1 pin high or low individually to each device on the addressed SPI.
   a. Assert TRG1 pin high on device whose NAD is incorrectly mapped, while asserting TRG1 pin low on other devices on the addressed SPI.
   b. Read STATUS1 of each one of the devices on the addressed SPI bus. Since STATUS1 reads TRG1_PIN_LVL, the device with TRG1 high will detect an SDO conflict with the other device and back off transmitting on SDO with a NAD_ERR.
   c. Follow the NAD_RECOVERY steps to correct the NAD_ERR.

8.2.4.2 Device Initialization - Configuration

The steps below describe the procedure for device configuration.

1. Calculate the CRC8 for the 9 bytes of the desired CONFIG register space settings. The 9 bytes are contructed by appending all the CONFIG registers, starting at CONFIG0 to CONFIG4, MSB to LSB.
2. Write CONFIG0 – CONFIG4 to configure the device as needed along with the calculated CRC8 in the CONFIG4 register lower byte.
3. Issue a CLR_FAULT command and read STATUS0
4. A normal response would include:

a. Correct address & NAD values
b. POR bit cleared
c. WARNINGS bit cleared
d. Correct status of the trigger pins (TRGx_PIN_STAT)

8.2.4.3 System Initialization

1. Perform all the system initialization checks **as needed** at this point. Note that these tests are only meant to be performed in the device STANDBY state. These include:
   a. Trigger PWM Pattern Check.
   b. Device Timing Check.
   c. nFAULT Signaling Check.
   d. Secondary Logic Check.
2. Perform Off-State Diagnostics - Initial Check.

8.2.4.3.1 Trigger PWM Pattern Check

This test is recommended to be performed during system initialization to establish compatability between the pattern transmitter (e.g. over current sensor) and the device, needed only if TRGx PWM signalling is used.

1. Write CMD0 = 18h - Triggers disabled,
2. Issue deploy pattern on each of the TRGx pins,
3. Read TRGx_PIN_STAT in the STATUS0 register to check the pattern detection,
4. Issue normal pattern on each of the TRGx pins,
5. Read TRGx_PIN_STAT in the STATUS0 register to check the heartbeat detection,
6. Write CMD0 = 00h - Triggers enabled,

8.2.4.3.2 Device Timing Check

This test is recommended to be performed during system initialization only if device timing check is needed.

1. Write CMD0 = 1Bh - Triggers disabled, request timing signal assert on nFAULT.
2. nFAULT pin will be driven with a 75% 16K Hz PWM output.
3. Write CMD0 = 18h - Triggers remain disabled, request timing signal de-assert.
4. Write CMD1 = 80h – CLR_FAULT so that request is processed.
5. nFAULT pin will be controlled by nFAULT_CONFIG settings at this point.

8.2.4.3.3 nFAULT Signalling Check

This test is recommended to be performed during system initialization only if nFAULT pin fault signalling is used.

1. Write CMD0 = 19h - Triggers disabled, request nFAULT assert.
2. Write CMD1 = 80h – CLR_FAULT so that request is processed.
3. nFAULT pin will be asserted low. This can be confirmed by reading back nFAULT_PIN_STAT in STATUS0 register.
4. Write CMD0 = 18h - Triggers remain disabled, request nFAULT de-assert.
5. Write CMD1 = 80h – CLR_FAULT so that request is processed.
6. nFAULT pin will be controlled by nFAULT_CONFIG settings at this point.

8.2.4.3.4 Secondary Logic Check

This test is recommended to be performed during system initialization only if the safety layer check of the device is needed.

1. Write CMD0 = 1Ah - Triggers disabled, force secondary logic time out assert
2. Within 40 msec, nFAULT pin will be asserted low to indicate time out. Also SDO is HiZ once time out occurs.
3. Write CMD0 = 18h - Triggers disabled, request secondary logic time out de-assert.
4. SDO resumes normal operation.
5. Write CMD1 = 80h – CLR_FAULT so that time out de-assert request is processed.

6. nFAULT pin will be controlled by nFAULT_CONFIG settings at this point

8.2.4.3.5 Off-State Diagnostics - Initial Check

All 8 tests in the off-state diagnostics are recommended to be performed as part of system initialization.

1. Ensure CONFIG1 lower byte = 00h so that all tests are enabled
2. Write CMD1 = 94h to trigger the test sequence (CLR_FAULT also asserted), followed by CMD1 = 00h. Response will include previous command content (command confirmation).
3. Wait ~14 msec (depends on the CONFIG settings for testxxx_TSEL) for tests to complete
4. Read STATUS0 and STATUS3
5. A normal response should indicate
   a. OFF_DIAG_SUM = 2h
   b. VREG voltage measurement - VREG_VMEAS
   c. VREG capacitance estimation - T_VREG_CAP
6. It is recommended that subsequent periodic off-state diagnostics need only weak pull up & pull down followed by VREG and RLOAD measurements. Accordingly, issue CONFIG1 lower byte = 9Ch along with CONFIG4 CRC8 update.
7. Issue CMD0 = 0x00h to enable all TRGx pins
8. Also, it is recommended to issue CMD1 = 40h to set LOCK_CONFIG to prevent any inadvertent configuration register SPI write during operation.

8.2.4.4 Off-State Diagnostics - Periodic Check

This subset of 4 tests out of 8 tests in the off-state diagnostics is recommended to be performed periodically to validate the health of the deployment function.

1. It is assumed that CONFIG1 lower byte = 9Ch so that only weak pull up & pull down followed by VREG and RLOAD measurements tests are enabled
2. Write CMD1 = D4h to trigger the test sequence (CLR_FAULT, LOCK_CONFIG also asserted), followed by CMD1 = 40h. Response will include previous command content (command confirmation).
3. Wait ~8 msec (depends on the CONFIG settings for testxxx_TSEL) for tests to complete
4. Read STATUS0 and STATUS3
5. A normal response should indicate
   a. OFF_DIAG_SUM = 2h
   b. VREG voltage measurement - VREG_VMEAS
   c. VREG capacitance estimation - T_VREG_CMPx

8.2.4.5 Deployment

8.2.4.5.1 Targeted Device Deployment

1. Write CMD1 = D8h (No deployment delay) or DCh (with deployment delay) to trigger the deployment (CLR_FAULT, LOCK_CONFIG also asserted), followed by CMD1 = 40h. Response will include previous command content (command confirmation).
2. Wait ~1 msec or ~3 msec (depends on the DEPLOY_ISEL settings) for deployment to complete
3. Read STATUS0, STATUS2 , MEAS0 and MEAS1
4. A normal response should indicate
   a. DEPLOY_SUM = 2h
   b. DEPLOY_STAT = 0h
   c. Deployment start time measurement - TSTART_MEAS

Deployment current duration measurement – TDEPLOY_MEAS

8.2.4.5.2 Broadcast Deployment

1. Write CMD2 = 84h (No deployment delay) or 86h (with deployment delay) to trigger the deployment (CLR_FAULT, LOCK_CONFIG also asserted), followed by CMD2 = 00h. Response will include previous command content (command confirmation).
2. Wait ~1 msec or ~3 msec (depends on the DEPLOY_ISEL settings) for deployment to complete
3. Read STATUS0, STATUS2 , MEAS0 and MEAS1
4. A normal response should indicate
   a. DEPLOY_SUM = 2h
   b. DEPLOY_STAT = 0h
   c. Deployment start time measurement - TSTART_MEAS
   d. Deployment current duration measurement – TDEPLOY_MEAS

8.2.4.5.3 Off-State Diagnostics - Post Deployment

1. Issue CMD1 = 00h to unlock CONFIG (assuming that it was locked before)
2. Write CONFIG1 lower byte = FDh so that only RLOAD measurements test is enabled, along with CONFIG4 lower byte CRC8 update. Optional - Write OFF_DIAG_RMEAS_THRS_H_SEL = 3h for highest threshold setting.
3. Write CMD1 = D4h to trigger the test sequence (CLR_FAULT, LOCK_CONFIG also asserted), followed by CMD1 = 40h. Response will include previous command content (command confirmation).
4. Wait ~2 msec (depends on the CONFIG settings for OFF_DIAG_RMEAS_TSEL) for test to complete
5. Read STATUS0 and STATUS3
6. A normal response should indicate OFF_DIAG_SUM = 4h, indicating that the load resistance is high

8.3 Power Supply Recommendations

PVDD/VREG/VDRV: The DRV3901-Q1 has multiple power pins to enable several features on the primary power supply. These features include the option for an energy reservoir capacitor (C_{VREG}) and a reverse current blocking diode. PVDD is the power supply connection from the system and should be connected to the system high voltage supply and to the DRV3901-Q1 PVDD pin. PVDD should be connected to the VREG pin with an external diode (D0) sized for the inrush current of the squib and inrush current of the energy reservoir capacitor if in use. VREG can either be directly connected to VDRV by shorting the pins together, or optionally a reverse current blocking diode (D1) can be connected if the system must protect against a failure mode condition where OUTL is shorted to power supply, while VREG/PVDD are low.

VDD: The device requires a 5V low voltage supply to function as both the logic supply and as a redundant power supply for several safety monitoring functions.

8.4 Layout

8.4.1 Layout Guidelines

- TRGx pin if not used can be shorted to GND, pin 24 (No connect) can be shorted to GND.
- The VDRV supply pin must be bypassed to ground (optionally the PVDD and VDD pins) using low-ESR ceramic bypass capacitors with recommended values. These capacitors should be placed as close to the pins as possible with a thick trace or ground plane connection to the device GND pin. Additional bulk capacitance for energy reservoir may be required to on VREG pin. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.
- OUTH pins #10,11,18,19 and OUTL pins # 8,9,20,21 are internally connected. Given that deployment times are typically small, it can be ok to leave one side of the OUTH / OUTL pins OPEN, while connecting only the other side to the load if the PCB layout requires.
  1. Example 1: Connect load between pins # 8,9 and pins # 10,11. Leave pins # 18,19,20,21 OPEN.
  2. Example 2: Connect load between pin#18,19 and pins # 20,21. Leave pins # 8,9,10,11 OPEN.

8.4.2 Layout Example

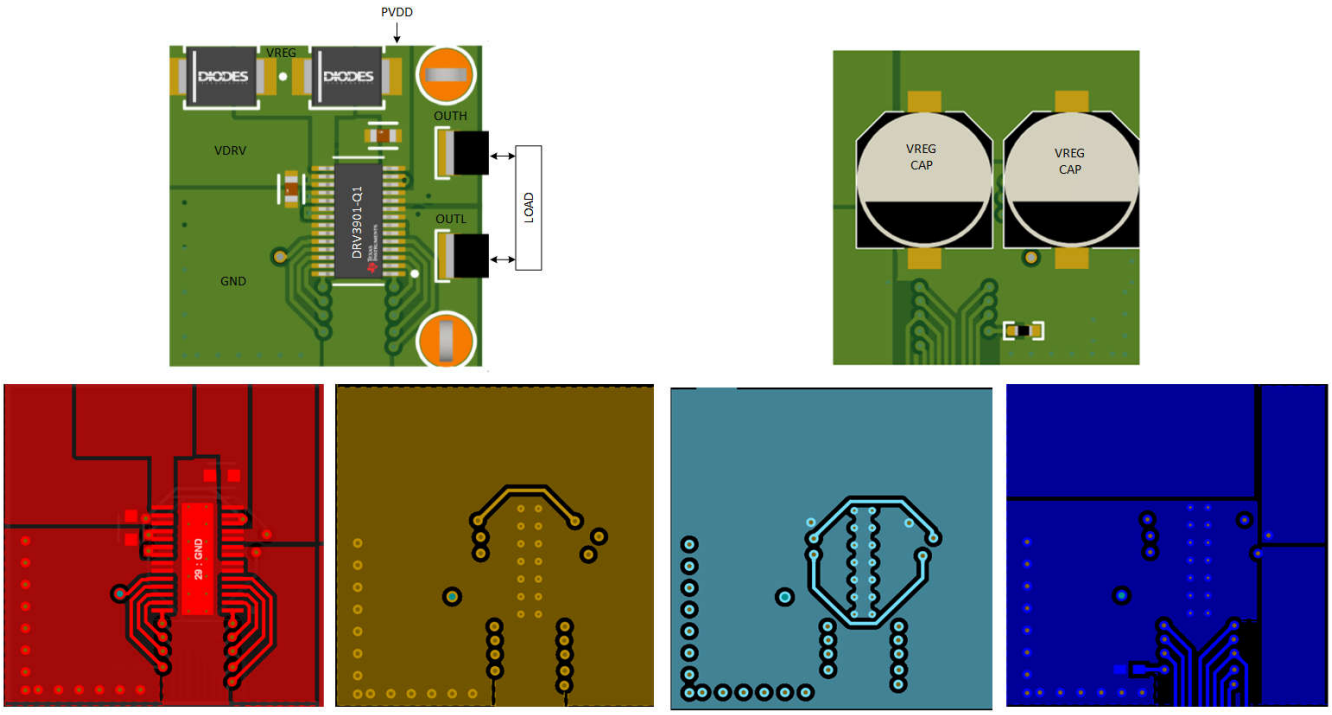


Figure 8-6. DRV3901-Q1 Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical Packaging and Orderable Information

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
DRV3901QDGQRQ1	ACTIVE	HVSSOP	DGQ	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	3901

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

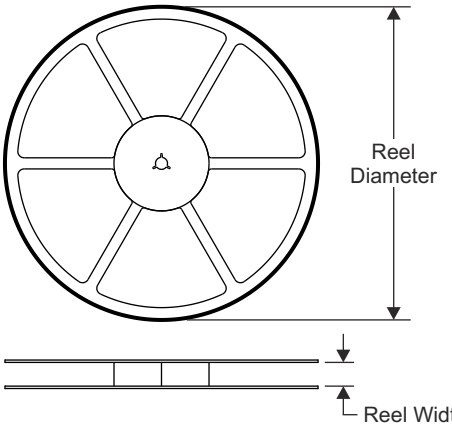
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

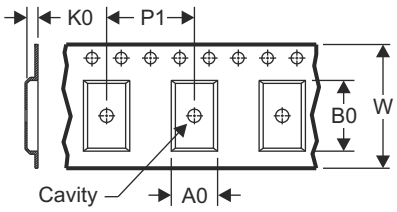
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

10.2 Tape and Reel Information

REEL DIMENSIONS

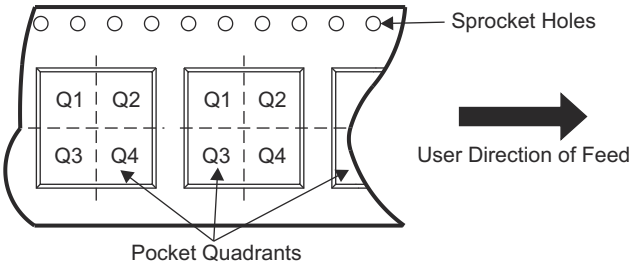


TAPE DIMENSIONS



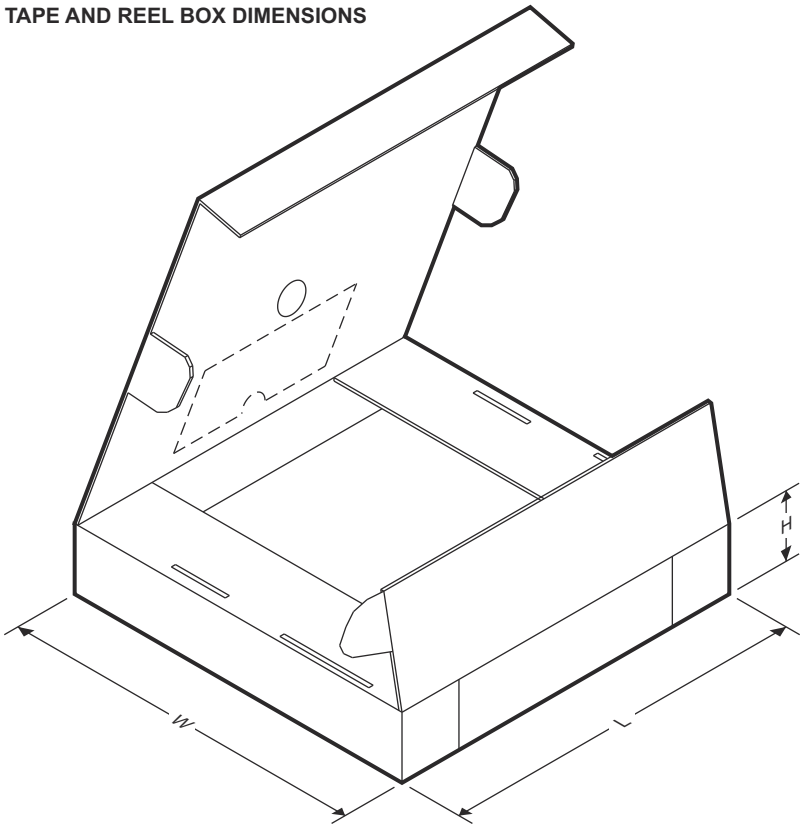
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3901QDGQRQ1	HVSSOP	DGQ	28	2500	330.00	16.40	5.50	7.40	1.45	8.00	16.00	Q1

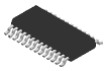
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3901QDGQRQ1	HVSSOP	DGQ	28	2500	356	356	35

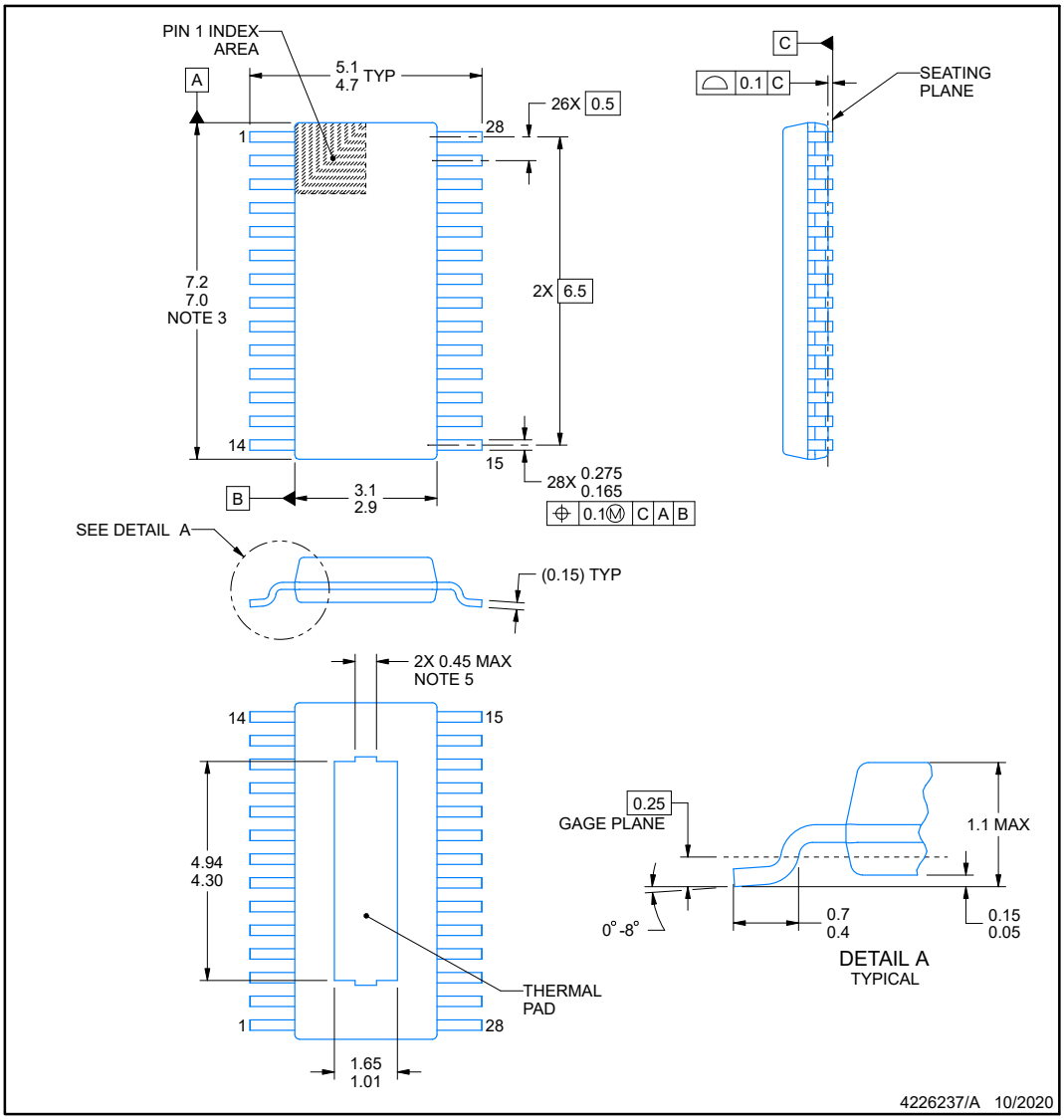
PACKAGE OUTLINE

DGQ0028A



PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

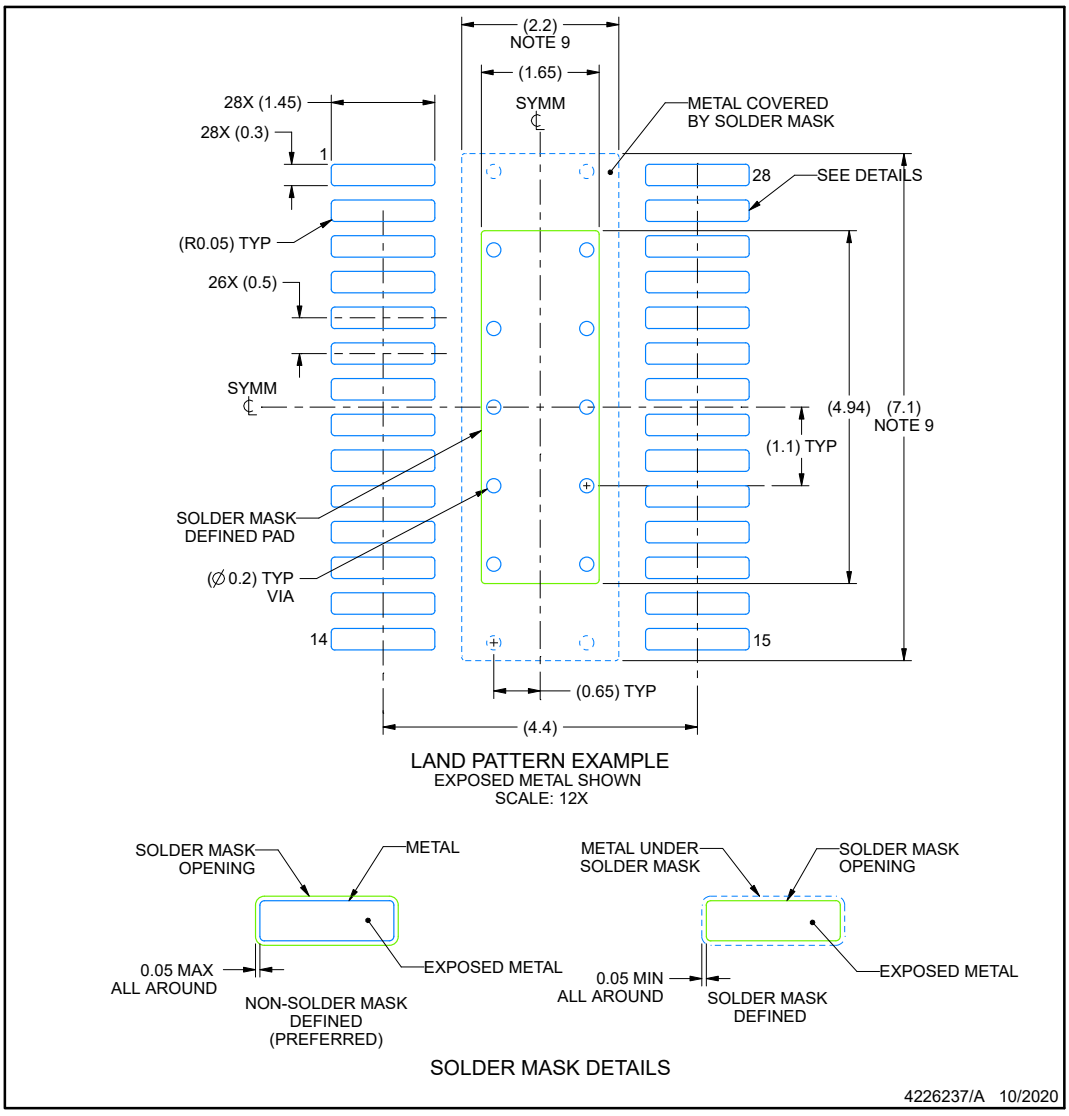
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGQ0028A — **PowerPAD™ VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



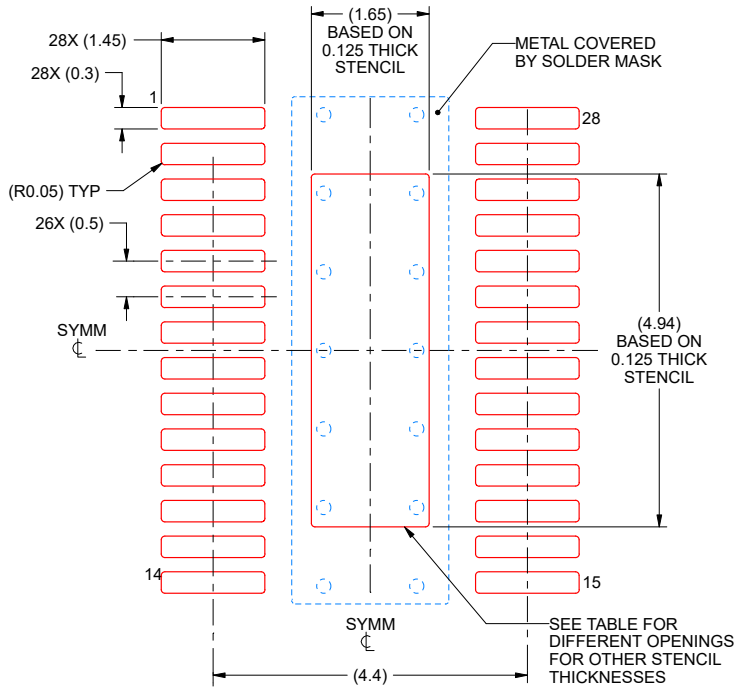
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGQ0028A — **PowerPAD™ VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 5.52
0.125	1.65 X 4.94 (SHOWN)
0.15	1.51 X 4.51
0.175	1.39 X 4.18

4226237/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV3901QDGQRQ1	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3901
DRV3901QDGQRQ1.A	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	3901

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

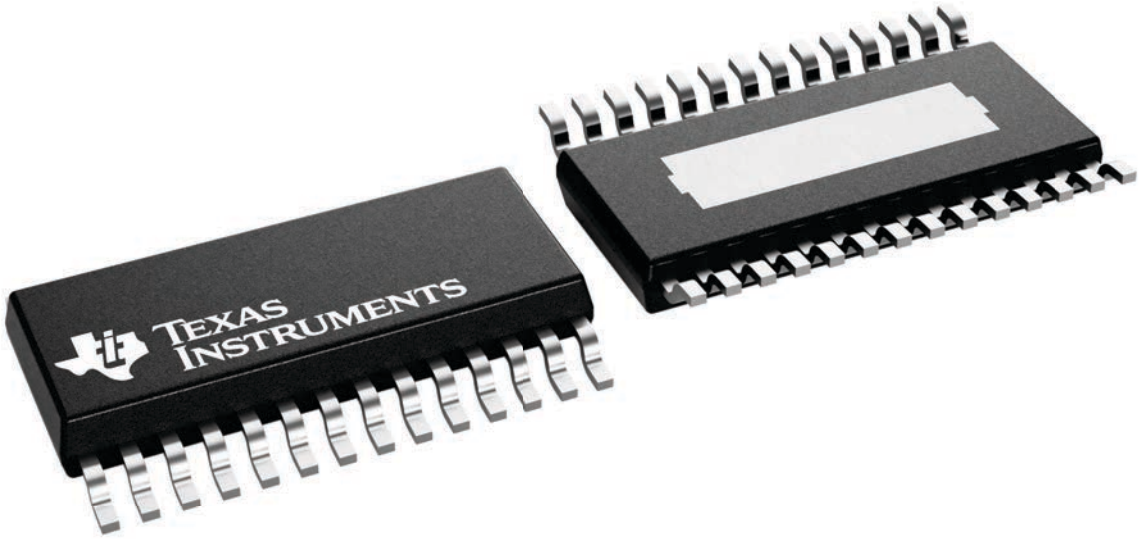
DGQ 28

HVSSOP - 1.1 mm max height

3 x 7.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



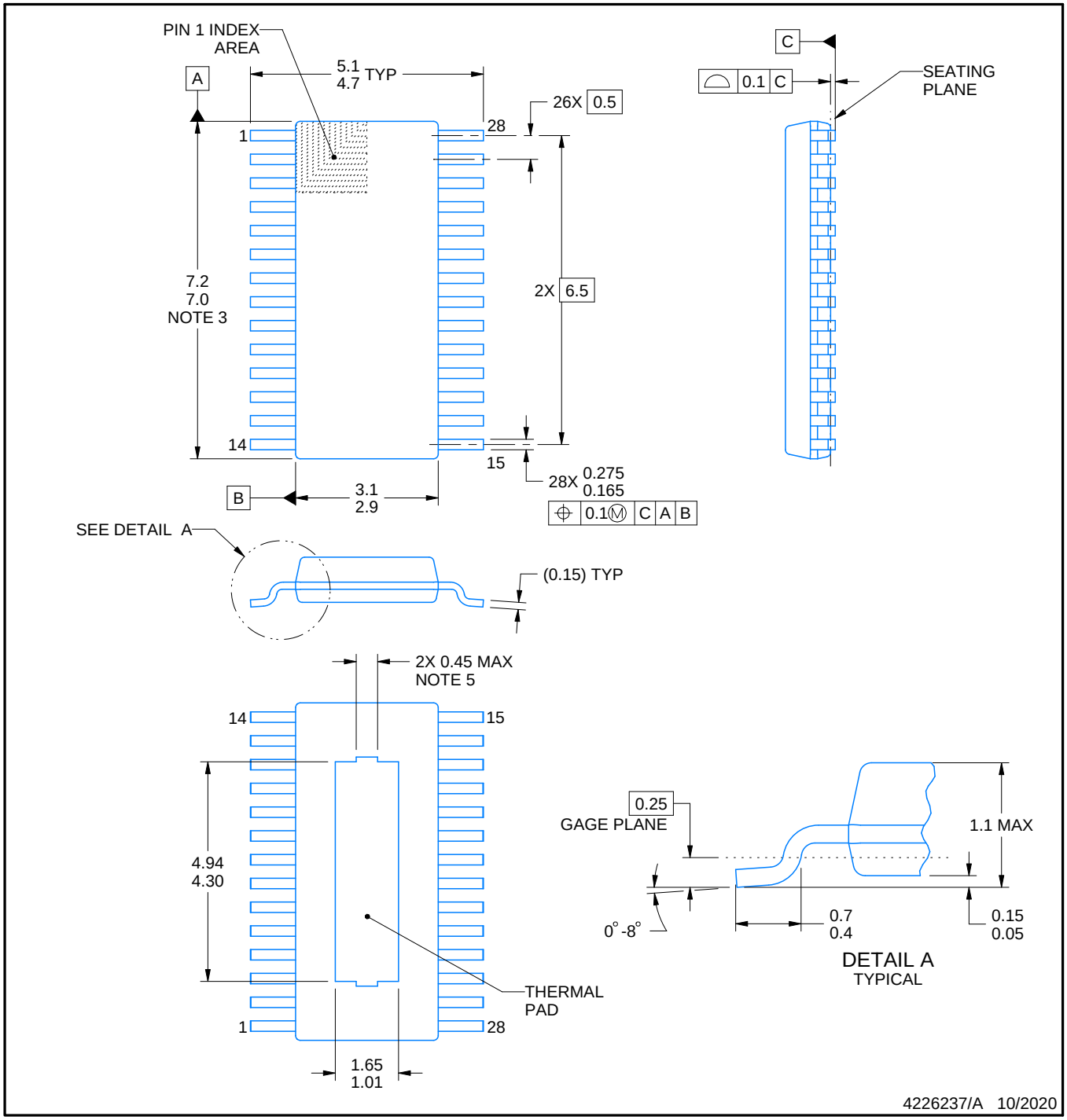
4226530/A

PACKAGE OUTLINE

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

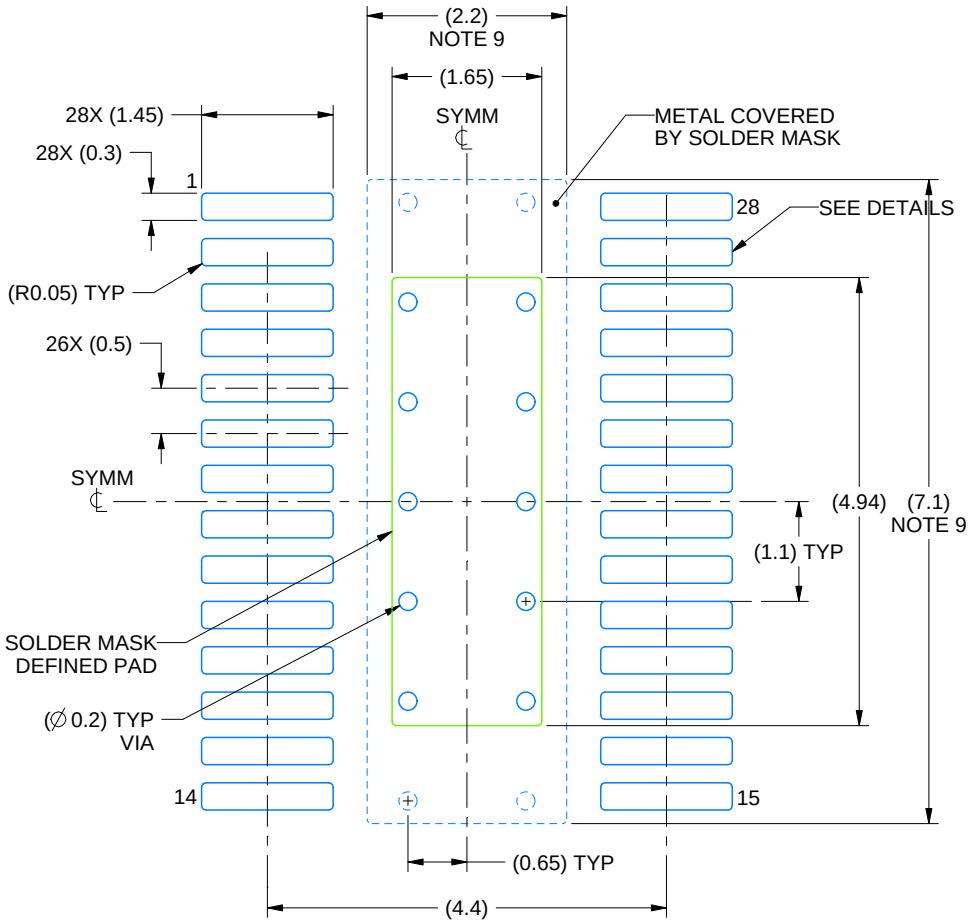
SMALL OUTLINE PACKAGE



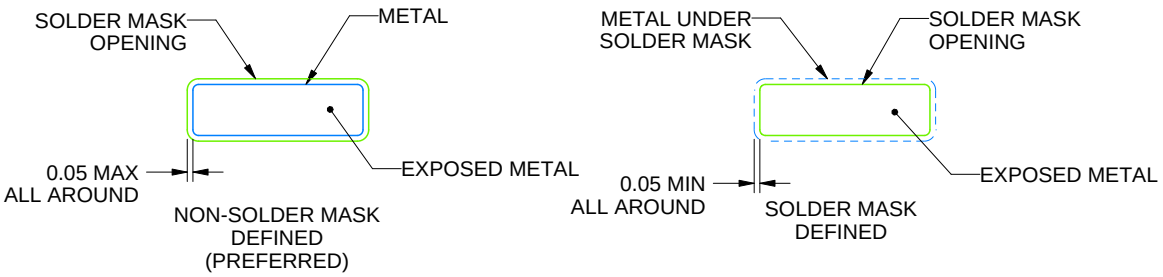
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

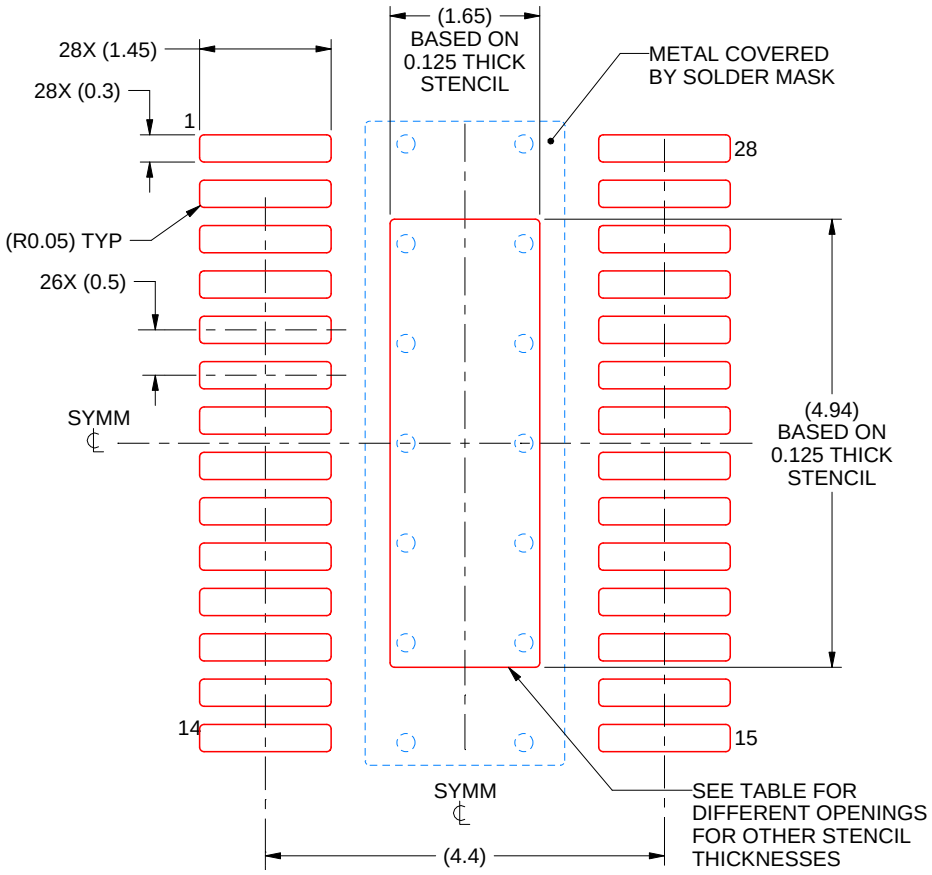


SOLDER MASK DETAILS

4226237/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 5.52
0.125	1.65 X 4.94 (SHOWN)
0.15	1.51 X 4.51
0.175	1.39 X 4.18

4226237/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025