# DRV3245Q-Q1 3-Phase Automotive Gate Driver Unit (GDU) With High Performance Sensing, Protection and Diagnostics

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, $T_A$
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL D
  - Systematic capability up to ASIL D
- 4.5-V to 45-V operating voltage
- Programmable peak gate drive currents up to 1A
- Charge-pump gate driver for 100% Duty Cycle
- Current-shunt amplifiers and phase comparators
  - A / C Device: 3 current-shunt amplifiers(1) and 3-phase comparators with status through SPI [1]
  - B Device: 2 current-shunt amplifiers and 3-phase comparators with real-time monitor through digital pins
  - S Device: 3 current-shunt amplifiers
- 3-PWM or 6-PWM input control up to 20 kHz
- Single PWM-mode commutation capability
- Supports both 3.3-V and 5-V digital interface
- Serial peripheral interface (SPI)
- Thermally-enhanced 48-Pin HTQFP
- Protection features:
  - Internal regulators, battery voltage monitor
  - SPI CRC
  - Clock monitor
  - Analog built-in self test
  - Programmable dead-time control
  - MOSFET shoot-through prevention
  - MOSFET $V_{DS}$ overcurrent monitors
  - Gate-source voltage real time monitor
  - Overtemperature warning and Shutdown

## 2 Applications

- 12-V automotive motor-control applications
  - Electrical power steering (EPS, EHPS)
  - Electrical brake and brake assist
  - Transmissions and pumps

## 3 Description

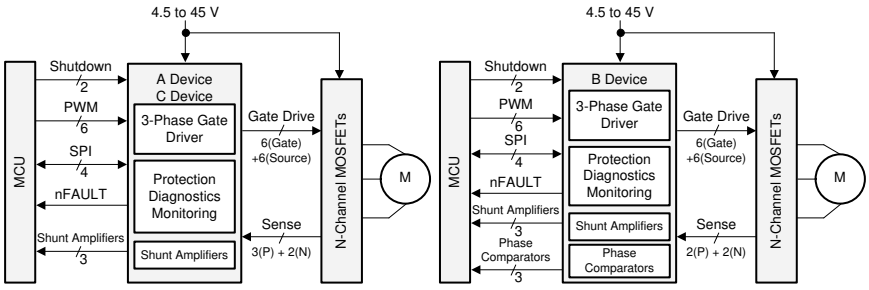
The DRV3245Q-Q1 device is a FET gate driver IC for three-phase motor-drive applications designed according to the applicable requirements of ISO 26262 for functional safety applications. The device provides three half-bridge drivers each capable of driving a high-side and low-side N-channel MOSFET while also providing sophisticated protection and monitoring of the FETs. A charge-pump driver enables 100% duty cycle and supports low battery voltages during cold-crank operation. The integration of current-sense amplifiers, integrated phase comparators, and SPI-based configuration of the driver and its peripherals enable reduction of the bill of materials (BOM) and space on the printed circuit board (PCB) because of the elimination of most external and passive components.

The DRV3245Q-Q1 device also integrates diagnostics and protection for each internal block and provides support for common system diagnostic checks each of which can be instantiated and reported through SPI. This flexibility of the integrated features allows the device to integrate seamlessly into a variety of safety architectures.

**Package Information**

| PART NUMBER(1) | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV3245Q-Q1 | PHP (HTQFP,48) | 7.00 mm × 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Simplified Schematic**

[1] C device : Low-drift offset high-precision amplifiers

# Table of Contents

# 4 Device and Documentation Support

## 4.1 Device Support

### 4.1.1 Device Nomenclature

Figure 4-1 shows a legend for reading the complete orderable device name for the DRV3245Q-Q1 device

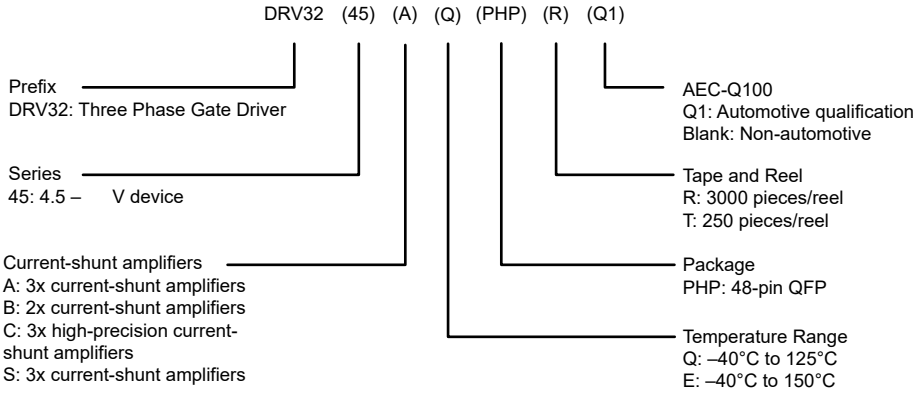



**Figure 4-1. Device Nomenclature**

## 4.2 Documentation Support

### 4.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *PowerPAD™ Integrated Circuit Package Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Integrated Circuit Package Made Easy* application report
- Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430™Microtocontroller* application report
- Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers* application report

## 4.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 4.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 4.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (May 2023) to Revision D (June 2024) | Page |
|---|---|
| • Updated functional safety bullet | 1 |

| Changes from Revision B (October 2019) to Revision C (May 2023) | Page |
|---|---|
| • Added the DRV3245S device | 1 |
| • Changed all instances of legacy terminology to controller and peripheral where SPI is mentioned | 1 |

| Changes from Revision A (May 2018) to Revision B (October 2019) | Page |
|---|---|
| • Added DRV3245C device | 1 |

| Changes from Revision * (November 2017) to Revision A (May 2018) | Page |
|---|---|
| • Changed the device status from: *Advance Information* to: *Production Data* | 1 |

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 6.1 Package Option Addendum

**Table 6-1. Packaging Information**

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish(4) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking(5) (6) |
|---|---|---|---|---|---|---|---|---|---|---|
| DRV3245AQPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV3245AQ |
| DRV3245BQPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV3245BQ |
| DRV3245CQPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV3245CQ |
| DRV3245SQPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV3245SQ |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PRE_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

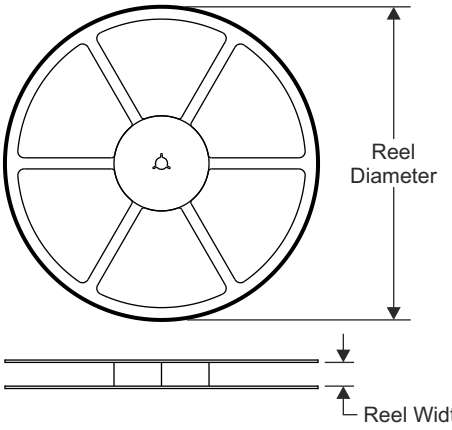
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

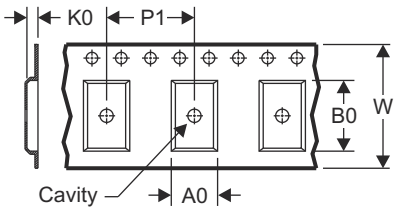
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

## 6.2 Tape and Reel Information

**REEL DIMENSIONS**

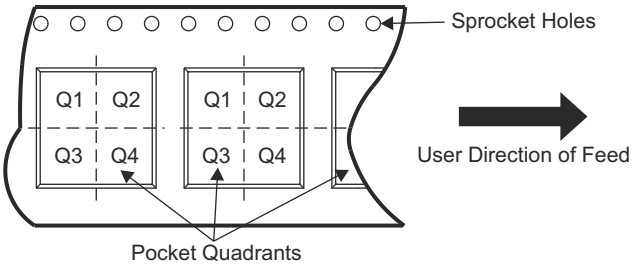



**TAPE DIMENSIONS**



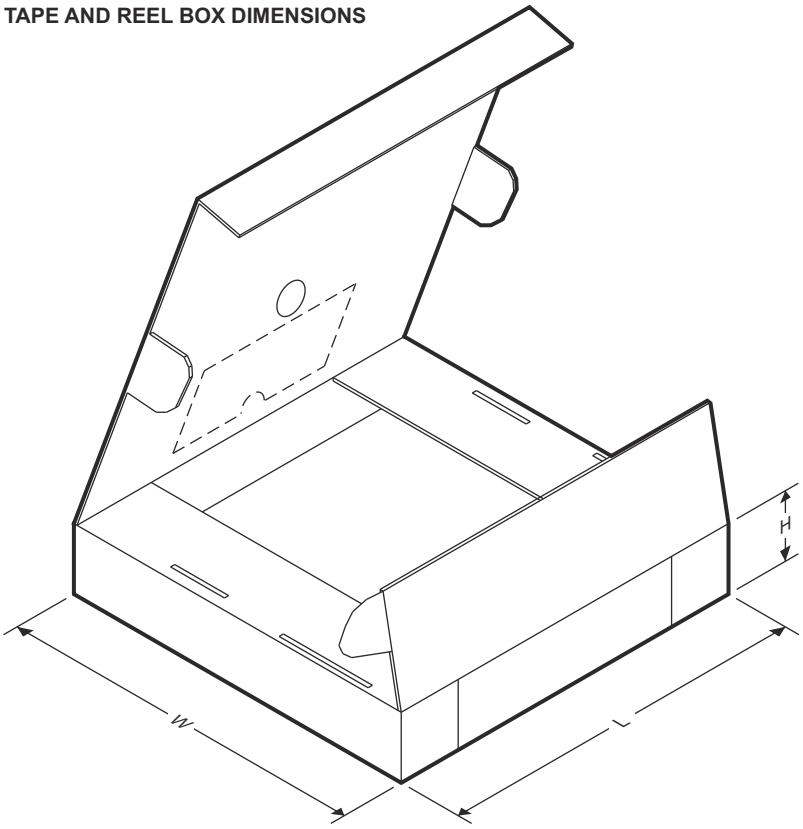

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV3245AQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| DRV3245BQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| DRV3245CQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| DRV3245SQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



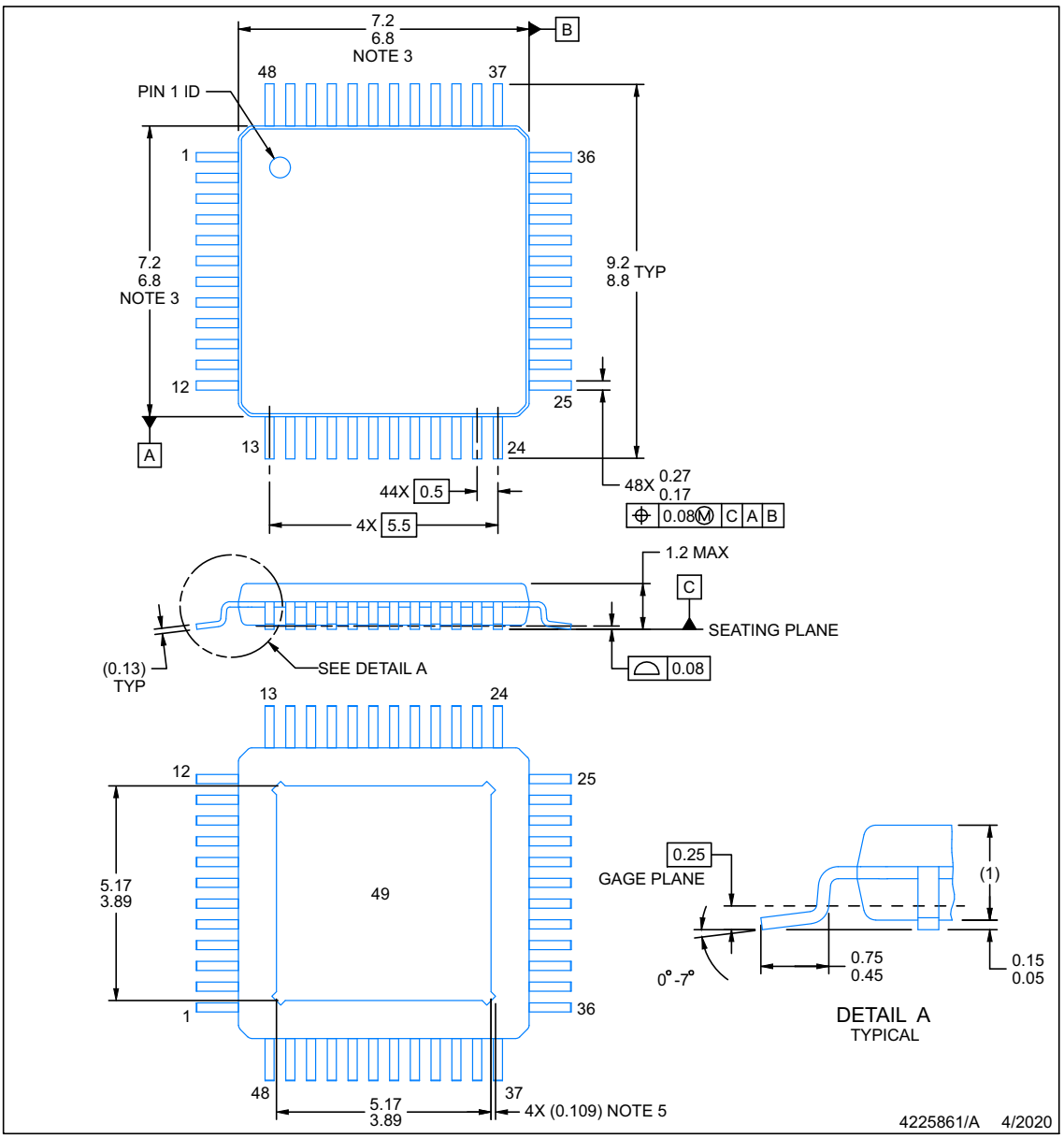

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV3245AQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |
| DRV3245BQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |
| DRV3245CQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |
| DRV3245SQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |

## 6.3 Mechanical Data

### PACKAGE OUTLINE

**PHP0048G** — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK




PowerPAD is a trademark of Texas Instruments.

NOTES:

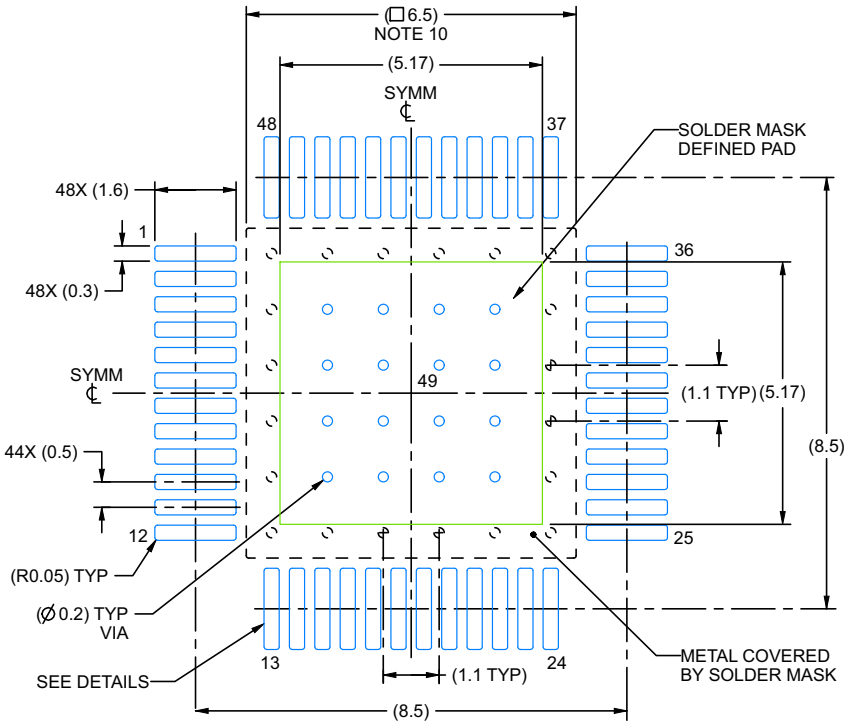
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

# EXAMPLE BOARD LAYOUT

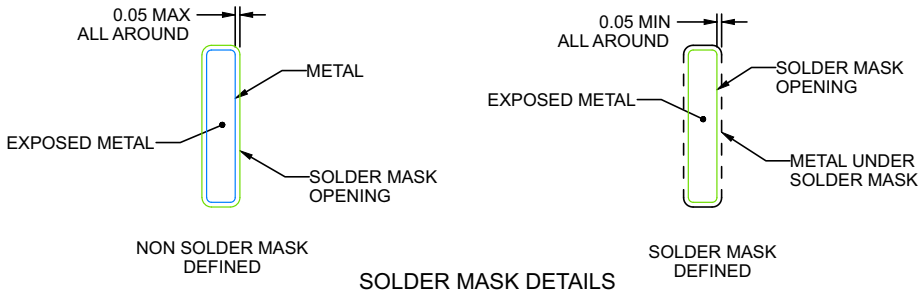
## PHP0048G

**PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4225861/A 4/2020

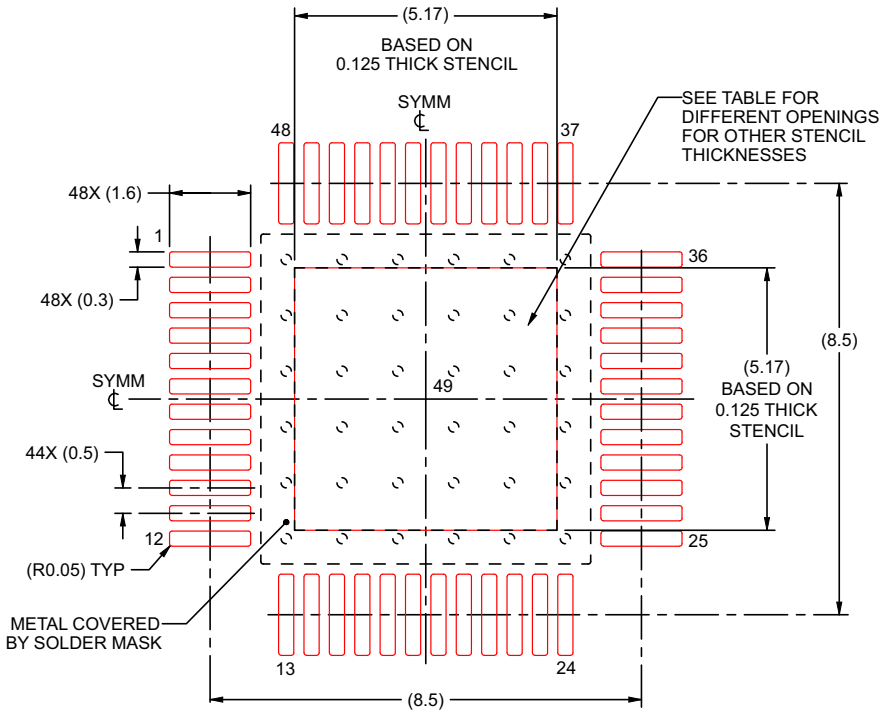
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

**PHP0048G** — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 5.78 X 5.78 |
| 0.125 | 5.17 X 5.17 (SHOWN) |
| 0.150 | 4.72 X 4.72 |
| 0.175 | 4.37 X 4.37 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DRV3245AQPHPRQ1 | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DR3245AQ |
| DRV3245AQPHPRQ1.A | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DR3245AQ |
| DRV3245BQPHPRQ1 | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DR3245BQ |
| DRV3245BQPHPRQ1.A | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DR3245BQ |
| DRV3245CQPHPRQ1 | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DR3245CQ |
| DRV3245CQPHPRQ1.A | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DR3245CQ |
| DRV3245SQPHPRQ1 | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 150 | DR3245SQ |
| DRV3245SQPHPRQ1.A | Active | Production | HTQFP (PHP) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 150 | DR3245SQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

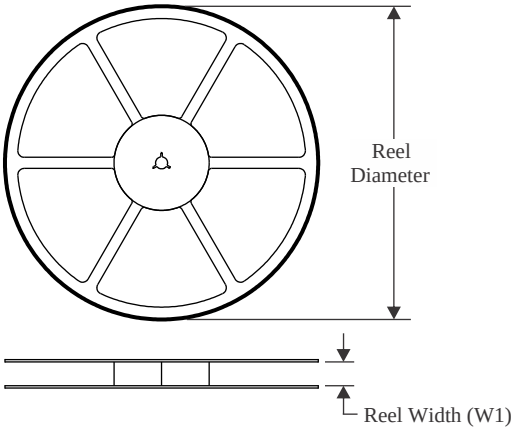
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

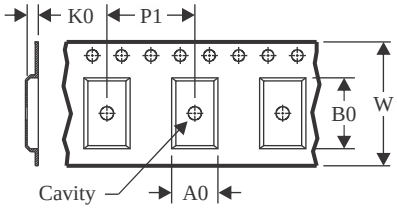
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

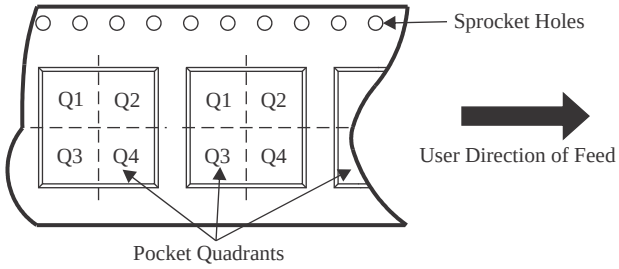



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

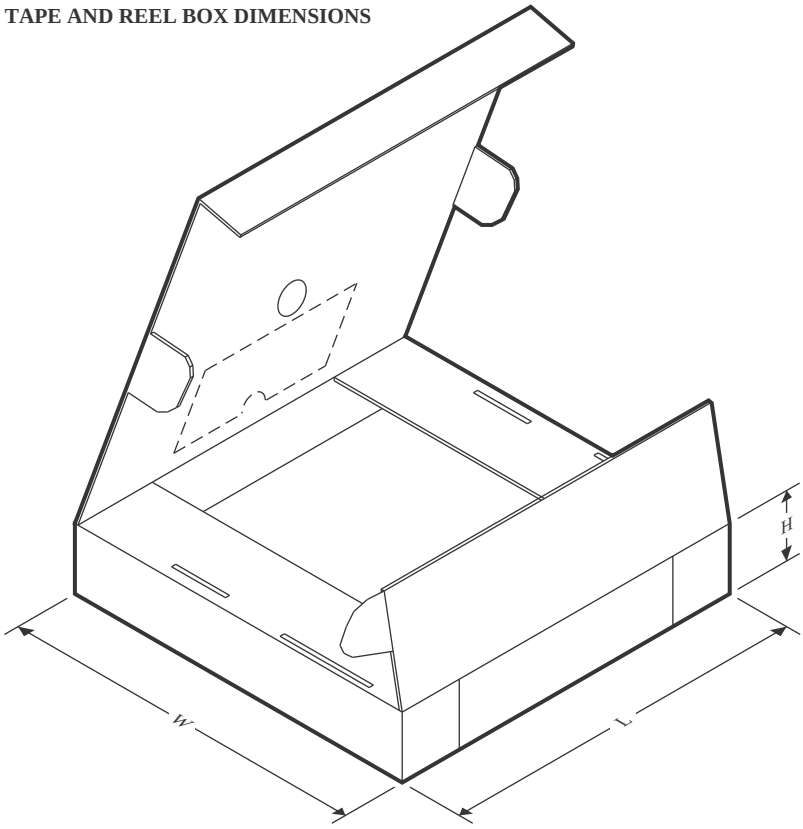
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV3245AQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| DRV3245BQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| DRV3245CQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| DRV3245SQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV3245AQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |
| DRV3245BQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |
| DRV3245CQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |
| DRV3245SQPHPRQ1 | HTQFP | PHP | 48 | 1000 | 350.0 | 350.0 | 43.0 |

# GENERIC PACKAGE VIEW

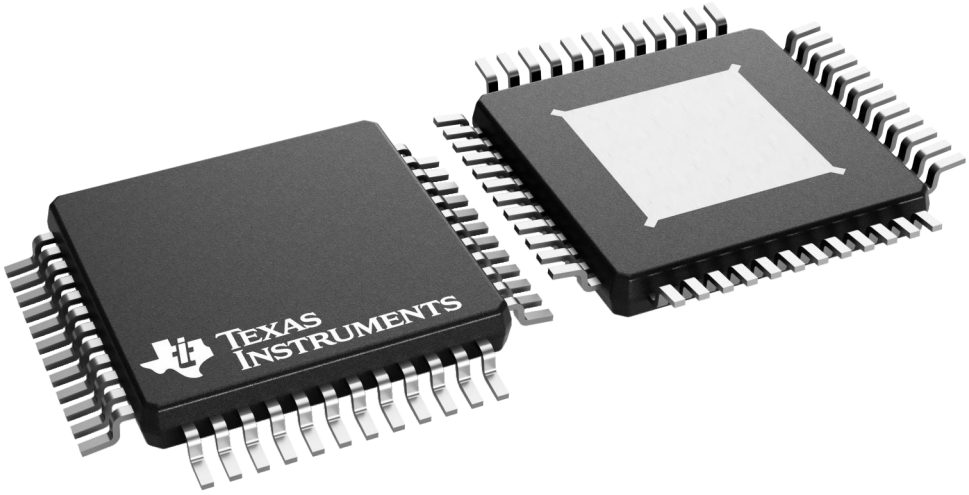
## PHP 48

## TQFP - 1.2 mm max height

**7 x 7, 0.5 mm pitch**

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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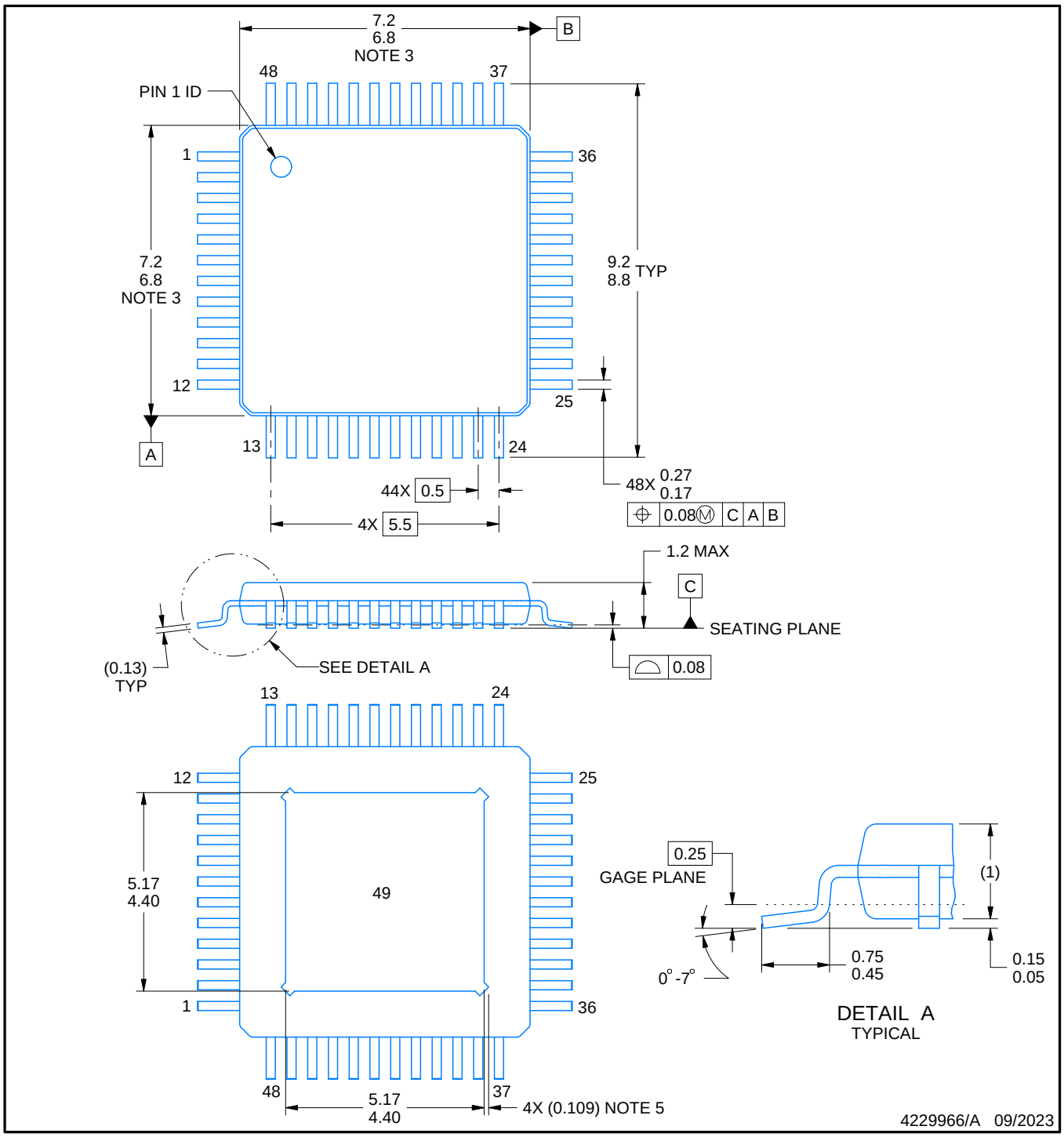
# PACKAGE OUTLINE

## PHP0048N

## PowerPAD™ HTQFP - 1.2 mm max height

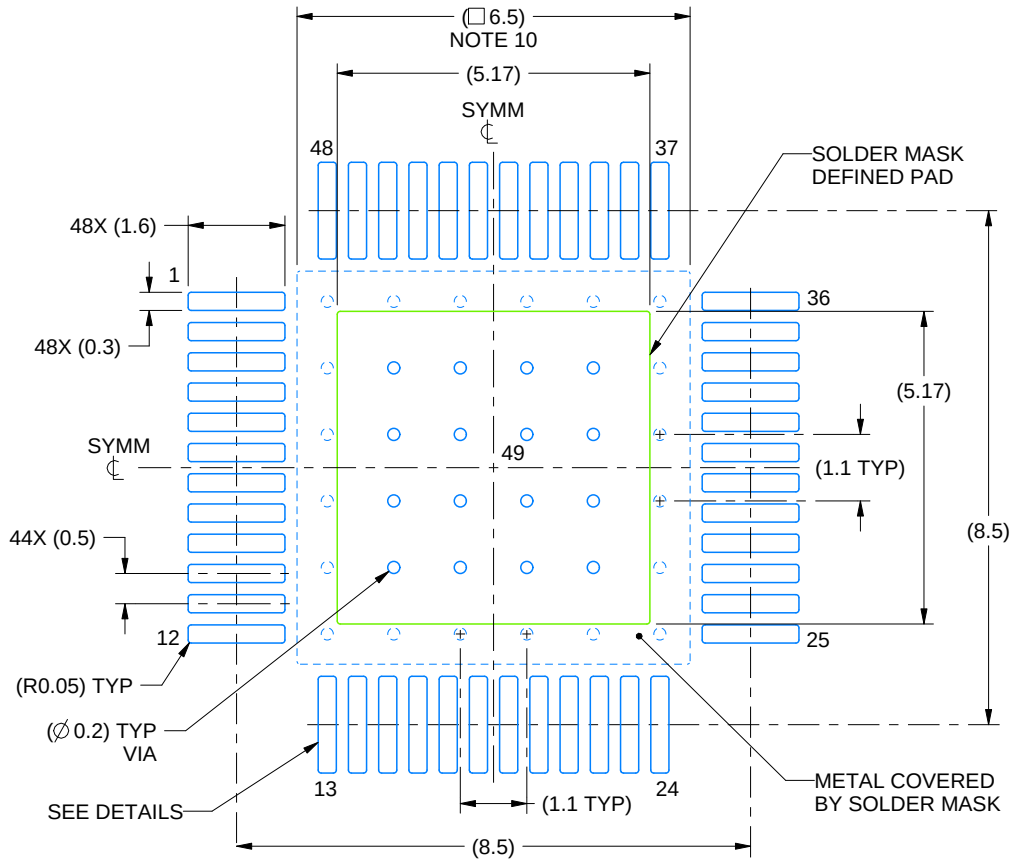
PLASTIC QUAD FLATPACK



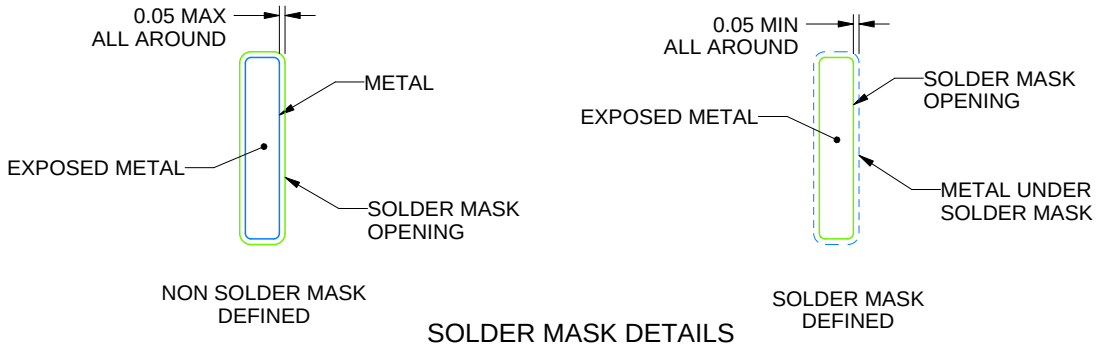

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

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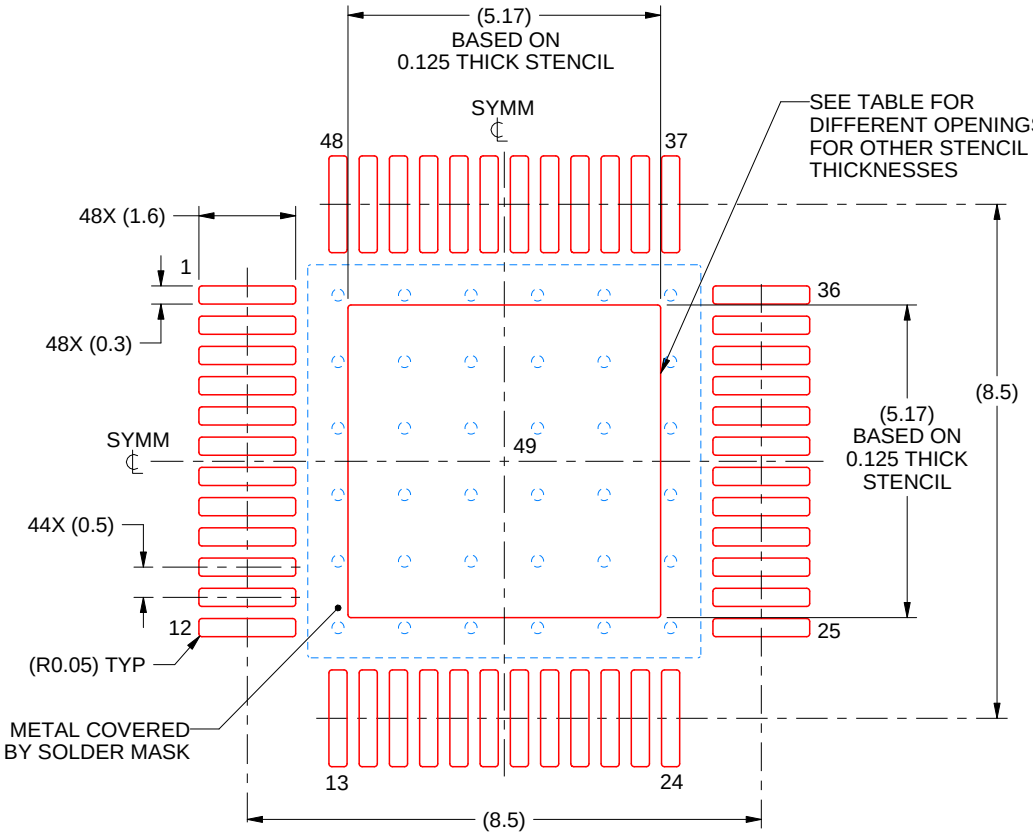
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 5.78 X 5.78 |
| 0.125 | 5.17 X 5.17 (SHOWN) |
| 0.150 | 4.72 X 4.72 |
| 0.175 | 4.37 X 4.37 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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