DRV2911-Q1 Full-Bridge PWM Input Piezo Driver for Ultrasonic Lens Cleaning

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C ≤ TA ≤ 125°C
  - Wettable flank package
- 2-Channel half bridge driver
  - PWM-inputs for each half bridge control
  - Overcurrent protection
  - Supports up to 200kHz PWM frequency
- 5V to 35V operating voltage (40V abs max)
- High output current capability: 8A Peak
- Low MOSFET on-state resistance
  - 95mΩ (typ.) $R_{DS(ON)}$ (HS + LS) at T_A = 25°C
- Low power sleep mode
  - 2.5µA (max.) at V_{PVDD} = 13.5V, T_A = 25°C
- Supports 1.8V, 3.3V, and 5V logic inputs
- Built-in 3.3V, 30mA LDO regulator
- Integrated protection features
  - Supply undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal warning and shutdown (OTW/OTSD)
  - Fault condition indication pin (FAULTZ)

2 Applications

- Automotive Thermal Camera
- Camera module without processing
- Mirror replacement/camera mirror system
- Rear Camera
- Surround view system ECU

3 Description

DRV2911-Q1 integrates two H-bridges for driving piezo-based Lens Cover Systems, LCS, up to 40V absolute maximum capability while maintaining a very low $R_{DS(ON)}$ to reduce switching losses. DRV2911-Q1 integrates a power management LDO (3.3V / 30mA) and buck converter (5V to 5.7V, ≤200mA) that can be used to power external circuits like the Ultrasonic Lens Cleaning (ULC) controller, ULC1001.

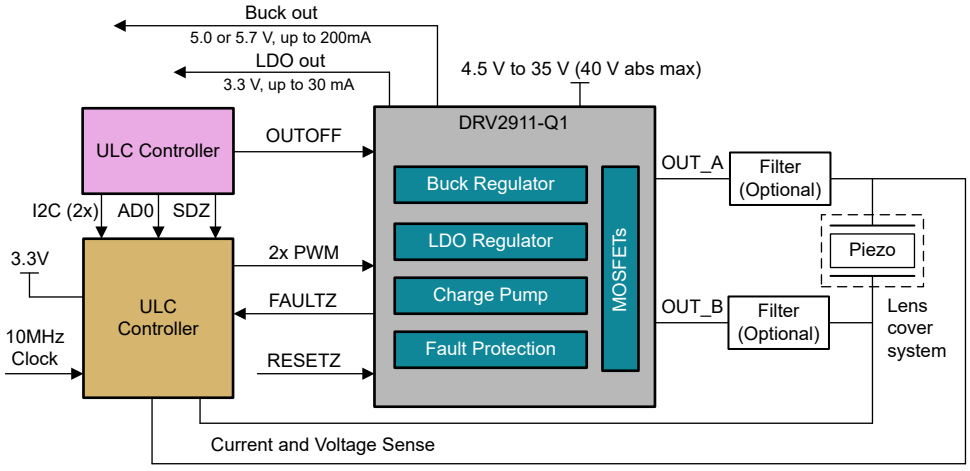
Each output driver channel consists of N-channel power MOSFETs configured in a half-bridge configuration. Two independent PWM inputs drive each half-bridge. The DRV2911-Q1 includes a 30mA, 3.3V LDO regulator.

Several protection features including supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), overcurrent protection (OCP), over-temperature warning (OTW), and over-temperature shutdown (OTSD) are integrated into DRV2911-Q1 to protect the device and system against fault events. Fault conditions are indicated by the FAULTZ pin. The fault pin can also be tied to the controller device, like ULC1001-Q1, where a fault can be recognized over I2C.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DRV2911-Q1	VQFN (40)	7mm x 5mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

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4 Pin Configuration and Functions

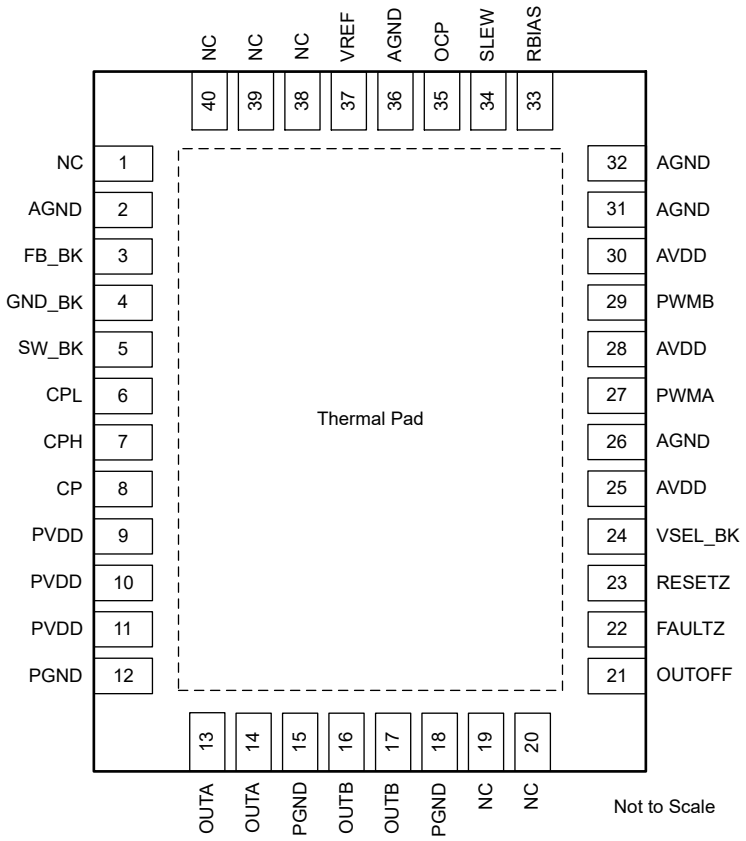

Figure 4-1. DRV2911-Q1 40-Pin VQFN With Thermal Pad Down (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	1, 19, 20, 38, 39, 40	NC	No connection, open.
AGND	2, 26, 31, 32, 36	GND	Device analog ground. Refer to Section 7.4.1 for connecting recommendations.
FB_BK	3	PWR I	Feedback for buck regulator. Connect to buck regulator output after the inductor/resistor.
GND_BK	4	GND	Buck regulator ground. Refer to Section 7.4.1 for connection recommendations.
SW_BK	5	PWR O	Buck switch node. Connect this pin to an inductor or resistor.
CPL	6	PWR	Charge pump switching node. Connect a X5R or X7R, 47nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
CPH	7	PWR	
CP	8	PWR O	Charge pump output. Connect a X5R or X7R, 1-µF, 16V ceramic capacitor between the CP and PVDD pins.
PVDD	9, 10, 11	PWR I	Power supply. Connect to supply voltage; bypass to PGND with two 0.1µF capacitors (for each pin) plus one bulk capacitor rated for PVDD. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
PGND	12, 15, 18	GND	Device power ground. Refer to Section 7.4.1 for connections recommendation.
OUTA	13, 14	PWR O	Half bridge output A.
OUTB	16, 17	PWR O	Half bridge output B.
OUTOFF	21	I	When this pin is logic high the four MOSFETs in the power stage are turned OFF making all outputs Hi-Z.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
FAULTZ	22	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to AVDD or an external source. Ensure that FAULTZ is pulled > 2.2V on power up.
RESETZ	23	I	Driver RESETZ. When this pin is logic low, the device goes into a low-power sleep mode. A 20 to 40µs low pulse can be used to reset fault conditions without entering sleep mode.
VSEL_BK	24	I	Buck output voltage setting. This pin is a 2-level input pin set by an external resistor. Refer to Figure 6-2.
AVDD	25, 28, 30	PWR O	3.3V internal regulator output. Connect an X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the AVDD (near pin 25) and AGND pins. This regulator can source up to 30 mA externally.
PWMA	27	I	PWM input for half-bridge A control.
PWMB	29	I	PWM input for half-bridge B control.
RBIAS	33	I	Tie 47kΩ resistor to AVDD.
SLEW	34	I	Slew rate control setting. This pin is a 4-level input pin set by an external resistor. Refer to Figure 6-2.
OCP	35	I	OCP level control setting. Refer to Figure 6-2.
VREF	37	PWR	Connect a X5R or X7R, 0.1µF, 6.3V ceramic capacitor between the VREF and AGND pins.
Thermal pad		GND	Must be connected to analog ground.

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (PVDD)	–0.3	40	V
Power supply voltage ramp (PVDD)		4	V/µs
Voltage difference between ground pins (GND_BK, PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CPH, CP)	–0.3	V_{PVDD}+ 6	V
Charge pump negative switching pin voltage (CPL)	–0.3	V_{PVDD} + 0.3	V
Switching regulator pin voltage (FB_BK)	–0.3	6	V
Switching node pin voltage (SW_BK)	–0.3	V_{PVDD} + 0.3	V
Analog regulator pin voltage (AVDD)	–0.3	4	V
Logic pin input voltage (OUTOFF, PWMx, RESETZ)	–0.3	5.75	V
Logic pin output voltage (FAULTZ)	–0.3	5.75	V
Output pin voltage (OUTA, OUTB)	–1	V_{PVDD}+ 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings Auto

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Power supply voltage	V_{PVDD}	4.5	24	35	V
f_{PWM}	Output PWM frequency	OUTA, OUTB			200	kHz
I_{OUT} (1)	Peak output current	OUTA, OUTB			8	A
V_{IN}	Logic input voltage	OUTOFF, PWMx, RESETZ	–0.1		5.5	V
V_{OD}	Open drain pullup voltage	FAULTZ	–0.1		5.5	V
I_{OD}	Open drain output current	FAULTZ			5	mA
V_{VREF}	Voltage reference pin voltage	VREF	2.8		AVDD	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

5.4 Thermal Information

THERMAL METRIC(1)		DRV2911-Q1 VQFN (RGF) 40 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{PVDD} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} > 6 V, RESETZ = 0, T_A = 25 °C		1.5	2.5	µA
		RESETZ = 0		2.5	5	µA
I_{PVDDS}	PVDD standby mode current	V_{PVDD} > 6 V, RESETZ = 1, PWMx = 0, I_{BK} = 0, T_A = 25 °C		5	6	mA
		RESETZ = 1, PWMx = 0, I_{BK} = 0		6	10	mA
I_{PVDD}	PVDD operating mode current	V_{PVDD} > 6 V, RESETZ = 1, f_{PWM} = 25 kHz, T_A = 25 °C		11	13	mA
		V_{PVDD} > 6 V, RESETZ = 1, f_{PWM} = 200 kHz, T_A = 25 °C		19	22	mA
		RESETZ =1, f_{PWM} = 25 kHz		12	17	mA
		RESETZ =1, f_{PWM} = 200 kHz		18	30	mA
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 30 mA	3.1	3.3	3.465	V
I_{AVDD}	External analog regulator load				30	mA
V_{VCP}	Charge pump regulator voltage	VCP with respect to PVDD	3.6	4.7	5.25	V
t_{WAKE}	Wakeup time	V_{PVDD} > V_{UVLO}, RESETZ = 1 to outputs ready and FAULTZ released			1	ms
t_{SLEEP}	Sleep Pulse time	RESETZ = 0 period to enter sleep mode	120			µs
t_{RST}	Reset Pulse time	RESETZ = 0 period to reset faults	20		40	µs
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF)	V_{PVDD} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	V
		V_{PVDD} > 6.7 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin tied to AVDD	5.2	5.7	5.8	V
		V_{PVDD} < 6.0 V, 0 mA ≤ I_{BK} ≤ 200 mA		V_{PVDD}– I_{BK}*(R_{LBK}+ 2)(1)		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF)	V_{PVDD} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	V
		V_{PVDD} > 6.7 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin tied to AVDD	5.2	5.7	5.8	V
		V_{PVDD} < 6.0 V, 0 mA ≤ I_{BK} ≤ 50 mA		V_{PVDD}– I_{BK}*(R_{LBK}+ 2)(1)		V

T_J = –40°C to +150°C, V_{PVDD} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF)	V_{PVDD} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	V
		V_{PVDD} > 6.7 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin tied to AVDD	5.2	5.7	5.8	V
		V_{PVDD} < 6.0 V, 0 mA ≤ I_{BK} ≤ 40 mA		V_{PVDD}– I_{BK}*(R_{BK}+2)		V
V_{BK_RIP}	Buck regulator ripple voltage	V_{PVDD} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, Buck regulator with inductor, L_{BK} = 47 uH, C_{BK} = 22 µF	–100		100	mV
		V_{PVDD} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with inductor, L_{BK} = 22 uH, C_{BK} = 22 µF	–100		100	mV
		V_{PVDD} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with resistor; R_{BK} = 22 Ω, C_{BK} = 22 µF	–100		100	mV
I_{BK}	External buck regulator load	L_{BK} = 47 uH, C_{BK} = 22 µF			200 – I_{AVDD}	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF			50 – I_{AVDD}	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF			40 – I_{AVDD}	mA
f_{SW_BK}	Buck regulator switching frequency	Regulation Mode	20		535	kHz
		Linear Mode	20		535	kHz
V_{BK_UV}	Buck regulator undervoltage lockout	V_{BK} rising, VSEL_BK pin to Hi-Z	2.7	2.8	2.9	V
		V_{BK} falling, VSEL_BK pin to Hi-Z	2.5	2.6	2.7	V
		V_{BK} rising, VSEL_BK pin tied to AVDD	4.2	4.4	4.55	V
		V_{BK} falling, VSEL_BK pin tied to AVDD	4.0	4.2	4.35	V
$V_{BK\_UV\_HYS}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold	90	200	320	mV
I_{BK_CL}	Buck regulator Current limit threshold		360	600	900	mA
I_{BK_OCP}	Buck regulator Overcurrent protection trip point		2	3	4	A
t_{BK_RETRY}	Overcurrent protection retry time		0.7	1	1.3	ms
LOGIC-LEVEL INPUTS (OUTOFF, PWMx, RESETZ)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	Other Pins	1.5		5.5	V
		RESETZ	1.6		5.5	V
V_{HYS}	Input logic hysteresis	Other Pins	180	300	420	mV
		RESETZ	95	250	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA
I_{IH}	Input logic high current	RESETZ, V_{PIN} (Pin Voltage) = 5 V	10		30	µA
		Other pins, V_{PIN} (Pin Voltage) = 5 V	30		75	µA
R_{PD}	Input pulldown resistance	RESETZ	150	200	300	kΩ
		Other pins	70	100	130	kΩ
C_{ID}	Input capacitance			30		pF
FOUR-LEVEL INPUTS (SLEW)						
V_{L1}	Input mode 1 voltage (25V/µs)	Tied to AGND	0		0.2*AVDD	V

T_J = –40°C to +150°C, V_{PVDD} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{L2}	Input mode 2 voltage (50V/µs)	Hi-Z	0.27*AVDD	0.5*AVDD	0.545*AVDD	V
V_{L3}	Input mode 3 voltage (125V/µs)	47 kΩ +/- 5% tied to AVDD	0.606*AVDD	0.757*AVDD	0.909*AVDD	V
V_{L4}	Input mode 4 voltage (200V/µs)	Tied to AVDD	0.945*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD	70	100	130	kΩ
R_{PD}	Input pulldown resistance	To AGND	70	100	130	kΩ
TWO-LEVEL INPUTS (VSEL_BK)						
V_{L1}	Input mode 1 voltage (5.0V)	Hi-Z	0.27*AVDD	0.5*AVDD	0.545*AVDD	V
V_{L2}	Input mode 2 voltage (5.7V)	Tied to AVDD	0.945*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD	70	100	130	kΩ
R_{PD}	Input pulldown resistance	To AGND	70	100	130	kΩ
TWO-LEVEL INPUTS (OCP)						
V_{L1}	Input mode 1 voltage (16A limit)	Tied to AGND	0		0.09*AVDD	V
V_{L2}	Input mode 2 voltage (24A limit)	22 kΩ ± 5% to AGND	0.12*AVDD	0.15*AVDD	0.55*AVDD	V
R_{PU}	Input pullup resistance	To AVDD	80	100	120	kΩ
R_{PD}	Input pulldown resistance	To AGND	80	100	120	kΩ
OPEN-DRAIN OUTPUTS (FAULTZ)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{PVDD} > 6 V, I_{OUT} = 1 A, T_A = 25°C		95	120	mΩ
		V_{PVDD} < 6 V, I_{OUT} = 1 A, T_A = 25°C		105	130	mΩ
		V_{PVDD} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		140	185	mΩ
		V_{PVDD} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		145	190	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{PVDD} = 24 V, SLEW pin tied to AGND	14	25	45	V/µs
		V_{PVDD} = 24 V, SLEW pin to Hi-Z	30	50	80	V/µs
		V_{PVDD} = 24 V, SLEW pin to 47 kΩ +/- 5% to AVDD	80	125	185	V/µs
		V_{PVDD} = 24 V, SLEW pin tied to AVDD	130	200	280	V/µs
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{PVDD} = 24 V, SLEW pin tied to AGND	14	25	45	V/µs
		V_{PVDD} = 24 V, SLEW pin to Hi-Z	30	50	80	V/µs
		V_{PVDD} = 24 V, SLEW pin to 47 kΩ +/- 5% to AVDD	80	125	185	V/µs
		V_{PVDD} = 24 V, SLEW pin tied to AVDD	110	200	280	V/µs
I_{LEAK}	Leakage current on OUTx	V_{OUTx} = V_{PVDD}, RESETZ = 1			5	mA
	Leakage current on OUTx	V_{OUTx} = 0 V, RESETZ = 1			1	µA

T_J = –40°C to +150°C, V_{PVDD} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DEAD}	Output dead time (high to low / low to high)	V_{PVDD} = 24 V, SR = 25 V/µs, HS driver OFF to LS driver ON and LS driver OFF to HS driver ON		1800	3400	ns
		V_{PVDD} = 24 V, SR = 50 V/µs, HS driver OFF to LS driver ON and LS driver OFF to HS driver ON		1100	1550	ns
		V_{PVDD} = 24 V, SR = 125 V/µs, HS driver OFF to LS driver ON and LS driver OFF to HS driver ON		650	1000	ns
		V_{PVDD} = 24 V, SR = 200 V/µs, HS driver OFF to LS driver ON and LS driver OFF to HS driver ON		500	750	ns
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	V_{PVDD} = 24 V, INHx/INLx = 1 to OUTx transition, SR = 25 V/µs		2000	4550	ns
		V_{PVDD} = 24 V, INHx/INLx = 1 to OUTx transition, SR = 50V/µs		1200	2150	ns
		V_{PVDD} = 24 V, INHx/INLx = 1 to OUTx transition, SR = 125 V/µs		800	1350	ns
		V_{PVDD} = 24 V, INHx/INLx = 1 to OUTx transition, SR = 200 V/µs		650	1050	ns
t_{MIN_PULSE}	Minimum output pulse width	SR = 200 V/µs	600			ns
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	PVDD rising	4.3	4.4	4.5	V
		PVDD falling	4.1	4.2	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	140	200	350	mV
t_{UVLO}	Supply undervoltage lockout deglitch time		3	5	7	µs
V_{CPUV}	Charge pump undervoltage lockout (above PVDD)	Supply rising	2.3	2.5	2.7	V
		Supply falling	2.2	2.4	2.6	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	75	100	140	mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	180	200	240	mV
I_{OCP}	Overcurrent protection trip point	OCP pin tied to AGND	10	16	22	A
I_{OCP}	Overcurrent protection trip point	OCP pin tied to 22 kΩ ±5% to AGND	15	24	30	A
t_{OCP}	Overcurrent protection deglitch time		0.06	0.3	0.6	µs
t_{RETRY}	Overcurrent protection retry time		4	5	6	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	135	145	155	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	15	20	26	°C
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	170	180	190	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)	15	20	25	°C
T_{TSD_FET}	Thermal shutdown temperature (FET)	Die temperature (T_J)	165	175	187	°C
$T_{TSD\_FET\_HYS}$	Thermal shutdown hysteresis (FET)	Die temperature (T_J)	18	25	30	°C

(1) R_{LBK} is resistance of inductor L_{BK}

5.6 Typical Characteristics

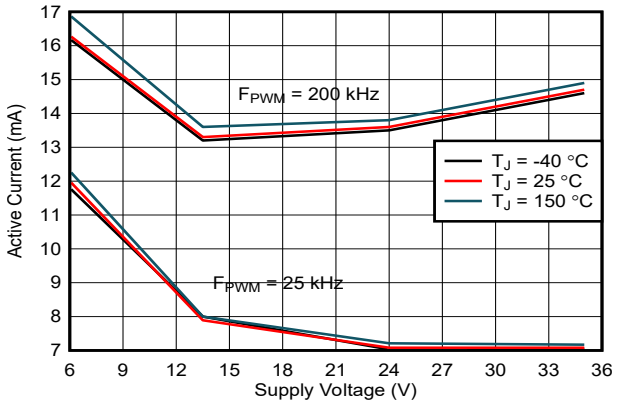

Figure 5-1. Supply current over supply voltage

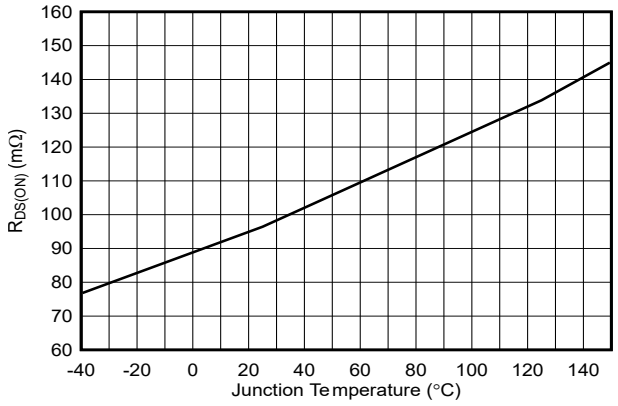

Figure 5-2. $R_{DS(ON)}$ (high and low side combined) for MOSFETs over temperature

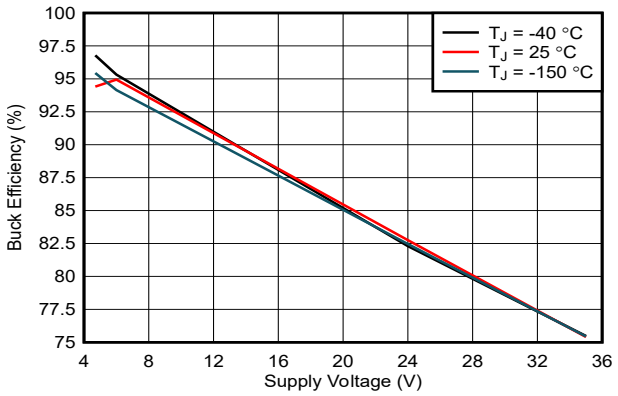

Figure 5-3. Buck regulator efficiency over supply voltage

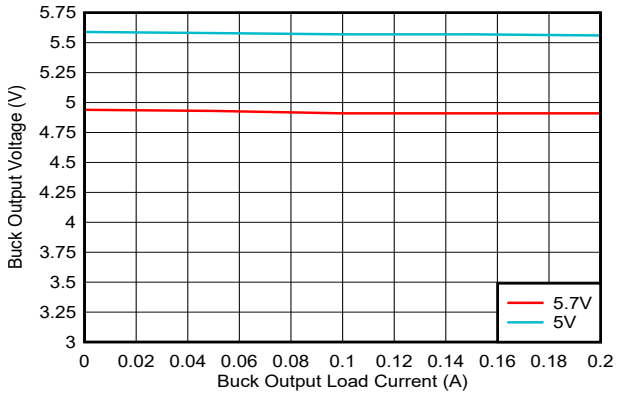

Figure 5-4. Buck regulator output voltage over load current

6 Detailed Description

6.1 Overview

The DRV2911-Q1 device is a one-channel differential piezo driver with integrated fault protection. The device reduces system footprint and complexity by integrating two half-bridge MOSFETs, gate drivers, charge pumps, and a linear regulator for driving the piezo-based Lens Cover System, LCS. A simple hardware interface allows for configuring the settings through fixed external resistors.

The architecture uses an internal state machine to protect against short-circuit events and control the slew rate of the internal power MOSFETs.

The DRV2911-Q1 provides a wide range of integrated protection features including power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD_UV), and overtemperature warning and shutdown (OTW and OTSD). Fault events are indicated by the FAULTZ pin, which can be tied to the ULC1001-Q1 controller device or host controller.

The DRV2911-Q1 device is available in 0.5mm pin pitch, VQFN surface-mount packages with wettable flanks. The VQFN package size is 7mm × 5mm.

6.2 Functional Block Diagram

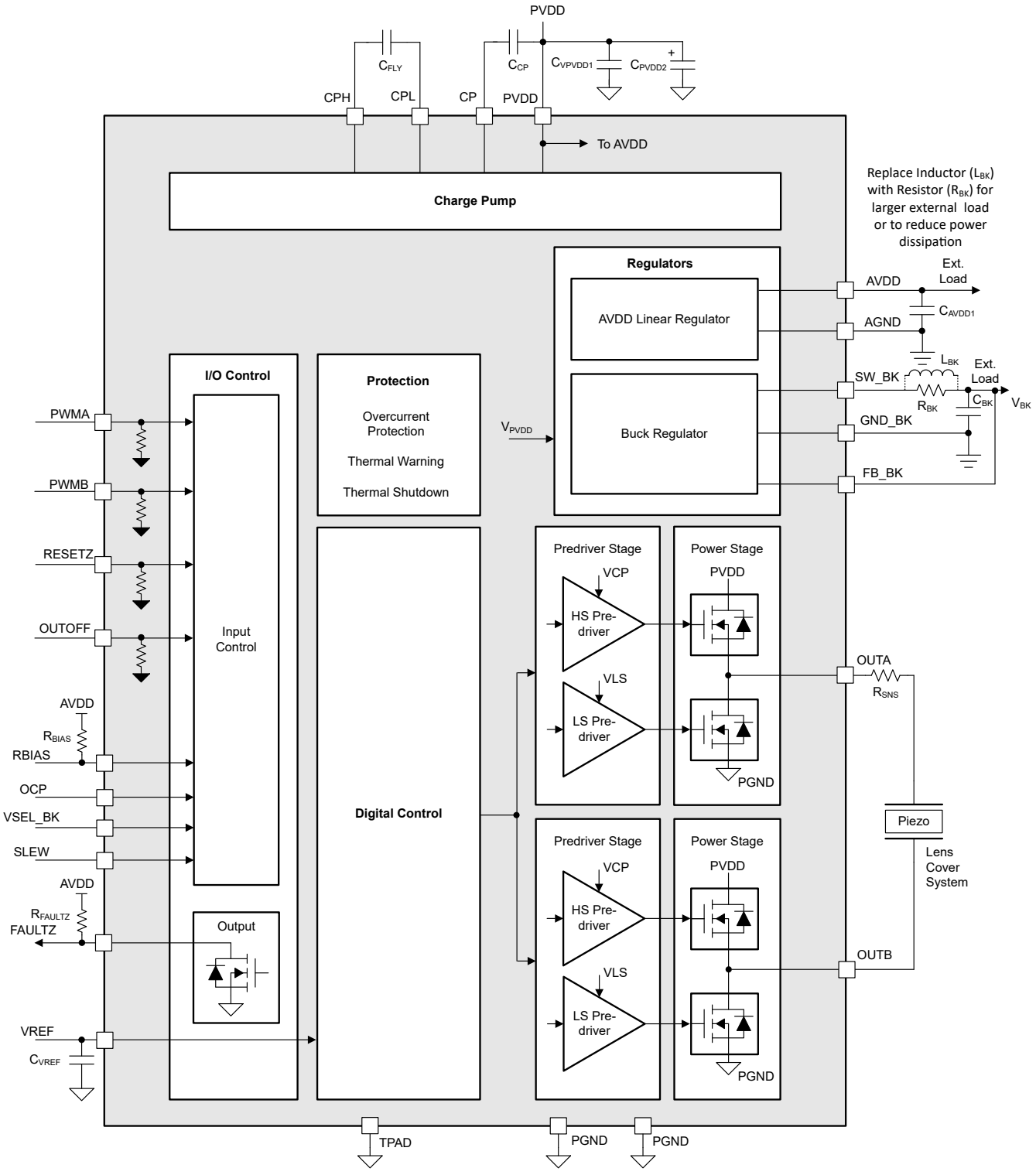

Figure 6-1. DRV2911-Q1 Block Diagram

6.3 Feature Description

Table 6-1 lists the recommended values of the external components for the driver.

Table 6-1. DRV2911-Q1 External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{PVDD1}	PVDD	PGND	X5R or X7R, 0.1-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{PVDD2}	PVDD	PGND	≥ 10-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	PVDD	X5R or X7R, 16-V, 1-µF
C_{FLY}	CPH	CPL	X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage
C_{AVDD}	AVDD	AGND	X5R or X7R, 1-µF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-µF to 1.3-µF at 3.3-V across operating temperature.
C_{VREF}	VREF	AGND	X5R or X7R, 0.1-µF, 6.3-V capacitor
R_{FAULTZ}	AVDD	FAULTZ	5.1-kΩ, Pullup resistor
R_{BIAS}	RBIAS	AVDD	47 kΩ, bias resistor
R_{SLEW}	SLEW	AGND or AVDD	Slew rate hardware interface
R_{OCP}	OCP	AGND	OCP hardware interface

Note

TI recommends connecting the pull-up on FAULTZ even if it is not used to avoid undesirable entry into internal test mode. If an external supply is used to pull up FAULTZ, ensure that it is pulled to >2.2V on power up or the device will enter internal test mode.

6.3.1 Output Stage

The DRV2911-Q1 device consists of an integrated 95mΩ (combined high-side and low-side FET's on-state resistance) NMOS FETs connected in two half-bridge configurations. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs. The device has three PVDD power-supply pins which are to be connected to the supply voltage.

6.3.2 Hardware Interface

The hardware interface contains three configurable pins SLEW, OCP, and VSEL_BK for controlling the driver output slew rate, over current protection level, and buck voltage, respectively. These pins allow the application designer to configure the device settings by tying each pin to logic high, logic low, floating, or pull-up to logic high with a suitable resistor. The hardware interface also contains the FAULTZ open-drain pin for reporting a driver fault.

- The SLEW pin configures the slew rate of the output voltage.
- The OCP pin is used to configure the over-current protection level.
- The VSEL_BK pin is used to configure the buck output voltage level.
- The FAULTZ pin is used to report driver faults and can be read over I^2C from the ULC controller.

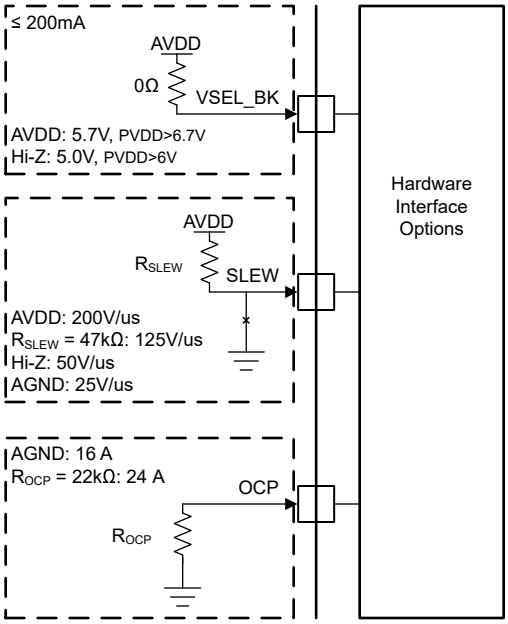

Figure 6-2. DRV2911-Q1 Hardware Interface

Figure 6-3 shows the structure of the four-level input pin, SLEW. The OCP and VSEL_BK pins utilize the same internal structure but only have two valid configurations.

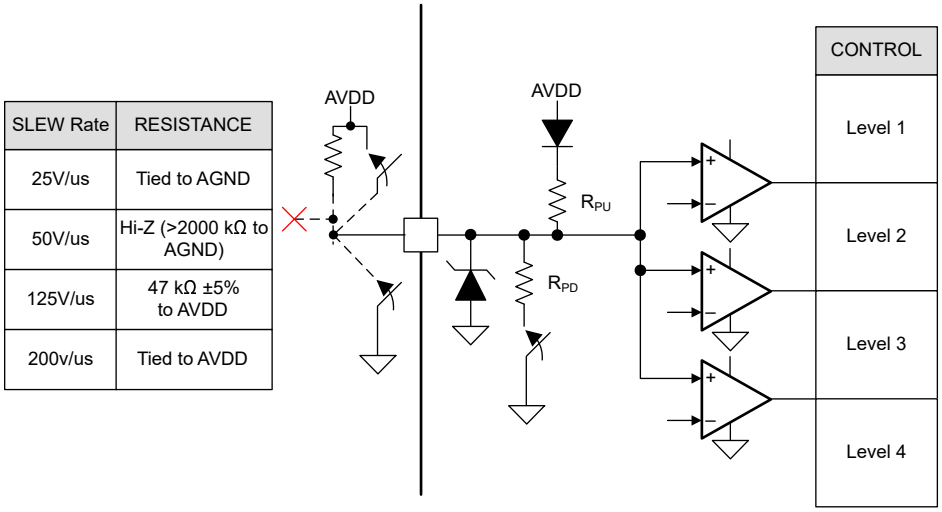

Figure 6-3. SLEW Input Pin Structure

Figure 6-4 shows the input structure for the logic level pins, OUTOFF, PWMx, and RESETZ. The input can be with a voltage or external resistor. It is recommended to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

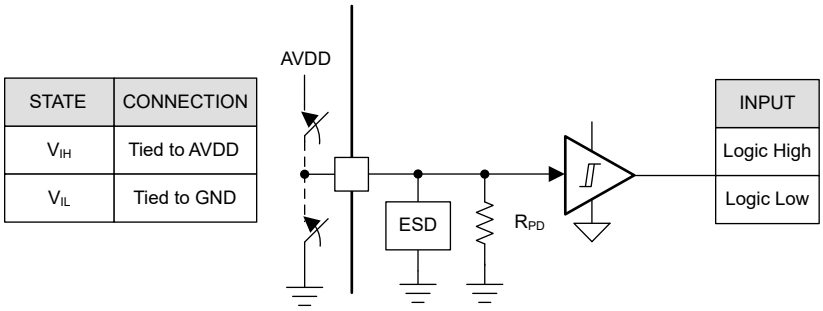

Figure 6-4. Logic-Level Input Pin Structure

Figure 6-5 shows the structure of the open-drain output FAULTZ. The open-drain output requires an external pullup resistor to function properly.

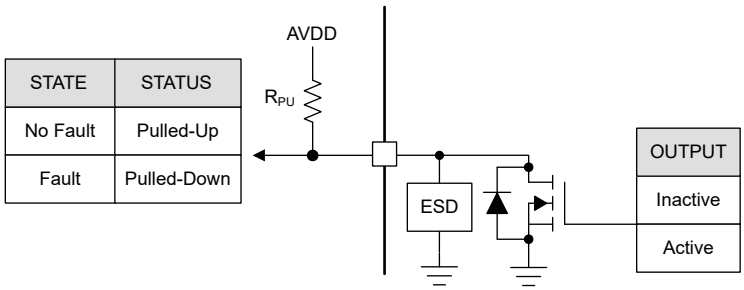

Figure 6-5. Open Drain

6.3.3 AVDD Linear Voltage Regulator

A 3.3V linear regulator is integrated into the DRV2911-Q1 family of devices and is available for use by external circuitry. The AVDD regulator is used for powering up the internal digital circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 30mA). The output of the AVDD regulator should be bypassed near the AVDD pin with an X5R or X7R, 1µF, 6.3V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3V.

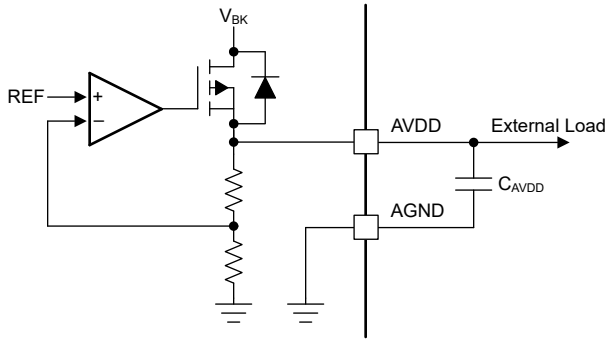

Figure 6-6. AVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device by the AVDD linear regulator based on V_{BK}.

$$\mathrm{P} = (V_{BK} - AVDD) \times I_{AVDD} \quad (1)$$

For example, at a V_{BK} of 30V, drawing 20mA out of AVDD results in power dissipation as shown in Equation 2.

$$P = (5V - 3.3V) \times 10\mathrm{mA} = 17mW \quad (2)$$

6.3.4 Step-Down Mixed-Mode Buck Regulator

The DRV2911-Q1 has an integrated mixed-mode buck regulator to supply regulated 5.0V power for an external controller or system voltage rail. The buck output can also be configured to 5.7V to support the extra headroom for external LDO for generating up to 5.0V. The output voltage of the buck is set by the VSEL_BK pin.

The buck regulator has a low quiescent current of ~1-2mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

Note

The buck regulator components L_{BK}/R_{BK} and C_{BK} must be connected. Internally, the buck powers the 3.3V AVDD supply.

Table 6-2. Recommended Settings for Buck Regulator

Buck Mode	Buck output voltage	Max output current from AVDD (I_{AVDD})	Max output current from Buck (I_{BK})	Buck current limit
Inductor - 47µH	5.0V or 5.7V	30mA	200mA - I_{AVDD}	600mA
Inductor - 22µH	5.0V or 5.7V	30mA	50mA	150mA
Resistor - 22Ω	5.0V or 5.7V	30mA	40mA	150mA

6.3.4.1 Buck in Inductor Mode

The buck regulator in DRV2911-Q1 device is primarily designed to support low inductance of 47µH and 22µH inductors. The 47µH inductor allows the buck regulator to operate up to 200mA load current support, whereas the 22µH inductor limits the load current to 50mA.

Figure 6-7 shows the connection of buck regulator in inductor mode.

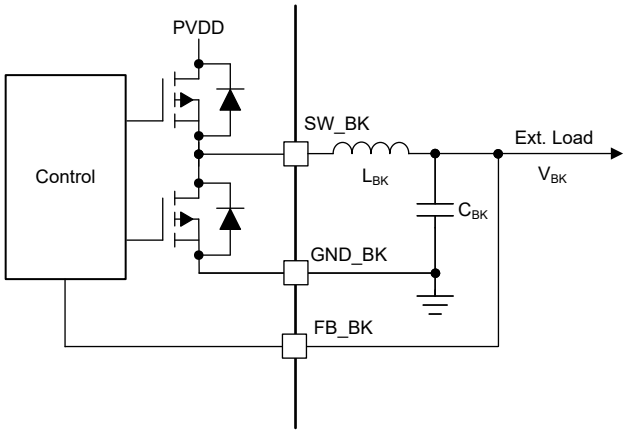

Figure 6-7. Buck (Inductor Mode)

6.3.4.2 Buck in Resistor mode

If the external load requirements is less than 40mA, the inductor can be replaced with a resistor. In resistor mode, the power is dissipated across the external resistor and the efficiency is lower than a buck in inductor mode. To appropriately scale the resistor, use the following equations. The ULC1001-Q1 max current consumption is approximately 10mA, I_{ULC}. Using DRV2911-Q1 internal current, I_{DRV_INT}, consumption assumed to be 10mA, PVDD equal to 25V, and buck voltage equal to 5V, the buck resistor should be rated higher than 400mW. When choosing a resistor rating, consider the layout's ambient temperature range and overall thermal dissipation.

$$P_{STANDBY} = V_{PVDD} \times (I_{ULC} + I_{DRV\_INT}) \quad (3)$$

$$P_{BK\_RES} = P_{STANDBY} - (V_{BUCK} \times I_{ULC + DRV\_INT}) \quad (4)$$

Figure 6-8 shows the connection of buck regulator in resistor mode.

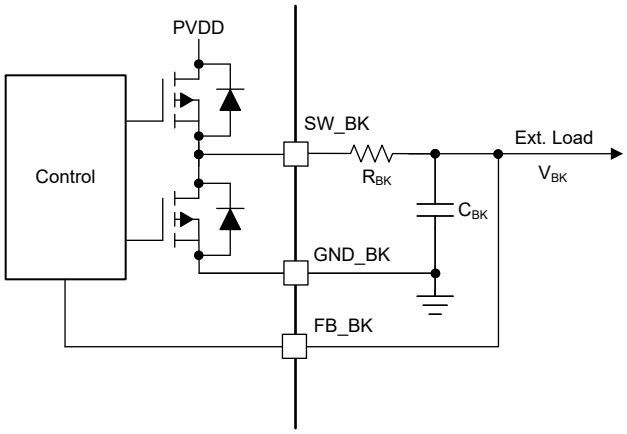

Figure 6-8. Buck (Resistor Mode)

6.3.4.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to be fed to external LDO to generate standard 3.3V or 5.0V output rail with higher accuracies. The buck output voltage should be configured to 5V or 5.7V to provide extra headroom to support the external LDO for generating 3.3V or 5V rail as shown in Figure 6-9.

This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

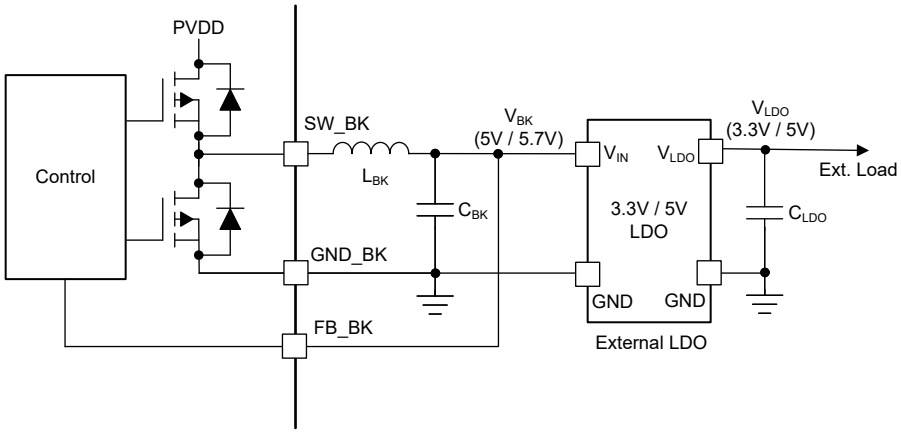

Figure 6-9. Buck Regulator with External LDO

6.3.4.4 AVDD Power Sequencing with Buck Regulator

The AVDD LDO has uses the power supply from the mixed mode buck regulator to reduce power dissipation internally. The LDO power supply from DC mains (PVDD) to buck output (VBK) are shown in Figure 6-10.

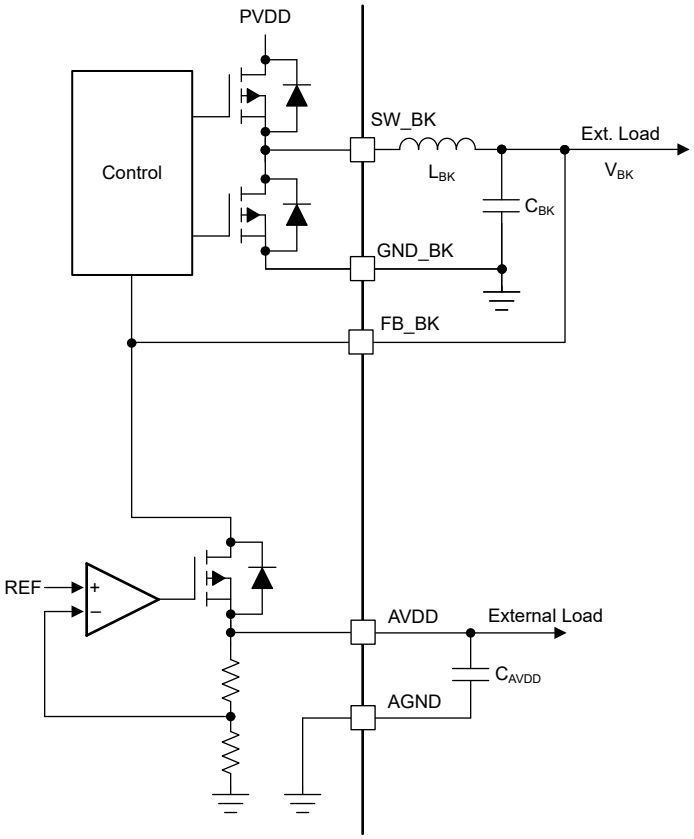

Figure 6-10. AVDD Power Sequencing on mixed mode Buck Regulator

6.3.4.5 Mixed mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage (V_{BK_REF}) which is internally generated depending on the buck-output voltage setting (BUCK_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ($V_{BK} < V_{BK\_REF}$) or low ($V_{BK} > V_{BK\_REF}$), the high-side power FET of the buck turns on and turns off respectively. An independent current control loop monitors the current in high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL}). This implements a current limit control for the buck regulator. Figure 6-11 shows the architecture of the buck and various control/protection loops.

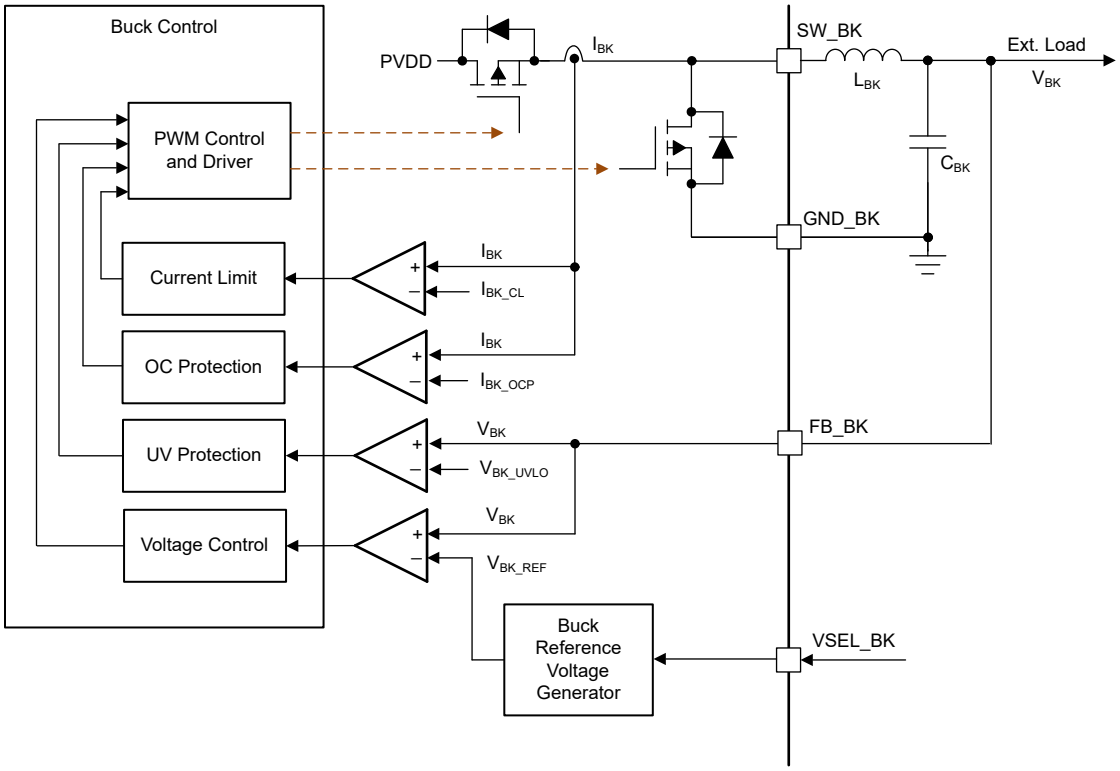

Figure 6-11. Buck Operation and Control Loops

6.3.4.6 Buck Undervoltage Lockout

If the input supply voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, all of both high-side and low-side MOSFETs of the buck regulator are disabled and the FAULTZ pin is driven low. Normal operation starts again (buck operation and the FAULTZ pin is released) when the VBK undervoltage condition clears.

6.3.4.7 Buck Overcurrent Protection

A buck overcurrent event is sensed by monitoring the current flowing through the buck regulator's FETs. If the current across the buck regulator FET exceeds the I_{BK_OCP} threshold for longer than the t_{BK_OCP} deglitch time, an OCP event is recognized. The buck OCP mode is configured in the automatic retry setting. In this setting, after a buck OCP event is detected, all the buck regulator's FETs are disabled and the FAULTZ pin is driven low. Normal operation starts again automatically (driver operation and the FAULTZ pin are released) after the t_{BK_RETRY} time elapses.

6.3.5 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the PVDD power supply to enhance the high-side FETs fully. The DRV2911-Q1 integrates a charge-pump circuit that generates a voltage above the PVDD supply for this purpose.

The charge pump requires two external capacitors for operation. See Figure 6-1, Section 4 and Section 6.3 for details on these capacitors.

The charge pump shuts down when RESETZ is low.

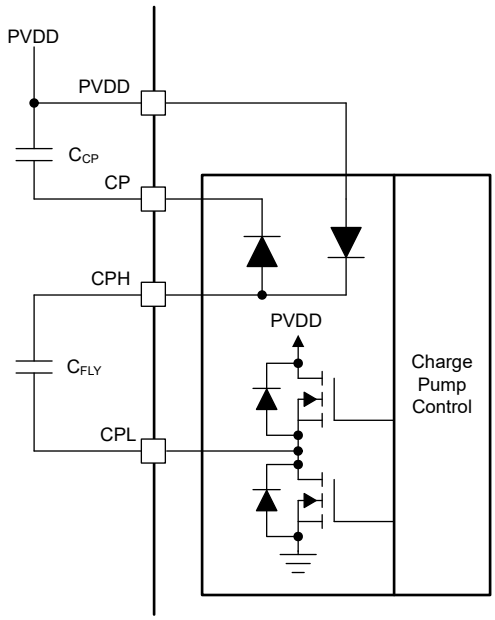

Figure 6-12. DRV2911-Q1 Charge Pump

6.3.6 Slew Rate Control

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in Figure 6-13.

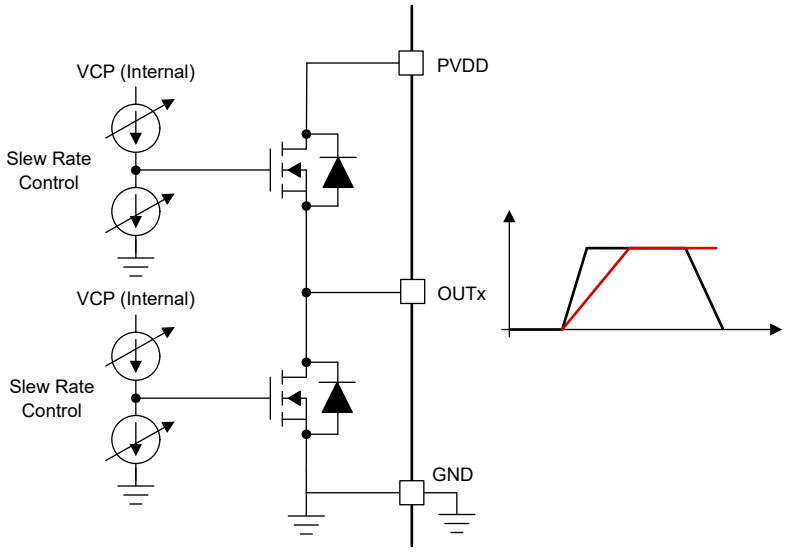

Figure 6-13. Slew Rate Circuit Implementation

The slew rate can be adjusted by the SLEW pin by following Figure 6-2. Four slew rate settings are available: 25V/µs, 50V/µs, 125V/µs or 200V/µs. The slew rate is calculated by the rise time and fall time of the voltage on the OUTx pin as shown in Figure 6-14.

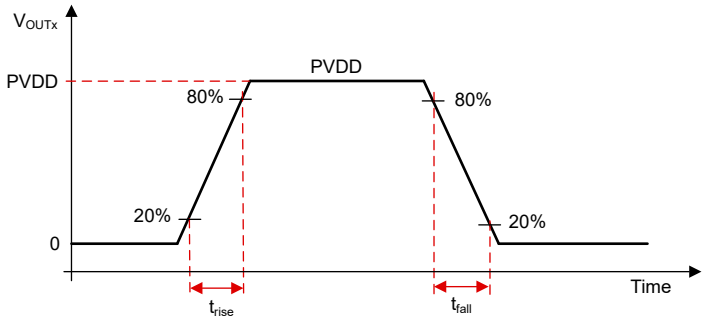

Figure 6-14. Slew Rate Timings

6.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross-conduction of MOSFETs - during the switching of high-side and low-side MOSFETs, DRV2911-Q1 avoids shoot-through events by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that the VGS of the high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of the same half-bridge (or vice-versa) as shown in Figure 6-15 and Figure 6-16.

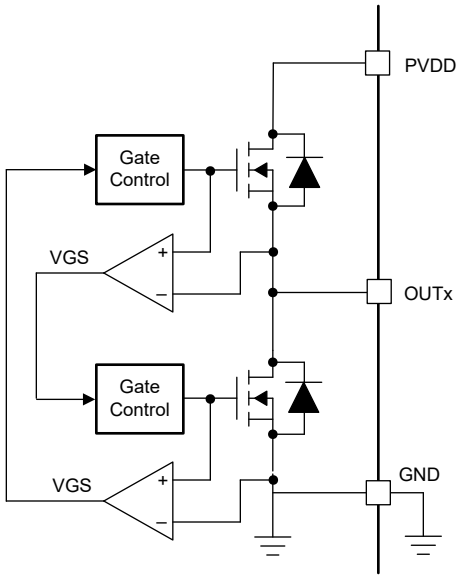

Figure 6-15. Cross Conduction Protection

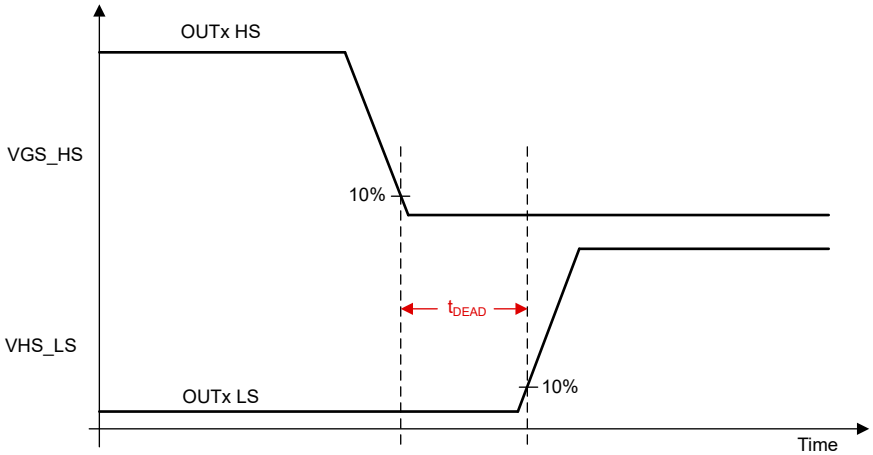

Figure 6-16. Dead Time

6.3.8 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage. This time has three parts consisting of the digital input deglitcher delay, analog driver, and comparator delay.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes, a small digital delay is added as the input command propagates through the device.

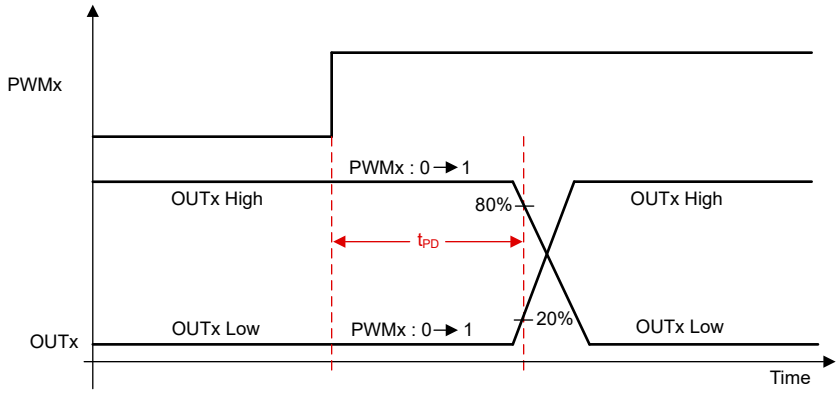

Figure 6-17. Propagation Delay

6.3.9 Protections

The DRV2911-Q1 family of devices is protected against PVDD undervoltage, charge pump undervoltage, and overcurrent events. The following sections summarize various fault details.

6.3.9.1 PVDD Supply Undervoltage Lockout

If at any time the input supply voltage on the PVDD pin falls lower than the V_{UVLO} threshold (PVDD UVLO falling threshold), all of the integrated FETs, driver charge-pump, and digital logic controller are disabled as shown in Figure 6-18. Normal operation resumes (driver operation) when the PVDD undervoltage condition is removed.

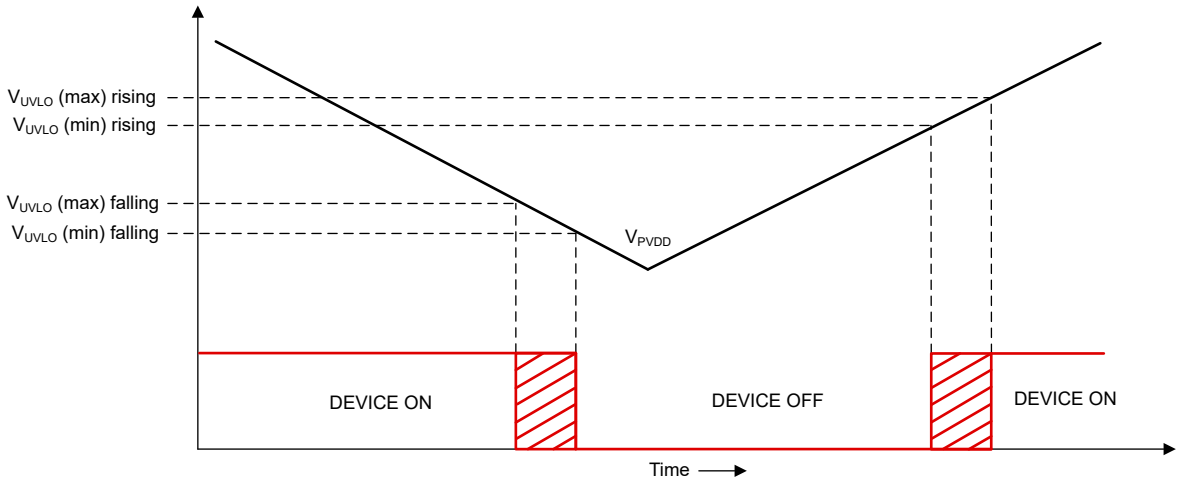

Figure 6-18. PVDD Supply Undervoltage Lockout

6.3.9.2 AVDD Undervoltage Lockout

If at any time the voltage on the AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge pumps, and digital logic controller are disabled. Normal operation resumes (driver operation) when the AVDD undervoltage condition is removed.

6.3.9.3 VCP Charge Pump Undervoltage Lockout

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the FAULTZ pin is driven low. Normal operation starts again (driver operation and the FAULTZ pin are released) when the VCP undervoltage condition clears.

6.3.9.4 Overcurrent Latched Protection

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and the output enters a latched shutdown state. The I_{OCP} threshold is set via OCP/SR pin, and the t_{OCP_DEG} is 0.6µs.

After an OCP event in this mode, all MOSFETs are disabled and the FAULTZ pin is driven low. Normal driver operation starts again and the FAULTZ pin is released when the OCP condition is cleared. Clear the OCP condition by toggling the RESETZ pin for the reset pulse (t_{RST}).

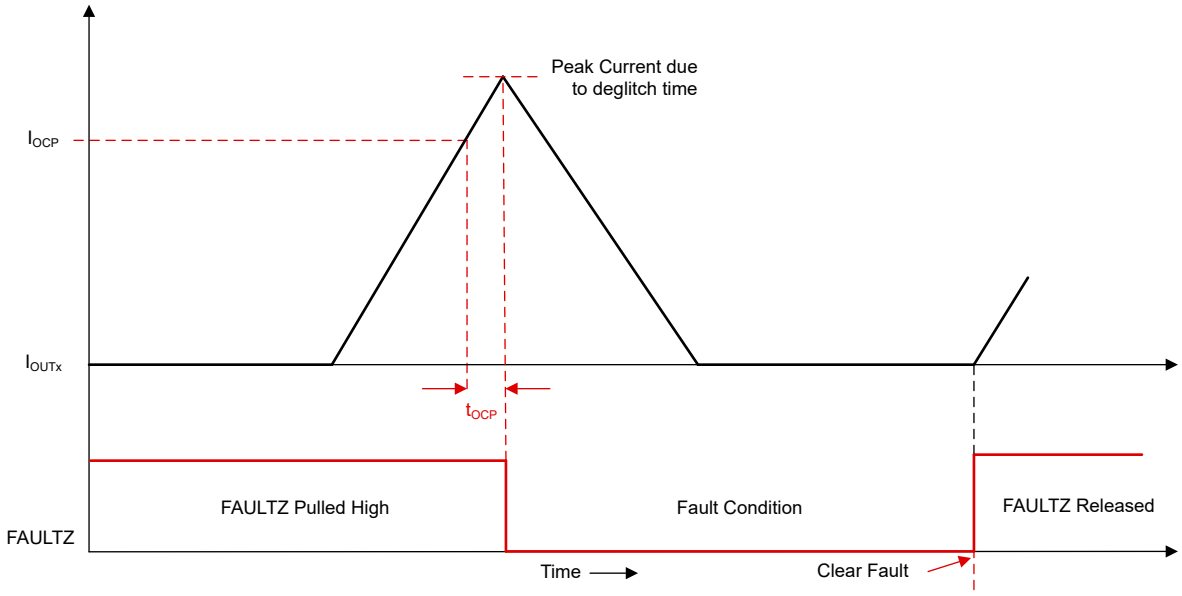

Figure 6-19. Overcurrent Protection - Latched Shutdown Mode

6.3.9.5 Thermal Shutdown (OTSD)

DRV2911-Q1 has 2 die temperature sensors for thermal shutdown, one near the FETs and one in another part of the die.

6.3.9.5.1 OTSD FET

If the die temperature near FET exceeds the trip point of the thermal shutdown limit (T_{TSD_FET}), all the FETs are disabled, the charge pump is shut down, and the FAULTZ pin is driven low. Normal operation starts again (driver operation and the FAULTZ pin is released) when the over temperature condition clears. This protection feature cannot be disabled.

6.3.9.5.2 OTSD (Non-FET)

If the die temperature in the device exceeds the trip point of the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the charge pump is shut down, and the FAULTZ pin is driven low. Normal operation starts again (driver operation and the FAULTZ pin is released) when the over temperature condition clears. This protection feature cannot be disabled.

6.4 Device Functional Modes

6.4.1 Functional Modes

6.4.1.1 Reset Mode

The RESETZ pin manages the state of the DRV2911-Q1. When the RESETZ pin is low, the device goes to a low-power sleep mode. In sleep mode, the output stage, charge pump, and AVDD are disabled. The t_{SLEEP} time must elapse after a falling edge on the RESETZ pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the RESETZ pin is pulled high. The t_{WAKE} time must elapse before the device is ready for input.

In sleep mode and when $V_{PVDD} < V_{UVLO}$, all MOSFETs are disabled.

Note

During power up and power down of the device through the RESETZ pin, the FAULTZ pin is held low as the internal regulators are enabled or disabled. After the regulators are enabled or disabled, the FAULTZ pin is automatically released. The duration that the FAULTZ pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

Note

TI recommends connecting the pull up on FAULTZ even if it is not used to avoid undesirable entry into internal test mode. If an external supply is used to pull up FAULTZ, ensure that it is pulled to >2.2V on power up or the device will enter internal test mode.

6.4.1.2 Operating Mode

When the RESETZ pin is high and the V_{PVDD} voltage is greater than the V_{UVLO} voltage, the device goes into operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump and AVDD regulator are active.

6.4.1.3 Fault Reset (RESETZ Pulse)

In the case of device latched faults, the DRV2911-Q1 goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by sending a reset pulse to the RESETZ pin. The RESETZ reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the RESETZ pin. The low period of the sequence should fall within the t_{RST} time window or else the device will start the complete shutdown sequence (low power sleep mode). The reset pulse has no effect on any of the regulators, or other functional blocks.

6.4.2 OUTOFF functionality

DRV2911-Q1 can disable pre-driver and MOSFETs bypassing the digital through the OUTOFF pin. When the OUTOFF pin is pulled high, the output FETs are disabled. If RESETZ is high when the OUTOFF pin is high, the charge pump and AVDD regulator are active and any driver-related faults such as OCP will be inactive. OUTOFF pin independently disables the output FETs irrespective of the status of PWMx input pins.

Note

Since the OUTOFF pin independently disables MOSFET, it can trigger fault conditions resulting in FAULTZ getting pulled low.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

DRV2911-Q1 is the driver in a two-chip Ultrasonic Lens Cleaning system or ULC system. When paired with the ULC1001-Q1 controller device, DRV2911-Q1 is capable of receiving PWM inputs and driving cleaning sequences to piezo-based Lens Cover Systems, LCS. The output signal to the LCS may be boosted to a higher voltage using an LC filter as shown in Figure 7-1.

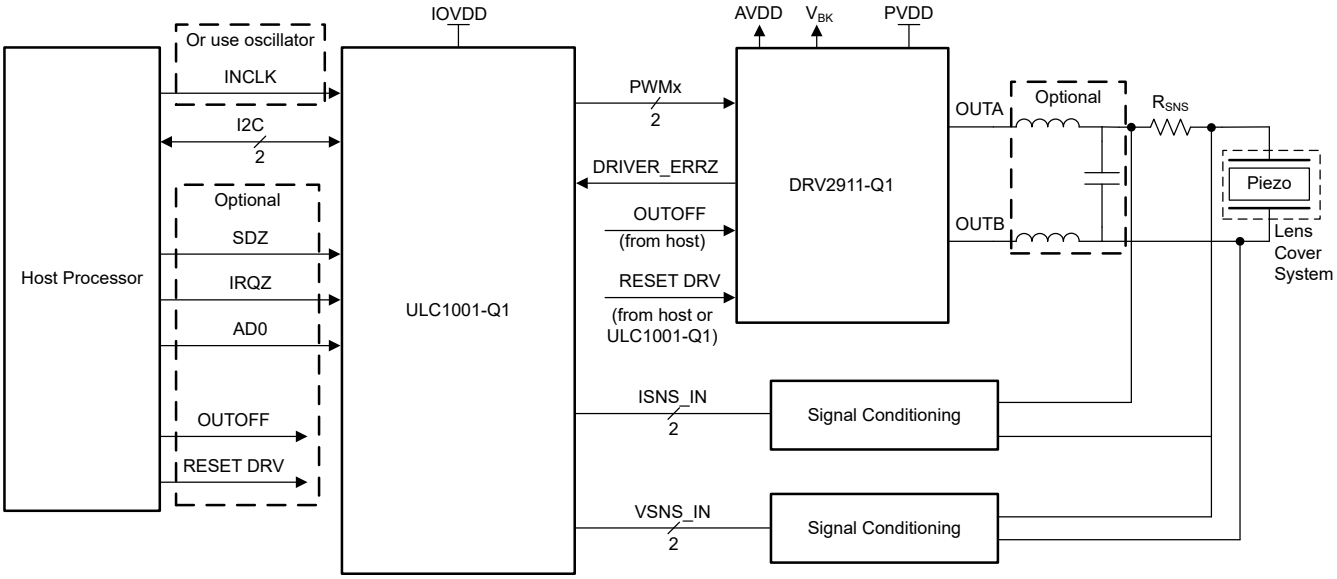

Figure 7-1. Ultrasonic Lens Cleaning Application Block Diagram

7.2 Typical Applications

Figure 7-2 shows an example schematic for an Ultrasonic Lens Cleaning application. The following design procedure outlines the setup process for DRV2911-Q1.

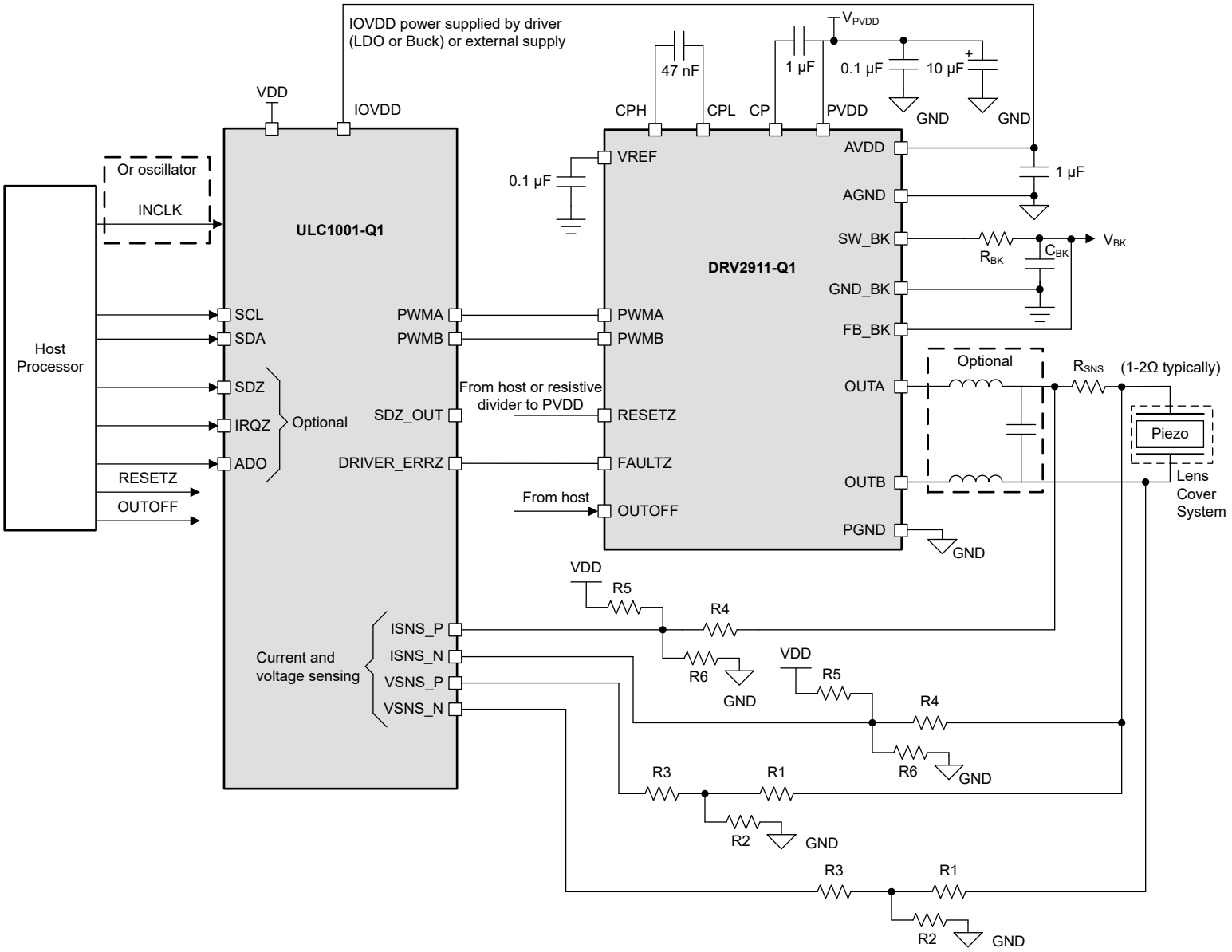

Figure 7-2. Ultrasonic Lens Cleaning Schematic

7.2.1 Design Procedure

The typical ULC application utilizes the host processor for configuring the ULC1001-Q1 controller, which subsequently drives a PWM signal to the DRV2911-Q1. The DRV2911-Q1 output may be passed through an LC filter before driving the piezo-based LCS. A sense resistor is placed in line with the OUTA driver output and has current sense connections on either side that route back to the controller device. Additionally, voltage sense connections across the LCS are routed to the controller.

When powering ULC1001-Q1 using the AVDD pin of DRV2911-Q1, the host processor must be used to control the DRV2911-Q1 RESETZ pin. Alternatively, RESETZ can be set high by using a resistive divider to PVDD. In the low-power reset mode (RESETZ = low), AVDD is disabled and powers down ULC1001-Q1.

When using an independent supply for ULC1001-Q1, the SDZ_OUT pin can be connected to RESETZ to control the DRV2911-Q1 functional mode using the ULC_TX_mode_cfg2 register. Additional DRV2911-Q1 hardware interface pin settings for SLEW and OCP are outlined in Hardware Interface and vary based on the system design.

Table 6-1 outlines recommendations for passive components shown in the schematic, Figure 7-2.

Lastly, the resistor values for R1 through R6 should be set based on the current and voltage levels required to drive the LCS. Refer to the next section Section 7.2.2 for details. R5 is pulled high to the VDD supply (1.8V) from ULC1001-Q1.

7.2.2 Voltage and Current Sense Circuitry

Each input into the ULC1001-Q1 current and voltage sense amplifiers require a voltage divider to decrease the high voltage across the transducer from 0V to 0.9V. The circuit representation of the current and voltage sense amplifiers is shown in Figure 7-3, where the items in I-sense Amp and V-sense Amp are internal to ULC1001-Q1. The resistors used in the voltage dividers must have a 0.1% tolerance to achieve high accuracy for power measurements. Three scale factors, USER_Params_ohms_sf_Q22, USER_Params_watts_sf_Q18, and USER_Params_Imag_max_sf_Q27, are used to convert the measured values into power, impedance, and current values, respectively. Use the below equation to determine the scale factors and the current and voltage sense amplifier gains. Table 7-1 containing typical resistor values for common voltage levels.

Note

The equivalent resistance between VDD and GND must be ≥ 4kΩ. R_F is fixed to 84kΩ.

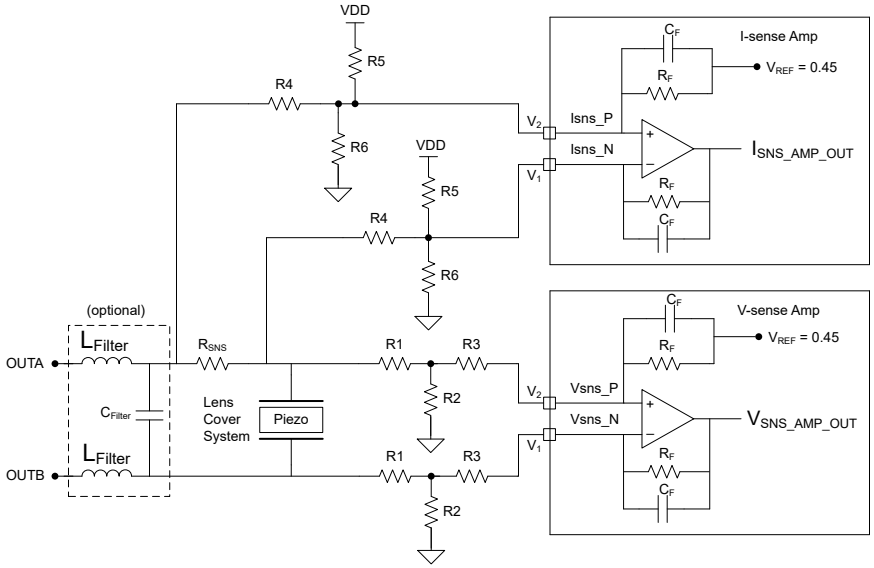

Figure 7-3. Voltage and Current Sense Amplifiers

$$\text{USER\_Params\_ohms\_sf\_Q22} = \frac{\text{ISNS}_{\text{GAIN}}}{\text{VSNS}_{\text{GAIN}}} \tag{5}$$

$$\text{USER\_Params\_watts\_sf\_Q18} = \frac{1}{\text{VSNS}_{\text{GAIN}}} \times \frac{1}{\text{ISNS}_{\text{GAIN}}} \times 0.2025 \tag{6}$$

$$\text{USER\_Params\_Imag\_max\_sf\_Q27} = \frac{0.9}{\text{ISNS}_{GAIN}} \tag{7}$$

$$\text{ISNS}_{\text{GAIN}}\left(\frac{V}{A}\right) = \frac{\text{R}_\text{f} \times R_{SNS}}{\text{R}_4} \tag{8}$$

$$\text{VSNS}_{\text{GAIN}}\left(\frac{V}{V}\right) = 1.043 \times \frac{\text{R}_\text{f}}{\text{R}_1 \times \text{R}_3 \times \left(\frac{1}{\text{R}_1} + \frac{1}{\text{R}_2} + \frac{1}{\text{R}_3}\right)} \tag{9}$$

Table 7-1. Voltage and Current Sense Resistor Reference Values

R5 = 6kΩ. R6 = 2kΩ

Differential Voltage (pk-pk)	R1	R2	R3	R4
460	1.3MΩ	6.34kΩ	294kΩ	422kΩ
90	360kΩ	30kΩ	1MΩ	150kΩ

Table 7-1. Voltage and Current Sense Resistor Reference Values (continued)

R5 = 6kΩ. R6 = 2kΩ

Differential Voltage (pk-pk)	R1	R2	R3	R4
40	150kΩ	30kΩ	1MΩ	150kΩ

7.3 Power Supply Recommendations

7.3.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in optimal driver performance. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and load
- The acceptable voltage ripple

The inductance between the power supply and the drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands with a change in voltage. When adequate bulk capacitance is used, the output voltage remains stable, and a high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

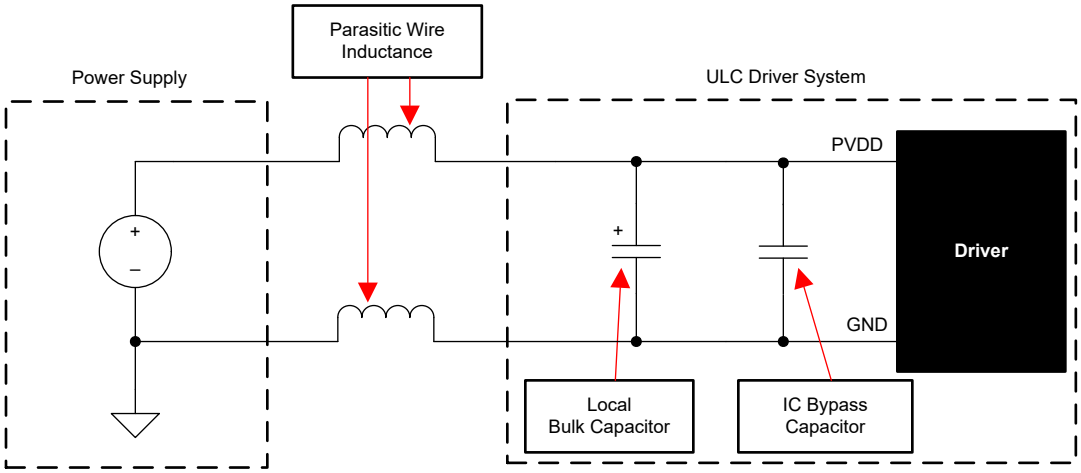

Figure 7-4. Example Setup of ULC Driver System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for optimal driver performance.

7.4 Layout

7.4.1 Layout Guidelines

The bulk capacitors should be placed to minimize the distance of the path to the driver. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high instantaneous current.

Small-value capacitors such as the charge pump, AVDD, and VREF capacitors should be ceramic and placed close to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the power loss that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW_BK and FB_BK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BK trace as much as possible to allow for faster load switching.

Figure 7-5 shows a layout example for the DRV2911-Q1.

7.4.2 Layout Example

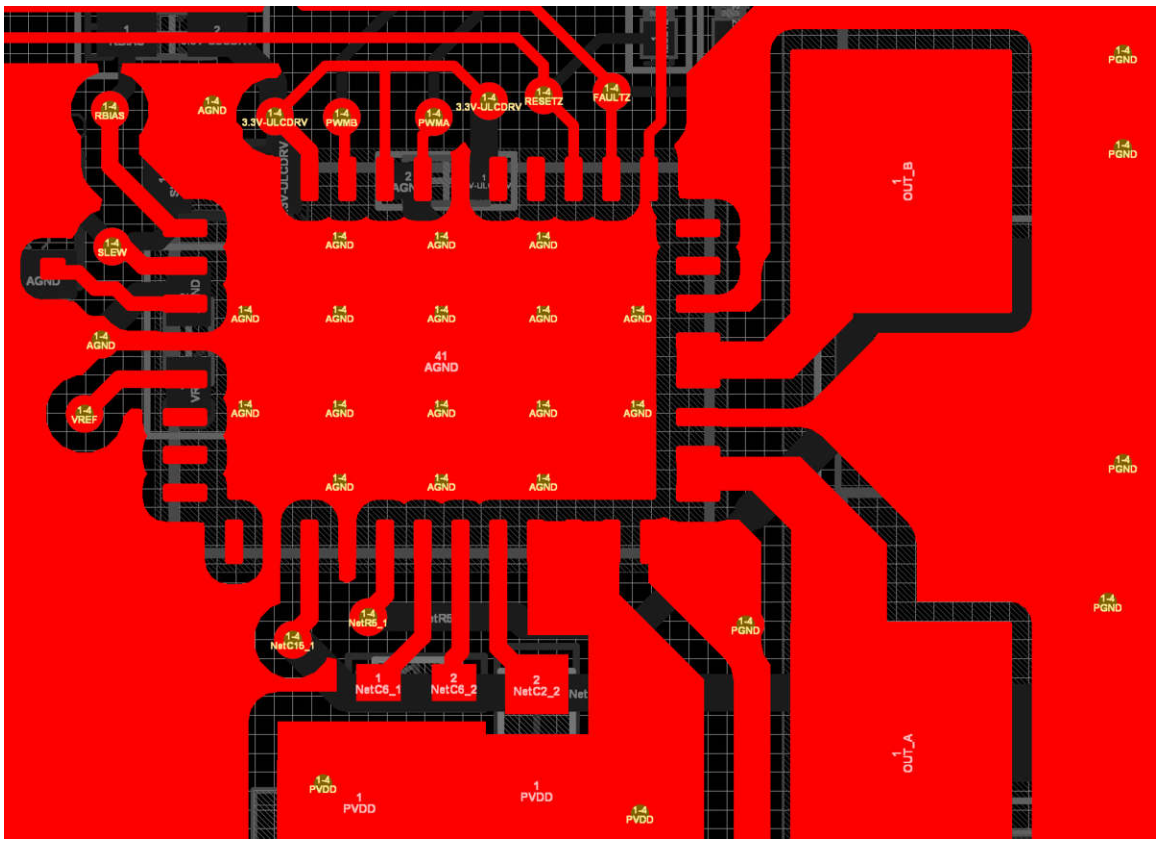

Figure 7-5. Recommended Layout Example for VQFN Package

7.4.3 Thermal Considerations

The DRV2911-Q1 has thermal shutdown (TSD) as previously described. A die temperature above 165°C (min.) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

7.4.3.1 Power Dissipation

The power loss in DRV2911-Q1 include standby power losses, LDO power losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation in DRV2911-Q1. The total device dissipation is the power dissipated in each of the two half bridges added together. The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking. Note that RDS,ON increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when designing the PCB and heatsinking.

A summary of equations for calculating each loss is shown in Table 7-2.

Table 7-2. DRV2911-Q1 Power Loss Approximations

Loss type	Approximate Power Loss Calculation
Standby power	$P_{standby} = V_{PVDD} \times I_{PVDD\_TA}$
LDO	$P_{LDO} = (V_{PVDD}-V_{AVDD}) \times I_{AVDD}$
FET conduction	$P_{CON} = 2 \times (I_{PK})^2 \times R_{ds,on(TA)}$
FET switching	$P_{SW} = I_{PK} \times V_{PVDD} \times t_{rise/fall} \times f_{PWM}$
Diode	$P_{diode} = 2 \times I_{PK} \times V_{F(diode)} \times t_{DEADTIME} \times f_{PWM}$

8 Device and Documentation Support

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- *EVM page ULC1001-DRV2911-EVM*
- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision * (June 2024) to Revision A (July 2025)	Page
• Changed pin 32 from: AVDD to: AGND in the *Pin Configuration and Functions*	3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV2911QRGFRQ1	Active	Production	VQFN (RGF) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	D2911Q1
DRV2911QRGFRQ1.A	Active	Production	VQFN (RGF) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	D2911Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

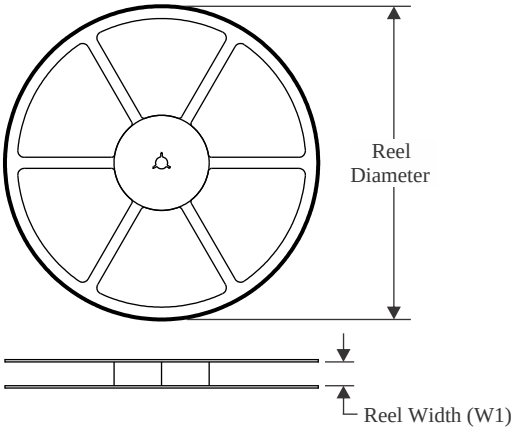
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

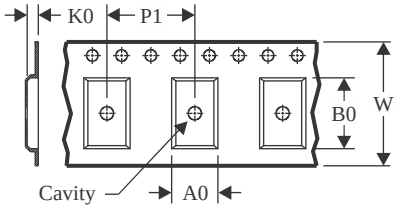
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

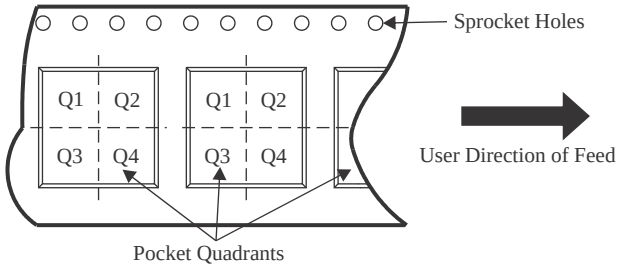


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

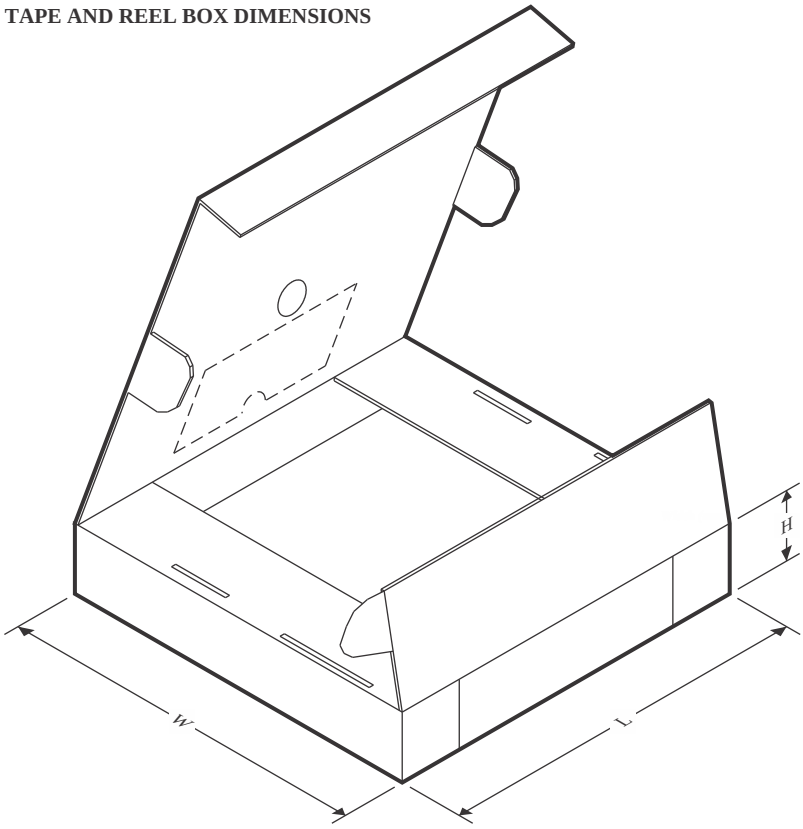
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2911QRGFRQ1	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2911QRGFRQ1	VQFN	RGF	40	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

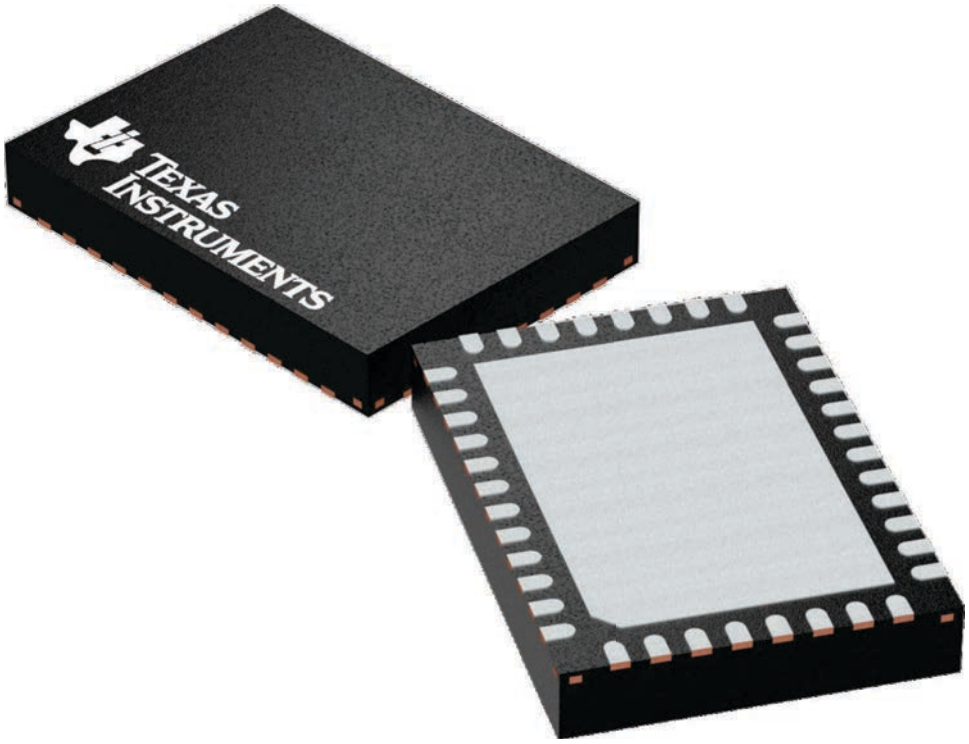
RGF 40

VQFN - 1 mm max height

5 x 7, 0.5 mm pitch

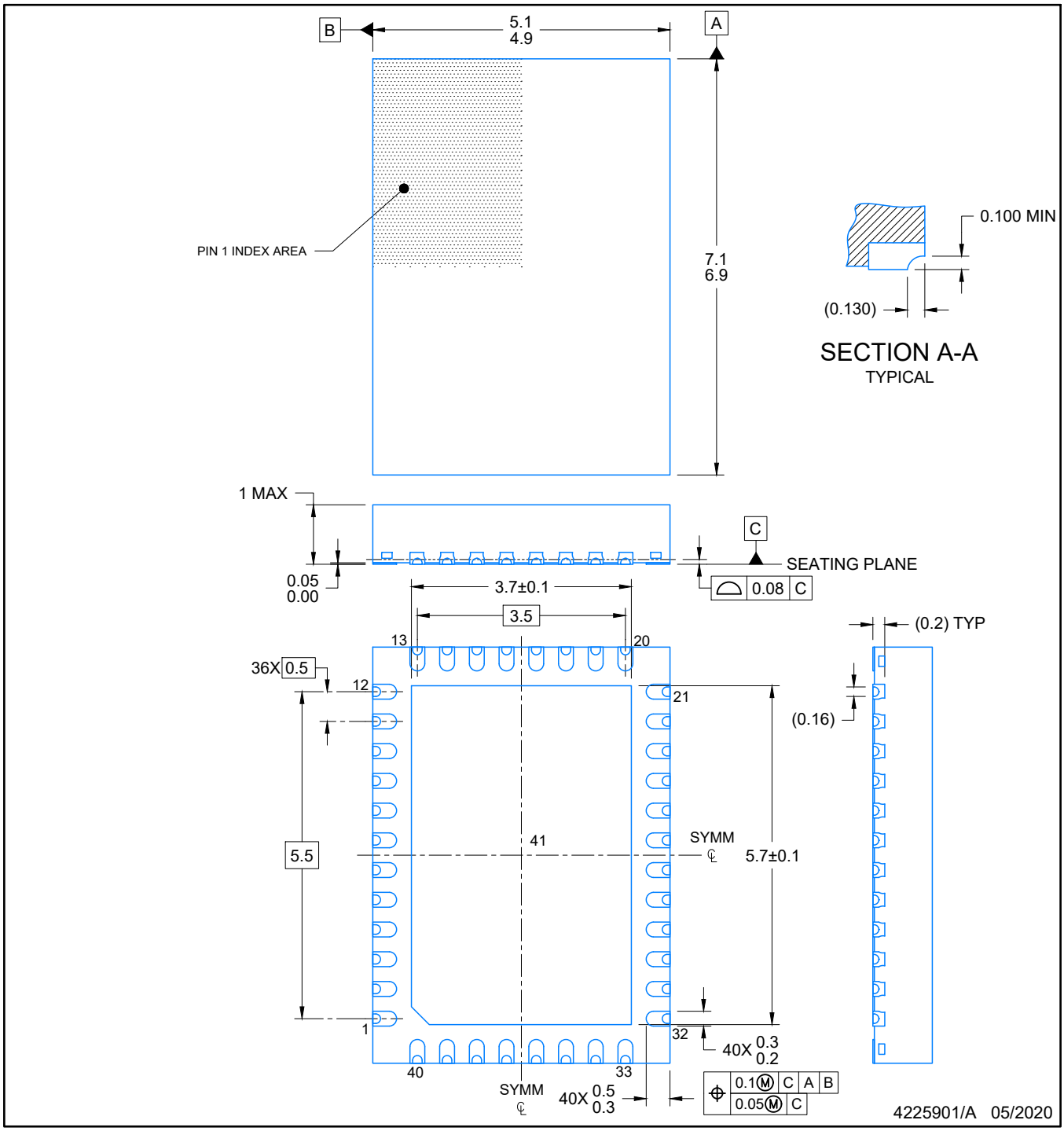
PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



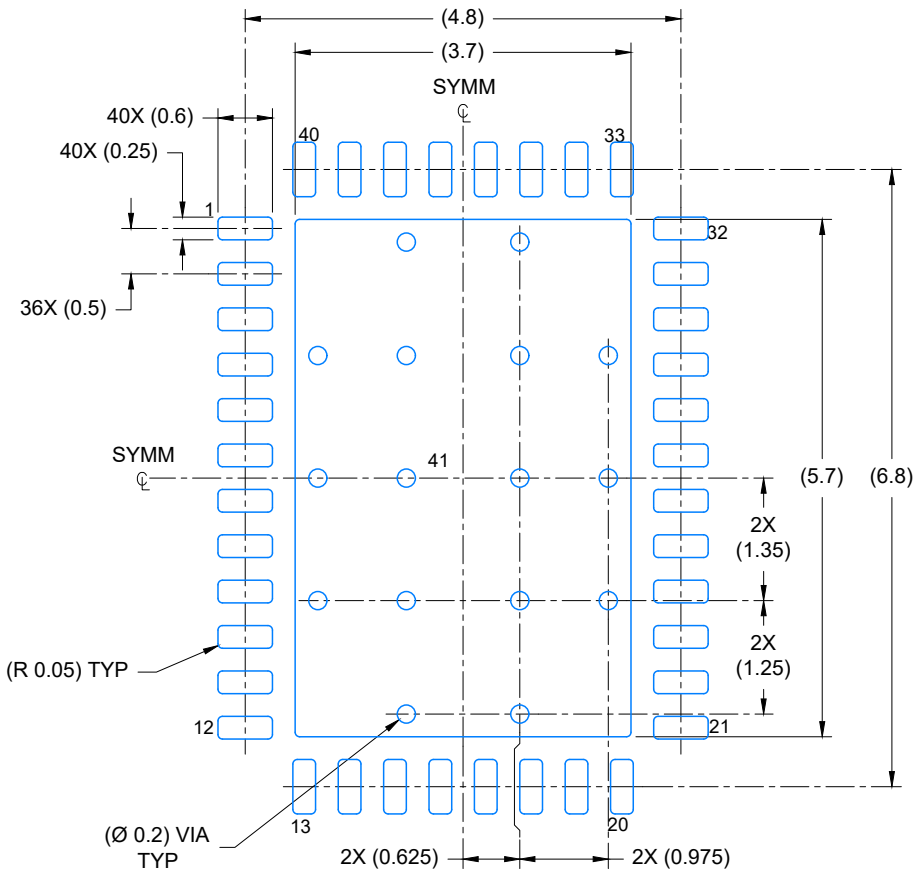
4225115/A

PLASTIC QUAD FLATPACK- NO LEAD

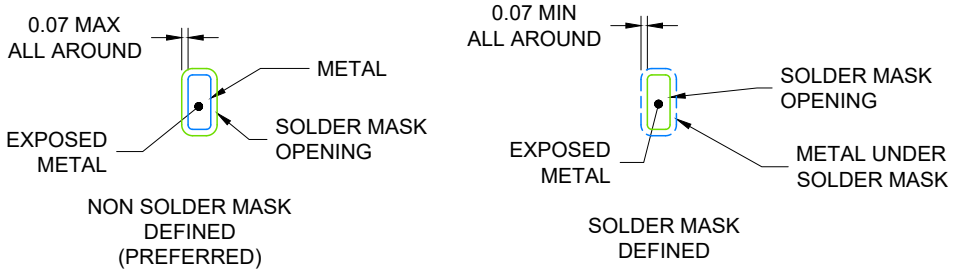


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

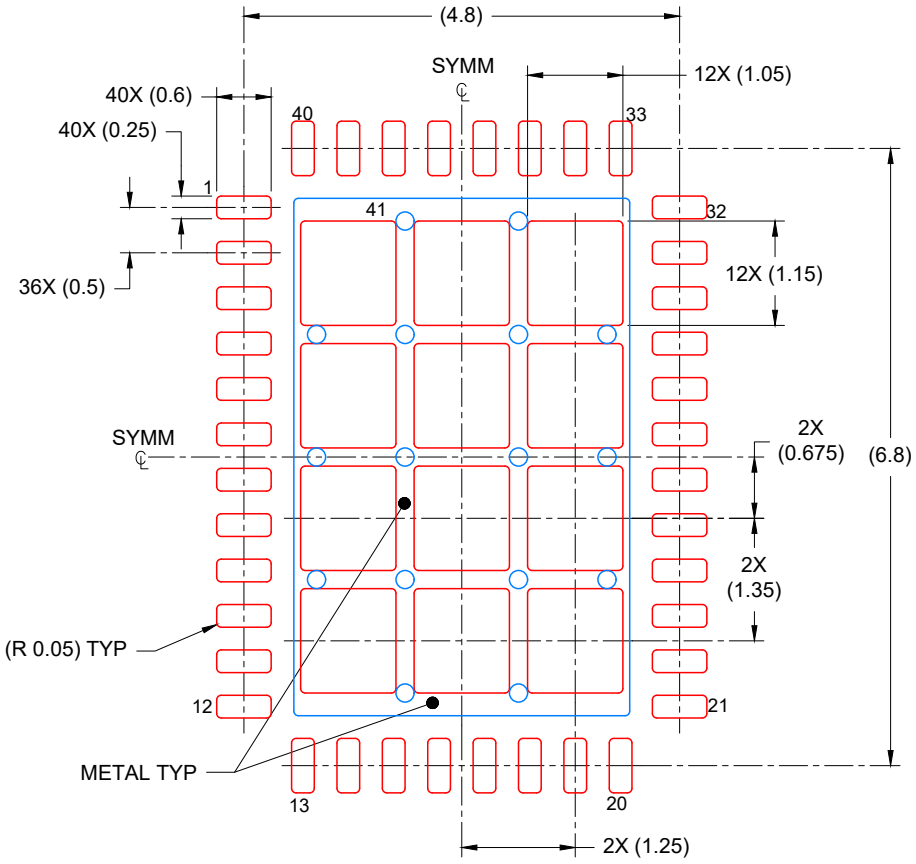


SOLDER MASK DETAILS

4225901/A 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4225901/A 05/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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