DP83TC816-Q1 100Base-T1 Automotive Ethernet PHY Transceiver With IEEE802.1AS, AVB Clocks and TC10 Sleep-Wake

1 Features

- IEEE802.3bw compliant 100BASE-T1 PHY
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- IEEE 802.1AS time synchronization
  - Highly accurate 1pps signal
  - Multiple IOs for event capture and trigger
- Synchronized audio clock generation for AVB
  - I2S and TDMx SCLK/FSYNC clock generation
  - Configurable FSYNC, SCLK, MCLK frequencies
  - Automatic phase adjustment through IEEE1722 CRF decode
- OA TC-10 compliant sleep, wake up
- Robust EMC performance
  - IEC62228-5, OA EMC compliant
  - IEC61000-4-2 ESD level 4 MDI: ±8kV CD
  - SAE J2962-3 EMC compliant
  - 39dBm DPI immunity with ±5% asymmetry
  - < 4dBµV radiated emissions in GPS and glonass bands
  - Stripline emissions: class-II compliant
- MAC Interfaces: MII, RMII, RGMII, SGMII
- Footprint compatible with TI's 100BASE-T1, 1000BASE-T1 PHY - with BOM options
- 48V ready: VBAT transients to MDI up to +/– 70V
- Diagnostic tool kit
  - Signal quality indication (SQI) and time domain reflectometry (TDR)
  - Voltage, temperature, and ESD sensors
  - PPM monitor: provides external clock ppm drift (up to ±100ppb accuracy)
- Single 3.3V supply capability

2 Applications

- ADAS
  - Radar synchronization
- Body electronics and lighting
  - Body control module
  - Zone control module
- Telematics

3 Description

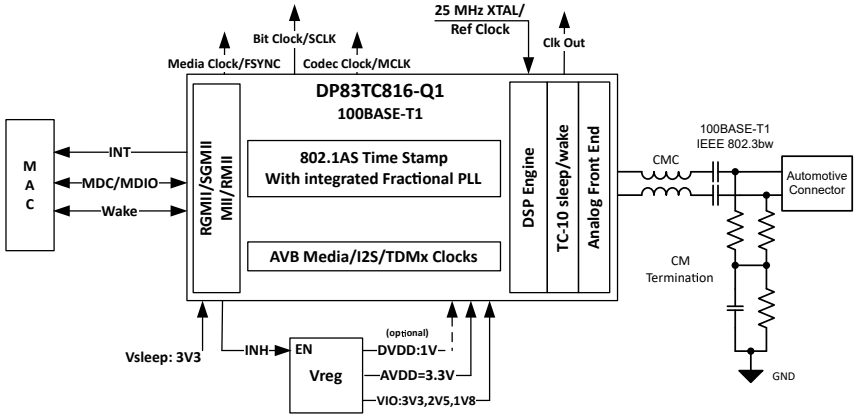
The DP83TC816-Q1 is an IEEE 802.3bw and Open Alliance (OA) compliant automotive qualified 100Base-T1 Ethernet physical layer transceiver. The device provides all physical layer functions needed to transmit and receive data over unshielded, shielded single twisted-pair cables with xMII interface flexibility.

DP83TC816-Q1 integrates IEEE802.1AS / IEEE1588v2 hardware time stamping and fractional PLL, enabling highly accurate time synchronization. The fractional PLL enables frequency and phase synchronization of the wall clock (eliminating the need for external VCXO) and generation of a wide range of time synchronized frequencies needed for audio and other ADAS applications. The PHY also integrates IEEE 1722 CRF decode to generate Media clock and Bit Clock for AVB and other audio applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DP83TC816-Q1	RHA (VQFN, 36)	6.00mm × 6.00mm

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematics

Table of Contents

4 Device Comparison Table

PART NUMBER	TC10?	MACsec?	802.1AS?	AVB CLOCKS?	FOOTPRINT COMPATIBLE?
DP83TC812x-Q1	Yes	No	No	No	Yes
DP83TC814x-Q1	No	No	No	No	Yes
DP83TC815-Q1	Yes	No	Yes	No	Yes
DP83TC816-Q1	Yes	No	Yes	Yes	Yes
DP83TC817S-Q1	Yes	Yes	Yes	No	Yes
DP83TC818S-Q1	Yes	Yes	Yes	Yes	Yes

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

DATE	REVISION	NOTES
November 2025	*	Initial Release

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83TC816RHARQ1	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	816

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

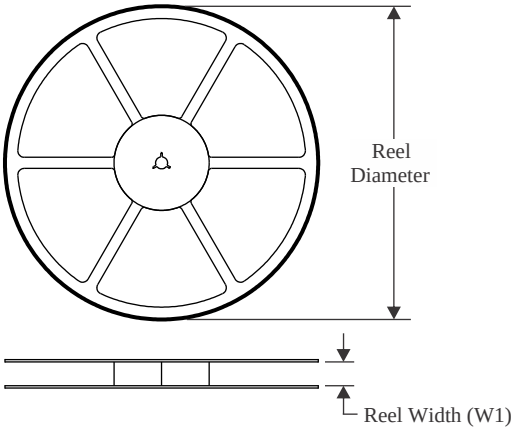
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

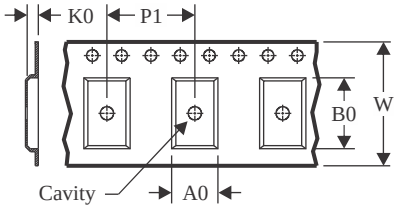
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

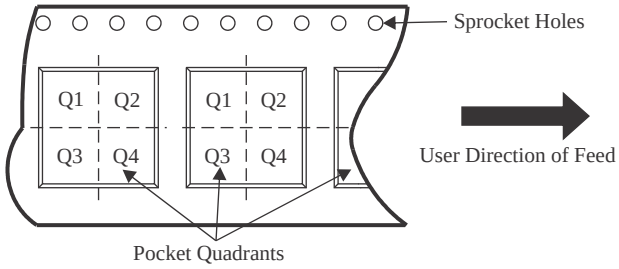


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

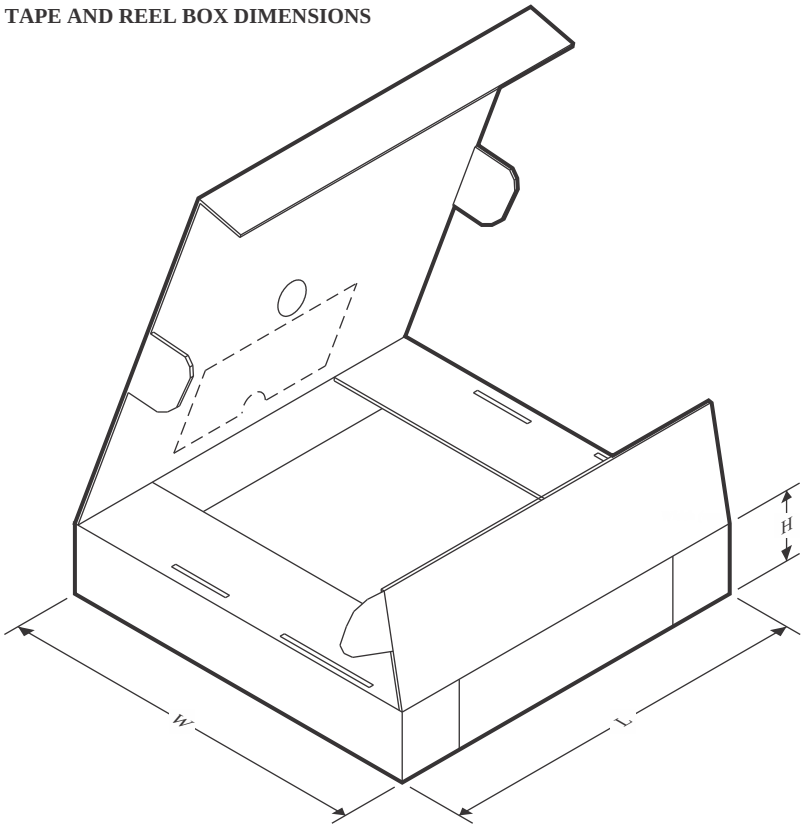
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83TC816RHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83TC816RHARQ1	VQFN	RHA	36	2500	360.0	360.0	36.0

GENERIC PACKAGE VIEW

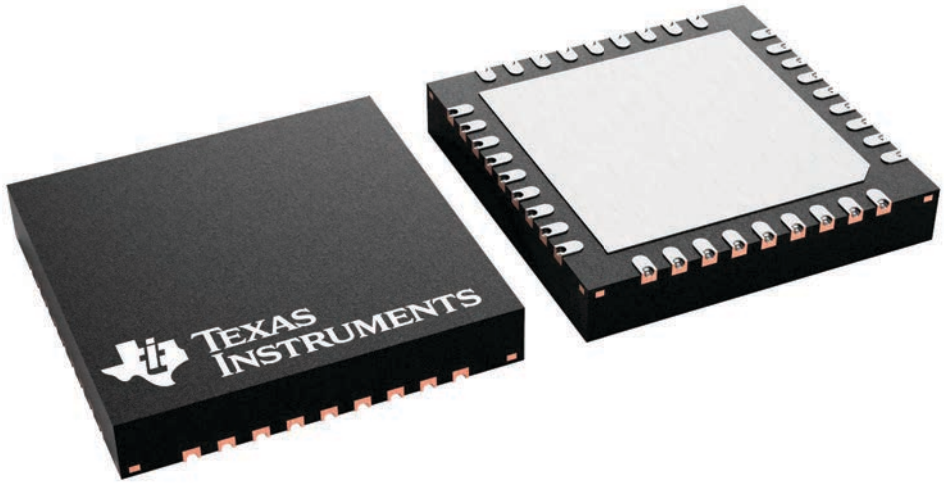
RHA 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



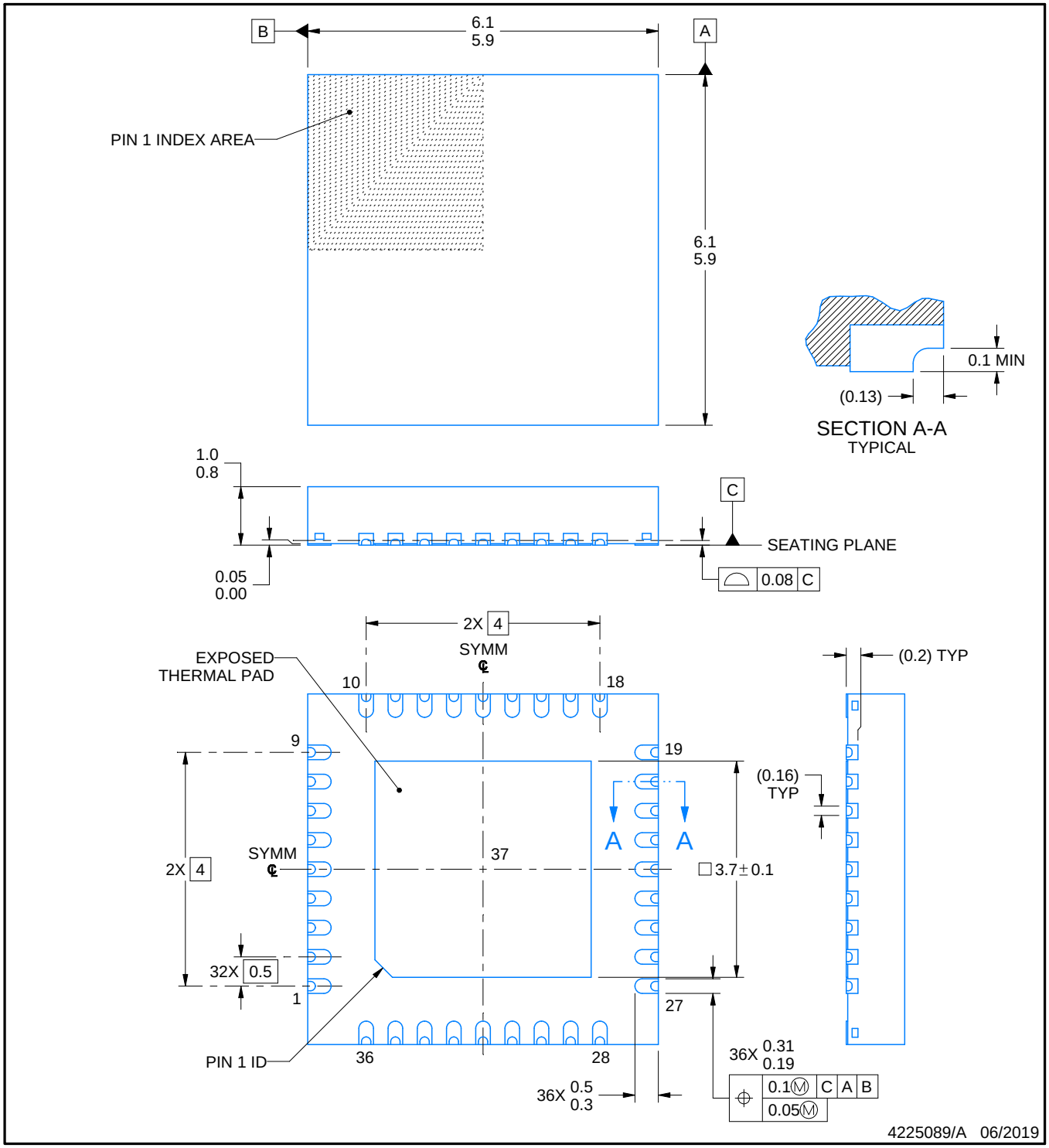
4228438/A

PACKAGE OUTLINE

RHA0036A

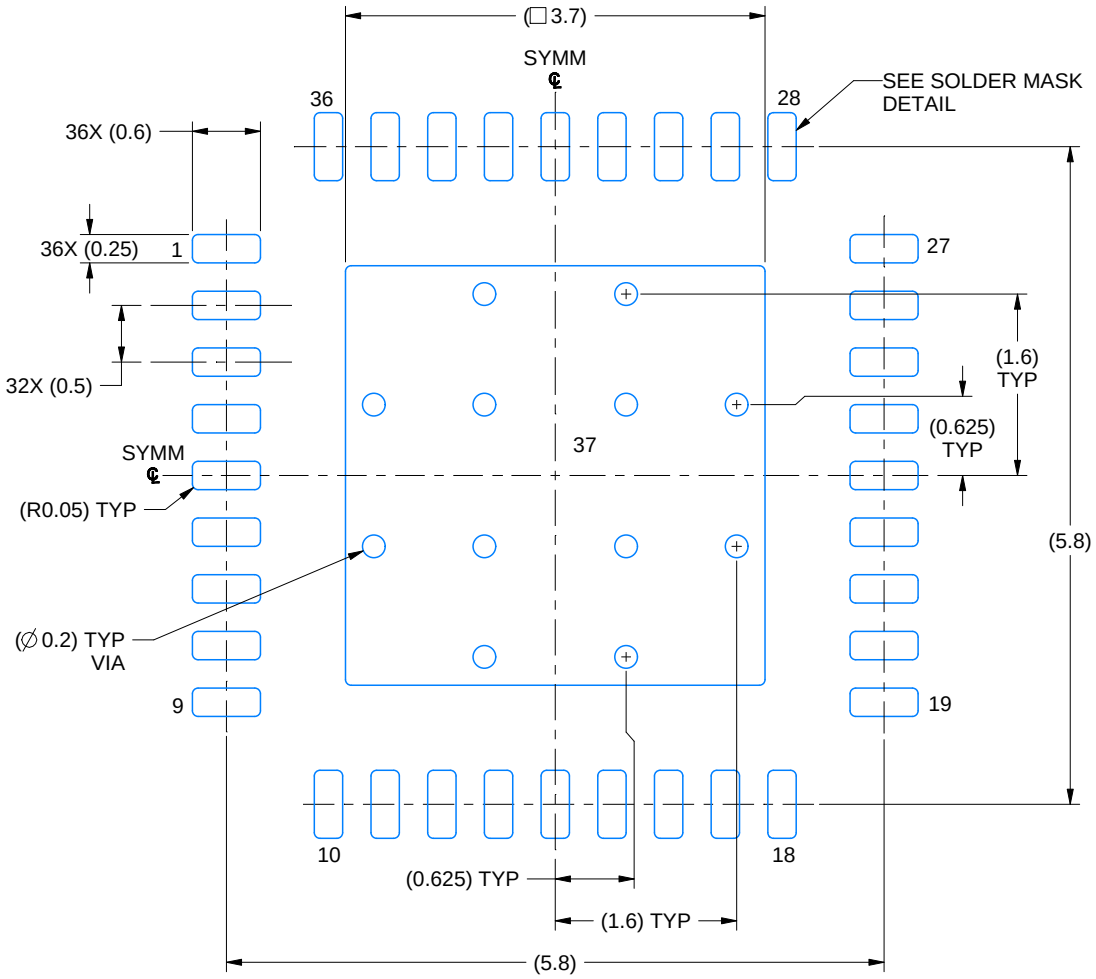
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

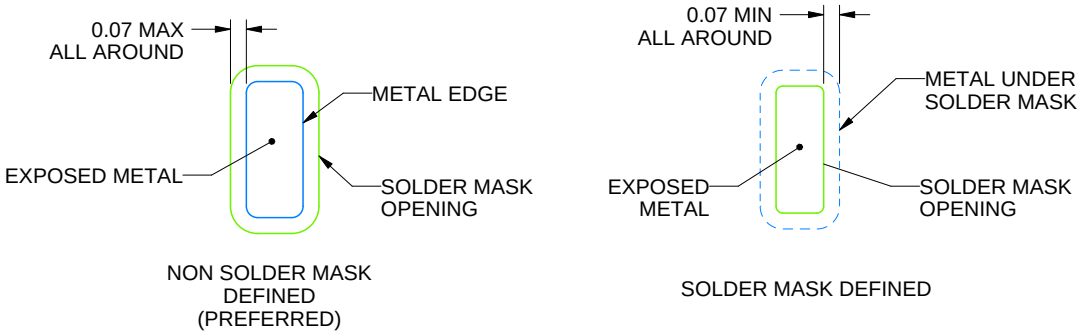


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225089/A 06/2019

NOTES: (continued)

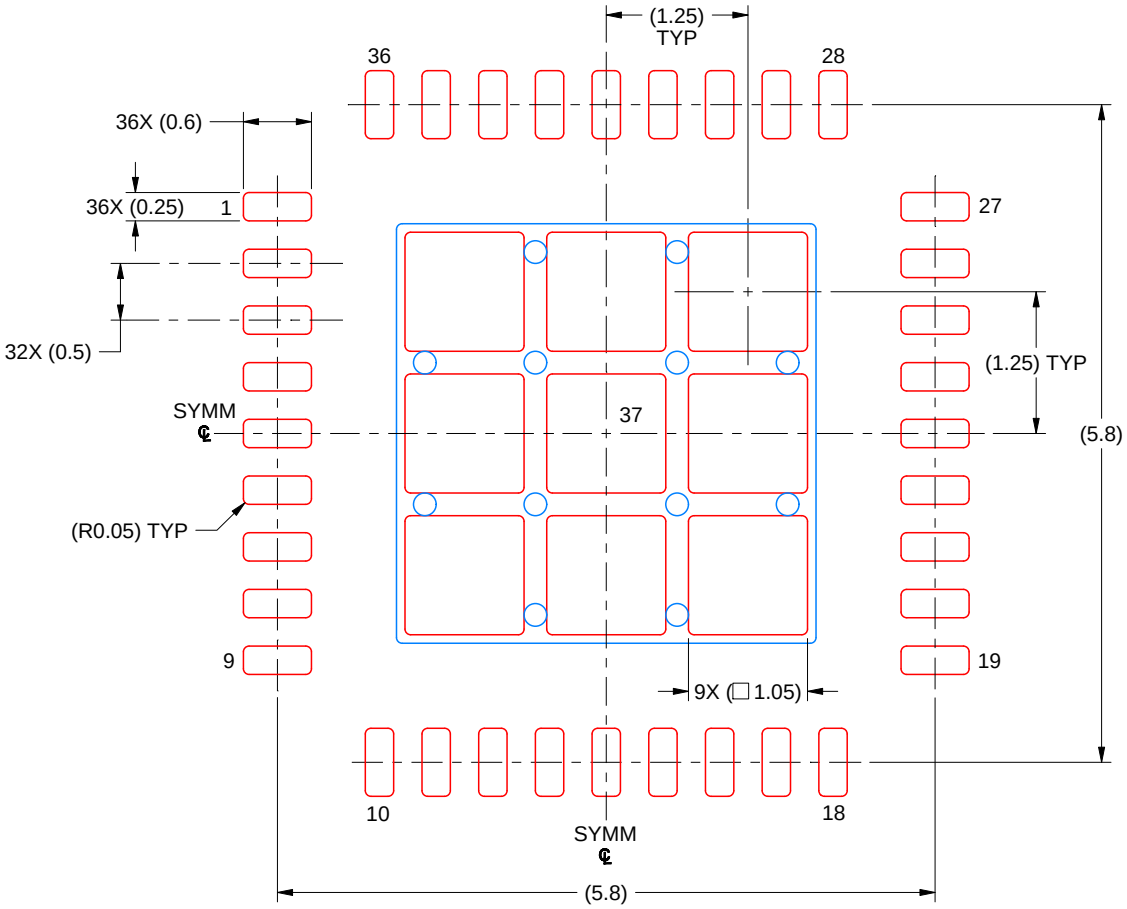
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0036A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225089/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025