DP83826 Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY

1 Features

- Low and deterministic latency
  - TX latency: 40ns, RX latency: 170ns
  - Deterministic latency over power cycles < ±2ns
  - Fixed phase XI to TX_CLK relationship < ±2ns
- Robust and small system implementation
  - Integrated circuitry for enhanced EMC
  - IEC 61000-4-2 ESD: ± 8kV contact, ±15kV air
  - IEC 61000-4-4 EFT: ±4 kV at 5kHz, 100kHz
  - CISPR 22 conducted emissions Class B
  - CISPR 22 radiated emissions Class B
  - Fast link-drop < 10µs
  - Cable reach > 150 meters
  - Voltage mode line driver
  - Integrated terminations on MAC interface
  - Voltage tolerance: ±10%
- Two selectable pin modes in single device
  - ENHANCED mode for additional features
  - BASIC mode for common Ethernet pinout
- Low power consumption < 160mW
- MAC interfaces: MII, RMII
- Programmable energy-saving modes
  - Active sleep
  - Deep power down
  - Energy Efficient Ethernet (EEE) IEEE 802.3az
  - Wake-on-LAN (WoL)
- Diagnostic tools: cable diagnostics, built-in self-test (BIST), loopback modes
- Single, 3.3V power supply
- I/O voltages: 1.8V or 3.3V
- RMII back-to-back repeater mode
- DP83826E operating temperature range: –40°C to 105°C
- DP83826I operating temperature range: –40°C to 85°C
- IEEE 802.3 compliant: 10BASE-Te, 100BASE-TX
- EtherCAT® compliant

2 Applications

- Factory automation, robotics and motion control
- Motor drives
- Grid infrastructure
- Building automation
- Industrial Ethernet fieldbus

3 Description

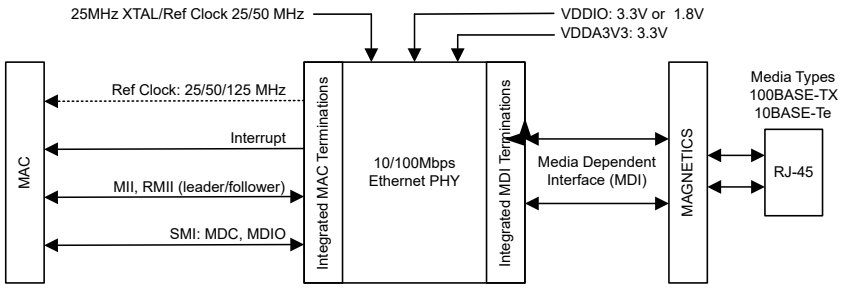
The DP83826 offers low and deterministic latency, low power and supports 10BASE-Te, 100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems. The device includes hardware bootstraps to achieve fast link-up time, fast link-drop detection modes and dedicated reference CLKOUT to clock synchronize other modules on the systems.

The two configurable modes are BASIC standard Ethernet mode that uses a common Ethernet pinout, and ENHANCED Ethernet mode which supports standard Ethernet mode and multiple industrial Ethernet fieldbus applications with the additional features and hardware bootstraps configuration.

Device Family Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)	ATTRIBUTES
DP83826E/I	VQFN (32)	5.00mm × 5.00mm	Lowest latency, common pinout
DP83825I	WQFN (24)	3.00mm × 3.00mm	Small size, optimized solution cost
DP83822HF/IF/H/I	VQFN (32)	5.00mm × 5.00mm	Wide temperature range, fiber, and RGMII support

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Mode Comparison Tables

The DP83826 can be strapped to operate in either ENHANCED mode or BASIC mode. ENHANCED mode allows the DP83826 to support real-time Ethernet applications in addition to standard Ethernet applications. BASIC mode allows the DP83826 to support standard Ethernet applications. Additionally, the DP83826 pinout in BASIC mode matches a common PHY pinout used in many applications.

Table 4-1. Selecting ENHANCED Mode or BASIC Mode

ENHANCED Mode	BASIC Mode
Leave ModeSelect (Pin 1) unconnected or Connect pin to VDDIO through pullup resistor	Short ModeSelect (Pin 1) to GND

Table 4-2. Pin Map Difference Between ENHANCED Mode and BASIC Mode

PIN NO.	ENHANCED MODE	BASIC MODE
31	CLKOUT/LED1	LED1/TX_ER
21	PWRDN/INT	INT

Table 4-3. Hardware Bootstraps Difference Between ENHANCED Mode and BASIC Mode

HARDWARE BOOTSTRAPS	ENHANCED Mode(3)	BASIC Mode
Fast link-drop enable and disable(1)	Yes	No (Always enabled)
Fast link-drop detection mechanism	Strap controllable	RX_Error and Signal Energy
Auto-MDIX enable and disable(1)	Yes	No
Force MDI/MDIX selection(1)	Yes	No
RMII back-to-back repeater mode configuration(2)	Yes	No
MII or RMII selection	Yes	Yes
Speed selection (10M or 100M)	No	Yes
MII isolate enable and disable	No	Yes
Auto-negotiation enable and disable	Yes	Yes
Number of PHY addresses available	8	8
Half or full duplex selection	No	Yes
CLKOUT in place of LED1	Yes	No
Odd Nibble Detection	Strap controllable	Disabled by default

(1) These pin bootstraps enable the ENHANCED mode DP83826 to meet the stringent requirements of real-time Ethernet applications.
(2) This pin bootstrap enables the ENHANCED mode DP83826 to function as an RMII repeater.
(3) ENHANCED mode includes all the modes of operation BASIC mode can be configured to. The difference is, in these modes of operation, ENHANCED mode requires register configuration.

Note

For a step by step approach on using the DP83826 BASIC mode in existing systems that use a common standard Ethernet pinout, please refer to SNLA338.

Note

For standardized list of Ethernet related acronyms, refer to *Chinese and English Definitions of Acronyms Related to Ethernet Products*.

5 Pin Configuration and Functions (ENHANCED Mode)

The ENHANCED mode is one of two modes that the DP83826 can be configured in at start-up. This mode allows the DP83826 to support real-time Ethernet applications in addition to the standard Ethernet applications. To configure the DP83826 to ENHANCED mode, leave ModeSelect (pin 1) unconnected or pull up with a resistor to VDDIO.

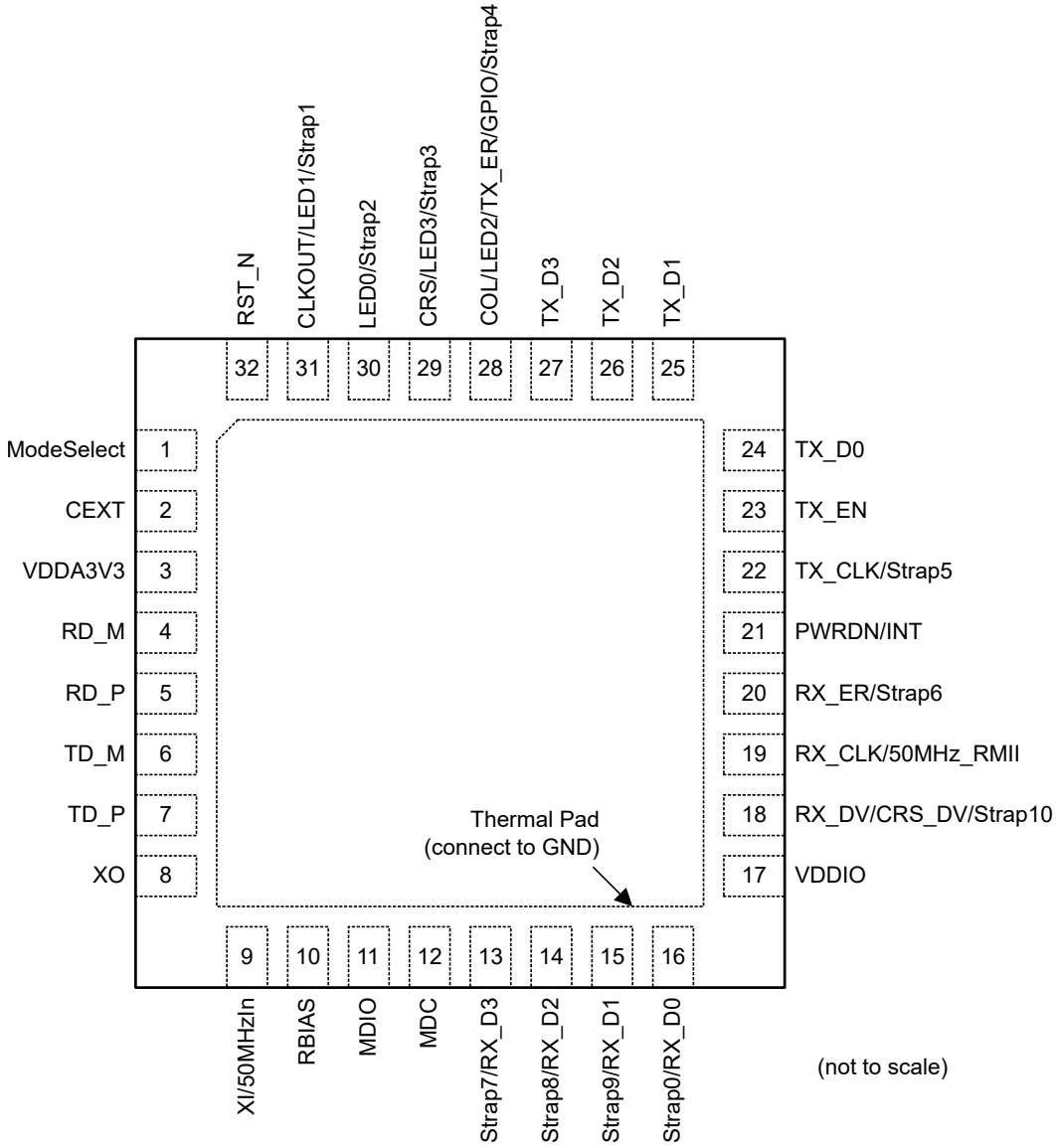


Figure 5-1. RHB Package
32-Pin QFN
(Top View)

Table 5-1. Pin Functions (ENHANCED Mode)

PIN		TYPE [1]	DESCRIPTION
NAME	NO		
ModeSelect	1	Reset: I, PU Active: I, PU	This pin selects the DP83826 operating mode: BASIC mode or ENHANCED mode. For ENHANCED mode, this pin shall be left NC or pulled-up with a resistor to VDDIO. For BASIC mode, this pin shall be shorted to GND.
CEXT	2	A	External capacitor: Connect the CEXT pin through a 2nF capacitor to GND.
VDDA3V3	3	Power	Input analog supply: 3.3V. For decoupling capacitor requirements, refer to *Power Supply Recommendations* section of data sheet.
RD_M	4	A	Differential receive input (physical media dependent: PMD): These differential inputs are automatically configured to accept either 10BASE-Te, 100BASE-TX specific signaling mode.
RD_P	5	A	
TD_M	6	A	Differential transmit output (PMD): These differential outputs are configured to either 10BASE-Te or 100BASE-TX signaling mode based on configuration chosen for PHY.
TD_P	7	A	
XO	8	A	Crystal output: Reference clock output. XO pin is used for crystal only. Leave this pin floating when a CMOS-level oscillator is connected to XI.
XI/50MHzIn	9	A	Crystal or oscillator input clock: MII mode, RMII leader mode: 25MHz ± 50ppm tolerance crystal or oscillator clock. RMII follower mode: 50MHz ± 50ppm tolerance CMOS-level oscillator clock.
RBIAS	10	A	RBIAS (Bias resistor) value 6.49kΩ with 1% precision connected to ground.
MDIO	11	Reset: I, PU Active: I/O, PU	Management data I/O: Bi-directional management data signal that can be sourced by the management station or the PHY. This pin has internal pullup resistor of 10kΩ. An external pullup resistor can be added if needed.
MDC	12	Reset: I, PD Active: I, PD	Management data clock: Synchronous clock to the MDIO serial management input/output data. This clock can be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25MHz. There is no minimum clock rate.
RX_D3	13	Reset: I, PD Active: O Strap7	Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK and contain valid data when RX_DV is asserted. A nibble RX_D[3:0] is received in MII mode. 2-bits RX_D[1:0] is received in RMII mode.
RX_D2	14	Reset: I, PD Active: O Strap8	
RX_D1	15	Reset: I, PD Active: O Strap9	
RX_D0	16	Reset: I, PD Active: O Strap0	
VDDIO	17	Power	I/O supply voltage: 3.3V or 1.8V. For decoupling capacitor requirements, refer to *Power Supply Decoupling Recommendations* section of data sheet.
RX_DV/ CRS_DV	18	Reset: I, PD Active: O Strap10	Receive data valid: This pin indicates valid data is present on the RX_D[3:0] for MII mode and on RX_D[1:0] in RMII mode. In MII mode, this pin acts as RX_DV. In RMII mode, this pin acts as CRS_DV and combines the RMII Carrier and Receive Data Valid indications. This pin can be configured to RX_DV in RMII mode to enable RMII Repeater Mode.
RX_CLK/ 50MHz_RMII	19	Reset: I, PD Active: O	MII receive clock: MII Receive Clock provides a 25MHz reference clock for 100bps speed and a 2.5MHz reference clock for 10Mbps speed, which is derived from the received data stream. In RMII leader mode, this provides 50MHz reference clock. In RMII follower mode, this pin is not used and remains Input, pulldown.
RX_ER	20	Reset: I, PD Active: O Strap6	Receive error: This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. RX_ER is asserted high for every reception error, including errors during Idle. This strap only latches on power-up and not on pin reset.

Table 5-1. Pin Functions (ENHANCED Mode) (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO		
PWRDN/INT	21	Reset: I, PU Active: I/O, PU	Power down (default), interrupt: The default function of this pin is power down. Register access is required to configure this pin as an interrupt. In power down function, an active low signal on this pin places the device in power down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup resistor (9.5kΩ). Some applications require an external PU resistor.
TX_CLK	22	Reset: I, PD Active: O Strap5	MII transmit clock: MII transmit clock provides a 25MHz reference clock for 100Mbps speed and a 2.5MHz reference clock for 10Mbps speed. Note that in MII mode, this clock has constant phase referenced to the input clock. Unused in RMII Mode.
TX_EN	23	Reset: I, PD Active: I, PD	Transmit enable: TX_EN is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D[3:0] in MII mode and on TX_D[1:0] in RMII mode. TX_EN is an active high signal.
TX_D0	24	Reset: I, PD Active: I, PD	Transmit data: In MII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] received from the MAC is synchronous to the rising edge of the reference clock.
TX_D1	25	Reset: I, PD Active: I, PD	
TX_D2	26	Reset: I, PD Active: I, PD	
TX_D3	27	Reset: I, PD Active: I, PD	
COL/LED2/ TX_ER/GPIO	28	Reset: I, PD Active: O Strap4	Collision Detect (default): In MII mode when the pin is acting as Collision Detect (COL), this pin is always LOW in Full Duplex mode. In Half Duplex mode, COL is asserted HIGH only when both transmit and receive media are non-idle. This pin can also be configured as a second additional LED driver (LED2), the MII TX_ER signal or general purpose I/O (GPIO) through register configurations. In RMII mode, this pin acts as LED2 by default.
CRS/LED3	29	Reset: I, PD Active: O Strap3	Carrier sense (default): In MII mode this pin is asserted high when the receive or transmit medium is non-idle. Carrier sense and receive data valid. This pin can be configured as third LED (LED3) through register configuration. In RMII mode, this pin is configured as LED3 by default.
LED0	30	Reset: I, PD Active: O Strap2	LED0: This LED indicates transmit and receive activity in addition to the status of the Link. The LED is ON when link is good. The LED blinks when the transmitter or receiver is active. LED polarity is auto-detected (Active Low/ Active High) based on external pull-up or pull-down on the pin.
CLKOUT/ LED1	31	Reset: I, PU Active: O Strap1	This pin provides 25MHz reference clock from XI as default output after power-on reset (POR). The output is not affected by Resets allowing Application to reset PHY without impacting other system getting impacted. The output clock switches off only by Deep Power Down. The pin can be configured to act as LED1 using strap or register configuration. The strap only latches on power-up and not on pin reset. The LED is ON when link is 100Mbps. LED remains OFF if Link is 10Mbps or no Link. LED polarity is auto-detected (Active Low/ Active High) based on external pull-up or pull-down on the pin. This strap only latches on power-up and not on pin reset.
RST_N	32	Reset: I, PU Active: I, PU	Reset low: RST_N pin is an active low reset input. Asserting this pin low for at least 25µs forces a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value.

(1) I = Input, O = Output, I/O = Input/Ouput, A = Analog, PU or PD = Internal pullup or pulldown: Hardware bootstrap configuration

6 Pin Configuration and Functions (BASIC Mode)

The BASIC mode is one of two modes that the DP83826 can be configured in at start-up. This mode allows the DP83826 to support all the standard Ethernet applications and matches a common pinout configuration used in many of today's applications. To configure the DP83826 to BASIC mode, short ModeSelect (pin 1) to GND.

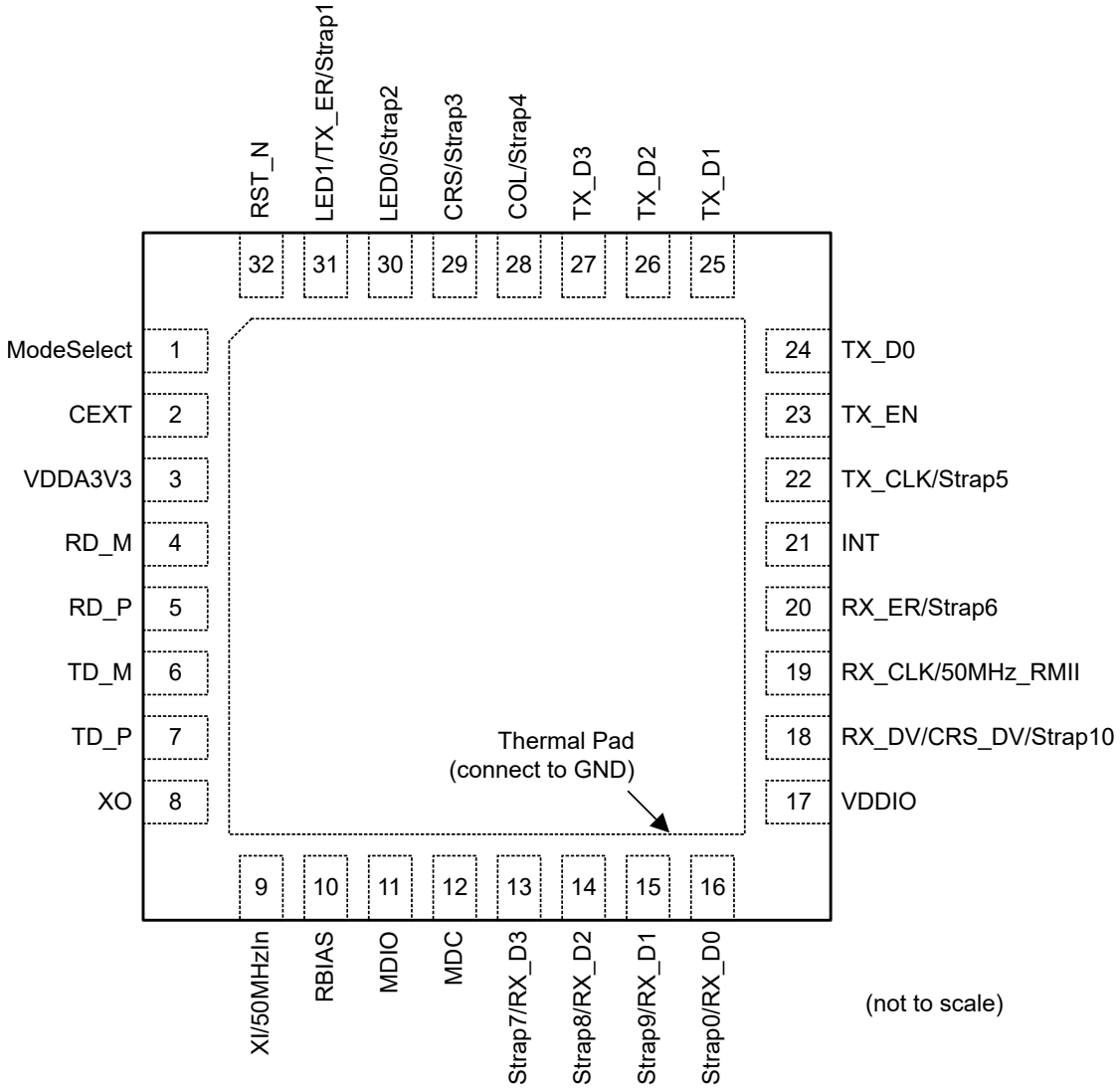


Figure 6-1. RHB Package
32-Pin QFN
(Top View)

Table 6-1. Pin Functions (BASIC Mode)

PIN		TYPE [1]	DESCRIPTION
NAME	NO		
ModeSelect	1	Reset: I, PU Active: I, PU	This pin selects the operating mode: BASIC mode or ENHANCED mode. This pin shall be shorted to GND to configure DP83826 in BASIC mode. For ENHANCED mode, this pin shall be left NC or pulled-up with a resistor to VDDIO.
CEXT	2	A	External capacitor: Connect the CEXT pin through a 2nF capacitor to GND.
VDDA3V3	3	Power	Input analog supply: 3.3V. For decoupling capacitor requirements, refer to *Power Supply Recommendations* section of data sheet.

Table 6-1. Pin Functions (BASIC Mode) (continued)

PIN		TYPE [1]	DESCRIPTION
NAME	NO		
RD_M	4	A	Differential receive input (PMD): These differential inputs are automatically configured to accept either 10BASE-Te or 100BASE-TX specific signaling mode.
RD_P	5	A	
TD_M	6	A	Differential transmit output (PMD): These differential outputs are configured to either 10BASE-Te or 100BASE-TX signaling mode based on the configuration chosen for the PHY.
TD_P	7	A	
XO	8	A	Crystal output: reference clock output. XO pin is used for crystal only. Leave this pin floating when a CMOS-level oscillator is connected to XI.
XI/50MHzIn	9	A	Crystal or oscillator input clock: MII mode or RMII leader mode: 25MHz ± 50ppm tolerance crystal or oscillator clock. RMII follower mode: 50MHz ± 50ppm tolerance CMOS-level oscillator clock.
RBIAS	10	A	Bias resistance: R_{BIAS} value 6.49kΩ 1% precision connected to ground.
MDIO	11	Reset: I, PU Active: I/O, PU	Management data I/O: Bi-directional management data signal that can be sourced by the management station or the PHY. This pin has internal pullup resistor of 10kΩ. An external pullup resistor can be added if needed.
MDC	12	Reset: I, PD Active: I, PD	Management data clock: Synchronous clock to the MDIO serial management input/output data. This clock can be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25MHz. There is no minimum clock rate.
RX_D3	13	Reset: I, PU Active: O Strap7	Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. and contains valid data when RX_DV is asserted. A nibble RX_D[3:0] is received in MII mode. 2-bits RX_D[1:0] is received in RMII mode.
RX_D2	14	Reset: I, PD Active: O Strap8	
RX_D1	15	Reset: I, PD Active: O Strap9	
RX_D0	16	Reset: I, PU Active: O Strap0	
VDDIO	17	Power	I/O supply voltage: 3.3V or 1.8V. For decoupling capacitor requirements, refer to *Power Supply Recommendations* section of data sheet.
RX_DV/ CRS_DV	18	Reset: I, PD Active: O Strap10	Receive data valid: This pin indicates valid data is present on the RX_D[3:0] for MII mode and on RX_D[1:0] in RMII mode. In MII mode, this pin acts as RX_DV. In RMII mode, this pin acts as CRS_DV and combines the RMII carrier and receive data valid indications.
RX_CLK/ 50MHz_RMII	19	Reset: I, PD Active: O	MII receive clock: MII receive clock provides a 25MHz reference clock for 100Mbps speed and a 2.5MHz reference clock for 10Mbps speed, which is derived from the received data stream. In RMII leader mode, this provides 50MHz reference clock. In RMII follower mode, this pin is not used and remains Input/PD.
RX_ER	20	Reset: I, PD Active: O Strap6	Receive Error: This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. RX_ER is asserted high for every reception error, including errors during Idle.
INT	21	Reset: I, PU; Active: O, PU	Interrupt: This pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup resistor (9.5kΩ). Some applications require an external PU resistor.
TX_CLK	22	Reset: I, PD Active: O Strap5	MII transmit clock: MII Transmit Clock provides a25MHz reference clock for 100Mbps speed and a 2.5MHz reference clock for 10Mbps speed. Note that in MII mode, this clock has constant phase referenced to the reference clock. Applications requiring such constant phase can use this feature. Unused in RMII Mode.
TX_EN	23	Reset: I, PD Active: I, PD	Transmit enable: TX_EN is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D[3:0] in MII mode and on TX_D[1:0] in RMII mode. TX_EN is an active high signal.

Table 6-1. Pin Functions (BASIC Mode) (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO		
TX_D0	24	Reset: I, PD Active: I, PD	Transmit data: In MII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] received from the MAC is synchronous to the rising edge of the reference clock.
TX_D1	25	Reset: I, PD Active: I, PD	
TX_D2	26	Reset: I, PD Active: I, PD	
TX_D3	27	Reset: I, PD Active: I, PD	
COL	28	Reset: I, PD Active: O Strap4	Collision detect: In MII mode: For Full-Duplex mode, this pin is always LOW. In Half Duplex mode, this pin is asserted HIGH only when both transmit and receive media are non-idle. In RMII mode, this pin is not used.
CRS	29	Reset: I, PD Active: O Strap3	Carrier sense: In MII mode this pin is asserted high when the receive or transmit medium is non-idle. carrier sense or receive data valid. In RMII mode, this pin is not used.
LED0	30	Reset: I, PU Active: O Strap2	LED0: This LED indicates transmit and receive activity in addition to the status of the Link. The LED is ON when link is good. The LED blinks when the transmitter or receiver is active. LED polarity is fixed Active Low. If an external pull-down is required for strapping purposes, both the strap and LED series resistance need adjustment for correct operation of both the LED and the strap. Please see the LED section for further details.
LED1/TX_ER	31	Reset: I, PU Active: O Strap1	LED1: The pin acts as LED1 as default. The LED is ON when link is 100Mbps. LED remains OFF if the Link is 10Mbps, or there is no Link. This pin can be configured to TX_ER through register configuration. LED polarity is fixed Active Low. If an external pull-down is required for strapping purposes, both the strap and LED series resistance need adjustment for correct operation of both the LED and the strap. Please see the LED section for further details.
RST_N	32	Reset: I, PU Active: I, PU	Reset low: RST_N pin is an active low reset input. Asserting this pin low for at least 25µs forces a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value.

(1) I = Input, O = Output, I/O = Input/Ouput, A = Analog, PU or PD = Internal pullup or pulldown: Hardware bootstrap configuration

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Analog supply voltage	VDDA3V3	–0.3	4	V
IO supply voltage	VDDIO3V3	–0.3	4	V
IO supply voltage	VDDIO1V8	–0.3	2.1	V
Storage Temperature	Tstg	–65	150	°C
MDI pins	TX_P, TX_M, RX_P, RX_M	–0.6	4	V
MAC interface pins	TX_CLK, TX_D[3:0], TX_EN, TX_ER, RX_CLK, RX_D[3:0], RX_ER, RX_DV, CRS, COL	–0.3	4	V
Serial management interface pins	MDIO, MDC	–0.3	4	V
Crystal/Oscillator pins	XI, XO	–0.3	4	V
Reset pin	RST_N	–0.3	4	V

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
ESD (HBM)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) MDI (Media Dependent Interface) pins	±5	kV
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) All pins except MDI	±2	kV
ESD (CDM)	Charged device model (CDM) per JEDEC specification JESD22-C101(2), all pins	±750	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 500V HBM is possible with the necessary precautions. Pins listed as ±5kV and/or ± 4kV can actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 250V CDM is possible with the necessary precautions. Pins listed as ±750V can actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Analog supply voltage	VDDA3V3	3	3.3	3.6	V
IO supply voltage	VDDIO3V3	3	3.3	3.6	V
	VDDIO1V8	1.62	1.8	1.98	V
Operating Free Air Temperature (DP83826E)	T_A	–40	25	105	°C
Operating Free Air Temperature (DP83826I)	T_A	–40	25	85	°C
VDDIO: 1.8V	TX_EN, TX_D0, TX_D1, TX_D2, TX_D3, TX_CLK, RX_D0, RX_D1, RX_D2, RX_D3 RX_DV, RX_ER, MDIO, MDC, COL/LED2, CRS, CLKOUT/LED1, INT/PWDN, RESET, TX_ER	1.62	1.8	1.98	V
	XI Osclliator Input	1.62	1.8	1.98	V
	LED0	1.62	1.8	1.98	V

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
VDDIO: 3.3V	TX_EN, TX_D0, TX_D1, TX_D2, TX_D3, TX_CLK, RX_D0, RX_D1, RX_D2, RX_D3 RX_DV, RX_ER, MDIO, MDC, COL/LED2, CRS, CLKOUT/LED1, INT/PWDN, RESET, TX_ER	3.0	3.3	3.6	V
	XI Osclliator Input	3.0	3.3	3.6	V
	LED0	3.0	3.3	3.6	V

7.4 Thermal Information

(1)

THERMAL METRIC			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	°C/W
Y_{JT}	Junction-to-top characterization parameter	2.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Over operating free-air temperature range with VDDA3V3 = 3V3 (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEEE Tx Conformance (100BaseTx)						
V_{OD}	Differential output voltage		950		1050	mV
IEEE Tx Conformance (10BaseTe)						
V_{OD}	Output differential voltage [2]		1.54	1.75	1.96	V
Power consumption Baseline (Active mode, 50% Traffic, Packet Size : 1518, Random Content, 150 meter Cable)						
$I_{(VDDA3V3=3V3)}$	MII (100BaseTx)			45	53	mA
$I_{(VDDA3V3=3V3)}$	MII (10BaseTe)			35	46	mA
$I_{(VDDA3V3=3V3)}$	RMII coordinator (100BaseTx)			45	53	mA
$I_{(VDDA3V3=3V3)}$	RMII coordinator (10BaseTe)			35	46	mA
$I_{(VDDA3V3=3V3)}$	RMII follower (100BaseTx)			45	53	mA
$I_{(VDDA3V3=3V3)}$	RMII follower (10BaseTe)			35	46	mA
$I_{(VDDIO=3V3)}$	MII (100BaseTx)			8	14	mA
$I_{(VDDIO=3V3)}$	MII (10BaseTe)			5	12	mA
$I_{(VDDIO=3V3)}$	RMII coordinator (100BaseTx)			9	14	mA
$I_{(VDDIO=3V3)}$	RMII coordinator (10BaseTe)			9	12	mA
$I_{(VDDIO=3V3)}$	RMII follower (100BaseTx)			7	8.5	mA
$I_{(VDDIO=3V3)}$	RMII follower (10BaseTe)			5	6	mA
$I_{(VDDIO=1V8)}$	MII (100BaseTx)			5	7	mA
$I_{(VDDIO=1V8)}$	MII (10BaseTe)			3	6	mA
$I_{(VDDIO=1V8)}$	RMII coordinator (100BaseTx)			5	7	mA
$I_{(VDDIO=1V8)}$	RMII coordinator (10BaseTe)			5	6	mA
$I_{(VDDIO=1V8)}$	RMII follower (100BaseTx)			3	6	mA
$I_{(VDDIO=1V8)}$	RMII follower (10BaseTe)			2	3	mA
Power consumption (Active mode worst case, 100% Traffic, Packet Size : 1518, Random Content, 150 meter Cable)						
$I_{(VDDA3V3=3V3)}$	MII (100BaseTx)			44	55	mA
$I_{(VDDA3V3=3V3)}$	MII (10BaseTe)			35	48	mA
$I_{(VDDA3V3=3V3)}$	RMII coordinator (100BaseTx)			44	55	mA
	RMII coordinator (10BaseTe)			35	48	mA
	RMII follower (100BaseTx)			44	55	mA
	RMII follower (10BaseTe)			35	48	mA

7.5 Electrical Characteristics (continued)

Over operating free-air temperature range with VDDA3V3 = 3V3 (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(VDDIO=3V3)}$	MII (100BaseTx)			10	15	mA
$I_{(VDDIO=3V3)}$	MII (10BaseTe)			5	12	mA
$I_{(VDDIO=3V3)}$	RMII coordinator (100BaseTx)			11	15	mA
	RMII coordinator (10BaseTe)			9	12	mA
	RMII follower (100BaseTx)			8	12	mA
	RMII follower (10BaseTe)			5	10	mA
$I_{(VDDIO=1V8)}$	MII (100BaseTx)			6	9	mA
$I_{(VDDIO=1V8)}$	MII (10BaseTe)			2	6	mA
$I_{(VDDIO=1V8)}$	RMII coordinator (100BaseTx)			6	9	mA
	RMII coordinator (10BaseTe)			5	7	mA
	RMII follower (100BaseTx)			4	8	mA
	RMII follower (10BaseTe)			2	6	mA
Power Consumption (Low power modes)						
$I_{(AVDD3V3=3V3)}$	100 BaseTx EEE mode	100 BaseTx link in EEE mode with LPIs ON		15		mA
$I_{(AVDD3V3=3V3)}$	IEEE Power Down				11	mA
$I_{(AVDD3V3=3V3)}$	Active Sleep				18	mA
$I_{(AVDD3V3=3V3)}$	RESET				12.5	mA
I(VDDIO=3V3)	100 BaseTx EEE mode	100 BaseTx link in EEE mode with LPIs ON		6		mA
I(VDDIO=3V3)	IEEE Power Down				10.5	mA
I(VDDIO=3V3)	Active Sleep				10.5	mA
I(VDDIO=3V3)	RESET				10.5	mA
I(VDDIO=1V8)	100 BaseTx EEE mode	100 BaseTx link in EEE mode with LPIs ON		4		mA
I(VDDIO=1V8)	IEEE Power Down				5.5	mA
I(VDDIO=1V8)	Active Sleep				5.5	mA
I(VDDIO=1V8)	RESET				5.5	mA
Bootstrap DC Characteristics (2 Level)						
V_{IH_3v3}	High Level bootstrap threshold : 3V3		1.3			V
V_{IL_3v3}	Low Level bootstrap threshold : 3V3				0.6	V
V_{IH_1v8}	High Level bootstrap threshold:1V8		1.3			V
V_{IL_1v8}	Low Level bootstrap threshold :1V8				0.6	V
Crystal oscillator						
C_{OSC_EXT}	External load capacitance			15	30	pF
IO						

7.5 Electrical Characteristics (continued)

Over operating free-air temperature range with VDDA3V3 = 3V3 (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_3V3}	High level input voltage	VDDIO = 3.3V ±10%	1.7			V
V_{IL_3V3}	Low level input voltage	VDDIO = 3.3V ±10%			0.8	V
V_{OH_3V3}	High level output voltage	I_{OH} = –2mA, VDDIO = 3.3V ±10%	2.4			V
V_{OL_3V3}	Low level output voltage	I_{OL} = 2mA, VDDIO = 3.3V ±10%			0.8	V
V_{IH_1V8}	High level input voltage	VDDIO = 1.8V ±10%	0.65 x VDDIO			V
V_{IL_1V8}	Low level input voltage	VDDIO = 1.8V ±10%			0.35 x VDDIO	V
V_{OH_1V8}	High level output voltage	I_{OH} = –2mA, VDDIO = 1.8V ±10%	VDDIO – 0.45			V
V_{OL_1V8}	Low level output voltage	I_{OL} = 2mA, VDDIO = 1.8V ±10%			0.45	V
I_{IH}	Input high current	T_A = –40°C to 85°C, VIN=VDDIO			15	µA
I_{IH}	Input high current	T_A = –40°C to 105°C, VIN=VDDIO			25	µA
I_{IL}	Input low current	T_A = –40°C to 85°C, VIN=GND			15	µA
I_{IL}	Input low current	T_A = –40°C to 105°C, VIN=GND			25	µA
I_{OZH}	Tri-state output high current	T_A = –40°C to 85°C	–15		15	µA
I_{OZH}	Tri-state output high current	T_A = –40°C to 105°C	–25		25	µA
I_{OZL}	Tri-state output low current	T_A = –40°C to 85°C	–15		15	µA
I_{OZL}	Tri-state output low current	T_A = –40°C to 105°C	–25		25	µA
R_{PD}	Internal pull down resistor		7.5	10	12.5	kΩ
R_{PU}	Internal pull up resistor		7.5	10	12.5	kΩ
C_{IN}	Input capacitance	XI pin		1		pF
C_{IN}	Input capacitance	Input pins		5		pF
C_{OUT}	Output capacitance	XO pin		1		pF
C_{OUT}	Output capacitance	Output pins		5		pF
$V_{CM\text{-}OSC}$	XI input osc clock common mode voltage	VDDIO = 1.8V		0.9		V
$V_{CM\text{-}OSC}$	XI input osc clock common mode voltage	VDDIO = 3.3V		1.65		V
R_{series}	Integrated MAC series termination resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK, TX_CLK		50		Ω

(1) Specified by production test, characterization or design
(2) Requires register 0x030E to program to 0x4A40

7.6 Timing Requirements

(1)

PARAMETER		MIN	NOM	MAX	UNIT
Power Up Timing					
T1	Voltage ramp duration (0% to 100% VDDIO)	0.5		50	ms
T2	Supply sequencing VDDA3V3 followed by VDDIO or VDDIO followed by VDDA3V3 (2) (4)	0		200	ms
T3	Voltage ramp duration (0% to 100% of VDDA3V3)	0.5		50	ms
T4	POR release time / Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access			50	ms
T5	Powerup to FLP		1500		ms
	Pedestal voltage on VDDA3V3, VDDIO before Power Ramp			0.3	V
Reset Timing					
T1	RESET PULSE Width: Miminum reset pulse width to be able to reset (w/o debouncing caps)	25			µs
T2	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access			2	ms
T3	Reset to FLP		1500		ms
	Reset to 100M signaling (strapped mode)		0.5		ms
	Reset to RMII coordinator clock		0.2		ms
Fast Link Pulse Timing					
T1	Clock pulse to clock pulse period	111	125	139	µs
T2	Clock pulse to data pulse period	55.5	62.5	69.5	µs
T3	Clock/Data pulse width		104		ns
T4	FLP burst to FLP burst period	8	16	24	ms
T5	FLP burst width		2		ms
	Pulse in burst width	17		33	
Link Up Timing					
	Fast Link Drop enabled using straps , 150 meter cable			10	µs
	Fast Link Drop Time using Mode 1 (Signal/Energy Loss indication)			10	µs
	Fast Link Drop Time using Mode 2 (Low SNR Threshold) (5)			10	µs
	Fast Link Drop Time using Mode 3 (MLT3 Error count) (5)			10	µs
	Fast Link Drop Time using Mode 4 (RX Error count)			10	µs
	Fast Link Drop Time using Mode 5 (Descrambler link drop) (5)			11	µs
100M EEE timings					
	Sleep time		210		µs
	Quiet time		20		ms
	Wake Time (Tw_sys_tx)		36		µs
	Refresh time		200		µs
100M MII Receive Timing					
T1	RX_CLK high / low time	16	20	24	ns
T2	RX_D[3:0], RX_ER, RX_DV delay from RX_CLK rising	10		30	ns
100M MII Transmit Timing					
T1	TX_CLK high / low time	16	20	24	ns
T2	TX_D[3:0], TX_ER, TX_EN setup to TX_CLK	10			ns
T3	TX_D[3:0], TX_ER, TX_EN hold from TX_CLK	0			ns
10M MII Receive Timing					
T1	RX_CLK high / low time(3)	160	200	240	ns

7.6 Timing Requirements (continued)

(1)

PARAMETER		MIN	NOM	MAX	UNIT
T2	RX_D[3:0], RX_ER, RX_DV delay from RX_CLK rising(3)	100		300	ns
10M MII Transmit Timing					
T1	TX_CLK high / low time	190	200	210	ns
T2	TX_D[3:0], TX_ER, TX_EN setup to TX_CLK	25			ns
T3	TX_D[3:0], TX_ER, TX_EN hold from TX_CLK	0			ns
100M RMII Leader Timing					
	RMII leader clock period		20		ns
	RMII leader clock duty cycle	35		65	%
100M RMII Follower Timing					
T2	TX_D[1:0], TX_ER, TX_EN setup to reference clock rising. Refer to RMII Transmit Timing.	4			ns
T3	TX_D[1:0], TX_ER, TX_EN hold from reference clock rising. Refer to RMII Transmit Timing.	2			ns
T4	RX_D[1:0], RX_ER, CRS_DV delay from reference clock rising. Refer to RMII Receive Timing.	4		14	ns
SMI Timing					
T1	MDC to MDIO (output) delay time	0		13	ns
T2	MDIO (input) to MDC setup time	10			ns
T3	MDIO (input) to MDC hold time	10			ns
T4	MDC frequency		2.5	24	MHz
Output Clock Timing (50M RMII Leader Clock)					
	Frequency (PPM)			50	ppm
	Jitter (Long term 500 cycles)			450	ps
	Rise / Fall time			5	ns
	Duty cycle	40		60	%
Output Clock Timing (25M Clockout)					
	Frequency (PPM)			50	ppm
	Duty cycle	35		65	%
	Rise time			4000	ps
	Fall time			5000	ps
	Jitter (long term: 500 cycles)			300	ps
	Jitter (short term)			250	ps
	Frequency		25		MHz
25MHz Input Clock Tolerance					
	Frequency tolerance (Same as 'PLL ouptut frequency PPM' from ElectChar_Sections)	–100		100	ppm
	Rise / Fall time			5	ns
	Jitter tolerance (RMS)			50	ps
	Input phase noise at 1kHz			–98	dBc/Hz
	Input phase noise at 10kHz			–113	dBc/Hz
	Input phase noise at 100kHz			–113	dBc/Hz
	Input phase noise at 1MHz			–113	dBc/Hz
	Input phase noise at 10MHz			–113	dBc/Hz
	Duty cycle	40		60	%
50MHz Input Clock tolerance					

7.6 Timing Requirements (continued)

(1)

PARAMETER		MIN	NOM	MAX	UNIT
	Frequency tolerance	–100		100	ppm
	Rise / Fall time			5	ns
	Jitter tolerance (RMS)			50	ps
	Jitter tolerance long term jitter derived from Phase Noise (100,000 Cycles)				ps
	Input phase noise at 1kHz			–87	dBc/Hz
	Input phase noise at 10kHz			–107	dBc/Hz
	Input phase noise at 100kHz			–107	dBc/Hz
	Input phase noise at 1MHz			–107	dBc/Hz
	Input phase noise at 10MHz			–107	dBc/Hz
	Duty cycle	40		60	%
Latency Timing					
	MII 100M Tx (MII to MDI): Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI, FAST RX_DV enabled, 100 meter Cable	38		40	ns
	MII 100 Rx (MDI to MII): SSD symbol on MDI to Rising edge of RX_CLK with assertion of RX_DV, FAST RX_DV enabled, 100 meter Cable	166		170	ns
	MII 10M Tx (MII to MDI): Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI			540	ns
	RMII follower 100M Tx (RMII to MDI) :Follower RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI, FAST RX_DV enabled, 100 meter Cable	88		96	ns
	RMII leader 100M Tx (RMII to MDI): Leader RMII rising edge clock with assertion TX_EN to SSD symbol on MDI, FAST RX_DV enabled, 100 meter Cable	88		96	ns
	RMII follower 10M Tx (RMII to MDI): Follower RMII rising edge XI clock with assertion TX_EN to SSD symbol on MDI			1360	ns
	RMII leader 10M Tx (RMII to MDI): Leader RMII rising edge clock with assertion TX_EN to SSD symbol on MDI			1360	ns
	MII 10M Rx (MDI to MII): SSD symbol on MDI to Rising edge of RX_CLK with assertion of RX_DV, FAST RX_DV enabled, 100 meter Cable			1640	ns
	RMII follower 100M Rx (MDI to RMII): SSD symbol on MDI to follower RMII rising edge of XI clock with assertion of CRS_DV, FAST RX_DV enabled, 100 meter Cable	268		288	ns
	RMII leader 100M Rx (MDI to RMII): SSD symbol on MDI to leader RMII rising edge of leader clock with assertion of CRS_DV	252		270	ns
	RMII follower 10M (MDI to RMII): SSD symbol on MDI to follower RMII rising edge of XI clock with assertion of CRS_DV (10M)	2110		2152	ns
	RMII leader 10M (MDI to RMII): SSD symbol on MDI to leader RMII rising edge of leader clock with assertion of CRS_DV (10M)	2110		2152	ns
	MII : XI to TXCLK phase difference (across Resets, Power Cycle)	0	2	4	ns

(1) Specified by Design, Production or Characterization test
(2) Clock shall be available at start of power ramp of supplies. If clock is delayed, additional RESET_N is needed post POR completion. Reset can be initiated after 100µs of clock stabilization and POR completion
(3) While receiving first nibble of data, PHY switches source from local to recovered clock causing RX_CLK to stretch and impacting the RX_CLK to RX_DV delay
(4) Both VDDIO or AVDD supply can ramp together or ramp of any of them can be delayed up to max value)
(5) Enable Rx_Error count or Signal/Energy Loss indication to meet maximum limit

7.7 Timing Diagrams

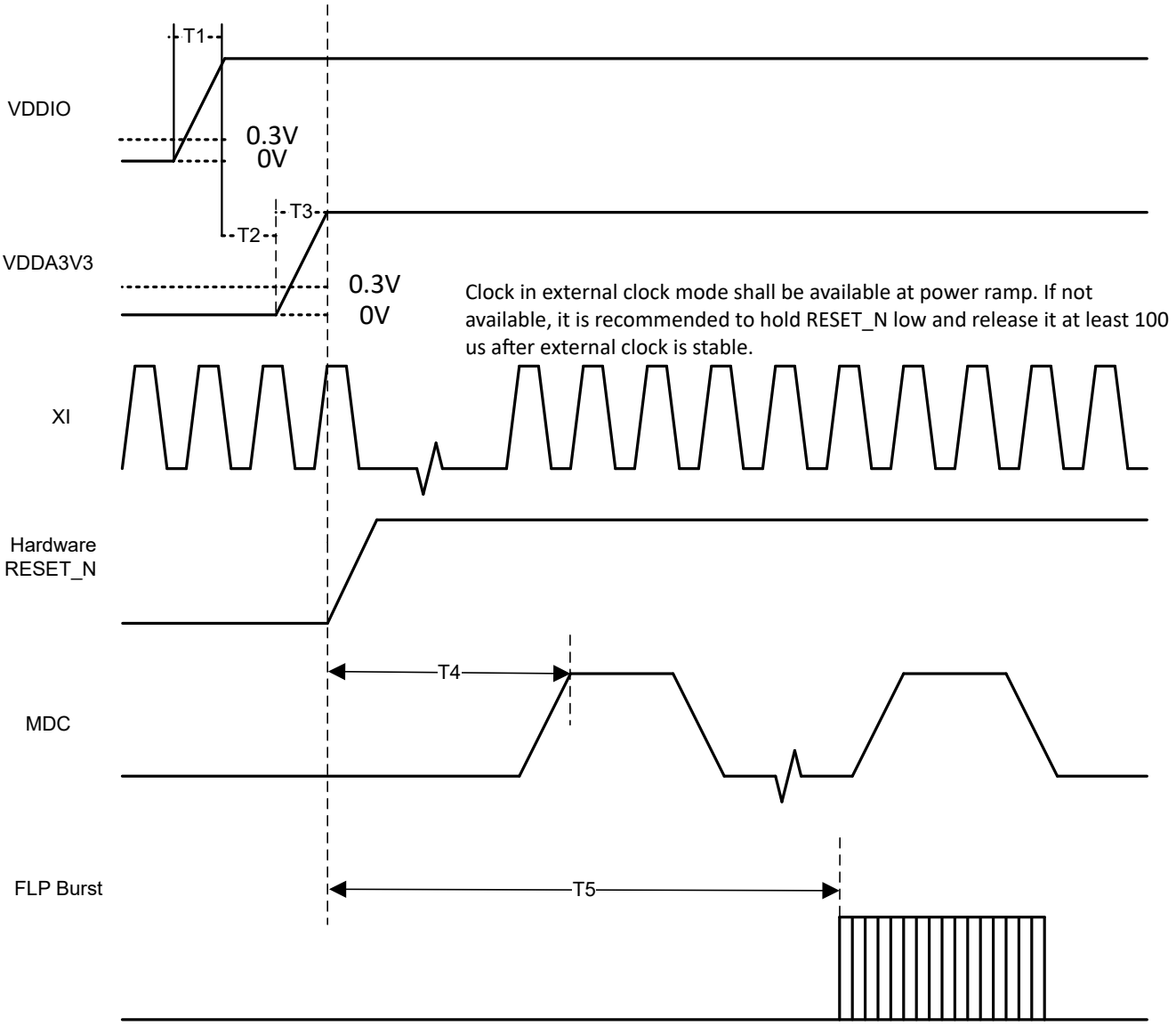


Figure 7-1. Power-Up Timing (Power Sequencing)

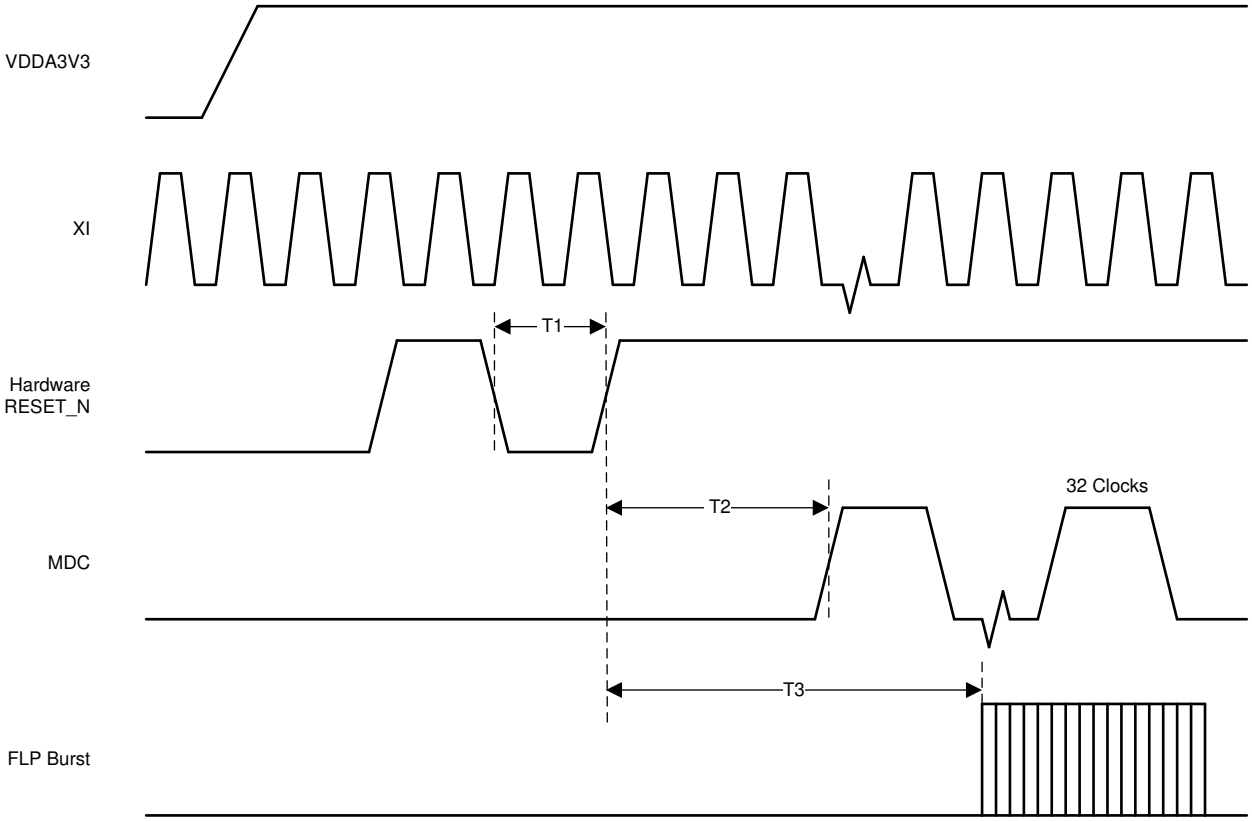


Figure 7-2. Reset Timing (POR)

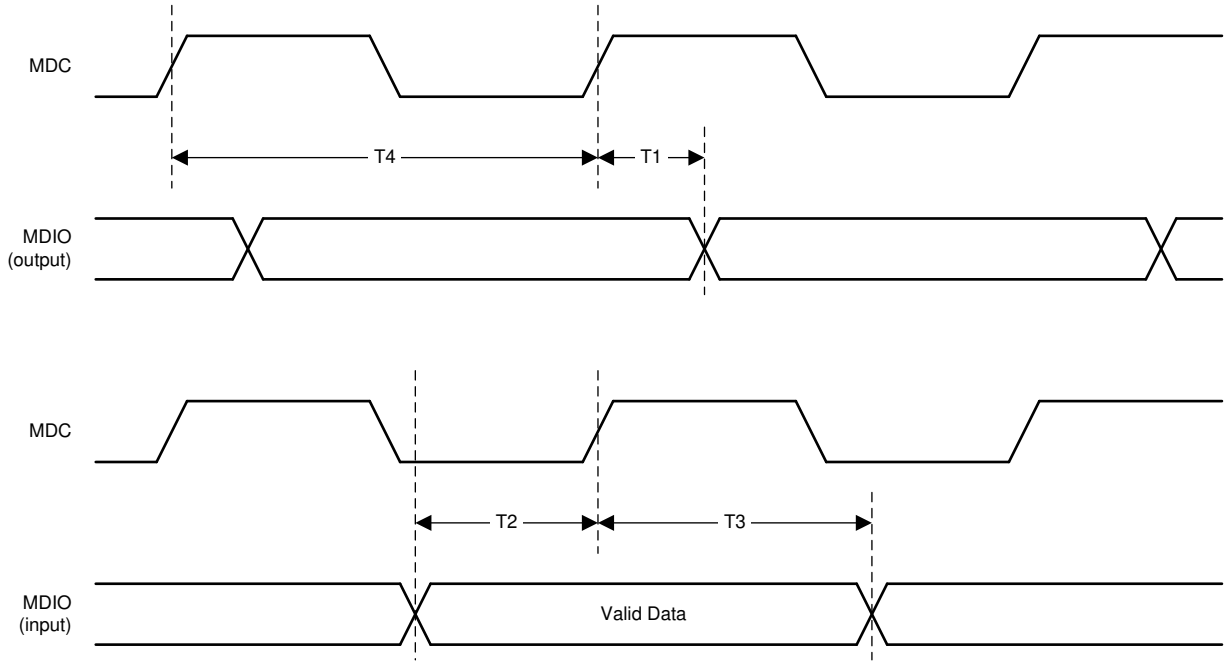


Figure 7-3. Serial Management Timing

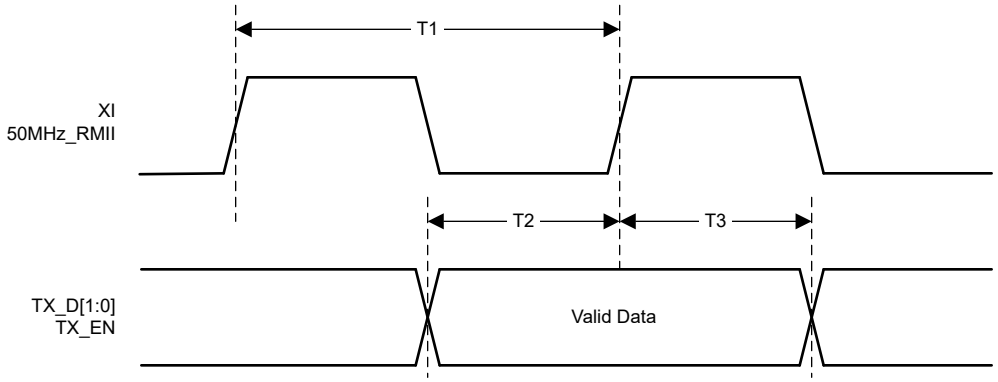


Figure 7-4. RMII Transmit Timing

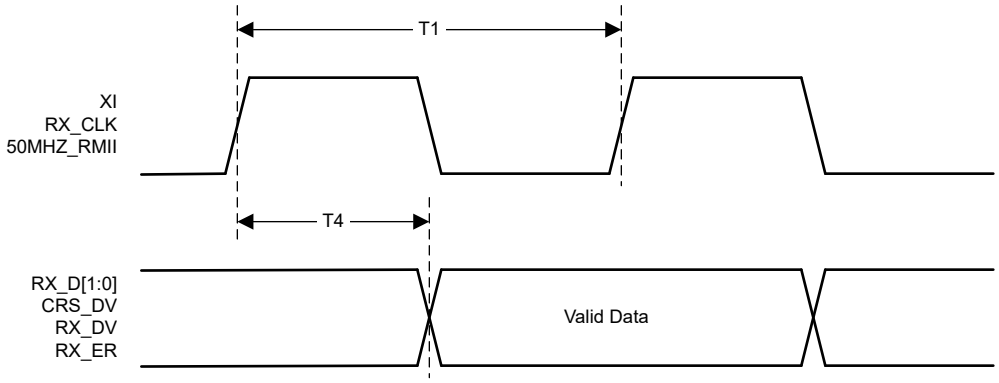


Figure 7-5. RMII Receive Timing

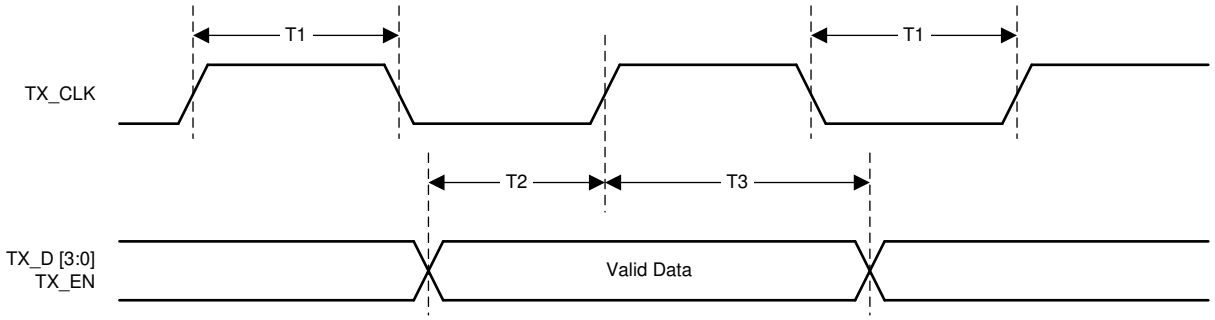


Figure 7-6. 100M MII Transmit Timing

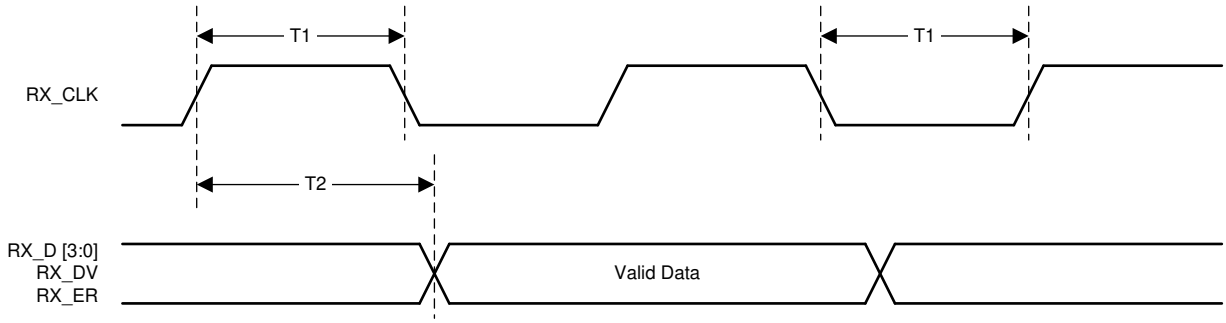


Figure 7-7. 100M MII Receive Timing

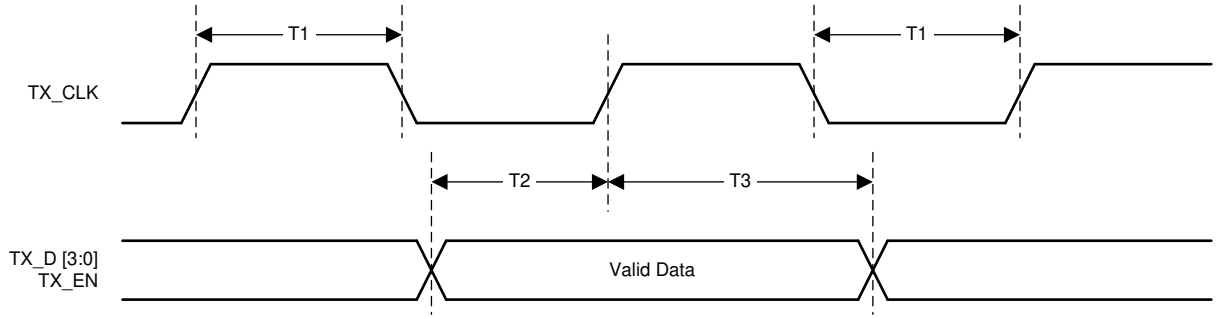


Figure 7-8. 10M MII Transmit Timing

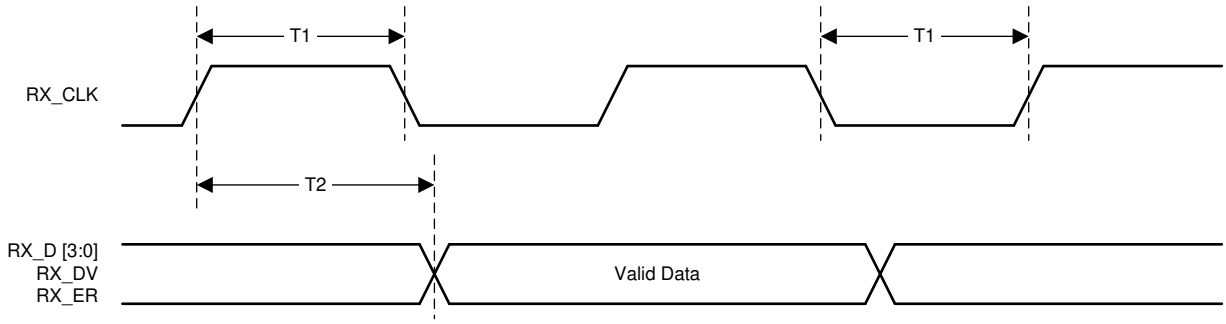


Figure 7-9. 10M MII Receive Timing

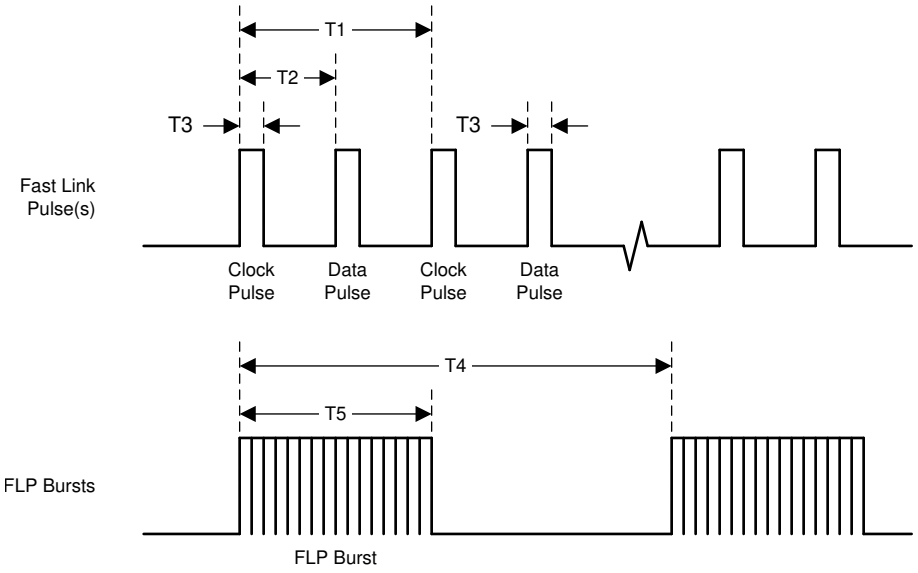


Figure 7-10. Fast Link Pulse Timing

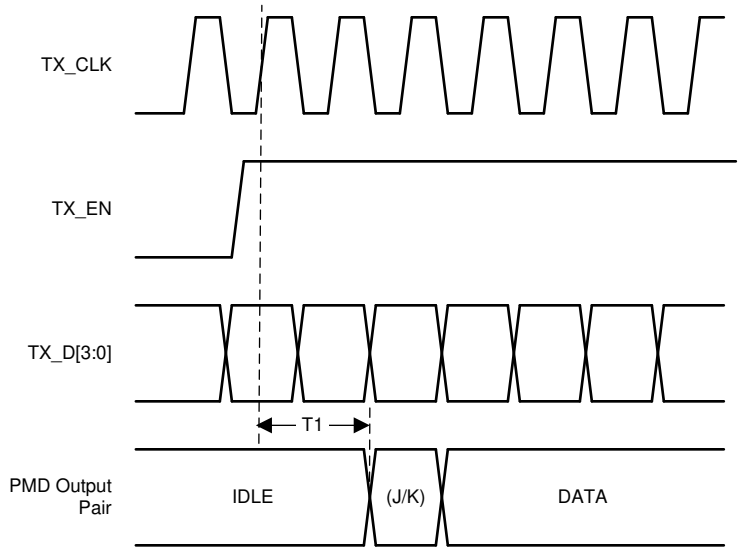


Figure 7-11. 100BASE-TX Transmit Latency Timing

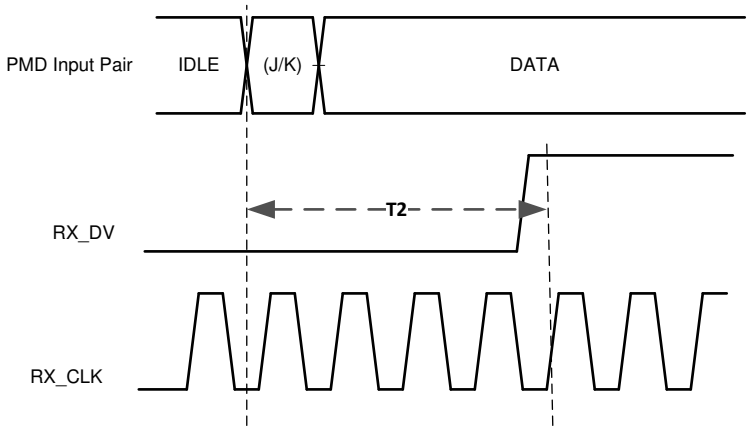


Figure 7-12. 100BASE-TX Receive Latency Timing

7.8 Typical Characteristics

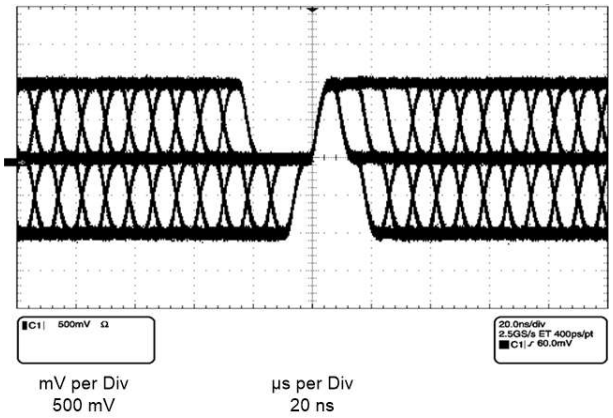


Figure 7-13. 100BASE-TX PMD Eye Waveform

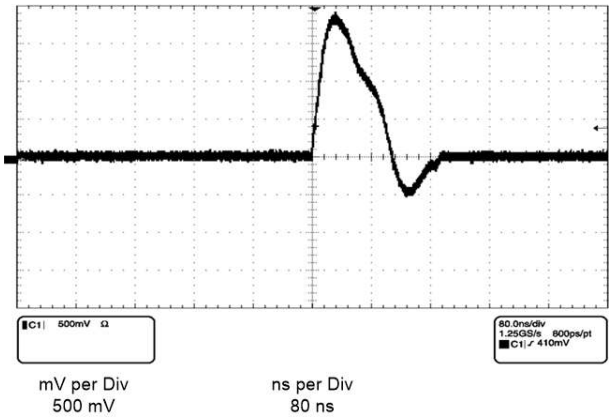


Figure 7-14. 10BASE-Te Link Pulse Waveform

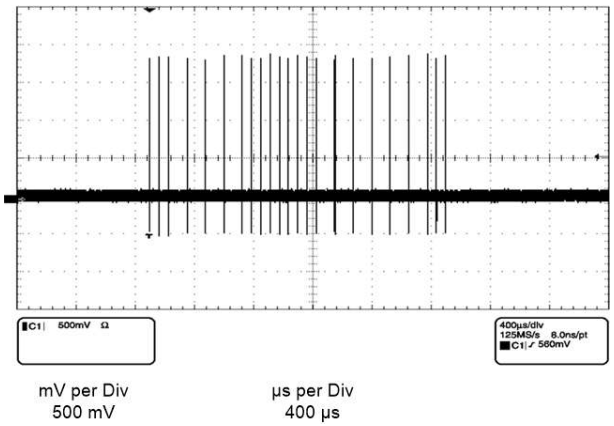


Figure 7-15. Auto-Negotiation Fast Link Pulses Waveform

8 Detailed Description

8.1 Overview

The DP83826 is a single-port physical layer transceiver compliant to IEEE802.3 10BASE-Te and 100BASE-TX standards. The DP83826 is designed to meet stringent Industrial fieldbus applications' needs and offers very low latency, deterministic variation in latency (across reset, power cycle), fixed phase between XI and TX_CLK, low power, and configuration using hardware bootstraps to achieve fast link up. The device supports the standard MII and RMII (Leader mode and Follower mode) for direct connection to the media access controller (MAC). The device dedicated CLKOUT pin can be used to clock other modules on the system. In addition, the PWRDN pin controls the DP83826 link up from power-on-reset (POR) and helps with design of asynchronous power-up of the DP83826 and host system-on-a-chip (SoC) or field-programmable-gate-array (FPGA) controller.

The device operates from a single 3.3V power supply and has an integrated LDO to provide voltage rails needed for internal blocks. The device allows I/O voltage interfaces of 3.3V or 1.8V, which in turn enables the DP83826 to operate as a single-supply PHY. Automatic supply configuration within the DP83826 allows for any combination of VDDIO supply without the need for additional configuration settings.

The DP83826 uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over a CAT5e twisted-pair cable length greater than 150 meters.

DP83826 offers two modes selectable during the power-up sequence using hardware bootstraps.

- BASIC mode
- ENHANCED mode

BASIC mode provides all the features required for standard Ethernet applications, using a common pinout configuration used in many of today's applications simplifying evaluation and testing in existing platforms. The integrated MAC and MDI terminations streamline the design of boards when using the DP83826. All the required clock outputs are generated from a single PLL with a 25MHz external crystal or oscillator input.

Note

For a step-by-step approach on using the DP83826 BASIC mode in existing systems that use a common standard Ethernet pinout, please refer to SNLA338.

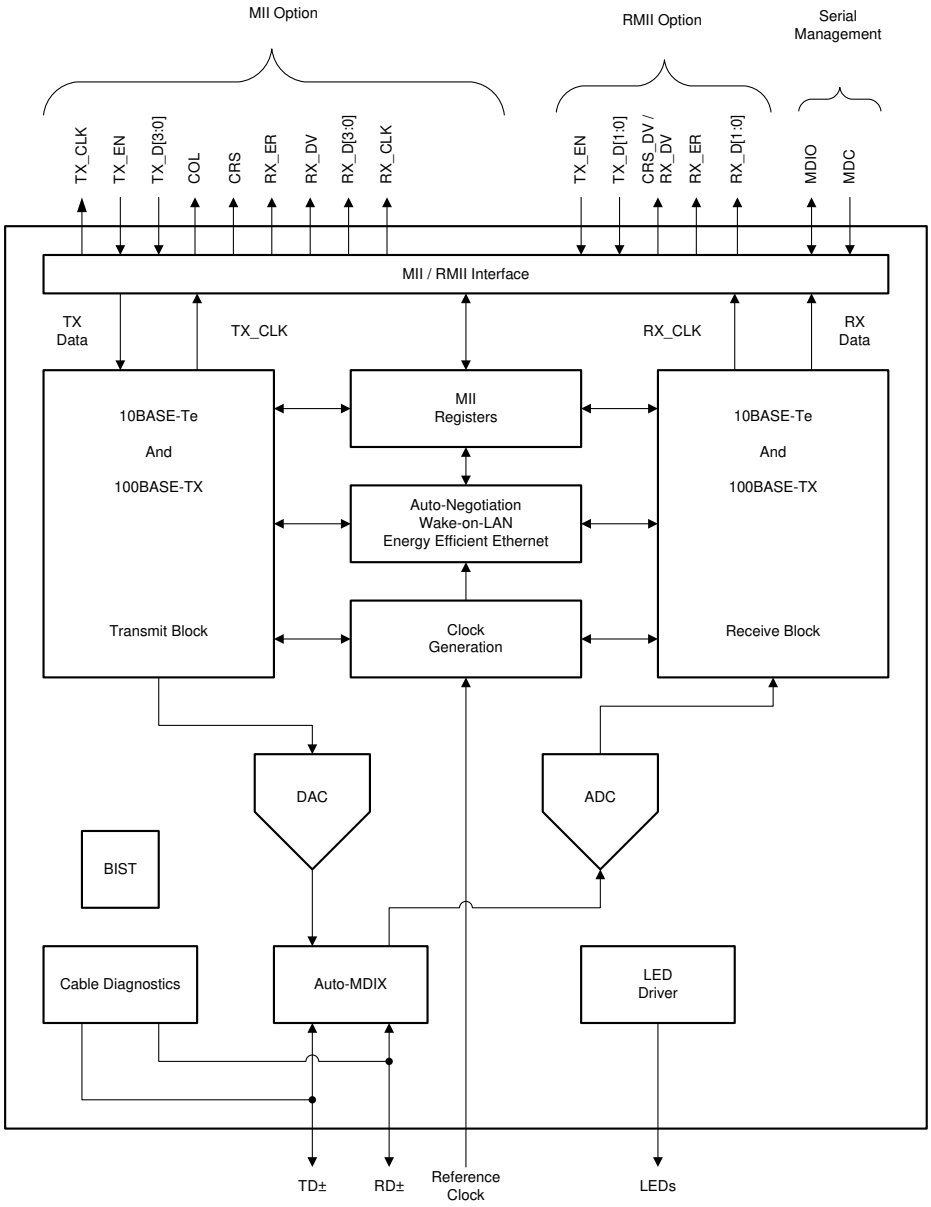
ENHANCED mode includes all the modes of operation described in BASIC Mode, however, the change in pins enable additional features. The DP83826 in ENHANCED Mode can be used for Ethernet fieldbus applications in addition to the standard Ethernet applications. The feature includes:

- Dedicated Reference Clock Output: CLKOUT (pin 31) can be used to synchronize the whole system resulting in lower latency (reduced FIFO on MAC). This clock is enabled at POR and remains available across the reset. This feature also reduces the need for a dedicated clock for other PHYs and the host SoC/FPGA on the board.
- Dedicated HW Strap to use Force Mode, MDI or MDIX for fast link-up from POR and Reset.
- IEEE Power Down Pin: PWRDN (pin 21) helps asynchronous power-up of the DP83826 and host SoC/FPGA control, and can still manage the DP83826 link-up through this dedicated pin.
- PHY address hardware bootstraps on non MAC interface pins to improve Signal Integrity on MII and RMII MAC interface pins.

For pin maps of both modes, refer to section *Section 5* and *Section 6*.

To configure the hardware bootstraps for both modes, refer to sections *Section 8.4.1.1* and *Section 8.4.1.2*.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto-Negotiation (Speed/Duplex Selection)

Auto-Negotiation provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging fast link pulses (FLP). FLPs are burst pulses that provide the information used to communicate the abilities between two devices at each end of a link segment. The DP83826 supports 100BASE-TX and 10BASE-Te modes of operation for auto-negotiation. Auto-negotiation makes sure that the highest common speed is selected based on the advertised abilities of the link partner and the local device. Auto-negotiation can be enabled or disabled in hardware, using the bootstrap, or by register configuration, using bit[12] in the BASIC mode Control Register (BMCR, address 0x0000). For further details regarding auto-negotiation, refer to Clause 28 of the IEEE 802.3 specification.

8.3.2 Auto-MDIX Resolution

The DP83826 can determine if a “straight” or “crossover” cable is used to connect to the link partner. The DP83826 can automatically re-assign to Td (MDI) channel and Rd (MDIX) channel to establish link with the link partner. Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2 and is not a required implementation for 10BASE-Te and 100BASE-TX. Auto-MDIX can also be used when operating the PHY in Force Mode.

Auto-MDIX can be enabled or disabled in hardware, using the hardware bootstrap, or by register configuration, using bit[15] of the PHY Control Register (PHYCR, address 0x0019). When Auto-MDIX is disabled, the PMA is forced to either MDI (“straight”) or MDIX (“crossover”). Manual configuration of MDI or MDIX can also be accomplished using register configuration, using bit[14] of the PHYCR or hardware bootstraps in ENHANCED mode.

8.3.3 Energy Efficient Ethernet

8.3.3.1 EEE Overview

Energy Efficient Ethernet (EEE), defined by IEEE 802.3az, is a capability integrated into Layer 1 (Physical Layer) and Layer 2 (Data Link Layer) to operate in Low Power Idle (LPI) mode. In LPI mode, power is saved during periods of low packet utilization. EEE defines the protocol to enter and exit LPI mode without dropping the link or corrupting packets.

The DP83826 EEE supports 100Mbps and 10Mbps speeds. EEE is supported for both MII and RMII MAC interface. In 10BASE-Te operation, EEE operates with a reduced transmit amplitude that is fully interoperable with a 10BASE-T PHY.

EEE must be enabled through register programming. The steps below describe how to configure the DP83826 for EEE through the MDC/MDIO interface.

Register Address	Data
001Fh	8000h
203Ch	0002h
04D1h	008Bh
04D3h	4F12h
04DFh	0180h
033Eh	A681h
033Fh	0003h
0123h	0800h
031Bh	8848h
0466h	FE00h
04CFh	261Dh
0416h	1F30h
04F5h	2864h
04E0h	FFF2h
031Fh	FE36h
0308h	0000h
04F4h	0800h
0000h	3300h

8.3.3.2 EEE Negotiation

EEE is advertised during auto-negotiation. Auto-Negotiation is performed at power up, on management command, after link failure, or due to user intervention. EEE is supported if and only if both link partners advertise EEE capabilities. If EEE is not supported, all EEE functions are disabled and the MAC must not assert LPI. To advertise EEE capabilities, the PHY needs to exchange an additional formatted next page and unformatted next page in sequence.

EEE Negotiation can be activated using Register Access. IEEE 802.3az defines MMD3 and MMD7 as the locations for EEE control and status registers. The MMD3 registers 0x1014, 0x1001, 0x1016, and MMD7 registers 0x203C and 0x203D contain all the required controls and status indications for operating EEE. The Energy Efficient Ethernet Configuration Register 3 (EEECFG3, address 0x04D1) contains controls for EEE configuration bypass.

By default, EEE capabilities are bypassed. To advertise EEE based on MMD3 and MMD7 registers, EEE capabilities bypass needs to be disabled (0x04D1.0 = 1, 0x04D1.3 = 1) and EEE Advertisement shall be enabled (MMD7 0x203C.1 = 1).

8.3.4 EEE for Legacy MACs Not Supporting 802.3az

The device can be configured to initiate LPI signaling (Idle and Refresh) through register programming as well. This feature enables the system to perform EEE even when the MAC used is not supporting EEE. In this mode, responsibility of enabling and disabling LPI signaling lies on the Host Controller Application. While the *DP83826* is in LPI signaling mode, the application moves the DP83826 into active mode before sending any data over the MAC interface.

The DP83826 does not have buffering capability to store the data while in LPI signaling mode. To enable EEE through register configuration, the following registers must be configured:

1. Enable EEE capabilities by writing 0x04D1.0 = 1, 0x04D1.3 = 1
2. Advertise EEE capabilities during auto-negotiation by writing (MMD7 0x203C.1 = 1)
3. Renegotiate the link by writing 0x0000.9 = 1
4. Forced Tx LPI idles by writing 0x04D1.12 = 1
5. Write 0x04D1.12 = 0 to stop transmitting LPI Idles

8.3.5 Wake-on-LAN Packet Detection

Wake-on-LAN (WoL) provides a mechanism to detect specific frames and notify the connected controller through either register status change, GPIO indication, or an interrupt flag. The WoL feature within the DP83826 device allows for connected devices residing above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. This device supports WoL Magic Packet™ frame type. When a qualifying WoL frame is received, the device WoL logic circuit generates a user-defined event (either pulses or level change) through the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred. The device includes a cycle redundancy check (CRC) gate to prevent invalid packets from triggering a wake-up event. The Wake-on-LAN feature includes:

- Identification of WoL frames in all supported speeds (100BASE-TX and 10BASE-Te)
- Wake-up interrupt generation upon reception of a WoL frame
- CRC error checking of WoL frames to prevent interrupt generation from invalid frames
- Magic Packet technology with SecureOn password protection

8.3.5.1 Magic Packet Structure

When configured for Magic Packet detection, the DP83826 scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which can be the receiving station's IEEE address or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions, followed by Secure-ON password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF.

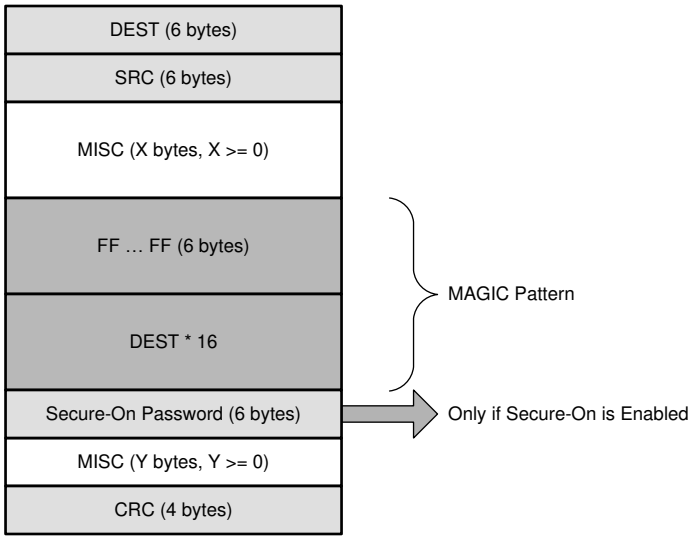


Figure 8-1. Magic Packet Structure

8.3.5.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a SecureOn password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
DESTINATION SOURCE MISC FF FF FF FF FF FF
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

8.3.5.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the Receive Configuration Register (RXFCFG, address 0x04A0). Wake-on-LAN status is reported in the Receiver Status Register (RXFS, address 0x04A1). The Wake-on-LAN interrupt flag configuration and status is located in the MII Interrupt Status Register 2 (MISR2, address 0x0013).

8.3.6 Low Power Modes

The DP83826 device supports three low power modes. This section discusses the principles behind these low power modes and configuration to enable them.

8.3.6.1 Active Sleep

Active sleep mode reduces power consumption when no link partner is connected. The feature can be enabled during initialization of the PHY by writing the correct bit to the PHYSCR register. The feature can be verified by reading the BISCR register.

Once Active Sleep in enabled and when the PHY does not detect a cable connection, the PHY automatically enters active sleep mode. When the device enters this mode, all internal circuitry shuts down except for the SMI circuitry and energy detection circuitry on the TD± and RD± pins. In active sleep mode, the device transmits

normal link pulses (NLP) every 1.4 seconds to check for the presence of a link partner. When a link partner is detected, the PHY automatically switches back to Normal mode, powering the rest of the internal circuitry.

The device enables active sleep mode by setting bits[14:12] = 0b110 in the PHY Specific Control Register (PHYSCR, address 0x0011).

8.3.6.2 IEEE Power-Down

IEEE power-down switch disables all PHY circuitry except the SMI and internal clock circuitry.

IEEE power-down switch can be activated by either register access or through the INTR/PWRDN pin when the pin is configured for power-down function.

To enable IEEE power-down switch through the INTR/PWRDN pin, the pin must be driven LOW to ground.

To enable IEEE power-down switch through the SMI, set bit[11] = 1 in the BASIC mode Control Register (BMCR, address 0x0000).

8.3.6.3 Deep Power Down State

A Deep Power Down state (DPD) disables all PHY circuitry except the SMI. In this mode, the device disables the PHY PLL to further reduce power consumption.

The device uses this sequence to enter DPD state.

1. Enable DPD state (0x0428.2 = 1)
2. Enable IEEE power-down state (pin or 0x0000.11 = 1)

8.3.7 RMII Repeater Mode

The DP83826 device provides the option to enable RMII back-to-back repeater mode functionality to extend cable reach. Two DP83826 devices can be connected in RMII repeater mode without need of any external configuration. The DP83826 provides a hardware strap to configure the CRS_DV pin of RMII interface to RX_DV pin for back-to-back operation. Figure 8-2 and Figure 8-3 show the RMII pin connections that enables the device to operate in repeater mode.

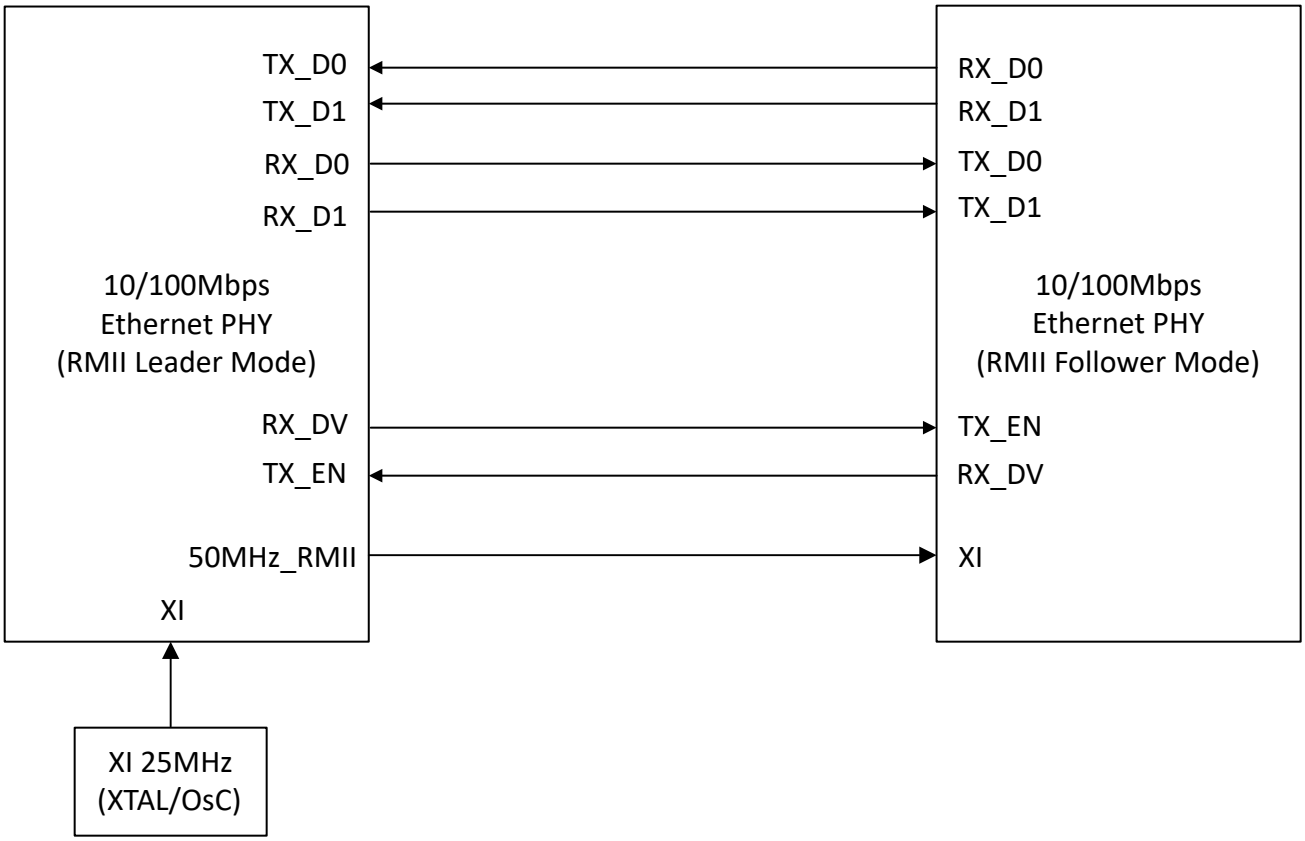


Figure 8-2. RMII Repeater Mode: Leader-Follower

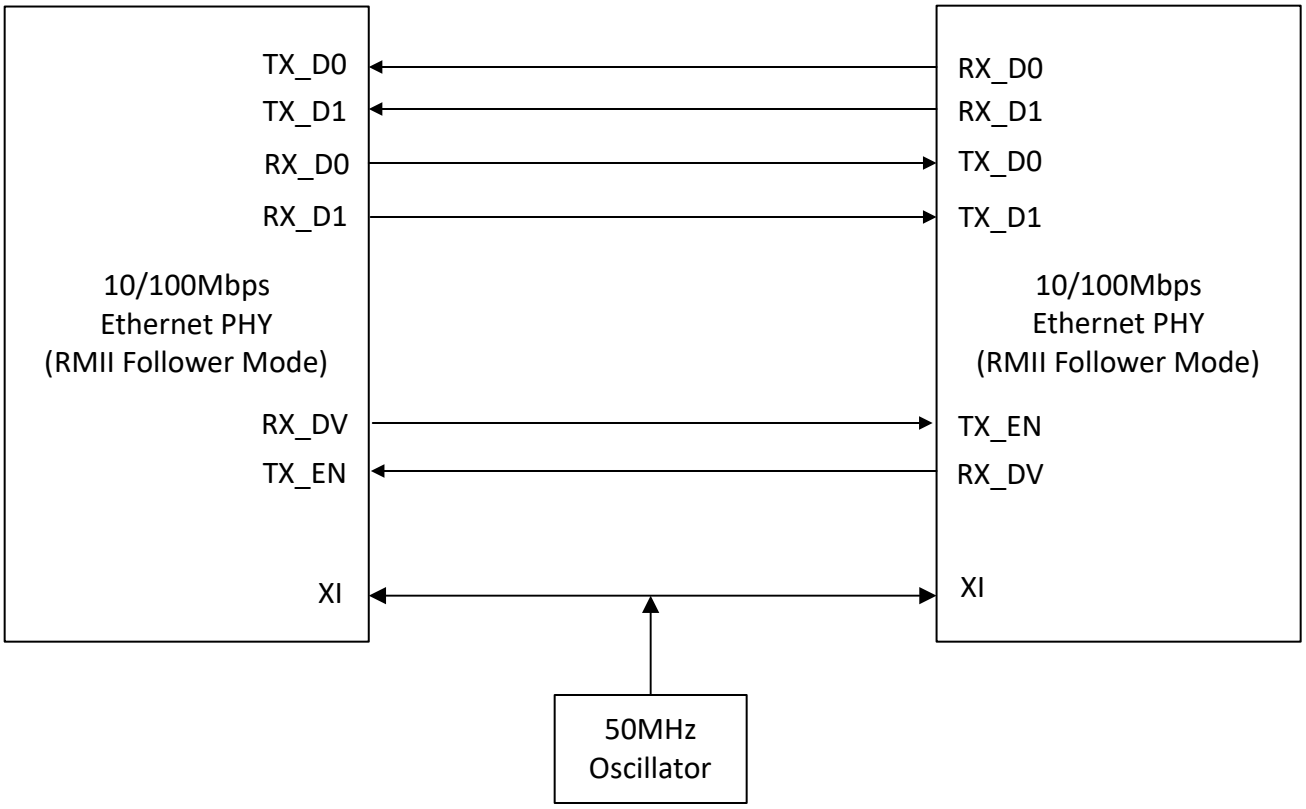


Figure 8-3. RMII Repeater Mode: Follower-Follower

8.3.8 Clock Output

The device has several clock output configuration options. An external crystal or CMOS-level oscillator provides the stimulus for the internal PHY reference clock. The local reference clock acts as the central source for all clocking within the device.

Clock output options supported by the device include:

- MAC IF clock
- XI clock
- Free-running clock
- Recovered clock

MAC IF clock operates at the same rate as the MAC interface selected. For RMII operation, MAC IF Clock frequency is 50MHz.

XI clock is a pass-through option, which allows for the XI pin clock to be passed to a GPIO pin. Note that the clock is buffered prior to transmission out of the GPIOs, and output clock amplitude is at the selected VDDIO level. This clock is available on CLK_OUT/LED1 pin by default after POR release (Refer to T4 in Power-Up Timing).

The Free-running clock is an internally generated 125MHz free-running clock generated by the PLL. The free-running clock is useful for asynchronous data transmission applications.

The recovered clock is a 125MHz recovered clock that is recovered from the connected link partner. The PHY recovers the clock from the data received (transmitted from the link partner).

All clock configuration options are enabled using the LED GPIO configuration registers.

CLKOUT can be disabled by configuring this pin as an input pin via register configuration, register 0x304[2:0].

8.3.9 Media Independent Interface (MII)

The media-independent interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2002 clause 22.

The MII signals are summarized below:

Table 8-1. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_EN
	RX_DV
Line-Status Signals	CRS
	COL
Error Signals	RX_ER

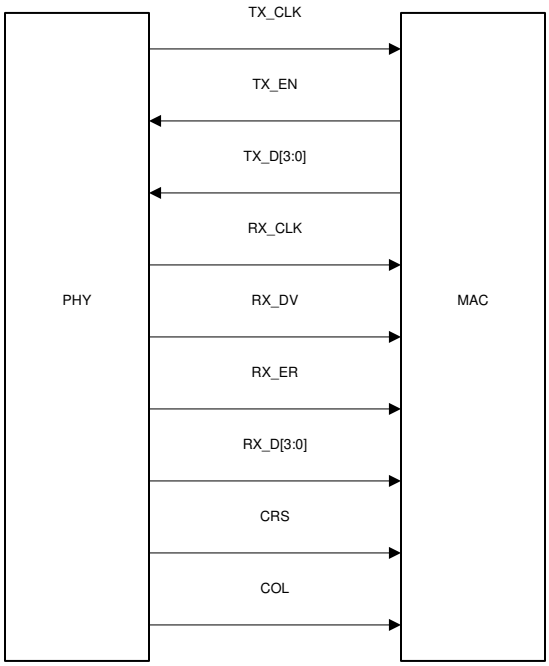


Figure 8-4. MII Signaling

Additionally, the MII interface includes the carrier sense signal (CRS), as well as a collision detect signal (COL). The CRS signal asserts to indicate the reception or transmission of data. The COL signal asserts as an indication of a collision which can occur during half-duplex mode when both transmit and receive operations occur simultaneously.

8.3.10 Reduced Media Independent Interface (RMII)

The DP83826 incorporates the reduced media-independent interface (RMII) as specified in the RMII specification v1.2. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3 MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The DP83826 offers two types of RMII operations: RMII Follower and RMII Leader. In RMII Leader operation, the DP83826 operates from either a 25MHz CMOS-level oscillator connected to XI pin, a 25MHz crystal connected across XI and XO pins. A 50MHz output clock referenced from DP83826 can be connected to the MAC. In RMII Follower operation, the DP83826 operates from a 50MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, in RMII follower mode, the PHY can operate from a 50MHz clock provided by the Host MAC

The RMII specification has the following characteristics:

- Supports 100BASE-TX and 10BASE-Te
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels, the same levels as the MII interface

In this mode, data transfers are 2 bits for every clock cycle using the internal 50MHz reference clock for both transmit and receive paths.

The RMII signals are summarized below:

Table 8-2. RMII Signals

FUNCTION	PINS
Receive data lines	TX_D[1:0]
Transmit data lines	RX_D[1:0]
Receive control signal	TX_EN
Transmit control signal	CRS_DV

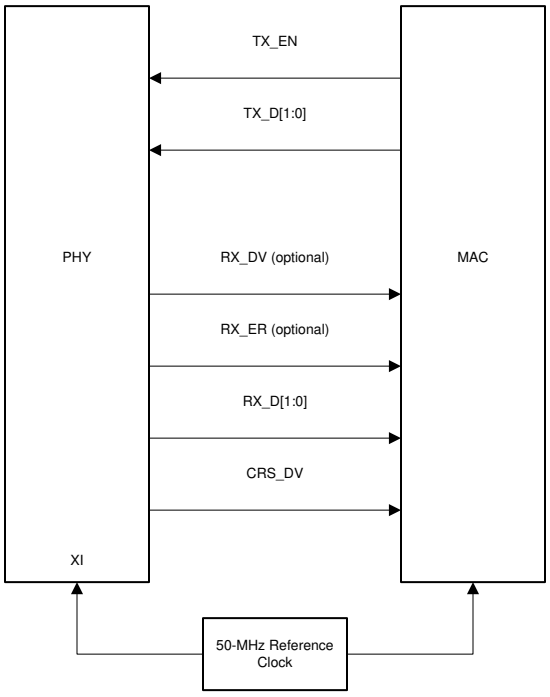


Figure 8-5. RMII Follower Signaling

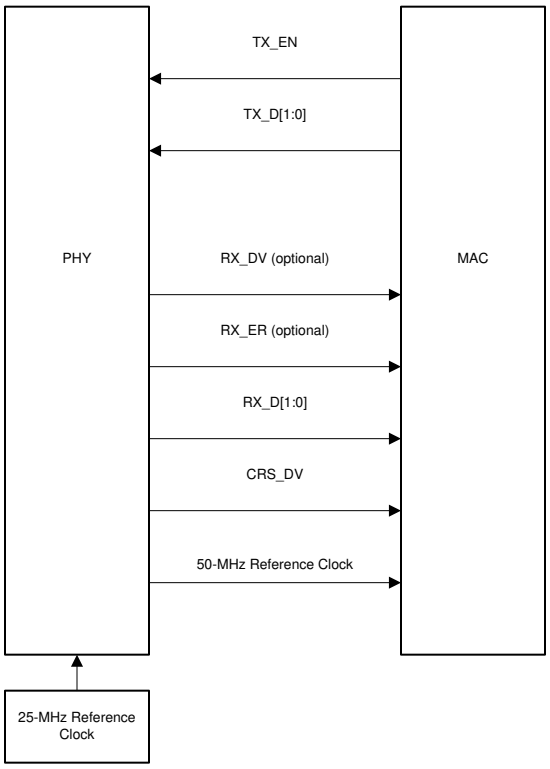


Figure 8-6. RMII Leader Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the 50MHz clock in RMII leader mode and follower mode. Data on RX_D[1:0] is provided in reference to 50MHz clock.

In addition, CRX_DV can be configured as RX_DV signal. This allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication.

8.3.11 Serial Management Interface

The Serial Management Interface provides access to the DP83826 internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83826.

The SMI includes the management clock (MDC) and the management input/output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2KΩ or 1.5KΩ are widely used values), which pulls MDIO high during IDLE and turnaround.

Up to 8 PHYs can share a common SMI bus. To distinguish between the PHYs, during power up or hardware reset, the DP83826 latches the Phy_Address[2:0] configuration pins to determine the address.

The management entity must not start an SMI transaction in the first cycle after power up or hardware reset. To maintain valid operation, the SMI bus must remain inactive at least until 50ms after power-up and at least until 2ms after reset is de-asserted (Refer to T4 in Power-up Timing and T2 in Reset Timing). In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device must actively drive the MDIO signal during the first bit of turnaround. The addressed DP83826 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83826, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 8-3. SMI Protocol

SMI PROTOCOL	<idle><start><op code><PHY address><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

8.3.11.1 Extended Register Space Access

The DP83826 SMI function supports read and write access to the extended register set using the Register Control Register (REGCR, address 0x000D), the Data Register (ADDAR, address 0x000E), and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah draft for Clause 22 for accessing the extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR and register ADDAR, which are accessed only using the normal MDIO transaction. The SMI function ignores indirect access to these registers.

REGCR is the MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of the ADDAR register to the appropriate MMD.

The DP83826 supports three MMD device addresses:

1. The Vendor-Specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.
2. DEVAD[4:0] = 00011 is used for Energy Efficient Ethernet MMD register accesses. Register names for registers accessible at this device address are preceded by MMD3.
3. DEVAD[4:0] = 00111 is used for Energy Efficient Ethernet MMD registers accesses. Register names for registers accessible at this device address are preceded by MMD7.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01).

- ADDAR is the address/data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of the address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111). For register accesses to the MMD3 or MMD7 registers the corresponding device address can be used.

8.3.11.2 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

8.3.11.3 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

8.3.11.4 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

8.3.11.5 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) results in the output of the register set in step 3.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

8.3.11.6 Example Write Operation (No Post Increment)

This example demonstrates a write operation with no post increment. In this example, the MAC impedance is adjusted to 99.25Ω using the IO MUX GPIO Control Register (IOCTRL, address 0x0461).

1. Write the value 0x001F to register 0x000D.
2. Write the value 0x0461 to register 0x000E (sets desired register to the IOCTRL).
3. Write the value 0x401F to register 0x000D.
4. Write the value 0x0400 to register 0x000E (sets MAC impedance to 99.25Ω).

8.3.12 100BASE-TX

8.3.12.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125Mbps serial data stream on the MDI. 4B5B encoding and decoding is detailed in Table 8-4 below.

The transmitter section consists of the following functional blocks:

1. Code-Group Encoder and Injection Block
2. Scrambler Block with Bypass Option
3. NRZ to NRZI Encoder Block
4. Binary to MLT-3 Converter / Common Driver Block

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83826 implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3 Standard, Clause 24.

Table 8-4. 4B5B Code-Group Encoding / Decoding

NAME	PCS 5B CODE-GROUP	MII 4B NIBBLE CODE
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES(1)		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000
J	11000	First Start of Packet - 0101
K	10001	Second Start of Packet - 0101
T	01101	First End of Packet - 0000
R	00111	Second End of Packet - 0000
P	00000	EEE LPI - 0001(2)
INVALID CODES		
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	
V	10000	
V	11001	

(1) Control code-groups I, J, K, T and R in data fields are mapped as invalid codes, together with RX_ER asserted.
(2) Energy Efficient Ethernet LPI must also have TX_ER / RX_ER asserted and TX_EN / RX_DV deasserted.

8.3.12.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 8-4 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of transmit enable (TX_EN) signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of transmit enable).

8.3.12.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the MDI and on the cable can peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is, continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20dB.

8.3.12.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI encoded to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 unshielded twisted pair cable. There is no ability to bypass this block within the DP83826. The NRZI data is sent to the 100Mbps Driver.

8.3.12.1.4 Binary to MLT-3 Converter

The binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a minimal current MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD output pair common driver is slew rate controlled. The slew rate must be considered when selecting AC coupling magnetics to meet TP-PMD standard compliant transition times (3ns < T_{RISE} (and T_{FALL}) < 5ns).

8.3.12.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125Mbps serial data stream to synchronous to 4-bit data provided to the MII and 2-bit wide data to the RMII.

The receive section consists of the following functional blocks:

- Input and BLW compensation
- Signal detect
- Digital adaptive equalization
- MLT-3 to binary decoder
- Clock recovery module
- NRZI to NRZ decoder
- Descrambler
- Serial-to-parallel data conversion
- Code-group alignment
- 4B/5B decoder
- Link integrity monitor
- Bad SSD detection

8.3.13 10BASE-Te

The 10BASE-Te transceiver module is IEEE 802.3 compliant. The transceiver module includes the receiver, transmitter, collision detection, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard.

Note

When using the DP83826 for 10BASE-Te applications, configure VOD_CFG3 (register address: 0x030E) to 0x4A40.

8.3.13.1 Squelch

Squelch is responsible for determining when valid data is present on the differential receive inputs. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-Te standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50ns. Finally, the signal must again exceed the original squelch level no earlier than 50ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

DP83826 supports both IEEE Preamble Mode and Short Preamble Mode. Refer to the 10M_CFG Register (address = 0x2A).

8.3.13.2 Normal Link Pulse Detection and Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-Te standard. Each link pulse is nominally 100ns in duration and transmitted every 16ms in the absence of transmit data. Link pulses are used to check the integrity of the connection with the remote end.

8.3.13.3 Jabber

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the DP83826 output and disables the transmitter if the transmitter attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100ms. When disabled by the Jabber function, the transmitter stays disabled for the entire time that the module's internal transmit enable is asserted. This signal must be de-asserted for approximately 500ms (unjab time) before the Jabber function re-enables the transmit outputs. The Jabber function is only available and active in 10BASE-Te Mode.

8.3.13.4 Active Link Polarity Detection and Correction

Swapping the wires within the twisted-pair causes polarity errors. Wrong polarity affects 10BASE-Te connections. 100BASE-TX is immune to polarity problems because of MLT-3 encoding. 10BASE-Te receive block automatically detects reversed polarity.

8.3.14 Loopback Modes

There are several loopback options within the DP83826 that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83826 can be configured to any one of the Near-end Loopback modes or to the far-end (reverse) loopback mode. MII loopback is configured using the BASIC mode Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100 Mbps and all MAC interfaces).

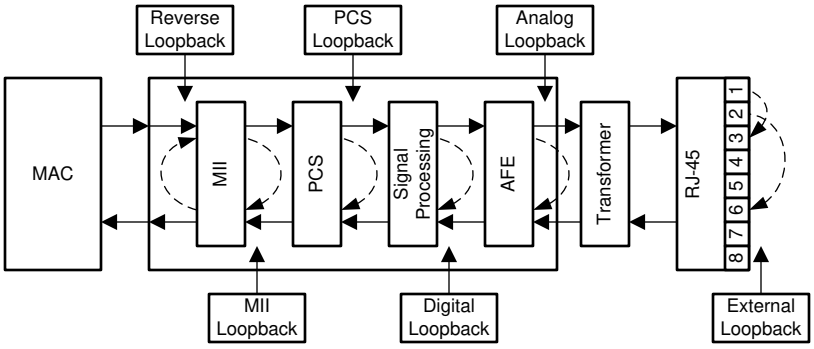


Figure 8-7. Loopback Test Modes

8.3.14.1 Near-end Loopback

Near-end Loopback provides the ability to loop the transmitted data back to the receiver via the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits[3:0] in the BISCR register. Disable Auto-Negotiation before selecting the Near-end Loopback modes. This constraint does not apply for External Loopback Mode.

8.3.14.2 MII Loopback

MII Loopback is the shallowest loop through the PHY and is a useful test mode to validate communications between the MAC and the PHY. When in MII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83826 to the RX pins where the data can be checked by the MAC.

MII Loopback is enabled by setting bit[14] in the BMCR and bit[2] in BISCR.

8.3.14.3 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

PCS Input Loopback is enabled by setting bit[0] in the BISCR.

PCS Output Loopback is enabled by setting bit[1] in the BISCR.

8.3.14.4 Digital Loopback

Digital Loopback includes the entire digital transmit and receive paths. Data is looped back prior to the analog circuitry.

Digital Loopback is requires following configuration:

- 0x0000 = 0x2100 // Disable Auto-Neg
- 0x0016 = 0x0104 // Digital Loopback
- 0x0122 = 0x2000 /
- 0x0123 = 0x2000
- 0x0130 = 0x47FF
- 0x001F = 0x4000 // Soft Reset

8.3.14.5 Analog Loopback

When operating in 10BASE-Te or 100BASE-TX mode, signals can be looped back after the analog front-end.

Analog Loopback is enabled by setting bit[3] in the BISCR.

8.3.14.6 Far-End (Reverse) Loopback

Far-End (Reverse) loopback is a special test mode to allow PHY testing with a link partner. In this mode, data that is received from the Link Partner passes through the PHY's receiver, is looped back at the MAC interface and then transmitted back to the Link Partner. While in reverse loopback mode, all data signals that come from the MAC are ignored.

Reverse Loopback is enabled by setting bit[4] in the BISCR.

8.3.15 BIST Configurations

The DP83826 incorporates an internal PRBS built-in self-test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. The BIST can be performed using both internal loopbacks (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and inter-packet gap (IPG) on the lines. The BIST allows full control of the packet lengths and the IPG.

The BIST packet length is controlled using bits[10:0] in the BIST Control and Status Register #2 (BICSR2, address 0x001C). The BIST IPG length is controlled using bits[7:0] in the BIST Control and Status Register #1 (BICSR1, address 0x001B).

The BIST is implemented with independent transmit and receive paths, with the transmit clock generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for BIST. Received data is compared to the generated pseudo-random data to determine pass/fail status. The number of error bytes that the PRBS checker received is stored in bits[15:8] of the BICSR1. PRBS lock status and sync can be read from the BIST Control Register (BISCR, address 0x0016).

The PRBS test can be put in a continuous mode by using bit[14] in the BISCR. In continuous mode, when the BIST error counter reaches the maximum value, the counter starts counting from zero again. To read the BIST error count, bit[15] in the BICSR1 must be set to '1'. This setting locks the current value of the BIST errors for reading. Setting bit[15] also clears the BIST Error Counter.

8.3.16 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for a reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies and connectors deployed results in the need to non-intrusively identify and report cable faults. The DP83826 offers time domain reflectometry (TDR) capabilities in the Cable Diagnostic tool kit.

8.3.16.1 Time Domain Reflectometry (TDR)

The DP83826 uses TDR to determine the quality of the cables, connectors and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts and any other discontinuities along the cable.

The DP83826 transmits a test pulse of known amplitude (1V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, connector and from the end of the cable. After the pulse transmission, the DP83826 measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors) and improperly terminated cables with ±1 meter accuracy.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the following scenarios:

- While the link partner is disconnected – cable is unplugged at the other side
- Link partner is connected but remains “quiet” (for example, in power down mode)
- TDR can be automatically activated when the link fails or is dropped

TDR Auto-Run can be enabled by using bit[8] in the Control Register #1 (CR1, address 0x0009). When a link-drops, TDR automatically executes and stores the results in the respective TDR Cable Diagnostic Location Result Registers #1 - #5 (CDLRR, addresses 0x0180 to 0x0184) and the Cable Diagnostic Amplitude Result Registers #1 - #5 (CDLAR, addresses 0x0185 to 0x0189). TDR can also be run manually using bit[15] in the Cable Diagnostic Control Register (CDCR, address 0x001E). Cable diagnostic status is obtained by reading bits[1:0] in the CDCR. Additional TDR functions including cycle averaging and crossover disable can be found in the Cable Diagnostic Specific Control Register (CDSCR, address 0x0170). Refer to the application report *Time Domain Reflectometry with DP83826* for details.

8.3.17 Fast Link-Drop Functionality

The DP83826 includes advanced link-drop capabilities that support various real-time applications. The link-drop mechanism is configurable and includes enhanced modes that allow extremely fast link-drop reaction times.

The DP83826 supports an enhanced link-drop mechanism, also called fast link-drop (FLD), which shortens the observation window for determining link. There are multiple ways of determining link status, which can be enabled or disabled based on user preference.

Depending on what mode the DP83826 is in, the default state of FLD differs. In ENHANCED mode, FLD and all the detection mechanisms are disabled by default through pulling down Strap7. For EtherCAT applications or applications with Fast link drop enabled and expect to handle Baseline wander packets, recommend disable signal energy detect, which can be done by setting Strap8. The table below summarizes the modes enabled by strap.

Table 8-5. FLD Detection Modes by Strap in ENHANCED Mode

Strap Configuration	RX Error Count	MLT3 Error Count	Low SNR Threshold	Signal/Energy Loss	Descrambler Link Loss
(Default) Strap7 = LOW Strap1 = X Strap8 = X	Disabled	Disabled	Disabled	Disabled	Disabled
Strap7 = HIGH Strap1 = HIGH Strap8 = LOW	Enabled		Enabled	Enabled	Enabled
Strap7 = HIGH Strap1 = LOW Strap8 = LOW	Enabled		Disabled	Enabled	Disabled
Strap7 = HIGH Strap1 = LOW Strap8 = HIGH	Enabled		Disabled	Disabled	Disabled

In BASIC mode, fast link-drop is enabled by default. The default mechanisms in BASIC mode is RX error and signal/energy loss.

In both modes, FLD can be configured using the Control Register 3 (CR3, register address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled. When link-drop occurs, indication of a particular fault condition can be read from the Fast Link Drop Status Register (FLDS, register address 0x000F).

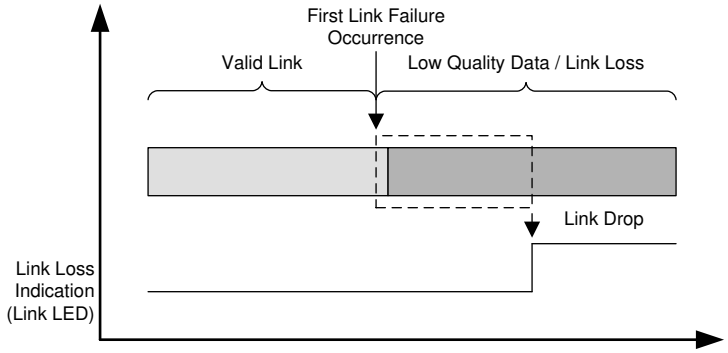


Figure 8-8. Fast Link-Drop

Fast link-drop criteria include:

- RX error count - when a predefined number of 32 RX_ERs occur in a 10µs window, the link is dropped.
- MLT3 error count - when a predefined number of 20 MLT3 errors occur in a 10µs window, the link is dropped. To use the MLT3 error based FLD, please configure register Fast Link Drop Config Register 1 (FLDCFG1, register address 0x0117) to 0x0417.
- Low SNR threshold - when a predefined number of 20 threshold crossings occur in a 10µs window, the link is dropped.
- Signal/energy loss - when the energy detector indicates energy loss, the link is dropped.
- Descrambler link loss - when the Descrambler loses lock, the link is dropped. To use the Descrambler link loss based FLD, please configure bits[5:0] of Fast Link Drop Config Register 2 (FLDCFG2, register address 0x0131) to 0x08.

The fast link-drop functionality allows the use of each of these options separately or in any combination.

8.3.18 LED and GPIO Configuration

The DP83826 offers flexible LED and GPIO pins which can be set for various functions using register configuration. Refer to Figure 8-9, for details on LED and GPIO configuration.

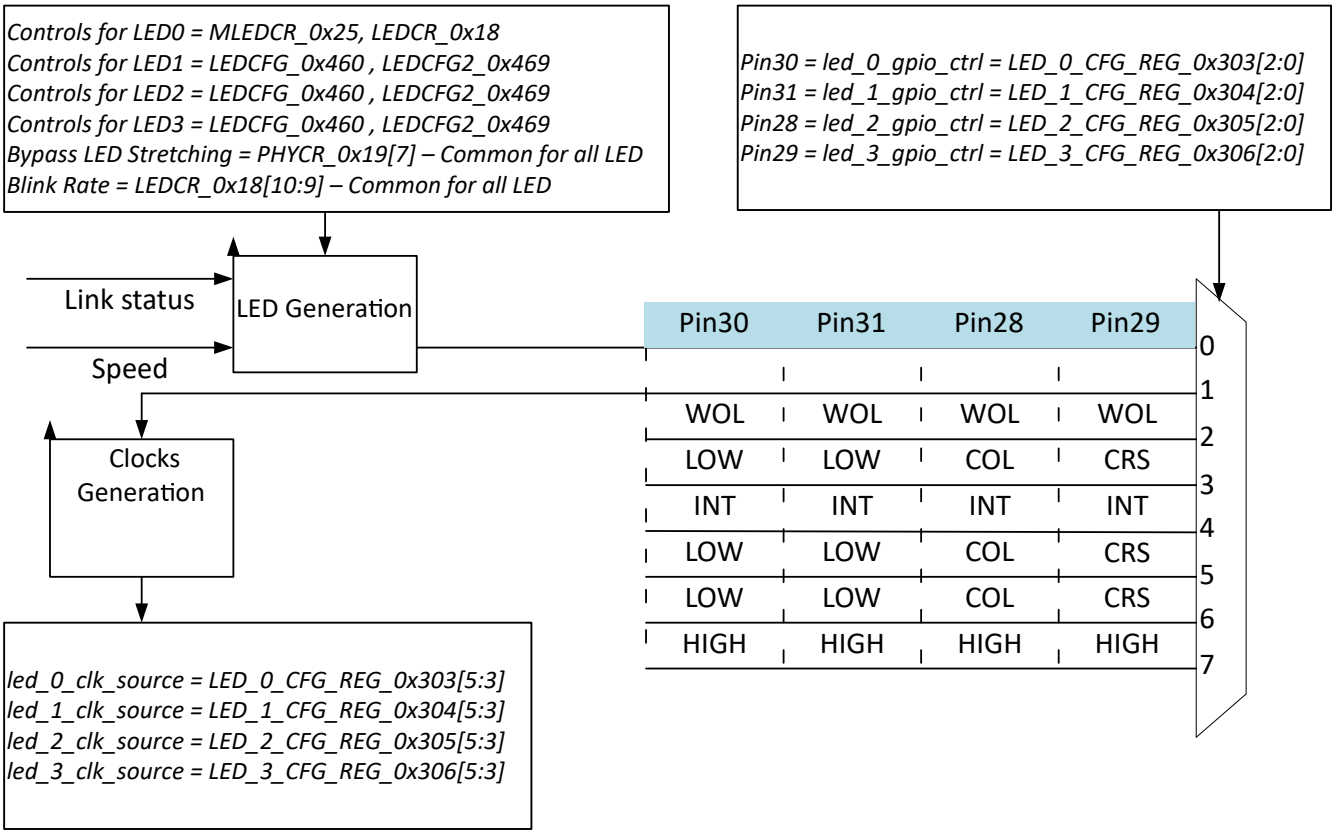


Figure 8-9. LED and GPIO Configuration

Note

A clock output is available on Pin 28 and 29 in ENHANCED mode only. These pins can be configured to output only a 25MHz or 50MHz clock.

In ENHANCED mode, the LEDs have auto-polarity detection. The LED drive adjusts according to the strap configured on the pin. For example, if the LED pin is configured for a pull-down strap, then the PHY assigns the LED polarity as active high. If the LED pin is configured with a pull-up, the PHY assigns the LED polarity as active low.

In BASIC mode, the LED polarity is always be active low. In the case that the LED pin must be strapped low, a 1kΩ pull-up resistor in series with the LED must be used and a 1.5kΩ pull-down resistor. This results in the strap selecting 0. Please note that using higher resistance can decrease the brightness of the LED.

Figure 8-10 shows the two proper ways of connecting LEDs directly to the DP83826.

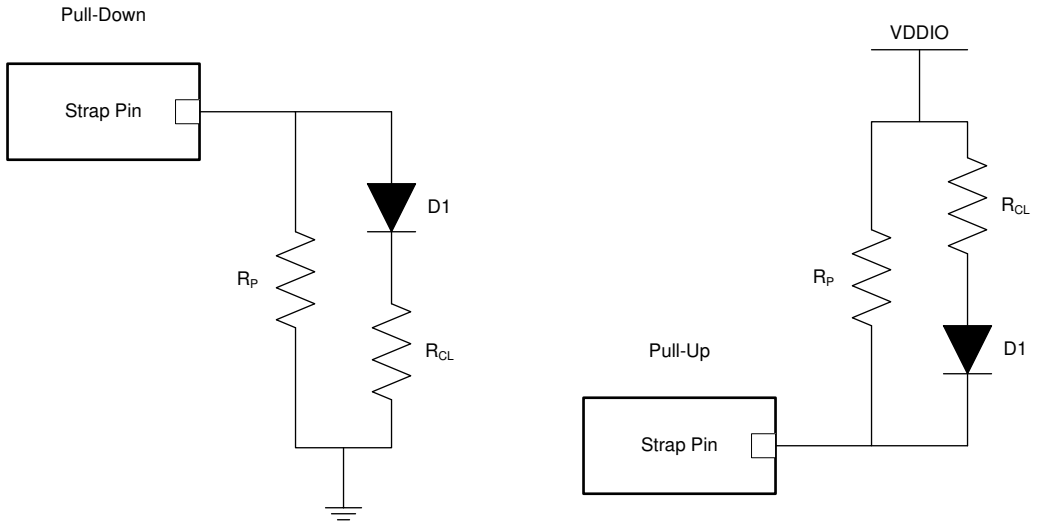


Figure 8-10. Example LED Strap Connections

8.4 Programming

The DP83826 provides hardware based configuration (via bootstraps) and the IEEE defined register set for programming and status indications. The DP83826 also provides an additional register set to configure other features not supported through IEEE registers.

8.4.1 Hardware Bootstraps Configuration

DP83826 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below. Configuration of the device can be done through the strap pins or through the management register interface. A pullup resistor or a pulldown resistor of suggested values is used to set the voltage ratio of the strap pin input and the supply to select one of the possible selected modes. All strap pins have two levels.

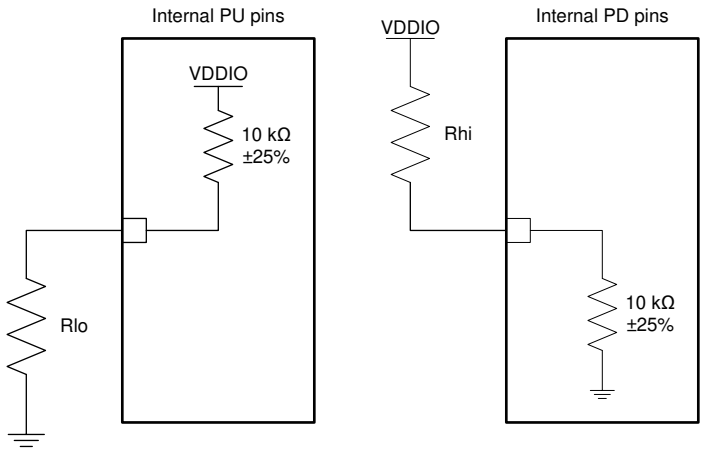


Figure 8-11. Strap Circuit

Table 8-6. 2-Level Strap Resistor Ratios

Mode (1)	SUGGESTED RESISTORS	
	R_{HI} (kΩ)	R_{LO} (kΩ)
INTERNAL 10kΩ PULLDOWN (PD) PINS		
0-DEFAULT	OPEN	OPEN
1	2.49	OPEN
INTERNAL 10kΩ PULLUP (PU) PINS		
0	OPEN	1.5
1-DEFAULT	OPEN	OPEN

(1) Resistor ratios are only a recommendation. Use the bootstrap threshold values contained within the Electrical Characteristics table for more precise mode selections. Recommended tolerance is 1%.

8.4.1.1 Bootstrap Configurations (ENHANCED Mode)

This section describes the hardware bootstraps available for some options for DP83826's Enhanced Mode. If no strap resistors are implemented, the default value is Odd Nibble Enabled, MII mode, FLD disabled. '0' corresponds to Mode 0 while '1' corresponds to Mode 1.

FLD feature only supported when DP83826 is configured for MII MAC interface. MII is selected when either Strap1 = '0' or when Strap1 = '1' and Strap8 = '0' as depicted in Table 8-7and Table 8-8.

RX_D0, RX_D1, RX_DV, RX_ER, LED0, CRS/LED3, COL/LED2 strapping is independent of this flowchart.

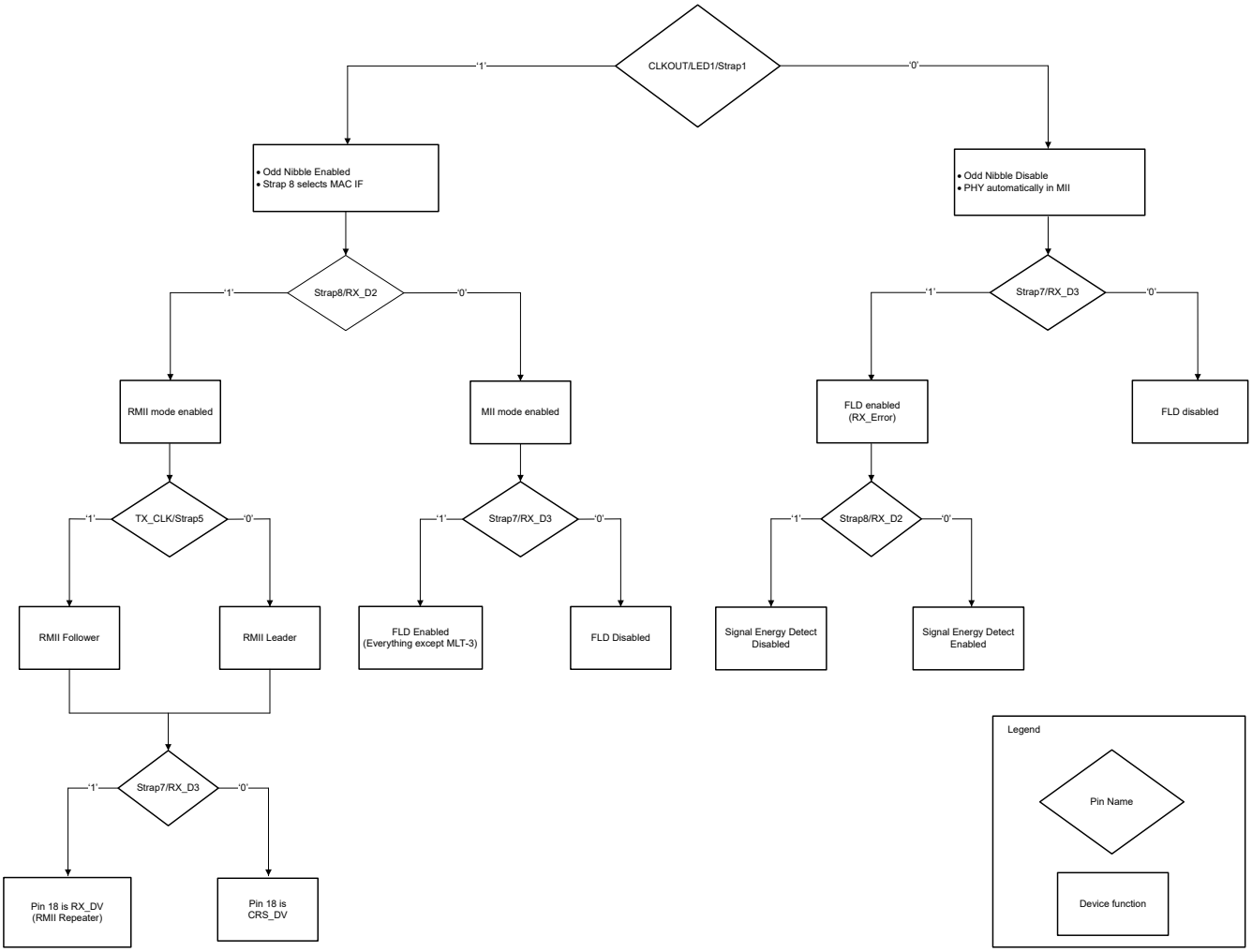


Figure 8-12. Enhanced Bootstrap Flowchart

Table 8-7. Odd Nibble Detection Bootstrap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
CLKOUT/LED1	Strap1 (Latched at POR only. HW reset does not re-latch this strap)	31	1	0	• Odd Nibble Detection disabled • MAC IF fixed to MII • If Strap7 = 1, only RX_Error and Signal Energy detect is enabled for FLD.
				1	• Odd Nibble Detection enabled • MAC IF (MII or RMII) determined by Strap8

Table 8-8. MAC Mode Selection Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D2	Strap8	14	0	0	MII MAC mode ALT. Function: When Strap1 =0 AND Strap7 =1, Signal Energy Detect enabled
				1	RMII MAC mode ALT. Function: When Strap1 =0 AND Strap7 =1, Signal Energy Detect disabled

Table 8-9. MII MAC Mode Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D3	Strap7	13	0	0	Fast link-drop disable
				1	Fast link-drop enable. Refer to Table 8-5 for FLD strap options. All available mechanisms is enabled except MLT3_Error.

Table 8-10. RMII MAC Mode Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
TX_CLK	Strap5	22	0	0	RMII leader mode
				1	RMII follower mode
RX_D3	Strap7	13	0	0	RMII_CRS_DV
				1	RMII_RX_DV (for RMII repeater mode)

Table 8-11. Auto_Neg Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D1	Strap9	15	0	0	auto MDIX enable
				1	auto MDIX disable
RX_D0	Strap0	16	0	0	auto-negotiation enable
				1	auto negotiation disable. force mode 100M enabled
RX_DV	Strap10	18	0	0	MDIX (applicable only when auto-MDIX is disabled)
				1	MDI (applicable only when auto-MDIX is disabled)

Table 8-12. CLKOUT/LED1 Bootstrap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_ER	Strap6 (Latched at POR only. HW reset does not re-latch this strap)	20	0	0	CLKOUT 25MHz on Pin 31
				1	LED1 on Pin 31

Table 8-13. PHY Address Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED0	Strap2	30	0		PHY_ADD0
				0	0
				1	1
CRS/LED3	Strap3	29	0		PHY_ADD1
				0	0
				1	1
COL/LED2	Strap4	28	0		PHY_ADD2
				0	0
				1	1

8.4.1.2 Strap Configuration (BASIC Mode)

This section describes the strap configuration available for BASIC mode.

Table 8-14. PHY Address Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D3	Strap7	13	1		PHY_ADD0
				0	1
				1	0
RX_D2	Strap8	14	0		PHY_ADD1
				0	0
				1	1
RX_D1	Strap9	15	0		PHY_ADD2
				0	0
				1	1

Table 8-15. MAC Mode Selection Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Strap10	Strap4	Function
COL	Strap4	28	0	0	0	MII MAC mode
				0	1	RMII leader mode
				1	1	RMII follower mode
RX_DV	Strap10	18	0	Other values are reserved. Do not use.		
CRS[1]	Strap3	29	0			

Table 8-16. Auto Negotiation Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED0	Strap2	30	1	0	Auto Negotiation Disable
				1	Auto Negotiation Enable

Table 8-17. Speed Strap

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED1/ TX_ER	Strap1	31	1	0	Speed 10M
				1	Speed 100M

Table 8-18. Full/Half Duplex

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D0	Strap0	16	1	0	Full Duplex
				1	Half Duplex

Table 8-19. MII Isolate Bootstraps

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_ER	Strap6	20	0	0	MII Isolate Disable
				1	MII Isolate Enable

[1] CRS strap is reserved. Do not connect this pin to supply via PU resistor.

8.5 Register Maps

8.5.1 DP83826 Registers

Table 8-20 lists the memory-mapped registers for the DP83826 registers. All register offset addresses not listed in Table 8-20 should be considered as reserved locations and the register contents should not be modified.

Table 8-20. DP83826 Registers

Offset	Acronym	Register Name	Section
0h	BMCR Register	Basic Mode Control Register	Go
1h	BMSR Register	Basic Mode Status Register	Go
2h	PHYIDR1 Register	PHY Identifier Register #1	Go
3h	PHYIDR2 Register	PHY Identifier Register #2	Go
4h	ANAR Register	Auto-Negotiation Advertisement Register	Go
5h	ALNPAR Register	Auto-Negotiation Link Partner Ability Register	Go
6h	ANER Register	Auto-Negotiation Expansion Register	Go
7h	ANNPTR Register	Auto-Negotiation Next Page Register	Go
8h	ANLNPTR Register	Auto-Negotiation Link Partner Ability Next Page Register	Go
9h	CR1 Register	Control Register #1	Go
Ah	CR2 Register	Control Register #2	Go
Bh	CR3 Register	Control Register #3	Go
Dh	REGCR Register	Extended Register Control Register	Go
Eh	ADDAR Register	Extended Register Data Register	Go
Fh	FLDS Register	Fast Link Down Status Register	Go
10h	PHYSTS Register	PHY Status Register	Go
11h	PHYSCR Register	PHY Specific Control Register	Go
12h	MISR1 Register	MII Interrupt Status Register #1	Go
13h	MISR2 Register	MII Interrupt Status Register #2	Go
14h	FCSCR Register	False Carrier Sense Counter Register	Go
15h	RECR Register	Receive Error Count Register	Go
16h	BISCR Register	BIST Control Register	Go
17h	RCSR Register	RMII and Status Register	Go
18h	LEDCR Register	LED Control Register	Go
19h	PHYCR Register	PHY Control Register	Go
1Ah	10BTSCR Register	10Base-Te Status/Control Register	Go
1Bh	BICSR1 Register	BIST Control and Status Register #1	Go
1Ch	BICSR2 Register	BIST Control and Status Register #2	Go
1Eh	CDCR Register	Cable Diagnostic Control Register	Go
1Fh	PHYRCR Register	PHY Reset Control Register	Go
25h	MLEDCR Register	Multi-LED Control Register	Go
27h	COMPT Regsiter	Compliance Test Register	Go
2Ah	10M_CFG		Go
117h	FLD_CFG1		Go
131h	FLD_CFG2		Go
170h	CDSCR Register	Cable Diagnostic Specific Control Register	Go
171h	CDSCR2 Register	Cable Diagnostic Specific Control Register 2	Go
173h	CDSCR3 Register	Cable Diagnostic Specific Control Register 3	Go
175h	TDR_175 Register	TDR Control Register #1	Go

Table 8-20. DP83826 Registers (continued)

Offset	Acronym	Register Name	Section
176h	TDR_176 Register	TDR Control Register #2	Go
177h	CDSCR4 Register	Cable Diagnostic Specific Control Register 4	Go
178h	TDR_178 Register	TDR Control Register #3	Go
180h	CDLRR1 Register	Cable Diagnostic Location Result Register #1	Go
181h	CDLRR2 Register	Cable Diagnostic Location Result Register #2	Go
182h	CDLRR3 Register	Cable Diagnostic Location Result Register #3	Go
183h	CDLRR4 Register	Cable Diagnostic Location Result Register #4	Go
184h	CDLRR5 Register	Cable Diagnostic Location Result Register #5	Go
185h	CDLAR1 Register	Cable Diagnostic Amplitude Result Register #1	Go
186h	CDLAR2 Register	Cable Diagnostic Amplitude Result Register #2	Go
187h	CDLAR3 Register	Cable Diagnostic Amplitude Result Register #3	Go
188h	CDLAR4 Register	Cable Diagnostic Amplitude Result Register #4	Go
189h	CDLAR5 Register	Cable Diagnostic Amplitude Result Register #5	Go
18Ah	CDLAR6 Register	Cable Diagnostic Amplitude Result Register #6	Go
218h	MSE_Val		Go
302h	IO_CFG1 Register	GPIO Pin configuration Register #1	Go
303h	LED0_GPIO_CFG		Go
304h	LED1_GPIO_CFG		Go
305h	LED2_GPIO_CFG		Go
306h	LED3_GPIO_CFG		Go
308h	CLK_OUT_LED_STATUS register	CLK_OUT_LED_STATUS configuration Register #3	Go
30Bh	VOD_CFG1 Register	VoD Config Register #1	Go
30Ch	VOD_CFG2 Register	VoD Config Register #2	Go
30Eh	VOD_CFG3 Register	VoD Config Register #3	Go
404h	ANA_LD_PROG_SL Register	Line Driver Config Register	Go
40Dh	ANA_RX10BT_CTRL Register	Receive Configuration Register 10M	Go
456h	GENCFG Register	General Configuration Register	Go
460h	LEDCFG Register	LEDs Configuration Register #1	Go
461h	IOCTRL Register	IO MUX GPIO Control Register	Go
467h	SOR1 Register	Strap Latch-In Register #2	Go
468h	SOR2 Register	Strap Latch-In Register #2	Go
469h	LEDCFG2 Register	LEDs Configuration Register #2	Go
4A0h	RXFCFG1 Register	Receive Configuration Register #1	Go
4A1h	RXFS Register	Receive Status Register	Go
4A2h	RXFPMD1 Register	Receive Perfect Match Data Register #1	Go
4A3h	RXFPMD2 Register	Receive Perfect Match Data Register #2	Go
4A4h	RXFPMD3 Register	Receive Perfect Match Data Register #3	Go
4A5h	RXFSOP1 Register	Receive Secure-ON Password Register #1	Go
4A6h	RXFSOP2 Register	Receive Secure-ON Password Register #2	Go
4A7h	RXFSOP3 Register	Receive Secure-ON Password Register #3	Go

Complex bit access types are encoded to fit into small table cells. Table 8-21 shows the codes that are used for access types in this section.

Table 8-21. DP83826 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RCH	R C H	Read to Clear Set or cleared by hardware
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0C	W 0C	Write 0 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

8.5.1.1 BMCR Register (Offset = 0h) [Reset = XX00h]

BMCR Register is shown in Table 8-22.

Return to the Summary Table.

Basic Mode Control Register

Table 8-22. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reset	RH/W1S	0h	PHY Software Reset: Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is completed,, this bit is cleared to 0 automatically. PHY Vendor Specific registers are not cleared. 0h = Normal Operation 1h = Initiate software Reset / Reset in Progress
14	MII Loopback	R/W	0h	MII Loopback: When MII loopback mode is activated, the transmitted data presented on MII TXD is looped back to MII RXD internally. Additionally set following additional bit BISCR 0x0016[4:0] = 0b00100 for 100Base-TX and BISCR 0x0016[4:0] = 00001b for 10Base-Te 0h = Normal Operation 1h = MII Loopback enabled
13	Speed Selection	RH/W	X	Speed Selection: When Auto-Negotiation is disabled (bit [12] = 0 in Register 0x0000), writing to this bit allows the port speed to be selected. In BASIC Mode: It is also determined by strap when Auto-Negotiation is disabled. 0h = 10 Mbps 1h = 100 Mbps
12	Auto-Negotiation Enable	RH/W	X	Auto-Negotiation Enable: In BASIC Mode and ENHANCED Mode: Latched by strap 0h = Disable Auto-Negotiation - bits [8] and [13] determine the port speed and duplex mode 1h = Enable Auto-Negotiation - bits [8] and [13] of this register are ignored when this bit is set

Table 8-22. BMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	IEEE Power Down	R/W	0h	Power Down: The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N (in ENHANCED mode) pin. When the active low INT/PWDN_N is asserted, this bit is set. 0h = Normal Operation 1h = IEEE Power Down
10	Isolate	RH/W	X	In BASIC Mode, the value is Latched by strap 0h = Normal Operation 1h = Isolates the port from the MII with the exception of the serial management interface. It also disables50MHz clock in RMII Leader mode
9	Restart Auto-Negotiation	RH/W1S	0h	Restart Auto-Negotiation: If Auto-Negotiation is disabled (bit [12] = 0), bit [9] is ignored. This bit is self-clearing and returns a value of 1 until Auto-Negotiation is initiated, whereupon this bit clears. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0h = Normal Operation 1h = Restarts Auto-Negotiation, Re-initiates the Auto-Negotiation process
8	Duplex Mode	RH/W	X	Duplex Mode: When Auto-Negotiation is disabled, writing to this bit allows the port Duplex capability to be selected. In BASIC Mode, this bit is Latched by strap 0h = Half-Duplex 1h = Full-Duplex
7	Collision Test	R/W	0h	Collision Test: When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the de-assertion to TX_EN. 0h = Normal Operation 1h = Enable COL Signal Test
6-0	RESERVED	R	0h	

8.5.1.2 BMSR Register (Offset = 1h) [Reset = 7849h]

BMSR Register is shown in Table 8-23.

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Basic Mode Status Register

Table 8-23. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4	R	0h	100Base-T4 Capable: This protocol is not available. Always reads as 0.
14	100Base-TX Full-Duplex	R	1h	100Base-TX Full-Duplex Capable: 0h = Device not able to perform Full-Duplex 100Base-TX 1h = Device able to perform Full-Duplex 100Base-TX
13	100Base-TX Half-Duplex	R	1h	100Base-TX Half-Duplex Capable: 0h = Device not able to perform Half-Duplex 100Base-TX 1h = Device able to perform Half-Duplex 100Base-TX
12	10Base-T Full-Duplex	R	1h	10Base-T Full-Duplex Capable: 0h = Device not able to perform Full-Duplex 10Base-T 1h = Device able to perform Full-Duplex 10Base-T
11	10Base-T Half-Duplex	R	1h	10Base-T Half-Duplex Capable: 0h = Device not able to perform Half-Duplex 10Base-T 1h = Device able to perform Half-Duplex 10Base-T
10-7	RESERVED	R	0h	

Table 8-23. BMSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SMI Preamble Suppression	R	1h	Preamble Suppression Capable: If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. The device requires minimum of 500ns gap between two transactions, followed by one positive edge of MDC and MDIO=1, before starting the next transaction. 0h = Device not able to perform management transaction with preambles suppressed 1h = Device able to perform management transaction with preamble suppressed
5	Auto-Negotiation Complete	RH	0h	Auto-Negotiation Complete: 0h = Auto Negotiation process not completed (either still in process, disabled or reset) 1h = Auto-Negotiation process completed
4	Remote Fault	RC	0h	Remote Fault: Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset. 0h = No remote fault condition detected 1h = Remote fault condition detected
3	Auto-Negotiation Ability	R	1h	Auto-Negotiation Ability: 0h = Device is not able to perform Auto-Negotiation 1h = Device is able to perform Auto-Negotiation
2	Link Status	RC	0h	Link Status: Last latched value is cleared on read 0h = Link not established 1h = Valid link established (for either 10 Mbps or 100 Mbps operation)
1	Jabber Detect	RH	0h	Jabber Detect: 0h = No jabber condition detected This bit only has meaning for 10Base-T operation. 1h = Jabber condition detected
0	Extended Capability	R	1h	Extended Capability: 0h = Basic register set capabilities only 1h = Extended register capabilities

8.5.1.3 PHYIDR1 Register (Offset = 2h) [Reset = 2000h]

PHYIDR1 Register is shown in Table 8-24.

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PHY Identifier Register #1

Table 8-24. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally Unique Identifier Bits 21:6	R	2000h	PHY Identifier Register #1

8.5.1.4 PHYIDR2 Register (Offset = 3h) [Reset = A131h]

PHYIDR2 Register is shown in Table 8-25.

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PHY Identifier Register #2

Table 8-25. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally Unique Identifier Bits 5:0	R	28h	PHY Identifier Register #2
9-4	Model Number	R	13h	Vendor Model Number: The six bits of vendor model number are mapped from bits [9] to [4] 11h = Basic Mode 13h = ENHANCED Mode
3-0	Revision Number	R	1h	Model Revision Number: Four bits of the vendor model revision number are mapped from bits [3:0]. This field is incremented for all major device changes.

8.5.1.5 ANAR Register (Offset = 4h) [Reset = 0XX1h]

ANAR Register is shown in Table 8-26.

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Auto-Negotiation Advertisement Register

Table 8-26. ANAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R/W	0h	Next Page Indication: 0h = Next Page Transfer not desired 1h = Next Page Transfer desired
14	RESERVED	R	0h	
13	Remote Fault	R/W	0h	Remote Fault: 0h = No Remote Fault detected 1h = Advertises that this device has detected a Remote Fault. Please note DP83826 does not support Remote Fault. This bit shall not be set by Application
12	RESERVED	R	0h	
11	Asymmetric Pause	R/W	0h	Asymmetric Pause Support For Full-Duplex Links: 0h = Do not advertise asymmetric pause ability 1h = Advertise asymmetric pause ability
10	Pause	R/W	0h	Pause Support for Full-Duplex Links: 0h = Do not advertise pause ability 1h = Advertise pause ability
9	100Base-T4	R	0h	100Base-T4 Support: 0h = Do not advertise 100Base-T4 ability 1h = Advertise 100Base-T4 ability
8	100Base-TX Full-Duplex	RH/W	X	100Base-TX Full-Duplex Support: Values does not matter in force-mode BASIC Mode : Latched by strap 0h = Do not advertise 100Base-TX Full-Duplex ability Values does not matter in force-mode 1h = Advertise 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	RH/W	X	100Base-TX Half-Duplex Support: Values does not matter in force-mode BASIC Mode: Latched by strap 0h = Do not advertise 100Base-TX Half-Duplex ability Values does not matter in force-mode 1h = Advertise 100Base-TX Half-Duplex ability
6	10Base-T Full-Duplex	RH/W	X	10Base-T Full-Duplex Support: Values does not matter in force-mode BASIC Mode: Latched by strap 0h = Do not advertise 10Base-T Full-Duplex ability Values does not matter in force-mode 1h = Advertise 10Base-T Full-Duplex ability

Table 8-26. ANAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	10Base-T Half-Duplex	RH/W	X	10Base-T Half-Duplex Support: Values does not matter in force-mode BASIC Mode/ENHANCED Mode : Latched by strap 0h = Do not advertise 10Base-T Half-Duplex ability Values does not matter in force-mode 1h = Advertise 10Base-T Half-Duplex ability
4-0	Selector Field	R/W	1h	Protocol Selection Bits: Technology selector field (IEEE802.3u <00001>)

8.5.1.6 ALNPAR Register (Offset = 5h) [Reset = 0000h]

ALNPAR Register is shown in Table 8-27.

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Auto-Negotiation Link Partner Ability Register

Table 8-27. ALNPAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R	0h	Next Page Indication: 0h = Link partner does not desire Next Page Transfer 1h = Link partner desires Next Page Transfer
14	Acknowledge	R	0h	Acknowledge: 0h = Link partner does not acknowledge reception of link code word 1h = Link partner acknowledges reception of link code word
13	Remote Fault	R	0h	Remote Fault: 0h = Link partner does not advertise remote fault event detection 1h = Link partner advertises remote fault event detection
12	RESERVED	R	0h	
11	Asymmetric Pause	R	0h	Asymmetric Pause: 0h = Link partner does not advertise asymmetric pause ability 1h = Link partner advertises asymmetric pause ability
10	Pause	R	0h	Pause: 0h = Link partner does not advertise pause ability 1h = Link partner advertises pause ability
9	100Base-T4	R	0h	100Base-T4 Support: 0h = Link partner does not advertise 100Base-T4 ability 1h = Link partner advertises 100Base-T4 ability
8	100Base-TX Full-Duplex	R	0h	100Base-TX Full-Duplex Support: 0h = Link partner does not advertise 100Base-TX Full-Duplex ability 1h = Link partner advertises 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	R	0h	100Base-TX Half-Duplex Support: 0h = Link partner does not advertise 100Base-TX Half-Duplex ability 1h = Link partner advertises 100Base-TX Half-Duplex ability
6	10Base-T Full-Duplex	R	0h	10Base-T Full-Duplex Support: 0h = Link partner does not advertise 10Base-T Full-Duplex ability 1h = Link partner advertises 10Base-T Full-Duplex ability
5	10Base-T Half-Duplex	R	0h	10Base-T Half-Duplex Support: 0h = Link partner does not advertise 10Base-T Half-Duplex ability 1h = Link partner advertises 10Base-T Half-Duplex ability
4-0	Selector Field	R	0h	Protocol Selection Bits: Technology selector field (IEEE802.3 <00001>)

8.5.1.7 ANER Register (Offset = 6h) [Reset = 0004h]

ANER Register is shown in Table 8-28.

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Auto-Negotiation Expansion Register

Table 8-28. ANER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	
4	Parallel Detection Fault	RH	0h	Parallel Detection Fault: 0h = No fault detected 1h = A fault has been detected during the parallel detection process
3	Link Partner Next Page Able	R	0h	Link Partner Next Page Ability: 0h = Link partner is not able to exchange next pages 1h = Link partner is able to exchange next pages
2	Local Device Next Page Able	R	1h	Next Page Ability: 0h = Local device is not able to exchange next pages 1h = Local device is able to exchange next pages
1	Page Received	RH	0h	Link Code Word Page Received: 0h = A new page has not been received 1h = A new page has been received
0	Link Partner Auto-Negotiation Able	R	0h	Link Partner Auto-Negotiation Ability: 0h = Link partner does not support Auto-Negotiation 1h = Link partner supports Auto-Negotiation

8.5.1.8 ANNPTR Register (Offset = 7h) [Reset = 2001h]

ANNPTR Register is shown in Table 8-29.

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Auto-Negotiation Next Page Register

Table 8-29. ANNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R/W	0h	Next Page Indication: 0h = Do not advertise desire to send additional next pages 1h = Advertise desire to send additional next pages
14	RESERVED	R	0h	
13	Message Page	R/W	1h	Message Page: 0h = Current page is an unformatted page 1h = Current page is a message page
12	Acknowledge 2	R/W	0h	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0h = Cannot comply with message 1h = Complies with message
11	Toggle	R	0h	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0h = Value of toggle bit in previously transmitted Link Code Word was 1 1h = Value of toggle bit in previously transmitted Link Code Word was 0

Table 8-29. ANNPTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-0	CODE	R/W	1h	This field represents the code field of the next page transmission. If the Message Page bit is set (bit [13] of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.5.1.9 ANLNPTR Register (Offset = 8h) [Reset = 0000h]

ANLNPTR Register is shown in Table 8-30.

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Auto-Negotiation Link Partner Ability Next Page Register

Table 8-30. ANLNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R	0h	Next Page Indication: 0h = Do not advertise desire to send additional next pages 1h = Advertise desire to send additional next pages
14	Acknowledge	R	0h	Acknowledge: 0h = Link partner does not acknowledge reception of link code work 1h = Link partner acknowledges reception of link code word
13	Message Page	R	0h	Message Page: 0h = Current page is an unformatted page 1h = Current page is a message page
12	Acknowledge 2	R	0h	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0h = Cannot comply with message 1h = Complies with message
11	Toggle	R	0h	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0h = Value of toggle bit in previously transmitted Link Code Word was 1 1h = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	Message/Unformatted Field	R	0h	This field represents the code field of the next page transmission. If the Message Page bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.5.1.10 CR1 Register (Offset = 9h) [Reset = 0000h]

CR1 Register is shown in Table 8-31.

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Control Register #1

Table 8-31. CR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	

Table 8-31. CR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RESERVED	R/W	0h	
8	TDR Auto-Run	R/W	0h	TDR Auto-Run at Link Down 0h = Disable automatic execution of TDR 1h = Enable execution of TDR procedure after link down event
7	Link Loss Recovery	R/W	0h	Link Loss Recovery: 0h = Normal Link Loss operation This mode allows recovery from short interference and continue to hold the link up for a few additional mSec until the short interference is gone and the signal is OK. Under Normal Link Loss operation, Link status goes down approximately 250µs from signal loss. 1h = Enable Link Loss Recovery mechanism
6	RESERVED	R/W	0h	
5	Robust Auto MDIX	R/W	0h	Robust Auto-MDIX: If link partners are configured for operational modes that are not supported by normal Auto-MDIX, Robust Auto-MDIX allows MDI/MDIX resolution and prevents deadlock. When using in Force Mode, Robust Auto-MDIX shall be enabled 0h = Disable Auto-MDIX 1h = Enable Robust Auto-MDIX
4	RESERVED	R/W	0h	
3-2	RESERVED	R/W	0h	
1	Fast RXDV Detection	R/W	0h	Fast RXDV Detection: 0h = Disable Fast RX_DV detection. The PHY operates in normal mode. RX_DV assertion after detection of /JK/. 1h = Enable assertion high of RX_DV on receive packet due to detection of /J/ symbol only. If a consecutive /K/ does not appear, RX_ER is generated.
0	RESERVED	R	0h	

8.5.1.11 CR2 Register (Offset = Ah) [Reset = 010Xh]

CR2 Register is shown in Table 8-32.

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Control Register #2

Table 8-32. CR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	
14	RESERVED	R/W	0h	
13-7	RESERVED	R/W	2h	
6	RESERVED	R/W	0h	
5	Extended Full-Duplex Ability	R/W	0h	Extended Full-Duplex Ability: 0h = Disable Extended Full-Duplex Ability. Decision to work in Full-Duplex or Half-Duplex mode follows IEEE specification 1h = Enable Full-Duplex while working with link partner in force 100Base-TX. When the PHY is set to Auto-Negotiation or Force 100Base-TX and the link partner is operated in Force 100Base-TX, the link is always Full-Duplex
4	RESERVED	R/W	0h	
3	RESERVED	R/W	0h	
2	RX_ER During IDLE	R/W	0h	Detection of Receive Symbol Error During IDLE State: 0h = Disable detection of Receive symbol error during IDLE state 1h = Enable detection of Receive symbol error during IDLE state

Table 8-32. CR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	Odd-Nibble Detection Disable	RH/W	X	Detection of Transmit Error. ENHANCED mode: Enabled by default, can be changed with Strap1 BASIC mode: Disabled 0h = Enable detection of de-assertion of TX_EN on an odd-nibble boundary. In this case TX_EN is extended by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle 1h = Disable detection of transmit error in odd-nibble boundary
0	RESERVED	R/W	0h	

8.5.1.12 CR3 Register (Offset = Bh) [Reset = 0000h]

CR3 Register is shown in Table 8-33.

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Control Register #3

Table 8-33. CR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R/W	0h	
10	Descrambler Fast Link Down Mode	R/W	0h	Descrambler Fast Link Drop: This option can be enabled in parallel to the other fast link down modes in bits [3:0]. 0h = Do not drop the link on descrambler link loss 1h = Drop the link on descrambler link loss
9	RESERVED	R	0h	
8	RESERVED	R/W	0h	
7	RESERVED	R/W	0h	
6	Polarity Swap	R/W	0h	Polarity Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [5] high. 1h = Inverted polarity on both pairs: TD+ and TD-, RD+ and RD- 0h = Normal polarity
5	MDI/MDIX Swap	R/W	0h	MDI/MDIX Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [6] high. 0h = MDI pairs normal (Receive on RD pair, Transmit on TD pair) 1h = Swap MDI pairs (Receive on TD pair, Transmit on RD pair)
4	RESERVED	R/W	0h	
3-0	Fast Link Down Mode	RH/W	0h	Fast Link Down Modes: Bit 3 Drop the link based on RX Error count of the MII interface. When a predefined number of 32 RX Error occurences in a 10us interval is reached, the link is dropped. Bit 2 Drop the link based on MLT3 Error count (Violation of the MLT3 coding in the DSP output). When a predefined number of 20 MLT3 Error occurences in 10µs interval is reached, the link is dropped. Bit 1 Drop the link based on Low SNR Threshold. When a predefined number of 20 Threshold crossing occurences in a 10µs interval is reached, the link is dropped. Bit 0 Drop the link based on Signal/ Energy Loss indication. When the Energy detector indicates Energy Loss, the link is dropped. Typical reaction time is 10µs C : Bit 0 default is 0 NC+ MII: Bit 0 is taken from STRAP in ENHANCED mode NC + RMII: Bit 0 default is 0 The Fast Link Down function is an OR of all 5 options (bits [10] and [3:0]), the designer can enable any combination of these conditions.

8.5.1.13 REGCR Register (Offset = Dh) [Reset = 0000h]

REGCR Register is shown in Table 8-34.

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Table 8-34. REGCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended Register Command	R/W	0h	Extended Register Command: 0h = Address 1h = Data, no post increment 2h = Data, post increment on read and write 3h = Data, post increment on write only
13-5	RESERVED	R	0h	
4-0	DEVAD	R/W	0h	Device Address: Bits [4:0] are the device address, DEVAD, that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the DP83826 uses the vendor specific DEVAD [4:0] = '11111' for accesses to registers 0x04D1 and lower. For MMD3 access, the DEVAD[4:0] = '00011'. For MMD7 access, the DEVAD[4:0] = '00111'. All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD, MMD3 or MMD7. Transactions with other DEVAD are ignored.

8.5.1.14 ADDAR Register (Offset = Eh) [Reset = 0000h]

ADDAR Register is shown in Table 8-35.

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Table 8-35. ADDAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0h	If REGCR register bits [15:14] = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

8.5.1.15 FLDS Register (Offset = Fh) [Reset = 0000h]

FLDS Register is shown in Table 8-36.

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Table 8-36. FLDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	
8-4	Fast Link Down Status	RC	0h	Fast Link Down Status: Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming the modes were enabled) 1h = Signal/Energy Lost 2h = SNR Level 4h = MLT3 Errors 8h = RX Errors 10h = Descrambler Loss Sync
3-0	RESERVED	R	0h	

8.5.1.16 PHYSTS Register (Offset = 10h) [Reset = 0002h]

PHYSTS Register is shown in Table 8-37.

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Table 8-37. PHYSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	MDI/MDIX Mode	R	0h	MDI/MDIX Mode Status: 0h = MDI Pairs normal (Receive on RD pair, Transmit on TD pair) 1h = MDI Pairs swapped (Receive on TD pair, Transmit on RD pair)
13	Receive Error Latch	RC	0h	Receive Error Latch: This bit is cleared upon a read of the RECR register 0h = No receive error event has occurred 1h = Receive error event has occurred since last read of RXERCNT register (0x0015)
12	Polarity Status	RC	0h	Polarity Status: This bit is a duplication of bit [4] in the 10BTSCR register (0x001A). This bit is cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 0h = Correct Polarity detected 1h = Inverted Polarity detected
11	False Carrier Sense Latch	RC	0h	False Carrier Sense Latch: This bit is cleared upon a read of the FCSR register. 0h = No False Carrier event has occurred 1h = False Carrier even has occurred since last read of FCSCR register (0x0014)
10	Signal Detect	RC	0h	Signal Detect: Active high 100Base-TX unconditional Signal Detect indication from PMD
9	Descrambler Lock	RC	0h	Descrambler Lock: Active high 100Base-TX Descrambler Lock indication from PMD
8	Page Received	RC	0h	Link Code Word Page Received: This bit is a duplicate of Page Received (bit [1]) in the ANER register and it is cleared on read of the ANER register (0x0006). 0h = Link Code Word Page has not been received 1h = A new Link Code Word Page has been received
7	MII Interrupt	RC	0h	MII Interrupt Pending: Interrupt source can be determined by reading the MISR register (0x0012). Reading the MISR clears this interrupt bit indication. 0h = No interrupt pending 1h = Indicates that an internal interrupt is pending
6	Remote Fault	RC	0h	Remote Fault: Cleared on read of BMSR register (0x0001) or by reset. 1h = Remote Fault condition detected. Fault criteria: notification from link partner of Remote Fault via Auto-Negotiation 0h = No Remote Fault condition detected
5	Jabber Detect	RC	0h	Jabber Detection: This bit is only for 10 Mbps operation. This bit is a duplicate of the Jabber Detect bit in the BMSR register (0x0001) and is not cleared upon a read of the PHYSTS register. 0h = No Jabber 1h = Jabber condition detected
4	Auto-Negotiation Status	R	0h	Auto-Negotiation Status: 0h = Auto-Negotiation not complete 1h = Auto-Negotiation complete
3	MII Loopback Status	R	0h	MII Loopback Status: 0h = Normal operation 1h = Loopback enabled
2	Duplex Status	RH	0h	Duplex Status: BASIC Mode: Latched by Strap when Auto-Negotiation is disabled ENHANCED Mode : 1 when Auto-Negotiation is disabled 0h = Half-Duplex mode 1h = Full-Duplex mode

Table 8-37. PHYSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	Speed Status	RH	1h	Speed Status: BASIC Mode : Latched by Strap when Auto-Negotiation is disabled ENHANCED Mode : 1 when Auto-Negotiation is disabled 0h = 100 Mbps mode 1h = 10 Mbps mode
0	Link Status	R	0h	Link Status: This bit is duplicated from the Link Status bit in the BMSR register (address 0x0001) and is not cleared upon a read of the PHYSTS register. 0h = No link established 1h = Valid link established (for either 10 Mbps or 100 Mbps)

8.5.1.17 PHYSCR Register (Offset = 11h) [Reset = 0108h]

PHYSCR Register is shown in Table 8-38.

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Table 8-38. PHYSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Disable PLL	R/W	0h	Disable PLL: Note: clock circuitry can be disabled only in IEEE power down mode. 0h = Normal operation 1h = Disable internal clocks circuitry
14	Power Save Mode Enable	R/W	0h	Power Save Mode Enable: 0h = Normal operation 1h = Enable power save modes
13-12	Power Save Modes	R/W	0h	Power Save Mode: 0h = Normal operation mode. PHY is fully functional 1h = Reserved 2h = Active Sleep, Low Power Active Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 seconds to wake up link partner. Automatic power-up is done when link partner is detected.
11	Scrambler Bypass	R/W	0h	Scrambler Bypass: 0h = Scrambler bypass disabled 1h = Scrambler bypass enabled
10	RESERVED	R/W	0h	
9-8	Loopback FIFO Depth	R/W	1h	Far-End Loopback FIFO Depth: This FIFO is used to adjust RX (receive) clock rate to TX clock rate. FIFO depth needs to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles. 0h = 4 nibbles FIFO 1h = 5 nibbles FIFO 2h = 6 nibbles FIFO 3h = 8 nibbles FIFO
7-5	RESERVED	R	0h	
4	COL Full-Duplex Enable	R/W	0h	Collision in Full-Duplex Mode: 0h = Disable Collision in Full-Duplex mode. Collision remains active in Half-Duplex only. 1h = Enable generating Collision signaling in Full-Duplex mode
3	Interrupt Polarity	R/W	1h	Interrupt Polarity: 0h = Steady state (normal operation) is 0 logic and during interrupt is 1 logic 1h = Steady state (normal operation) is 1 logic and during interrupt is 0 logic

Table 8-38. PHYSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	Test Interrupt	R/W	0h	Test Interrupt: Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts continue to be generated as long as this bit remains set. 0h = Do not generate interrupt 1h = Generate an interrupt
1	Interrupt Enable	R/W	0h	Interrupt Enable: Enable interrupt dependent on the event enables in the MISR register (0x0012). 0h = Disable event based interrupts 1h = Enable event based interrupts
0	Interrupt Output Enable	R/W	0h	Interrupt Output Enable: Enable active low interrupt events via the INTR/PWERDN pin by configuring the INTR/PWRDN pin as an output(for ENHANCED mode) 0h = INTR/PWRDN is a Power Down pin 1h = INTR/PWRDN is an interrupt output

8.5.1.18 MISR1 Register (Offset = 12h) [Reset = 0000h]

MISR1 Register is shown in Table 8-39.

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Table 8-39. MISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link Quality Interrupt	RC	0h	Change of Link Quality Status Interrupt: 0h = Link quality is Good 1h = Change of link quality when link is ON
14	Energy Detect Interrupt	RC	0h	Change of Energy Detection Status Interrupt: 0h = No change of energy detected 1h = Change of energy detected
13	Link Status Changed Interrupt	RC	0h	Change of Link Status Interrupt: 0h = No change of link status 1h = Change of link status interrupt is pending
12	Speed Changed Interrupt	RC	0h	Change of Speed Status Interrupt: 0h = No change of speed status 1h = Change of speed status interrupt is pending
11	Duplex Mode Changed Interrupt	RC	0h	Change of Duplex Status Interrupt: 0h = No change of duplex status 1h = Change of duplex status interrupt is pending
10	Auto-Negotiation Completed Interrupt	RC	0h	Auto-Negotiation Complete Interrupt: 0h = No Auto-Negotiation complete event is pending 1h = Auto-Negotiation complete interrupt is pending
9	False Carrier Counter Half-Full Interrupt	RC	0h	False Carrier Counter Half-Full Interrupt: 0h = False Carrier half-full event is not pending 1h = False Carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending
8	Receive Error Counter Half-Full Interrupt	RC	0h	Receiver Error Counter Half-Full Interrupt: 0h = Receive Error half-full event is not pending 1h = Receive Error counter (Register RECR, address 0x0015) exceeds half-full interrupt is pending
7	Link Quality Interrupt Enable	R/W	0h	Enable interrupt on change of link quality
6	Energy Detect Interrupt Enable	R/W	0h	Enable interrupt on change of energy detection
5	Link Status Changed Enable	R/W	0h	Enable interrupt on change of link status

Table 8-39. MISR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	Speed Changed Interrupt Enable	R/W	0h	Enable Interrupt on change of speed status
3	Duplex Mode Changed Interrupt Enable	R/W	0h	Enable Interrupt on change of duplex status
2	Auto-Negotiation Completed Enable	R/W	0h	Enable Interrupt on Auto-negotiation complete event
1	False Carrier HF Enable	R/W	0h	Enable Interrupt on False Carrier Counter Register half-full event
0	Receive Error HF Enable	R/W	0h	Enable Interrupt on Receive Error Counter Register half-full event

8.5.1.19 MISR2 Register (Offset = 13h) [Reset = 0000h]

MISR2 Register is shown in Table 8-40.

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Table 8-40. MISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EEE Error Interrupt	RC	0h	Energy Efficient Ethernet Error Interrupt: 0h = EEE error has not occurred 1h = EEE error has occurred
14	Auto-Negotiation Error Interrupt	RC	0h	Auto-Negotiation Error Interrupt: 0h = No Auto-Negotiation error even pending 1h = Auto-Negotiation error interrupt is pending
13	Page Received Interrupt	RC	0h	Page Receiver Interrupt: 0h = Page has not been received 1h = Page has been received
12	Loopback FIFO OF/UF Event Interrupt	RC	0h	Loopback FIFO Overflow/Underflow Event Interrupt: 0h = No FIFO Overflow/Underflow event pending 1h = FIFO Overflow/Underflow event interrupt pending
11	MDI Crossover Change Interrupt	RC	0h	MDI/MDIX Crossover Status Change Interrupt: 0h = MDI crossover status has not changed 1h = MDI crossover status changed interrupt is pending
10	Sleep Mode Interrupt	RC	0h	Sleep Mode Event Interrupt: 0h = No Sleep mode event pending 1h = Sleep mode event interrupt is pending
9	Inverted Polarity Interrupt / WoL Packet Received Interrupt	RC	0h	Inverted Polarity Interrupt / WoL Packet Received Interrupt: 0h = No Inverted polarity event pending / No WoL oacket received 1h = Inverted Polarity interrupt pending / WoL packet was recieved
8	Jabber Detect Interrupt	RC	0h	Jabber Detect Event Interrupt: 0h = No Jabber detect event pending 1h = Jabber detect even interrupt pending
7	EEE Error Interrupt Enable	R/W	0h	Enable interrupt on EEE Error
6	Auto-Negotiation Error Interrupt Enable	R/W	0h	Enable Interrupt on Auto-Negotiation error event
5	Page Received Interrupt Enable	R/W	0h	Enable Interrupt on page receive event
4	Loopback FIFO OF/UF Enable	R/W	0h	Enable Interrupt on loopback FIFO Overflow/Underflow event
3	MDI Crossover Change Enable	R/W	0h	Enable Interrupt on change of MDI/X status
2	Sleep Mode Event Enable	R/W	0h	Enable Interrupt on sleep mode event
1	Polarity Changed / WoL Packet Enable	R/W	0h	Enable Interrupt on change of polarity status
0	Jabber Detect Enable	R/W	0h	Enable Interrupt on Jabber detection event

8.5.1.20 FCSCR Register (Offset = 14h) [Reset = 0000h]

FCSCR Register is shown in Table 8-41.

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Table 8-41. FCSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	False Carrier Event Counter	RC	0h	False Carrier Event Counter: This 8-bit counter increments on every false carrier event. This counter stops when the maximum count (FFh) is reached. When the counter exceeds half-full (7Fh), an interrupt event is generated. This register is cleared on read.

8.5.1.21 RECR Register (Offset = 15h) [Reset = 0000h]

RECR Register is shown in Table 8-42.

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Table 8-42. RECR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Receive Error Counter	RC	0h	RX_ER Counter: When a valid carrier is presented (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt is generated. This register is cleared on read.

8.5.1.22 BISCR Register (Offset = 16h) [Reset = 0100h]

BISCR Register is shown in Table 8-43.

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Table 8-43. BISCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	BIST Error Counter Mode	R/W	0h	BIST Error Counter Mode: 0h = Single mode, when BIST Error Counter reaches the max value, PRBS checker stops counting. 1h = Continuous mode, when the BIST Error counter reaches the max value, a pulse is generated and the counter starts counting from zero again.
13	PRBS Checker Config	R/W	0h	PRBS Checker Config:bit[13:12] 0h = PRBS Generator and Checker both are disabled 1h = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 2h = PRBS Generation is disabled. PRBS Checker is Enabled 3h = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C
12	Packet Generation Enable	R/W	0h	Packet Generation Enable:bit[13:12] 0h = PRBS Generator and Checker both are disabled 1h = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 2h = PRBS Generation is disabled. PRBS Checker is Enabled 3h = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C

Table 8-43. BISCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	PRBS Checker Lock/Sync	R	0h	PRBS Checker Lock/Sync Indication: 0h = PRBS checker is not locked 1h = PRBS checker is locked and synced on received bit stream
10	PRBS Checker Sync Loss	RH	0h	PRBS Checker Sync Loss Indication: 0h = PRBS checker has not lost sync 1h = PRBS checker has lost sync
9	Packet Generator Status	R	0h	Packet Generation Status Indication: 0h = Packet Generator is off 1h = Packet Generator is active and generating packets
8	Power Mode	R	1h	Sleep Mode Indication: 0h = Indicates that the PHY is in active sleep mode 1h = Indicates that the PHY is in normal power mode
7	RESERVED	R	0h	
6	Transmit in MII Loopback	R/W	0h	Transmit Data in MII Loopback Mode (valid only at 100 Mbps) 0h = Data is not transmitted to the line in MII loopback 1h = Enable transmission of data from the MAC received on the TX pins to the line in parallel to the MII loopback to RX pins. This bit can be set only in MII Loopback mode - setting bit [14] in BMCR register (0x0000)
5	RESERVED	R	0h	
4-0	Loopback Mode	R/W	0h	Loopback Mode Select: The PHY provides several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the DP83826 digital and analog data paths 1h = PCS Input Loopback (Use for 10Base-Te only) 2h = PCS Output Loopback 4h = Digital Loopback (Use for 100Base-TX Only) Additional Register writes are required. 8h = Analog Loopback (requires 100Ω termination) 10h = Reverse Loopback

8.5.1.23 RCSR Register (Offset = 17h) [Reset = 00X1h]

RCSR Register is shown in Table 8-44.

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Table 8-44. RCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RMII TX Clock Shift	R/W	0h	RMII TX Clock Shift: Applicable only in RMII Follower mode 0h = Transmit path internal clock shift is disabled 1h = Transmit path internal clock shift is enabled
7	RMII Clock Select	RH/W	X	RMII Reference Clock Select: BASIC Mode: Latched by strap ENHANCED Modie: Latched by strap 0h = 25MHz clock reference, crystal or CMOS-level oscillator 1h = 50MHz clock reference, CMOS-level oscillator
6	RESERVED	R/W	1h	
5	RMII Mode	RH/W	X	RMII or MII MAC Interface Enable: 0h = Enable MII mode of operation 1h = Enable RMII mode of operation

Table 8-44. RCSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RMII Revision Select	R/W	0h	RMII Revision Select: 0h = (RMII revision 1.2) CRS_DV toggles at the end of a packet to indicate de-assertion of CRS 1h = (RMII revision 1.0) CRS_DV remains asserted until final data is transferred. CRS_DV does not toggle at the end of a packet
3	RMII Overflow Status	RC	0h	RX FIFO Overflow Status: 0h = Overflow detected 1h = Normal
2	RMII Underflow Status	RC	0h	RX FIFO Underflow Status: 0h = Underflow detected 1h = Normal
1-0	Receive Elasticity Buffer Size	R/W	1h	Receive Elasticity Buffer Size: This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at +/-50ppm accuracy. For greater frequency tolerance, the packet lengths may be scaled (for +/-100ppm), divide the packet lengths by 2). 0h = 14 bit tolerance (up to 16800 byte packets) 1h = 2 bit tolerance (up to 2400 byte packets) 2h = 6 bit tolerance (up to 7200 byte packets) 3h = 10 bit tolerance (up to 12000 byte packets)

8.5.1.24 LEDCR Register (Offset = 18h) [Reset = 04X0h]

LEDCR Register is shown in Table 8-45.

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Table 8-45. LEDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	
10-9	Blink Rate	R/W	2h	LED Blinking Rate (ON/OFF duration): 0h = 20Hz (50 ms) 1h = 10Hz (100 ms) 2h = 5Hz (200 ms) 3h = 2Hz (500 ms)
8	RESERVED	R/W	0h	
7	LED Link Polarity	RH/W	X	LED Link Polarity Setting: Link LED polarity is Active Low in BASIC mode and defined by direction of strapping on this pin in ENHANCED mode. This register allows for override of this strap value. 0h = Active Low polarity setting 1h = Active High polarity setting
6-5	RESERVED	R/W	0h	
4	Drive Link LED	R/W	0h	Drive Link LED Select: 0h = Normal operation 1h = Drive value of ON/OFF bit [1] onto LED0 output pin
3-2	RESERVED	R/W	0h	
1	Link LED ON/OFF Setting	R/W	0h	Value to force on Link LED output 0h = LOW 1h = HIGH
0	RESERVED	R/W	0h	

8.5.1.25 PHYCR Register (Offset = 19h) [Reset = X0XXh]

PHYCR Register is shown in Table 8-46.

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Table 8-46. PHYCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Auto MDI/X Enable	RH/W	X	Auto-MDIX Enable: BASIC Mode: Default to A-MDIX enabled. ENHANCED Mode : Latched by strap A-MDIX 0h = Disable Auto-Negotiation Auto-MDIX capability 1h = Enable Auto-Negotiation Auto-MDIX capability
14	Force MDI/X	RH/W	X	Force MDIX: ENHANCED Mode: When A-MDIX strap is disabled, latched by FORCE MDI/MDIX strap 0h = Normal operation (Receive on RD pair, Transmit on TD pair) 1h = Force MDI pairs to cross (Receive on TD pair, Transmit on RD pair)
13	Pause RX Status	R	0h	Pause Receive Negotiation Status: Indicates that pause receive can be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. The function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
12	Pause TX Status	R	0h	Pause Transmit Negotiated Status: Indicates that pause should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
11	MII Link Status	R	0h	MII Link Status: 0h = No active 100Base-TX Full-Duplex link, established using Auto-Negotiation 1h = 100Base-TX Full-Duplex link is active and it was established using Auto-Negotiation
10-8	RESERVED	R	0h	
7	Bypass LED Stretching	R/W	0h	Bypass LED Stretching: Set this bit to '1' to bypass the LED stretching, the LED reflects the internal value. 0h = Normal LED operation 1h = Bypass LED stretching
6	RESERVED	R/W	0h	
5	LED Configuration	R/W	0h	
4-0	PHY Address	RH	X	PHY Address: BASIC Mode: Latched by Strap ENHANCED Mode: Latched by Strap

8.5.1.26 10BTSCR Register (Offset = 1Ah) [Reset = 0000h]

10BTSCR Register is shown in Table 8-47.

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Table 8-47. 10BTSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	
13	Receiver Threshold Enable	R/W	0h	Lower Receiver Threshold Enable: 0h = Normal 10Base-T operation 1h = Enable 10Base-T lower receiver threshold to allow operation with longer cables

Table 8-47. 10BTSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	Squelch	R/W	0h	Squelch Configuration: Used to set the Peak Squelch 'ON' threshold for the 10Base-T receiver. Starting from 200mV to 600mV, step size of 50mV with some overlapping as shown below: 0h = 200mV 1h = 250mV 2h = 300mV 3h = 350mV 4h = 400mV 5h = 450mV 6h = 500mV 7h = 550mV 8h = 600mV
8	RESERVED	R/W	0h	
7	NLP Disable	R/W	0h	NLP Transmission Control: 0h = Enable transmission of NLPs 1h = Disable transmission of NLPs
6-5	RESERVED	R	0h	
4	Polarity Status	R	0h	Polarity Status: This bit is a duplication of bit [12] in the PHYSTS register (0x0010). Both bits are cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register. 0h = Correct Polarity detected 1h = Inverted Polarity detected
3-1	RESERVED	R	0h	
0	Jabber Disable	R/W	0h	Jabber Disable: Note: This function is only applicable in 10Base-Te operation. 0h = Jabber function enabled 1h = Jabber function disabled

8.5.1.27 BICSR1 Register (Offset = 1Bh) [Reset = 007Dh]

BICSR1 Register is shown in Table 8-48.

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Table 8-48. BICSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	BIST Error Count	R	0h	BIST Error Count: Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to bit [15]. When BIST Error Counter Mode is set to '0', count stops on 0xFF (see register 0x0016) Note: Writing '1' to bit [15] locks the counter's value for successive read operation and clear the BIST Error Counter.
7-0	BIST IPG Length	R/W	7Dh	BIST IPG Length: Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 125 bytes*4 = 500 bytes). Binary values shall be multiplied by 4 to get the actual IPG length

8.5.1.28 BICSR2 Register (Offset = 1Ch) [Reset = 05EEh]

BICSR2 Register is shown in Table 8-49.

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Table 8-49. BICSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	
10-0	BIST Packet Length	R/W	5EEh	BIST Packet Length: Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x05EE, which is equal to 1518 bytes.

8.5.1.29 CDCR Register (Offset = 1Eh) [Reset = 0102h]

CDCR Register is shown in Table 8-50.

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Table 8-50. CDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Cable Diagnostic Start	R/W	0h	Cable Diagnostic Process Start: Diagnostic Start bit is cleared once Diagnostic Done indication bit is triggered. 0h = Cable Diagnostic is disabled 1h = Start cable measurement
14	cfg_rescal_en	R/W	0h	Resistor calibration Start
13-2	RESERVED	R	40h	
1	Cable Diagnostic Status	R	1h	Cable Diagnostic Process Done: 0h = Cable Diagnostic had not completed 1h = Indication that cable measurement process is complete
0	Cable Diagnostic Test Fail	R	0h	Cable Diagnostic Process Fail: 0h = Cable Diagnostic has not failed 1h = Indication that cable measurement process failed

8.5.1.30 PHYRCR Register (Offset = 1Fh) [Reset = 0000h]

PHYRCR Register is shown in Table 8-51.

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Table 8-51. PHYRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Software Hard Reset	RH/W1S	0h	Software Hard Reset: 0h = Normal Operation 1h = Reset PHY. This bit is self cleared and has the same effect as Hardware reset pin.
14	Digital reset	RH/W1S	0h	Software Restart: 0h = Normal Operation 1h = Restart PHY. This bit is self cleared and resets all PHY circuitry except the registers.
13	RESERVED	R/W	0h	
12-0	RESERVED	R/W	0h	

8.5.1.31 MLEDCR Register (Offset = 25h) [Reset = 0041h]

MLEDCR Register is shown in Table 8-52.

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Table 8-52. MLEDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9	MLED Polarity Swap	R/W	0h	MLED Polarity Swap: The polarity of MLED depends on the routing configuration and the strap on LED1 pin, but only in ENHANCED mode. If the pin strap is Pull-Up then polarity is active low. If the pin strap is Pull-Down then polarity is active high. In BASIC mode, the polarity is always active low.
8-7	RESERVED	R/W	0h	
6-3	LED0 Configuration	R/W	8h	MLED Configurations: Selects the source for LED0 0h = LINK OK 1h = RX/TX Activity 2h = TX Activity 3h = RX Activity 4h = Collision 5h = Speed, High for 100BASE-TX 6h = Speed, High for 10BASE-T 7h = Full-Duplex 8h = LINK OK / BLINK on TX/RX Activity 9h = Active Stretch Signal Ah = MII LINK (100BT+FD) Bh = LPI Mode (EEE) Ch = TX/RX MII Error Dh = Link Lost (remains on until register 0x0001 is read) Eh = Blink for PRBS error (remains ON for single error, remains until counter is cleared) Fh = Reserved
2-1	RESERVED	R	0h	
0	cfg_mled_en	R/W	1h	MLED Route to LED0: 0h = Reserved 1h = Value routed as per MLEDCR[6:3]

8.5.1.32 COMPT Regsiter Register (Offset = 27h) [Reset = 0000h]

COMPT Regsiter is shown in Table 8-53.

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Table 8-53. COMPT Regsiter Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	

Table 8-53. COMPT Regsiter Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	Compliance Test Configuration	R/W	0h	Compliance Test Configuration Select: Bit [4] in Register 0x0027 = 1, Enables 10Base-T Test Patterns Bit [4] in Register 0x0428 = 1, Enables 100Base-TX Test Modes Bits [3:0] select the 10Base-T test pattern, as follows: 0000 = Single NLP 0001 = Single Pulse 1 0010 = Single Pulse 0 0011 = Repetitive 1 0100 = Repetitive 0 0101 = Preamble (repetitive '10') 0110 = Single 1 followed by TP_IDLE 0111 = Single 0 followed by TP_IDLE 1000 = Repetitive '1001' sequence 1001 = Random 10Base-T data 1010 = TP_IDLE_00 1011 = TP_IDLE_01 1100 = TP_IDLE_10 1101 = TP_IDLE_11 100Base-TX Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' ... 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register Note 1: To reconfigure the 100Base-TX Test Mode, bit [4] must be cleared in register 0x0428 and then reset to '1' to configure the new pattern. Note 2: When performing 100Base-TX or 10Base-T tests modes, the speed must be force using the Basic Mode Control Register (BMCR), address 0x0000.

8.5.1.33 10M_CFG Register (Offset = 2Ah) [Reset = 7998h]

10M_CFG is shown in Table 8-54.

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Table 8-54. 10M_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	10M Preamble Mode	R/W	1h	The device supports two preamble size for 10Mbps. - (0) Long Preamble Mode (1) Short Preamble Mode, This does not affect the 100Mbps mode. In Long Preamble mode, "Long" denotes the number of preamble received from MDI. In this mode, the receiver takes up to 7 bytes of preamble to declare this as a valid preamble. The preamble on the MAC can have lesser preambles than the bytes from MDI. The device expects at least 7 bytes of preamble to be on the MDI line. In Short Preamble mode, "Short" denotes the preamble bytes on the MDI line. In this mode, the receiver can work with shorter preambles > 3 bytes. If Link Partner is expected to transfer shorter preamble (< 3 bytes), it is recommended to configure to "Long" preamble mode. 0h = Long Preamble Mode 1h = Short Preamble Mode

Table 8-54. 10M_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-0	RESERVED	R/W	3998h	

8.5.1.34 FLD_CFG1 Register (Offset = 117h) [Reset = 8147h]

FLD_CFG1 is shown in Table 8-55.

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Table 8-55. FLD_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Config MLT3 Error Cnt Len	R/W	20h	MLT3 Error count window. Sets the window in terns if number of clocks (8ns). The counter counts in steady state. 0h = Reserved 1h = 2 cycle 3Fh = 64 cycle
9-4	Config MLT3 Error Number Cnt	R/W	14h	Numbers of MLT3 errors to be counted for link down 0h = Reserved 1h = 1 Error 3Fh = 63 Errors
3-0	RESERVED	R	7h	

8.5.1.35 FLD_CFG2 Register (Offset = 131h) [Reset = 2284h]

FLD_CFG2 is shown in Table 8-56.

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Table 8-56. FLD_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	8Ah	
5-0	Config Scrambler Threshold	R/W	4h	Configures the window to declare link down based on descrambler errors.

8.5.1.36 CDSCR Register (Offset = 170h) [Reset = 0C12h]

CDSCR Register is shown in Table 8-57.

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Table 8-57. CDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	Cable Diagnostic Cross Disable	R/W	0h	Cross TDR Diagnostic Mode: 0h = TDR looks for reflections on channel other than the transmit channel configured by 0x170[13] 1h = TDR looks for reflections on same channel as transmit channel configured by 0x170[13]
13	cfg_tdr_chan_sel	R/W	0h	TDR TX channel select: 0h = Select channel A as transmit channel. 1h = Select channel B as transmit channel.
12	cfg_tdr_dc_rem_no_init	R/W	0h	To make sure DC removal module is not reset before TDR and dc removal is effective on TDR reflection
11	RESERVED	R/W	1h	

Table 8-57. CDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	Cable Diagnostic Average Cycles	R/W	4h	Number of TDR Cycles to Average: 0h = 1 TDR cycle 1h = 2 TDR cycles 2h = 4 TDR cycles 3h = 8 TDR cycles 4h = 16 TDR cycles 5h = 32 TDR cycles 6h = 64 TDR cycles 7h = Reserved
7	RESERVED	R/W	0h	
6-4	cfg_tdr_seg_num	R/W	1h	Selects cable segment on which TDR is to be performed - 000b = Reserved 001b = 0m to 10m 010b = 10m to 20m 011b = 20m to 40m 100b = 40m to 80m 101b = 80m and beyond 110b = Reserved 111b = Reserved
3-0	RESERVED	R/W	2h	

8.5.1.37 CDSCR2 Register (Offset = 171h) [Reset = C850h]

CDSCR2 Register is shown in Table 8-58.

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Table 8-58. CDSCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	C850h	

8.5.1.38 CDSCR3 Register (Offset = 173h) [Reset = 0D04h]

CDSCR3 Register is shown in Table 8-59.

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Table 8-59. CDSCR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_tdr_seg_duration	R/W	Dh	Duration of the segment selected for TDR, calculated by - (Length_in_meters*2*5.2)/8 For Segment #1, 8'hD For Segment #2, 8'hD For Segment #3, 8'h1A For Segment #4, 8'h34 For Segment #5, 8'h8F
7-0	cfg_tdr_initial_skip	R/W	4h	No of samples to be avoided before start of segment configured - For Segment #1, 8'h7 For Segment #2, 8'h14 For Segment #3, 8'h21 For Segment #4, 8'h3B For Segment #5, 8'h6F

8.5.1.39 TDR_175 Register (Offset = 175h) [Reset = 1004h]

TDR_175 Register is shown in Table 8-60.

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Table 8-60. TDR_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	
13-11	cfg_tdr_sdw_avg_loc	R/W	2h	TDR shadow average location - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h2
10-5	RESERVED	R	0h	

Table 8-60. TDR_175 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	R/W	0h	
3-0	cfg_tdr_fwd_shadow	R/W	4h	Length of forward shadow for the segment configured (to avoid shadow of a fault peak be seen as another fault peak) - For Segment #1, 4'h4 For Segment #2, 4'h4 For Segment #3, 4'h5 For Segment #4, 4'h8 For Segment #5, 4'hB

8.5.1.40 TDR_176 Register (Offset = 176h) [Reset = 0005h]

TDR_176 Register is shown in Table 8-61.

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Table 8-61. TDR_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	
4-0	cfg_tdr_p_loc_thresh_seg	R/W	5h	

8.5.1.41 CDSCR4 Register (Offset = 177h) [Reset = 1E00h]

CDSCR4 Register is shown in Table 8-62.

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Table 8-62. CDSCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12-8	Short Cables Threshold	R/W	1Eh	TH to compensate for strong reflections in short cables
7-0	RESERVED	R/W	0h	

8.5.1.42 TDR_178 Register (Offset = 178h) [Reset = 0002h]

TDR_178 Register is shown in Table 8-63.

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Table 8-63. TDR_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	
2-0	cfg_tdr_tx_pulse_width_seg	R/W	2h	TDR TX Pulse width for Segment - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h6

8.5.1.43 CDLRR1 Register (Offset = 180h) [Reset = 0000h]

CDLRR1 Register is shown in Table 8-64.

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Table 8-64. CDLRR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	

Table 8-64. CDLRR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	TD Peak Location 1	R	0h	Location of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

8.5.1.44 CDLRR2 Register (Offset = 181h) [Reset = 0000h]

CDLRR2 Register is shown in Table 8-65.

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Table 8-65. CDLRR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.45 CDLRR3 Register (Offset = 182h) [Reset = 0000h]

CDLRR3 Register is shown in Table 8-66.

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Table 8-66. CDLRR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.46 CDLRR4 Register (Offset = 183h) [Reset = 0000h]

CDLRR4 Register is shown in Table 8-67.

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Table 8-67. CDLRR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.47 CDLRR5 Register (Offset = 184h) [Reset = 0000h]

CDLRR5 Register is shown in Table 8-68.

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Table 8-68. CDLRR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.48 CDLAR1 Register (Offset = 185h) [Reset = 0000h]

CDLAR1 Register is shown in Table 8-69.

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Table 8-69. CDLAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	

Table 8-69. CDLAR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	TD Peak Amplitude 1	R	0h	Amplitude of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

8.5.1.49 CDLAR2 Register (Offset = 186h) [Reset = 0000h]

CDLAR2 Register is shown in Table 8-70.

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Table 8-70. CDLAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.50 CDLAR3 Register (Offset = 187h) [Reset = 0000h]

CDLAR3 Register is shown in Table 8-71.

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Table 8-71. CDLAR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.51 CDLAR4 Register (Offset = 188h) [Reset = 0000h]

CDLAR4 Register is shown in Table 8-72.

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Table 8-72. CDLAR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.52 CDLAR5 Register (Offset = 189h) [Reset = 0000h]

CDLAR5 Register is shown in Table 8-73.

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Table 8-73. CDLAR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	

8.5.1.53 CDLAR6 Register (Offset = 18Ah) [Reset = 0000h]

CDLAR6 Register is shown in Table 8-74.

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Table 8-74. CDLAR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	

Table 8-74. CDLAR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TD Peak Polarity 1	R	0h	Polarity of the First peak discovered by the TDR mechanism on Transmit Channel (TD).
10-6	RESERVED	R	0h	
5	Cross Detect on TD	R	0h	Cross Reflections were detected on TD. Indicate on Short between TD+ and TD-
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1-0	RESERVED	R	0h	

8.5.1.54 MSE_Val Register (Offset = 218h) [Reset = 0000h]

MSE_Val is shown in Table 8-75.

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Table 8-75. MSE_Val Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Mean Square Error	R	0h	Mean square error. Refer to SNLA423 for more details

8.5.1.55 IO_CFG1 Register (Offset = 302h) [Reset = 0X00h]

IO_CFG1 Register is shown in Table 8-76.

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Table 8-76. IO_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	MaC Impedance Control	R/W	0h	MAC Impedance Control: MAC interface impedance control sets the series termination for the digital pins. 0h = Slow Mode 1h = Fast Mode
13	RESERVED	R/W	0h	
12-9	RESERVED	R/W	0h	
8	cfg_crs_dv_vs_rx_dv	RH/W	X	Selects the CRS_DV pin to be operating as CRS_DV or RX_DV in RMII mode. Default value selected by the strap. 0h = RMII_CRS_DV 1h = RMII_RX_DV
7	RESERVED	R/W	0h	
6	cfg_clkout25m_off	R/W	0h	For ENHANCED Mode only : Configure Clockout or LED1 0h = CLKOUT25 available 1h = LED1_GPIO is available
5-0	RESERVED	R	0h	

8.5.1.56 LED0_GPIO_CFG Register (Offset = 303h) [Reset = 0008h]

LED0_GPIO_CFG is shown in Table 8-77.

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Table 8-77. LED0_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	

Table 8-77. LED0_GPIO_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	cfg_led0_clk_sel	R/W	1h	Selects one of the internal clock, for output on LED0. This is enabled when cfg_led0_gpio_ctrl[2:0] = 001b. The possible configurations are: 0h = Reserved 1h = Reserved 2h = Reserved 3h = Reserved 4h = Reserved 5h = PLL Clock out 6h = Recovered Clock 7h = Reserved
2-0	cfg_led0_gpio_ctrl	R	0h	GPIO Configuration for LED0: 0h = LED0 1h = Clock output selected by register field cfg_led0_clk_sel 2h = WoL 3h = 0 4h = Interrupt 5h = 0 6h = 0 7h = 1

8.5.1.57 LED1_GPIO_CFG Register (Offset = 304h) [Reset = 0008h]

LED1_GPIO_CFG is shown in Table 8-78.

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Table 8-78. LED1_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	
5-3	cfg_led1_clk_sel	R/W	1h	Selects one of the internal clock, for output on LED1. This is enabled when cfg_led1_gpio_ctrl[2:0] = 001b. The possible configurations are: 0h = Reserved 1h = Reserved 2h = Reserved 3h = Reserved 4h = Reserved 5h = PLL Clock out 6h = Recovered Clock 7h = Reserved
2-0	cfg_led1_gpio_ctrl	R/W	0h	GPIO Configuration for LED1: 0h = LED1 (default in BASIC mode) 1h = Reserved 2h = WoL 3h = Reserved 4h = Interrupt 5h = TX_ER 6h = CLKOUT25M (default in ENHANCED Mode, selectable by Strap) 7h = Reserved

8.5.1.58 LED2_GPIO_CFG Register (Offset = 305h) [Reset = 0008h]

LED2_GPIO_CFG is shown in Table 8-79.

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Table 8-79. LED2_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	
5-3	RESERVED	R/W	1h	
2-0	cfg_led2_gpio_ctrl	R/W	0h	GPIO Configuration for LED2: 0h = LED2 1h = Reserved 2h = WoL 3h = COL 4h = Interrupt 5h = COL 6h = COL 7h = High

8.5.1.59 LED3_GPIO_CFG Register (Offset = 306h) [Reset = 0008h]

LED3_GPIO_CFG is shown in Table 8-80.

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Table 8-80. LED3_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	
5-3	RESERVED	R/W	1h	
2-0	cfg_led3_gpio_ctrl	R	0h	GPIO Configuration for LED3: 0h = LED3 1h = Reserved 2h = WoL 3h = CRS 4h = Interrupt 5h = CRS 6h = CRS 7h = High

8.5.1.60 CLK_OUT_LED_STATUS register Register (Offset = 308h) [Reset = 0002h]

CLK_OUT_LED_STATUS register is shown in Table 8-81.

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Table 8-81. CLK_OUT_LED_STATUS register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	1h	
0	cfg_clkout_25m_off_status	R	0h	This bit is applicable in ENHANCED mode only 0h = CLKOUT25 available 1h = LED1_GPIO is available

8.5.1.61 VOD_CFG1 Register (Offset = 30Bh) [Reset = 3C00h]

VOD_CFG1 Register is shown in Table 8-82.

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Table 8-82. VOD_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	

Table 8-82. VOD_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	cfg_dac_minus_one_val_mdix_5_to_4	R/W	3h	LD data for mlt3 encoded data of minus one in MDIX mode. The 6 bit data is split into two fields - {cfg_dac_minus_one_val_mdix_5_to_4, cfg_dac_minus_one_val_mdix_3_to_0} 28h = 150% 29h = 143.75% 2Ah = 137.50% 2Bh = 131.25% 2Ch = 125% 2Dh = 118.75% 2Eh = 112.50% 2Fh = 106.25% 30h = 100% 31h = 93.75% 32h = 87.50% 33h = 81.25% 34h = 75% 35h = 68.75% 36h = 62.50% 37h = 56.25% 38h = 50%
11-6	cfg_dac_minus_one_val_mdi	R/W	30h	LD data for mlt3 encoded data of minus one in MDI mode. 28h = 150% 29h = 143.75% 2Ah = 137.50% 2Bh = 131.25% 2Ch = 125% 2Dh = 118.75% 2Eh = 112.50% 2Fh = 106.25% 30h = 100% 31h = 93.75% 32h = 87.50% 33h = 81.25% 34h = 75% 35h = 68.75% 36h = 62.50% 37h = 56.25% 38h = 50%
5-0	cfg_dac_zero_val	R/W	0h	LD data for mlt3 encoded data of zero

8.5.1.62 VOD_CFG2 Register (Offset = 30Ch) [Reset = 0410h]

VOD_CFG2 Register is shown in Table 8-83.

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Table 8-83. VOD_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_dac_minus_one_val_mdix_3_to_0	R/W	0h	LD data for mlt3 encoded data of minus one in MDX mode. 6 bit data is split into two fields - {cfg_dac_minus_one_val_mdix_5_to_4, cfg_dac_minus_one_val_mdix_3_to_0} 28h = 150% 29h = 143.75% 2Ah = 137.50% 2Bh = 131.25% 2Ch = 125% 2Dh = 118.75% 2Eh = 112.50% 2Fh = 106.25% 30h = 100% 31h = 93.75% 32h = 87.50% 33h = 81.25% 34h = 75% 35h = 68.75% 36h = 62.50% 37h = 56.25% 38h = 50%
11-6	cfg_dac_plus_one_val_mdix	R/W	10h	LD data for mlt3 encoded data of plus one in MDIX mode 08h = 50% 09h = 56.25% 0Ah = 62.50% 0Bh = 68.75% 0Ch = 75% 0Dh = 81.25% 0Eh = 87.50% 0Fh = 93.75% 10h = 100% 11h = 106.25% 12h = 112.50% 13h = 118.75% 14h = 125% 15h = 131.25% 16h = 137.50% 17h = 143.75% 18h = 150%
5-0	cfg_dac_plus_one_val_mdi	R/W	10h	LD data for mlt3 encoded data of plus one in MDI mode 08h = 50% 09h = 56.25% 0Ah = 62.50% 0Bh = 68.75% 0Ch = 75% 0Dh = 81.25% 0Eh = 87.50% 0Fh = 93.75% 10h = 100% 11h = 106.25% 12h = 112.50% 13h = 118.75% 14h = 125% 15h = 131.25% 16h = 137.50% 17h = 143.75% 18h = 150%

8.5.1.63 VOD_CFG3 Register (Offset = 30Eh) [Reset = 8400h]

VOD_CFG3 Register is shown in Table 8-84.

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Table 8-84. VOD_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	ld_term_mdi_10M_reg	R/W	8h	10M mode, MDI Termination Value Register 0h = 122 1h = 119 2h = 116 3h = 113 4h = 110 5h = 107 6h = 105 7h = 102 8h = 100 9h = 98 Ah = 96 Bh = 94 Ch = 92 Dh = 90 Eh = 88 Fh = 86
11	ld_term_mdi_10M_en	R/W	0h	10M mode, MDI Termination Value Register Enable 0h = Disable 1h = Enable
10-7	ld_term_mdix_10M_reg	R/W	8h	10M mode, MDIX Termination Value Register 0h = 122 1h = 119 2h = 116 3h = 113 4h = 110 5h = 107 6h = 105 7h = 102 8h = 100 9h = 98 Ah = 96 Bh = 94 Ch = 92 Dh = 90 Eh = 88 Fh = 86
6	ld_term_mdix_10M_en	R/W	0h	10M mode, MDIX Termination Value Register Enable 0h = Disable 1h = Enable
5-2	RESERVED	R/W	0h	
1-0	RESERVED	R	0h	

8.5.1.64 ANA_LD_PROG_SL Register (Offset = 404h) [Reset = 0080h]

ANA_LD_PROG_SL Register is shown in Table 8-85.

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Table 8-85. ANA_LD_PROG_SL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	80h	

8.5.1.65 ANA_RX10BT_CTRL Register (Offset = 40Dh) [Reset = 0008h]

ANA_RX10BT_CTRL Register is shown in Table 8-86.

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Table 8-86. ANA_RX10BT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	
4-0	rx10bt_comp_sl	R/W	8h	10B-T current Gain, common for both POS and NEG, Starting from 200mV to 575mV, step size of 25mV

8.5.1.66 GENCFG Register (Offset = 456h) [Reset = 0008h]

GENCFG Register is shown in Table 8-87.

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Table 8-87. GENCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	
3	Min IPG Enable	R/W	1h	Min IPG Enable: 0h = Minimal IPG set to 200 ns 1h = Enable Minimum Interpacket Gap (IPG is set to 120ns instead of 200ns)
2-0	RESERVED	R/W	0h	

8.5.1.67 LEDCFG Register (Offset = 460h) [Reset = 5665h]

LEDCFG Register is shown in Table 8-88.

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Table 8-88. LEDCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	LED3 Control	R/W	5h	LED3 Control: Selects the source for LED3. 0h = LINK OK 1h = RX/TX Activity 2h = TX Activity 3h = RX Activity 4h = Collision 5h = Speed, High for 100BASE-TX 6h = Speed, High for 10BASE-T 7h = Full-Duplex 8h = LINK OK / BLINK on TX/RX Activity 9h = Active Stretch Signal Ah = MII LINK (100BT+FD) Bh = LPI Mode (Energy Efficient Ethernet) Ch = TX/RX MII Error Dh = Link Lost (remains on until register 0x0001 is read) Eh = Blink for PRBS error (remains ON for single error, remains until counter is cleared) Fh = Reserved

Table 8-88. LEDCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	LED2 Control	R/W	6h	LED2 Control: Selects the source for LED2. 0h = LINK OK 1h = RX/TX Activity 2h = TX Activity 3h = RX Activity 4h = Collision 5h = Speed, High for 100BASE-TX 6h = Speed, High for 10BASE-T 7h = Full-Duplex 8h = LINK OK / BLINK on TX/RX Activity 9h = Active Stretch Signal Ah = MII LINK (100BT+FD) Bh = LPI Mode (Energy Efficient Ethernet) Ch = TX/RX MII Error Dh = Link Lost (remains on until register 0x0001 is read) Eh = Blink for PRBS error (remains ON for single error, remains until counter is cleared) Fh = Reserved
7-4	LED1 Control	R/W	6h	LED1 Control:Selects the source for LED1. 0h = LINK OK 1h = RX/TX Activity 2h = TX Activity 3h = RX Activity 4h = Collision 5h = Speed, High for 100BASE-TX 6h = Speed, High for 10BASE-T 7h = Full-Duplex 8h = LINK OK / BLINK on TX/RX Activity 9h = Active Stretch Signal Ah = MII LINK (100BT+FD) Bh = LPI Mode (Energy Efficient Ethernet) Ch = TX/RX MII Error Dh = Link Lost (remains on until register 0x0001 is read) Eh = Blink for PRBS error (remains ON for single error, remains until counter is cleared) Fh = Reserved
3-0	RESERVED	R/W	5h	

8.5.1.68 IOCTRL Register (Offset = 461h) [Reset = 0010h]

IOCTRL Register is shown in Table 8-89.

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Table 8-89. IOCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	
14	RESERVED	R/W	0h	
13-12	RESERVED	R/W	0h	
11	RESERVED	R/W	0h	
10-7	RESERVED	R/W	0h	
6-5	RESERVED	R/W	0h	
4-0	MAC Impedance Control	R/W	10h	Controls the Slew Rate of the IO. Only LSB is used. 10h = Fast 11h = Slow

8.5.1.69 SOR1 Register (Offset = 467h) [Reset = 0000h]

SOR1 Register is shown in Table 8-90.

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Table 8-90. SOR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10	Strap10	R	0h	Strap on pin#18 0h = active low, 1h = active high
9	Strap9	R	0h	Strap on pin#15 0h = active low, 1h = active high
8	Strap8	R	0h	Strap on pin#14 0h = active low, 1h = active high
7	Strap7	R	0h	Strap on pin#13 0h = active low, 1h = active high
6	Strap6	R	0h	Strap on pin#20 0h = active low, 1h = active high
5	Strap5	R	0h	Strap on pin#22 0h = active low, 1h = active high
4	Strap4	R	0h	Strap on pin#28 0h = active low, 1h = active high
3	Strap3	R	0h	Strap on pin#29 0h = active low, 1h = active high
2	Strap2	R	0h	Strap on pin#30 0h = active low, 1h = active high
1	Strap1	R	0h	Strap on pin#31 0h = active low, 1h = active high
0	Strap0	R	0h	Strap on pin#16 0h = active low, 1h = active high

8.5.1.70 SOR2 Register (Offset = 468h) [Reset = 0287h]

SOR2 Register is shown in Table 8-91.

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Table 8-91. SOR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	

Table 8-91. SOR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	XMII_ISOLATE_EN	R	0h	Applicable in BASIC Mode. Controls the MII Isolation bit field in register BMCR[10] 0h = No Isolation 1h = MAC pins Isolated
13	RESERVED	R	0h	
12	CRS_DV_vs_RX_DV	RH	0h	RMII mode RX_DV pin as CRS_DV or RX_DV 0h = RMI CRS_DV 1h = RMII RX_DV
11	LED_3_POLARITY	RH	0h	LED3 Polarity Detection. Controls the LED3 Polarity 0h = Active Low polarity setting 1h = Active High polarity setting
10	LED_2_POLARITY	RH	0h	LED2 Polarity Detection. Controls the LED2 Polarity 0h = Active Low polarity setting 1h = Active High polarity setting
9	CFG_LED_LINK_POL	RH	1h	Link LED Polarity Detection. Controls the LED0 Polarity 0h = Active Low polarity setting 1h = Active High polarity setting
8	CFG_FLD_EN	RH	0h	Status of Fast Link Drop. 0h = FLD Disabled 1h = FLD Enabled. See CR3[10,3:0] for more information
7	CFG_AMDIX	RH	1h	AMDIX Enable. This captures the inversion of AMDIX_DIS strap 0h = AMDIX Disable 1h = AMDIX Enable
6	RESERVED	R	0h	
5	LED_SPEED_POL	RH	0h	Speed LED Polarity Detection. Controls the LED1 Polarity 0h = Active Low polarity setting 1h = Active High polarity setting
4	CFG_RMII_MODE	RH	0h	MII/RMII mode Selection 0h = MII 1h = RMII
3	CFG_XI_50_FOLLOWER	RH	0h	RMII Leader / Follower mode Selection 0h = RMII Leader Mode 1h = RMII Follower Mode
2	CFG_AN_1	R	1h	This is to derive ANAR register bit [8:5]
1	CFG_AN_0	R	1h	This is to derive ANAR register bit [8:5]
0	CFG_AN_EN	R	1h	ANEG Enable. This captures the inversion of ANEG_DIS

8.5.1.71 LEDCFG2 Register (Offset = 469h) [Reset = 0XXXh]

LEDCFG2 Register is shown in Table 8-92.

Return to the Summary Table.

Table 8-92. LEDCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	
10	RESERVED	RH/W	X	
9	RESERVED	R/W	0h	
8	RESERVED	R/W	0h	
7	RESERVED	R	0h	
6	LED2_polarity	RH/W	X	led 2 polarity 0h = active low, 1h = active high
5	LED2_drv_val	R/W	0h	led 2 drive value

Table 8-92. LEDCFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LED2_drv_en	R/W	0h	led 2 drive enable 0h = Normal operation 1h = drive LED polarity,
3	RESERVED	R	0h	
2	LED1_polarity	RH/W	X	led 1 polarity 0h = active low, 1h = active high
1	LED1_drv_val	R/W	0h	led1 drive value
0	LED1_drv_en	R/W	0h	led 1 drive enable 0h = Normal operation 1h = drive LED polarity,

8.5.1.72 RXFCFG1 Register (Offset = 4A0h) [Reset = 108Xh]

RXFCFG1 Register is shown in Table 8-93.

Return to the Summary Table.

Table 8-93. RXFCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	CRC Gate	R/W	1h	CRC Gate: If Magic Packet has Bad CRC then no indication (status, interrupt, GPIO) when enabled. 0h = Bad CRC does not gate Magic Packet or Pattern Indications 1h = Bad CRC gates Magic Packet and Pattern Indications
11	WoL Level Change Indication Clear	W0C	0h	WoL Level Change Indication Clear: If WoL Indication is set for Level change mode, this bit clears the level upon a write. 0h = Clear
10-9	WoL Pulse Indication Select	R/W	0h	WoL Pulse Indication Select: Only valid when WoL Indication is set for Pulse mode. 0h = 8 clock cycles (of 125MHz clock) 1h = 16 clock cycles 2h = 32 clock cycles 3h = 64 clock cycles
8	WoL Indication Select	R/W	0h	WoL Indication Select: 0h = Pulse mode 1h = Level change mode
7	WoL Enable	R/W	1h	WoL Enable: 0h = normal operation 1h = Enable Wake-on-LAN (WoL)
6	Bit Mask Flag	R/W	0h	Bit Mask Flag
5	Secure-ON Enable	R/W	0h	Enable Secure-ON password for Magic Packets
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	WoL Magic Packet Enable	RH/W	X	Enable Interrupt upon reception of Magic Packet

8.5.1.73 RXFS Register (Offset = 4A1h) [Reset = 1000h]

RXFS Register is shown in Table 8-94.

Return to the Summary Table.

Table 8-94. RXFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	
12	WoL Interrupt Source	R/W	1h	WoL Interrupt Source: Source of Interrupt for bit [1] of register 0x0013. When enabling WoL, this bit is automatically set to WoL Interrupt. 0h = Data Polarity Interrupt 1h = WoL Interrupt
11-8	RESERVED	R	0h	
7	SFD Error	RCH	0h	SFD Error: 0h = No SFD error 1h = Packet with SFD error (without the SFD byte indicated in bit [13] register 0x04A0)
6	Bad CRC	RCH	0h	Bad CRC: 0h = No bad CRC received 1h = Bad CRC was received
5	Secure-On Hack Flag	RCH	0h	Secure-ON Hack Flag: 0h = Valid Secure-ON Password 1h = Invalid Password detected in Magic Packet
4	RESERVED	RCH	0h	
3	RESERVED	RCH	0h	
2	RESERVED	RCH	0h	
1	RESERVED	RCH	0h	
0	WoL Magic Packet Status	RCH	0h	WoL Magic Packet Status:

8.5.1.74 RXFPMD1 Register (Offset = 4A2h) [Reset = 0000h]

RXFPMD1 Register is shown in Table 8-95.

Return to the Summary Table.

Table 8-95. RXFPMD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Destination Address Byte 4	R/W	0h	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC Destination Address Byte 5 (MSB)	R/W	0h	Perfect Match Data: Configured for MAC Destination Address

8.5.1.75 RXFPMD2 Register (Offset = 4A3h) [Reset = 0000h]

RXFPMD2 Register is shown in Table 8-96.

Return to the Summary Table.

Table 8-96. RXFPMD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Destination Address Byte 2	R/W	0h	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC Destination Address Byte 3	R/W	0h	Perfect Match Data: Configured for MAC Destination Address

8.5.1.76 RXFPMD3 Register (Offset = 4A4h) [Reset = 0000h]

RXFPMD3 Register is shown in Table 8-97.

Return to the Summary Table.

Table 8-97. RXFPMD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Destination Address Byte 0	R/W	0h	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC Destination Address Byte 1	R/W	0h	Perfect Match Data: Configured for MAC Destination Address

8.5.1.77 RXFSOP1 Register (Offset = 4A5h) [Reset = 0000h]

RXFSOP1 Register is shown in Table 8-98.

Return to the Summary Table.

Table 8-98. RXFSOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Secure-ON Password Byte 1	R/W	0h	Secure-ON Password Select: Secure-ON password for Magic Packets
7-0	Secure-ON Password Byte 0	R/W	0h	Secure-ON Password Select: Secure-ON password for Magic Packets

8.5.1.78 RXFSOP2 Register (Offset = 4A6h) [Reset = 0000h]

RXFSOP2 Register is shown in Table 8-99.

Return to the Summary Table.

Table 8-99. RXFSOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Secure-ON Password Byte 3	R/W	0h	Secure-ON Password Select: Secure-ON password for Magic Packets
7-0	Secure-ON Password Byte 2	R/W	0h	Secure-ON Password Select: Secure-ON password for Magic Packets

8.5.1.79 RXFSOP3 Register (Offset = 4A7h) [Reset = 0000h]

RXFSOP3 Register is shown in Table 8-100.

Return to the Summary Table.

Table 8-100. RXFSOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Secure-ON Password Byte 5	R/W	0h	Secure-ON Password Select: Secure-ON password for Magic Packets
7-0	Secure-ON Password Byte 4	R/W	0h	Secure-ON Password Select: Secure-ON password for Magic Packets

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warranty the accuracy or completeness of the informatioin. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DP83826 is a single-port 10/100Mbps Ethernet PHY and supports connections to an Ethernet MAC through MII and RMII. Connections to the Ethernet media are made via the IEEE 802.3 defined media-dependent interface.

When using the device for Ethernet applications, certain requirements must be meet for normal operation. The following subsections are intended to assist in appropriate component selection and required circuit connections.

Note

For a step-by-step approach to using the DP83826 BASIC mode in existing systems that use a common standard Ethernet pinout Refer to SNLA338

9.2 Typical Applications

Following figure shows a typical application for the DP83826.

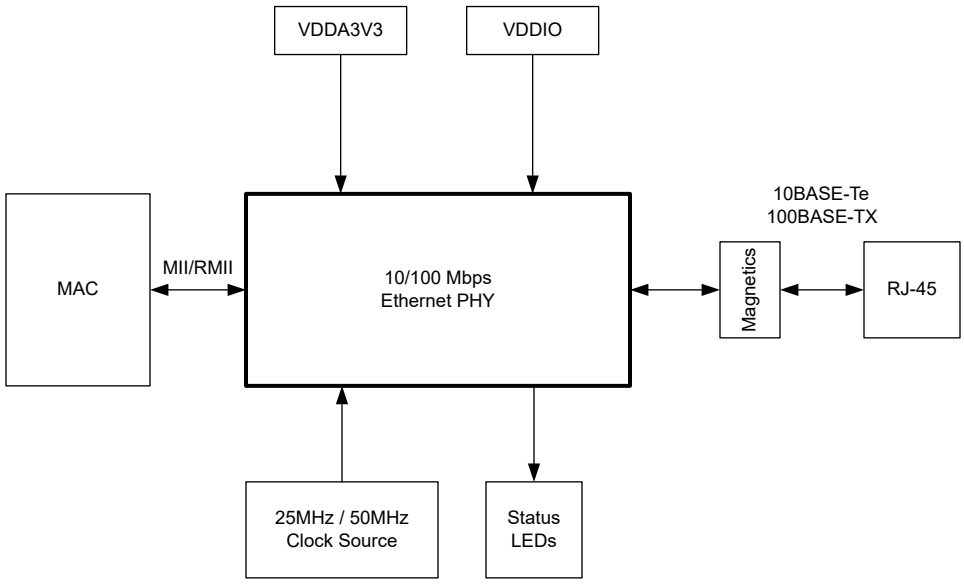


Figure 9-1. Typical DP83826 Application

9.2.1 Twisted-Pair Interface (TPI) Network Circuit

Figure 9-2 shows the recommended twisted-pair interface network circuit for 10Mbps or 100Mbps. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

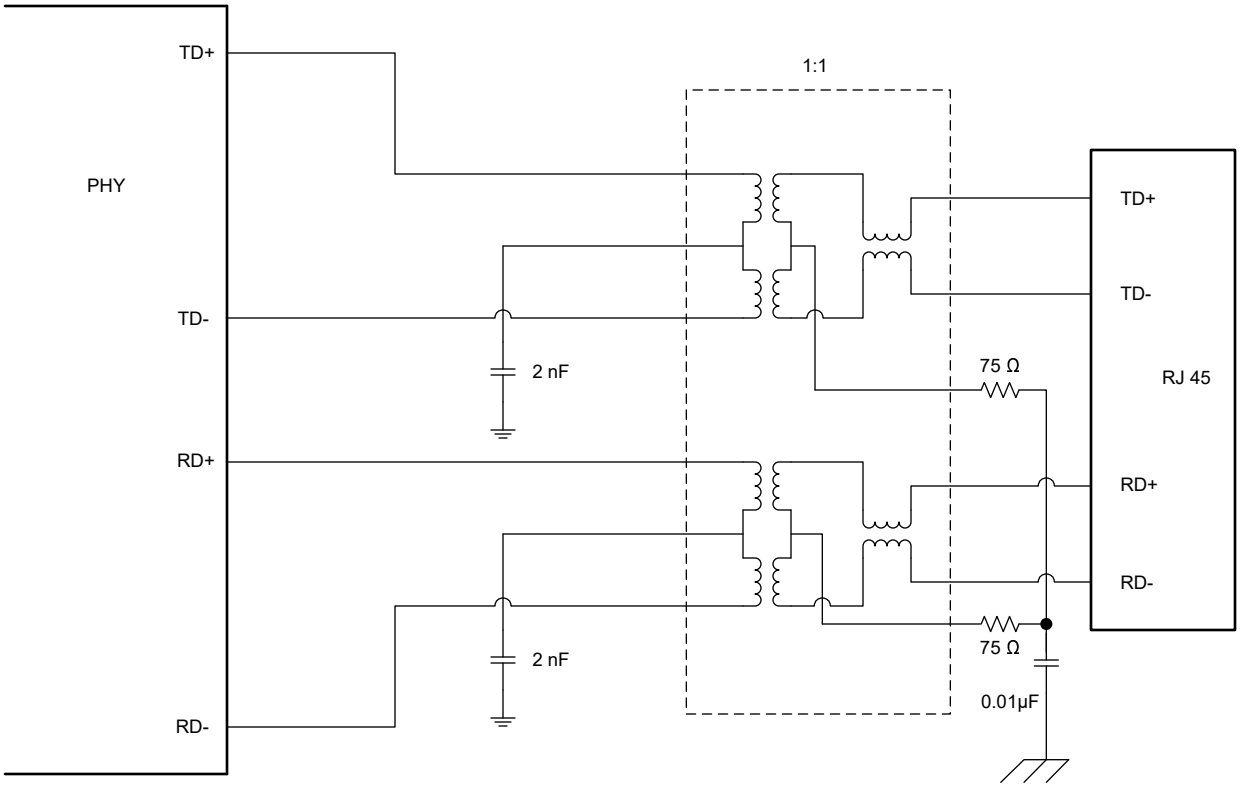


Figure 9-2. TPI Network Circuit

9.2.2 Transformer Recommendations

The following magnetics have been tested using the DP83826.

Table 9-1. Recommended Transformers

MANUFACTURER	PART NUMBER
Pulse electronics	HX1198FNL
	HX1188NL
	HX1188FNL

Table 9-2. Transformer Electrical Specifications

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turn ratio	±2%	1:1	-
Insertion loss	1 to 100MHz	–1	dB
Return loss	1 to 30MHz	–16	dB
	30 to 60MHz	–12	dB
	60 to 80MHz	–10	dB
Differential to common rejection ratio	1 to 50MHz	–30	dB
	50 to 150MHz	–20	dB
Crosstalk	30MHz	–35	dB
	60MHz	–30	dB

Table 9-2. Transformer Electrical Specifications (continued)

PARAMETER	TEST CONDITIONS	TYP	UNIT
Isolation	HPOT	1500	Vrms

9.2.3 Capacitive DC Blocking

To meet the operational requirements of transformer-less network applications, the following design showed in the schematic in Figure 9-3 must be used.

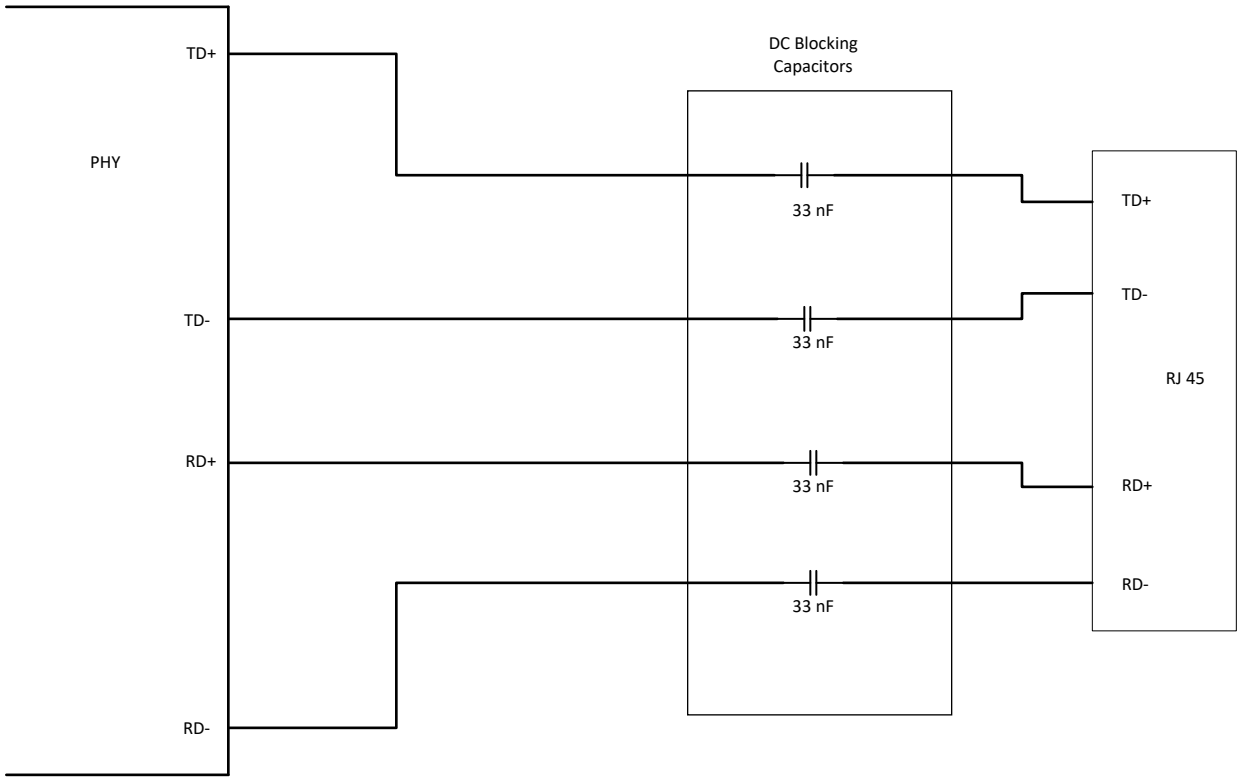


Figure 9-3. Transformerless DC Blocking Configuration

9.2.4 Design Requirements

The design requirements for the DP83826 in TPI operation (100BASE-TX or 10BASE-Te) are:

- VDDA3V3 supply = 3.3V
- VDDIO supply = 3.3V or 1.8V
- Reference clock input = 25MHz or 50MHz (RMII follower)

9.2.4.1 Clock Requirements

The DP83826 supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

9.2.4.1.1 Oscillator

If an external clock source is used, tie XI to the clock source, and leave XO floating. The amplitude of the oscillator clock must be a nominal voltage of VDDIO.

9.2.4.1.2 Crystal

The use of a 25MHz, parallel resonant, 20pF load crystal is recommended if operating with a crystal. See Figure 9-4 for a typical connection diagram for a crystal resonator circuit. The load capacitor values vary with the crystal vendors; check with the vendor for the recommended loads. Refer to the application report *Selection and specification of crystals for Texas Instruments ethernet physical layer transceivers* for more details.

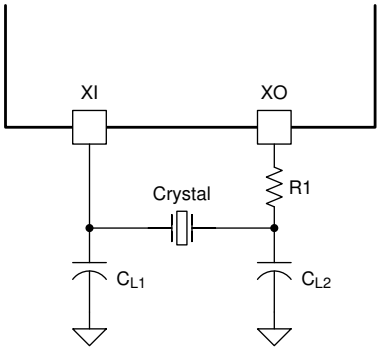


Figure 9-4. Crystal Oscillator Circuit

Table 9-3. 25MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Including operational temperature, aging and other factors	–100		100	ppm
Load capacitance			15	40	pF
ESR				50	Ω

9.2.5 Detailed Design Procedure

9.2.5.1 MII Layout Guidelines

1. MII signals are single-ended signals
2. Route traces with 50Ω impedance to ground
3. Keep trace lengths as short as possible, less than two inches (5-cm) is recommended and less than six inches (15-cm) maximum

9.2.5.2 RMII Layout Guidelines

- RMII signals are single-ended signals
- Route traces with 50Ω impedance to ground
- Keep trace lengths as short as possible, less than two inches (5cm) is recommended and less than six inches (15cm) maximum

9.2.5.3 MDI Layout Guidelines

- MDI signals are differential.
- Route traces with 50Ω impedance to ground and 100Ω differential controlled impedance.
- Route MDI traces to the transformer on the same layer.
- Use a metal shielded RJ-45 connector and electrically connect the shield to chassis ground.
- Avoid supplies and ground beneath the magnetics.
- Do not overlap the circuit ground and chassis ground planes. Keep chassis ground and circuit ground isolated by turning chassis ground into an isolated island by leaving a gap between the planes. Connecting a 1206 (size) capacitor between chassis ground and circuit ground is recommended to avoid floating metal. Capacitors less than 805 (size) can create an arching path for ESD due to a small air-gap.

9.2.6 Application Curves

Figure 9-5 depicts the DP83826 output pin drive characteristics for I/O supply voltages of 1.8V and 3.3V.

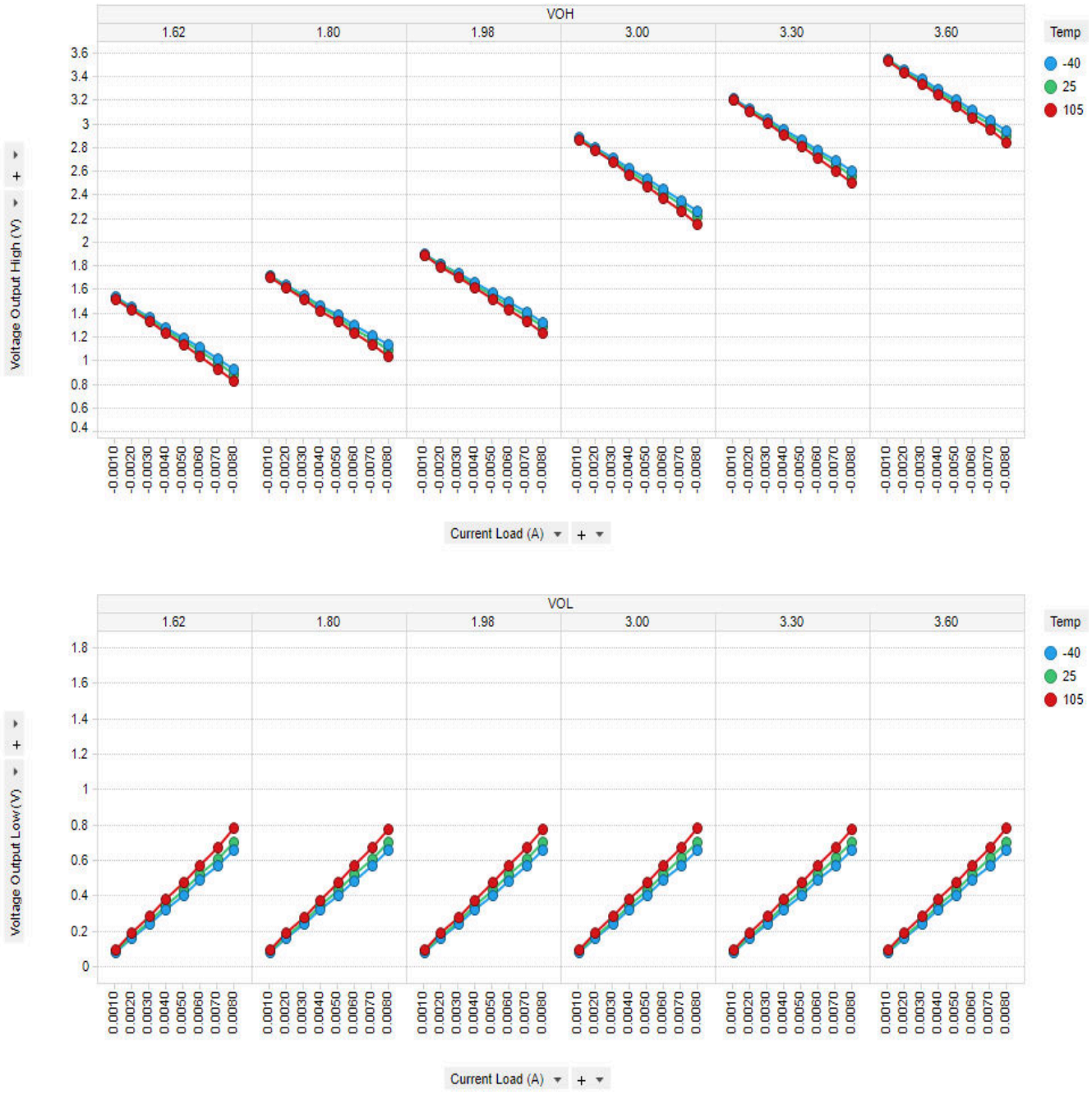


Figure 9-5. DP83826 Output Pin Drive Characteristics

9.3 Power Supply Recommendations

The DP83826 is capable of operating with a 3.3-V or 1.8-V I/O supply voltage along with an analog supply of 3.3-V. If a 3.3-V I/O supply voltage is desired, the DP83826 can also operate on a single 3.3-V power rail. An internal LDO generates all the power rails required for the device to operate. The single voltage supply simplifies

the design requirements, decreases the BOM cost and the overall solution size, making the DP83826 a viable solution in a wide range of applications. The recommended power supply de-coupling network is shown below:

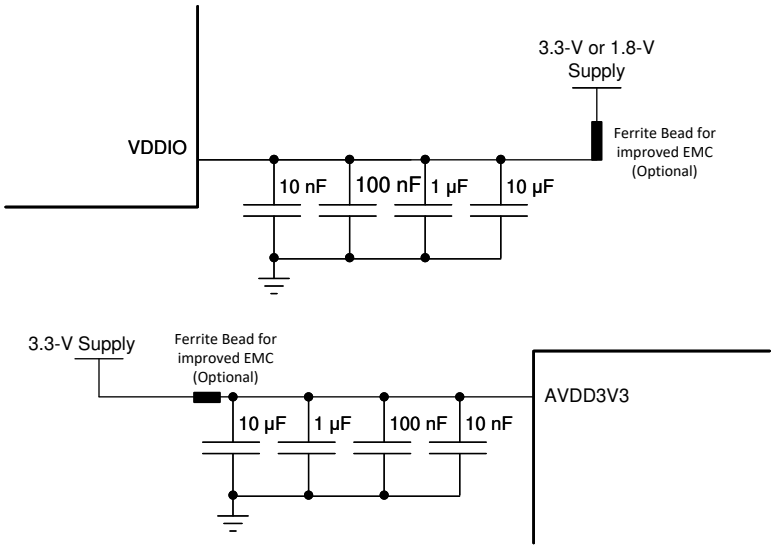


Figure 9-6. Power Supply Decoupling Recommendation

9.4 Layout

9.4.1 Layout Guidelines

Please see DP83826EVM.

9.4.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Keep all traces as short as possible. Unless mentioned otherwise, all signal traces must be 50Ω single-ended impedance. Differential traces must be 100Ω differential. Make sure impedance is controlled throughout. Impedance discontinuities causes reflections leading to emissions and signal integrity issues. Stubs must be avoided on all signal traces, especially differential signal pairs.

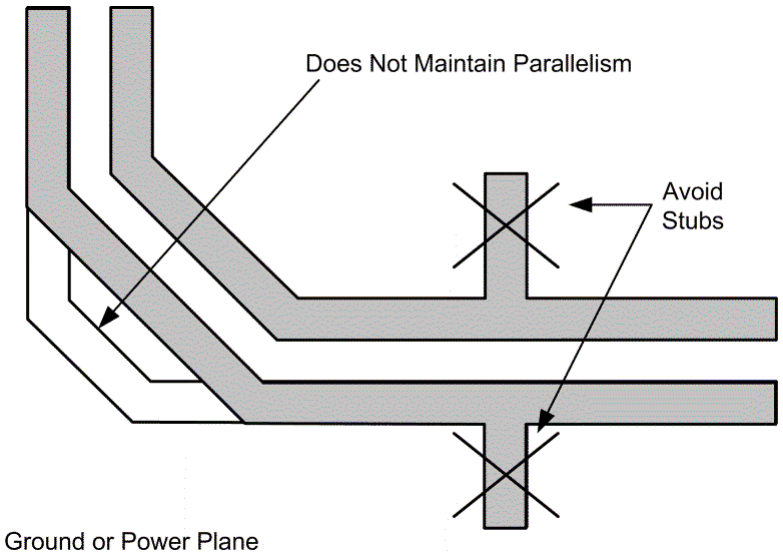


Figure 9-7. Differential Signal Traces

Within the differential pairs, trace lengths must be run parallel to each other and be matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All MII and RMII transmit signal traces must be length matched to each other and all MII and RMII receive signal traces must be length matched to each other.

There must be no crossover or vias on signal path traces. Vias present impedance discontinuities and must be minimized when possible. Route trace pairs on the same layer. Signals on different layers must not cross each other without at least one return path plane between them. Differential pairs must always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

9.4.1.2 Return Path

A general best practice is to have a solid return path beneath all MDI signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Avoid breaks in return path between the signal traces at all cost. A signal crossing a split plane can cause unpredictable return path currents and impact signal quality and result in emissions issues.

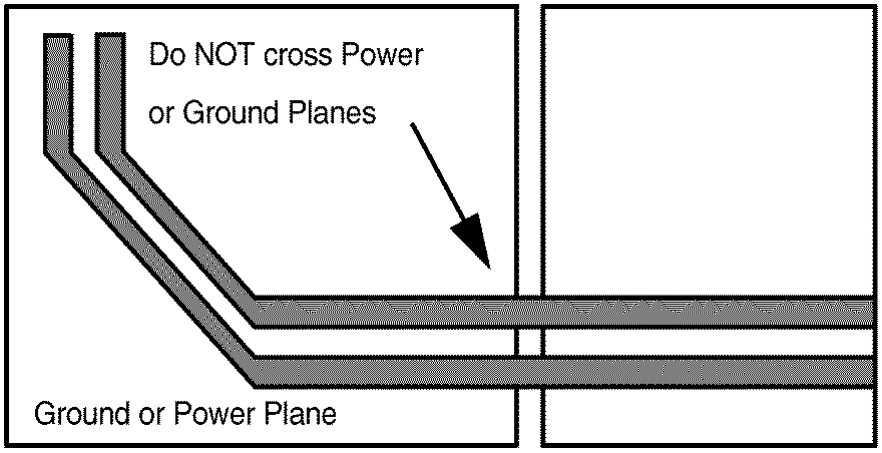


Figure 9-8. Differential Signal Pair and Plane Crossing

9.4.1.3 Transformer Layout

There must be no metal layer running beneath the transformer. Transformers can inject noise into metal beneath them, which can affect the performance of the system. See Figure 9-2.

9.4.1.4 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

9.4.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, use a six-layer PCB when possible.

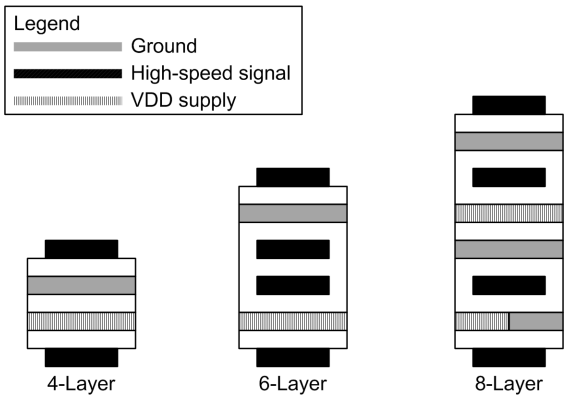


Figure 9-9. Recommended Layer Stack-Up

9.4.1.5.1 Layout Example

See the DP83826EVM for more information regarding layout.

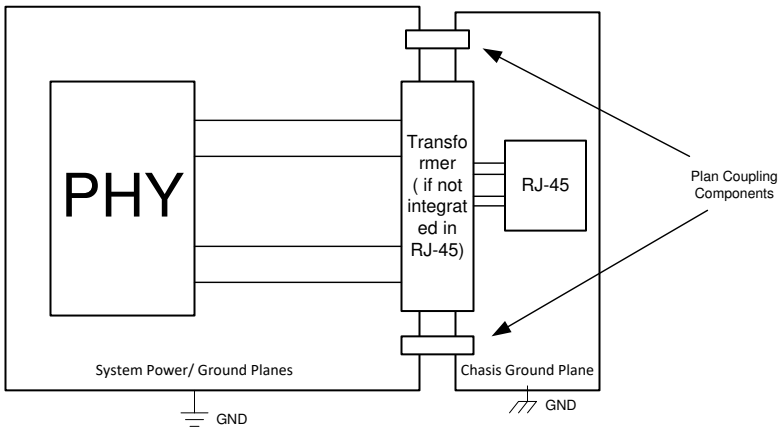


Figure 9-10. Layout Example

10 Device and Documentation Support

10.1 Related Documentation

For related documentation see the following:

Time Domain Reflectometry with DP83826

DP83826 Troubleshooting Guide

Selection and specification of crystals for Texas Instruments ethernet physical layer transceivers

Chinese and English Definitions of Acronyms Related to Ethernet Products

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

10.4 Trademarks

Magic Packet™ is a trademark of Advanced Micro Devices, Inc..
EtherCAT® is a registered trademark of Beckhoff Automation GmbH, Germany.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (July 2023) to Revision H (May 2025)	Page
• Changed master to leader throughout the document	1
• Changed slave to follower throughout the document	1
• Change pin 21 TYPE from Active: I to Active: I/O	4
• Change pin 21 TYPE from Active: I to Active: O	7
• Changed T2 to T4 in the *RMII Receive Timing* graphic	18
• Change LED pull-down resistor from 5k to 1.5k in basic mode	47
• Add LED example strap connections	47
• Update master and slave to leader/follower	50
• When Mode = 0 in BASIC Mode *PHY Address Strap* table, changed PHY_ADD0 = 1 from PHY_ADD0 = 0.	53
• When Mode = 1 in BASIC Mode *PHY Address Strap* table, changed PHY_ADD0 = 0 from PHY_ADD0 = 1.	53

Changes from Revision F (November 2022) to Revision G (July 2023)	Page
• Adjusted tables to clarify accurate representation of device performance	3
• Corrected pin 16 reset state. Clarified pin 31 functionality	4

- Adjusted pin 20 and 21 description 7
- Clarified how to disable CLKOUT 31
- Adjusted hyperlink to app note 44
- Revised description of which configurations are used to control respective mechanisms of FLD. Simplified table description 45
- Updated flowchart 50
- Clarified Strap6 and Strap1 are both latched at POR only 50
- Consolidated and clarified MAC Mode Selection Strap Table 53
- Updated device registers 54
- Updated links 104

Changes from Revision E (February 2022) to Revision F (November 2022) **Page**

- Corrected Reset states for RX_D3, LED0 7
- Updated thermal metric 11
- Adjusted *Power-Up Timing (Power Sequencing)* graphic 18
- Adjusted *RMII Repeater Mode: Leader-Follower* and *RMII Repeater Mode: Follower-Follower* graphics 29
- Clarified MDIO pullup resistor values 35
- Changed Rlo strap for internal PU pin to 1.5kΩ. Added recommended tolerance for resistor values 49
- Added *Enhanced Bootstrap Flowchart* graphic 50
- Corrected Strap0 default and functionality in Enhanced Mode 50
- Updated device registers 54
- Adjusted location of *Transformer Recommendations* 97

Changes from Revision D (October 2020) to Revision E (February 2022) **Page**

- Pin 31 default is changed to LED1, added odd nibble detection and FLD detection mechanisms in hardware bootstrap differences table 3
- Added TX_ER to pin 28 4
- Pin 31 default is changed to LED1 7
- Pin 31 default is changed to LED1, updated pin 16 and pin 31 to PU 7
- Added fast link drop modes table, updated description for fast link drop functionality in Included specification for the different defaults between enhanced and basic mode, added strap8 description 45
- Added description that LED1/0 are autopolarity (enhanced), active low by default (basic) 47
- Added odd nibble detection table, added strap7 and strap1 interaction to MII MAC mode strap table, added signal energy alternate function to strap8 50
- Pin 31 default is changed to LED1, pin 16 default changed to half duplex 53
- TPI network cap updates 97

Changes from Revision C (July 2020) to Revision D (October 2020) **Page**

- Updated Electrical Characteristics table 10
- Added section 98

Changes from Revision B (March 2020) to Revision C (July 2020) **Page**

- Added link to SNLA338 application note 3
- Added link to SNLA338 24
- Energy Efficient Ethernet section 26
- EEE Overview section 26

- EEE Negotiation section....27
- Added EEE for Legacy MACs Not Supporting 802.3az section....27
- Updated device registers....54
- Added link to SNLA338 application note....96

Changes from Revision A (February 2020) to Revision B (March 2020) **Page**

- Added DP83826I temperature range in Electrical Section also....1
- Added DP83826I to Device Family Information table....1

Changes from Revision * (January 2020) to Revision A (February 2020) **Page**

- Added link to DP83826EVM User's Guide....1
- Deleted pin 18 from Table 4-2....3
- Changed ENHANCED Mode pin map and pin functions table to match pin names....4
- Changed BASIC Mode pin map and pin functions table to match pin names....7
- Deleted "This pin can be configured to RX_DV in RMII mode to enable RMII Repeater Mode." from Pin Functions (BASIC Mode)....7
- Added the *100BASE-TX Transmit Latency Timing* graphic....18
- Added the *100BASE-TX Receive Latency Timing* graphic....18
- Added steps to disable CLKOUT via register configuration in Section 8.3.8....31
- Deleted mentions of "clause 45" from Section 8.3.11 and Section 8.3.11.1....35
- Deleted "Analog Loopback requires 100Ω terminations across pins 1 and 2 as well as 100Ω terminations across pins 3 and 6 at the RJ45." from Section 8.3.14.5....43
- Added row for RMII follower mode configuration in *MAC Mode Selection Strap Table*....53

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83826ERHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	826E
DP83826ERHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	826E
DP83826ERHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	826E
DP83826ERHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	826E
DP83826IRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	826I
DP83826IRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	826I
DP83826IRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	826I
DP83826IRHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	826I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

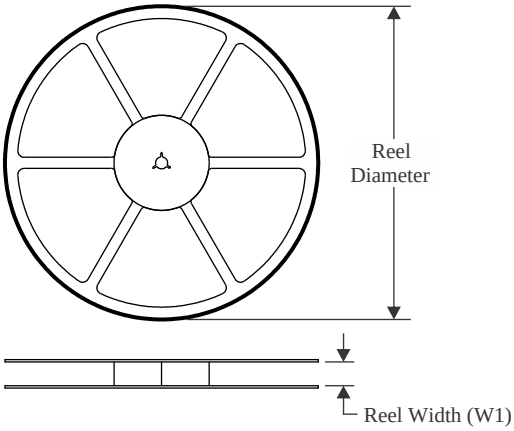
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

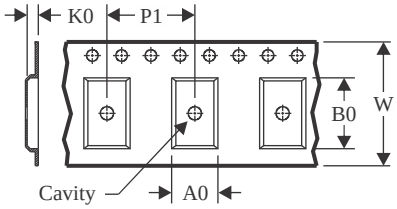
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

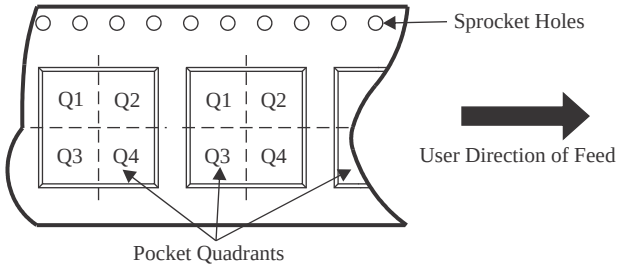


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

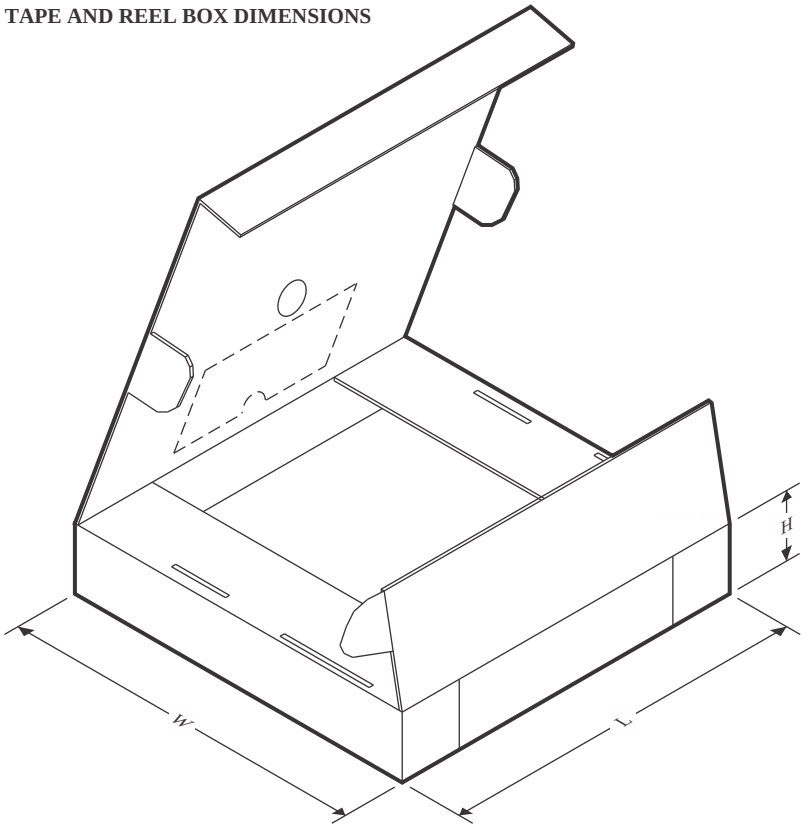
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83826ERHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DP83826ERHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DP83826IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DP83826IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83826ERHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83826ERHBT	VQFN	RHB	32	250	210.0	185.0	35.0
DP83826IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83826IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

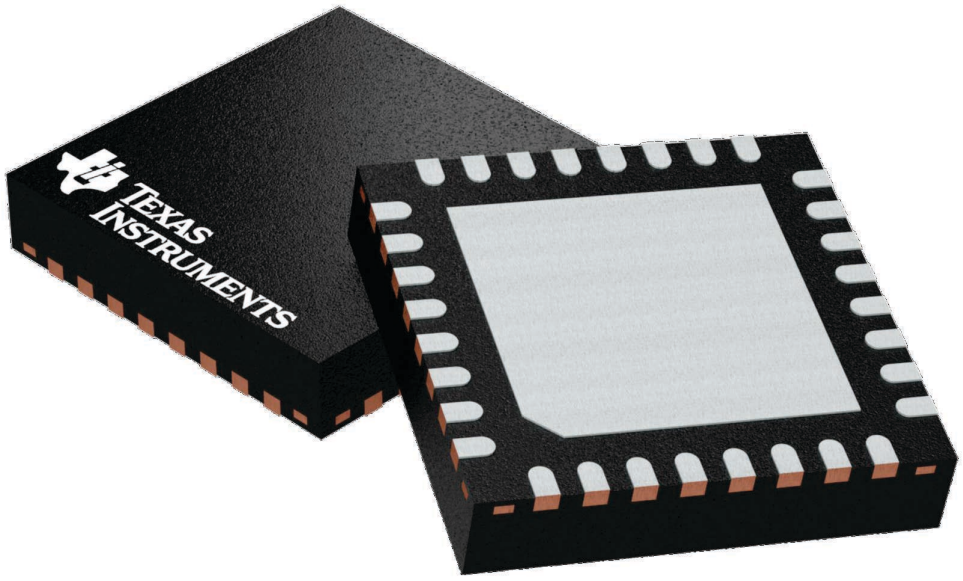
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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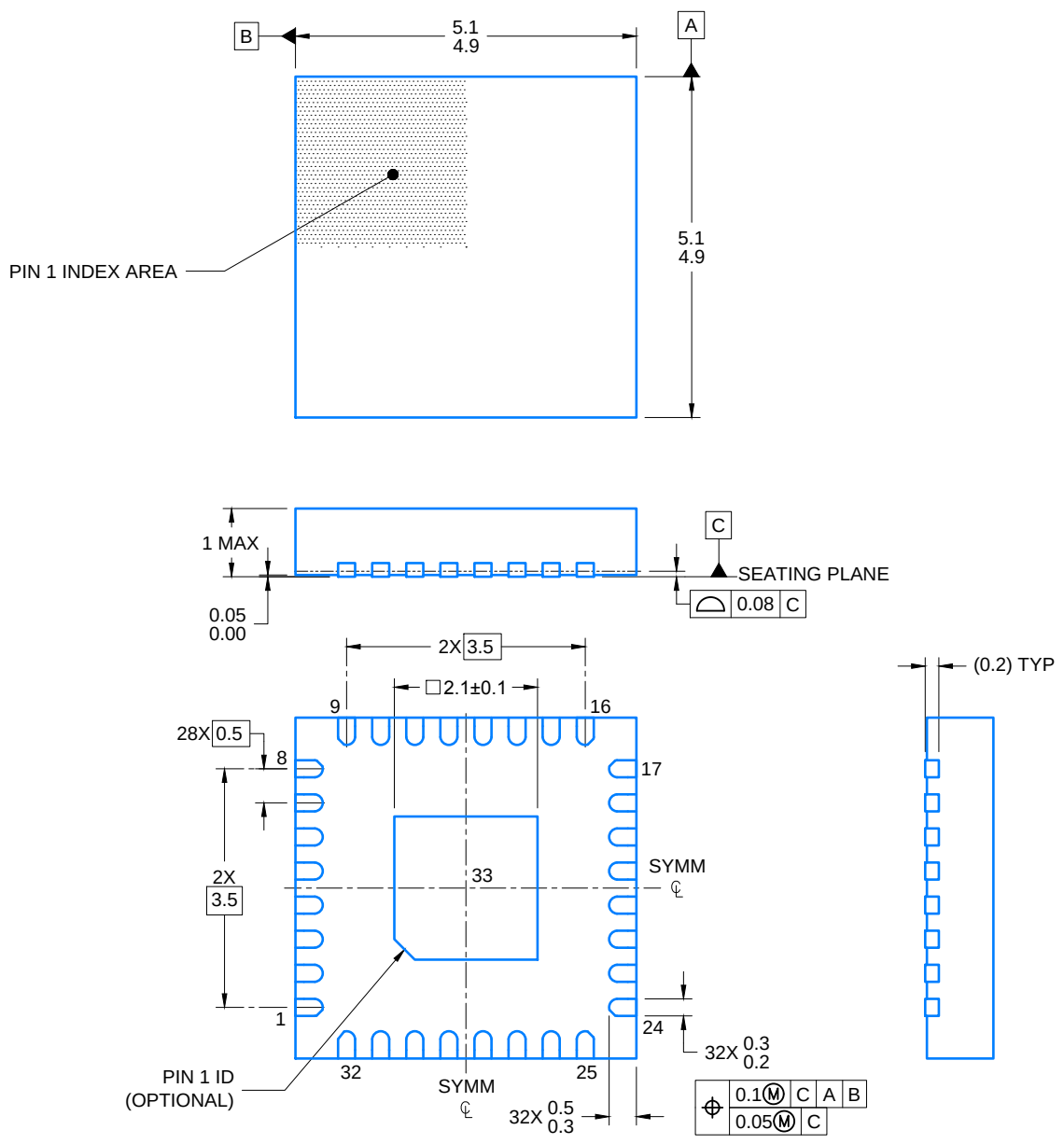
PACKAGE OUTLINE

RHB0032M

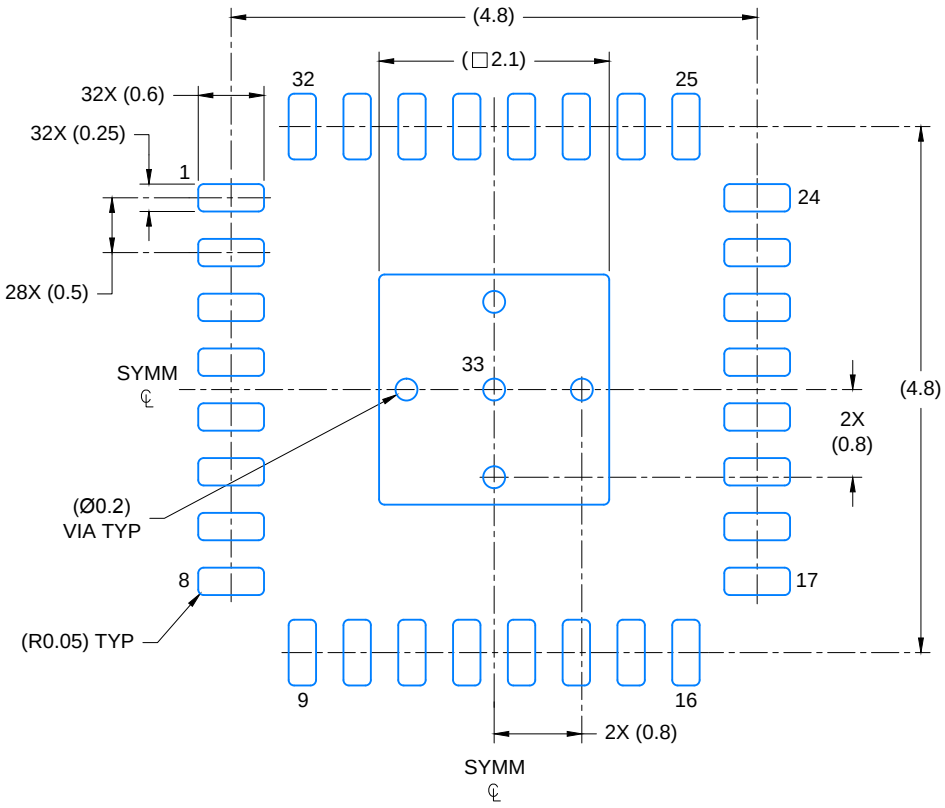
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

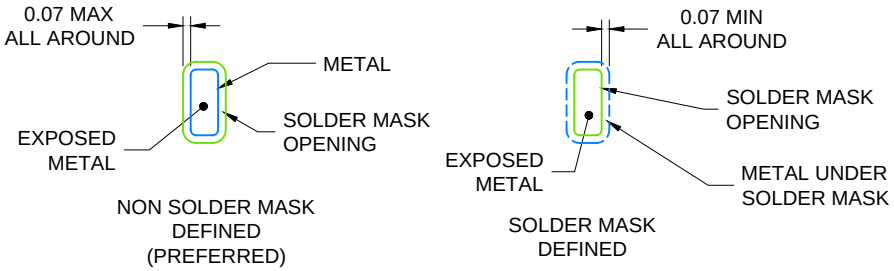


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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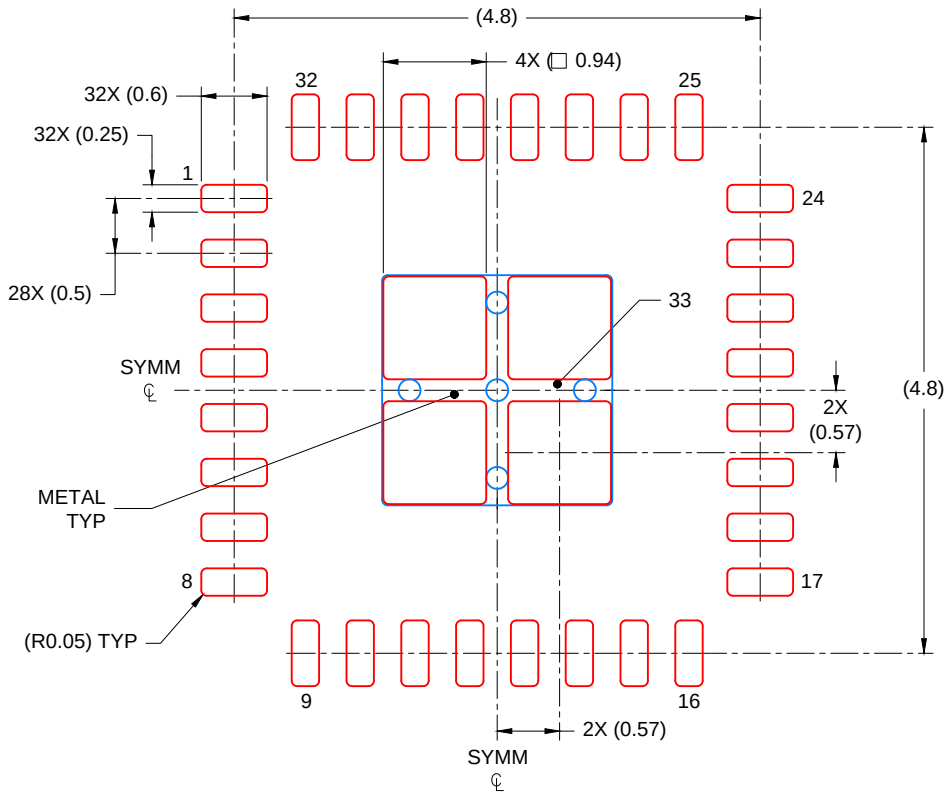
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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