DP83640 Precision PHYTER™ - IEEE 1588 Precision Time Protocol Transceiver

1 Device Overview

1.1 Features

- IEEE 1588 V1 and V2 Supported
- UDP/IPv4, UDP/IPv6, and Layer2 Ethernet Packets Supported
- IEEE 1588 Clock Synchronization
- Timestamp Resolution of 8 ns
- Allows Sub 10-ns Synchronization to Master Reference
- 12 IEEE 1588 GPIOs for Trigger or Capture
- Deterministic, Low Transmit and Receive Latency
- Selectable Frequency Synchronized Clock Output
- Dynamic Link Quality Monitoring
- TDR Based Cable Diagnostic and Cable Length Detection
- 10/100 Mb/s Packet BIST (Built-in Self Test)
- Error-Free Operation up to 150 Meters CAT5 Cable
- ESD Protection - 8 kV Human Body Model
- 2.5-V and 3.3-V I/Os and MAC Interface
- Auto-MDIX for 10/100 Mbps
- RMII Rev. 1.2 and MII MAC Interface
- 25-MHz MDC and MDIO Serial Management Interface
- IEEE 802.3 100BASE-FX Fiber Interface
- IEEE 1149.1 JTAG
- Programmable LED Support for Link, 10/100 Mb/s Mode, Duplex, Activity, and Collision Detect
- Optional 100BASE-TX Fast Link-loss Detection
- Industrial Temperature Range
- 48-pin LQFP Package (7 mm × 7 mm)

1.2 Applications

- Factory Automation
  - Ethernet/IP
  - CIP Sync
- Test and Measurement
  - LXI Standard
- Telecom
  - Basestation
- Real Time Networking

1.3 Description

The DP83640 Precision PHYTER™ device delivers the highest level of precision clock synchronization for real time industrial connectivity based on the IEEE 1588 standard. The DP83640 has deterministic, low latency and allows choice of microcontroller with no hardware customization required. The integrated 1588 functionality allows system designers the flexibility and precision of a close to the wire timestamp. The three key 1588 features supported by the device are:

- Packet time stamps for clock synchronization
- Integrated IEEE 1588 synchronized clock generation
- Synchronized event triggering and time stamping through GPIO

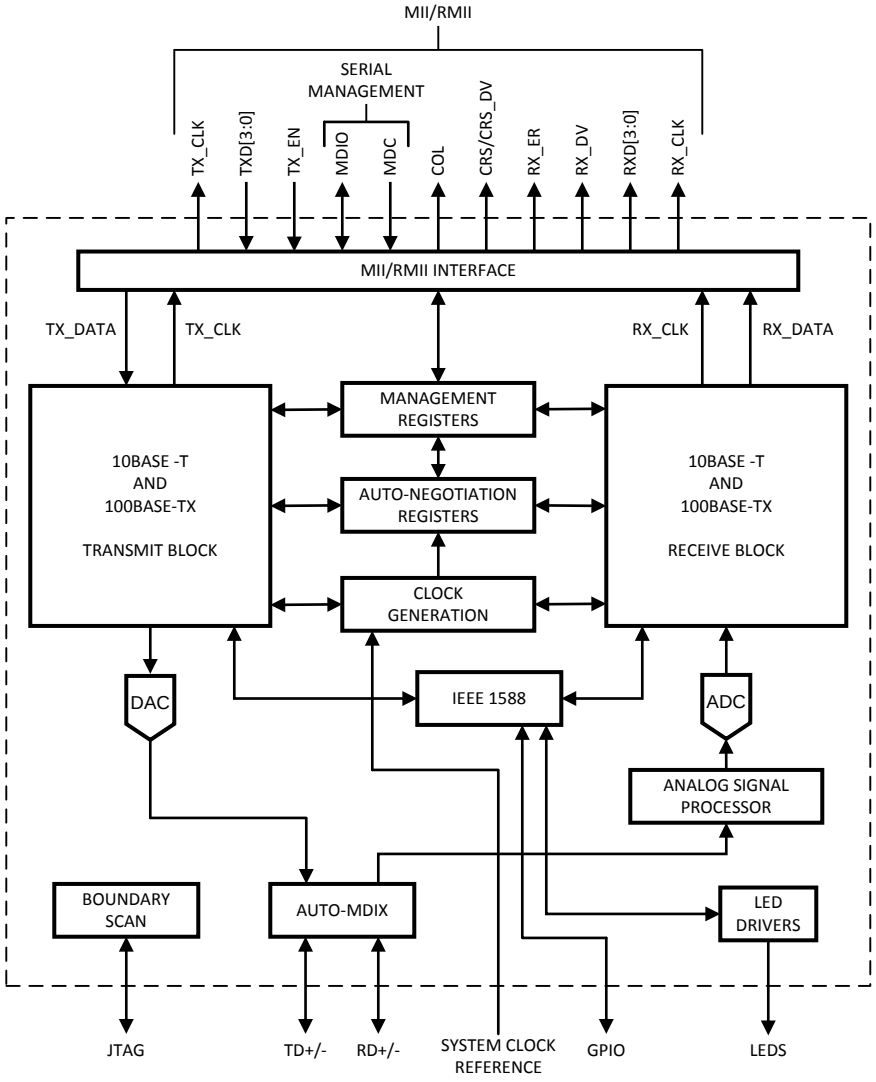
DP83640 offers innovative diagnostic features unique to Texas Instruments, including dynamic monitoring of link quality during standard operation for fault prediction. These advanced features allow the system designer to implement a fault prediction mechanism to detect and warn of deteriorating and changing link conditions. This single port fast Ethernet transceiver can support both copper and fiber media.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DP83640	LQFP (48)	7.00 mm × 7.00 mm

(1) For more information, see Section 8, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram



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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision D (April 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format 112

3 Pin Configuration and Functions

The DP83640 pins are classified into the following interface categories (each interface is described in the sections that follow):

- Serial Management Interface
- MAC Data Interface
- Clock Interface
- LED Interface
- IEEE 1588 Event/Trigger/Clock Interface
- JTAG Interface
- Reset and Power Down
- Strap Options
- 10/100 Mb/s PMD Interface
- Power Supply Pins

NOTE

Strapping pin option. See *Section 3.10* for strap definitions.

All DP83640 signal pins are I/O cells regardless of the particular use. The definitions below define the functionality of the I/O cells for each pin.

Type: I Input

Type: O Output

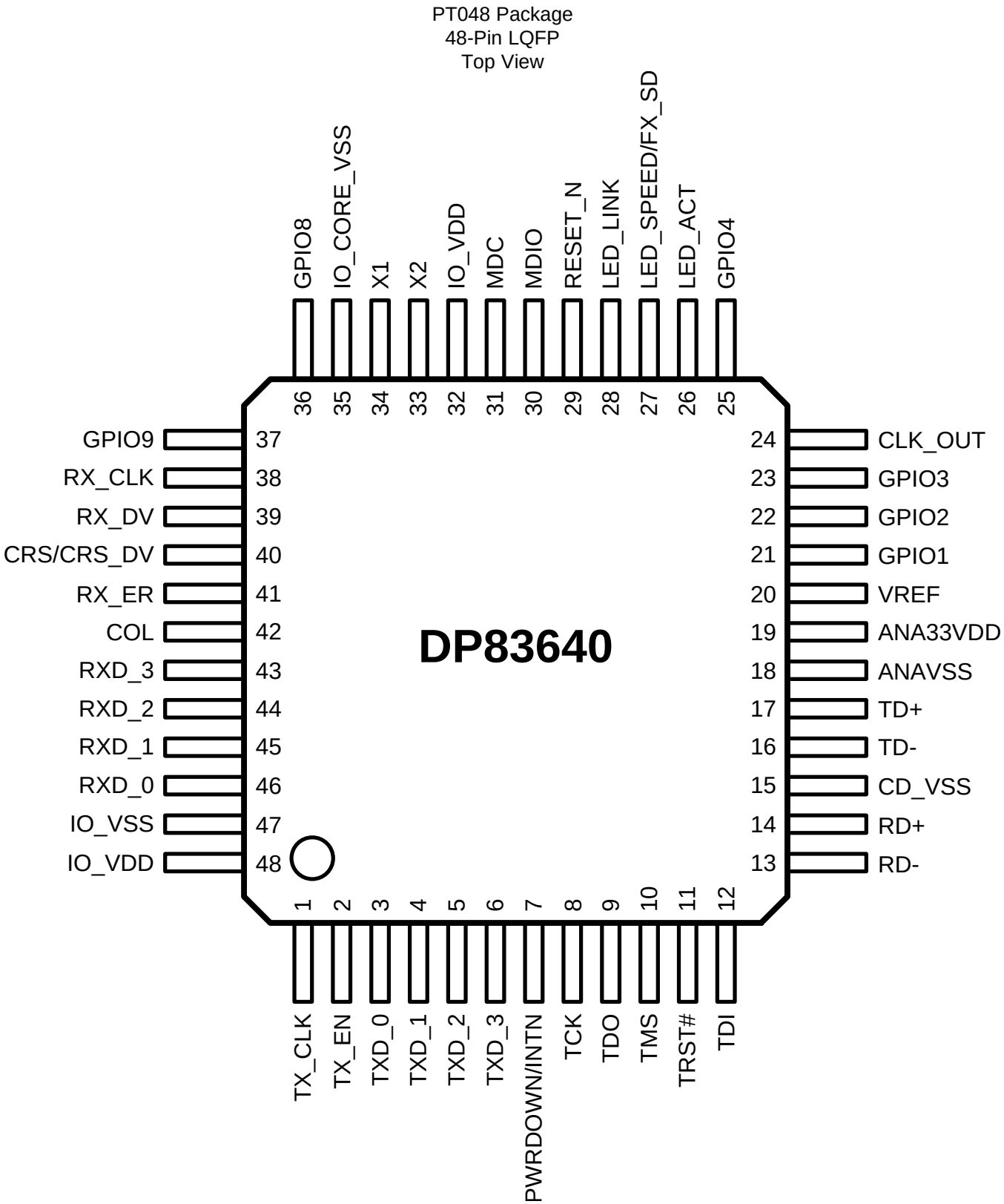
Type: I/O Input/Output

Type: OD Open Drain

Type: PD,PU Internal Pulldown/Pullup

Type: S Strapping Pin (All strap pins have weak internal pullups or pulldowns. If the default strap value is to be changed then an external 2.2-kΩ resistor should be used. See *Section 3.10* for details.)

3.1 Pin Layout



3.2 Package Pin Assignments

PIN		PIN	
NAME	NO.	NAME	NO.
ANA33VDD	19	RESET_N	29
ANAVSS	18	RX_CLK	38
CD_VSS	15	RX_DV	39
CLK_OUT	24	RX_ER	41
COL	42	RXD_0	46
CRS/CRS_DV	40	RXD_1	45
GPIO1	21	RXD_2	44
GPIO2	22	RXD_3	43
GPIO3	23	TCK	8
GPIO4	25	TD-	16
GPIO8	36	TD+	17
GPIO9	37	TDI	12
IO_CORE_VSS	35	TDO	9
IO_VDD	32	TRST#	11
IO_VDD	48	TX_CLK	1
IO_VSS	47	TX_EN	2
LED_ACT	26	TXD_0	3
LED_LINK	28	TXD_1	4
LED_SPEED/FX_SD	27	TXD_2	5
MDC	31	TXD_3	6
MDIO	30	TMS	10
PWRDOWN/INTN	7	VREF	20
RD-	13	X1	34
RD+	14	X2	33

3.3 Serial Management Interface (SMI)

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
MDC	MDC	I	31	**MANAGEMENT DATA CLOCK:** Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 25 MHz with no minimum clock rate.
MDIO	MDIO	I/O	30	**MANAGEMENT DATA I/O:** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 1.5-kΩ pullup resistor. Alternately, an internal pullup may be enabled by setting bit 3 in the CDCTRL1 register.

3.4 MAC Data Interface

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
TX_CLK	TX_CLK	O	1	**MII TRANSMIT CLOCK:** 25-MHz Transmit clock output in 100 Mb/s mode or 2.5 MHz in 10 Mb/s mode derived from the 25-MHz reference clock. The MAC should source TX_EN and TXD[3:0] using this clock. **RMII MODE:** Unused in RMII Slave mode. The device uses the X1 reference clock input as the 50 MHz reference for both transmit and receive. For RMII Master mode, the device outputs the internally generated 50-MHz reference clock on this pin. This pin provides an integrated 50-Ω signal termination, making external termination resistors unnecessary.
TX_EN	TX_EN	I, PD	2	**MII TRANSMIT ENABLE:** Active high input indicates the presence of valid data inputs on TXD[3:0]. **RMII TRANSMIT ENABLE:** Active high input indicates the presence of valid data on TXD[1:0].

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
TXD_0 TXD_1 TXD_2 TXD_3	TXD_0 TXD_1 TXD_2 TXD_3	I I I I, PD	3 4 5 6	**MII TRANSMIT DATA:** Transmit data MII input pins, TXD[3:0], that accept data synchronous to the TX_CLK (2.5 MHz in 10 Mb/s mode or 25 MHz in 100 Mb/s mode). **RMII TRANSMIT DATA:** Transmit data RMII input pins, TXD[1:0], that accept data synchronous to the 50-MHz reference clock.
RX_CLK	RX_CLK	O	38	**MII RECEIVE CLOCK:** Provides the 25-MHz recovered receive clocks for 100 Mb/s mode and 2.5 MHz for 10 Mb/s mode. **RMII MODE:** Unused in RMII Slave mode. The device uses the X1 reference clock input as the 50-MHz reference for both transmit and receive. For RMII Master mode, the device outputs the internally generated 50-MHz reference clock on this pin. This pin provides an integrated 50-Ω signal termination, making external termination resistors unnecessary.
RX_DV	RX_DV	O, PD	39	**MII RECEIVE DATA VALID:** Asserted high to indicate that valid data is present on the corresponding RXD[3:0]. **RMII RECEIVE DATA VALID:** This signal provides the RMII Receive Data Valid indication independent of Carrier Sense. This pin provides an integrated 50-Ω signal termination, making external termination resistors unnecessary.
RX_ER	RX_ER	S, O, PU	41	**MII RECEIVE ERROR:** Asserted high synchronously to RX_CLK to indicate that an invalid symbol has been detected within a received packet in 100 Mb/s mode. **RMII RECEIVE ERROR:** Asserted high synchronously to X1 whenever a media error is detected, and RX_DV is asserted in 100 Mb/s mode. This pin is not required to be used by a MAC in RMII mode because the PHY is required to corrupt data on a receive error. This pin provides an integrated 50-Ω signal termination, making external termination resistors unnecessary.
RXD_0 RXD_1 RXD_2 RXD_3	RXD_0 RXD_1 RXD_2 RXD_3	S, O, PD	46 45 44 43	**MII RECEIVE DATA:** Nibble wide receive data signals driven synchronously to the RX_CLK (25 MHz for 100 Mb/s mode, 2.5 MHz for 10 Mb/s mode). RXD[3:0] signals contain valid data when RX_DV is asserted. **RMII RECEIVE DATA:** 2-bits receive data signals, RXD[1:0], driven synchronously to the 50-MHz reference clock. These pins provide integrated 50-Ω signal terminations, making external termination resistors unnecessary.
CRS/CRS_DV	CRS/CRS_DV	S, O, PU	40	**MII CARRIER SENSE:** Asserted high to indicate the receive medium is non-idle. **RMII CARRIER SENSE/RECEIVE DATA VALID**: This signal combines the RMII Carrier and Receive Data Valid indications. For a detailed description of this signal, see the RMII Specification. This pin provides an integrated 50-Ω signal termination, making external termination resistors unnecessary.
COL	COL	S, O, PU	42	**MII COLLISION DETECT:** Asserted high to indicate detection of a collision condition (simultaneous transmit and receive activity) in 10 Mb/s and 100 Mb/s Half-Duplex Modes. While in 10BASE-T Half-Duplex mode with heartbeat enabled this pin is also asserted for a duration of approximately 1 µs at the end of transmission to indicate heartbeat (SQE test). In Full-Duplex Mode, for 10 Mb/s or 100 Mb/s operation, this signal is always logic 0. There is no heartbeat function during 10 Mb/s full-duplex operation. **RMII COLLISION DETECT:** Per the RMII Specification, no COL signal is required. The MAC will recover CRS from the CRS_DV signal and use that along with its TX_EN signal to determine collision. This pin provides an integrated 50-Ω signal termination, making external termination resistors unnecessary.

3.5 Clock Interface

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
X1	X1	I	34	**CRYSTAL/OSCILLATOR INPUT:** This pin is the primary clock reference input for the DP83640 and must be connected to a 25-MHz 0.005% (±50 ppm) clock source. The DP83640 supports either an external crystal resonator connected across pins X1 and X2 or an external CMOS-level oscillator source connected to pin X1 only. **RMII REFERENCE CLOCK:** For RMII Slave Mode, this pin must be connected to a 50-MHz 0.005% (±50 ppm) CMOS-level oscillator source. In RMII Master Mode, a 25-MHz reference is required, either from an external crystal resonator connected across pins X1 and X2 or from an external CMOS-level oscillator source connected to pin X1 only.
X2	X2	O	33	**CRYSTAL OUTPUT:** This pin is the primary clock reference output to connect to an external 25-MHz crystal resonator device. This pin must be left unconnected if an external CMOS oscillator clock source is used.
CLK_OUT	CLK_OUT	I/O, PD	24	**CLOCK OUTPUT:** This pin provides a highly configurable system clock, which may have one of four sources: 1. Relative to the internal PTP clock, with a default frequency of 25 MHz (default) 2. 50-MHz RMII reference clock in RMII Master Mode 3. 25-MHz Receive Clock (same as RX_CLK) in 100-Mb mode 4. 25-MHz or 50-MHz pass-through of X1 reference clock **CLOCK INPUT:** This pin is used to input an external IEEE 1588 reference clock for use by the IEEE 1588 logic. The CLK_OUT_EN strap should be disabled in the system to prevent possible contention. The PTP_CLKSRC register must be configured prior to enabling the IEEE 1588 function in order to allow correct operation.

3.6 LED Interface

The DP83640 supports three configurable LED pins. The LEDs support two operational modes which are selected by the LED mode strap and a third operational mode which is register configurable. The definitions for the LEDs for each mode are detailed below.

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
LED_LINK	LED_LINK	S, O, PU	28	**LINK LED:** In Mode 1, this pin indicates the status of the LINK. The LED will be ON when Link is good. **LINK/ACT LED:** In Mode 2 and Mode 3, this pin indicates transmit and receive activity in addition to the status of the Link. The LED will be ON when Link is good. It will blink when the transmitter or receiver is active.
LED_SPEED	LED_SPEED/FX_SD	S, O, PU	27	**SPEED LED:** The LED is ON when device is in 100 Mb/s and OFF when in 10 Mb/s. Functionality of this LED is independent of mode selected.
LED_ACT	LED_ACT	S, O, PU	26	**ACTIVITY LED:** In Mode 1, this pin is the Activity LED which is ON when activity is present on either Transmit or Receive. **COLLISION/DUPLEX LED:** In Mode 2, this pin by default indicates Collision detection. In Mode 3, this LED output indicates Full-Duplex status.

3.7 IEEE 1588 Event/Trigger/Clock Interface

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
GPIO1 GPIO2 GPIO3 GPIO4	GPIO1 GPIO2 GPIO3 GPIO4	I/O, PD	21 22 23 25	**General Purpose I/O:** These pins may be used to signal or detect events.
GPIO5 GPIO6 GPIO7	LED_ACT LED_SPEED/FX_SD LED_LINK	I/O, PU	26 27 28	**General Purpose I/O:** These pins may be used to signal or detect events. Care should be taken when designing systems that use LEDs but use these pins as GPIOs. To disable the LED functions, refer to *Section 5.6.1.2.5*.
GPIO8 GPIO9	GPIO8 GPIO9	I/O, PD	36 37	**General Purpose I/O:** These pins may be used to signal or detect events.
GPIO10 GPIO11	TDO TDI	I/O, PU	9 12	**General Purpose I/O:** These pins may be used to signal or detect events. Care should be taken when designing systems that use the JTAG interface but use these pins as GPIOs.
GPIO12	CLK_OUT	I/O, PD	24	**General Purpose I/O:** This pin may be used to signal or detect events or may output a programmable clock signal synchronized to the internal IEEE 1588 clock or may be used as an input for an externally generated IEEE 1588 reference clock. If the system does not require the CLK_OUT signal, the CLK_OUT output should be disabled through the CLK_OUT_EN strap.

3.8 JTAG Interface

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
TCK	TCK	I, PU	8	**TEST CLOCK** This pin has a weak internal pullup.
TDO	TDO	O	9	**TEST OUTPUT**
TMS	TMS	I, PU	10	**TEST MODE SELECT** This pin has a weak internal pullup.
TRST#	TRST#	I, PU	11	**TEST RESET:** Active low test reset. This pin has a weak internal pullup.
TDI	TDI	I, PU	12	**TEST DATA INPUT** This pin has a weak internal pullup.

3.9 Reset and Power Down

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
RESET_N	RESET_N	I, PU	29	**RESET:** Active Low input that initializes or re-initializes the DP83640. Asserting this pin low for at least 1 µs will force a reset process to occur. All internal registers will re-initialize to their default states as specified for each bit in the Register Block section. All strap options are re-initialized as well.
PWRDOWN/INTN	PWRDOWN/INTN	I, PU	7	The default function of this pin is POWER DOWN. **POWER DOWN:** Asserting this signal low enables the DP83640 Power Down mode of operation. In this mode, the DP83640 will power down and consume minimum power. Register access will be available through the Management Interface to configure and power up the device. **INTERRUPT:** This pin may be programmed as an interrupt output instead of a Powerdown input. In this mode, Interrupts will be asserted low using this pin. Register access is required for the pin to be used as an interrupt mechanism. See *Section 5.3.6.2* for more details on the interrupt mechanisms.

3.10 Strap Options

The DP83640 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below. The functional pin name is indicated in parentheses.

A 2.2-kΩ resistor should be used for pulldown or pullup to change the default strap option. If the default option is required, then there is no need for external pullup or pulldown resistors. Because these pins may have alternate functions after reset is deasserted, they should not be connected directly to V_{CC} or GND.

<table>
<tr><th>SIGNAL NAME</th><th>PIN NAME</th><th>TYPE</th><th>PIN #</th><th>DESCRIPTION</th></tr>
<tr><td>PHYAD0
PHYAD1
PHYAD2
PHYAD3
PHYAD4</td><td>COL
RXD_3
RXD_2
RXD_1
RXD_0</td><td>S, O, PU
S, O, PD
S, O, PD
S, O, PD
S, O, PD</td><td>42
43
44
45
46</td><td>PHY ADDRESS [4:0]: The DP83640 provides five PHY address pins, the state of which are latched into the PHYCTRL register at system Hardware-Reset.
The DP83640 supports PHY Address strapping values 0 (<00000>) through 31 (<11111>).A PHY Address of 0 puts the part into the MII Isolate Mode. The MII isolate mode must be selected by strapping PHY Address 0; changing to Address 0 by register write will not put the PHY in the MII isolate mode.
PHYAD[0] pin has weak internal pullup resistor.
PHYAD[4:1] pins have weak internal pulldown resistors.</td></tr>
<tr><td>AN_EN
AN1

AN0</td><td>LED_LINK
LED_SPEED/FX_SD

LED_ACT</td><td>S, O, PU
S, O, PU

S, O, PU</td><td>28
27

26</td><td>AUTO-NEGOTIATION ENABLE: When high, this enables Auto-Negotiation with the capability set by AN0 and AN1 pins. When low, this puts the part into Forced Mode with the capability set by AN0 and AN1 pins.
AN0 / AN1: These input pins control the forced or advertised operating mode of the DP83640 according to the following table. The value on these pins is set by connecting the input pins to GND (0) or V_{CC} (1) through 2.2-kΩ resistors. These pins should NEVER be connected directly to GND or V_{CC}.
The value set at this input is latched into the DP83640 at Hardware-Reset.
The float/pulldown status of these pins are latched into the Basic Mode Control Register and the Auto_Negotiation Advertisement Register during Hardware-Reset.
The default is 111 because these pins have internal pullups.
FIBER MODE DUPLEX SELECTION: If Fiber mode is strapped using the FX_EN_Z pin (FX_EN_Z = 0), the AN0 strap value is used to select half or full duplex. AN_EN and AN1 are ignored in Fiber mode because it is 100 Mb only and does not support Auto-Negotiation. In Fiber mode, AN1 should not be connected to any system components except the fiber transceiver.
<table>
<tr><th>FX_EN_Z</th><th>AN_EN</th><th>AN1</th><th>AN0</th><th>Forced Mode</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10BASE-T, Half-Duplex</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>10BASE-T, Full-Duplex</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>100BASE-TX, Half-Duplex</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>100BASE-TX, Full-Duplex</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>0</td><td>100BASE-FX, Half-Duplex</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>1</td><td>100BASE-FX, Full-Duplex</td></tr>
<tr><th>FX_EN_Z</th><th>AN_EN</th><th>AN1</th><th>AN0</th><th>Advertised Mode</th></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>10BASE-T, Half/Full-Duplex</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>100BASE-TX, Half/Full-Duplex</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>100BASE-TX, Full-Duplex</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>10BASE-T, Half/Full-Duplex,
100BASE-TX, Half/Full-Duplex</td></tr>
</table></td></tr>
<tr><td>CLK_OUT_EN</td><td>GPIO1</td><td>S, I, PD</td><td>21</td><td>CLK_OUT OUTPUT ENABLE: When high, enables clock output on the CLK_OUT pin at power-up.</td></tr>
</table>

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
FX_EN_Z	RX_ER	S, O, PU	41	**FX ENABLE:** This strapping option enables 100Base-FX (Fiber) mode. This mode is disabled by default. An external pulldown will enable 100Base-FX mode.
LED_CFG	CRS/CRS_DV	S, O, PU	40	**LED CONFIGURATION:** This strapping option determines the mode of operation of the LED pins. Default is Mode 1. Mode 1 and Mode 2 can be controlled through the strap option. All modes are configurable through register access. See Table 5-2 for LED Mode Selection.
MII_MODE	RX_DV	S, O, PD	39	**MII MODE SELECT:** This strapping option determines the operating mode of the MAC Data Interface. Default operation is MII Mode with a value of 0 due to the internal pulldown. Strapping MII_MODE high will cause the device to be in RMII mode of operation.
				MII_MODE / **MAC Interface Mode** 0 / MII Mode 1 / RMII Mode
PCF_EN	GPIO2	S, I, PD	22	**PHY CONTROL FRAME ENABLE:** When high, allows the DP83640 to respond to PHY Control Frames.
RMII_MAS	TXD_3	S, I, PD	6	**RMII MASTER ENABLE:** When MII_MODE is strapped high, this strapping option enables RMII Master mode, in which the DP83640 uses a 25-MHz crystal connection on X1/X2 and generates the 50-MHz RMII reference clock. If strapped low when MII_MODE is strapped high, default RMII operation (RMII Slave) is enabled, in which the DP83640 uses a 50 MHz oscillator input on X1 as the RMII reference clock. This strap option is ignored if the MII_MODE strap is low.

3.11 10 Mb/s and 100 Mb/s PMD Interface

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
TD- TD+	TD- TD+	I/O	16 17	Differential common driver transmit output (PMD Output Pair). These differential outputs are automatically configured to either 10BASE-T or 100BASE-TX signaling. In Auto-MDIX mode of operation, this pair can be used as the Receive Input pair. In 100BASE-FX mode, this pair becomes the 100BASE-FX Transmit pair. These pins require 3.3-V bias for operation.
RD- RD+	RD- RD+	I/O	13 14	Differential receive input (PMD Input Pair). These differential inputs are automatically configured to accept either 100BASE-TX or 10BASE-T signaling. In Auto-MDIX mode of operation, this pair can be used as the Transmit Output pair. In 100BASE-FX mode, this pair becomes the 100BASE-FX Receive pair. These pins require 3.3-V bias for operation.
FX_SD	LED_SPEED/FX_SD	S, I/O, PU	27	**FIBER MODE SIGNAL DETECT:** This pin provides the Signal Detect input for 100BASE-FX mode.

3.12 Power Supply Pins

SIGNAL NAME	PIN NAME	TYPE	PIN #	DESCRIPTION
ANAVSS	ANAVSS	Ground	18	Analog Ground
ANA33VDD	ANA33VDD	Supply	19	Analog VDD Supply
CD_VSS	CD_VSS	Ground	15	Analog Ground
IO_CORE_VSS	IO_CORE_VSS	Ground	35	Digital Ground
IO_VDD	IO_VDD	Supply	32 48	I/O VDD Supply
IO_VSS	IO_VSS	Ground	47	Digital Ground
VREF	VREF		20	Bias Resistor Connection. A 4.87-kΩ 1% resistor should be connected from VREF to GND.

4 Specifications

4.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V_{CC})	–0.5	4.2	V
DC Input Voltage (V_{IN})		–0.5 to V_{CC} + 0.5	V
DC Output Voltage (V_{OUT})		–0.5 to V_{CC} + 0.5	V
Maximum Case Temperature for T_A = 85 °C		95	°C
Maximum Die Temperature (T_J)		150	°C
Lead Temperature (T_L) (Soldering, 10 s)		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	

(1) R_{ZAP} = 1.5k, C_{ZAP} = 120 pF
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Analog Supply Voltage (V_{CC})		3.3 ± 0.3	V
I/O Supply Voltage ($V_{I/O}$)		3.3 ± 10% or 2.5 ± 5%	V
Industrial Temperature (T_I)	–40	85	°C
Power Dissipation (P_D) with $V_{I/O}$ = 3.3 V		290	mW
Power Dissipation (P_D) with $V_{I/O}$ = 2.5 V		260	mW

4.4 Thermal Information

THERMAL METRIC(1)		PT 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.3(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) No Airflow @ 1 W.

4.5 DC Specifications

	PIN TYPES	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	I I/O	Input High Voltage		2.0			V
V_{IL}	I I/O	Input Low Voltage	$V_{I/O}$ = 3.3 V			0.8	V
			$V_{I/O}$ = 2.5 V			0.7	V
I_{IH}	I I/O	Input High Current	V_{IN} = $V_{I/O}$			10	µA
I_{IL}	I I/O	Input Low Current	V_{IN} = GND			10	µA
V_{OL}	O I/O	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	O I/O	Output High Voltage	I_{OH} = -4 mA	$V_{I/O}$ - 0.5			V
I_{OZ}	O I/O	TRI-STATE Output Leakage Current	V_{OUT} = $V_{I/O}$ or GND	–10		10	µA
V_{TPTD_100}	PMD Output Pair	100M Transmit Voltage		0.95	1	1.05	V
$V_{TPTDsym}$	PMD Output Pair	100M Transmit Voltage Symmetry				±2%	
V_{TPTD_10}	PMD Output Pair	10M Transmit Voltage		2.2	2.5	2.8	V
V_{FXTD_100}	PMD Output Pair	FX 100M Transmit Voltage		0.3	0.5	0.93	V
C_{IN1}	I	CMOS Input Capacitance			8		pF
C_{OUT1}	O	CMOS Output Capacitance			8		pF
S_{DTHon}	PMD Input Pair	100BASE-TX Signal detect turnon threshold				1000	mV diff pk-pk
S_{DTHoff}	PMD Input Pair	Signal detect turnoff threshold		200			mV diff pk-pk
V_{TH}	PMD Input Pair	10BASE-T Receive Threshold		300		585	mV
I_{dd100}	Supply	100BASE-TX (Full Duplex)	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V, I_{OUT} = 0 mA(1)		88		mA
			V_{CC} = 3.3 V, $V_{I/O}$ = 2.5 V, I_{OUT} = 0 mA(1)		84		mA
I_{dd10}	Supply	10BASE-T (Full Duplex)	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V, I_{OUT} = 0 mA(1)		105		mA
			V_{CC} = 3.3 V, $V_{I/O}$ = 2.5 V, I_{OUT} = 0 mA(1)		103		mA
I_{dd}	Supply	Power Down Mode	CLK_OUT disabled		10		mA

(1) For I_{dd} measurements, outputs are not loaded

4.6 AC Timing Requirements

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
POWER-UP TIMING (Refer to Figure 4-1)						
T2.1.1	Post Power Up Stabilization time prior to MDC preamble for register accesses(1)	MDIO is pulled high for 32-bit serial management initialization.	167			ms
T2.1.2	Hardware Configuration Latch-in Time from power up(1)	Hardware Configuration Pins are described in *Section 3*.	167			
T2.1.3	Hardware Configuration pins transition to output drivers			50		ns
RESET TIMING (Refer to Figure 4-2)						
T2.2.1	Post RESET Stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization		3		µs
T2.2.2	Hardware Configuration Latch-in Time from the Deassertion of RESET (either soft or hard)	Hardware Configuration Pins are described in *Section 3*		3		µs
T2.2.3	Hardware Configuration pins transition to output drivers(2)			50		ns
T2.2.4	RESET pulse width	X1 Clock must be stable for at min. of 1 µs during RESET pulse low time.	1			µs
MII SERIAL MANAGEMENT TIMING (Refer to Figure 4-3)						
T2.3.1	MDC to MDIO (Output) Delay Time		0		20	ns
T2.3.2	MDIO (Input) to MDC Setup Time		10			
T2.3.3	MDIO (Input) to MDC Hold Time		10			
T2.3.4	MDC Frequency			2.5	25	MHz
100 Mb/s MII TRANSMIT TIMING (Refer to Figure 4-4)						
T2.4.1	TX_CLK High/Low Time	100 Mb/s Normal mode	16	20	24	ns
T2.4.2	TXD[3:0], TX_EN Data Setup to TX_CLK		10			
T2.4.3	TXD[3:0], TX_EN Data Hold from TX_CLK		0			
100 Mb/s MII RECEIVE TIMING (Refer to Figure 4-5)						
T2.5.1	RX_CLK High/Low Time(3)	100 Mb/s Normal mode	16	20	24	ns
T2.5.2	RX_CLK to RXD[3:0], RX_DV, RX_ER Delay		10		30	
100BASE-TX AND 100BASE-FX MII TRANSMIT PACKET LATENCY TIMING (Refer to Figure 4-6)						
T2.6.1	TX_CLK to PMD Output Pair Latency(4)	100BASE-TX and 100BASE-FX modes IEEE 1588 One-Step Operation enabled(5)		5 9		bits
100BASE-TX AND 100BASE-FX MII TRANSMIT PACKET DEASSERTION TIMING (Refer to Figure 4-7)						
T2.7.1	TX_CLK to PMD Output Pair Deassertion(6)	100BASE-TX and 100BASE-FX modes		5		bits

(1) In RMII Slave Mode, the minimum Post Power up Stabilization and Hardware Configuration Latch-in times are 84 ms.
(2) It is important to choose pullup and/or pulldown resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver.
(3) RX_CLK may be held low or high for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.
(4) Enabling PHY Control Frames will add latency equal to 8 bits times the PCF_BUF_SIZE setting. For example if PCF_BUF_SIZE is set to 15, then the additional delay will be 15*8= 120 bits.
(5) For Normal mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the “J” code group as output from the PMD Output Pair. 1 bit time = 10 ns in 100 Mb/s mode.
(6) Deassertion is determined by measuring the time from the first rising edge of TX_CLK occurring after the deassertion of TX_EN to the first bit of the "T" code group as output from the PMD Output Pair. 1 bit time = 10 ns in 100 Mb/s mode.

AC Timing Requirements *(continued)*

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
100BASE-TX TRANSMIT TIMING ($t_{R/F}$ and Jitter) (Refer to Figure 4-8)						
T2.8.1	100 Mb/s PMD Output Pair t_R and t_F (7)		3	4	5	ns
	100 Mb/s t_R and t_F Mismatch (8)				500	ps
T2.8.2	100 Mb/s PMD Output Pair Transmit Jitter				1.4	ns
100BASE-TX AND 100BASE-FX MII RECEIVE PACKET LATENCY TIMING (Refer to Figure 4-9)						
T2.9.1	Carrier Sense ON Delay (9)	100BASE-TX mode		20		bits (10)
		100BASE-FX mode		10		
T2.9.2	Receive Data Latency (11) (12)	100BASE-TX mode		24		
		100BASE-FX mode		14		
100BASE-TX AND 100BASE-FX MII RECEIVE PACKET DEASSERTION TIMING (Refer to Figure 4-10)						
T2.10.1	Carrier Sense OFF Delay (13)	100BASE-TX mode		24		bits (14)
		100BASE-FX mode		14		
10 Mb/s MII TRANSMIT TIMING (15) (Refer to Figure 4-11)						
T2.11.1	TX_CLK High/Low Time	10 Mb/s MII mode	190	200	210	ns
T2.11.2	TXD[3:0], TX_EN Data Setup to TX_CLK falling edge	10 Mb/s MII mode	25			
T2.11.3	TXD[3:0], TX_EN Data Hold from TX_CLK rising edge	10 Mb/s MII mode	0			
10 Mb/s MII RECEIVE TIMING (Refer to Figure 4-12)						
T2.12.1	RX_CLK High/Low Time (16)		160	200	240	ns
T2.12.2	RXD[3:0], RX_DV transition delay from RX_CLK rising edge	10 Mb/s MII mode	100			
T2.12.3	RX_CLK rising edge delay from RXD[3:0], RX_DV valid data	10 Mb/s MII mode	100			
10BASE-T MII TRANSMIT TIMING (START OF PACKET) (Refer to Figure 4-13)						
T2.13.1	Transmit Output Delay from the Falling Edge of TX_CLK	10 Mb/s MII mode		3.5		bits (17)
10BASE-T MII TRANSMIT TIMING (END OF PACKET) (Refer to Figure 4-14)						
T2.14.1	End of Packet High Time (with '0' ending bit)		250	300		ns
T2.14.2	End of Packet High Time (with '1' ending bit)		250	300		ns
10BASE-T MII RECEIVE TIMING (START OF PACKET) (Refer to Figure 4-15)						
T2.15.1	Carrier Sense Turnon Delay (PMD Input Pair to CRS)			630	1000	ns

(7) Rise and fall times taken at 10% and 90% of the +1 or –1 amplitude.
(8) Normal Mismatch is the difference between the maximum and minimum of all rise and fall times.
(9) Carrier Sense On Delay is determined by measuring the time from the first bit of the “J” code group to the assertion of Carrier Sense.
(10) 1 bit time = 10 ns in 100 Mb/s mode.
(11) Enabling IEEE 1588 Receive Timestamp insertion will increase the Receive Data Latency by 40 bit times.
(12) Enabling PHY Status Frames will introduce variability in Receive Data Latency due to insertion of PHY Status Frames into the receive datapath.
(13) Carrier Sense Off Delay is determined by measuring the time from the first bit of the “T” code group to the deassertion of Carrier Sense.
(14) 1 bit time = 10 ns in 100 Mb/s mode.
(15) An attached Mac should drive the transmit signals using the positive edge of TX_CLK. As shown above, the MII signals are sampled on the falling edge of TX_CLK.
(16) RX_CLK may be held low for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.
(17) 1 bit time = 100 ns in 10 Mb/s mode.

AC Timing Requirements *(continued)*

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
T2.15.2	RX_DV Latency(18)			10		bits(19)
T2.15.3	Receive Data Latency	Measurement shown from SFD		8		
10BASE-T MII RECEIVE TIMING (END OF PACKET) (Refer to Figure 4-16)						
T2.16.1	Carrier Sense Turnoff Delay				1.0	µs
10 Mb/s HEARTBEAT TIMING (Refer to Figure 4-17)						
T2.17.1	CD Heartbeat Delay	All 10 Mb/s modes		1200		ns
T2.17.2	CD Heartbeat Duration	All 10 Mb/s modes		1000		
10 Mb/s JABBER TIMING (Refer to Figure 4-18)						
T2.18.1	Jabber Activation Time			85		ms
T2.18.2	Jabber Deactivation Time			500		
10BASE-T NORMAL LINK PULSE TIMING(20) (Refer to Figure 4-19)						
T2.19.1	Pulse Width			100		ns
T2.19.2	Pulse Period			16		ms
AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING(21) (Refer to Figure 4-20)						
T2.20.1	Clock, Data Pulse Width			100		ns
T2.20.2	Clock Pulse to Clock Pulse Period			125		µs
T2.20.3	Clock Pulse to Data Pulse Period	Data = 1		62		
T2.20.4	Burst Width			2		ms
T2.20.5	FLP Burst to FLP Burst Period			16		
100BASE-TX SIGNAL DETECT TIMING(22) (Refer to Figure 4-21)						
T2.21.1	SD Internal Turnon Time				1	ms
T2.21.2	SD Internal Turnoff Time	Default operation Fast link-loss indication enabled(23)		250 1.3	300	µs µs
100 Mb/s INTERNAL LOOPBACK TIMING (Refer to Figure 4-22)						
T2.22.1	TX_EN to RX_DV Loopback(24)	100 Mb/s internal loopback mode(25)			240	ns
10 Mb/s INTERNAL LOOPBACK TIMING (Refer to Figure 4-23)						
T2.23.1	TX_EN to RX_DV Loopback	10 Mb/s internal loopback mode(26)			2	µs
RMII TRANSMIT TIMING (SLAVE MODE) (Refer to Figure 4-24)						
T2.24.1	X1 Clock Period	50-MHz Reference Clock		20		ns
T2.24.2	TXD[1:0], TX_EN, Data Setup to X1 rising edge		4			
T2.24.3	TXD[1:0], TX_EN, Data Hold from X1 rising edge		2			
T2.24.4	X1 Clock to PMD Output Pair Latency (100 Mb)(27)	100BASE-TX or 100BASE-FX		11		bits

(18) 10BASE-T RX_DV Latency is measured from first bit of preamble on the wire to the assertion of RX_DV.
(19) 1 bit time = 100 ns in 10 Mb/s mode.
(20) These specifications represent transmit timings.
(21) These specifications represent transmit timings.
(22) The signal amplitude on PMD Input Pair must be TP-PMD compliant.
(23) Fast Link-loss detect is enabled by setting the SD_CNFG[8] register bit to a 1.
(24) Due to the nature of the descrambler function, all 100BASE-TX Loopback modes will cause an initial “dead-time” of up to 550 µs during which time no data will be present at the receive MII outputs. The 100BASE-TX timing specified is based on device delays after the initial 550 µs “dead-time”.
(25) Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.
(26) Measurement is made from the first falling edge of TX_CLK after assertion of TX_EN.
(27) Latency measurement is made from the X1 rising edge to the first bit of symbol.

AC Timing Requirements *(continued)*

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
RMII TRANSMIT TIMING (MASTER MODE) (Refer to Figure 4-25)						
T2.25.1	RX_CLK, TX_CLK, CLK_OUT Period	50-MHz Reference Clock		20		ns
T2.25.2	TXD[1:0], TX_EN Data Setup to RX_CLK, TX_CLK, CLK_OUT rising edge		4			
T2.25.3	TXD[1:0], TX_EN Data Hold from RX_CLK, TX_CLK, CLK_OUT rising edge		2			
T2.25.4	RX_CLK, TX_CLK, CLK_OUT to PMD Output Pair Latency(28)	From RX_CLK rising edge to first bit of symbol		11		bits
RMII RECEIVE TIMING (SLAVE MODE)(29) (Refer to Figure 4-26)						
T2.26.1	X1 Clock Period	50-MHz Reference Clock		20		ns
T2.26.2	RXD[1:0], CRS_DV, and RX_ER output delay from X1 rising edge(30)		2		14	
T2.26.3	CRS ON delay(31)	100BASE-TX mode		18.5		bits
		100BASE-FX mode		9		
T2.26.4	CRS OFF delay (32)	100BASE-TX mode		27		
		100BASE-FX mode		17		
T2.26.5	RXD[1:0] and RX_ER latency(33)(34)(35)	100BASE-TX mode		38		
		100BASE-FX mode		27		
RMII RECEIVE TIMING (MASTER MODE)(36) (Refer to Figure 4-27)						
T2.27.1	RX_CLK, TX_CLK, CLK_OUT Clock Period	50-MHz Reference Clock		20		ns
T2.27.2	RXD[1:0], CRS_DV, RX_DV and RX_ER output delay from RX_CLK, TX_CLK, CLK_OUT rising edge(37)		2		14	
T2.27.3	CRS ON delay(38)	100BASE-TX mode		18.5		bits
		100BASE-FX mode		9		
T2.27.4	CRS OFF delay (39)	100BASE-TX mode		27		
		100BASE-FX mode		17		
T2.27.5	RXD[1:0] and RX_ER latency (40)	100BASE-TX mode		38		
		100BASE-FX mode		27		
RX_CLK TIMING (RMII MASTER MODE) (Refer to Figure 4-28)						
T2.28.1	RX_CLK High Time(41)			12		ns
T2.28.2	RX_CLK Low Time(41)			8		
T2.28.3	RX_CLK Period			20		

(28) Latency measurement is made from the RX_CLK rising edge to the first bit of symbol.
(29) Per the RMII Specification, output delays assume a 25-pF load.
(30) CRS_DV is asserted asynchronously in order to minimize latency of control signals through the PHY. CRS_DV may toggle synchronously at the end of the packet to indicate CRS deassertion.
(31) CRS ON delay is measured from the first bit of the JK symbol on the PMD Input Pair to initial assertion of CRS_DV.
(32) CRS OFF delay is measured from the first bit of the TR symbol on the PMD Input Pair to initial deassertion of CRS_DV.
(33) Receive Latency is measured from the first bit of the symbol pair on the PMD Input Pair. Typical values are with the Elasticity Buffer set to the default value (01).
(34) Enabling IEEE 1588 Receive Timestamp insertion will increase the Receive Data Latency by 40 bit times.
(35) Enabling PHY Status Frames will introduce variability in Receive Data Latency due to insertion of PHY Status Frames into the receive datapath.
(36) Per the RMII Specification, output delays assume a 25-pF load.
(37) CRS_DV is asserted asynchronously in order to minimize latency of control signals through the PHY. CRS_DV may toggle synchronously at the end of the packet to indicate CRS deassertion.
(38) CRS ON delay is measured from the first bit of the JK symbol on the PMD Input Pair to initial assertion of CRS_DV.
(39) CRS OFF delay is measured from the first bit of the TR symbol on the PMD Input Pair to initial deassertion of CRS_DV.
(40) Receive Latency is measured from the first bit of the symbol pair on the PMD Input Pair. Typical values are with the Elasticity Buffer set to the default value (01).
(41) The High Time and Low Tme will add up to 20 ns.

AC Timing Requirements *(continued)*

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
CLK_OUT TIMING (RMII SLAVE MODE) (Refer to Figure 4-29)						
T2.29.1	CLK_OUT High/Low Time			10		ns
T2.29.2	CLK_OUT propagation delay	Relative to X1			8	
SINGLE CLOCK MII (SCMII) TRANSMIT TIMING (Refer to Figure 4-30)						
T2.30.1	X1 Clock Period	25-MHz Reference Clock		40		ns
T2.30.2	TXD[3:0], TX_EN Data Setup	To X1 rising edge	4			
T2.30.3	TXD[3:0], TX_EN Data Hold	From X1 rising edge	2			
T2.30.4	X1 Clock to PMD Output Pair Latency (100 Mb)(42)	100BASE-TX or 100BASE-FX		13		bits
SINGLE CLOCK MII (SCMII) RECEIVE TIMING (Refer to Figure 4-31)						
T2.31.1	X1 Clock Period	25-MHz Reference Clock(43)		40		ns
T2.31.2	RXD[3:0], RX_DV and RX_ER output delay(44)	From X1 rising edge	2		18	
T2.31.3	CRS ON delay (45)	100BASE-TX mode		19		bits
		100BASE-FX mode		9		
T2.31.4	CRS OFF delay (46)	100BASE-TX mode		26		
		100BASE-FX mode		16		
T2.31.5	RXD[3:0] and RX_ER latency(47)	100BASE-TX mode		56		
		100BASE-FX mode		46		
100 Mb/s X1 TO TX_CLK TIMING (Refer to Figure 4-32)						
T2.32.1	X1 to TX_CLK delay(48)	100 Mb/s Normal mode	0		5	ns

(42) Latency measurement is made from the X1 rising edge to the first bit of symbol.
(43) CRS is asserted and deasserted asynchronously relative to the reference clock.
(44) Output delays assume a 25-pF load.
(45) CRS ON delay is measured from the first bit of the JK symbol on the PMD Input Pair to assertion of CRS_DV.
(46) CRS OFF delay is measured from the first bit of the TR symbol on the PMD Input Pair to deassertion of CRS_DV.
(47) Receive Latency is measured from the first bit of the symbol pair on the PMD Input Pair. Typical values are with the Elasticity Buffer set to the default value (01).
(48) X1 to TX_CLK timing is provided to support devices that use X1 instead of TX_CLK as the reference for transmit MII data.

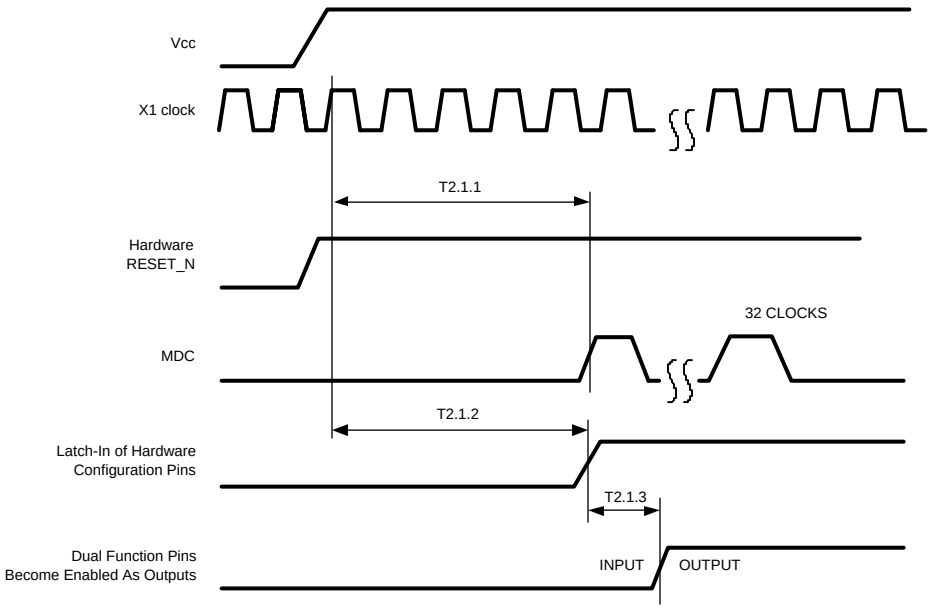


Figure 4-1. Power Up Timing

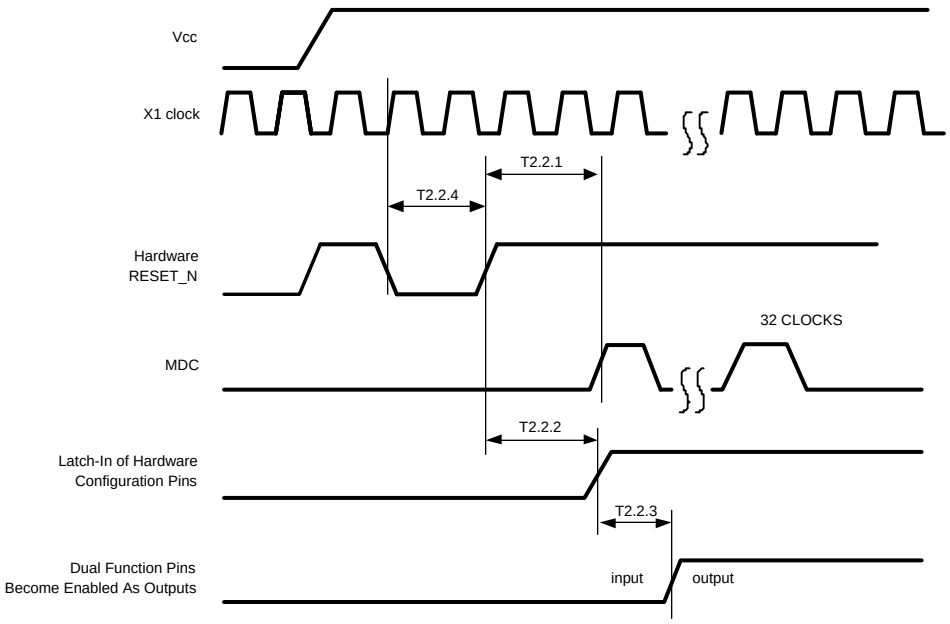


Figure 4-2. Reset Timing

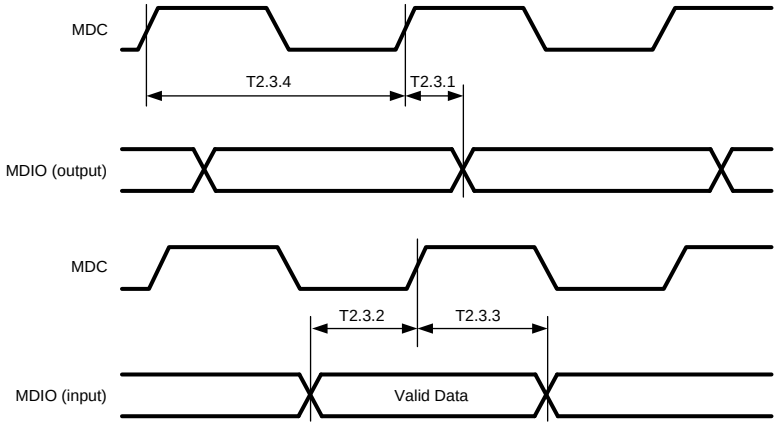


Figure 4-3. MII Serial Management Timing

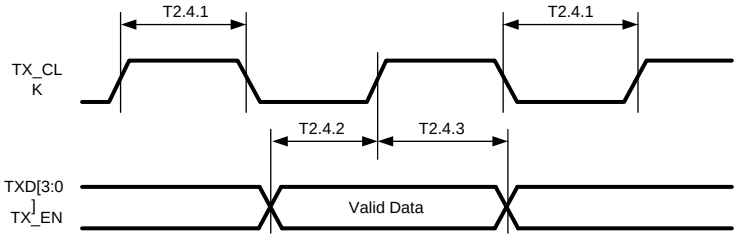


Figure 4-4. 100 Mb/s MII Transmit Timing

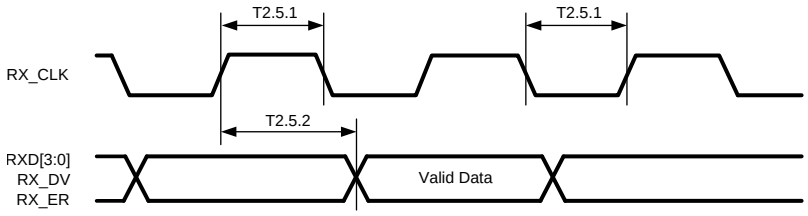


Figure 4-5. 100 Mb/s MII Receive Timing

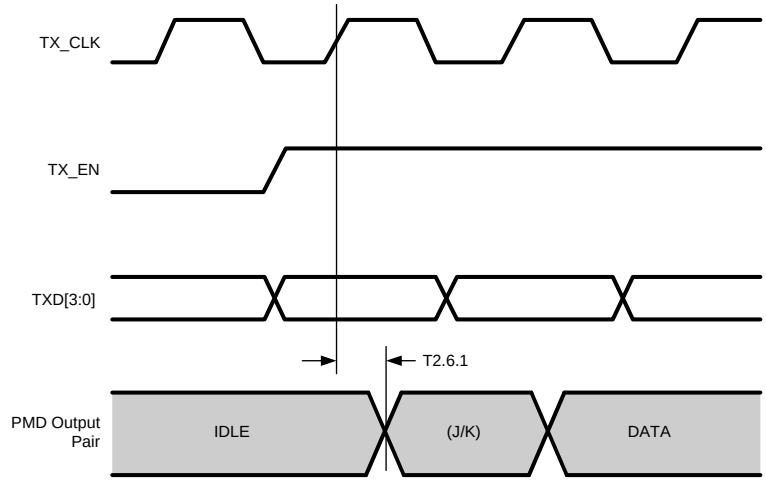


Figure 4-6. 100BASE-TX and 100BASE-FX MII Transmit Packet Latency Timing

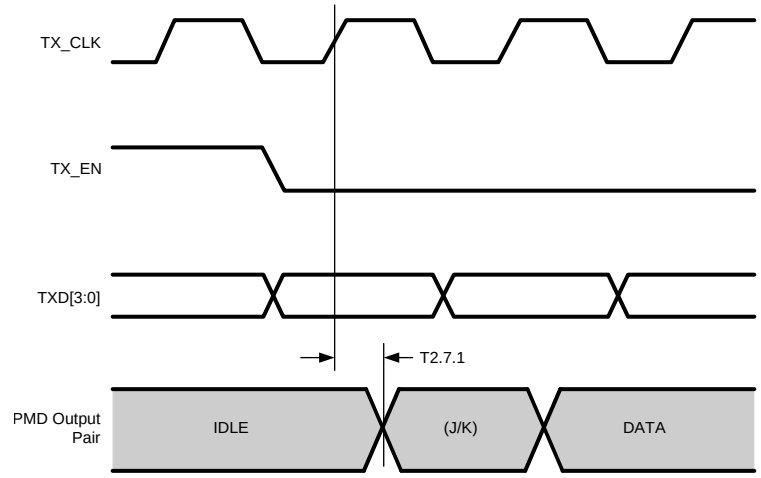


Figure 4-7. 100BASE-TX and 100BASE-FX MII Transmit Packet Deassertion Timing

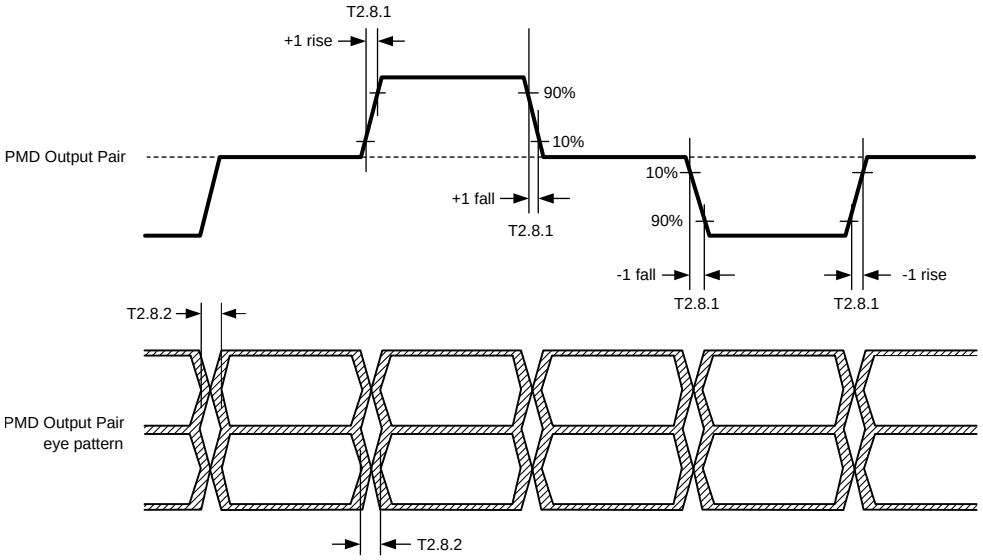


Figure 4-8. 100BASE-TX Transmit Timing ($t_{R/F}$ and Jitter)

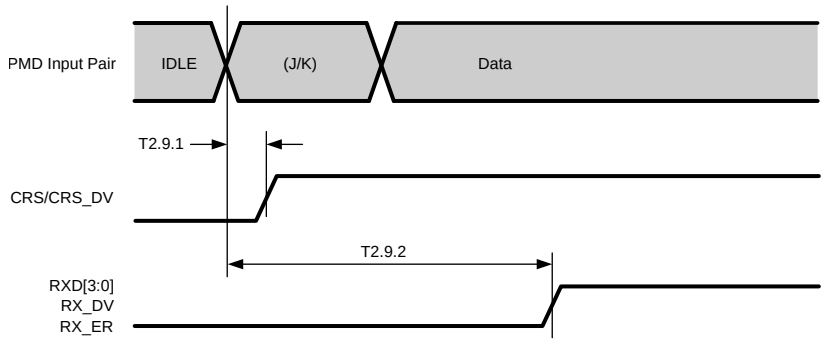


Figure 4-9. 100BASE-TX and 100BASE-FX MII Receive Packet Latency Timing

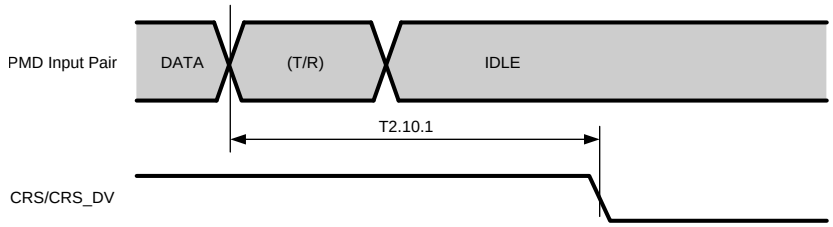


Figure 4-10. 100BASE-TX and 100BASE-FX MII Receive Packet Deassertion Timing

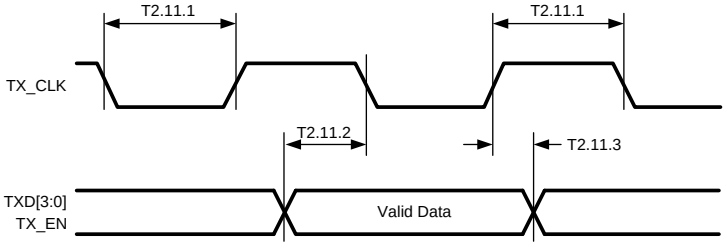


Figure 4-11. 10 Mb/s MII Transmit Timing

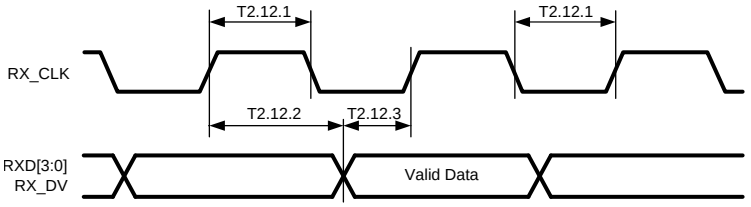


Figure 4-12. 10 Mb/s MII Receive Timing

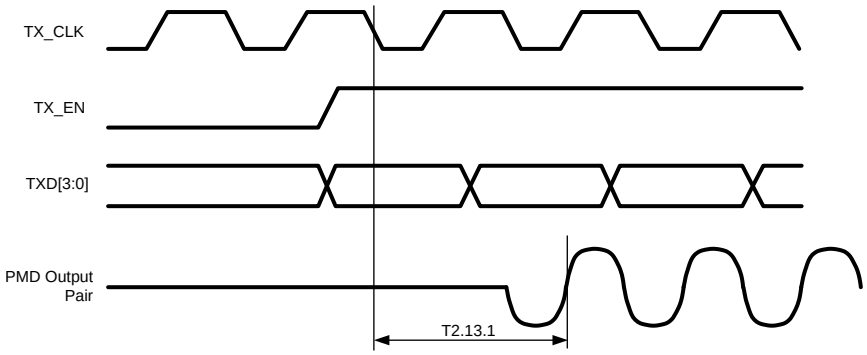


Figure 4-13. 10BASE-T MII Transmit Timing (Start of Packet)

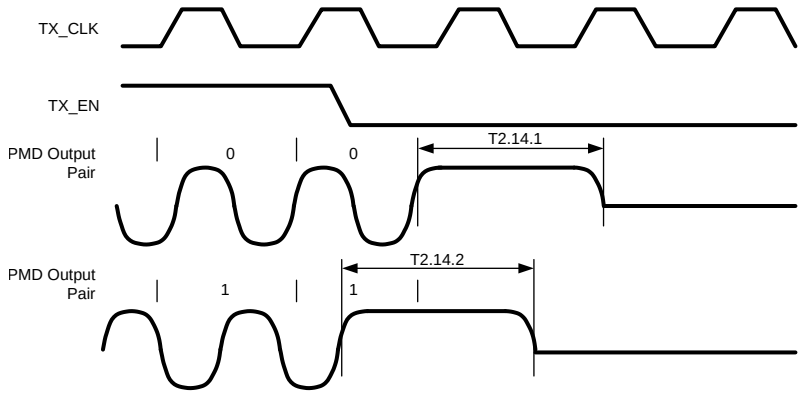


Figure 4-14. 10BASE-T MII Transmit Timing (End of Packet)

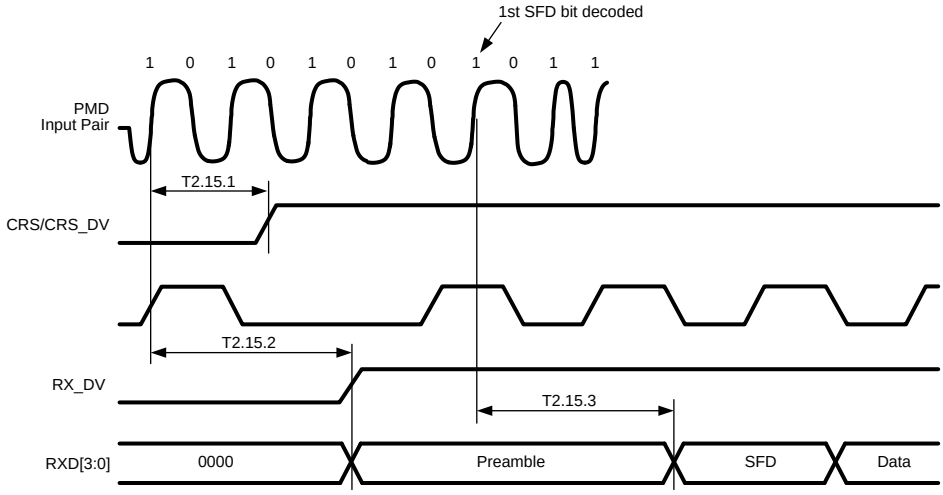


Figure 4-15. 10BASE-T MII Receive Timing (Start of Packet)

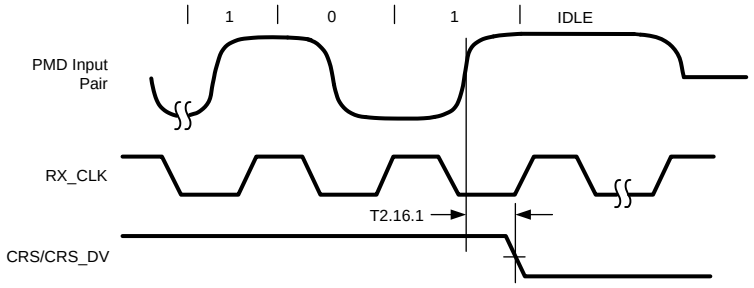


Figure 4-16. 10BASE-T MII Receive Timing (End of Packet)

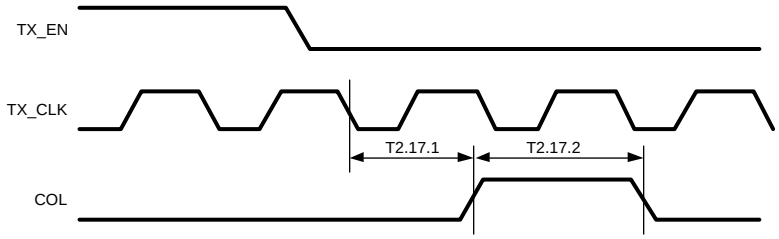


Figure 4-17. 10 Mb/s Heartbeat Timing

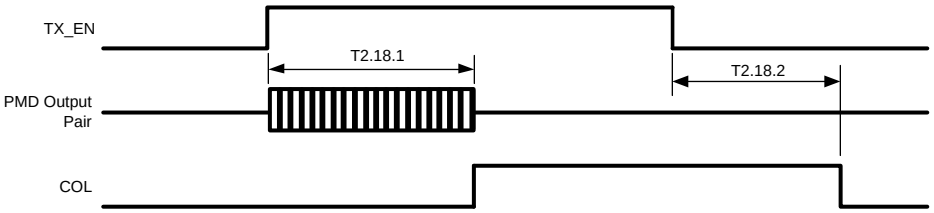


Figure 4-18. 10 Mb/s Jabber Timing

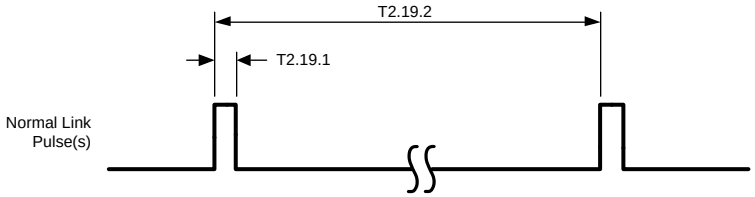


Figure 4-19. 10BASE-T Normal Link Pulse Timing

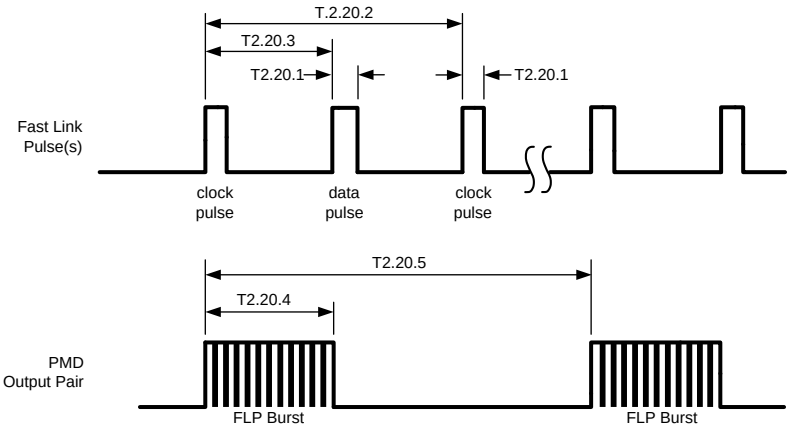


Figure 4-20. Auto-Negotiation Fast Link Pulse (FLP) Timing

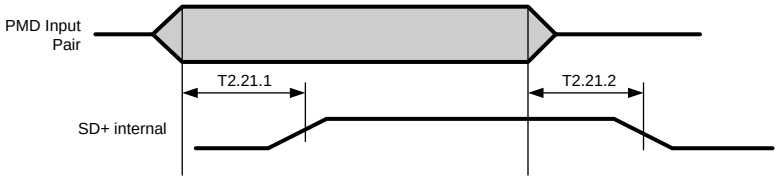


Figure 4-21. 100BASE-TX Signal Detect Timing

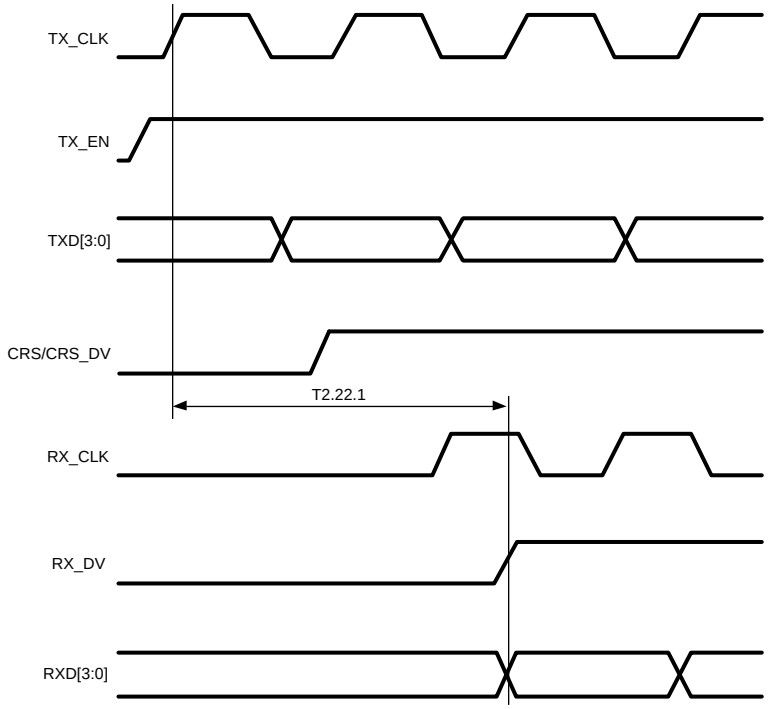


Figure 4-22. 100 Mb/s Internal Loopback Timing

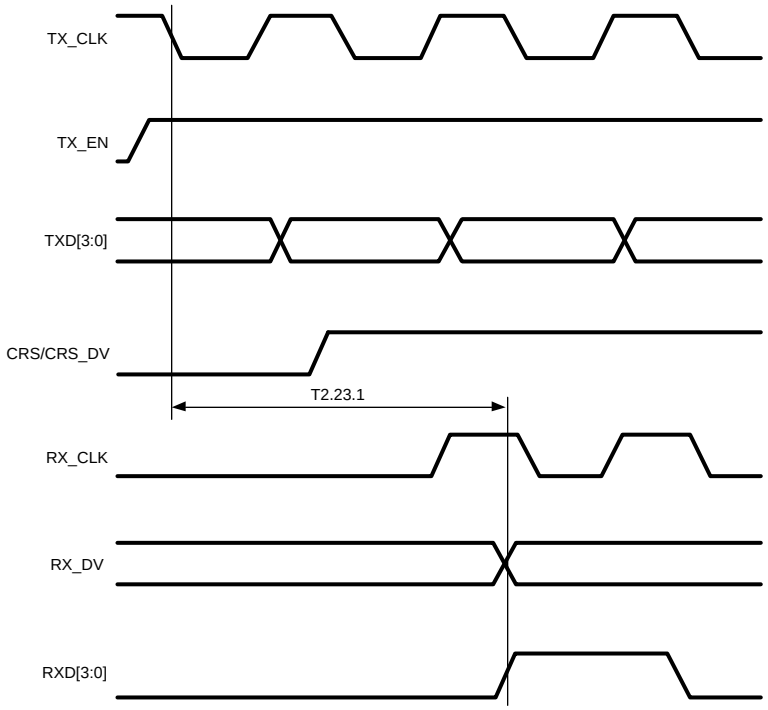


Figure 4-23. 10 Mb/s Internal Loopback Timing

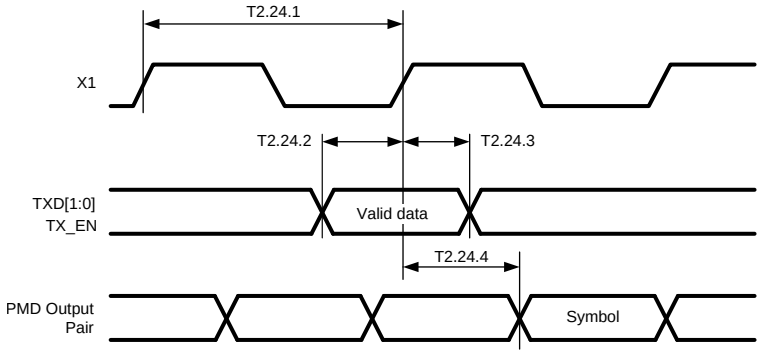


Figure 4-24. RMII Transmit Timing (Slave Mode)

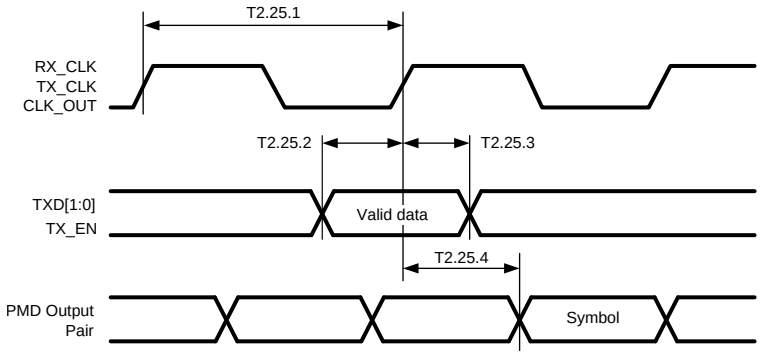


Figure 4-25. RMII Transmit Timing (Master Mode)

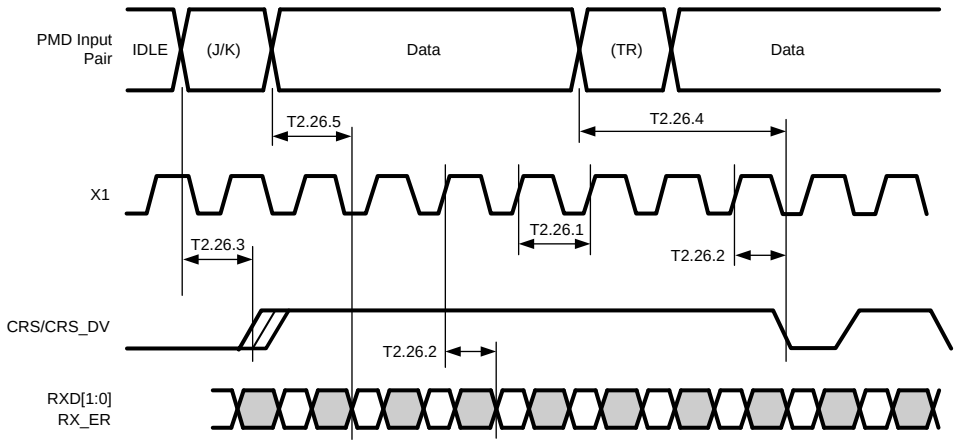


Figure 4-26. RMII Receive Timing (Slave Mode)

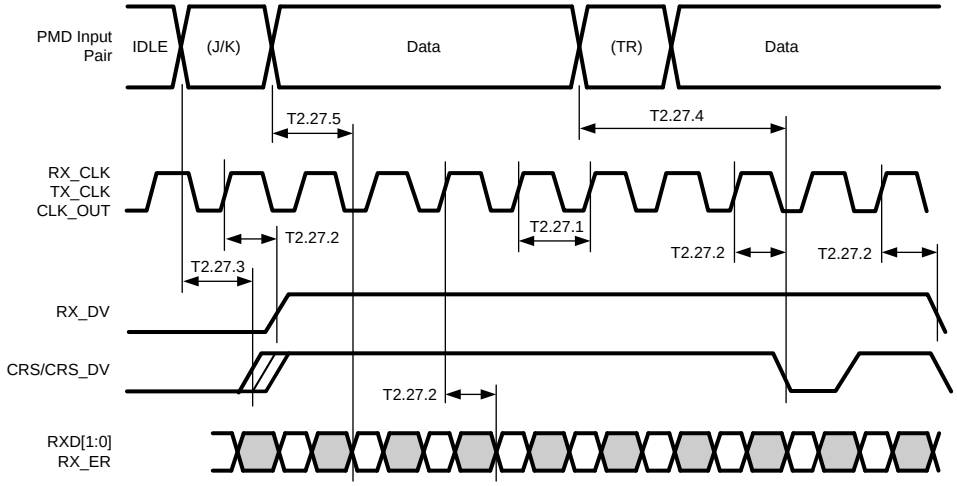


Figure 4-27. RMII Receive Timing (Master Mode)

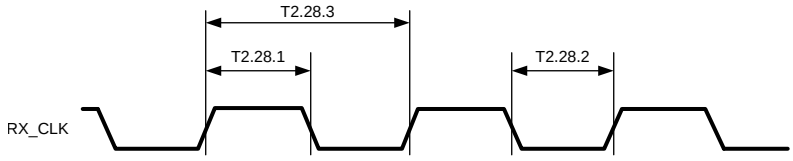


Figure 4-28. RX_CLK Timing (RMII Master Mode)

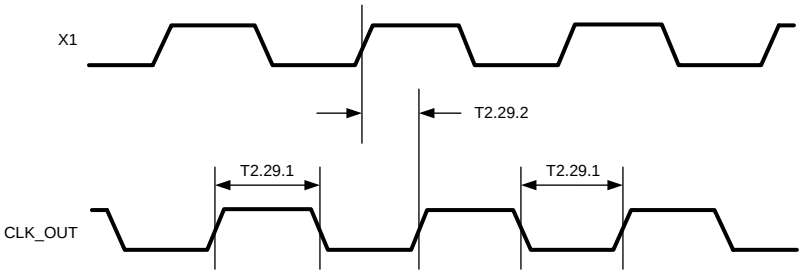


Figure 4-29. CLK_OUT Timing (RMII Slave Mode)

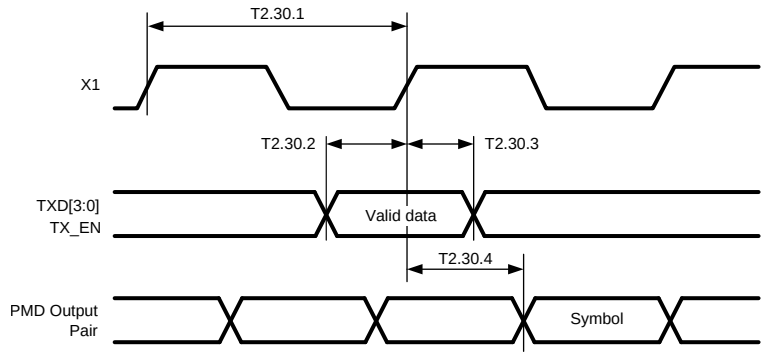


Figure 4-30. Single Clock MII (SCMII) Transmit Timing

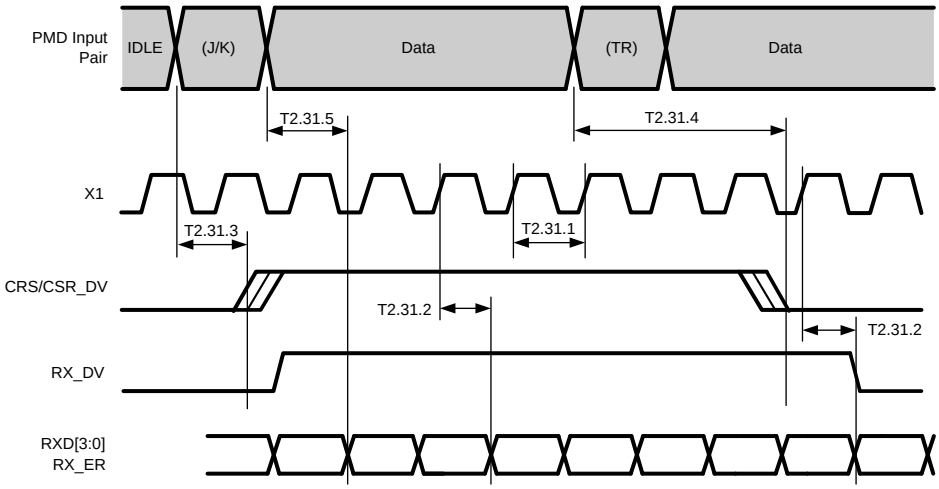


Figure 4-31. Single Clock MII (SCMII) Receive Timing

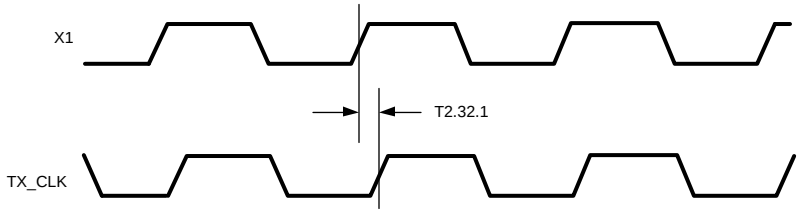


Figure 4-32. 100 Mb/s X1 to TX_CLK Timing

5 Detailed Description

5.1 Overview

The DP83640 supports many key parameters for industrial Ethernet including deterministic, low transmit and receive latency, high ESD and EMC tolerance, excellent cable reach, innovative cable diagnostics capabilities, and industrial temperature range. The MAC interface supports operation through MII or RMII and allows operation from a 25-MHz clock source in RMII Master mode. The transceiver interface supports operation over a twisted pair interface or a fiber interface. These characteristics comprise a robust, rugged, and reliable Ethernet PHY suitable for a broad range of applications.

5.2 Functional Block Diagram

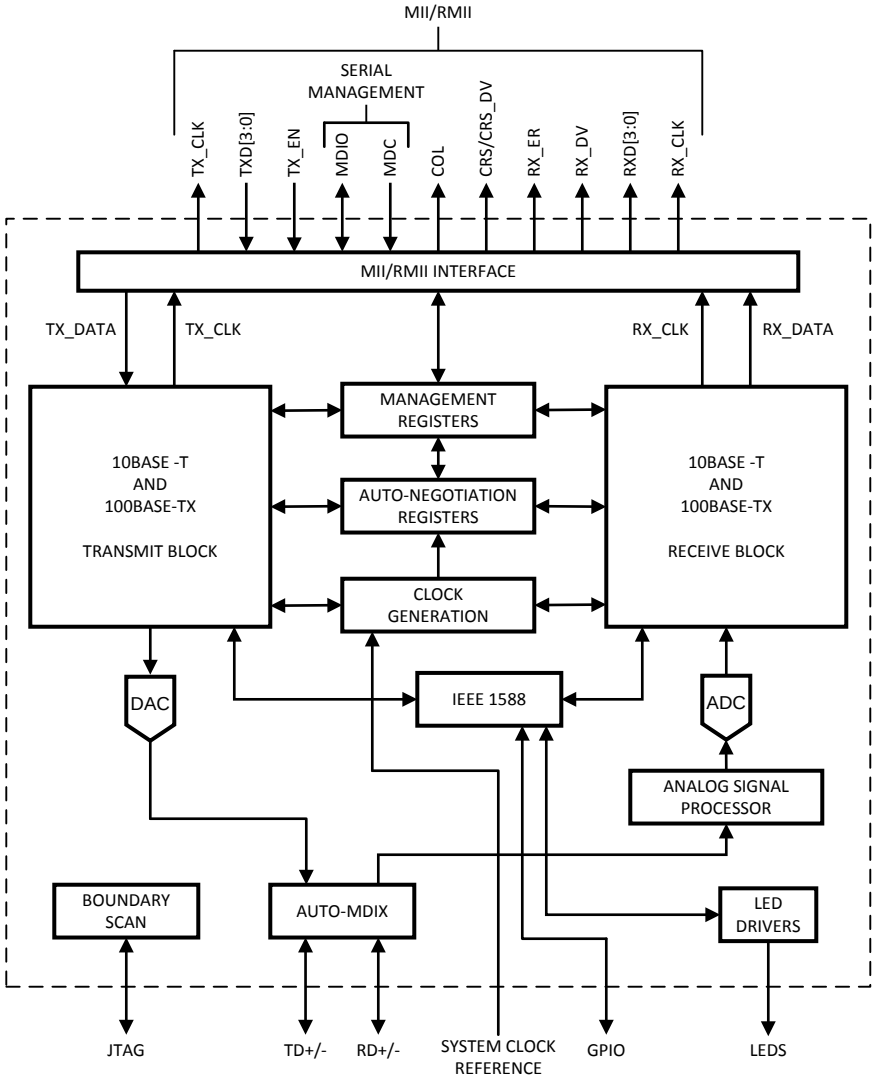


Figure 5-1. DP83640 Functional Block Diagram

5.3 Feature Description

5.3.1 Media Configuration

The DP83640 supports both Twisted Pair (100BASE-TX and 10BASE-T) and Fiber (100BASE-FX) media. The port may be configured for Twisted Pair (TP) or Fiber (FX) operation by strap option or by register access.

At power-up/reset, the state of the RX_ER pin will select the media for the port. The default selection is twisted pair mode, while an external pulldown will select FX mode of operation. Strapping the port into FX mode also automatically sets the Far-End Fault Enable, bit 3 of PCSR (16h), the Scramble Bypass, bit 1 of PCSR (16h) and the Descrambler Bypass, bit 0 of PCSR (16h). In addition, the media selection may be controlled by writing to bit 6, FX_EN, of PCSR (16h).

5.3.2 Auto-Negotiation

The Auto-Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate Auto-Negotiation abilities between two devices at each end of a link segment. For further detail regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification. The DP83640 supports four different Ethernet protocols (10 Mb/s Half Duplex, 10 Mb/s Full Duplex, 100 Mb/s Half Duplex, and 100 Mb/s Full Duplex), so the inclusion of Auto-Negotiation ensures that the highest performance protocol will be selected based on the advertised ability of the Link Partner. The Auto-Negotiation function within the DP83640 can be controlled either by internal register access or by the use of the AN_EN, AN1 and AN0 pins.

5.3.2.1 Auto-Negotiation Pin Control

The state of AN_EN, AN0 and AN1 determines whether the DP83640 is forced into a specific mode or Auto-Negotiation will advertise a specific ability (or set of abilities) as given in Table 5-1. These pins allow configuration options to be selected without requiring internal register access.

The state of AN_EN, AN0 and AN1, upon power-up/reset, determines the state of bits [8:5] of the ANAR register.

The Auto-Negotiation function selected at power-up or reset can be changed at any time by writing to the Basic Mode Control Register (BMCR) at address 00h.

Table 5-1. Auto-Negotiation Modes

AN_EN	AN1	AN0	FORCED MODE
0	0	0	10BASE-T, Half-Duplex
0	0	1	10BASE-T, Full-Duplex
0	1	0	100BASE-TX, Half-Duplex
0	1	1	100BASE-TX, Full-Duplex
AN_EN	**AN1**	**AN0**	**ADVERTISED MODE**
1	0	0	10BASE-T, Half/Full-Duplex
1	0	1	100BASE-TX, Half/Full-Duplex
1	1	0	100BASE-TX Full-Duplex
1	1	1	10BASE-T, Half/Full-Duplex
			100BASE-TX, Half/Full-Duplex

5.3.2.2 Auto-Negotiation Register Control

When Auto-Negotiation is enabled, the DP83640 transmits the abilities programmed into the Auto-Negotiation Advertisement register (ANAR) at address 04h through FLP Bursts. Any combination of 10 Mb/s, 100 Mb/s, Half-Duplex, and Full-Duplex modes may be selected.

Auto-Negotiation Priority Resolution:

1. 100BASE-TX Full Duplex (Highest Priority)
2. 100BASE-TX Half Duplex
3. 10BASE-T Full Duplex
4. 10BASE-T Half Duplex (Lowest Priority)

The Basic Mode Control Register (BMCR) at address 00h provides control for enabling, disabling, and restarting the Auto-Negotiation process. When Auto-Negotiation is disabled, the SPEED SELECTION bit in the BMCR controls switching between 10 Mb/s or 100 Mb/s operation, and the DUPLEX MODE bit controls switching between full-duplex operation and half-duplex operation. The SPEED SELECTION and DUPLEX MODE bits have no effect on the mode of operation when the Auto-Negotiation Enable bit is set.

The Link Speed can be examined through the PHY Status Register (PHYSTS) at address 10h after a Link is achieved.

The Basic Mode Status Register (BMSR) indicates the set of available abilities for technology types, Auto-Negotiation ability, and Extended Register Capability. These bits are permanently set to indicate the full functionality of the DP83640 (only the 100BASE-T4 bit is not set because the DP83640 does not support that function).

The BMSR also provides status on:

- Whether or not Auto-Negotiation is complete
- Whether or not the Link Partner is advertising that a remote fault has occurred
- Whether or not valid link has been established
- Support for Management Frame Preamble suppression

The Auto-Negotiation Advertisement Register (ANAR) indicates the Auto-Negotiation abilities to be advertised by the DP83640. All available abilities are transmitted by default, but any ability can be suppressed by writing to the ANAR. Updating the ANAR to suppress an ability is one way for a management agent to change (restrict) the technology that is used.

The Auto-Negotiation Link Partner Ability Register (ANLPAR) at address 05h is used to receive the base link code word as well as all next page code words during the negotiation. Furthermore, the ANLPAR will be updated to either 0081h or 0021h for parallel detection to either 100 Mb/s or 10 Mb/s respectively.

The Auto-Negotiation Expansion Register (ANER) indicates additional Auto-Negotiation status. The ANER provides status on:

- Whether or not a Parallel Detect Fault has occurred
- Whether or not the Link Partner supports the Next Page function
- Whether or not the DP83640 supports the Next Page function
- Whether or not the current page being exchanged by Auto-Negotiation has been received
- Whether or not the Link Partner supports Auto-Negotiation

5.3.2.3 Auto-Negotiation Parallel Detection

The DP83640 supports the Parallel Detection function as defined in the IEEE 802.3 specification. Parallel Detection requires both the 10 Mb/s and 100 Mb/s receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation but is transmitting link signals that the 100BASE-TX or 10BASE-T PMAs recognize as valid link signals.

If the DP83640 completes Auto-Negotiation as a result of Parallel Detection, bits 5 and 7 within the ANLPAR register will be set to reflect the mode of operation present in the Link Partner. Note that bits 4:0 of the ANLPAR will also be set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that negotiation completed through Parallel Detection by reading a zero in the Link Partner Auto-Negotiation Able bit once the Auto-Negotiation Complete bit is set. If configured for parallel detect mode and any condition other than a single good link occurs then the parallel detect fault bit will be set.

5.3.2.4 Auto-Negotiation Restart

Once Auto-Negotiation has completed, it may be restarted at any time by setting bit 9 (Restart Auto-Negotiation) of the BMCR to one. If the mode configured by a successful Auto-Negotiation loses a valid link, then the Auto-Negotiation process will resume and attempt to determine the configuration for the link. This function ensures that a valid configuration is maintained if the cable becomes disconnected.

A renegotiation request from any entity, such as a management agent, will cause the DP83640 to halt any transmit data and link pulse activity until the break_link_timer expires (approximately 1500 ms). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The DP83640 will resume Auto-Negotiation after the break_link_timer has expired by issuing FLP (Fast Link Pulse) bursts.

5.3.2.5 Enabling Auto-Negotiation Through Software

It is important to note that if the DP83640 has been initialized upon power-up as a non-auto-negotiating device (forced technology), and it is then required that Auto-Negotiation or re-Auto-Negotiation be initiated through software, bit 12 (Auto-Negotiation Enable) of the Basic Mode Control Register (BMCR) must first be cleared and then set for any Auto-Negotiation function to take effect.

5.3.2.6 Auto-Negotiation Complete Time

Parallel detection and Auto-Negotiation take approximately 2-3 seconds to complete. In addition, Auto-Negotiation with next page should take approximately 2-3 seconds to complete, depending on the number of next pages sent.

Refer to Clause 28 of the IEEE 802.3 standard for a full description of the individual timers related to Auto-Negotiation.

5.3.3 Auto-MDIX

When enabled, this function uses Auto-Negotiation to determine the proper configuration for transmission and reception of data and subsequently selects the appropriate MDI pair for MDI/MDIX operation. The function uses a random seed to control switching of the crossover circuitry. This implementation complies with the corresponding IEEE 802.3 Auto-Negotiation and Crossover Specifications.

Auto-MDIX is enabled by default and can be configured through PHYCR (19h) register, bits [15:14].

Neither Auto-Negotiation nor Auto-MDIX is required to be enabled in forcing crossover of the MDI pairs. Forced crossover can be achieved through the FORCE_MDIX bit, bit 14 of PHYCR (19h) register.

NOTE: Auto-MDIX will not work in a forced mode of operation.

5.3.4 LED Interface

The DP83640 supports three configurable Light Emitting Diode (LED) pins: LED_LINK, LED_SPEED/FX_SD, and LED_ACT.

Several functions can be multiplexed onto the three LEDs using three different modes of operation. The LED operation mode can be selected by writing to the LED_CFG[1:0] register bits in the PHY Control Register (PHYCR) at address 19h, bits [6:5]. LED_CFG[1] is only controllable through register access and cannot be set by a strap pin.

See Table 5-2 for LED Mode selection.

Table 5-2. LED Mode Selection

MODE	LED_CFG[1]	LED_CFG[0]	LED_LINK	LED_SPEED	LED_ACT
1	don't care	1	ON for Good Link	ON in 100 Mb/s	ON for Activity
			OFF for No Link	OFF in 10 Mb/s	OFF for No Activity
2	0	0	ON for Good Link	ON in 100 Mb/s	ON for Collision
			BLINK for Activity	OFF in 10 Mb/s	OFF for No Collision
3	1	0	ON for Good Link	ON in 100 Mb/s	ON for Full Duplex
			BLINK for Activity	OFF in 10 Mb/s	OFF for Half Duplex

The LED_LINK pin in Mode 1 indicates the link status of the port. In 100BASE-TX mode, link is established as a result of input receive amplitude compliant with the TP-PMD specifications which will result in internal generation of signal detect. A 10 Mb/s Link is established as a result of the reception of at least seven consecutive normal Link Pulses or the reception of a valid 10BASE-T packet. This will cause the assertion of LED_LINK. LED_LINK will deassert in accordance with the Link Loss Timer as specified in the IEEE 802.3 specification. In 100BASE-TX mode, an optional fast link loss detection may be enabled by setting the SD_TIME control in the SD_CNFG register. Enabling fast link loss detection will result in the LED_LINK deassertion within approximately 1.3 µs of loss of signal on the wire.

The LED_LINK pin in Mode 1 will be OFF when no LINK is present.

The LED_LINK pin in Mode 2 and Mode 3 will be ON to indicate Link is good and BLINK to indicate activity is present on activity. The BLINK frequency is defined in BLINK_FREQ, bits [7:6] of register LEDCR (18h).

Activity is defined as configured in LEDACT_RX, bit 8 of register LEDCR (18h). If LEDACT_RX is 0, Activity is signaled for either transmit or receive. If LEDACT_RX is 1, Activity is only signaled for receive.

The LED_SPEED/FX_SD pin indicates 10- or 100 Mb/s data rate of the port. The standard CMOS driver goes high when operating in 100 Mb/s operation. The functionality of this LED is independent of mode selected.

The LED_ACT pin in Mode 1 indicates the presence of either transmit or receive activity. The LED will be ON for Activity and OFF for No Activity. In Mode 2, this pin indicates the Collision status of the port. The LED will be ON for Collision and OFF for No Collision.

The LED_ACT pin in Mode 3 indicates Duplex status for 10- Mb/s or 100 Mb/s operation. The LED will be ON for Full Duplex and OFF for Half Duplex.

In 10 Mb/s half-duplex mode, the collision LED is based on the COL signal.

Because these LED pins are also used as strap options, the polarity of the LED is dependent on whether the pin is pulled up or down.

5.3.4.1 LEDs

Because the Auto-Negotiation (AN) strap options share the LED output pins, the external components required for strapping and LED usage must be considered in order to avoid contention.

Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding AN input upon power-up/reset. For example, if a given AN input is resistively pulled low, then the corresponding output will be configured as an active high driver. Conversely, if a given AN input is resistively pulled high, then the corresponding output will be configured as an active low driver.

Refer to Figure 5-2 for an example of AN connections to external components. In this example, the AN strapping results in Auto-Negotiation disabled with 100 Full-Duplex forced.

The adaptive nature of the LED outputs helps to simplify potential implementation issues of these dual purpose pins.

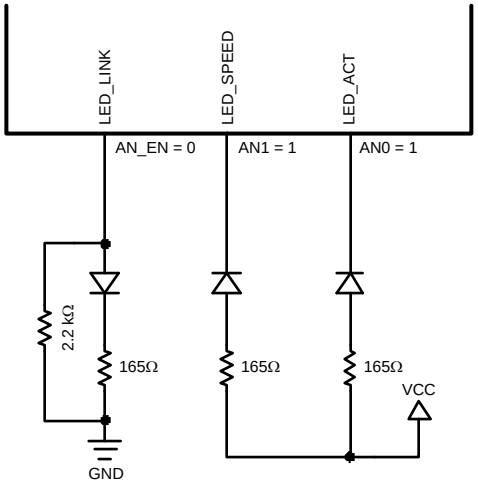


Figure 5-2. AN Strapping and LED Loading Example

5.3.4.2 LED Direct Control

The DP83640 provides another option to directly control any or all LED outputs through the LED Direct Control Register (LEDCR), address 18h. The register does not provide read access to LEDs.

5.3.5 Internal Loopback

The DP83640 includes a Loopback Test mode for facilitating system diagnostics. The Loopback mode is selected through bit 14 (Loopback) of the Basic Mode Control Register (BMCR). Writing 1 to this bit enables MII transmit data to be routed to the MII receive outputs. Loopback status may be checked in bit 3 of the PHY Status Register (PHYSTS). While in Loopback mode the data will not be transmitted onto the media. To ensure that the desired operating mode is maintained, Auto-Negotiation should be disabled before selecting the Loopback mode.

5.3.6 Power Down/Interrupt

The Power Down and Interrupt functions are multiplexed on pin 7 of the device. By default, this pin functions as a power-down input and the interrupt function is disabled. Setting bit 0 (INT_OE) of MICR (11h) will configure the pin as an active low interrupt output.

5.3.6.1 Power Down Control Mode

The PWRDOWN/INTN pin can be asserted low to put the device in a Power Down mode. This is equivalent to setting bit 11 (POWER DOWN) in the Basic Mode Control Register, BMCR (00h). An external control signal can be used to drive the pin low, overcoming the weak internal pullup resistor. Alternatively, the device can be configured to initialize into a Power Down state by use of an external pulldown resistor on the PWRDOWN/INTN pin. Because the device will still respond to management register accesses, setting the INT_OE bit in the MICR register will disable the PWRDOWN/INTN input, allowing the device to exit the Power Down state.

5.3.6.2 Interrupt Mechanisms

The interrupt function is controlled through register access. All interrupt sources are disabled by default. Setting bit 1 (INTEN) of MICR (11h) will enable interrupts to be output, dependent on the interrupt mask set in the lower byte of the MISR (12h). The PWRDOWN/INTN pin is asynchronously asserted low when an interrupt condition occurs. The source of the interrupt can be determined by reading the upper byte of the MISR. One or more bits in the MISR will be set, denoting all currently pending interrupts. Reading of the MISR clears ALL pending interrupts.

Example: To generate an interrupt on a change of link status or on a change of energy detect power state, the steps would be:

- Write 0003h to MICR to set INTEN and INT_OE
- Write 0060h to MISR to set ED_INT_EN and LINK_INT_EN
- Monitor PWRDOWN/INTN pin

When PWRDOWN/INTN pin asserts low, the user would read the MISR register to see if the ED_INT or LINK_INT bits are set, that is, which source caused the interrupt. After reading the MISR, the interrupt bits should clear and the PWRDOWN/INTN pin will deassert.

5.3.7 Energy Detect Mode

When Energy Detect is enabled and there is no activity on the cable, the DP83640 will remain in a low power mode while monitoring the transmission line. Activity on the line will cause the DP83640 to go through a normal power up sequence. Regardless of cable activity, the DP83640 will occasionally wake up the transmitter to put ED pulses on the line, but will otherwise draw as little power as possible. Energy detect functionality is controlled through register Energy Detect Control (EDCR), address 1Dh.

5.3.8 Link Diagnostic Capabilities

The DP83640 contains several system diagnostic capabilities for evaluating link quality and detecting potential cabling faults in twisted pair cabling. Software configuration is available through the Link Diagnostics Registers - Page 2 which can be selected through Page Select Register (PAGESEL), address 13h. These capabilities include:

- Linked Cable Status
- Link Quality Monitor
- TDR (Time Domain Reflectometry) Cable Diagnostics

5.3.8.1 Linked Cable Status

In an active connection with a valid link status, the following diagnostic capabilities are available:

- Polarity reversal
- Cable swap (MDI vs MDIX) detection
- 100-Mb Cable Length Estimation
- Frequency offset relative to link partner
- Cable Signal Quality Estimation

5.3.8.1.1 Polarity Reversal

The DP83640 detects polarity reversal by detecting negative link pulses. The Polarity indication is available in bit 12 of the PHYSTS (10h) or bit 4 of the 10BTSCR (1Ah). Inverted polarity indicates the positive and negative conductors in the receive pair are swapped. Because polarity is corrected by the receiver, this does not necessarily indicate a functional problem in the cable.

Because the polarity indication is dependent on link pulses from the link partner, polarity indication is only valid in 10-Mb modes of operation, or in 100-Mb Auto-Negotiated mode. Polarity indication is not available in 100-Mb forced mode of operation or in a parallel detected 100-Mb mode.

5.3.8.1.2 Cable Swap Indication

As part of Auto-Negotiation, the DP83640 has the ability (using Auto-MDIX) to automatically detect a cable with swapped MDI pairs and select the appropriate pairs for transmitting and receiving data. Normal operation is termed MDI, while crossed operation is MDIX. The MDIX status can be read from bit 14 of the PHYSTS (10h).

5.3.8.1.3 100-Mb Cable Length Estimation

The DP83640 provides a method of estimating cable length based on electrical characteristics of the 100-Mb link. This essentially provides an effective cable length rather than a measurement of the physical cable length. The cable length estimation is only available in 100-Mb mode of operation with a valid link status. The cable length estimation is available at the Link Diagnostics Registers - Page 2, register 100 Mb Length Detect (LEN100_DET), address 14h.

5.3.8.1.4 Frequency Offset Relative to Link Partner

As part of the 100-Mb clock recovery process, the DSP implementation provides a frequency control parameter. This value may be used to indicate the frequency offset of the device relative to the link partner. This operation is only available in 100-Mb operation with a valid link status. The frequency offset can be determined using the register 100-Mb Frequency Offset Indication (FREQ100), address 15h, of the Link Diagnostics Registers - Page 2.

Two different versions of the Frequency Offset may be monitored through bits [7:0] of register FREQ100 (15h). The first is the long-term Frequency Offset. The second is the current Frequency Control value, which includes short-term phase adjustments and can provide information on the amount of jitter in the system.

5.3.8.1.5 Cable Signal Quality Estimation

The cable signal quality estimator keeps a simple tracking of results of the DSP and can be used to generate an approximate Signal-to-Noise Ratio for the 100 Mb receiver. This information is available to software through the Link Diagnostics Registers - Page 2: Variance Control Register (VAR_CTRL), address 1Ah and Variance Data Register (VAR_DATA), address 1Bh.

The variance computation times (VAR_TIMER) can be chosen from the set of {2, 4, 6, 8} ms. The 32-bit variance sum can be read by two consecutive reads of the VAR_DATA register. This sum can be used to compute an SNR estimate by software using the following equation:

$$SNR = 10\log_{10}((37748736 * VAR\_TIMER) / Variance) \quad (1)$$

5.3.8.2 Link Quality Monitor

The Link Quality Monitor allows a method to generate an alarm when the DSP adaption strays from a programmable window. This could occur due to changes in the cable which could indicate a potential problem. Software can program thresholds for the following DSP parameters to be used to interrupt the system:

- Digital Equalizer C1 Coefficient (DEQ C1)
- Digital Adaptive Gain Control (DAGC)
- Digital Base-Line Wander Control (DBLW)
- Recovered Clock Long-Term Frequency Offset (FREQ)
- Recovered Clock Frequency Control (FC)
- Signal-to-Noise Ratio (SNR) Variance

Software is expected to read initial adapted values and then program the thresholds based on an expected valid range. This mechanism takes advantage of the fact that the DSP adaptation should remain in a relatively small range once a valid link has been established.

5.3.8.2.1 Link Quality Monitor Control and Status

Control of the Link Quality Monitor is done through the Link Quality Monitor Register (LQMR), address 1Dh and the Link Quality Data Register (LQDR), address 1Bh of the Link Diagnostics Registers - Page 2. The LQMR register includes a global enable to enable the Link Quality Monitor function. In addition, it provides warning status from both high and low thresholds for each of the monitored parameters except SNR Variance.. The LQMR2 register provides warning status for the high threshold of SNR Variance (upper 16 bits); there is no low threshold. Note that individual low or high parameter threshold comparisons can be disabled by setting to the minimum or maximum values.

To allow the Link Quality Monitor to interrupt the system, the Interrupt must be enabled through the interrupt control registers, MICR (11h) and MISR (12h).

The Link Quality Monitor may also be used to automatically reset the DSP and restart adaption. Separate enable bits in LQMR and LQMR2 allow for automatic reset based on each of the parameter values. If enabled, a violation of one of the thresholds will result in a restart of the DSP adaption. In addition if the PCSR:SD_OPTION register bit is set to 0, the violation will also result in a drop in Link Status.

5.3.8.2.2 Checking Current Parameter Values

Prior to setting Threshold values, it is recommended that software check current adapted values. The thresholds may then be set relative to the adapted values. The current adapted values can be read using the LQDR register by setting the SAMPLE_PARAM bit [13] of LQDR, address (1Eh).

For example, to read the DBLW current value:

1. Write 2400h to LQDR (1Eh) to set the SAMPLE_PARAM bit and set the LQ_PARAM_SEL[2:0] to 010.
2. Read LQDR (1Eh). Current DBLW value is returned in the low 8 bits.

5.3.8.2.3 Threshold Control

The LQDR (1Eh) register also provides a method of programming high and low thresholds for each of the five parameters that can be monitored. The register implements an indirect read/write mechanism.

Writes are accomplished by writing data, address, and a write strobe to the register. Reads are accomplished by writing the address to the register, and reading back the value of the selected threshold. Setting thresholds to the maximum or minimum values will disable the threshold comparison because values have to exceed the threshold to generate a warning condition.

Warnings are not generated if the parameter is equal to the threshold. By default, all thresholds are disabled by setting to the minimum or maximum values. Table 5-3 shows the five parameters and range of values:

Table 5-3. Link Quality Monitor Parameter Ranges

PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	MIN (2-s COMP)	MAX (2-s COMP)
DEQ_C1	–128	+127	0x80	0x7F
DAGC	0	+255	0x00	0xFF
DBLW	–128	+127	0x80	0x7F
Frequency Offset	–128	+127	0x80	0x7F
Frequency Control	–128	+127	0x80	0x7F
SNR Variance	0	+2304	0x0000	0x900

Note that values are signed 2-s complement values except for DAGC and Variance which are always positive. The maximum SNR Variance is calculated by assuming the worst-case squared error (144) is accumulated every 8 ns for $8*2^{20}$ ns (roughly 8 ms or exactly 1,048,576 clock cycles).

For example, to set the DBLW Low threshold to –38:

1. Write 14DAh to LQDR to set the Write_LQ_Thr bit, select the DBLW Low Threshold, and write data of –38 (0xDA).
2. Write 8000 to LQMR to enable the Link Quality Monitor (if not already enabled).

5.3.8.3 TDR Cable Diagnostics

The DP83640 implements a Time Domain Reflectometry (TDR) method of cable length measurement and evaluation which can be used to evaluate a connected twisted pair cable. The TDR implementation involves sending a pulse out on either the Transmit or Receive conductor pair and observing the results on either pair. By observing the types and strength of reflections on each pair, software can determine the following:

- Cable short
- Cable open
- Distance to fault
- Identify which pair has a fault
- Pair skew

The TDR cable diagnostics works best in certain conditions. For example, an unterminated cable provides a good reflection for measuring cable length, while a cable with an ideal termination to an unpowered partner may provide no reflection at all.

5.3.8.4 TDR Pulse Generator

The TDR implementation can send two types of TDR pulses. The first option is to send 50-ns or 100-ns link pulses from the 10-Mb Common Driver. The second option is to send pulses from the 100-Mb Common Driver in 8-ns increments up to 56 ns in width. The 100-Mb pulses will alternate between positive and negative pulses. The shorter pulses provide better ability to measure short cable lengths, especially because they will limit overlap between the transmitted pulse and a reflected pulse. The longer pulses may provide better measurements of long cable lengths.

In addition, if the pulse width is programmed to 0, no pulse will be sent, but the monitor circuit will still be activated. This allows sampling of background data to provide a baseline for analysis.

5.3.8.5 TDR Pulse Monitor

The TDR function monitors data from the Analog to Digital Converter (ADC) to detect both peak values and values above a programmable threshold. It can be programmed to detect maximum or minimum values. In addition, it records the time, in 8 ns intervals, at which the peak or threshold value first occurs.

The TDR monitor implements a timer that starts when the pulse is transmitted. A window may be enabled to qualify incoming data to look for response only in a desired range. This is especially useful for eliminating the transmitted pulse, but also may be used to look for multiple reflections.

5.3.8.6 TDR Control Interface

The TDR Control Interface is implemented in the Link Diagnostics Registers - Page 2 through TDR Control (TDR_CTRL), address 16h and TDR Window (TDR_WIN), address 17h. The following basic controls are:

- **TDR Enable:** Enable bit 15 of TDR_CTRL (16h) to allow the TDR function. This bypasses normal operation and gives control of the CD10 and CD100 block to the TDR function.
- **TDR Send Pulse:** Enable bit 11 of TDR_CTRL (16h) to send the TDR pulse and starts the TDR Monitor

The following transmit mode controls are available:

- **Transmit Mode:** Enables use of 10 Mb Link pulses from the 10 Mb Common Driver or data pulses from the 100 Mb Common Driver by enabling TDR_100 Mb, bit 14 of TDR_CRTL (16h).

- **Transmit Pulse Width:** Bits [10:8] of TDR_CTRL (16h) allows sending of 0 to 7 clock width pulses. Actual pulses are dependent on the transmit mode. If the pulse width is set to 0, then no pulse will be sent.
- **Transmit Channel Select:** The transmitter can send pulses down either the transmit pair or the receive pair by enabling bit 13 of TDR_CTRL (16h). Default value is to select the transmit pair.

The following receive mode controls are available:

- **Min/Max Mode Control:** Bit 7 of TDR_CTRL (16h) controls the TDR Monitor operation. In default mode, the monitor will detect maximum (positive) values. In Min Mode, the monitor will detect minimum (negative) values.
- **Receive Channel Select:** The receiver can monitor either the transmit pair or the receive pair by enabling bit 12 of TDR_CTRL (16h). Default value is to select the transmit pair.
- **Receive Window:** The receiver can monitor receive data within a programmable window using the TDR Window Register (TDR_WIN), address 17h. The window is controlled by two register values: TDR Start Window, bits [15:8] of TDR_WIN (17h) and TDR Stop Window, bits [7:0] of TDR_WIN (17h). The TDR Start Window indicates the first clock to start sampling. The TDR Stop Window indicates the last clock to sample. By default, the full window is enabled, with Start set to 0 and Stop set to 255. The window range is in 8-ns clock increments, so the maximum window size is 2048 ns.

5.3.8.7 TDR Results

The results of a TDR peak and threshold measurement are available in the TDR Peak Measurement Register (TDR_PEAK), address 18h and TDR Threshold Measurement Register (TDR_THR), address 19h. The threshold measurement may be a more accurate method of measuring the length of longer cables because it provides a better indication of the start of the received pulse, rather than the peak value.

Software utilizing the TDR function should implement an algorithm to send TDR pulses and evaluate results. Multiple runs should be used to best qualify any received pulses as multiple reflections could exist. In addition, when monitoring the transmitting pair, the window feature should be used to disqualify the transmitted pulse. Multiple runs may also be used to average the values providing more accurate results.

Actual distance measurements are dependent on the velocity of propagation of the cable. The delay value is typically on the order of 4.6 to 4.9 ns/m.

5.3.9 BIST

The DP83640 incorporates an internal Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. BIST testing can be performed with the part in the internal loopback mode or externally looped back using a loopback cable fixture. BIST testing can also be performed between two directly connected DP83640 devices.

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo random sequence. The user can select a 9 bit or 15 bit pseudo random sequence from the PSR_15 bit in the PHY Control Register (PHYCR). The received data is compared to the generated pseudo-random data by the BIST Linear Feedback Shift Register (LFSR) to determine the BIST pass/fail status.

The pass/fail status of the BIST is stored in the BIST status bit in the PHYCR register. The status bit defaults to 0 (BIST fail) and will transition on a successful comparison. If an error (mis-compare) occurs, the status bit is latched and is cleared upon a subsequent write to the Start/Stop bit.

For transmit VOD testing, the Packet BIST Continuous Mode can be used to allow continuous data transmission by setting the BIST_CONT_MODE, bit 5, of CDCTRL1 (1Bh).

The number of BIST errors can be monitored through the BIST Error Count in the CDCTRL1 (1Bh), bits [15:8].

5.4 Device Functional Modes

5.4.1 MAC Interface

The DP83640 supports several modes of operation using the MII interface pins. The options are defined in the following sections and include:

- MII Mode
- RMII Mode
- Single Clock MII Mode (SCMII)

In addition, the DP83640 supports the standard 802.3 MII Serial Management Interface.

The modes of operation can be selected by strap options or register control. For RMII Slave mode, it is recommended to use the strap option because it requires a 50-MHz clock instead of the normal 25 MHz.

In each of these modes, the IEEE 802.3 serial management interface is operational for device configuration and status. The serial management interface of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHY(s).

5.4.2 MII Interface

The DP83640 incorporates the Media Independent Interface (MII) as specified in Clause 22 of the IEEE 802.3 standard. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems. This section describes the nibble wide MII data interface.

The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC).

5.4.2.1 Nibble-Wide MII Data Interface

Clause 22 of the IEEE 802.3 specification defines the Media Independent Interface. This interface includes a dedicated receive bus and a dedicated transmit bus. These two data buses, along with various control and status signals, allow for the simultaneous exchange of data between the DP83640 and the upper layer agent (MAC).

The receive interface consists of a nibble-wide data bus RXD[3:0], a receive error signal RX_ER, a receive data valid flag RX_DV, and a receive clock RX_CLK for synchronous transfer of the data. The receive clock operates at either 2.5 MHz to support 10 Mb/s operation modes or at 25 MHz to support 100 Mb/s operational modes.

The transmit interface consists of a nibble-wide data bus TXD[3:0], a transmit enable control signal TX_EN, and a transmit clock TX_CLK which runs at either 2.5 MHz or 25 MHz.

Additionally, the MII includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half-Duplex mode. The COL signal asserts as an indication of a collision which can occur during half-duplex operation when both a transmit and receive operation occur simultaneously.

5.4.2.2 Collision Detect

For Half Duplex, a 10BASE-T or 100BASE-TX collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

If the DP83640 is transmitting in 10 Mb/s mode when a collision is detected, the collision is not reported until seven bits have been received while in the collision state. This prevents a collision being reported incorrectly due to noise on the network. The COL signal remains set for the duration of the collision.

If a collision occurs during a receive operation, it is immediately reported by the COL signal.

When heartbeat is enabled (only applicable to 10 Mb/s operation), approximately 1 µs after the transmission of each packet, a Signal Quality Error (SQE) signal of approximately 10 bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

Collision is not indicated during Full-Duplex operation.

5.4.2.3 Carrier Sense

In 10 Mb/s operation, Carrier Sense (CRS) is asserted due to receive activity once valid data is detected through the Smart Squelch function. During 100 Mb/s operation CRS is asserted when a valid link (SD) and two non-contiguous zeros are detected on the line.

For 10- or 100 Mb/s Half-Duplex operation, CRS is asserted during either packet transmission or reception.

For 10- or 100 Mb/s Full-Duplex operation, CRS is asserted only due to receive activity.

CRS is deasserted following an end of packet.

5.4.3 Reduced MII Interface

The DP83640 incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification (rev 1.2) from the RMII Consortium. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems using a reduced number of pins. In this mode, data is transferred 2-bits at a time using the 50-MHz RMII_REF clock for both transmit and receive. The following pins are used in RMII mode:

- TX_EN
- TXD[1:0]
- RX_ER (optional for MAC)
- CRS/CRS_DV
- RXD[1:0]
- X1 (25 MHz in RMII Master mode, 50 MHz in RMII Slave mode)
- RX_CLK, TX_CLK, CLK_OUT (50-MHz RMII reference clock in RMII Master mode only)

In addition, the RMII mode supplies an RX_DV signal which allows for a simpler method of recovering receive data without having to separate RX_DV from the CRS_DV indication. This is especially useful for systems which do not require CRS, such as systems that only support full-duplex operation. This signal is also useful for diagnostic testing where it may be desirable to loop external Receive RMII data directly to the transmitter.

The RX_ER output may be used by the MAC to detect error conditions. It is asserted for symbol errors received during a packet, False Carrier events, and also for FIFO underrun or overrun conditions. Because the PHY is required to corrupt receive data on an error, a MAC is not required to use RX_ER.

Because the reference clock operates at 10 times the data rate for 10 Mb/s operation, transmit data is sampled every 10 clocks. Likewise, receive data will be generated every 10th clock so that an attached device can sample the data every 10 clocks.

RMII Slave mode requires a 50-MHz oscillator to be connected to the device X1 pin. A 50-MHz crystal is not supported. RMII Master mode can use either a 25-MHz oscillator connected to X1 or a 25-MHz crystal connected to X1 and X2.

To tolerate potential frequency differences between the 50-MHz reference clock and the recovered receive clock, the receive RMII function includes a programmable elasticity buffer. The elasticity buffer is programmable to minimize propagation delay based on expected packet size and clock accuracy. This allows for supporting a range of packet sizes including jumbo frames.

The elasticity buffer will force Frame Check Sequence errors for packets which overrun or underrun the FIFO. Underrun and overrun conditions can be reported in the RMII and Bypass Register (RBR). Table 5-4 indicates how to program the elasticity buffer FIFO (in 4-bit increments) based on expected maximum packet size and clock accuracy. It assumes both clocks (RMII Reference clock and far-end Transmitter clock) have the same accuracy.

Packet lengths can be scaled linearly based on accuracy (±25 ppm would allow packets twice as large). If the threshold setting must support both 10-Mb and 100-Mb operation, the setting should be made to support both speeds.

Table 5-4. Supported Packet Sizes at ±50 ppm Frequency Accuracy

START THRESHOLD RBR[1:0]	LATENCY TOLERANCE		RECOMMENDED PACKET SIZE at ±50 ppm	
	100 Mb	10 Mb	100 Mb	10 Mb
01 (default)	2 bits	8 bits	2,400 bytes	9,600 bytes
10	6 bits	4 bits	7,200 bytes	4,800 bytes
11	10 bits	8 bits	12,000 bytes	9,600 bytes
00	14 bits	12 bits	16,800 bytes	14,400 bytes

5.4.3.1 RMII Master Mode

In RMII Master Mode, the DP83640 uses a 25-MHz crystal on X1/X2 and internally generates the 50-MHz RMII reference clock for use by the RMII logic. The 50-MHz clock is output on RX_CLK, TX_CLK, and CLK_OUT for use as the reference clock for an attached MAC. RX_CLK operates at 25 MHz during reset.

5.4.3.2 RMII Slave Mode

In RMII Slave Mode, the DP83640 takes a 50-MHz reference clock input on X1 from an external oscillator or another DP83640 in RMII Master Mode. The 50 MHz is internally divided down to 25 MHz for use as the reference clock for non-RMII logic. RX_CLK, TX_CLK, and CLK_OUT should not be used as the RMII reference clock in this mode but may be used for other system devices.

5.4.4 Single Clock MII Mode

Single Clock MII (SCMII) Mode allows MII operation using a single 25-MHz reference clock. Normal MII Mode requires three clocks, a reference clock for physical layer functions, a transmit MII clock, and a receive MII clock. Similar to RMII mode, Single Clock MII mode requires only the reference clock. In addition to reducing the number of pins required, this mode allows the attached MAC device to use only the reference clock domain. AC Timing requirements for SCMII operation are similar to the RMII timing requirements.

For 10 Mb operation, as in RMII mode, data is sampled and driven every 10 clocks because the reference clock is at 10 times the data rate.

Separate control bits allow enabling the Transmit and Receive Single Clock modes separately, allowing just transmit or receive to operate in this mode. Control of Single Clock MII mode is through the RBR register.

Single Clock MII mode incorporates the use of the RMII elasticity buffer, which is required to tolerate potential frequency differences between the 25-MHz reference clock and the recovered receive clock. Settings for the elasticity buffer for SCMII mode are detailed in Table 5-5.

Table 5-5. Supported SCMII Packet Sizes at ±50 ppm Frequency Accuracy

START THRESHOLD RBR[1:0]	LATENCY TOLERANCE		RECOMMENDED PACKET SIZE at ±50 ppm	
	100 Mb	10 Mb	100 Mb	10 Mb
01 (default)	4 bits	8 bits	4,000 bytes	9,600 bytes
10	4 bits	8 bits	4,000 bytes	9,600 bytes
11	8 bits	8 bits	9,600 bytes	9,600 bytes
00	8 bits	8 bits	9,600 bytes	9,600 bytes

5.4.5 IEEE 802.3 MII Serial Management Interface

5.4.5.1 Serial Management Register Access

The serial management MII specification defines a set of thirty-two 16-bit status and control registers that are accessible through the management interface pins MDC and MDIO. The DP83640 implements all the required MII registers as well as several optional registers. These registers are fully described in *Section 5.6*. A description of the serial management access protocol follows.

Table 5-6. Typical MDIO Frame Format

MII MANAGEMENT SERIAL PROTOCOL	<idle><start><opcode><device addr><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

5.4.5.2 Serial Management Access Protocol

The serial control interface consists of two pins, Management Data Clock (MDC) and Management Data Input/Output (MDIO). MDC has a maximum clock rate of 25 MHz and no minimum rate. The MDIO line is bi-directional and may be shared by up to 32 devices. The MDIO frame format is shown in Table 5-6.

The MDIO pin requires a pullup resistor (1.5 kΩ) which, during IDLE and turnaround, will pull MDIO high. The DP83640 also includes an option to enable an internal pullup on the MDIO pin, MDIO_PULL_EN bit in the CDCTRL1 register. In order to initialize the MDIO interface, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide the DP83640 with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pullup resistor to pull the MDIO pin high during which time 32 MDC clock cycles are provided. In addition 32 MDC clock cycles should be used to re-sync the device if an invalid Start, Opcode, or turnaround bit is detected.

The DP83640 waits until it has received this preamble sequence before responding to any other transaction. Once the DP83640 serial management port has been initialized no further preamble sequencing is required until after a power-on/reset, invalid Start, invalid Opcode, or invalid turnaround (TA) bit has occurred.

The Start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state.

Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device shall actively drive the MDIO signal during the first bit of Turnaround. The addressed DP83640 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 5-3 shows the timing relationship between MDC and the MDIO as driven/received by the Station (STA) and the DP83640 (PHY) for a typical register read access.

For write transactions, the station management entity writes data to the addressed DP83640 thus eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity by inserting <10>. Figure 5-4 shows the timing relationship for a typical MII register write access.

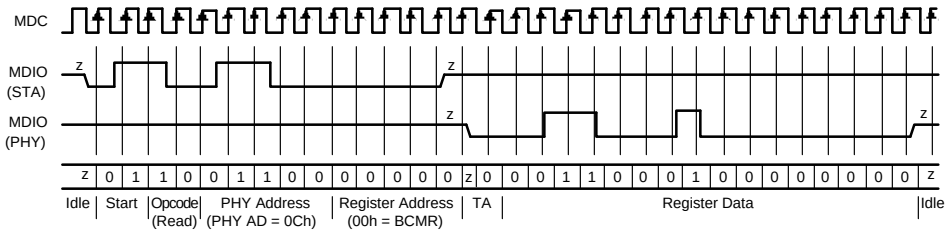


Figure 5-3. Typical MDC/MDIO Read Operation

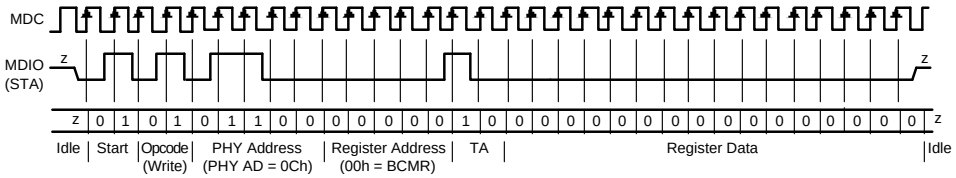


Figure 5-4. Typical MDC/MDIO Write Operation

5.4.5.3 Serial Management Preamble Suppression

The DP83640 supports a Preamble Suppression mode as indicated by a one in bit 6 of the Basic Mode Status Register (BMSR, address 01h.) If the station management entity (that is, MAC or other management controller) determines that all PHYs in the system support Preamble Suppression by returning a one in this bit, then the station management entity need not generate preamble for each management transaction.

The DP83640 requires a single initialization sequence of 32 bits of preamble following hardware/software reset. This requirement is generally met by the mandatory pullup resistor on MDIO in conjunction with a continuous MDC, or the management access made to determine whether Preamble Suppression is supported.

While the DP83640 requires an initial preamble sequence of 32 bits for management initialization, it does not require a full 32-bit sequence between each subsequent transaction. A *minimum of one idle bit between management transactions is required* as specified in the IEEE 802.3 specification.

5.4.6 PHY Control Frames

The DP83640 supports a packet-based control mechanism for use in situations where the Serial Management Interface is not available or does not provide enough throughput. Application software may build a packet, called a PHY Control Frame (PCF), to be passed to the PHY through the MAC Transmit Data interface. The PHY will intercept these packets and use them to assert writes to Management Registers as if they occurred through the Management Interface. Multiple register writes may be incorporated in a single frame.

The PHY Control Frame may also be used to read a register location. The read value will be returned in a PHY Status Frame if that function is enabled. Only a single read may be outstanding at any time, so only one read should be included in a single PHY Control Frame.

The PHY Control Frame block performs the following functions:

- Parse incoming transmit packets to detect PHY Control Frames
- Truncate PHY Control Frames to prevent complete frame from reaching the transmit physical medium
- Buffer up to 15 bytes of the Frame to be intercepted by the PHY with no portion reaching physical medium
- Detect commands in the PHY Control Frame and pass them to the register block
- Check CRC to detect error conditions

- Report CRC and invalid command errors to the system through register status and/or interrupt

PHY Control Frames can be enabled through the PCF_Enable bit in the PHY Control Frames Configuration Register (PCFCR). PHY Control Frames can also be enabled by using the PCF_EN strap option. For a more detailed discussion on the use of PHY Control Frames, refer to the Software Development Guide for the DP83640.

5.4.7 PHY Status Frames

The DP83640 implements a packet-based status mechanism that allows the PHY to queue up events and pass them to the microcontroller through the receive data interface. The packet, called a PHY Status Frame, may be used to provide IEEE 1588 status for transmit packet timestamps, receive packet timestamps, event timestamps, and trigger conditions. In addition the device can generate status messages indicating packet buffering errors and to return data read using the PHY Control Frame register access mechanism.

Each PHY Status Frame may include multiple status messages. The packet will be framed such that it will look like a IEEE 1588 frame to ensure that it will get to the IEEE 1588 software stack. The PHY will provide buffering of any incoming packet to allow the status packet to be passed to the MAC. Programmable inter-frame gap and preamble length allow the PHY to recover lost bandwidth in the case of heavy receive traffic.

In a PHY Status Frame, status messages are not provided in a chronological order. Instead, they are provided in the following order of priority:

1. PHY Control Frame Read Data
2. Packet Buffer Error
3. Transmit Timestamp
4. Receive Timestamp
5. Trigger Status
6. Event Timestamp

Each of the message types may be individually enabled, allowing options on which functions may be delivered in a PHY Status Frame.

Timestamps that are delivered through PHY Status Frames will not be reflected in the corresponding status and timestamp registers nor will they generate an interrupt.

The packet format may be configured to look like a Layer 2 Ethernet frame or a UDP/IPv4 frame.

For a more detailed discussion on the use of PHY Status Frames, refer to the Software Development Guide for the DP83640.

5.4.8 PHY Address

The five PHY address strapping pins are shared with the RXD[3:0] pins and COL pin as shown in Table 5-7.

Table 5-7. PHY Address Mapping

PIN #	PHYAD FUNCTION	RXD FUNCTION
42	PHYAD0	COL
43	PHYAD1	RXD_3
44	PHYAD2	RXD_2
45	PHYAD3	RXD_1
46	PHYAD4	RXD_0

The DP83640 can be set to respond to any of 32 possible PHY addresses through strap pins. The information is latched into the PHYCR register (address 19h, bits [4:0]) at device power-up and hardware reset. Each DP83640 or port sharing an MDIO bus in a system must have a unique physical address.

The DP83640 supports PHY Address strapping values 0 (<00000>) through 31 (<11111>). **Strapping PHY Address 0 puts the part into Isolate Mode.** It should also be noted that selecting PHY Address 0 through an MDIO write to PHYCR will not put the device in Isolate Mode. See Section 5.6.1.2.6 for more information.

For further detail relating to the latch-in timing requirements of the PHY Address pins, as well as the other hardware configuration pins, refer to the Reset summary in Section 5.4.10.

Because the PHYAD[0] pin has weak internal pullup resistor and PHYAD[4:1] pins have weak internal pulldown resistors, the default setting for the PHY address is 00001 (01h).

Refer to Figure 5-5 for an example of a PHYAD connection to external components. In this example, the PHYAD strapping results in address 00011 (03h).

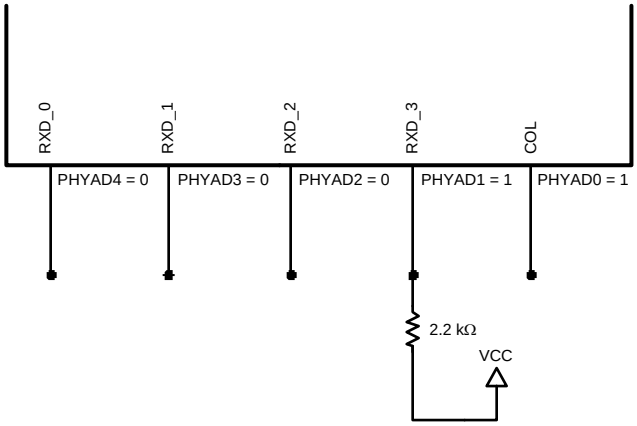


Figure 5-5. PHYAD Strapping Example

5.4.8.1 MII Isolate Mode

It is recommended that the user have a basic understanding of Clause 22 of the 802.3 standard.

The DP83640 can be put into MII Isolate Mode by writing a 1 to bit 10 of the BMCR register. Strapping the PHY Address to 0 will force the device into Isolate Mode when powered up. It should be noted that selecting Physical Address 0 through an MDIO write to PHYCR will not put the device in the MII isolate mode.

When in the MII Isolate Mode, the DP83640 does not respond to packet data present at TXD[3:0] and TX_EN inputs and presents a high impedance on the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS/CRS_DV outputs. When in Isolate Mode, the DP83640 will continue to respond to all serial management transactions over the MII.

While in Isolate Mode, the PMD output pair will not transmit packet data but will continue to source 100BASE-TX scrambled idles or 10BASE-T normal link pulses.

The DP83640 can Auto-Negotiate or parallel detect to a specific technology depending on the receive signal at the PMD input pair. A valid link can be established for the receiver even when the DP83640 is in Isolate Mode.

5.4.8.2 Broadcast Mode

The DP83640 is also capable of accepting broadcast messages (register writes to PHY address 0x1F). Setting the BC_WRITE to 1, bit 11 of the PHY Control Register 2 (PHYCR2) at address 0x1C, will configure the device to accept broadcast messages independent of the local PHY Address value.

5.4.9 Half Duplex vs. Full Duplex

The DP83640 supports both half- and full-duplex operation at both 10 Mb/s and 100 Mb/s speeds.

Half duplex relies on the CSMA/CD protocol to handle collisions and network access. In Half-Duplex mode, Carrier Sense (CRS) responds to both transmit and receive activity in order to maintain compliance with the IEEE 802.3 specification.

Because the DP83640 is designed to support simultaneous transmit and receive activity it is capable of supporting full-duplex switched applications with a throughput of up to 200 Mb/s when operating in either 100BASE-TX or 100BASE-FX. Because the CSMA/CD protocol does not apply to full-duplex operation, the DP83640 disables its own internal collision sensing and reporting functions and modifies the behavior of CRS such that it indicates only receive activity. This allows a full-duplex capable MAC to operate properly.

All modes of operation (100BASE-TX, 100BASE-FX, 10BASE-T) can run either half duplex or full duplex. Additionally, other than CRS and collision reporting, all remaining MII signaling remains the same regardless of the selected duplex mode.

It is important to understand that while Auto-Negotiation with the use of Fast Link Pulse code words can interpret and configure to full-duplex operation, parallel detection can not recognize the difference between full and half duplex from a fixed 10 Mb/s or 100 Mb/s link partner over twisted pair. As specified in the 802.3 specification, if a far-end link partner is configured to a forced full-duplex 100BASE-TX ability, the parallel detection state machine in the partner would be unable to detect the full-duplex capability of the far-end link partner. This link segment would negotiate to a half-duplex 100BASE-TX configuration (same scenario for 10 Mb/s).

Auto-Negotiation is not supported in 100BASE-FX operation. Selection of Half or Full-duplex operation is controlled by bit 8 of the Basic Mode Control Register (BMCR), address 00h. If 100BASE-FX mode is strapped using the RX_ER pin, the AN0 strap value is used to set the value of bit 8 of the BMCR (00h) register. Note that the other Auto-Negotiation strap pins (AN_EN and AN1) are ignored in 100BASE-FX mode.

5.4.10 Reset Operation

The DP83640 includes an internal power-on reset (POR) function and does not need to be explicitly reset for normal operation after power up. If required during normal operation, the device can be reset by a hardware or software reset.

5.4.10.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to the RESET_N pin. This will reset the device such that all registers will be reinitialized to default values and the hardware configuration values will be re-latched into the device (similar to the power-up/reset operation).

5.4.10.2 Full Software Reset

A full-chip software reset is accomplished by setting the RESET bit (bit 15) of the Basic Mode Control Register (BMCR). The period from the point in time when the reset bit is set to the point in time when software reset has concluded is approximately 1 µs.

The software reset will reset the device such that all registers will be reset to default values and the hardware configuration values will be maintained. Software driver code must wait 3 µs following a software reset before allowing further serial MII operations with the DP83640.

5.4.10.3 Soft Reset

A partial software reset can be initiated by setting the SOFT_RESET bit (bit 9) in the PHYCR2 Register. Setting this bit will reset all transmit and receive operations, but will not reset the register space. All register configurations will be preserved. Register space will remain available following a soft reset.

5.4.10.4 PTP Reset

The entire PTP function, including the IEEE 1588 clock, associated logic, and PTP register space (with two exceptions), can be reset through the PTP_RESET bit in the PTP_CTL register. The PTP_COC and PTP_CLKSRC registers are not reset in order to preserve the nominal operation of the clock output.

5.5 Programming

5.5.1 Architecture

This section describes the operations within each transceiver module, 100BASE-TX and 10BASE-T. Each operation consists of several functional blocks and is described in the following:

- 100BASE-TX Transmitter
- 100BASE-TX Receiver
- 100BASE-FX Operation
- 10BASE-T Transceiver Module

5.5.1.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125 Mb/s serial data stream. Because the 100BASE-TX TP-PMD is integrated, the differential output pins, PMD Output Pair, can be directly routed to the magnetics.

The block diagram in Figure 5-6 provides an overview of each functional block within the 100BASE-TX transmit section.

The Transmitter section consists of the following functional blocks:

- Code-Group Encoder and Injection block
- Scrambler block (bypass option)
- NRZ to NRZI Encoder block
- Binary to MLT-3 Converter / Common Driver block

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83640 implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3 Standard, Clause 24.

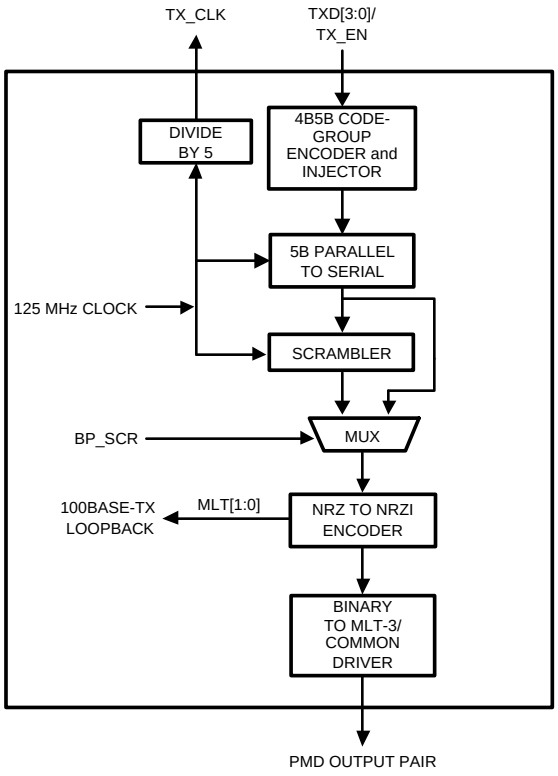


Figure 5-6. 100BASE-TX Transmit Block Diagram

Table 5-8. 4B5B Code-Group Encoding/Decoding

NAME	PCS 5B CODE-GROUP	MII 4B NIBBLE CODE
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000 (1)
J	11000	First Start of Packet - 0101 (1)
K	10001	Second Start of Packet - 0101 (1)
T	01101	First End of Packet - 0000 (1)
R	00111	Second End of Packet - 0000 (1)
INVALID CODES		
V	00000	
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	
V	10000	
V	11001	
Note 1:		

(1) Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

5.5.1.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 5-8 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of Transmit Enable signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of Transmit Enable).

5.5.1.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted pair cable (for 100BASE-TX applications). By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the PMD and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is,, continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB. The DP83640 uses the PHY_ID (pins PHYAD [4:0]) to set a unique seed value.

5.5.1.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI encoded in order to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 Unshielded twisted pair cable. There is no ability to bypass this block within the DP83640. The NRZI data is sent to the 100-Mb Driver. In addition, this module creates an encoded MLT value for use in 100-Mb Internal Loopback.

5.5.1.1.4 Binary to MLT-3 Convertor

The Binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a minimal current MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD Output Pair common driver is slew rate controlled. This should be considered when selecting AC coupling magnetics to ensure TP-PMD Standard compliant transition times (3 ns < Tr < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83640 is capable of sourcing only MLT-3 encoded data. Binary output from the PMD Output Pair is not possible in 100 Mb/s mode.

5.5.1.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125 Mb/s serial data stream to synchronous 4-bit nibble data that is provided to the MII. Because the 100BASE-TX TP-PMD is integrated, the differential input pins, RD±, can be directly routed from the AC coupling magnetics.

See Figure 5-7 for a block diagram of the 100BASE-TX receive function. This provides an overview of each functional block within the 100BASE-TX receive section.

The Receive section consists of the following functional blocks:

- Analog Front End
- Input and BLW Compensation
- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler (bypass option)
- Code Group Alignment
- 4B/5B Decoder
- Link Integrity Monitor
- Bad SSD Detection

5.5.1.2.1 Analog Front End

In addition to the Digital Equalization and Gain Control, the DP83640 includes Analog Equalization and Gain Control in the Analog Front End. The Analog Equalization reduces the amount of Digital Equalization required in the DSP.

5.5.1.2.2 Digital Signal Processor

The Digital Signal Processor includes Base Line Wander Compensation and Adaptive Equalization with Gain Control.

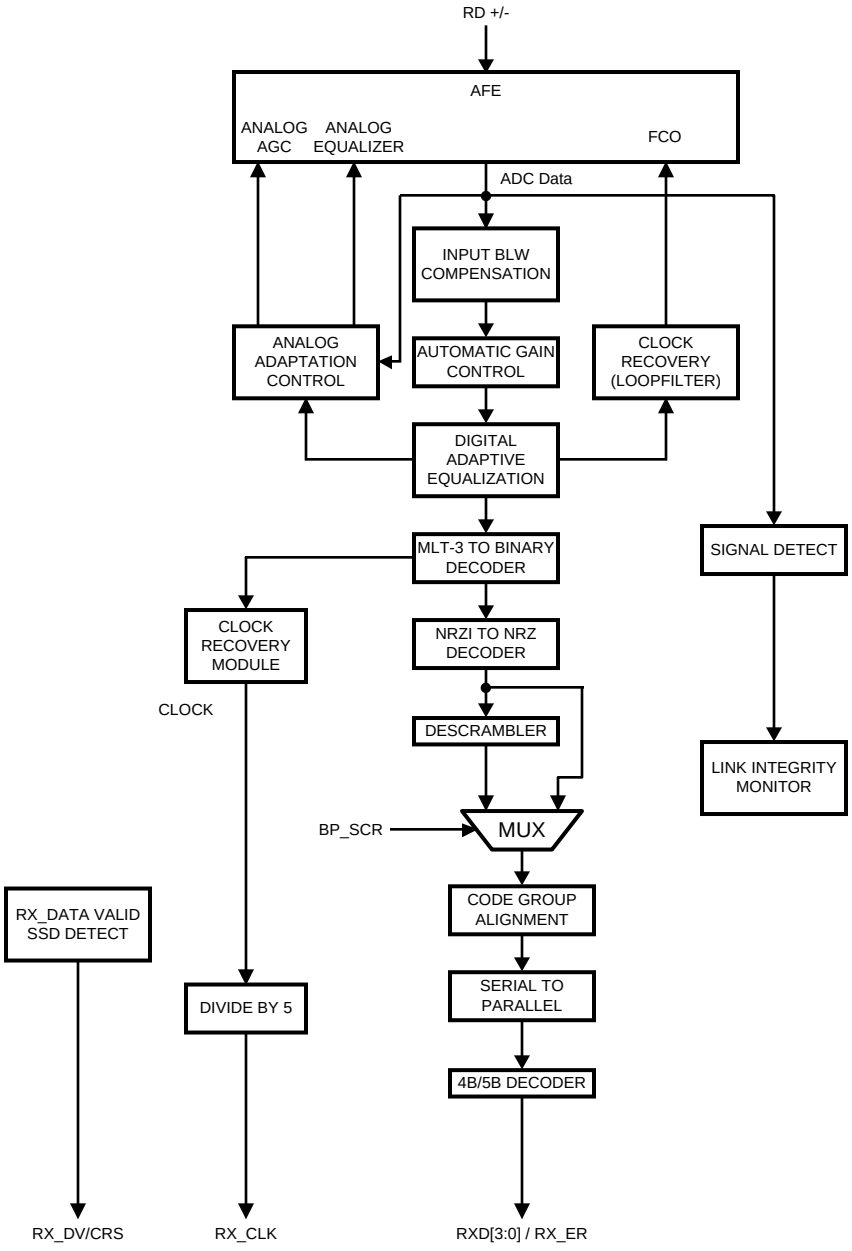


Figure 5-7. 100BASE-TX Receive Block Diagram

5.5.1.2.2.1 Base Line Wander Compensation

The DP83640 is completely ANSI TP-PMD compliant and includes Base Line Wander (BLW) compensation. The BLW compensation block can successfully recover the TP-PMD defined “killer” pattern.

5.5.1.2.2.2 Digital Adaptive Equalization and Gain Control

The DP83640 uses an extremely robust equalization scheme referred as 'Digital Adaptive Equalization.'

The Digital Equalizer removes ISI (inter-symbol interference) from the receive data stream by continuously adapting to provide a filter with the inverse frequency response of the channel. Equalization is combined with an adaptive gain control stage. This enables the receive 'eye pattern' to be opened sufficiently to allow very reliable data recovery.

5.5.1.2.3 Signal Detect

The signal detect function of the DP83640 is incorporated to meet the specifications mandated by the ANSI FDDI TP-PMD Standard as well as the IEEE 802.3 100BASE-TX Standard for both voltage thresholds and timing parameters.

Note that the reception of normal 10BASE-T link pulses and fast link pulses per IEEE 802.3 Auto-Negotiation by the 100BASE-TX receiver do not cause the DP83640 to assert signal detect.

5.5.1.2.4 MLT-3 to Binary Decoder

The DP83640 decodes the MLT-3 information from the Digital Adaptive Equalizer block to binary NRZI data.

5.5.1.2.5 Clock Recovery Module

The Clock Recovery function is implemented as a Phase detector and Loop Filter which accepts data and error from the receive datapath to detect the phase of the recovered data. This phase information is fed into the loop filter to determine an 8-bit signed frequency control. The 8-bit signed frequency control is sent to the FCO in the Analog Front End to derive the receive clock. The extracted and synchronized clock and data are used as required by the synchronous receive operations as generally depicted in Figure 5-7.

5.5.1.2.6 NRZI to NRZ Decoder

In a typical application, the NRZI to NRZ decoder is required in order to present NRZ formatted data to the descrambler (or to the code-group alignment block if the descrambler is bypassed).

5.5.1.2.7 Serial-to-Parallel

The 100BASE-TX receiver includes a Serial-to-Parallel converter which supplies 5-bit wide data symbols to the PCS Rx state machine.

5.5.1.2.8 Descrambler

A serial descrambler is used to de-scramble the received NRZ data. The descrambler has to generate an identical data scrambling sequence (N) in order to recover the original unscrambled data (UD) from the scrambled data (SD) as represented in the equations:

$$SD = (UD \oplus N) \quad (2)$$

$$UD = (SD \oplus N) \quad (3)$$

Synchronization of the descrambler to the original scrambling sequence (N) is achieved based on the knowledge that the incoming scrambled data stream consists of scrambled IDLE data. After the descrambler has recognized 12 consecutive IDLE code-groups, where an unscrambled IDLE code-group in 5B NRZ is equal to five consecutive ones (11111), it will synchronize to the receive data stream and generate unscrambled data in the form of unaligned 5B code-groups.

In order to maintain synchronization, the descrambler must continuously monitor the validity of the unscrambled data that it generates. To ensure this, a line state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler, the hold timer starts a 722-µs countdown. Upon detection of sufficient IDLE code-groups (58 bit times) within the 722-µs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue

indefinitely given a properly operating network connection with good signal integrity. If the line state monitor does not recognize sufficient unscrambled IDLE code-groups within the 722-µs period, the entire descrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization. The DP83604T also provides a bit (DESC_TIME, bit 7) in the PCSR register (0x16) that increases the descrambler timeout from 722 µs to 2 ms to allow reception of packets up to 9 kB in size without losing descrambler lock.

5.5.1.2.9 Code-Group Alignment

The code-group alignment module operates on unaligned 5-bit data from the descrambler (or, if the descrambler is bypassed, directly from the NRZI/NRZ decoder) and converts it into 5B code-group data (5 bits). Code-group alignment occurs after the J/K code-group pair is detected. Once the J/K code-group pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

5.5.1.2.10 4B/5B Decoder

The code-group decoder functions as a look up table that translates incoming 5B code-groups into 4B nibbles. The code-group decoder first detects the J/K code-group pair preceded by IDLE code-groups and replaces the J/K with MAC preamble. Specifically, the J/K 10-bit code-group pair is replaced by the nibble pair (0101 0101). All subsequent 5B code-groups are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the T/R code-group pair denoting the End-of-Stream Delimiter (ESD) or with the reception of a minimum of two IDLE code-groups.

5.5.1.2.11 100BASE-TX Link Integrity Monitor

The 100BASE-TX link monitor ensures that a valid and stable link is established before enabling both the Transmit and Receive PCS layer.

Signal detect must be valid for 395 µs to allow the link monitor to enter the 'Link Up' state and enable the transmit and receive functions.

5.5.1.2.12 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is any transition from consecutive idle code-groups to non-idle code-groups which is not prefixed by the code-group pair /J/K.

If this condition is detected, the DP83640 will assert RX_ER and present RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code-groups are detected. In addition, the False Carrier Sense Counter register (FCSCR) will be incremented by one.

Once at least two IDLE code-groups are detected, RX_ER and CRS become deasserted.

5.5.1.3 100BASE-FX Operation

The DP83640 provides IEEE 802.3 compliant 100BASE-FX operation. Configuration of FX mode is through strap option, or through the register interface.

5.5.1.3.1 100BASE-FX Transmit

In 100BASE-FX mode, the device Transmit pins connect to an industry standard Fiber Transceiver with PECL signaling through a capacitively coupled circuit.

In FX mode, the device bypasses the Scrambler and the MLT3 encoder. This allows for the transmission of serialized 5B4B encoded NRZI data at 125 MHz.

The only added functionality from 100BASE-TX is the support for Far-End Fault data generation.

5.5.1.3.2 100BASE-FX Receive

In 100BASE-FX mode, the device Receive pins connect to an industry standard Fiber Transceiver with PECL signaling.

In FX mode, the device bypasses the MLT3 Decoder and the Descrambler. This allows for the reception of serialized 5B4B encoded NRZI data at 125 MHz.

The only added functionality for 100BASE-FX from 100BASE-TX is the support of Far-End Fault detection.

5.5.1.3.3 Far-End Fault

Because 100BASE-FX does not support Auto-Negotiation, a Far-End Fault facility is included which allows for detection of link failures.

When no signal is being received as determined by the Signal Detect function, the device sends a Far-End Fault indication to the far-end peer. The Far-End Fault indication is comprised of 3 or more repeating cycles, each consisting of 84 one's followed by 1 zero. The pattern is such that it will not satisfy the 100BASE-X carrier sense mechanism, but is easily detected as the Fault indication. The pattern will be transparent to devices that do not support Far-End Fault.

The Far-End Fault detection process continuously monitors the receive data stream for the Far-End Fault indication. When detected, the Link Monitor is forced to deassert Link status. This causes the device to transmit IDLE's on its transmit path.

5.5.1.4 10BASE-T Transceiver Module

The 10BASE-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard. An external filter is not required on the 10BASE-T interface because this is integrated inside the DP83640. This section focuses on the general 10BASE-T system level operation.

5.5.1.4.1 Operational Modes

The DP83640 has two basic 10BASE-T operational modes:

- Half-Duplex mode
- Full-Duplex mode

Half-Duplex Mode

In Half-Duplex mode the DP83640 functions as a standard IEEE 802.3 10BASE-T transceiver supporting the CSMA/CD protocol.

Full-Duplex Mode

In Full-Duplex mode the DP83640 is capable of simultaneously transmitting and receiving without asserting the collision signal. The DP83640's 10 Mb/s ENDEC is designed to encode and decode simultaneously.

5.5.1.4.2 Smart Squelch

The smart squelch is responsible for determining when valid data is present on the differential receive inputs. The DP83640 implements an intelligent receive squelch to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. Smart-squelch operation is independent of the 10BASE-T operational mode.

The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-T standard) to determine the validity of data on the twisted-pair inputs (refer to Figure 5-8).

The signal at the start of a packet is checked by the smart squelch and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150 ns. Finally the signal must again exceed the original squelch level within 150 ns to ensure that the input waveform will not be rejected. This checking procedure results in the loss of typically three preamble bits at the beginning of each packet.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time, the smart-squelch circuitry is reset.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 150 ns, indicating the End of Packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise causing premature End-of-Packet detection.

The receive squelch threshold level can be lowered for use in longer cable or STP applications. This is achieved by configuring the SQUELCH bits (11:9) in the 10BTSCR register (0x1A).

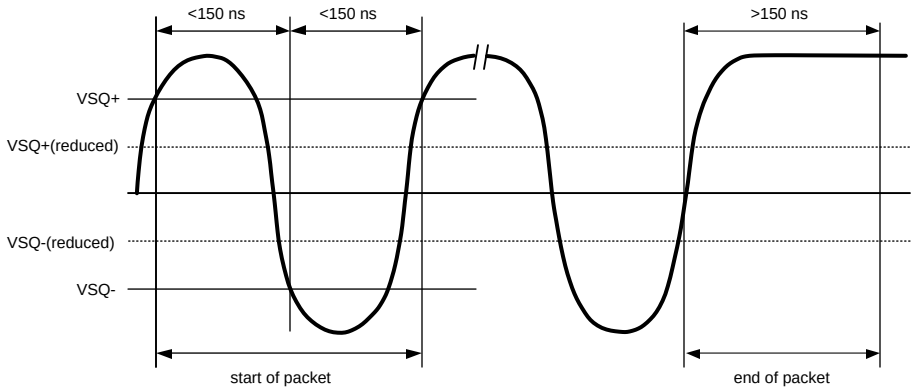


Figure 5-8. 10BASE-T Twisted-Pair Smart-Squelch Operation

5.5.1.4.3 Collision Detection and SQE

When in Half Duplex, a 10BASE-T collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII. Collisions are also reported when a jabber condition is detected.

The COL signal remains set for the duration of the collision. If the ENDEC is receiving when a collision is detected it is reported immediately (through the COL pin).

When heartbeat is enabled, approximately 1 µs after the transmission of each packet, a Signal Quality Error (SQE) signal of approximately 10-bit times is generated to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

The SQE test is inhibited when the PHY is set in full-duplex mode. SQE can also be inhibited by setting the HEARTBEAT_DIS bit (1) in the 10BTSCR register (0x1A).

5.5.1.4.4 Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity once valid data is detected through the squelch function.

For 10 Mb/s Half-Duplex operation, CRS is asserted during either packet transmission or reception.

For 10 Mb/s Full-Duplex operation, CRS is asserted only during receive activity.

CRS is deasserted following an end of packet.

5.5.1.4.5 Normal Link Pulse Detection/Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-T standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data.

Link pulses are used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10BASE-T twisted pair transmitter, receiver and collision detection functions.

When the link integrity function is disabled (FORCE_LINK_10 of the 10BTSCR register), a good link is forced and the 10BASE-T transceiver will operate regardless of the presence of link pulses.

5.5.1.4.6 Jabber Function

The jabber function monitors the DP83640's output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 85 ms.

Once disabled by the Jabber function, the transmitter stays disabled for the entire time that the ENDEC module's internal transmit enable is asserted. This signal has to be deasserted for approximately 500 ms (the “unjab” time) before the Jabber function re-enables the transmit outputs.

The Jabber function is only relevant in 10BASE-T mode.

5.5.1.4.7 Automatic Link Polarity Detection and Correction

The DP83640's 10BASE-T transceiver module incorporates an automatic link polarity detection circuit. When three consecutive inverted link pulses are received, bad polarity is reported. The bad polarity condition is latched in the 10BTSCR register.

The DP83640's 10BASE-T transceiver module corrects for this error internally and will continue to decode received data correctly. This eliminates the need to correct the wiring error immediately.

A polarity reversal can be caused by a wiring error at either end of the cable, usually at the Main Distribution Frame (MDF) or patch panel in the wiring closet.

5.5.1.4.8 Transmit and Receive Filtering

External 10BASE-T filters are not required when using the DP83640, as the required signal conditioning is integrated into the device.

Only isolation transformers and impedance matching resistors are required for the 10BASE-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30 dB.

5.5.1.4.9 Transmitter

The encoder begins operation when the Transmit Enable input (TX_EN) goes high and converts NRZ data to pre-emphasized Manchester data for the transceiver. For the duration of TX_EN, the serialized Transmit Data (TXD) is encoded for the transmit-driver pair (PMD Output Pair). TXD must be valid on the rising edge of Transmit Clock (TX_CLK). Transmission ends when TX_EN deasserts. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

5.5.1.4.10 Receiver

The decoder consists of a differential receiver and a PLL to separate a Manchester encoded data stream into internal clock signals and data. The differential input must be externally terminated with a differential 100-Ω termination network to accommodate UTP cable.

The decoder detects the end of a frame when no additional mid-bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is deasserted. Receive clock stays active for five more bit times after CRS goes low, to verify the receive timings of the controller.

5.6 Memory

5.6.1 Register Block

Table 5-9. Register Map

Offset		Access	Tag	Description
Hex	Decimal			
00h	0	RW	BMCR	Basic Mode Control Register
01h	1	RO	BMSR	Basic Mode Status Register
02h	2	RO	PHYIDR1	PHY Identifier Register #1
03h	3	RO	PHYIDR2	PHY Identifier Register #2
04h	4	RW	ANAR	Auto-Negotiation Advertisement Register
05h	5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register
06h	6	RW	ANER	Auto-Negotiation Expansion Register
07h	7	RW	ANNPTR	Auto-Negotiation Next Page TX Register
08h-0Fh	8-15		RESERVED	RESERVED
10h	16	RO	PHYSTS	PHY Status Register
11h	17	RW	MICR	MII Interrupt Control Register
12h	18	RW	MISR	MII Interrupt Status and Event Control Register
13h	19	RW	PAGESEL	Page Select Register
EXTENDED REGISTERS - PAGE 0				
14h	20	RO	FCSCR	False Carrier Sense Counter Register
15h	21	RO	RECR	Receive Error Counter Register
16h	22	RW	PCSR	PCS Sub-Layer Configuration and Status Register
17h	23	RW	RBR	RMII and Bypass Register
18h	24	RW	LEDCR	LED Direct Control Register
19h	25	RW	PHYCR	PHY Control Register
1Ah	26	RW	10BTSCR	10Base-T Status/Control Register
1Bh	27	RW	CDCTRL1	CD Test Control Register and BIST Extensions Register
1Ch	28	RW	PHYCR2	PHY Control Register 2
1Dh	29	RW	EDCR	Energy Detect Control Register
1Eh	30		RESERVED	RESERVED
1Fh	31	RW	PCFCR	PHY Control Frames Configuration Register
TEST REGISTERS - PAGE 1				
14h - 1Dh	20 - 29		RESERVED	RESERVED
1Eh	30	RW	SD_CNFG	Signal Detect Configuration
1Fh	31		RESERVED	RESERVED
LINK DIAGNOSTICS REGISTERS - PAGE 2				
14h	20	RO	LEN100_DET	100 Mb Length Detect Register
15h	21	RW	FREQ100	100 Mb Frequency Offset Indication Register
16h	22	RW	TDR_CTRL	TDR Control Register
17h	23	RW	TDR_WIN	TDR Window Register
18h	24	RO	TDR_PEAK	TDR Peak Measurement Register
19h	25	RO	TDR_THR	TDR Threshold Measurement Register
1Ah	26	RW	VAR_CTRL	Variance Control Register
1Bh	27	RO	VAR_DAT	Variance Data Register
1Ch	28		RESERVED	RESERVED
1Dh	29	RW	LQMR	Link Quality Monitor Register
1Eh	30	RW	LQDR	Link Quality Data Register
1Fh	31	RW	LQMR2	Link Quality Monitor Register 2

Table 5-9. Register Map (continued)

Offset		Access	Tag	Description
Hex	Decimal			
RESERVED REGISTERS - PAGE 3				
14h - 1Fh	20 - 31		RESERVED	RESERVED
PTP 1588 BASE REGISTERS - PAGE 4				
14h	20	RW	PTP_CTL	PTP Control Register
15h	21	RW	PTP_TDR	PTP Time Data Register
16h	22	RW	PTP_STS	PTP Status Register
17h	23	RW	PTP_TSTS	PTP Trigger Status Register
18h	24	RW	PTP_RATEL	PTP Rate Low Register
19h	25	RW	PTP_RATEH	PTP Rate High Register
1Ah	26	RO	PTP_RDCKSUM	PTP Page 4 Read Checksum
1Bh	27	RO	PTP_WRCKSUM	PTP Page 4 Write Checksum
1Ch	28	RO	PTP_TXTS	PTP Transmit TimeStamp Register
1Dh	29	RO	PTP_RXTS	PTP Receive TimeStamp Register
1Eh	30	RO	PTP_ESTS	PTP Event Status Register
1Fh	31	RO	PTP_EDATA	PTP Event Data Register
PTP 1588 CONFIGURATION REGISTERS - PAGE 5				
14h	20	RW	PTP_TRIG	PTP Trigger Configuration Register
15h	21	RW	PTP_EVNT	PTP Event Configuration Register
16h	22	RW	PTP_TXCFG0	PTP Transmit Configuration Register 0
17h	23	RW	PTP_TXCFG1	PTP Transmit Configuration Register 1
18h	24	RW	PSF_CFG0	PHY Status Frames Configuration Register 0
19h	25	RW	PTP_RXCFG0	PTP Receive Configuration Register 0
1Ah	26	RW	PTP_RXCFG1	PTP Receive Configuration Register 1
1Bh	27	RW	PTP_RXCFG2	PTP Receive Configuration Register 2
1Ch	28	RW	PTP_RXCFG3	PTP Receive Configuration Register 3
1Dh	29	RW	PTP_RXCFG4	PTP Receive Configuration Register 4
1Eh	30	RW	PTP_TRDL	PTP Temporary Rate Duration Low Register
1Fh	31	RW	PTP_TRDH	PTP Temporary Rate Duration High Register
PTP 1588 CONFIGURATION REGISTERS - PAGE 6				
14h	20	RW	PTP_COC	PTP Clock Output Control Register
15h	21	RW	PSF_CFG1	PHY Status Frames Configuration Register 1
16h	22	RW	PSF_CFG2	PHY Status Frames Configuration Register 2
17h	23	RW	PSF_CFG3	PHY Status Frames Configuration Register 3
18h	24	RW	PSF_CFG4	PHY Status Frames Configuration Register 4
19h	25	RW	PTP_SFDCFG	PTP SFD Configuration Register
1Ah	26	RW	PTP_INTCTL	PTP Interrupt Control Register
1Bh	27	RW	PTP_CLKSRC	PTP Clock Source Register
1Ch	28	RW	PTP_ETR	PTP Ethernet Type Register
1Dh	29	RW	PTP_OFF	PTP Offset Register
1Eh	30	RO	PTP_GPIOMON	PTP GPIO Monitor Register
1Fh	31	RW	PTP_RXHASH	PTP Receive Hash Register

Table 5-10. Register Table

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Basic Mode Control Register	00h	BMCR	Reset	Loopback	Speed Selection	Auto-Neg Enable	Power Down	Isolate	Restart Auto-Neg	Duplex Mode	Collision Test	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Basic Mode Status Register	01h	BMSR	100Base-T4	100Base-TX FDX	100Base-TX HDX	10Base-T FDX	10Base-T HDX	Reserved	Reserved	Reserved	Unidirectional Ability	MF Preamble Suppress	Auto-Neg Complete	Remote Fault	Auto-Neg Ability	Link Status	Jabber Detect	Extended Capability
PHY Identifier Register #1	02h	PHYIDR1	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB
PHY Identifier Register #2	03h	PHYIDR2	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	VNDR_MDL	VNDR_MDL	VNDR_MDL	VNDR_MDL	VNDR_MDL	VNDR_MDL	MDL_REV	MDL_REV	MDL_REV	MDL_REV
Auto-Negotiation Advertisement Register	04h	ANAR	Next Page Ind	Reserved	Remote Fault	Reserved	ASM_DIR	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Link Partner Ability Register (Base Page)	05h	ANLPAR	Next Page Ind	ACK	Remote Fault	Reserved	ASM_DIR	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Link Partner Ability Register Next Page	05h	ANLPARNP	Next Page Ind	ACK	Message Page	ACK2	Toggle	Code	Code	Code	Code	Code	Code	Code	Code	Code	Code	Code
Auto-Negotiation Expansion Register	06h	ANER	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PDF	LP_NP_ABLE	NP_ABLE	PAGE_RX	LP_AN_ABLE
Auto-Negotiation Next Page TX Register	07h	ANNPTR	Next Page Ind	Reserved	Message Page	ACK2	TOG_TX	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE
RESERVED	08-0fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
PHY Status Register	10h	PHYSTS	Reserved	MDIX mode	Rx Err Latch	Polarity Status	False Carrier Sense	Signal Detect	Descrambler Lock	Page Receive	MII Interrupt	Remote Fault	Jabber Detect	Auto-Neg Complete	Loopback Status	Duplex Status	Speed Status	Link Status
MII Interrupt Control Register	11h	MICR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PTP_INT_SEL	TINT	INTEN	INT_OE

Table 5-10. Register Table (continued)

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MII Interrupt Status and Misc. Control Register	12h	MISR	LQ_INT	ED_INT	LINK_INT	SPD_INT or SPD_DUP_INT	DUP_INT or PTP_INT	ANC_INT	FHF_INT or CTR_INT	RHF_INT or PCF_INT	LQ_INT_EN	ED_INT_EN	LINK_INT_EN	SPED_INT_EN	DUP_INT_EN	ANC_INT_EN	FHF_INT_EN or CTR_INT_EN	RHF_INT_EN or PCF_INT_EN
Page Select Register	13h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Page_Sel Bit	Page_Sel Bit	Page_Sel Bit
EXTENDED REGISTERS - PAGE 0																		
False Carrier Sense Counter Register	14h	FCSCR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT
Receive Error Counter Register	15h	RECR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT
PCS Sub-Layer Configuration and Status Register	16h	PCSR	Reserved	Reserved	Reserved	Reserved	FREE_CLK	TQ_EN	SD_FORCE_PMA	SD_OPTION	DESC_TIME	FX_EN	FORCE_100_OK	Reserved	FEFI_EN	NRZI_BYPASS	SCRAM_BYPASS	DE SCRAM_BYPASS
RMII and Bypass Register	17h	RBR	Reserved	RMII_MASTER	DIS_TX_OPT	RX_PORT	RX_PORT	TX_SOURCE	TX_SOURCE	PMD_LOOP	SCMII_RX	SCMII_TX	RMII_MODE	RMII_REV1_0	RX_OVF_STS	RX_UNF_STS	ELAST_BUF	ELAST_BUF
LED Direct Control Register	18h	LEDCR	Reserved	Reserved	Reserved	Reserved	DIS_SPDLED	DIS_LNKLED	DIS_ACTLED	LEDACT_RX	BLINK_FREQ	BLINK_FREQ	DRV_SPDLED	DRV_LNKLED	DRV_ACTLED	SPDLED	LNKLED	ACTLED
PHY Control Register	19h	PHYCR	MDIX_EN	FORCE_MDIX	PAUSE_RX	PAUSE_TX	BIST_FE	PSR_15	BIST_STATUS	BIST_START	BP_STRETCH	LED_CNFG[1]	LED_CNFG[0]	PHY ADDR	PHY ADDR	PHY ADDR	PHY ADDR	PHY ADDR
10Base-T Status/Control Register	1Ah	10BTSCR	Reserved	Reserved	Reserved	Reserved	SQUELCH	SQUELCH	SQUELCH	LOOPBACK_10_DIS	LP_DIS	FORCE_LINK_10	FORCE_POL COR	POLARITY	AUTOPOL_DIS	10BT_SCALE_MSB	HEARTBEAT_DIS	JABBER_DIS
CD Test Control and BIST Extensions Register	1Bh	CDCTRL1	BIST_ERROR_COUNT	BIST_ERROR_COUNT	BIST_ERROR_COUNT	BIST_ERROR_COUNT	BIST_ERROR_COUNT	BIST_ERROR_COUNT	BIST_ERROR_COUNT	BIST_ERROR_COUNT	Reserved	MII_CLOCK_EN	BIST_CONT	CDPATTEN_10	MDIO_PULL_EN	PATT_GAP_10M	CDPATTSEL	CDPATTSEL
PHY Control Register 2	1Ch	PHYCR2	Reserved	Reserved	SYNC_ENET_EN	CLK_OUT RXCLK	BC_WRITE	PHYTER_COMP	SOFT_RESET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CLK_OUT_DIS	Reserved
Energy Detect Control Register	1Dh	EDCR	ED_EN	ED_AUTO_UP	ED_AUTO_DOWN	ED_MAN	ED_BURST_DIS	ED_PWR_STATE	ED_ERR_MET	ED_DATA_MET	ED_ERR_COUNT	ED_ERR_COUNT	ED_ERR_COUNT	ED_ERR_COUNT	ED_DATA_COUNT	ED_DATA_COUNT	ED_DATA_COUNT	ED_DATA_COUNT
RESERVED	1Eh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 5-10. Register Table (continued)

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PHY Control Frames Configuration Register	1Fh	PCFCR	PCF_STS_ERR	PCF_STS_OK	Reserved	Reserved	Reserved	Reserved	Reserved	PCF_DA_SEL	PCF_INT_CTL	PCF_INT_CTL	PCF_BC_DIS	PCF_BUF	PCF_BUF	PCF_BUF	PCF_BUF	PCF_EN
TEST REGISTERS - PAGE 1																		
RESERVED	14h-1Dh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Signal Detect Configuration Register	1Eh	SD_CNFG	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SD_Time	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
RESERVED	1Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
LINK DIAGNOSTICS REGISTERS - PAGE 2																		
100 Mb Length Detect Register	14h	LEN100_DET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN
100 Mb Frequency Offset Indication Register	15h	FREQ100	SAMPLE_FREQ	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SEL_FC	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET
TDR Control Register	16h	TDR_CTRL	TDR_ENABLE	TDR_100Mb	TX_CHANNEL	RX_CHANNEL	SEND_TDR	TDR_WIDTH	TDR_WIDTH	TDR_WIDTH	TDR_MIN_MODE	Reserved	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD
TDR Window Register	17h	TDR_WIN	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP
TDR Peak Measurement Register	18h	TDR_PEAK	Reserved	Reserved	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME
TDR Threshold Measurement Register	19h	TDR_THR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TDR_THR_MET	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME
Variance Control Register	1Ah	VAR_CTRL	VAR_RDY	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LOAD_VAR_HI	LOAD_VAR_LO	VAR_FREEZE	VAR_TIMER	VAR_TIMER	VAR_ENABLE
Variance Data Register	1Bh	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATA
Reserved	1Ch	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Link Quality Monitor Register	1Dh	LQMR	LQM_ENABLE	RESTART_ON_FC	RESTART_ON_FREQ	RESTART_ON_DBLW	RESTART_ON_DAGC	RESTART_ON_C1	FC_HI_WARN	FC_LO_WARN	FREQ_HI_WARN	FREQ_LO_WARN	DBLW_HI_WARN	DBLW_LO_WARN	DAGC_HI_WARN	DAGC_LO_WARN	C1_HI_WARN	C1_LO_WARN
Link Quality Data Register	1Eh	LQDR	Reserved	Reserved	SAMPLE_PARAM	WRITE_LQ_THR	LQ_PARAM_SEL	LQ_PARAM_SEL	LQ_PARAM_SEL	LQ_THR_SEL	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA

Table 5-10. Register Table (continued)

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Link Quality Monitor Register 2	1Fh	LQMR2	Reserved	Reserved	Reserved	Reserved	Reserved	RESTART_ON_VAR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VAR_HI_WARN	Reserved
RESERVED REGISTERS - PAGE 3																		
RESERVED	14h-1Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
PTP 1588 BASE REGISTERS - PAGE 4																		
PTP Control Register	14h	PTP_CTL	Reserved	Reserved	Reserved	TRIG_SEL	TRIG_SEL	TRIG_SEL	TRIG_DIS	TRIG_EN	TRIG_READ	TRIG_LOAD	PTP_RD_CLK	PTP_LOAD_CLK	PTP_STEP_CLK	PTP_ENABLE	PTP_DISABLE	PTP_RESET
PTP Time Data Register	15h	PTP_TDR	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA	TIME_DATA
PTP Status Register	16h	PTP_STS	Reserved	Reserved	Reserved	Reserved	TXTS_RDY	RXTS_RDY	TRIG_DONE	EVENT_RDY	Reserved	Reserved	Reserved	Reserved	TXTS_IE	RXTS_IE	TRIG_IE	EVENT_IE
PTP Trigger Status Register	17h	PTP_TSTS	TRIG7_ERROR	TRIG7_ACTIVE	TRIG6_ERROR	TRIG6_ACTIVE	TRIG5_ERROR	TRIG5_ACTIVE	TRIG4_ERROR	TRIG4_ACTIVE	TRIG3_ERROR	TRIG3_ACTIVE	TRIG2_ERROR	TRIG2_ACTIVE	TRIG1_ERROR	TRIG1_ACTIVE	TRIG0_ERROR	TRIG0_ACTIVE
PTP Rate Low Register	18h	PTP_RATEL	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo	PTP_Rate_Lo
PTP Rate High Register	19h	PTP_RATEH	PTP_RATE_DIR	PTP_TMP_RATE	Reserved	Reserved	Reserved	Reserved	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi	PTP_Rate_Hi
PTP Page 4 Read Checksum	1Ah	PTP_RDCKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM	RD_CKSUM
PTP Page 4 Write Checksum	1Bh	PTP_WRCKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM	WR_CKSUM
PTP Transmit TimeStamp Register	1Ch	PTP_TXTS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS	PTP_TX_TS
PTP Receive TimeStamp Register	1Dh	PTP_RXTS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS	PTP_RX_TS
PTP Event Status Register	1Eh	PTP_ESTS	Reserved	Reserved	Reserved	Reserved	Reserved	EVNTS_MISSED	EVNTS_MISSED	EVNTS_MISSED	EVNT_TS_LEN	EVNT_TS_LEN	EVNT_RF	EVNT_NUM	EVNT_NUM	EVNT_NUM	MULT_EVNT	EVENT_DET
PTP Event Data Register Status	1Fh	PTP_EDATA	E7_RISE	E7_DET	E6_RISE	E6_DET	E5_RISE	E5_DET	E4_RISE	E4_DET	E3_RISE	E3_DET	E2_RISE	E2_DET	E1_RISE	E1_DET	E0_RISE	E0_DET
PTP Event Data Register Timestamp	1Fh	PTP_EDATA	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS	PTP_EVNT_TS
PTP 1588 CONFIGURATION REGISTERS - PAGE 5																		
PTP Trigger Configuration Register	14h	PTP_TRIG	TRIG_PULSE	TRIG_PER	TRIG_IF_LATE	TRIG_NOTIFY	TRIG_GPIO	TRIG_GPIO	TRIG_GPIO	TRIG_GPIO	TRIG_TOGGLE	Reserved	Reserved	Reserved	TRIG_CSEL	TRIG_CSEL	TRIG_CSEL	TRIG_WR

Table 5-10. Register Table (continued)

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTP Event Configuration Register	15h	PTP_EVNT	Reserved	EVNT_RISE	EVNT_FALL	Reserved	EVNT_GPIO	EVNT_GPIO	EVNT_GPIO	EVNT_GPIO	Reserved	Reserved	Reserved	Reserved	EVNT_SEL	EVNT_SEL	EVNT_SEL	EVNT_WR
PTP Transmit Configuration Register 0	16h	PTP_TXCFG0	SYNC_1STEP	Reserved	DR_INSERT	Reserved	RESERVED_1	CRC_1STEP	CHK_1STEP	IP1588_EN	TX_L2_EN	TX_IPV6_EN	TX_IPV4_EN	TX_PTP_VER	TX_PTP_VER	TX_PTP_VER	TX_PTP_VER	TX_TS_EN
PTP Transmit Configuration Register 1	17h	PTP_TXCFG1	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA
PHY Status Frame Configuration Register 0	18h	PSF_CFG0	Reserved	Reserved	Reserved	MAC_SRC_ADD	MAC_SRC_ADD	MIN_PRE	MIN_PRE	MIN_PRE	PSF_ENDIAN	PSF_IPV4	PSF_PCF_RD	PSF_ERR_EN	PSF_TXTS_EN	PSF_RXTS_EN	PSF_TRIG_EN	PSF_EVNT_EN
PTP Receive Configuration Register 0	19h	PTP_RXCFG0	DOMAIN_EN	Reserved	USER_IP_SEL	USER_IP_EN	RX_SLAVE	IP1588_EN	IP1588_EN	IP1588_EN	RX_L2_EN	RX_IPV6_EN	RX_IPV4_EN	RX_PTP_VER	RX_PTP_VER	RX_PTP_VER	RX_PTP_VER	RX_TS_EN
PTP Receive Configuration Register 1	1Ah	PTP_RXCFG1	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_MASK	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA	BYTE0_DATA
PTP Receive Configuration Register 2	1Bh	PTP_RXCFG2	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA	IP_ADDR_DATA
PTP Receive Configuration Register 3	1Ch	PTP_RXCFG3	TS_MIN_IFG	TS_MIN_IFG	TS_MIN_IFG	TS_MIN_IFG	ACC_UDP	ACC_CRC	TS_APPEND	TS_INSERT	PTP_DOMAIN	PTP_DOMAIN	PTP_DOMAIN	PTP_DOMAIN	PTP_DOMAIN	PTP_DOMAIN	PTP_DOMAIN	PTP_DOMAIN
PTP Receive Configuration Register 4	1Dh	PTP_RXCFG4	IPV4_UDP_MOD	TS_SEC_EN	TS_SEC_LEN	TS_SEC_LEN	RXTS_NS_OFF	RXTS_NS_OFF	RXTS_NS_OFF	RXTS_NS_OFF	RXTS_NS_OFF	RXTS_NS_OFF	RXTS_SEC_OFF	RXTS_SEC_OFF	RXTS_SEC_OFF	RXTS_SEC_OFF	RXTS_SEC_OFF	RXTS_SEC_OFF
PTP Temporary Rate Duration Low Register	1Eh	PTP_TRDL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL	PTP_TR_DURL
PTP Temporary Rate Duration High Register	1Fh	PTP_TRDH	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH	PTP_TR_DURH
PTP 1588 CONFIGURATION REGISTERS - PAGE 6																		
PTP Clock Output Control Register	14h	PTP_COC	PTP_CLKOUTEN	PTP_CLKOUTSEL	PTP_CLKOUTSPEEDSEL	Reserved	Reserved	Reserved	Reserved	Reserved	PTP_CLKDIV	PTP_CLKDIV	PTP_CLKDIV	PTP_CLKDIV	PTP_CLKDIV	PTP_CLKDIV	PTP_CLKDIV	PTP_CLKDIV
PHY Status Frame Configuration Register 1	15h	PSF_CFG1	PTPRESERVED	PTPRESERVED	PTPRESERVED	PTPRESERVED	VERSIONPTP	VERSIONPTP	VERSIONPTP	VERSIONPTP	TRANSPORTSPECIFIC	TRANSPORTSPECIFIC	TRANSPORTSPECIFIC	TRANSPORTSPECIFIC	MESSAGETYPE	MESSAGETYPE	MESSAGETYPE	MESSAGETYPE

Table 5-10. Register Table (continued)

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status Frame Configuration Register 2	16h	PSF_CFG2	IP_SA_BYTE1	IP_SA_BYTE1	IP_SA_BYTE1	IP_SA_BYTE1	IP_SA_BYTE1	IP_SA_BYTE1	IP_SA_BYTE1	IP_SA_BYTE1	IP_SA_BYTE0	IP_SA_BYTE0	IP_SA_BYTE0	IP_SA_BYTE0	IP_SA_BYTE0	IP_SA_BYTE0	IP_SA_BYTE0	IP_SA_BYTE0
Status Frame Configuration Register 3	17h	PSF_CFG3	IP_SA_BYTE3	IP_SA_BYTE3	IP_SA_BYTE3	IP_SA_BYTE3	IP_SA_BYTE3	IP_SA_BYTE3	IP_SA_BYTE3	IP_SA_BYTE3	IP_SA_BYTE2	IP_SA_BYTE2	IP_SA_BYTE2	IP_SA_BYTE2	IP_SA_BYTE2	IP_SA_BYTE2	IP_SA_BYTE2	IP_SA_BYTE2
Status Frame Configuration Register 4	18h	PSF_CFG4	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM	IP_CHKSUM
PTP SFD Congiguration Register	19h	PTP_SFDCFG	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TX_SFD_GPIO	TX_SFD_GPIO	TX_SFD_GPIO	TX_SFD_GPIO	RX_SFD_GPIO	RX_SFD_GPIO	RX_SFD_GPIO	RX_SFD_GPIO
PTP Interrupt Control Register	1Ah	PTP_INTCTL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PTP_INT_GPIO	PTP_INT_GPIO	PTP_INT_GPIO	PTP_INT_GPIO
PTP Clock Source Register	1Bh	PTP_CLKSRC	CLK_SRC	CLK_SRC	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CLK_SRC_PER	CLK_SRC_PER	CLK_SRC_PER	CLK_SRC_PER	CLK_SRC_PER	CLK_SRC_PER	CLK_SRC_PER
PTP Ethernet Type Register	1Ch	PTP_ETR	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE	PTP_ETYPE
PTP Offset Register	1Dh	PTP_OFF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PTP_OFFSET	PTP_OFFSET	PTP_OFFSET	PTP_OFFSET	PTP_OFFSET	PTP_OFFSET	PTP_OFFSET	PTP_OFFSET
PTP GPIO Monitor Register	1Eh	PTP_GPIOMON	Reserved	Reserved	Reserved	Reserved	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN	PTP_GPIO_IN
PTP Receive Hash Register	1Fh	PTP_RXHASH	Reserved	Reserved	Reserved	RX_HASH_EN	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH	PTP_RX_HASH

5.6.1.1 Register Definition

In the register definitions under the 'Default' heading, the following definitions hold true:

- **RW** = **R**ead **W**rite access
- **SC** = Register sets on event occurrence and **S**elf-**C**lears when event ends
- **RW/SC** = **R**ead**W**rite access/**S**elf **C**learing bit
- **RO** = **R**ead **O**nly access
- **COR** = **C**lear **O**n **R**ead
- **RO/COR** = **R**ead **O**nly, **C**lear **O**n **R**ead
- **RO/P** = **R**ead **O**nly, **P**ermanently set to a default value
- **LL** = **L**atched **L**ow and held until read, based upon the occurrence of the corresponding event
- **LH** = **L**atched **H**igh and held until read, based upon the occurrence of the corresponding event

5.6.1.1.1 Basic Mode Control Register (BMCR)

Table 5-11. Basic Mode Control Register (BMCR), Address 0x00

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESET	0, RW/SC	**Reset:** 1 = Initiate software Reset / Reset in Process. 0 = Normal operation. This bit, which is self-clearing, returns a value of one until the reset process is complete. The configuration is re-strapped.
14	LOOPBACK	0, RW	**Loopback:** 1 = Loopback enabled. 0 = Normal operation. The loopback function enables MII transmit data to be routed to the MII receive data path. Setting this bit may cause the descrambler to lose synchronization and produce a 500 µs "dead time" before any valid data will appear at the MII receive outputs.
13	SPEED SELECTION	Strap, RW	**Speed Select:** When auto-negotiation is disabled writing to this bit allows the port speed to be selected. 1 = 100 Mb/s. 0 = 10 Mb/s.
12	AUTO-NEGOTIATION ENABLE	Strap, RW	**Auto-Negotiation Enable:** Strap controls initial value at reset. If FX is enabled (FX_EN = 1), then this bit will be reset to 0. 1 = Auto-Negotiation Enabled - bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled - bits 8 and 13 determine the port speed and duplex mode.
11	POWER DOWN	0, RW	**Power Down:** 1 = Power down. 0 = Normal operation. Setting this bit powers down the PHY. Only the register block is enabled during a power-down condition. This bit is ORd with the input from the PWRDOWN_INT pin. When the active low PWRDOWN_INT pin is asserted, this bit will be set.
10	ISOLATE	0, RW	**Isolate:** 1 = Isolates the Port from the MII with the exception of the serial management. 0 = Normal operation.

Table 5-11. Basic Mode Control Register (BMCR), Address 0x00 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
9	RESTART AUTO-NEGOTIATION	0, RW/SC	**Restart Auto-Negotiation:** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation.
8	DUPLEX MODE	Strap, RW	**Duplex Mode:** When auto-negotiation is disabled writing to this bit allows the port Duplex capability to be selected. 1 = Full-Duplex operation. 0 = Half-Duplex operation.
7	COLLISION TEST	0, RW	**Collision Test:** 1 = Collision test enabled. 0 = Normal operation. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN within 512-bit times. The COL signal will be deasserted within 4-bit times in response to the deassertion of TX_EN.
6	RESERVED	0, RO	**RESERVED:** Write ignored, read as 0.
5	UNIDIRECTIONAL ENABLE	0, RW	**Unidirectional Enable:** 1 = Allow 100-Mb transmit activity independent of link status. 0 = Require link up for 100 Mb/s transmit activity. This bit has no effect in 10 Mb/s mode..
4:0	RESERVED	0 0000, RO	**RESERVED:** Write ignored, read as 0.

5.6.1.1.2 Basic Mode Status Register (BMSR)

Table 5-12. Basic Mode Status Register (BMSR), Address 0x01

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BASE-T4	0, RO/P	**100BASE-T4 Capable:** 0 = Device not able to perform 100BASE-T4 mode.
14	100BASE-TX FULL DUPLEX	1, RO/P	**100BASE-TX Full Duplex Capable:** 1 = Device able to perform 100BASE-TX in full-duplex mode.
13	100BASE-TX HALF DUPLEX	1, RO/P	**100BASE-TX Half Duplex Capable:** 1 = Device able to perform 100BASE-TX in half-duplex mode.
12	10BASE-T FULL DUPLEX	1, RO/P	**10BASE-T Full Duplex Capable:** 1 = Device able to perform 10BASE-T in full-duplex mode.
11	10BASE-T HALF DUPLEX	1, RO/P	**10BASE-T Half Duplex Capable:** 1 = Device able to perform 10BASE-T in half-duplex mode.
10:8	RESERVED	000, RO	**RESERVED**: Write as 0, read as 0.
7	UNIDIRECTIONAL ABILITY	1, RO/P	**Unidirectional Ability:** 1 = Device able to transmit in 100 Mb/s mode independent of link status.
6	MF PREAMBLE SUPPRESSION	1, RO/P	**Preamble Suppression Capable:** 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0 = Normal management operation.
5	AUTO-NEGOTIATION COMPLETE	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process complete. 0 = Auto-Negotiation process not complete.

Table 5-12. Basic Mode Status Register (BMSR), Address 0x01 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
4	REMOTE FAULT	0, RO/LH	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	AUTO-NEGOTIATION ABILITY	1, RO/P	**Auto Negotiation Ability:** 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	LINK STATUS	0, RO/LL	**Link Status:** 1 = Valid link established (for either 10- or 100 Mb/s operation). 0 = Link not established. The criteria for link validity is implementation specific. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read through the management interface.
1	JABBER DETECT	0, RO/LH	**Jabber Detect:** This bit only has meaning in 10 Mb/s mode. 1 = Jabber condition detected. 0 = No Jabber. This bit is implemented with a latching function, such that the occurrence of a jabber condition causes it to set until it is cleared by a read to this register by the management interface or by a reset.
0	EXTENDED CAPABILITY	1, RO/P	**Extended Capability:** 1 = Extended register capabilities. 0 = Basic register set capabilities only.

The PHY Identifier Registers #1 and #2 together form a unique identifier for the DP83640. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. Texas Instruments's IEEE assigned OUI is 080017h.

5.6.1.1.3 PHY Identifier Register #1 (PHYIDR1)

Table 5-13. PHY Identifier Register #1 (PHYIDR1), Address 0x02

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	OUI_MSB	0010 0000 0000 0000, RO/P	**OUI Most Significant Bits:** Bits 3 to 18 of the OUI (080017h) are stored in bits 15 to 0 of this register. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

5.6.1.1.4 PHY Identifier Register #2 (PHYIDR2)

Table 5-14. PHY Identifier Register #2 (PHYIDR2), Address 0x03

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	0101 11, RO/P	**OUI Least Significant Bits:** Bits 19 to 24 of the OUI (080017h) are mapped from bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	00 1110, RO/P	**Vendor Model Number:** The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	0001, RO/P	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

5.6.1.1.5 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation. Any writes to this register prior to completion of Auto-Negotiation (as indicated in the Basic Mode Status Register (address 01h) Auto-Negotiation Complete bit, BMSR[5]) should be followed by a renegotiation. This will ensure that the new values are properly used in the Auto-Negotiation.

Table 5-15. Auto-Negotiation Advertisement Register (ANAR), Address 0x04

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = Next Page Transfer not desired. 1 = Next Page Transfer desired.
14	RESERVED	0, RO/P	**RESERVED by IEEE**: Writes ignored, Read as 0.
13	RF	0, RW	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault. 0 = No Remote Fault detected.
12	RESERVED	0, RW	**RESERVED for Future IEEE use:** Write as 0, Read as 0
11	ASM_DIR	0, RW	**Asymmetric PAUSE Support for Full-Duplex Links:** The ASM_DIR bit indicates that asymmetric PAUSE is supported. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3. 0 = No MAC-based full-duplex flow control.
10	PAUSE	0, RW	**PAUSE Support for Full-Duplex Links:** The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3. 0 = No MAC-based full-duplex flow control.
9	T4	0, RO/P	**100BASE-T4 Support:** 1 = 100BASE-T4 is supported by the local device. 0 = 100BASE-T4 not supported.
8	TX_FD	Strap, RW	**100BASE-TX Full-Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the local device. 0 = 100BASE-TX Full Duplex not supported.
7	TX	Strap, RW	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the local device. 0 = 100BASE-TX not supported.
6	10_FD	Strap, RW	**10BASE-T Full-Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the local device. 0 = 10BASE-T Full Duplex not supported.
5	10	Strap, RW	**10BASE-T Support:** 1 = 10BASE-T is supported by the local device. 0 = 10BASE-T not supported.
4:0	SELECTOR	0 0001, RW	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3.

5.6.1.1.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page)

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. The content changes after the successful auto-negotiation if Next-pages are supported.

Table 5-16. Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page), Address 0x05

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 0 = Link Partner does not desire Next Page Transfer. 1 = Link Partner desires Next Page Transfer.
14	ACK	0, RO	**Acknowledge**: 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control this bit based on the incoming FLP bursts.
13	RF	0, RO	**Remote Fault:** 1 = Remote Fault indicated by Link Partner. 0 = No Remote Fault indicated by Link Partner.
12	RESERVED	0, RO	**RESERVED for Future IEEE use:** Write as 0, read as 0.
11	ASM_DIR	0, RO	**ASYMMETRIC PAUSE:** 1 = Asymmetric pause is supported by the Link Partner. 0 = Asymmetric pause is not supported by the Link Partner.
10	PAUSE	0, RO	**PAUSE:** 1 = Pause function is supported by the Link Partner. 0 = Pause function is not supported by the Link Partner.
9	T4	0, RO	**100BASE-T4 Support:** 1 = 100BASE-T4 is supported by the Link Partner. 0 = 100BASE-T4 not supported by the Link Partner.
8	TX_FD	0, RO	**100BASE-TX Full-Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the Link Partner. 0 = 100BASE-TX Full Duplex not supported by the Link Partner.
7	TX	0, RO	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the Link Partner. 0 = 100BASE-TX not supported by the Link Partner.
6	10_FD	0, RO	**10BASE-T Full-Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the Link Partner. 0 = 10BASE-T Full Duplex not supported by the Link Partner.
5	10	0, RO	**10BASE-T Support:** 1 = 10BASE-T is supported by the Link Partner. 0 = 10BASE-T not supported by the Link Partner.
4:0	SELECTOR	0 0000, RO	**Protocol Selection Bits:** Link Partner's binary encoded protocol selector.

5.6.1.1.7 Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page)

Table 5-17. Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page), Address 0x05

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 1 = Link Partner desires Next Page Transfer. 0 = Link Partner does not desire Next Page Transfer.
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control this bit based on the incoming FLP bursts. Software should not attempt to write to this bit.
13	MP	0, RO	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RO	**Acknowledge 2:** 1 = Link Partner does have the ability to comply to next page message. 0 = Link Partner does not have the ability to comply to next page message.
11	TOGGLE	0, RO	**Toggle:** 1 = Previous value of the transmitted Link Code word equaled 0. 0 = Previous value of the transmitted Link Code word equaled 1.
10:0	CODE	000 0000 0000, RO	**Code:** This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a Message Page, as defined in IEEE 802.3 Annex 28C of Clause 28. Otherwise, the code shall be interpreted as an Unformatted Page, and the interpretation is application specific.

5.6.1.1.8 Auto-Negotiate Expansion Register (ANER)

This register contains additional Local Device and Link Partner status information.

Table 5-18. Auto-Negotiate Expansion Register (ANER), Address 0x06

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0000 0000 000, RO	**RESERVED**: Writes ignored, Read as 0.
4	PDF	0, RO	**Parallel Detection Fault:** 1 = A fault has been detected through the Parallel Detection function. 0 = A fault has not been detected.
3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able:** 1 = Link Partner does support Next Page. 0 = Link Partner does not support Next Page.
2	NP_ABLE	1, RO/P	**Next Page Able:** 1 = Indicates local device is able to send additional Next Pages.
1	PAGE_RX	0, RO/COR	**Link Code Word Page Received:** 1 = Link Code Word has been received, cleared on a read. 0 = Link Code Word has not been received.
0	LP_AN_ABLE	0, RO	**Link Partner Auto-Negotiation Able:** 1 = Indicates that the Link Partner supports Auto-Negotiation. 0 = Indicates that the Link Partner does not support Auto-Negotiation.

5.6.1.1.9 Auto-Negotiation Next Page Transmit Register (ANNPTR)

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 5-19. Auto-Negotiation Next Page Transmit Register (ANNPTR), Address 0x07

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = No other Next Page Transfer desired. 1 = Another Next Page desired.
14	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
13	MP	1, RW	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RW	**Acknowledge2:** 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was 0. 0 = Value of toggle bit in previously transmitted Link Code Word was 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	000 0000 0001, RW	**Code:** This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in Annex 28C of IEEE 802.3. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3.

5.6.1.1.10 PHY Status Register (PHYSTS)

This register provides a single location within the register set for quick access to commonly accessed information.

Table 5-20. PHY Status Register (PHYSTS), Address 0x10

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Write ignored, read as 0.
14	MDIX MODE	0, RO	**MDIX mode as reported by the Auto-Negotiation logic:** This bit will be affected by the settings of the MDIX_EN and FORCE_MDIX bits in the PHYCR register. When MDIX is enabled, but not forced, this bit will update dynamically as the Auto-MDIX algorithm swaps between MDI and MDIX configurations. 1 = MDI pairs swapped (Receive on TPTD pair, Transmit on TPRD pair) 0 = MDI pairs normal (Receive on TPRD pair, Transmit on TPTD pair)

Table 5-20. PHY Status Register (PHYSTS), Address 0x10 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
13	RECEIVE ERROR LATCH	0, RO/LH	**Receive Error Latch:** This bit will be cleared upon a read of the RECR register. 1 = Receive error event has occurred since last read of RXERCNT (address 15h, Page 0). 0 = No receive error event has occurred.
12	POLARITY STATUS	0, RO	**Polarity Status:** This bit is a duplication of bit 4 in the 10BTSCR register. This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 1 = Inverted Polarity detected. 0 = Correct Polarity detected.
11	FALSE CARRIER SENSE LATCH	0, RO/LH	**False Carrier Sense Latch:** This bit will be cleared upon a read of the FCSR register. 1 = False Carrier event has occurred since last read of FCSCR (address 14h). 0 = No False Carrier event has occurred.
10	SIGNAL DETECT	0, RO/LL	**100Base-TX qualified Signal Detect from PMA:** This is the SD that goes into the link monitor. It is the AND of raw SD and descrambler lock, when address 16h, bit 8 (page 0) is set. When bit 8 of address 16h is cleared, it will be equivalent to the raw SD from the PMD.
9	DESCRAMBLER LOCK	0, RO/LL	100Base-TX Descrambler Lock from PMD.
8	PAGE RECEIVED	0, RO	**Link Code Word Page Received:** This is a duplicate of the Page Received bit in the ANER register, but this bit will not be cleared upon a read of the PHYSTS register. 1 = A new Link Code Word Page has been received. Cleared on read of the ANER (address 06h, bit 1). 0 = Link Code Word Page has not been received.
7	MII INTERRUPT	0, RO	**MII Interrupt Pending:** 1 = Indicates that an internal interrupt is pending. Interrupt source can be determined by reading the MISR Register (12h). Reading the MISR will clear the Interrupt. 0 = No interrupt pending.
6	REMOTE FAULT	0, RO	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read of BMSR (address 01h) register or by reset). Fault criteria: notification from Link Partner of Remote Fault through Auto-Negotiation. 0 = No remote fault condition detected.
5	JABBER DETECT	0, RO	**Jabber Detect:** This bit only has meaning in 10 Mb/s mode. This bit is a duplicate of the Jabber Detect bit in the BMSR register, except that it is not cleared upon a read of the PHYSTS register. 1 = Jabber condition detected. 0 = No Jabber.
4	AUTO-NEG COMPLETE	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation complete. 0 = Auto-Negotiation not complete.
3	LOOPBACK STATUS	0, RO	**Loopback:** 1 = Loopback enabled. 0 = Normal operation.

Table 5-20. PHY Status Register (PHYSTS), Address 0x10 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
2	DUPLEX STATUS	0, RO	**Duplex:** This bit indicates duplex status and is determined from Auto-Negotiation or Forced Modes. 1 = Full-duplex mode. 0 = Half-duplex mode. *Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.*
1	SPEED STATUS	0, RO	**Speed10:** This bit indicates the status of the speed and is determined from Auto-Negotiation or Forced Modes. 1 = 10 Mb/s mode. 0 = 100 Mb/s mode. *Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.*
0	LINK STATUS	0, RO	**Link Status:** This bit is a duplicate of the Link Status bit in the BMSR register, except that it will not be cleared upon a read of the PHYSTS register. 1 = Valid link established (for either 10- or 100 Mb/s operation). 0 = Link not established.

5.6.1.1.11 MII Interrupt Control Register (MICR)

This register implements the MII Interrupt PHY Specific Control register. Sources for interrupt generation include: Link Quality Monitor, Energy Detect State Change, Link State Change, Speed Status Change, Duplex Status Change, Auto-Negotiation Complete or any of the counters becoming half-full. The individual interrupt events must be enabled by setting bits in the MII Interrupt Status and Event Control Register (MISR).

Table 5-21. MII Interrupt Control Register (MICR), Address 0x11

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	0000 0000 0000, RO	**RESERVED:** Writes ignored, read as 0.
3	PTP_INT_SEL	0, RW	**PTP Interrupt Select:** Maps PTP Interrupt to the MISR register in place of the Duplex Interrupt. The Duplex Interrupt will be combined with the Speed Interrupt. 1 = Map PTP Interrupt to MISR[11] , Speed/Duplex Interrupt to MISR[12] 0 = Map Duplex Interrupt to MISR[11], Speed Interrupt to MISR[12]
2	TINT	0, RW	**Test Interrupt:** Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set. 1 = Generate an interrupt. 0 = Do not generate interrupt.
1	INTEN	0, RW	**Interrupt Enable:** Enable interrupt dependent on the event enables in the MISR register. 1 = Enable event based interrupts. 0 = Disable event based interrupts.
0	INT_OE	0, RW	**Interrupt Output Enable:** Enable interrupt events to signal through the PWRDOWN/INTN pin by configuring the PWRDOWN/INTN pin as an output. 1 = PWRDOWN/INTN is an Interrupt Output. 0 = PWRDOWN/INTN is a Power Down Input.

5.6.1.1.12 MII Interrupt Status and Event Control Register (MISR)

This register contains event status and enables for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. If the corresponding enable bit in the register is set, an interrupt will be generated if the event occurs. The MICR register controls must also be set to allow interrupts. The status indications in this register will be set even if the interrupt is not enabled.

Table 5-22. MII Interrupt Status and Event Control Register (MISR), Address 0x12

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	LQ_INT	0, RO/COR	**Link Quality Interrupt:** 1 = Link Quality interrupt is pending and is cleared by the current read. 0 = No Link Quality interrupt pending.
14	ED_INT	0, RO/COR	**Energy Detect Interrupt:** 1 = Energy detect interrupt is pending and is cleared by the current read. 0 = No energy detect interrupt pending.
13	LINK_INT	0, RO/COR	**Change of Link Status Interrupt:** 1 = Change of link status interrupt is pending and is cleared by the current read. 0 = No change of link status interrupt pending.
12	SPD_INT or SPD_DUP_INT	0, RO/COR	**Change of Speed Status Interrupt:** Change of speed status interrupt. This function is selected if MICR[3] is set to 0. 1 = Speed status change interrupt is pending and is cleared by the current read. 0 = No speed status change interrupt pending. **Change of Speed/Duplex Interrupt:** Change of speed or duplex status interrupt. This function is selected if MICR[3] is set to 1. 1 = Speed/duplex status change interrupt is pending and is cleared by the current read. 0 = No speed/duplex status change interrupt pending.
11	DUP_INT or PTP_INT	0, RO/COR	**Change of Duplex Status Interrupt:** Change of duplex status interrupt. This function is selected if MICR[3] is set to 0. 1 = Duplex status change interrupt is pending and is cleared by the current read. 0 = No duplex status change interrupt pending. **PTP Interrupt:** PTP interrupt. This function is selected if MICR[3] is set to 1. PTP interrupt status should be read from the PTP_STS register. This interrupt will not be rearmed until the PTP_STS register indicates no further PTP status is available. 1 = PTP interrupt is pending and is cleared by the current read. 0 = No PTP interrupt pending.
10	ANC_INT	0, RO/COR	**Auto-Negotiation Complete Interrupt:** 1 = Auto-negotiation complete interrupt is pending and is cleared by the current read. 0 = No Auto-negotiation complete interrupt pending.
9	FHF_INT or CTR_INT	0, RO/COR	**False Carrier Counter Half-Full Interrupt:** False carrier counter half-full interrupt. This function is selected if the PHYCR2[8:7] are both 0. 1 = False carrier counter half-full interrupt is pending and is cleared by the current read. 0 = No false carrier counter half-full interrupt pending. **CTR Interrupt:** False carrier or Receive Error counter half-full interrupt. This function is selected if either of PHYCR2[8:7] are set. 1 = False carrier or receive error counter half-full interrupt is pending and is cleared by the current read. 0 = No false carrier or receive error counter half-full interrupt pending.

Table 5-22. MII Interrupt Status and Event Control Register (MISR), Address 0x12 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
8	RHF_INT or PCF_INT	0, RO/COR	**Receive Error Counter half-full interrupt:** Receive error counter half-full interrupt. This function is selected if the PHYCR2[8:7] are both 0. 1 = Receive error counter half-full interrupt is pending and is cleared by the current read. 0 = No receive error carrier counter half-full interrupt pending. **PCF Interrupt:** PHY Control Frame interrupt. This function is selected if either of PHYCR2[8:7] are set. 1 = PHY Control Frame interrupt is pending and is cleared by the current read. 0 = No PHY Control Frame interrupt pending.
7	LQ_INT_EN	0, RW	Enable Interrupt on Link Quality Monitor event.
6	ED_INT_EN	0, RW	Enable Interrupt on energy detect event.
5	LINK_INT_EN	0, RW	Enable Interrupt on change of link status.
4	SPD_INT_EN	0, RW	Enable Interrupt on change of speed status.
3	DUP_INT_EN or PTP_INT_EN	0, RW	**Duplex Interrupt:** Enable Interrupt on change of duplex status. This function is selected if MICR[3] is set to 0. **PTP Interrupt:** PTP interrupt. This function is selected if MICR[3] is set to 1.
2	ANC_INT_EN	0, RW	Enable Interrupt on auto-negotiation complete event.
1	FHF_INT_EN or CTR_INT_EN	0, RW	**FHF Interrupt:** Enable Interrupt on False Carrier Counter Register halffull event. This function is selected if the PHYCR2[8:7] are both 0. **CTR Interrupt:** Enable interrupt on either Receive Error Counter Register half-full event or False Carrier Counter Register half-full event. This function is selected if either of PCFCR[7:6] are set.
0	RHF_INT_EN or PCF_INT_EN	0, RW	**RHF Interrupt:** Enable Interrupt on Receive Error Counter Register halffull event. This function is selected if the PHYCR2[8:7] are both 0. **PCF Interrupt:** Enable Interrupt on a PHY Control Frame event. This function is selected if either of PCFCR[7:6] are set.

5.6.1.1.13 Page Select Register (PAGESEL)

This register is used to enable access to the Link Diagnostics Registers.

Table 5-23. Page Select Register (PAGESEL), Address 0x13

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:3	RESERVED	0000 0000 0000 0, RO	**RESERVED**: Writes ignored, read as 0
2:0	PAGE_SEL	000, RW	**Page_Sel Bits:** Selects between paged registers for address 14h to 1Fh. 0 = Extended Registers Page 0 1 = RESERVED 2 = Link Diagnostics Registers Page 2 3 = RESERVED 4 = PTP 1588 Base Registers Page 4 5 = PTP 1588 Config Registers Page 5 6 = PTP 1588 Config Registers Page 6

5.6.1.2 Extended Registers - Page 0

5.6.1.2.1 False Carrier Sense Counter Register (FCSCR)

This counter provides information required to implement the “False Carriers” attribute within the MAU managed object class of Clause 30 of the IEEE 802.3 specification.

Table 5-24. False Carrier Sense Counter Register (FCSCR), Address 0x14

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0000 0000, RO	**RESERVED:** Writes ignored, read as 0
7:0	FCSCNT[7:0]	0000 0000, RO/COR	**False Carrier Event Counter:** This 8-bit counter increments on every false carrier event. This counter sticks when it reaches its maximum count (FFh).

5.6.1.2.2 Receiver Error Counter Register (RECR)

This counter provides information required to implement the “Symbol Error During Carrier” attribute within the PHY managed object class of Clause 30 of the IEEE 802.3 specification.

Table 5-25. Receiver Error Counter Register (RECR), Address 0x15

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0000 0000, RO	**RESERVED**: Writes ignored, read as 0.
7:0	RXERCNT[7:0]	0000 0000, RO/COR	**RX_ER Counter:** When a valid carrier is present and there is at least one occurrence of an invalid data symbol, this 8-bit counter increments for each receive error detected. This event can increment only once per valid carrier event. If a collision is present, the attribute will not increment. The counter sticks when it reaches its maximum count.

5.6.1.2.3 100 Mb/s PCS Configuration and Status Register (PCSR)

This register contains control and status information for the 100BASE Physical Coding Sublayer.

Table 5-26. 100 Mb/s PCS Configuration and Status Register (PCSR), Address 0x16

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0000, RW	**RESERVED**: Must be 0.
11	FREE_CLK	0, RW	**Receive Clock:** 1 = RX_CLK is free-running. 0 = RX_CLK phase adjusted based on alignment.
10	TQ_EN	0, RW	**100 Mb/s True Quiet Mode Enable:** 1 = Transmit True Quiet Mode. 0 = Normal Transmit Mode.
9	SD FORCE PMA	0, RW	**Signal Detect Force PMA:** 1 = Forces Signal Detection in PMA. 0 = Normal SD operation.
8	SD_OPTION	1, RW	**Signal Detect Option:** 1 = Default operation. Link will be asserted following detection of valid signal level and Descrambler Lock. Link will be maintained as long as signal level is valid. A loss of Descrambler Lock will not cause Link Status to drop. 0 = Modified signal detect algorithm. Link will be asserted following detection of valid signal level and Descrambler Lock. Link will be maintained as long as signal level is valid and Descrambler remains locked.

Table 5-26. 100 Mb/s PCS Configuration and Status Register (PCSR), Address 0x16 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
7	DESC_TIME	0, RW	**Descrambler Timeout:** Increase the descrambler timeout. When set, this allows the device to receive larger packets (>9k bytes) without loss of synchronization. 1 = 2 ms. 0 = 722 µs (per ANSI X3.263: 1995 (TP-PMD) 7.2.3.3e).
6	FX_EN	Strap, RW	**FX Fiber Mode Enable:** This bit is set when the FX_EN strap option is selected for the respective port. Write PHYCR2[9], SOFT_RESET, after enabling or disabling Fiber Mode through register access to ensure correct configuration. 1 = Enables FX operation. 0 = Disables FX operation.
5	FORCE_100_OK	0, RW	**Force 100 Mb/s Good Link:** OR'ed with MAC_FORCE_LINK_100 signal. 1 = Forces 100 Mb/s Good Link. 0 = Normal 100 Mb/s operation.
4	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
3	FEFI_EN	Strap, RW	**Far End Fault Indication Mode Enable:** This bit is set when the FX_EN strap option is selected for the respective port. 1 = FEFI Mode Enabled. 0 = FEFI Mode Disabled.
2	NRZI_BYPASS	0, RW	**NRZI Bypass Enable:** 1 = NRZI Bypass Enabled. 0 = NRZI Bypass Disabled.
1	SCRAM BYPASS	Strap, RW	**Scrambler Bypass Enable:** This bit is set when the FX_EN strap option is selected. In the FX mode, the scrambler is bypassed. 1 = Scrambler Bypass Enabled. 0 = Scrambler Bypass Disabled.
0	DESCRAM BYPASS	Strap, RW	**Descrambler Bypass Enable:** This bit is set when the FX_EN strap option is selected. In the FX mode, the descrambler is bypassed. 1 = Descrambler Bypass Enabled. 0 = Descrambler Bypass Disabled.

5.6.1.2.4 RMII and Bypass Register (RBR)

This register configures the RMII/MII Interface Mode of operation. This register controls selecting MII, RMII, or Single Clock MII mode for Receive or Transmit. In addition, several additional bits are included to allow datapath selection for Transmit and Receive in multiport applications.

Table 5-27. RMII and Bypass Register (RBR), Address 0x17

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RW	**RESERVED**: Must be 0.
14	RMII_MASTER	Strap, RW	**RMII Master Mode:** Setting this bit allows the core to use a 25-MHz input reference clock and generate its own 50-MHz RMII reference clock. The generated RMII reference clock will also be used by the attached MAC. 1 = RMII Master Mode (25-MHz input reference) 0 = RMII Slave Mode (50-MHz input reference) Note: Due to clock muxing and divider operation, this bit should normally only be reconfigured through the strap option.

Table 5-27. RMII and Bypass Register (RBR), Address 0x17 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
13	DIS_TX_OPT	0, RW	**Disable RMII TX Latency Optimization:** Normally the RMII Transmitter will minimize the transmit latency by realigning the transmit clock with the reference clock phase at the start of a packet transmission. Setting this bit will disable phase realignment and ensure that IDLE bits will always be sent in multiples of the symbol size. This will result in a larger uncertainty in RMII transmit latency.
12:9	RESERVED	0000, RW	**RESERVED:** Must be 0.
8	PMD_LOOP	0, RW	**PMD Loopback:** 0 = Normal Operation. 1 = Remote (PMD) Loopback. Setting this bit will cause the device to Loopback data received from the Physical Layer. The loopback is done prior to the MII or RMII interface. Data received at the internal MII or RMII interface will be applied to the transmitter. This mode should only be used if RMII mode or Single Clock MII mode is enabled.
7	SCMII_RX	0, RW	**Single Clock RX MII Mode:** 0 = Standard MII mode. 1 = Single Clock RX MII Mode. Setting this bit will cause the device to generate receive data (RX_DV, RX_ER, RXD[3:0]) synchronous to the X1 Reference clock. RX_CLK is not used in this mode. This mode uses the RMII elasticity buffer to tolerate variations in clock frequencies. This bit cannot be set if RMII_MODE is set to a 1.
6	SCMII_TX	0, RW	**Single Clock TX MII Mode:** 0 = Standard MII mode. 1 = Single Clock TX MII Mode. Setting this bit will cause the device to sample transmit data (TX_EN, TXD[3:0]) synchronous to the X1 Reference clock. TX_CLK is not used in this mode. This bit cannot be set if RMII_MODE is set to a 1.
5	RMII_MODE	Strap, RW	**Reduced MII Mode:** 0 = Standard MII Mode. 1 = Reduced MII Mode.
4	RMII_REV1_0	0, RW	**Reduced MII Revision 1.0:** This bit modifies how CRS_DV is generated. 0 = (RMII revision 1.2) CRS_DV will toggle at the end of a packet to indicate deassertion of CRS. 1 = (RMII revision 1.0) CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet.
3	RX_OVF_STS	0, RO	**RX FIFO Over Flow Status:** 0 = Normal. 1 = Overflow detected.
2	RX_UNF_STS	0, RO	**RX FIFO Under Flow Status:** 0 = Normal. 1 = Underflow detected.
1:0	ELAST_BUF[1:0]	01, RW	**Receive Elasticity Buffer:** This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50 MHz RMII clock and the recovered data. See Section 5.4.3 for more information on Elasticity Buffer settings in RMII mode. See Section 5.4.4 for more information on Elasticity Buffer settings in SCMII mode.

5.6.1.2.5 LED Direct Control Register (LEDCR)

This register provides the ability to directly control any or all LED outputs. It does not provide read access to LEDs. In addition, it provides control for the Activity source and blinking LED frequency.

Table 5-28. LED Direct Control Register (LEDCR), Address 0x18

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0000, RO	**RESERVED**: Writes ignored, read as 0.
11	DIS_SPDLED	0, RW	1 = Disable LED_SPEED output 0 = Enable LED_SPEED output
10	DIS_LNKLED	0, RW	1 = Disable LED_LINK output 0 = Enable LED_LINK output
9	DIS_ACTLED	0, RW	1 = Disable LED_ACT output 0 = Enable LED_ACT output
8	LEDACT_RX	0, RW	1 = Activity is only indicated for Receive traffic 0 = Activity is indicated for Transmit or Receive traffic
7:6	BLINK_FREQ	00, RW	**LED Blink Frequency:** These bits control the blink frequency of the LED_LINK output when blinking on activity is enabled. 0 = 6 Hz 1 = 12 Hz 2 = 24 Hz 3 = 48 Hz
5	DRV_SPDLED	0, RW	1 = Drive value of SPDLED bit onto LED_SPEED output 0 = Normal operation
4	DRV_LNKLED	0, RW	1 = Drive value of LNKLED bit onto LED_LINK output 0 = Normal operation
3	DRV_ACTLED	0, RW	1 = Drive value of ACTLED bit onto LED_ACT output 0 = Normal operation
2	SPDLED	0, RW	Value to force on LED_SPEED output
1	LNKLED	0, RW	Value to force on LED_LINK output
0	ACTLED	0, RW	Value to force on LED_ACT output

5.6.1.2.6 PHY Control Register (PHYCR)

This register provides control for PHY functions such as MDIX, BIST, LED configuration, and PHY address. It also provides Pause Negotiation status.

Table 5-29. PHY Control Register (PHYCR), Address 0x19

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	MDIX_EN	1, RW	**Auto-MDIX Enable:** 1 = Enable Auto-neg Auto-MDIX capability. 0 = Disable Auto-neg Auto-MDIX capability.
14	FORCE_MDIX	0, RW	**Force MDIX**: 1 = Force MDI pairs to cross. (Receive on TD pair, Transmit on RD pair) 0 = Normal operation.
13	PAUSE_RX	0, RO	**Pause Receive Negotiated:** Indicates that pause receive should be enabled in the MAC. Based on ANAR[11:10] and ANLPAR[11:10] settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, “Pause Resolution”, only if the Auto-Negotiated Highest Common Denominator is a full-duplex technology.
12	PAUSE_TX	0, RO	**Pause Transmit Negotiated:** Indicates that pause transmit should be enabled in the MAC. Based on ANAR[11:10] and ANLPAR[11:10] settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, Pause Resolution, only if the Auto-Negotiated Highest Common Denominator is a full-duplex technology.
11	BIST_FE	0, RW/SC	**BIST Force Error:** 1 = Force BIST Error. 0 = Normal operation. This bit forces a single error, and is self clearing.
10	PSR_15	0, RW	**BIST Sequence select:** 1 = PSR15 selected. 0 = PSR9 selected.
9	BIST_STATUS	0, LL/RO	**BIST Test Status:** 1 = BIST pass. 0 = BIST fail. Latched, cleared when a BIST failure occurs or BIST is stopped. For a count number of BIST errors, see the BIST Error Count in the CDCTRL1 register.
8	BIST_START	0, RW	**BIST Start:** *Writes:* 1 = BIST start. Writing 1 to this bit enables transmission of BIST packets and enables the receive BIST engine to start looking for packet traffic. 0 = BIST stop. Stop the BIST. Writing 0 to this bit also clears the BIST_STATUS bit. *Reads:* 1 = BIST active. This bit reads 1 after the transmit BIST engine has been enabled and the receive BIST engine has detected packet traffic. 0 = BIST inactive. This bit will read 0 if the BIST is disabled or if the BIST is enabled but no receive traffic has been detected.
7	BP_STRETCH	0, RW	**Bypass LED Stretching:** This will bypass the LED stretching and the LEDs will reflect the internal value. 1 = Bypass LED stretching. 0 = Normal operation.

Table 5-29. PHY Control Register (PHYCR), Address 0x19 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
6 5	LED_CNFG[1] LED_CNFG[0]	0, RW Strap, RW	**LED Configuration**
			LED_CNFG[1] / **LED_CNFG[0]** / **Mode Description** Don't care / 1 / Mode 1 0 / 0 / Mode 2 1 / 0 / Mode 3
			In **Mode 1**, LEDs are configured as follows: LED_LINK = ON for Good Link, OFF for No Link LED_SPEED = ON in 100 Mb/s, OFF in 10 Mb/s LED_ACT = ON for Activity, OFF for No Activity
			In **Mode 2**, LEDs are configured as follows: LED_LINK = ON for Good Link, BLINK for Activity LED_SPEED = ON in 100 Mb/s, OFF in 10 Mb/s LED_ACT = ON for Collision, OFF for No Collision
			In **Mode 3**, LEDs are configured as follows: LED_LINK = ON for Good Link, BLINK for Activity LED_SPEED = ON in 100 Mb/s, OFF in 10 Mb/s LED_ACT = ON for Full Duplex, OFF for Half Duplex
4:0	PHYADDR[4:0]	Strap, RW	**PHY Address:** PHY address for port. **Note:** The local PHY address cannot be changed through a broadcast write - writing to PHY address 0x1F register 0x19 will not change the PHYADDR bits.

5.6.1.2.7 10Base-T Status/Control Register (10BTSCR)

This register is used for control and status for 10BASE-T device operation.

Table 5-30. 10Base-T Status/Control Register (10BTSCR), Address 0x1A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
14:12	RESERVED	000, RW	**RESERVED:** Must be zero.
11:9	SQUELCH	100, RW	**Squelch Configuration:** Used to set the Squelch 'ON' threshold for the receiver. Default Squelch 'ON' is 330 mV peak.
8	LOOPBACK_10_DIS	0, RW	**10Base-T Loopback Disable:** This bit is OR'ed with bit 14 (Loopback) in the BMCR. 1 = 10BT Loopback is disabled 0 = 10BT Loopback is enabled
7	LP_DIS	0, RW	**Normal Link Pulse Disable:** This bit is OR'ed with the MAC_FORCE_LINK_10 signal. 1 = Transmission of NLPs is disabled. 0 = Transmission of NLPs is enabled.
6	FORCE_LINK_10	0, RW	**Force 10 Mb Good Link:** This bit is OR'ed with the MAC_FORCE_LINK_10 signal. 1 = Forced Good 10 Mb Link. 0 = Normal Link Status.
5	FORCE_POL COR	0, RW	**Force 10 Mb Polarity Correction:** 1 = Force inverted polarity 0 = Normal polarity
4	POLARITY	0, RO/LH	**10 Mb Polarity Status:** This bit is a duplication of bit 12 in the PHYSTS register. Both bits will be cleared upon a read of either register. 1 = Inverted Polarity detected. 0 = Correct Polarity detected.

Table 5-30. 10Base-T Status/Control Register (10BTSCR), Address 0x1A (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
3	AUTOPOL_DIS	0, RW	**Auto Polarity Detection and Correction Disable:** 1 = Polarity Correction disabled 0 = Polarity Correction enabled
2	10BT_SCALE - MSB	1, RW	**10BT Scale Configuration Most Significant Bit** Used in conjunction with bit 10 of SD_CNFG register to set the silence 'OFF' threshold for the receiver.
1	HEARTBEAT_DIS	0, RW	**Heartbeat Disable:** This bit only has influence in half-duplex 10 Mb mode. 1 = Heartbeat function disabled. 0 = Heartbeat function enabled. **When the device is operating at 100 Mb or configured for full-duplex operation, this bit will be ignored - the heartbeat function is disabled.**
0	JABBER_DIS	0, RW	**Jabber Disable:** This bit is only applicable in 10BASE-T. 1 = Jabber function disabled. 0 = Jabber function enabled.

5.6.1.2.8 CD Test and BIST Extensions Register (CDCTRL1)

This register controls test modes for the 10BASE-T Common Driver. In addition it contains extended control and status for the packet BIST function.

Table 5-31. CD Test and BIST Extensions Register (CDCTRL1), Address 0x1B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	BIST_ERROR_COUNT	0000 0000, RO	**BIST ERROR Counter:** Counts number of errored data nibbles during Packet BIST. This value will reset when Packet BIST is restarted. The counter sticks when it reaches its maximum count of FFh.
7	RESERVED	0, RW	**RESERVED:** Must be 0.
6	MII_CLOCK_EN	0, RW	Enables MII Clocks TX_CLK and RX_CLK independent of MAC interface mode selected; for example, normally TX_CLK and RX_CLK are disabled in RMII Slave mode. 1 = Enable TX_CLK and RX_CLK 0 = Default operation
5	BIST_CONT	0, RW	**Packet BIST Continuous Mode:** Allows continuous pseudorandom data transmission without any break in transmission. This can be used for transmit VOD testing. This is used in conjunction with the BIST controls in the PHYCR Register (19h). For 10 Mb operation, jabber function must be disabled, bit 0 of the 10BTSCR (1Ah), JABBER_DIS = 1.
4	CDPATTEN_10	0, RW	**CD Pattern Enable for 10 Mb:** 1 = Enabled. 0 = Disabled.
3	MDIO_PULL_EN	0, RW	**Enable Internal MDIO Pullup:** 1 = Internal MDIO pullup enabled 0 = Internal MDIO pullup disabled This bit is only reset on hard reset. This bit should not be set in systems that share the management interfaces among several ASICs.
2	PATT_GAP_10M	0, RW	**Defines gap between data or NLP test sequences:** 1 = 15 µs. 0 = 10 µs.

Table 5-31. CD Test and BIST Extensions Register (CDCTRL1), Address 0x1B (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
1:0	CDPATTSEL[1:0]	00, RW	**CD Pattern Select[1:0]:** If CDPATTEN_10 = 1: 00 = Data, EOP0 sequence. 01 = Data, EOP1 sequence. 10 = NLPs. 11 = Constant Manchester 1s (10-MHz sine wave) for harmonic distortion testing.

5.6.1.2.9 PHY Control Register 2 (PHYCR2)

This register provides additional general control.

Table 5-32. PHY Control Register 2 (PHYCR2), Address 0x1C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	00, RO	**RESERVED**: Writes ignored, read as 0.
13	SYNC_ENET EN	0, RW	**Synchronous Ethernet Enable:** When this bit is 1 and the device is in 100 Mb/s mode, and the MAC interface is either MII or RMII Master, enables fully synchronous communication relative to the recovered receive clock. The transmitter is synchronized to the receiver. When this bit is 0 or the device settings do not match the above conditions, the transmitter is synchronous to the local reference clock.
12	CLK_OUT RXCLK	0, RW	**Enable RX_CLK on CLK_OUT:** When this bit is 1 and the device is in 100 Mb/s mode, the 25-MHz recovered receive clock (RX_CLK) is driven on CLK_OUT in addition to RX_CLK. When this bit is 0 or the device is in 10 Mb/s mode, CLK_OUT reflects the Reference clock.
11	BC_WRITE	0, RW	**Broadcast Write Enable:** 1 = Enables the Serial Management Interface to accept register writes to PHY Address of 0x1F independent of the local PHY Address value. 0 = Normal operation
10	PHYTER_COMP	0, RW	**Phyter Compatibility Mode:** 1 = Enables Phyter (DP83848) Compatible pinout. Reorders the RX MII pins and Autonegotiation straps to match the DP83848. Also enables the CLK_OUT output. 0 = Normal operation
9	SOFT_RESET	0, RW/SC	**Soft Reset:** Resets the entire device minus the registers - all configuration is preserved. 1 = Reset, self-clearing.
8:2	RESERVED	0 0000 00, RO	**RESERVED:** Writes ignored, read as 0.
1	CLK_OUT_DIS	Strap, RW	**Disable CLK_OUT Output:** Disables the CLK_OUT output pin.
0	RESERVED	0, RW	**RESERVED:** Must be zero.

5.6.1.2.10 Energy Detect Control (EDCR)

This register provides control and status for the Energy Detect function.

Table 5-33. Energy Detect Control (EDCR), Address 0x1D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	ED_EN	0, RW	**Energy Detect Enable:** Allow Energy Detect Mode.
14	ED_AUTO_UP	1, RW	**Energy Detect Automatic Power Up:** Automatically begin power-up sequence when Energy Detect Data Threshold value (EDCR[3:0]) is reached. Alternatively, the device could be powered up manually using the ED_MAN bit (ECDR[12]).
13	ED_AUTO_DOWN	1, RW	**Energy Detect Automatic Power Down:** Automatically begin power-down sequence when no energy is detected. Alternatively, the device could be powered down using the ED_MAN bit (EDCR[12]).
12	ED_MAN	0, RW/SC	**Energy Detect Manual Power Up/Down:** Begin power-up/down sequence when this bit is asserted. When set, the Energy Detect algorithm will initiate a change of Energy Detect state regardless of threshold (error or data) and timer values. In managed applications, this bit can be set after clearing the Energy Detect interrupt to control the timing of changing the power state.
11	ED_BURST_DIS	0, RW	**Energy Detect Burst Disable:** Disable bursting of energy detect data pulses. By default, Energy Detect (ED) transmits a burst of 4 ED data pulses each time the CD is powered up. When bursting is disabled, only a single ED data pulse will be sent each time the CD is powered up.
10	ED_PWR_STATE	0, RO	**Energy Detect Power State:** Indicates current Energy Detect Power state. When set, Energy Detect is in the powered up state. When cleared, Energy Detect is in the powered down state. This bit is invalid when Energy Detect is not enabled.
9	ED_ERR_MET	0, RO/COR	**Energy Detect Error Threshold Met:** No action is automatically taken upon receipt of error events. This bit is informational only and would be cleared on a read.
8	ED_DATA_MET	0, RO/COR	**Energy Detect Data Threshold Met:** The number of data events that occurred met or surpassed the Energy Detect Data Threshold. This bit is cleared on a read.
7:4	ED_ERR_COUNT	0001, RW	**Energy Detect Error Threshold:** Threshold to determine the number of energy detect error events that should cause the device to take action. Intended to allow averaging of noise that may be on the line. Counter will reset after approximately 2 seconds without any energy detect data events.
3:0	ED_DATA_COUNT	0001, RW	**Energy Detect Data Threshold:** Threshold to determine the number of energy detect events that should cause the device to take actions. Intended to allow averaging of noise that may be on the line. Counter will reset after approximately 2 seconds without any energy detect data events.

5.6.1.2.11 PHY Control Frames Configuration Register (PCFCR)

This register provides configuration for the PHY Control Frame mechanism for register access.

Table 5-34. PHY Control Frames Configuration Register (PCFCR), Address 0x1F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	PCF_STS_ERR	0, RO/COR	**PHY Control Frame Error Detected:** Indicates an error was detected in a PCF Frame since the last read of this register. This bit will be cleared on read.
14	PCF_STS_OK	0, RO/COR	**PHY Control Frame OK:** Indicates a PCF Frame has completed without error since the last read of this register. This bit will be cleared on read.
13:9	RESERVED	00 000, RO	**Reserved:** Writes ignored, read as 0
8	PCF_DA_SEL	0, RW	**Select MAC Destination Address for PHY Control Frames:** 0 : Use MAC Address [08 00 17 0B 6B 0F] 1 : Use MAC Address [08 00 17 00 00 00] The device will also recognize packets with the above address with the Multicast bit set (that is, 09 00 17 ...).
7:6	PCF_INT_CTL	00, RW	**PHY Control Frame Interrupt Control:** Setting either of these bits enables control and status of the PCF Interrupt through the MISR Register (taking the place of the RHF Interrupt). 00 = PCF Interrupts Disabled x1 = Interrupt on PCF Frame OK 1x = Interrupt on PCF Frame Error
5	PCF_BC_DIS	0, RW	**PHY Control Frame Broadcast Disable:** By default, the device will accept broadcast PHY Control Frames which have a PHY Address field of 0x1F. If this bit is set to a 1, the PHY Control Frame must have a PHY Address field that exactly matches the device PHY Address.
4:1	PCF_BUF	0 000, RW	**PHY Control Frame Buffer Size:** Determines the buffer size for transmit to allow PHY Control Frame detection. All packets will be delayed as they pass through this buffer. If set to 0, packets will not be delayed and PHY Control frames will be truncated after the Destination Address field.
0	PCF_EN	Strap, RW	**PHY Control Frame Enable:** Enables Register writes using PHY Control Frames.

5.6.1.3 Test Registers - Page 1

Page 1 Test Registers are accessible by setting bits [2:0] = 001 of PAGESEL (13h).

5.6.1.3.1 Signal Detect Configuration (SD_CNFG), Page 1

This register contains Signal Detect configuration control as well as some test controls to speed up Auto-neg testing.

Table 5-35. Signal Detect Configuration (SD_CNFG), Address 0x1E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	1, RW	**RESERVED:** Write as 1, read as 1.
14:12	RESERVED	000, RW	**RESERVED:** Write as 0, read as 0.
11	RESERVED	0, RO	**RESERVED:** Write ignored, read as 0.
10:9	RESERVED	00, RW	**RESERVED:** Write as 0, read as 0.
8	SD_TIME	0, RW	**Signal Detect Time** Setting this bit to a 1 enables a fast detection of loss of Signal Detect. This will result in a fast loss of Link indication. Approximate times to detect signal detect deassertion are: 1 = 1 µs 0 = 250 µs
7:0	RESERVED	0000 0000, RW	**RESERVED:** Write as 0, read as 0.

5.6.1.4 Link Diagnostics Registers - Page 2

Page 2 Link Diagnostics Registers are accessible by setting bits [2:0] = 010 of PAGESEL (13h).

5.6.1.4.1 100 Mb Length Detect Register (LEN100_DET), Page 2

This register contains linked cable length estimation in 100 Mb operation. The cable length is an estimation of the effective cable length based on the characteristics of the recovered signal. The cable length is valid only during 100 Mb operation with a valid Link status indication.

Table 5-36. 100 Mb Length Detect Register (LEN100_DET), Address 0x14

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0000 0000, RO	**RESERVED:** Writes ignored, read as 0.
7:0	CABLE_LEN	1111 1111, RO	**Cable Length Estimate:** Indicates an estimate of effective cable length in meters. A value of FFh indicates cable length cannot be determined.

5.6.1.4.2 100 Mb Frequency Offset Indication Register (FREQ100), Page 2

This register returns an indication of clock frequency offset relative to the link partner. Two values can be read, the long term Frequency Offset, or a short term Frequency Control value. The Frequency Control value includes short term phase correction. The variance between the Frequency Control value and the Frequency Offset can be used as an indication of the amount of jitter in the system.

Table 5-37. 100 Mb Frequency Offset Indication Register (FREQ100), Address 0x15

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	SAMPLE_FREQ	0, WO	**Sample Frequency Offset:** If SEL_FC is set to a 0, then setting this bit to a 1 will poll the DSP for the long-term Frequency Offset value. The value will be available in the FREQ_OFFSET bits of this register. If SEL_FC is set to a 1, then setting this bit to a 1 will poll the DSP for the current Frequency Control value. The value will be available in the FREQ_OFFSET bits of this register. This register bit will always read back as 0.
14:9	RESERVED	000 000, RO	**RESERVED:** Writes ignored, read as 0.
8	SEL_FC	0, RW	**Select Frequency Control:** Setting this bit to a 1 will select the current Frequency Control value instead of the Frequency Offset. This value contains Frequency Offset plus the short term phase correction and can be used to indicate amount of jitter in the system. The value will be available in the FREQ_OFFSET bits of this register.
7:0	FREQ_OFFSET	0000 0000, RO	**Frequency Offset:** Frequency offset value loaded from the DSP following assertion of the SAMPLE_FREQ control bit. The Frequency Offset or Frequency Control value is a twos-complement signed value in units of approximately 5.1562 ppm. The range is as follows: 0x7F = +655 ppm 0x00 = 0 ppm 0x80 = –660 ppm

5.6.1.4.3 TDR Control Register (TDR_CTRL), Page 2

This register contains control for the Time Domain Reflectometry (TDR) cable diagnostics. The TDR cable diagnostics sends pulses down the cable and captures reflection data to be used to estimate cable length and detect certain cabling faults.

Table 5-38. TDR Control Register (TDR_CTRL), Address 0x16

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	TDR_ENABLE	0, RW	**TDR Enable:** Enable TDR mode. This forces the power-up state to the correct operating condition for sending and receiving TDR pulses.
14	TDR_100Mb	0, RW	**TDR 100Mb:** Sets the TDR controller to use the 100-Mb Transmitter. This allows for sending pulse widths in multiples of 8 ns. Pulses in 100 Mb mode will alternate between positive pulses and negative pulses. Default operation uses the 10-Mb Link Pulse generator. Pulses may include just the 50 ns pre-emphasis portion of the pulse or the 100-ns full link pulse (as controlled by setting TDR Width).
13	TX_CHANNEL	0, RW	**Transmit Channel Select:** Select transmit channel for sending pulses. The pulse can be sent on the Transmit or Receive pair. 0 : Transmit channel 1 : Receive channel
12	RX_CHANNEL	0, RW	**Receive Channel Select:** Select receive channel for detecting pulses. The pulse can be monitored on the Transmit or Receive pair. 0 : Transmit channel 1 : Receive channel
11	SEND_TDR	0, RW/SC	**Send TDR Pulse:** Setting this bit will send a TDR pulse and enable the monitor circuit to capture the response. This bit will automatically clear when the capture is complete.
10:8	TDR_WIDTH	000, RW	**TDR Pulse Width:** Pulse width in clocks for the transmitted pulse. In 100 Mb mode, pulses are in 8 ns increments. In 10 Mb mode, pulses are in 50 ns increments, but only 50 ns or 100 ns pulses can be sent. Sending a pulse of 0 width will not transmit a pulse, but allows for baseline testing.
7	TDR_MIN_MODE	0, RW	**Min/Max Mode control:** This bit controls direction of the pulse to be detected. Default looks for a positive peak. Threshold and peak values will be interpreted appropriately based on this bit. 0 : Max Mode, detect positive peak 1 : Min Mode, detect negative peak
6	RESERVED	0, RW	**RESERVED:** Must be zero.
5:0	RX_THRESHOLD	10 0000, RW	**RX Threshold:** This value provides a threshold for measurement to the start of a peak. If Min Mode is set to 0, data must be greater than this value to trigger a capture. If Min Mode is 1, data must be less than this value to trigger a capture. Data ranges from 0x00 to 0x3F, with 0x20 as the midpoint. Positive data is greater than 0x20, negative data is less than 0x20.

5.6.1.4.4 TDR Window Register (TDR_WIN), Page 2

This register contains sample window control for the Time Domain Reflectometry (TDR) cable diagnostics. The two values contained in this register specify the beginning and end times for the window to monitor the response to the transmitted pulse. Time values are in 8 ns increments. This provides a method to search for multiple responses and also to screen out the initial outgoing pulse.

Table 5-39. TDR Window Register (TDR_WIN), Address 0x17

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_START	0000 0000, RW	**TDR Start Window:** Specifies start time for monitoring TDR response.
7:0	TDR_STOP	0000 0000, RW	**TDR Stop Window:** Specifies stop time for monitoring TDR response. The Stop Window should be set to a value greater than or equal to the Start Window.

5.6.1.4.5 TDR Peak Register (TDR_PEAK), Page 2

This register contains the results of the TDR Peak Detection. Results are valid if the TDR_CTRL[11] is clear following sending the TDR pulse.

Table 5-40. TDR Peak Register (TDR_PEAK), Address 0x18

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	00, RO	**RESERVED:** Writes ignored, read as 0.
13:8	TDR_PEAK	00 0000, RO	**TDR Peak Value:** This register contains the peak value measured during the TDR sample window. If Min Mode control (TDR_CTRL[7]) is 0, this contains the maximum detected value. If Min Mode control is 1, this contains the minimum detected value.
7:0	TDR_PEAK_TIME	0000 0000, RO	**TDR Peak Time:** Specifies the time for the first occurrence of the peak value.

5.6.1.4.6 TDR Threshold Register (TDR_THR), Page 2

This register contains the results of the TDR Threshold Detection. Results are valid if the TDR_CTRL[11] is clear following sending the TDR pulse.

Table 5-41. TDR Threshold Register (TDR_THR), Address 0x19

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:9	RESERVED	0000 000, RO	**RESERVED:** Writes ignored, read as 0.
8	TDR_THR_MET	0, RO	**TDR Threshold Met:** This bit indicates the TDR threshold was met during the sample window. A value of 0 indicates the threshold was not met.
7:0	TDR_THR_TIME	0000 0000, RO	**TDR Threshold Time:** Specifies the time for the first data that met the TDR threshold. This field is only valid if the threshold was met.

5.6.1.4.7 Variance Control Register (VAR_CTRL), Page 2

The Variance Control and Data Registers provide control and status for the Cable Signal Quality Estimation function. The Cable Signal Quality Estimation allows a simple method of determining an approximate Signal-to-Noise Ratio for the 100 Mb receiver. This register contains the programmable controls and status bits for the variance computation, which can be used to make a simple Signal-to-Noise Ratio estimation.

Table 5-42. Variance Control Register (VAR_CTRL), Address 0x1A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	VAR_RDY	0, RO	**Variance Data Ready Status:** Indicates new data is available in the Variance data register. This bit will be automatically cleared after two consecutive reads of VAR_DATA.
14:4	RESERVED	000 0000 0000, RO	**RESERVED:** Writes ignored, read as 0.
3	VAR_FREEZE	0, RW	**Freeze Variance Registers:** Freeze VAR_DATA register. This bit is ensures that VAR_DATA register is frozen for software reads. This bit is automatically cleared after two consecutive reads of VAR_DATA.
2:1	VAR_TIMER	00, RW	**Variance Computation Timer (in ms):** Selects the Variance computation timer period. After a new value is written, computation is automatically restarted. New variance register values are loaded after the timer elapses. Var_Timer = 0 => 2 ms timer (default) Var_Timer = 1 => 4 ms timer Var_Timer = 2 => 6 ms timer Var_Timer = 3 => 8 ms timer Time units are actually 2^{17} cycles of an 8 ns clock, or 1.048576 ms.
0	VAR_ENABLE	0, RW	**Variance Enable:** Enable Variance computation. Off by default.

5.6.1.4.8 Variance Data Register (VAR_DATA), Page 2

This register contains the 32-bit Variance Sum. The contents of the data are valid only when VAR_RDY is asserted in the VAR_CTRL register. Upon detection of VAR_RDY asserted, software should set the VAR_FREEZE bit in the VAR_CTRL register to prevent loading of a new value into the VAR_DATA register. Because the Variance Data value is 32-bits, two reads of this register are required to get the full value.

Table 5-43. Variance Data Register (VAR_DATA), Address 0x1B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	VAR_DATA	0000 0000 0000 0000, RO	**Variance Data:** Two reads are required to return the full 32-bit Variance Sum value. Following setting the VAR_FREEZE control, the first read of this register will return the low 16 bits of the Variance data. A second read will return the high 16 bits of Variance data.

5.6.1.4.9 Link Quality Monitor Register (LQMR), Page 2

This register contains the controls for the Link Quality Monitor function. The Link Quality Monitor provides a mechanism for programming a set of thresholds for DSP parameters. If the thresholds are violated, an interrupt will be asserted if enabled in the MISR. Monitor control and status are available in this register, while the LQDR register controls read/write access to threshold values and current parameter values. Reading the LQMR register clears warning bits and re-arms the interrupt generation. In addition, this register provides a mechanisms for allowing automatic reset of the 100-Mb link based on the Link Quality Monitor status.

Table 5-44. Link Quality Monitor Register (LQMR), Address 0x1D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	LQM_ENABLE	0, RW	**Link Quality Monitor Enable:** Enables the Link Quality Monitor. The enable is qualified by having a valid 100-Mb link. In addition, the individual thresholds can be disabled by setting to the maximum or minimum values.
14	RESTART_ON_FC	0, RW	**Restart on Frequency Control Warning:** Allow automatic reset of DSP and restart of 100 Mb Adaption on detecting a Frequency Threshold violation. If the SD_Option bit, PCSR[8], is set to 0, the threshold violation will also result in a drop in Link status.
13	RESTART_ON _FREQ	0, RW	**Restart on Frequency Offset Warning:** Allow automatic reset of DSP and restart of 100 Mb Adaption on detecting a Frequency Offset Threshold violation. If the SD_Option bit, PCSR[8], is set to 0, the threshold violation will also result in a drop in Link status.
12	RESTART_ON _DBLW	0, RW	**Restart on DBLW Warning:** Allow automatic reset of DSP and restart of 100 Mb Adaption on detecting a DBLW Threshold violation. If the SD_Option bit, PCSR[8], is set to 0, the threshold violation will also result in a drop in Link status.
11	RESTART_ON _DAGC	0, RW	**Restart on DAGC Warning:** Allow automatic reset of DSP and restart of 100 Mb Adaption on detecting a DAGC Threshold violation. If the SD_Option bit, PCSR[8], is set to 0, the threshold violation will also result in a drop in Link status.
10	RESTART_ON_C1	0, RW	**Restart on C1 Warning:** Allow automatic reset of DSP and restart of 100 Mb Adaption on detecting a C1 Threshold violation. If the SD_Option bit, PCSR[8], is set to 0, the threshold violation will also result in a drop in Link status.
9	FC_HI_WARN	0, RO/COR	**Frequency Control High Warning:** This bit indicates the Frequency Control High Threshold was exceeded. This register bit will be cleared on read.
8	FC_LO_WARN	0, RO/COR	**Frequency Control Low Warning:** This bit indicates the Frequency Control Low Threshold was exceeded. This register bit will be cleared on read.
7	FREQ_HI_WARN	0, RO/COR	**Frequency Offset High Warning:** This bit indicates the Frequency Offset High Threshold was exceeded. This register bit will be cleared on read.
6	FREQ_LO_WARN	0, RO/COR	**Frequency Offset Low Warning:** This bit indicates the Frequency Offset Low Threshold was exceeded. This register bit will be cleared on read.
5	DBLW_HI_WARN	0, RO/COR	**DBLW High Warning:** This bit indicates the DBLW High Threshold was exceeded. This register bit will be cleared on read.
4	DBLW_LO_WARN	0, RO/COR	**DBLW Low Warning:** This bit indicates the DBLW Low Threshold was exceeded. This register bit will be cleared on read.
3	DAGC_HI_WARN	0, RO/COR	**DAGC High Warning:** This bit indicates the DAGC High Threshold was exceeded. This register bit will be cleared on read.

Table 5-44. Link Quality Monitor Register (LQMR), Address 0x1D (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
2	DAGC_LO_WARN	0, RO/COR	**DAGC Low Warning:** This bit indicates the DAGC Low Threshold was exceeded. This register bit will be cleared on read.
1	C1_HI_WARN	0, RO/COR	**C1 High Warning:** This bit indicates the DEQ C1 High Threshold was exceeded. This register bit will be cleared on read.
0	C1_LO_WARN	0, RO/COR	**C1 Low Warning:** This bit indicates the DEQ C1 Low Threshold was exceeded. This register bit will be cleared on read.

5.6.1.4.10 Link Quality Data Register (LQDR), Page 2

This register provides read/write control of thresholds for the 100 Mb Link Quality Monitor function. The register also provides a mechanism for reading current adapted parameter values. Threshold values may not be written if the device is powered-down.

Table 5-45. Link Quality Data Register (LQDR), Address 0x1E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	00, RO	**RESERVED:** Writes ignored, read as 0.
13	SAMPLE_PARAM	0, RW	**Sample DSP Parameter:** Setting this bit to a 1 enables reading of current parameter values and initiates sampling of the parameter value. The parameter to be read is selected by the LQ_PARAM_SEL bits.
12	WRITE_LQ_THR	0, RW	**Write Link Quality Threshold:** Setting this bit will cause a write to the Threshold register selected by LQ_PARAM_SEL and LQ_THR_SEL. The data written is contained in LQ_THR_DATA. This bit will always read back as 0.
11:9	LQ_PARAM_SEL	000, RW	**Link Quality Parameter Select:** This 3-bit field selects the Link Quality Parameter. This field is used for sampling current parameter values as well as for reads/writes to Threshold values. The following encodings are available: 000: DEQ_C1 001: DAGC 010: DBLW 011: Frequency Offset 100: Frequency Control 101: Variance most significant bits 31:16

Table 5-45. Link Quality Data Register (LQDR), Address 0x1E (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
8	LQ_THR_SEL	0, RW	**Link Quality Threshold Select:** This bit selects the Link Quality Threshold to be read or written. A 0 selects the Low threshold, while a 1 selects the high threshold. When combined with the LQ_PARAM_SEL field, the following encodings are available {LQ_PARAM_SEL, LQ_THR_SEL}: 000,0: DEQ_C1 Low 000,1: DEQ_C1 High 001,0: DAGC Low 001,1: DAGC High 010,0: DBLW Low 010,1: DBLW High 011,0: Frequency Offset Low 011,1: Frequency Offset High 100,0: Frequency Control Low 100,1: Frequency Control High 101,0: Variance High bits 7:0 (Variance bits 23:16) 101,1: Variance High bits 15:8 (Variance bits 31:24)
7:0	LQ_THR_DATA	1000 0000, RW	**Link Quality Threshold Data:** The operation of this field is dependent on the value of the SAMPLE_PARAM bit.
			If SAMPLE_PARAM = 0: On a write, this value contains the data to be written to the selected Link Quality Threshold register. On a read, this value contains the current data in the selected Link Quality Threshold register.
			If SAMPLE_PARAM = 1: On a read, this value contains the sampled parameter value. This value will remain unchanged until a new read sequence is started.

5.6.1.4.11 Link Quality Monitor Register 2 (LQMR2), Page 2

This register contains additional controls for the Link Quality Monitor function. The Link Quality Monitor provides a mechanism for programming a set of thresholds for DSP parameters. If the thresholds are violated, an interrupt will be asserted if enabled in the MISR. Monitor control and status are available in this register, while the LQDR register controls read/write access to threshold values and current parameter values. Reading of LQMR2 register clears its warning bits but does NOT re-arm the interrupt generation; LQMR must be read to re-arm interrupt generation. In addition, this register provides a mechanism for allowing automatic reset of the 100 Mb link based on the Link Quality Monitor variance status.

Table 5-46. Link Quality Monitor Register 2 (LQMR2), Address 0x1F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0000 0, RO	**Reserved:** Writes ignored, Read as 0
10	RESTART_ON_VAR	0, RW	**Restart on Variance Warning:** Allow automatic reset of DSP and restart of 100 Mb Adaption on detecting a Frequency Offset Threshold violation. If the SD_Option bit, PCSR[8], is set to 0, the threshold violation will also result in a drop in Link status.
9:2	RESERVED	00 0000 00, RO	**Reserved:** Writes ignored, Read as 0
1	VAR_HI_WARN	0, RO/COR	**Variance High Warning:** This bit indicates the Variance High Threshold was exceeded. This register bit will be cleared on read.
0	RESERVED	0, RO	**Reserved:** Writes ignored, Read as 0

5.6.1.5 PTP 1588 Base Registers - Page 4

Page 4 PTP 1588 Base Registers are accessible by setting bits [2:0] = 100 of PAGESEL (13h).

5.6.1.5.1 PTP Control Register (PTP_CTL), Page 4

This register provides basic control of the PTP 1588 operation.

Table 5-47. PTP Control Register (PTP_CTL), Address 0x14

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	RESERVED	000, RO	**Reserved:** Writes ignored, Read as 0
12:10	TRIG_SEL	000, RW	**PTP Trigger Select:** This field selects the Trigger for loading control information or for enabling the Trigger.
9	TRIG_DIS	0, RW/SC	**Disable PTP Trigger:** Setting this bit will disable the selected Trigger. This bit does not indicate Disable status for Triggers. The PTP Trigger Status Register should be used to determine Trigger Status. This bit is self-clearing and will always read back as 0. Disabling a Trigger will not disconnect it from a GPIO pin. The Trigger value will still be driven to the GPIO if the Trigger is assigned to a GPIO.
8	TRIG_EN	0, RW/SC	**Enable PTP Trigger:** Setting this bit will enable the selected Trigger. This bit does not indicate Enable status for Triggers. The PTP Trigger Status Register should be used to determine Trigger Status. This bit is self-clearing and will always read back as 0.
7	TRIG_READ	0, RW/SC	**Read PTP Trigger:** Setting this bit will begin the Trigger Read process. The Trigger is selected based on the setting of the TRIG_SEL bits in this register. Upon setting this bit, subsequent reads of the PTP_TDR will return the Trigger Control values. Fields are read in the same order as written.
6	TRIG_LOAD	0, RW/SC	**Load PTP Trigger:** Setting this bit will disable the selected Trigger and begin the Trigger load process. The Trigger is selected based on the setting of the TRIG_SEL bits in this register. Upon setting this bit, subsequent writes to the PTP_TDR will set the Trigger Control fields for the selected Trigger. The Trigger Load is completed once all fields have been written, or the TRIG_EN bit has been set in this register. This bit is self-clearing and will read back as 0 when the Trigger Load is completed either by writing all Trigger Control fields, or by setting the Trigger Enable.
5	PTP_RD_CLK	0, RW/SC	**Read PTP Clock:** Setting this bit will cause the device to sample the PTP Clock time value. The time value will be made available for reading through the PTP_TDR register. This bit is self-clearing and will always read back as 0.
4	PTP_LOAD_CLK	0, RW/SC	**Load PTP Clock:** Setting this bit will cause the device to load the PTP Clock time value from data previously written to the PTP_TDR register. This bit is self-clearing and will always read back as 0.
3	PTP_STEP_CLK	0, RW/SC	**Step PTP Clock:** Setting this bit will cause the device to add a value to the PTP Clock. The value to be added is the value previously written to the PTP_TDR register. This bit is selfclearing and will always read back as 0.
2	PTP_ENABLE	0, RW	**Enable PTP Clock:** Setting this bit will enable the PTP Clock. Reading this bit will return the current enabled value. Writing a 0 to this bit will have no effect.
1	PTP_DISABLE	0, RW/SC	**Disable PTP Clock:** Setting this bit will disable the PTP Clock. Writing a 0 to this bit will have no effect. This bit is self-clearing and will always read back as 0.
0	PTP_RESET	0, RW	**Reset PTP Clock:** Setting this bit will reset the PTP Clock and associated logic. In addition, the 1588 registers will be reset, with the exception of the PTP_COC and PTP_CLKSRC registers. Unlike other bits in this register, this bit is not self-clearing and must be written to 0 to release the clock and logic from reset.

5.6.1.5.2 PTP Time Data Register (PTP_TDR), Page 4

This register provides a mechanism for reading and writing the 1588 Time and Trigger Control values. The function of this register is determined by controls in the PTP_CTL register.

Table 5-48. PTP Time Data Register (PTP_TDR), Address 0x15

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	TIME_DATA	XXXX XXXX XXXX XXXX, RO XXXX XXXX XXXX XXXX, WO	**Time Data:** On Reads, successively returns 16-bit values of the Clock time or Trigger Control information as selected by controls in the PTP Control Register. Additional reads beyond the avaliable fields will always return 0. On Writes, successively stores the 16-bit values of Clock time or Trigger Control Information as selected by controls in the PTP Control Register.

5.6.1.5.3 PTP Status Register (PTP_STS), Page 4

This register provides basic status and interrupt control for the PTP 1588 operation.

Table 5-49. PTP Status Register (PTP_STS), Address 0x16

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0000, RO	**Reserved:** Writes ignored, Read as 0
11	TXTS_RDY	0, RO	**Transmit Timestamp Ready:** A Transmit Timestamp is available for an outbound PTP Message. This bit will be cleared upon read of the Transmit Timestamp if no other timestamps are ready.
10	RXTS_RDY	0, RO	**Receive Timestamp Ready:** A Receive Timestamp is available for an inbound PTP Message. This bit will be cleared upon read of the Receive Timestamp if no other timestamps are ready.
9	TRIG_DONE	0, RO/COR	**PTP Trigger Done:** A PTP Trigger has occured. This bit will be cleared upon read. This bit will only be set if Trigger Notification is turned on for the Trigger through the Trigger Configuration Registers.
8	EVENT_RDY	0, RO	**PTP Event Timestamp Ready:** A PTP Event Timestamp is available. This bit will be cleared upon read of the PTP Event Status Register if no other event timestamps are ready.
7:4	RESERVED	0000, RO	**Reserved:** Writes ignored, Read as 0
3	TXTS_IE	0, RW	**Transmit Timestamp Interrupt Enable:** Enable Interrupt on Transmit Timestamp Ready.
2	RXTS_IE	0, RW	**Receive Timestamp Interrupt Enable:** Enable Interrupt on Receive Timestamp Ready.
1	TRIG_IE	0, RW	**Trigger Interrupt Enable:** Enable Interrupt on Trigger Completion.
0	EVENT_IE	0, RW	**Event Interrupt Enable:** Enable Interrupt on Event Timestamp Ready.

5.6.1.5.4 PTP Trigger Status Register (PTP_TSTS), Page 4

This register provides status of the PTP 1588 Triggers. The bits in this register indicate the current status of each of the Trigger modules. The error bits will be set if the associated notification enable (TRIGN_NOTIFY) is set in the PTP Trigger Configuration Registers.

Table 5-50. PTP Trigger Status Register (PTP_TSTS), Address 0x17

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	TRIG7_ERROR	0, RO/SC	**Trigger 7 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
14	TRIG7_ACTIVE	0, RO/SC	**Trigger 7 Active:** This bit indicates the Trigger is enabled and has not completed.
13	TRIG6_ERROR	0, RO/SC	**Trigger 6 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
12	TRIG6_ACTIVE	0, RO/SC	**Trigger 6 Active:** This bit indicates the Trigger is enabled and has not completed.
11	TRIG5_ERROR	0, RO/SC	**Trigger 5 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
10	TRIG5_ACTIVE	0, RO/SC	**Trigger 5 Active:** This bit indicates the Trigger is enabled and has not completed.
9	TRIG4_ERROR	0, RO/SC	**Trigger 4 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
8	TRIG4_ACTIVE	0, RO/SC	**Trigger 4 Active:** This bit indicates the Trigger is enabled and has not completed.
7	TRIG3_ERROR	0, RO/SC	**Trigger 3 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
6	TRIG3_ACTIVE	0, RO/SC	**Trigger 3 Active:** This bit indicates the Trigger is enabled and has not completed.
5	TRIG2_ERROR	0, RO/SC	**Trigger 2 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
4	TRIG2_ACTIVE	0, RO/SC	**Trigger 2 Active:** This bit indicates the Trigger is enabled and has not completed.
3	TRIG1_ERROR	0, RO/SC	**Trigger 1 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
2	TRIG1_ACTIVE	0, RO/SC	**Trigger 1 Active:** This bit indicates the Trigger is enabled and has not completed.
1	TRIG0_ERROR	0, RO/SC	**Trigger 0 Error:** This bit indicates the Trigger was improperly programmed to trigger at a time prior to the current time. This bit will be cleared when the Trigger is disabled and/ or re-armed.
0	TRIG0_ACTIVE	0, RO/SC	**Trigger 0 Active:** This bit indicates the Trigger is enabled and has not completed.

5.6.1.5.5 PTP Rate Low Register (PTP_RATEL), Page 4

This register contains the low 16-bits of the PTP Rate control. The PTP Rate Control indicates a positive or negative adjustment to the reference clock period in units of 2^{-32} ns. On each reference clock cycle, the PTP Clock will be adjusted by adding REF_CLK_PERIOD +/- PTP_RATE. The PTP Rate should be written as PTP_RATEH, followed by PTP_RATEL. The rate will take effect on the write to the PTP_RATEL register.

Table 5-51. PTP Rate Low Register (PTP_RATEL), Address 0x18

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PTP_RATE_LO	0000 0000 0000 0000, RW	**PTP Rate Low 16-bits:** Writing to this register will set the low 16-bits of the Rate Control value. The Rate Control value is in units of 2^{-32} ns. Upon writing to this register, the full Rate Control value will be loaded to the device.

5.6.1.5.6 PTP Rate High Register (PTP_RATEH), Page 4

This register contains the upper bits of the PTP Rate control. In addition, it contains a direction control to indicate whether the device is operating faster or slower than the reference clock frequency. When setting the PTP Rate, this register should be written first, followed by a write to the PTP_RATEL register. The rate will take effect on the write to the PTP_RATEL register.

Table 5-52. PTP Rate High Register (PTP_RATEH), Address 0x19

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	PTP_RATE_DIR	0, RW	**PTP Rate Direction:** The setting of this bit controls whether the device will operate at a higher or lower frequency than the reference clock. 0 : Higher Frequency. The PTP_RATE value will be added to the clock on every cycle. 1 : Lower Frequency. The PTP_RATE value will be subtracted from the clock on every cycle.
14	PTP_TMP_RATE	0, RW	**PTP Temporary Rate:** Setting this bit will cause the rate to be applied to the clock for the duration set in the PTP Temporary Rate Duration Register (PTP_TRD). 1 : Temporary Rate 0 : Normal Rate
13:10	RESERVED	00 00, RO	**Reserved:** Writes ignored, Read as 0
9:0	PTP_RATE_HI	00 0000 0000, RW	**PTP Rate High 10-bits:** Writing to this register will set the high 10-bits of the Rate Control value. The Rate Control value is in units of 2^{-32} ns.

5.6.1.5.7 PTP Read Checksum (PTP_RDCKSUM), Page 4

This register keeps a running one's complement checksum of 16-bit read data values for valid Page 4 read accesses. Clear the checksum on a read to this register; read data from this register is not accumulated in the read checksum because the register is cleared on read. However, read data from the write checksum register is accumulated to allow cross checking. Checksums are not accumulated for PHY Control Frame register accesses, but are cleared on management or PHY Control Frame reads.

Table 5-53. PTP Read Checksum (PTP_RDCKSUM), Address 0x1A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	RD_CKSUM	XXXX XXXX XXXX XXXX, RO/ COR	PTP Read Checksum.

5.6.1.5.8 PTP Write Checksum (PTP_WRCKSUM), Page 4

This register keeps a running one's complement checksum of 16-bit write data values for Page 4 write accesses. Clear the checksum on a read. Write data to this register or the read checksum register ARE accumulated in the write checksum to allow cross checking. Read data from this register is accumulated in the read checksum to allow cross checking. Checksums are not accumulated for PHY Control Frame register accesses, but are cleared on management or PHY Control Frame reads.

Table 5-54. PTP Write Checksum (PTP_WRCKSUM), Address 0x1B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	WR_CKSUM	XXXX XXXX XXXX XXXX, RO/ COR	PTP Write Checksum.

5.6.1.5.9 PTP Transmit Timestamp Register (PTP_TXTS), Page 4

This register provides a mechanism for reading the Transmit Timestamp. The fields are read in the following order:

- Timestamp_ns [15:0]
- Overflow_cnt[1:0], Timestamp_ns[29:16]
- Timestamp_sec[15:0]
- Timestamp_sec[31:16]

The Overflow_cnt value indicates if timestamps were dropped due to an overflow of the Transmit Timestamp queue. The overflow counter will stick at a value of three if additional timestamps were missed.

Table 5-55. PTP Transmit Timestamp Register (PTP_TXTS), Address 0x1C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PTP_TX_TS	0000 0000 0000 0000, RO	**PTP Transmit Timestamp:** Reading this register will return the Transmit Timestamp in four 16-bit reads.

5.6.1.5.10 PTP Receive Timestamp Register (PTP_RXTS), Page 4

This register provides a mechanism for reading the Receive Timestamp and identification information. The fields are read in the following order:

- Timestamp_ns [15:0]
- Overflow_cnt[1:0], Timestamp_ns[29:16]
- Timestamp_sec[15:0]
- Timestamp_sec[31:16]
- sequenceId[15:0]
- messageType[3:0], source_hash[11:0]

The Overflow_cnt value indicates if timestamps were dropped due to an overflow of the Transmit Timestamp queue. The overflow counter will stick at a value of three if additional timestamps were missed.

Table 5-56. PTP Receive Timestamp Register (PTP_RXTS), Address 0x1D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PTP_RX_TS	0000 0000 0000 0000, RO	**PTP Receive Timestamp:** Reading this register will return the Receive Timestamp in four 16-bit reads.

5.6.1.5.11 PTP Event Status Register (PTP_ESTS), Page 4

This register provides Status for the Event Timestamp unit. Reading this register provides status for the next Event Timestamp contained in the Event Data Register. If this register is 0, no Event Timestamp is available in the Event Data Register. Reading this register will automatically move to the next Event in the queue.

Table 5-57. PTP Event Status Register (PTP_ESTS), Address 0x1E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0000 0, RO	**Reserved:** Writes ignored, Read as 0
10:8	EVNTS_MISSED	000, RO/SC	**Event Missed:** Indicates number of events have been missed prior to this timestamp for the EVNT_NUM indicated. This count value will stick at 7 if more than 7 events are missed.
7:6	EVNT_TS_LEN	00, RO/SC	**Event Timestamp Length:** Indicates length of the Timestamp field in 16-bit words minus 1. Although all fields are available, this indicates how many of the fields contain data different from the previous Event Timestamp. This allows software to avoid reading more significant fields if they have not changed since the previous timestamp. This field is valid for both single and multiple events. The following shows the number of least significant fields which have new data for each setting of TS_LENGTH: 00 : One 16-bit field is new (Timestamp_ns[15:0]) 01 : Two 16-bit fields are new 10 : Three 16-bit fields are new 11 : All four 16-bit fields are new
5	EVNT_RF	0, RO/SC	**Event Rise/Fall direction:** Indicates whether the event is a rise or falling event. If the MULT_EVNT bit is set to 1, this bit indicates the Rise/Fall direction for the event indicated by EVNT_NUM. 0 = Falling edge detected 1 = Rising edge detected
4:2	EVNT_NUM	000, RO/SC	**Event Number:** Indicates Event Timestamp Unit which detected an event. If the MULT_EVNT bit is set to 0, this indicates the lowest event number captured. If events have been missed prior to this timestamp, it indicates the lowest event number captured which had at least one missed event.
1	MULT_EVNT	0, RO/SC	**Multiple Event Detect:** Indicates multiple events were detected at the same time. If multiple events are detected, an extended event status field is available as the first data read from the Event Data Register. 0 = Single event detected 1 = Multiple events detected
0	EVENT_DET	0, RO/SC	**PTP Event Detected:** Indicates an Event has been detected by one of the Event Timestamp Units.

5.6.1.5.12 PTP Event Data Register (PTP_EDATA), Page 4

This register provides a mechanism for reading the Event Timestamp and extended event status. If present, the extended event status is read prior to reading the Event Timestamp. Presence of the Extended Event Status field is indicated by the MULT_EVNT bit in the PTP Event Status Register. The timestamp consists of four 16-bit fields. This register contains a valid timestamp if the PTP_ESTS register indicates an Event Timestamp is available. Not all fields have to be read for each timestamp. For example, if the EVNT_TS_LEN indicates the seconds field has not changed from the previous event, software may skip that read. Reading the PTP_ESTS register will cause the device to move to the next available timestamp.

The fields are read in the following order:

- Extended Event Status[15:0] (only available if PTP_ESTS indicates detection of multiple events)
- Timestamp_ns [15:0]
- Timestamp_ns[29:16] (upper 2 bits are always 0)
- Timestamp_sec[15:0]
- Timestamp_sec[31:16]

For Extended Event Status, the following definition is used for the PTP Event Data Register:

Table 5-58. PTP Event Data Register (PTP_EDATA), Address 0x1F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	E7_RISE	0, RO/SC	**Rise/Fall edge direction for Event 7:** Indicates direction of Event 7 0 = Fall 1 = Rise
14	E7_DET	0, RO/SC	**Event 7 detected:** Indicates Event 7 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.
13	E6_RISE	0, RO/SC	**Rise/Fall edge direction for Event 6:** Indicates direction of Event 6 0 = Fall 1 = Rise
12	E6_DET	0, RO/SC	**Event 6 detected:** Indicates Event 6 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.
11	E5_RISE	0, RO/SC	**Rise/Fall edge direction for Event 5:** Indicates direction of Event 5 0 = Fall 1 = Rise
10	E5_DET	0, RO/SC	**Event 5 detected:** Indicates Event 5 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.
9	E4_RISE	0, RO/SC	**Rise/Fall edge direction for Event 4:** Indicates direction of Event 4 0 = Fall 1 = Rise
8	E4_DET	0, RO/SC	**Event 4 detected:** Indicates Event 4 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.
7	E3_RISE	0, RO/SC	**Rise/Fall edge direction for Event 3:** Indicates direction of Event 3 0 = Fall 1 = Rise
6	E3_DET	0, RO/SC	**Event 3 detected:** Indicates Event 3 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.

Table 5-58. PTP Event Data Register (PTP_EDATA), Address 0x1F (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
5	E2_RISE	0, RO/SC	**Rise/Fall edge direction for Event 2:** Indicates direction of Event 2 0 = Fall 1 = Rise
4	E2_DET	0, RO/SC	**Event 2 detected:** Indicates Event 2 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.
3	E1_RISE	0, RO/SC	**Rise/Fall edge direction for Event 1:** Indicates direction of Event 1 0 = Fall 1 = Rise
2	E1_DET	0, RO/SC	**Event 1 detected:** Indicates Event 1 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.
1	E0_RISE	0, RO/SC	**Rise/Fall edge direction for Event 0:** Indicates direction of Event 0 0 = Fall 1 = Rise
0	E0_DET	0, RO/SC	**Event 0 detected:** Indicates Event 0 detected a rising or falling edge at the time contained in the PTP_EDATA register timestamp.

For timestamp fields, the following definition is used for the PTP Event Data Register:

Table 5-59. PTP Event Data Register (PTP_EDATA), Address 0x1F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PTP_EVNT_TS	XXXX XXXX XXXX XXXX, RO	**PTP Event Timestamp:** Reading this register will return 16 bits of the Event Timestamp.

5.6.1.6 PTP 1588 Configuration Registers - Page 5

Page 5 PTP 1588 Configuration Registers are accessible by setting bits [2:0] = 101 of PAGESEL (13h).

5.6.1.6.1 PTP Trigger Configuration Register (PTP_TRIG), Page 5

This register provides basic configuration for IEEE 1588 Triggers. To write configuration to a Trigger, set the TRIG_WR bit along with the TRIG_SEL and other control information. To read configuration from a Trigger, set the TRIG_SEL encoding to the Trigger desired, and set the TRIG_WR bit to 0. The subsequent read of the PTP_TRIG register will return the configuration information.

Table 5-60. PTP Trigger Configuration Register (PTP_TRIG), Address 0x14

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	TRIG_PULSE	0, RW	**Trigger Pulse:** Setting this bit will cause the Trigger to generate a Pulse rather than a single rising or falling edge.
14	TRIG_PER	0, RW	**Trigger Periodic:** Setting this bit will cause the Trigger to generate a periodic signal. If this bit is 0, the Trigger will generate a single Pulse or Edge depending on the Trigger Control settings.
13	TRIG_IF_LATE	0, RW	**Trigger-if-late Control:** Setting this bit will allow an immediate Trigger in the event the Trigger is programmed to a time value which is less than the current time. This provides a mechanism for generating an immediate trigger or to immediately begin generating a periodic signal. For a periodic signal, no notification be generated if this bit is set and a Late Trigger occurs.
12	TRIG_NOTIFY	0, RW	**Trigger Notification Enable:** Setting this bit will enable Trigger status to be reported on completion of a Trigger or on an error detection due to late trigger. If Trigger interrupts are enabled, the notification will also result in an interrupt being generated.

Table 5-60. PTP Trigger Configuration Register (PTP_TRIG), Address 0x14 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
11:8	TRIG_GPIO	0000, RW	**Trigger GPIO Connection:** Setting this field to a non-zero value will connect the Trigger to the associated GPIO pin. Valid settings for this field are 1 thru 12.
7	TRIG_TOGGLE	0, RW	**Trigger Toggle Mode Enable:** Setting this bit will put the trigger into toggle mode. In toggle mode, the initial value will be ignored and the trigger output will be toggled at the trigger time.
6:4	RESERVED	000, RO	**Reserved:** Writes ignored, Read as 0
3:1	TRIG_CSEL	000, RW	**Trigger Configuration Select:** This field selects the Trigger for configuration read or write.
0	TRIG_WR	0, RW/SC	**Trigger Configuration Write:** Setting this bit will generate a Configuration Write to the selected Trigger. This bit will always read back as 0.

5.6.1.6.2 PTP Event Configuration Register (PTP_EVNT), Page 5

This register provides basic configuration for IEEE 1588 Events. To write configuration to an Event Timestamp Unit, set the EVNT_WR bit along with the EVNT_SEL and other control information. To read configuration from an Event Timestamp Unit, set the EVNT_SEL encoding to the Event desired, and set the EVNT_WR bit to 0. The subsequent read of the PTP_EVNT register will return the configuration information.

Table 5-61. PTP Event Configuration Register (PTP_EVNT), Address 0x15

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**Reserved:** Writes ignored, Read as 0
14	EVNT_RISE	0, RW	**Event Rise Detect Enable:** Enable Detection of Rising edge on Event input.
13	EVNT_FALL	0, RW	**Event Fall Detect Enable:** Enable Detection of Falling edge on Event input.
12	EVNT_SINGLE	0, RW	**Single Event Capture:** Setting this bit to a 1 will enable single event capture operation. The EVNT_RISE and EVNT_FALL enables will be cleared upon a valid event timestamp capture.
11:8	EVNT_GPIO	0000, RW	**Event GPIO Connection:** Setting this field to a non-zero value will connect the Event to the associated GPIO pin. Valid settings for this field are 1 thru 12.
7:4	RESERVED	0000, RO	**Reserved:** Writes ignored, Read as 0
3:1	EVNT_SEL	000, RW	**Event Select:** This field selects the Event Timestamp Unit for configuration read or write.
0	EVNT_WR	0, RW	**Event Configuration Write:** Setting this bit will generate a Configuration Write to the selected Event Timestamp Unit.

5.6.1.6.3 PTP Transmit Configuration Register 0 (PTP_TXCFG0), Page 5

This register provides configuration for IEEE 1588 Transmit Timestamp operation.

Table 5-62. PTP Transmit Configuration Register 0 (PTP_TXCFG0), Address 0x16

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	SYNC_1STEP	0, RW	**Sync Message One-Step Enable:** Enable automatic insertion of timestamp into transmit Sync Messages. Device will automatically parse message and insert the timestamp in the correct location. UPD checksum and CRC fields will be regenerated.
14	RESERVED	0, RO	**Reserved:** Writes ignored, Read as 0
13	DR_INSERT	0, RW	**Insert Delay_Req Timestamp in Delay_Resp:** If this bit is set to a 1, the device insert the timestamp for transmitted Delay_Req messages into inbound Delay_Resp messages. The most recent timestamp will be used for any inbound Delay_Resp message. The receive timestamp insertion logic must be enabled through the PTP Receive Configuration Registers.
12	NTP_TS_EN	0, RW	**Enable Timestamping of NTP Packets:** If this bit is set to 0, the device will check the UDP protocol field for a PTP Event message (value 319). If this bit is set to 1, the device will check the UDP protocol field for an NTP message (value 123). This setting applies to the transmit and receive packet parsing engines.
11	IGNORE_2STEP	0, RW	**Ignore Two_Step flag for One-Step operation:** If this bit is set to a 0, the device will not insert a timestamp if the Two_Step bit is set in the flags field of the PTP header. If this bit is set to 1, the device will insert a timestamp independent of the setting of the Two_Step flag.
10	CRC_1STEP	0, RW	**Disable checking of CRC for One-Step operation:** If this bit is set to a 0, the device will force a CRC error for One-Step operation if the incoming frame has a CRC error. If this bit is set to a 1, the device will send the One- Step frame with a valid CRC, even if the incoming CRC is invalid.
9	CHK_1STEP	0, RW	**Enable UDP Checksum correction for One-Step Operation:** Enables correction of the UDP checksum for messages which include insertion of the timestamp. The checksum is corrected by modifying the last two bytes of the UDP data. The last two bytes must be transmitted by the MAC as 0's. This control must be set for proper IPv6/UDP One-Step operation. This control will have no effect for Layer2 Ethernet messages.
8	IP1588_EN	0, RW	**Enable IEEE 1588 defined IP address filter:** Enable filtering of UDP/IP Event messages using the IANA assigned IP Destination addresses. If this bit is set to 1, packets with IP Destination addresses which do not match the IANA assigned addresses will not be timestamped. This field affects operation for both IPv4 and IPv6. If this field is set to 0, IP destination addresses will be ignored.
7	TX_L2_EN	0, RW	**Layer2 Timestamp Enable:** Enables detection of IEEE 802.3/Ethernet encapsulated PTP event messages.
6	TX_IPV6_EN	0, RW	**IPv6 Timestamp Enable:** Enables detection of UDP/IPv6 encapsulated PTP event messages.
5	TX_IPV4_EN	0, RW	**IPv4 Timestamp Enable:** Enables detection of UDP/IPv4 encapsulated PTP event messages.
4:1	TX_PTP_VER	0 000, RW	**PTP Version:** Enable Timestamp capture for a specific version of the IEEE 1588 specification. This field may be programmed to any value between 1 and 15 and allows support for future versions of the IEEE 1588 specification. A value of 0 will disable version checking (not recommended).
0	TX_TS_EN	0, RW	**Transmit Timestamp Enable:** Enable Timestamp capture for Transmit.

5.6.1.6.4 PTP Transmit Configuration Register 1 (PTP_TXCFG1), Page 5

This register provides data and mask fields to filter the first byte in a PTP Message. This function will be disabled if all the mask bits are set to 0.

Table 5-63. PTP Transmit Configuration Register 1 (PTP_TXCFG1), Address 0x17

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	BYTE0_MASK	0000 0000, RW	**Byte0 Data:** Bit mask to be used for matching Byte0 of the PTP Message. A one in any bit enables matching for the associated data bit. If no matching is required, all bits of the mask should be set to 0.
7:0	BYTE0_DATA	0000 0000, RW	**Byte0 Mask:** Data to be used for matching Byte0 of the PTP Message.

5.6.1.6.5 PHY Status Frame Configuration Register 0 (PSF_CFG0), Page 5

This register provides configuration for the PHY Status Frame function.

Table 5-64. PHY Status Frame Configuration Register 0 (PSF_CFG0), Address 0x18

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	RESERVED	000, RO	**Reserved:** Writes ignored, Read as 0
12:11	MAC_SRC_ADD	0 0, RW	**PHY Status Frame Mac Source Address:** Selects source address as follows: 00 : Use Mac Address [08 00 17 0B 6B 0F] 01 : Use Mac Address [08 00 17 00 00 00] 10 : Use Mac Multicast Dest Address 11 : Use Mac Address [00 00 00 00 00 00]
10:8	MIN_PRE	000, RW	**PHY Status Frame Minimum Preamble:** Determines the minimum preamble bytes required for sending packets on the MII interface. It is recommended that this be set to the smallest value the MAC will tolerate.
7	PSF_ENDIAN	0, RW	**PHY Status Frame Endian Control:** For each 16-bit field in a Status Message, the data will normally be presented in network byte order (Most significant byte first). If this bit is set to a 1, the byte data fields will be reversed so that the least significant byte is first.
6	PSF_IPV4	0, RW	**PHY Status Frame IPv4 Enable:** This bit controls the type of packet used for PHY Status Frames. 0 = Layer2 Ethernet packets 1 = IPv4 packets.
5	PSF_PCF_RD	0, RW	**PHY Control Frame Read PHY Status Frame Enable:** Enable PHY Status Frame delivery of PHY Control Frame read data. Data read through a PHY Control Frame will be returned in a PHY Status Frame.
4	PSF_ERR_EN	0, RW	**PSF Error PHY Status Frame Enable:** Enable PHY Status Frame delivery of PHY Status Frame Errors. This bit will not independently enable PHY Status Frame operation. One of the other enable bits must be set for PHY Status Frames to be generated.
3	PSF_TXTS_EN	0, RW	**Transmit Timestamp PHY Status Frame Enable:** Enable PHY Status Frame delivery of Transmit Timestamps.
2	PSF_RXTS_EN	0, RW	**Receive Timestamp PHY Status Frame Enable:** Enable PHY Status Frame delivery of Receive Timestamps.
1	PSF_TRIG_EN	0, RW	**Trigger PHY Status Frame Enable:** Enable PHY Status Frame delivery of Trigger Status.
0	PSF_EVNT_EN	0, RW	**Event PHY Status Frame Enable:** Enable PHY Status Frame delivery of Event Timestamps.

5.6.1.6.6 PTP Receive Configuration Register 0 (PTP_RXCFG0), Page 5,

This register provides configuration for IEEE 1588 Receive Timestamp operation.

Table 5-65. PTP Receive Configuration Register 0 (PTP_RXCFG0), Address 0x19

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	DOMAIN_EN	0, RW	**Domain Match Enable:** If set to 1, the Receive Timestamp unit will require the Domain field to match the value programmed in the PTP_DOMAIN field of the PTP_RXCFG3 register. If set to 0, the Receive Timestamp will ignore the PTP_DOMAIN field.
14	ALT_MAST_DIS	0, RW	**Alternate Master Timestamp Disable:** Disables timestamp generation if the Alternate_Master flag is set: 1 = Do not generate timestamp if Alternate_Master = 1 0 = Ignore Alternate_Master flag
13	USER_IP_SEL	0, RW	**IP Address data select:** Selects portion of IP address accessible through the PTP_RXCFG2 register: 0 = Most Significant Octets 1 = Least Significant Octets
12	USER_IP_EN	0, RW	**Enable User-programmed IP address filter:** Enable detection of UDP/IP Event messages using a programmable IP addresses. The IP Address is set using the PTP_RXCFG2 register.
11	RX_SLAVE	0, RW	**Receive Slave Only:** By default, the Receive Timestamp Unit will provide Timestamps for event messages meeting other requirements. Setting this bit to a 1 will prevent Delay_Req messages from being Timestamped by requiring that the Control Field (offset 32 in the PTP message) be set to a value other than 1.
10:8	IP1588_EN	000, RW	**Enable IEEE 1588 defined IP address filters:** Enable detection of UDP/IP Event messages using the IANA assigned IP Destination addresses. This field affects operation for both IPv4 and IPv6. A Timestamp is captured for the PTP message if the IP destination address matches the following: IP1588_EN[0]: Dest IP address = 224.0.1.129 IP1588_EN[1]: Dest IP address = 224.0.1.130-132 IP1588_EN[2]: Dest IP address = 224.0.0.107
7	RX_L2_EN	0, RW	**Layer2 Timestamp Enable:** Enables detection of IEEE 802.3/Ethernet encapsulated PTP event messages.
6	RX_IPV6_EN	0, RW	**IPv6 Timestamp Enable:** Enables detection of UDP/IPv6 encapsulated PTP event messages.
5	RX_IPV4_EN	0, RW	**IPv4 Timestamp Enable:** Enables detection of UDP/IPv4 encapsulated PTP event messages.
4:1	RX_PTP_VER	0 000, RW	**PTP Version:** Enable Timestamp capture for a specific version of the IEEE 1588 specification. This field may be programmed to any value between 1 and 15 and allows support for future versions of the IEEE 1588 specification. A value of 0 will disable version checking (not recommended).
0	RX_TS_EN	0, RW	**Receive Timestamp Enable:** Enable Timestamp capture for Receive.

5.6.1.6.7 PTP Receive Configuration Register 1 (PTP_RXCFG1), Page 5

This register provides data and mask fields to filter the first byte in a PTP Message. This function will be disabled if all the mask bits are set to 0.

Table 5-66. PTP Receive Configuration Register 1 (PTP_RXCFG1), Address 0x1A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	BYTE0_MASK	0000 0000, RW	**Byte0 Data:** Bit mask to be used for matching Byte0 of the Receive PTP Message. A one in any bit enables matching for the associated data bit. If no matching is required, all bits of the mask should be set to 0.
7:0	BYTE0_DATA	0000 0000, RW	**Byte0 Mask:** Data to be used for matching Byte0 of the Receive PTP Message.

5.6.1.6.8 PTP Receive Configuration Register 2 (PTP_RXCFG2), Page 5

This register provides for programming an IP address to be used for filtering packets to detect PTP Event Messages. Because the IPv4 address is 32-bits, to write an IP address, software must write two 16-bit values. The USER_IP_SEL bit in the PTP_RXCFG0 register selects which octects of the IP address are accessible through this register. For example, to write an IP address of 224.0.1.129, software should do the following:

1. Set USER_IP_SEL bit in PTP_RXCFG0 register to 0
2. Write 0xE000 (224.00) to PTP_RXCFG2
3. Set USER_IP_SEL bit in the PTP_RXCFG0 register to 1
4. Write 0x0181 (01.129) to PTP_RXCFG2

Reading this registerwill return the IP address field selected by USER_IP_SEL.

Table 5-67. PTP Receive Configuration Register 2 (PTP_RXCFG2), Address 0x1B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	IP_ADDR_DATA	0000 0000 0000 0000, RW	**Receive IP Address Data:** 16-bits of the IP Address field to be read or written. The USER_IP_SEL bit in the PTP_RXCFG0 Register selects the portion of the IP address is to be read or written.

5.6.1.6.9 PTP Receive Configuration Register 3 (PTP_RXCFG3), Page 5

This register provides extended configuration for IEEE 1588 Receive Timestamp operation.

Table 5-68. PTP Receive Configuration Register 3 (PTP_RXCFG3), Address 0x1C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	TS_MIN_IFG	1100, RW	**Minimum Inter-frame Gap:** When a Timestamp is appended to a PTP Message, the length of the packet may get extended. This could reduce the Inter-frame Gap (IFG) between packets by as much as 8 byte times (640 ns at 100 Mb). This field sets a minimum on the IFG between packets in number of byte times. If the IFG is set larger than the actual IFG, preamble bytes of the subsequent packet will get dropped. This value should be set to the lowest possible value that the attached MAC can support.
11	ACC_UDP	0, RW	**Record Timestamp if UDP Checksum Error:** By default, Timestamps will be discarded for packets with UDP Checksum errors. If this bit is set, then the Timestamp will be made available in the normal manner.
10	ACC_CRC	0, RW	**Record Timestamp if CRC Error:** By default, Timestamps will be discarded for packets with CRC errors. If this bit is set, then the Timestamp will be made available in the normal manner.
9	TS_APPEND	0, RW	**Append Timestamp for L2:** For Layer 2 encapsulated PTP messages, if this bit is set, always append the Timestamp to end of the PTP message rather than inserted in unused message fields. This bit will be ignored if TS_INSERT is 0.
8	TS_INSERT	0, RW	**Enable Timestamp Insertion:** Enables Timestamp insertion into a packet containing a PTP Event Message. If this bit is set, the Timestamp will not be available through the PTP Receive Timestamp Register.
7:0	PTP_DOMAIN	0000 0000, RW	**PTP Domain:** Value of the PTP Message domainNumber field. If PTP_RXCFG0:DOMAIN_EN is set to 1, the Receive Timestamp unit will only capture a Timestamp if the domainNumber in the receive PTP message matches the value in this field. If the DOMAIN_EN bit is set to 0, the domainNumber field will be ignored.

5.6.1.6.10 PTP Receive Configuration Register 4 (PTP_RXCFG4), Page 5

This register provides extended configuration for IEEE 1588 Receive Timestamp operation.

Table 5-69. PTP Receive Configuration Register 4 (PTP_RXCFG4), Address 0x1D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	IPV4_UDP_MOD	0, RW	**Enable IPV4 UDP Modification:** When timestamp insertion is enabled, this bit controls how UDP checksums are handled for IPV4 PTP event messages. If set to a 0, the device will clear the UDP checksum. If a UDP checksum error is detected the device will force a CRC error. If set to a 1, the device will not clear the UDP checksum. Instead it will generate a 2-byte value to correct the UDP checksum and append this immediately following the PTP message. If an incoming UDP checksum error is detected, the device will cause a UDP checksum error in the modified field. This function should only be used if the incoming packets contain two extra bytes of UDP data following the PTP message. This should not be enabled for systems using version 1 of the IEEE 1588 specification.
14	TS_SEC_EN	0, RW	**Enable Timestamp Seconds:** Setting this bit to a 1 enables inserting a seconds field when Timestamp Insertion is enabled. If set to 0, only the nanoseconds portion of the Timestamp will be inserted in the packet. This bit will be ignored if TS_INSERT is 0.
13:12	TS_SEC_LEN	00, RW	**Inserted Timestamp Seconds Length:** This field indicates the length of the Seconds field to be inserted in the PTP message. This field will be ignored if TS_INSERT is 0 or if TS_SEC_EN is 0. The mapping is as follows: 00 : Least Significant Byte only of Seconds field 01 : Two Least Significant Bytes of Seconds field 10 : Three Least Significant Bytes of Seconds field 11 : All four Bytes of Seconds field
11:6	RXTS_NS_OFF	0000 00, RW	**Receive Timestamp Nanoseconds offset:** This field provides an offset to the Nanoseconds field when inserting a Timestamp into a received PTP message. If TS_APPEND is set to 1, the offset indicates an offset from the end of the PTP message. If TS_APPEND is set to 0, the offset indicates the byte offset from the beginning of the PTP message. This field will be ignored if TS_INSERT is 0.
5:0	RXTS_SEC_OFF	00 0000, RW	**Receive Timestamp Seconds offset:** This field provides an offset to the Seconds field when inserting a Timestamp into a received PTP message. If TS_APPEND is set to 1, the offset indicates an offset from the end of the inserted Nanoseconds field. If TS_APPEND is set to 0, the offset indicates the byte offset from the beginning of the PTP message. This field will be ignored if TS_INSERT is 0.

5.6.1.6.11 PTP Temporary Rate Duration Low Register (PTP_TRDL), Page 5

This register contains the low 16 bits of the duration in clock cycles to use the Temporary Rate as programmed in the PTP_RATEH and PTP_RATEL registers. Because the Temporary Rate takes affect upon writing the PTP_RATEL register, this register should be programmed before setting the Temporary Rate. This register does not need to be reprogrammed for each use of the Temporary Rate registers.

Table 5-70. PTP Temporary Rate Duration Low Register (PTP_TRDL), Address 0x1E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PTP_TR_DURL	0000 0000 0000 0000, RW	**PTP Temporary Rate Duration Low 16 bits:** This register sets the duration for the Temporary Rate in number of clock cycles. The actual Time duration is dependent on the value of the Temporary Rate.

5.6.1.6.12 PTP Temporary Rate Duration High Register (PTP_TRDH), Page 5

This register contains the high 10 bits of the duration in clock cycles to use the Temporary Rate as programmed in the PTP_RATEH and PTP_RATEL registers. Because the Temporary Rate takes affect upon writing the PTP_RATEL register, this register should be programmed before setting the Temporary Rate. This register does not need to be reprogrammed for each use of the Temporary Rate registers.

Table 5-71. PTP Temporary Rate Duration High Register (PTP_TRDH), Address 0x1F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	RESERVED	0000 00, RO	**Reserved:** Writes ignored, Read as 0
9:0	PTP_TR_DURH	00 0000 0000, RW	**PTP Temporary Rate Duration High 10 bits:** This register sets the duration for the Temporary Rate in number of clock cycles. The actual Time duration is dependent on the value of the Temporary Rate.

5.6.1.7 PTP 1588 Configuration Registers - Page 6

Page 6 PTP 1588 Configuration Registers are accessible by setting bits [2:0] = 110 of PAGESEL (13h).

5.6.1.7.1 PTP Clock Output Control Register (PTP_COC), Page 6

This register provides configuration for the PTP clock-synchronized output divide-by-N clock.

Table 5-72. PTP Clock Output Control Register (PTP_COC), Address 0x14

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	PTP_CLKOUT EN	1, RW	**PTP Clock Output Enable:** 1 = Enable PTP divide-by-N clock output. 0 = Disable PTP divide-by-N clock output.
14	PTP_CLKOUT SEL	0, RW	**PTP Clock Output Source Select:** 1 = Select the Phase Generation Module (PGM) as the root clock for generating the divide-by-N output. 0 = Select the Frequency-Controlled Oscillator (FCO) as the root clock for generating the divide-by-N output. For additional information related to the PTP clock output selection, refer to application note AN–1729(SNLA099).
13	PTP_CLKOUT SPEEDSEL	0, RW	**PTP Clock Output I/O Speed Select:** 1 = Enable faster rise/fall time for the divide-by-N clock output pin. 0 = Enable normal rise/fall time for the divide-by-N clock output pin.
12:8	RESERVED	0 0000, RO	**Reserved:** Writes ignored, Read as 0
7:0	PTP_CLKDIV	0000 1010, RW	**PTP Clock Divide-by Value:** This field sets the divide-by value for the output clock. The output clock is divided from an internal 250 MHz clock. Valid values range from 2 to 255 (0x02 to 0xFF), giving a nominal output frequency range of 125 MHz down to 980.4 kHz. Divide-by values of 0 and 1 are not valid and will stop the output clock.

5.6.1.7.2 PHY Status Frame Configuration Register 1 (PSF_CFG1), Page 6

This register provides configuration for the PHY Status Frame function. Specifically, the 16-bit value in this register is used as the first 16-bits of the PTP Header data for the PHY Status Frame.

Table 5-73. PHY Status Frame Configuration Register 1 (PSF_CFG1), Address 0x15

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	PTPRESERVED	0000, RW	**PTP v2 reserved field:** This field contains the reserved 4-bit field (at offset 1) to be sent in status packets from the PHY to the local MAC using the MII receive data interface.
11:8	VERSIONPTP	0000, RW	**PTP v2 versionPTP field:** This field contains the versionPTP field to be sent in status packets from the PHY to the local MAC using the MII receive data interface.
7:4	TRANSPORT-SPECIFIC	0000, RW	**PTP v2 Header transportSpecific field:** This field contains the MESSAGETYPE field to be sent in status packets from the PHY to the local MAC using the MII receive data interface.
3:0	MESSAGETYPE	0000, RW	**PTP v2 messageType field:** This field contains the MESSAGETYPE field to be sent in status packets from the PHY to the local MAC using the MII receive data interface.

5.6.1.7.3 PHY Status Frame Configuration Register 2 (PSF_CFG2), Page 6

This register provides configuration for the PHY Status Frame function. Specifically, the 16-bit value in this register is used as the first 16-bits of the IP Source address for an IPv4 PHY Status Frame.

Table 5-74. PHY Status Frame Configuration Register 2 (PSF_CFG2), Address 0x16

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	IP_SA_BYTE1	0000 0000, RW	**Second byte of IP source address:** This field contains the second byte of the IP source address.
7:0	IP_SA_BYTE0	0000 0000, RW	**First byte of IP source address:** This field contains the most significant byte of the IP source address.

5.6.1.7.4 PHY Status Frame Configuration Register 3 (PSF_CFG3), Page 6

This register provides configuration for the PHY Status Frame function. Specifically, the 16-bit value in this register is used as the second 16-bits of the IP Source address for an IPv4 PHY Status Frame.

Table 5-75. PHY Status Frame Configuration Register 3 (PSF_CFG3), Address 0x17

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	IP_SA_BYTE3	0000 0000, RW	**Fourth byte of IP source address:** This field contains the fourth byte of the IP source address.
7:0	IP_SA_BYTE2	0000 0000, RW	**Third byte of IP source address:** This field contains the third byte of the IP source address.

5.6.1.7.5 PHY Status Frame Configuration Register 4 (PSF_CFG4), Page 6

This register provides configuration for the PHY Status Frame function. Specifically, the 16-bit value in this register is used to assist in computation of the IP checksum for an IPv4 PHY Status Frame.

Table 5-76. PHY Status Frame Configuration Register 4 (PTP_PKTSTS4), Address 0x18

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	IP_CHKSUM	0000 0000 0000 0000, RW	**IP Checksum:** This field contains a precomputed value ones-complement addition of all fixed values in the IP Header. The device will add the Total Length and Identification values to generate the final checksum.

5.6.1.7.6 PTP SFD Configuration Register (PTP_SFDCFG), Page 6

This register provides configuration to enable outputting the RX and TX Start-of-Frame (SFD) signals on GPIO pins. Note that GPIO assignments are not exclusive.

Table 5-77. PTP SFD Configuration Register (PTP_SFDCFG), Address 0x19

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0000 0000, RO	**Reserved:** Writes ignored, Read as 0
7:4	TX_SFD_GPIO	0000, RW	**TX SFD GPIO Select:** This field controls the GPIO output to which the TX SFD signal is assigned. Valid values are 0 (disabled) or 1-12.
3:0	RX_SFD_GPIO	0000, RW	**RX SFD GPIO Select:** This field controls the GPIO output to which the RX SFD signal is assigned. Valid values are 0 (disabled) or 1-12.

5.6.1.7.7 PTP Interrupt Control Register (PTP_INTCTL), Page 6

This register provides configuration for the IEEE 1588 interrupt function, allowing the PTP Interrupt to use any of the GPIO pins.

Table 5-78. PTP Interrupt Control Register (PTP_INTCTL), Address 0x1A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	0000 0000 0000, RO	**Reserved:** Writes ignored, Read as 0
3:0	PTP_INT_GPIO	0000, RW	**PTP Interrupt GPIO Select:** To enable interrupts on a GPIO pin, this field should be set to the GPIO number. Setting this field to 0 will disable interrupts through the GPIO pins.

5.6.1.7.8 PTP Clock Source Register (PTP_CLKSRC), Page 6

This register provides configuration for the reference clock source driving the IEEE 1588 logic. The source clock period is also used by the 1588 clock nanoseconds adder to add the proper value every reference clock cycle.

Table 5-79. PTP Clock Source Register (PTP_CLKSRC), Address 0x1B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	CLK_SRC	00, RW	**PTP Clock Source Select:** Selects among three possible sources for the PTP reference clock: 00 : 125 MHz from internal PGM (default) 01 : Divide-by-N from 125-MHz internal PGM 1x : External reference clock
13:7	RESERVED	00 0000 0, RO	**Reserved:** Writes ignored, Read as 0
6:0	CLK_SRC_PER	000 0000, RW	**PTP Clock Source Period:** This field configures the PTP clock source period in nanoseconds. Values less than 8 are invalid and cannot be written; attempting to write a value less than 8 will cause CLK_SRC_PER to be 8. When the clock source selection is the Divide-by-N from the internal PGM, bits 6:3 are used as the N value; bits 2:0 are ignored in this mode.

5.6.1.7.9 PTP Ethernet Type Register (PTP_ETR), Page 6

This register provides the Ethernet Type (Ethertype) field for PTP transport over Ethernet (Layer2).

Table 5-80. PTP Ethernet Type Register (PTP_ETR), Address 0x1C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PTP_ETYPE	1111 0111 1000 1000, RW	**PTP Ethernet Type:** This field contains the Ethernet Type field used to detect PTP messages transported over Ethernet layer 2.

5.6.1.7.10 PTP Offset Register (PTP_OFF), Page 6

This register provides the byte offset to the PTP message in a Layer2 Ethernet frame.

Table 5-81. PTP Offset Register (PTP_OFF), Address 0x1D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0000 0000, RO	**Reserved:** Writes ignored, Read as 0
7:0	PTP_OFFSET	0000 0000, RO	**PTP Offset:** This field contains the offset in bytes to the PTP Message from the preceding header. For Layer2, this is the offset from the Ethernet Type Field. For UDP/IP, it is the offset from the end of the UDP Header.

5.6.1.7.11 PTP GPIO Monitor Register (PTP_GPIOMON), Page 6

This register provides read-only access to the current values on GPIO inputs.

Table 5-82. PTP GPIO Monitor Register (PTP_GPIOMON), Address 0x1E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0000, RO	**Reserved:** Writes ignored, Read as 0
11:0	PTP_GPIO_IN	0000 0000 0000, RO	**PTP GPIO Inputs:** This field reflects the current values seen on the GPIO inputs. GPIOs 12 through 1 are mapped to bits 11:0 in order.

5.6.1.7.12 PTP Receive Hash Register (PTP_RXHASH), Page 6

This register provides configuration for the source identity hash filter of the PTP receive packet parser. If enabled, the receive parse logic will deliver a receive timestamp only if the hash function on the ten octet sourcePortIdentity field correctly matches the programmed value. The source identity hash filter does not affect timestamp insertion.

Table 5-83. PTP Receive Hash Register (PTP_RXHASH), Address 0x1F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	RESERVED	000, RO	**Reserved:** Writes ignored, Read as 0
12	RX_HASH_EN	0, RW	**Receive Hash Enable:** Enables filtering of PTP messages based on the hash function on the ten octet sourcePortIdentity field.
11:0	PTP_RX_HASH	0000 0000 0000, RW	**Receive Hash:** This field contains the expected source identity hash value for incoming PTP event messages.

6 Application, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The DP83640 provides advanced and flexible support for IEEE 1588 for use in a highly-accurate IEEE 1588 system. It provides a 1588 digital clock implementation, IEEE 1588 Transmit and Receive packet parsing and Start-of-Frame detection, Transmit and Receive Timestamp units, trigger generation, event timestamp unit and a Pulse-Per-Second (PPS) generator.

6.1.1 Key IEEE 1588 Features

IEEE 1588 provides a time synchronization protocol, often referred to as the Precision Time Protocol (PTP), which synchronizes time across an Ethernet network. DP83640 supports IEEE 1588 Real Time Ethernet applications by providing hardware support for three time-critical elements.

- IEEE 1588 synchronized clock generation
- Packet timestamps for clock synchronization
- Event triggering and timestamping through GPIO

By combining the above capabilities, the DP83640 provides advanced and flexible support for IEEE 1588 for use in a highly-accurate IEEE 1588 system.

The DP83640 provides features for controlling the clock operation in Slave mode. The clock value can be updated to match the Master clock in several ways. In addition, the clock can be programmed to adjust its frequency to compensate for drift.

The DP83640 supports real time triggering activities and captures real time events to report to the microcontroller. Controlled devices can be connected to the DP83640 through the available GPIO.

The IEEE 1588 features are briefly presented below. For a more detailed discussion on configuring the IEEE 1588 features, refer to the Software Development Guide for the DP83640.

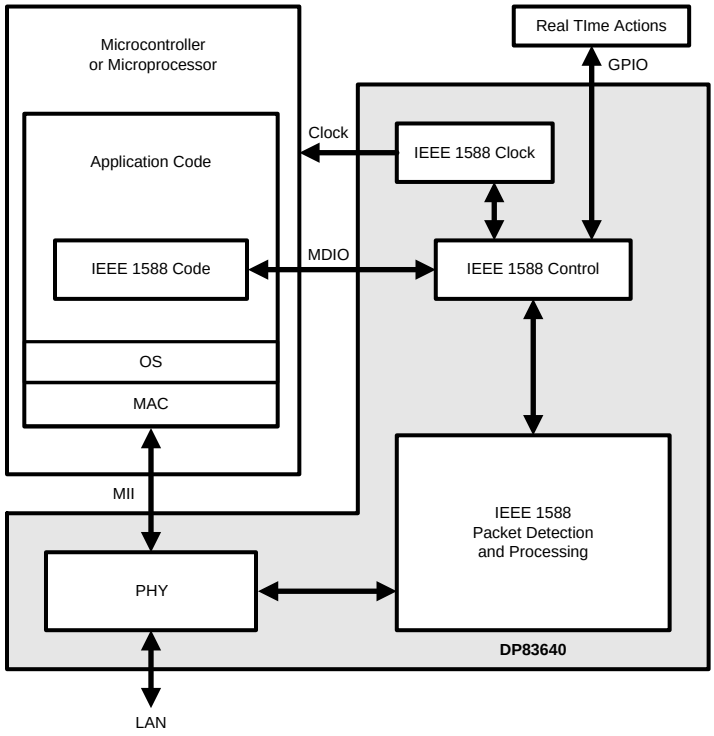


Figure 6-1. DP83640 Example System Application

6.1.1.1 IEEE 1588 Synchronized Clock

The DP83640 provides several mechanisms for updating the IEEE 1588 clock based on the synchronization protocol required:

- Directly Read/Writable
- Adjustable by Add/Subtract
- Frequency Scalable
- Temporary Frequency Control

The clock consists of the following fields: Seconds (32–bit field), Nanoseconds (30–bit field), and Fractional Nanoseconds (units of 2^{-32} ns).

A direct set of the time value can be done by setting a new time value. A step adjustment value in nanoseconds may be added to the current value. Note that the adjustment value can be positive or negative.

The clock can be programmed to operate at an adjusted frequency value by programming a rate adjustment value. The clock can also be programmed to perform a temporary adjusted frequency value by including a rate adjustment duration. The rate adjustment allows for correction on the order of 2^{-32} ns per reference clock cycle. The frequency adjustment will allow the clock to correct the offset over time, avoiding any potential side-effects caused by a step adjustment in the time value.

The method used to update the clock value may depend on the difference in the values. For example, at the initial synchronization attempt, the clocks may be very far apart, and therefore require a step adjustment or a direct time set. Later, when clocks are very close in value, the temporary rate adjustment method may be the best option.

The clock does not support negative time values. If negative time is required in the system, software will have to make conversions from the PHY clock time to actual time.

The clock also does not support the upper 16-bits of the seconds field as defined by the specification (Version 2 specifies a 48-bit seconds field). If this value is required to be greater than 0, it will have to be handled by software. Because a rollover of the seconds field only occurs every 136 years, it should not be a significant burden to software.

6.1.1.1.1 IEEE 1588 Clock Output

The DP83640 provides for a synchronized clock signal for use by external devices. The output clock signal can be any frequency generated from 250 MHz divided by n, where n is an integer in the range of 2 to 255. This provides nominal frequencies from 125 MHz down to 980.4 kHz. The clock output signal is controlled by the PTP_COC register. The output clock signal is generated using the rate information in the PTP_RATE registers and is therefore frequency accurate to the 1588 clock time of the device. In addition, if clock time adjustments are made using the Temporary Rate capabilities, then all time adjustments will be tracked by the output clock signal as well. Note that any step adjustment in the 1588 clock time will not be accurately represented on the 1588 clock output signal.

6.1.1.1.2 IEEE 1588 Clock Input

The IEEE 1588 PTP logic operates on a nominal 125-MHz reference clock generated by an internal Phase Generation Module (PGM). However, options are available to use a divided-down version of the PGM clock to reduce power consumption at the expense of precision, or to use an external reference clock of up to 125 MHz in the event the 1588 clock is tracked externally.

6.1.1.2 Packet Timestamps

6.1.1.2.1 IEEE 1588 Transmit Packet Parser and Timestamp

The IEEE 1588 transmit parser monitors transmit packet data to detect IEEE 1588 Version 1 and Version 2 Event messages. The transmit parser can detect PTP Event messages transported directly in Layer2 Ethernet packets as well as in UDP/IPv4 and UDP/IPv6 packets. Upon detection of a PTP Event Message, the device will capture the transmit timestamp and provide it to software.

Because software knows the order of packet transmission, only the timestamp is recorded (there is no need to record sequence number or other information). The device can buffer four timestamps.

If enabled, an interrupt may be generated upon a Transmit Timestamp Ready.

6.1.1.2.1.1 One-Step Operation

In some cases, the transmitter can be set to operate in a One-Step mode. For Sync Messages, a One-Step device can automatically insert timestamp information in the outgoing packet. This eliminates the need for software to read the timestamp and send a follow up message.

6.1.1.2.2 IEEE 1588 Receive Packet Parser and Timestamp

The IEEE 1588 receive parser monitors receive packet data to detect IEEE 1588 Version 1 and Version 2 Event messages. The receive parser can detect PTP Event messages transported directly in Ethernet packets as well as in UDP/IPv4 and UDP/IPv6 packets. Upon detection of a PTP Event message, the device will capture the receive timestamp and provide the timestamp value to software. In addition to the timestamp, the device will record the 16-bit SequenceId, the 4-bit messageType field, and generate a 12-bit hash value for octets 20-29 of the PTP event message. The device can buffer four timestamps.

An interrupt will be generated, if enabled, upon a Receive Timestamp Ready.

6.1.1.2.2.1 Receive Timestamp Insertion

The DP83640 can deliver the timestamp to software by inserting the timestamp in the received packet. This allows for a simple method to deliver the packet to software without having to match the timestamp to the correct packet. This also eliminates the need to read the receive timestamp through the Serial Management Interface.

6.1.1.2.3 NTP Packet Timestamp

The DP83640 may be programmed to timestamp NTP packets instead of PTP packets. This operation is enabled by setting the NTP_TS_EN control in the PTP_TXCFG0 register. When configured for NTP timestamps, the DP83640 will timestamp packets with the NTP UDP port number rather than the PTP port number (note that the device cannot be configured to timestamp both PTP and NTP packets). One-Step operation is not supported for NTP timestamps, so transmit timestamps cannot be inserted directly into outgoing NTP packets. Timestamp insertion is available for receive timestamps but must use a single, fixed location.

6.1.1.3 Event Triggering and Timestamping

6.1.1.3.1 IEEE 1588 Event Triggering

The DP83640 is capable of being programmed to generate a trigger signal on an output pin based on the IEEE 1588 time value. Each trigger can be programmed to generate a one-time rising or falling edge, a single pulse of programmable width, or a periodic signal.

For each trigger, the microcontroller specifies the desired GPIO and time that the activity is to occur. The trigger is generated when the internal IEEE 1588 clock matches the desired activation time.

The device supports up to 8 trigger signals which can be output on any of the GPIO signal pins. Multiple triggers may be assigned to a single GPIO, allowing generation of more complex waveforms (that is, a sequence of varying width pulses). The trigger signals are OR'ed together to form a combined signal.

The triggers are configured through the PTP Trigger Configuration Registers. The trigger time and width settings are controlled through the PTP Control and Time Data registers.

The DP83640 can be programmed to output a Pulse-Per-Second (PPS) signal using the trigger functions.

6.1.1.3.2 IEEE 1588 Event Timestamping

The DP83640 can be programmed to timestamp an event by monitoring an input signal. The event can be monitored for rising edge, falling edge, or either. The Event Timestamp Unit can monitor up to eight events which can be set to any of the GPIO signal pins. PTP event timestamps are stored in a queue which allows storage of up to eight timestamps.

When an event timestamp is available, the device will set the EVENT_RDY bit in the PTP Status Register. The PTP Event Status Register (PTP_ESTS) provides detailed information on the next available event timestamp, including information on the event number, rise/fall direction, and indication of events missed due to overflow of the devices Event queue.

Event timestamp values should be adjusted by 35 ns (3 times period of the IEEE 1588 reference clock frequency of 125 MHz + 11 ns) to compensate for input path and synchronization delays.

The Event Timestamp Unit is configured through the PTP Event Configuration Register (PTP_EVNT).

6.1.1.4 PTP Interrupts

The PTP module may interrupt the system using the PWRDOWN/INTN pin on the device, shared with other interrupts from the PHY. As an alternative, the device may be programmed to use a GPIO pin to generate PTP interrupts separate from other PHY interrupts.

6.1.1.5 GPIO

The DP83640 features 12 IEEE 1588 GPIO pins. These GPIO pins allow for event monitoring, triggering, interrupts, and a clock output. The LED pins comprise 3 of the 12 GPIO pins. If an LED pin is to be used as a GPIO, its LED function must be disabled prior to configuring the GPIO function.

6.2 Typical Application

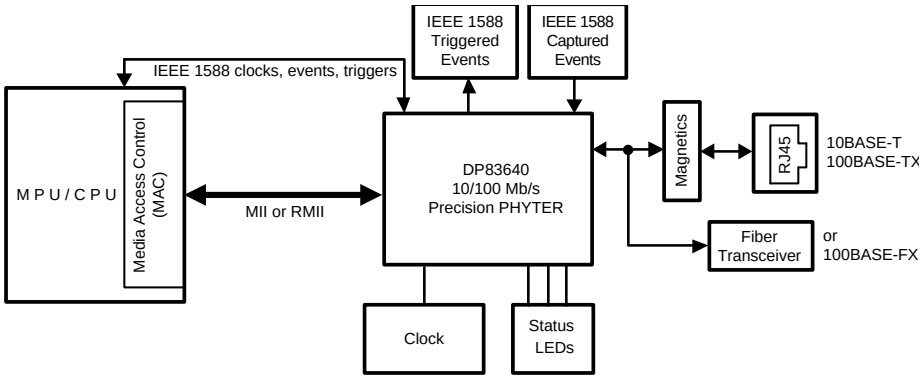


Figure 6-2. Typical Application Schematic

6.2.1 Design Requirements

The design requirements for DP83640 are:

- ANA33VDD = 3.3 V
- IO_VDD = 3.3 V or 2.5 V
- Clock Input = 25 MHz for MII and 50 MHz for RMII

6.2.1.1 TPI Network Circuit

Figure 6-3 shows the recommended circuit for a 10/100 Mb/s twisted-pair interface.

Below is a partial list of recommended transformers. It is important that the user realize that variations with PCB and component characteristics requires that the application be tested to ensure that the circuit meets the requirements of the intended application.

- Pulse H1102
- Pulse H2019
- Pulse J0011D21
- Pulse J0011D21B

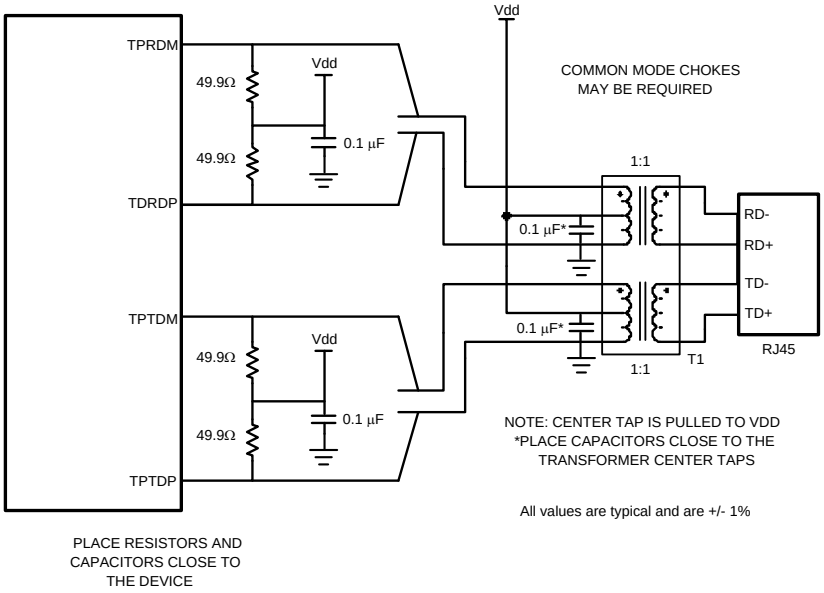


Figure 6-3. 10/100 Mb/s Twisted-Pair Interface

6.2.1.2 Fiber Network Circuit

Figure 6-4 shows the recommended circuit for a 100 Mb/s fiber-pair interface.

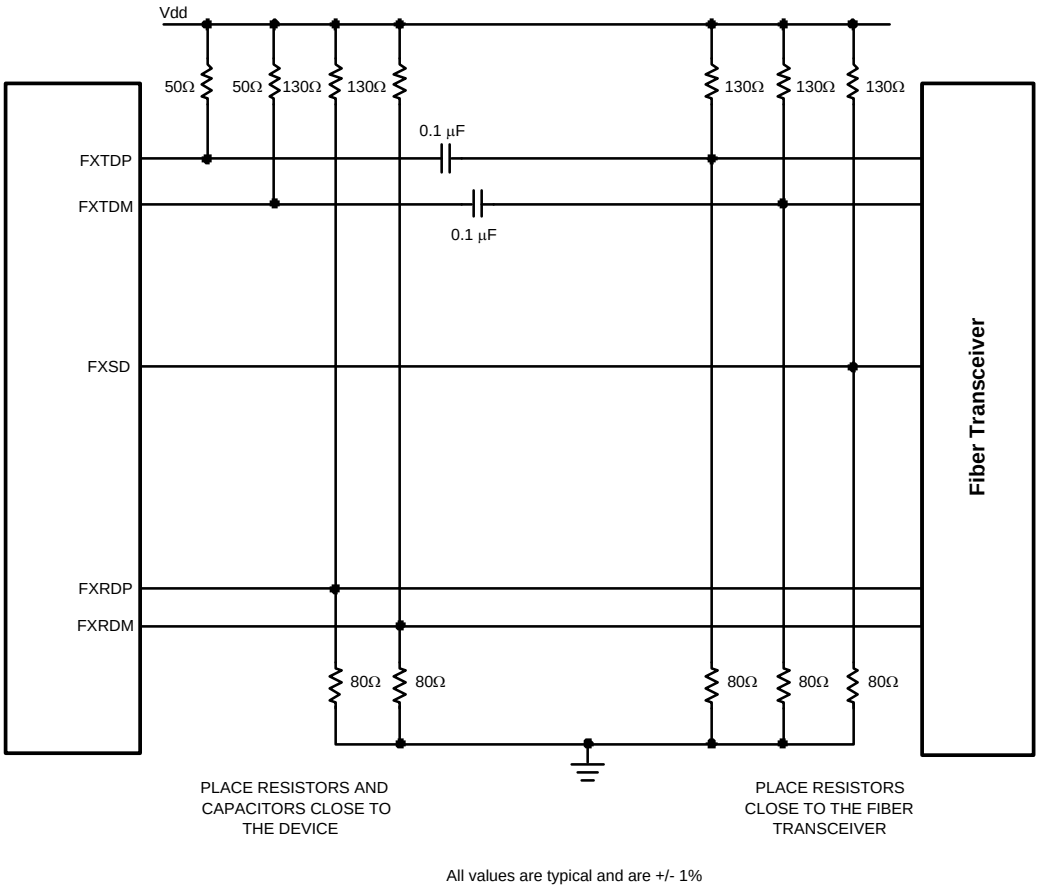


Figure 6-4. 100 Mb/s Fiber-Pair Interface

6.2.1.3 ESD Protection

Typically, ESD precautions are predominantly in effect when handling the devices or board before being installed in a system. In those cases, strict handling procedures need be implemented during the manufacturing process to greatly reduce the occurrences of catastrophic ESD events. After the system is assembled, internal components are less sensitive from ESD events.

The network interface pins are more susceptible to ESD events.

6.2.1.4 Clock In (X1) Recommendations

The DP83640 supports an external CMOS level oscillator source or a crystal resonator device.

6.2.1.4.1 Oscillator

If an external clock source is used, X1 should be tied to the clock source and X2 should be left floating.

The CMOS 25-MHz oscillator specifications for MII Mode are listed in Table 6-1. For RMII Slave Mode, the CMOS 50-MHz oscillator specifications are listed in Table 6-2. For RMII Slave mode, it is not recommended that the system clock out, Pin 24, be used as the reference clock to the MAC without first verifying the interface timing. See AN-1405 (SNLA076) for more details.

6.2.1.4.2 Crystal

A 25-MHz, parallel, 20-pF load crystal resonator should be used if a crystal source is desired. Figure 6-5 shows a typical connection for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

The oscillator circuit is designed to drive a parallel resonance AT cut crystal with a minimum drive level of 100 µW and a maximum of 500 µW. If a crystal is specified for a lower drive level, a current limiting resistor should be placed in series between X2 and the crystal.

As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, C_{L1} and C_{L2} should be set at 33 pF, and R_1 should be set at 0 Ω.

Specification for 25-MHz crystal are listed in Table 6-3.

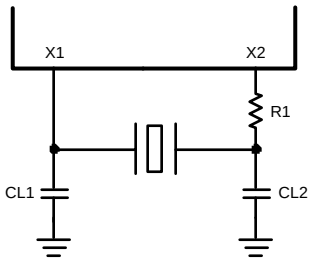


Figure 6-5. Crystal Oscillator Circuit

Table 6-1. 25-MHz Oscillator Specification

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency		25		MHz	
Frequency Tolerance			±50	ppm	Operational Temperature
Frequency Stability			±50	ppm	1 year aging
Rise / Fall Time			6	nsec	20% - 80%
Jitter			800 (1)	psec	Short term
Jitter			800 (1)	psec	Long term
Symmetry	40%		60%		Duty Cycle

(1) This limit is provided as a guideline for component selection and not verified by production testing. Refer to AN-1548, *PHYTER 100 Base-TX Reference Clock Jitter Tolerance* (SNLA091) for details on jitter performance.

Table 6-2. 50-MHz Oscillator Specification

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency		50		MHz	
Frequency Tolerance			±50	ppm	Operational Temperature
Frequency Stability			±50	ppm	Operational Temperature
Rise / Fall Time			6	nsec	20% - 80%
Jitter			800 (1)	psec	Short term
Jitter			800 (1)	psec	Long term
Symmetry	40%		60%		Duty Cycle

(1) This limit is provided as a guideline for component selection and not verified by production testing. Refer to AN-1548, *PHYTER 100 Base-TX Reference Clock Jitter Tolerance* (SNLA091) for details on jitter performance.

Table 6-3. 25-MHz Crystal Specification

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency		25		MHz	
Frequency Tolerance			±50	ppm	Operational Temperature
Frequency Stability			±50	ppm	1 year aging
Shunt Capacitance	25		40	pF	Range of $C_{L1}$and C_{L2}

6.2.1.5 Magnetics

The magnetics have a large impact on the PHY performance as well. While several components are listed below, others may be compatible following the requirements listed in Table 6-4. It is recommended that the magnetics include both an isolation transformer and an integrated common mode choke to reduce EMI. When doing the layout, do not run signals under the magnetics. This could cause unwanted noise crosstalk. Likewise void the planes under discrete magnetics, this will help prevent common mode noise coupling. To save board space and reduce component count, an RJ-45 with integrated magnetics may be used.

Table 6-4. Magnetics Requirements

PARAMETER	TYP	UNITS	CONDITION
Turn Ratio	1:1	—	±2%
Insertion Loss	–1	dB	1-100 MHz
Return Loss	–16	dB	1-30 MHz
	–12	dB	30-60 MHz
	10	dB	60-80 MHz
Differential to Common Rejection Ratio	–30	dB	1-50MHz
	–20	dB	50-150 MHz
Crosstalk	–35	dB	30 MHz
	–30	dB	60 MHz
Isolation	1,500	dB	HPOT

6.2.2 Detailed Design Procedure

6.2.2.1 MAC Interface (MII/RMII)

The Media Independent Interface (MII) connects the PHYTER component to the Media Access Controller (MAC). The MAC may in fact be a discrete device, integrated into a microprocessor, CPU or FPGA. On the MII signals, the IEEE specification states the bus should be 68-Ω impedance. For space critical designs, the PHYTER family of products also support Reduced MII (RMII). For additional information on this mode of operation, refer to the *AN-1405 DP83848 Single 10/100 Mb/s Ethernet Transceiver Reduced Media Independent Interface (RMII) Mode Application Report* (SNLA076).

6.2.2.1.1 Termination Requirement

To reduce digital signal energy, 50-Ω series termination resistors are recommended for all MII output signals (including RXCLK, TXCLK, and RX Data signals.)

6.2.2.1.2 Recommended Maximum Trace Length

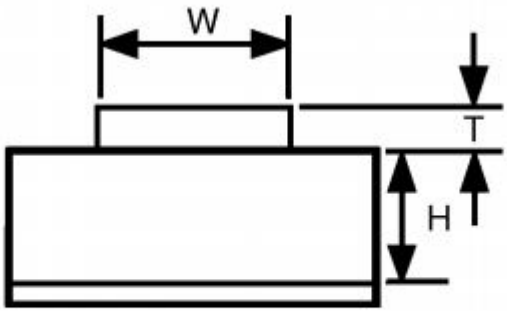
Although RMII and MII are synchronous bus architectures, there are a number of factors limiting signal trace lengths. With a longer trace, the signal becomes more attenuated at the destination and thus more susceptible to noise interference. Longer traces also act as antennas, and if run on the surface layer, can increase EMI radiation. If a long trace is running near and adjacent to a noisy signal, the unwanted signals could be coupled in as cross talk. It is recommended to keep the signal trace lengths as short as possible. Ideally, keep the traces under 6 inches. Trace length matching, to within 2.0 inches on the MII or RMII bus is also recommended. Significant differences in the trace lengths can cause data timing issues. As with any high speed data signal, good design practices dictate that impedance should be maintained and stubs should be avoided throughout the entire data path.

6.2.2.2 Calculating Impedance

The following equations can be used to calculate the differential impedance of the board. For microstrip traces, a solid ground plane is needed under the signal traces. The ground plane helps keep the EMI localized and the trace impedance continuous. Because stripline traces are typically sandwiched between the ground/supply planes, they have the advantage of lower EMI radiation and less noise coupling. The trade off of using strip line is lower propagation speed.

6.2.2.2.1 Microstrip Impedance - Single-Ended

$$Z_o = \left(\frac{87}{\sqrt{E_r + (1.41)}}\right) \ln\left(5.98 \frac{H}{0.8\,W + T}\right) \quad (4)$$

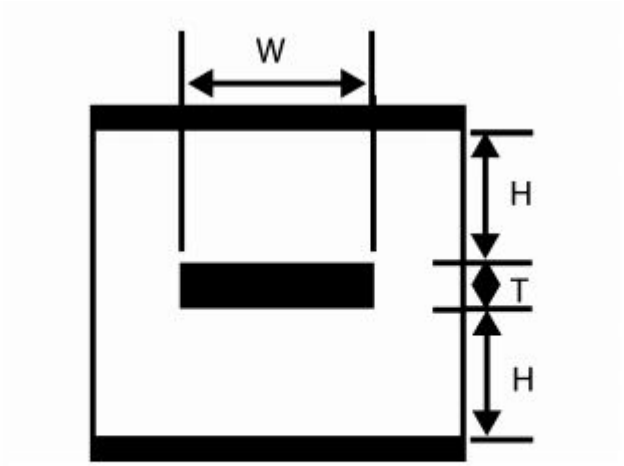


W = Width of the trace H = Height of dielectric above the return plane T = Trace thickness Er = Relative permittivity of the dielectric

Figure 6-6. Microstrip Impedance - Single-Ended

6.2.2.2.2 Stripline Impedance – Single-Ended

$$Z_o = \left(\frac{60}{\sqrt{E_r}}\right) \ln\left(1.98 \times \left(\frac{2 \times H + T}{0.8 \times W + T}\right)\right) \quad (5)$$

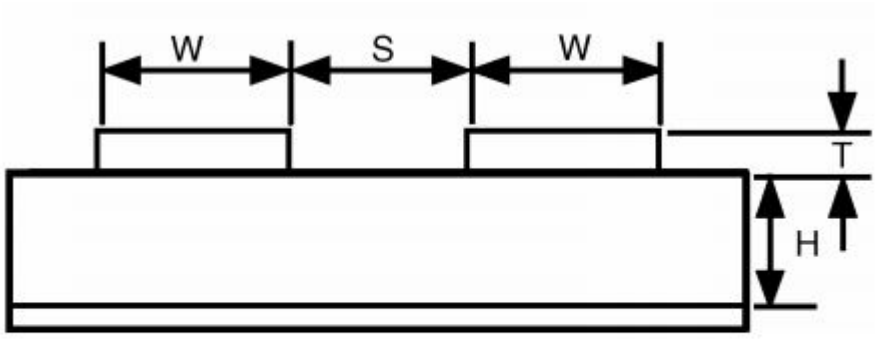


W = Width of the trace H = Height of dielectric above the return plane T = Trace thickness Er = Relative permittivity of the dielectric

Figure 6-7. Stripline Impedance – Single-Ended

6.2.2.2.3 Microstrip Impedance - Differential

$$Z_{diff} = 2 \times Z_o \times \left(1 - 0.48\left(e^{\left(-0.96\frac{S}{H}\right)}\right)\right) \quad (6)$$

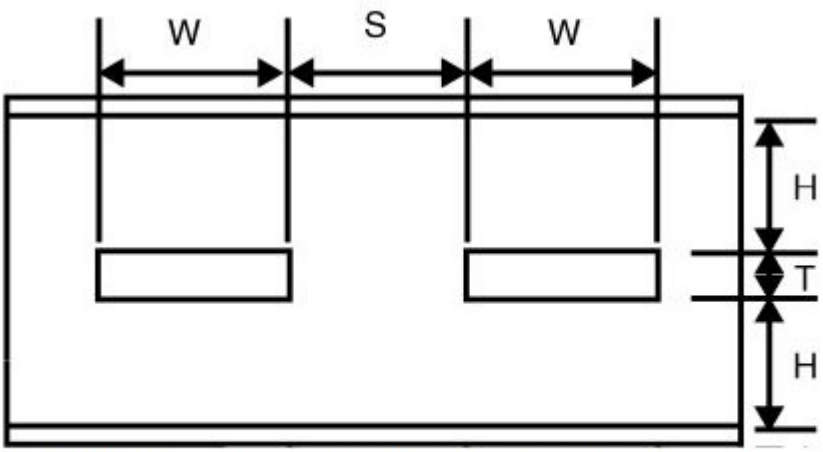


W = Width of the trace H = Height of dielectric above the return plane T = Trace thickness S = Space between traces Er = Relative permittivity of the dielectric

Figure 6-8. Microstrip Impedance - Differential

6.2.2.2.4 Stripline Impedance - Differential

$$Z_{diff} = 2 \times Z_o \left(1 - 0.347 \left(e^{\left(-2.9\frac{S}{H}\right)}\right)\right) \quad (7)$$



W = Width of the trace H = Height of dielectric above the return plane T = Trace thickness S = space between traces Er = Relative permittivity of the dielectric

Figure 6-9. Stripline Impedance - Differential

6.2.3 Application Curves

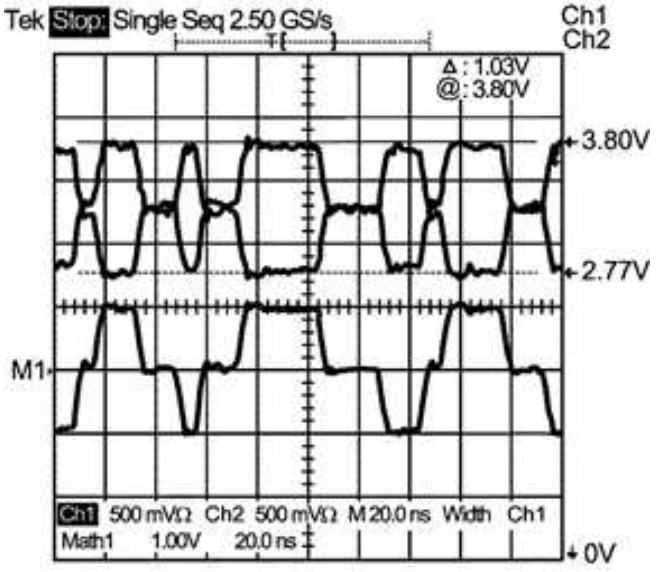


Figure 6-10. Sample 100 Mb/s Waveform (MLT-3)

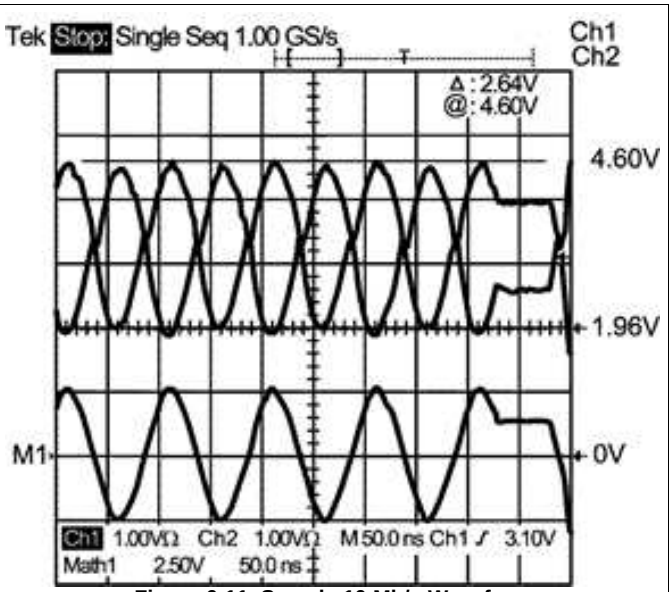


Figure 6-11. Sample 10 Mb/s Waveform

6.3 Layout

6.3.1 Layout Guidelines

6.3.1.1 PCB Layout Considerations

Place the 49.9-Ω, 1% resistors, and 0.1-µF decoupling capacitor, near the PHYTER TD± and RD± pins and via directly to the VDD plane.

Stubs should be avoided on all signal traces, especially the differential signal pairs. See Figure 6-12.

Within the pairs (for example, TD+ and TD-), the trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and increased EMI. See Figure 6-12.

Ideally, there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace pair on a single layer if possible.

PCB trace lengths should be kept as short as possible.

Signal traces should not be run such that they cross a plane split. See Figure 6-13. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems.

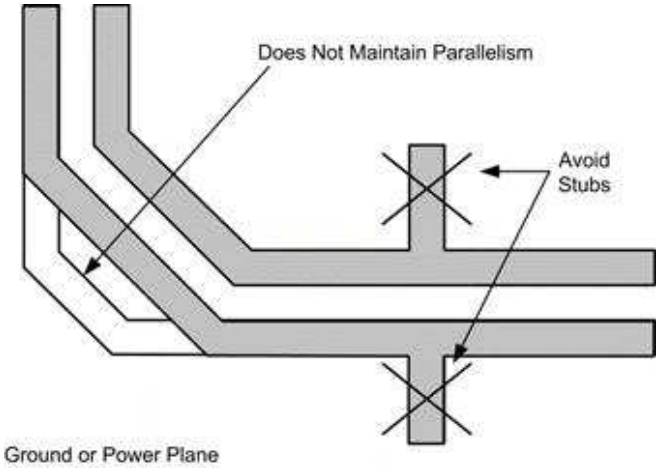


Figure 6-12. Avoiding Stubs in a Differential Signal Pair

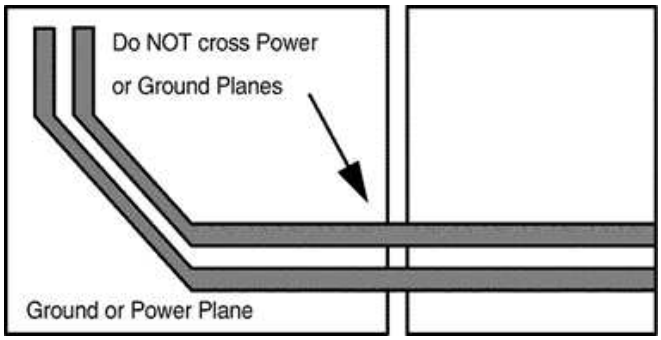


Figure 6-13. Differential Signal Pair-Plane Crossing

MDI signal traces should have 50 Ω to ground or 100-Ω differential controlled impedance. Many tools are available online to calculate this.

6.3.1.2 PCB Layer Stacking

To meet signal integrity and performance requirements, at minimum a four-layer PCB is recommended for implementing PHYTER components in end user systems. The following layer stack-ups are recommended for four, six, and eight-layer boards, although other options are possible.

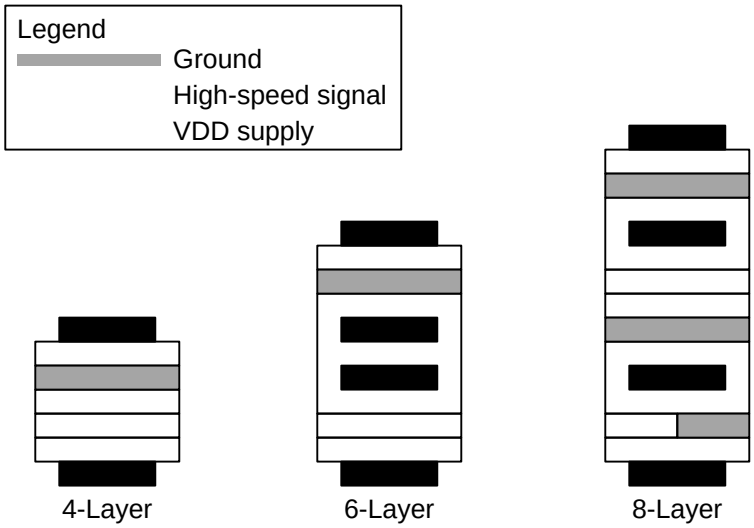


Figure 6-14. PCB Stripline Layer Stacking

Within a PCB, it may be desirable to run traces using different methods, microstrip vs. stripline, depending on the location of the signal on the PCB. For example, it may be desirable to change layer stacking where an isolated chassis ground plane is used. Figure 6-15 illustrates alternative PCB stacking options.

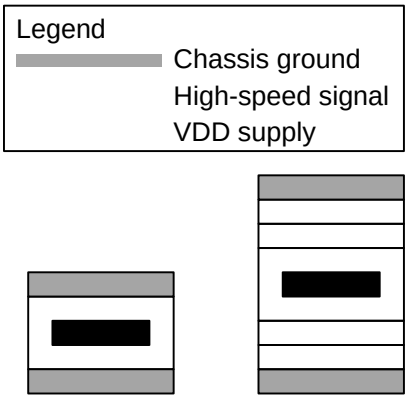


Figure 6-15. Alternative PCB Stripline Layer Stacking

6.3.2 Layout Example

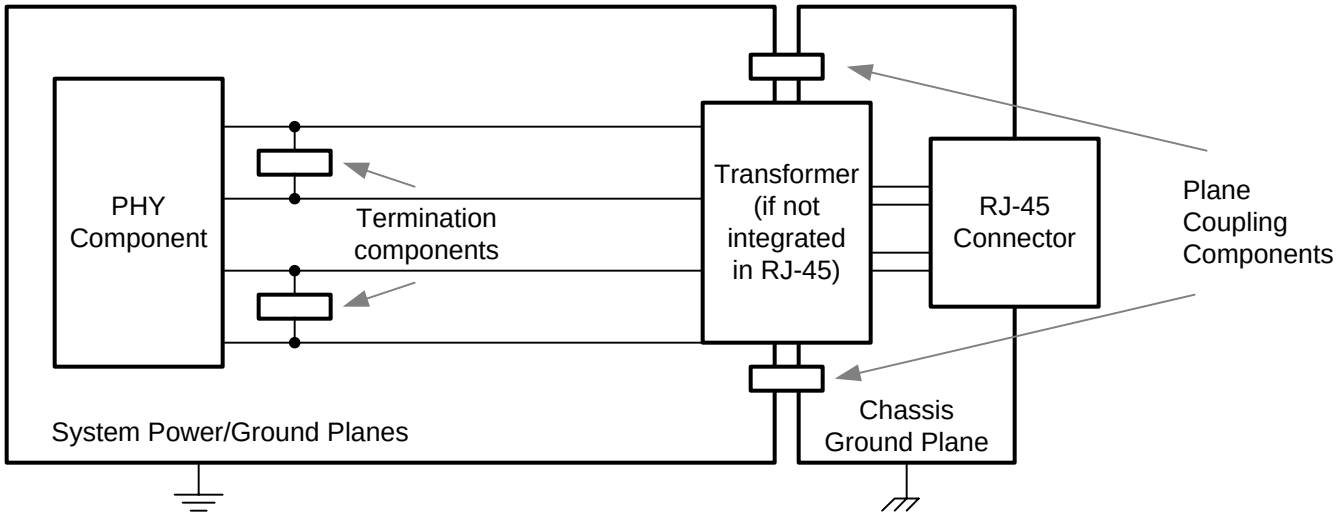


Figure 6-16. Layout Example

6.4 Power Supply Recommendations

The VDD supply pins of the device should be bypassed with low impedance 0.1-µF surface mount capacitors. To reduce EMI, the capacitors should be places as close as possible to the component VDD supply pins, preferably between the supply pins and the vias connecting to the power plane. In some systems it may be desirable to add 0-Ω resistors in series with supply pins, as the resistor pads provide flexibility if adding EMI beads becomes necessary to meet system level certification testing requirements (see Figure 6-17). It is recommended the PCB have at least one solid ground plane and one solid VDD plane to provide a low impedance power source to the component. This also provides a low impedance return path for non-differential digital MII and clock signals. A 10.0-µF capacitor should also be placed near the PHY component for local bulk bypassing between the VDD and ground planes.

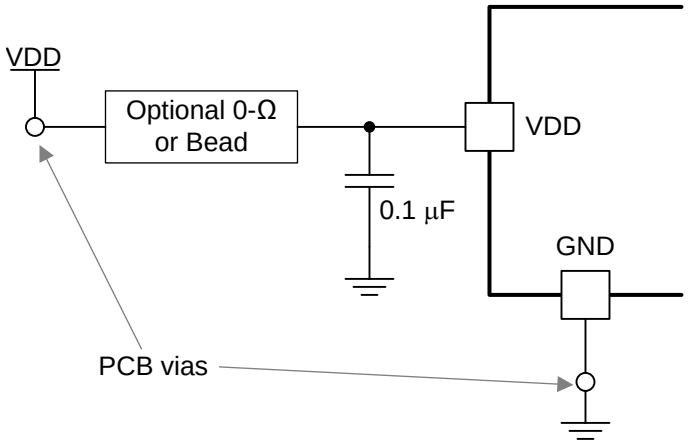


Figure 6-17. VDD Bypass Layout

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *Using RMII Master Mode*, AN-1794 (SNLA101)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *DP83640 Synchronous Ethernet Mode: Achieving Sub-ns Accuracy in PTP Applications* (SNLA100)
- *Synchronizing a DP83640 PTP Master to a GPS Receiver* (SNOA548)
- *IEEE 1588 Synchronization Over Standard Networks Using the DP83640* (SNLA116)
- *IEEE 1588 Boundary Clock and Transparent Clock Implementation Using the DP83640* (SNLA104)
- *DP83640 IEEE 1588 PTP Synchronized Clock Output* (SNLA099)
- *IEEE 1588 Precision Time Protocol Time Synchronization Performance* (SNLA098)
- *DP83640 Software Design Guide and C Software Reference Library* (SNLU049)

7.2 Trademarks

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7.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83640TVV/NOPB	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DP83640 TVV
DP83640TVV/NOPB.A	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DP83640 TVV
DP83640TVVX/NOPB	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	DP83640 TVV
DP83640TVVX/NOPB.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	DP83640 TVV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

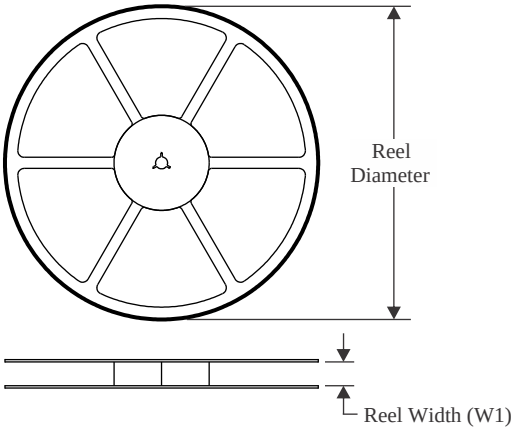
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

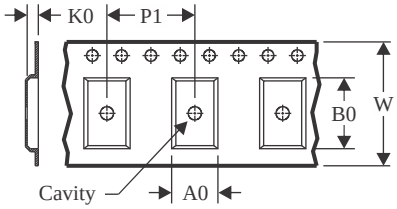
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

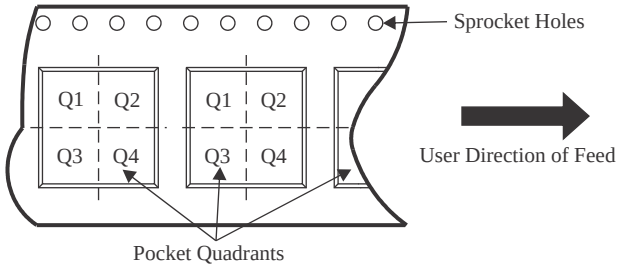


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

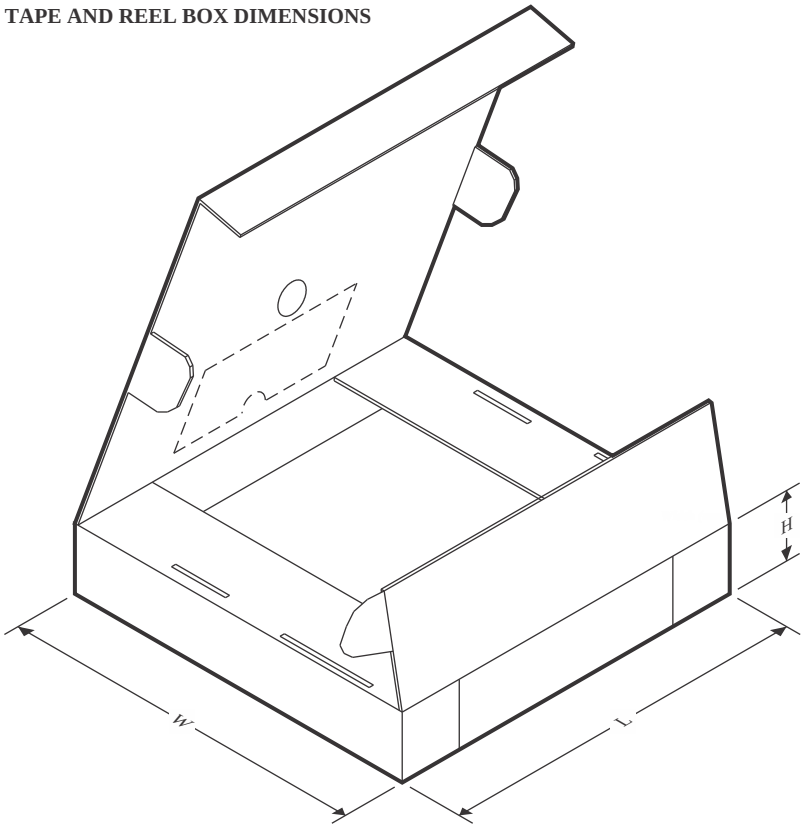
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83640TVVX/NOPB	LQFP	PT	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2

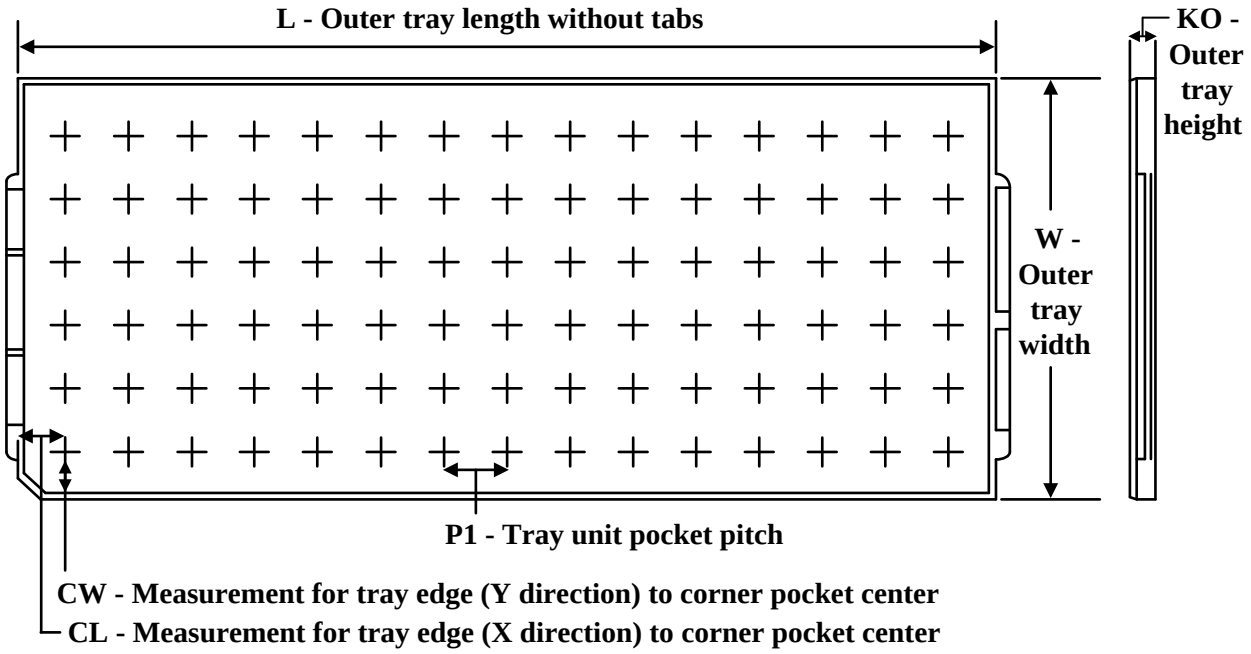
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83640TVVX/NOPB	LQFP	PT	48	1000	356.0	356.0	36.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

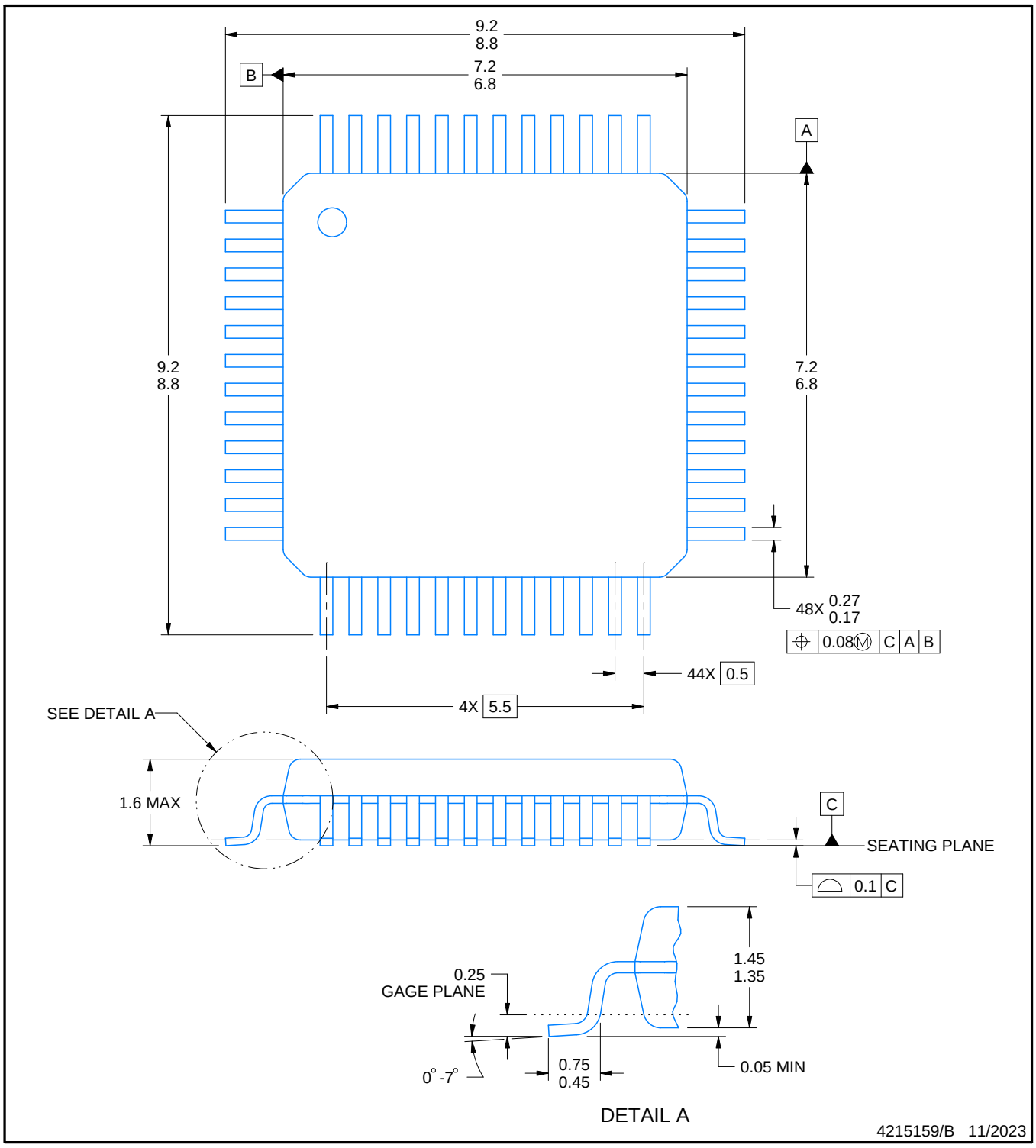
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DP83640TVV/NOPB	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DP83640TVV/NOPB.A	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PT0048A

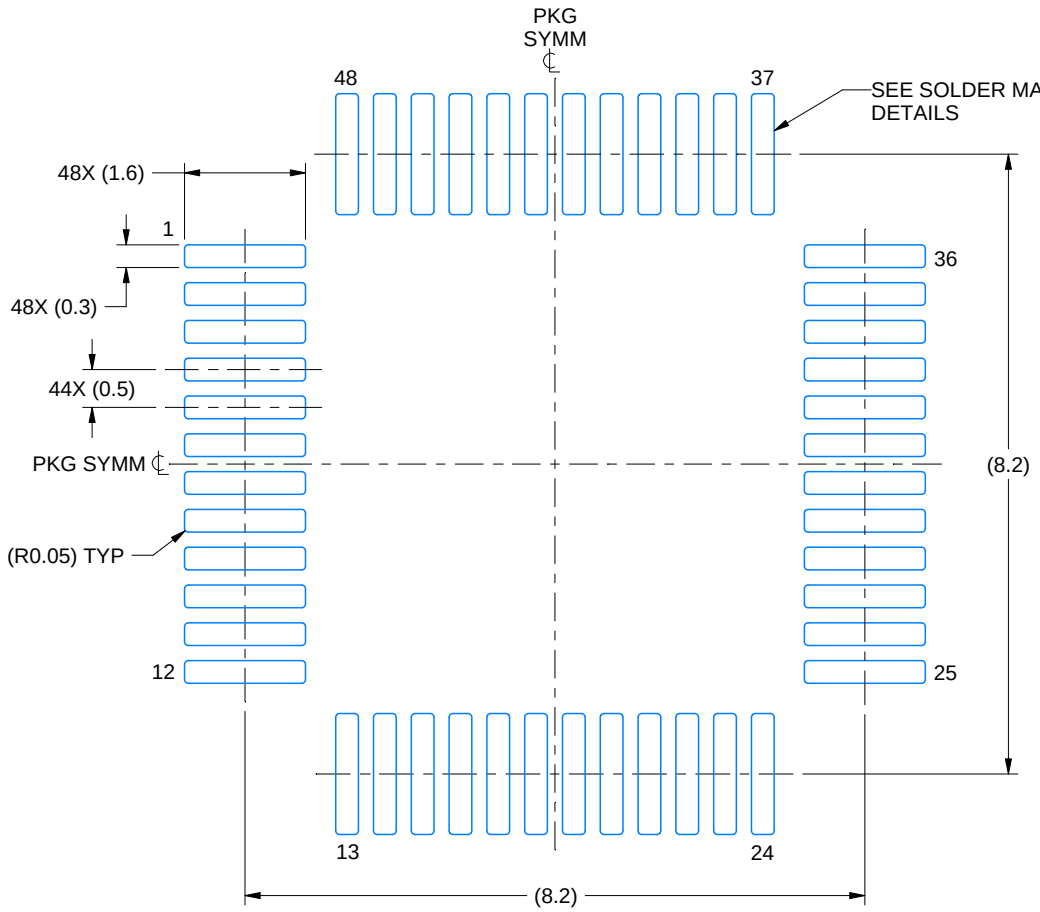
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

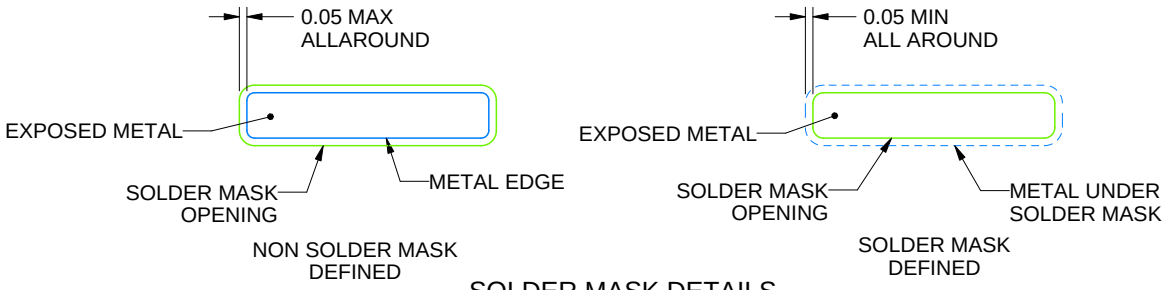


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

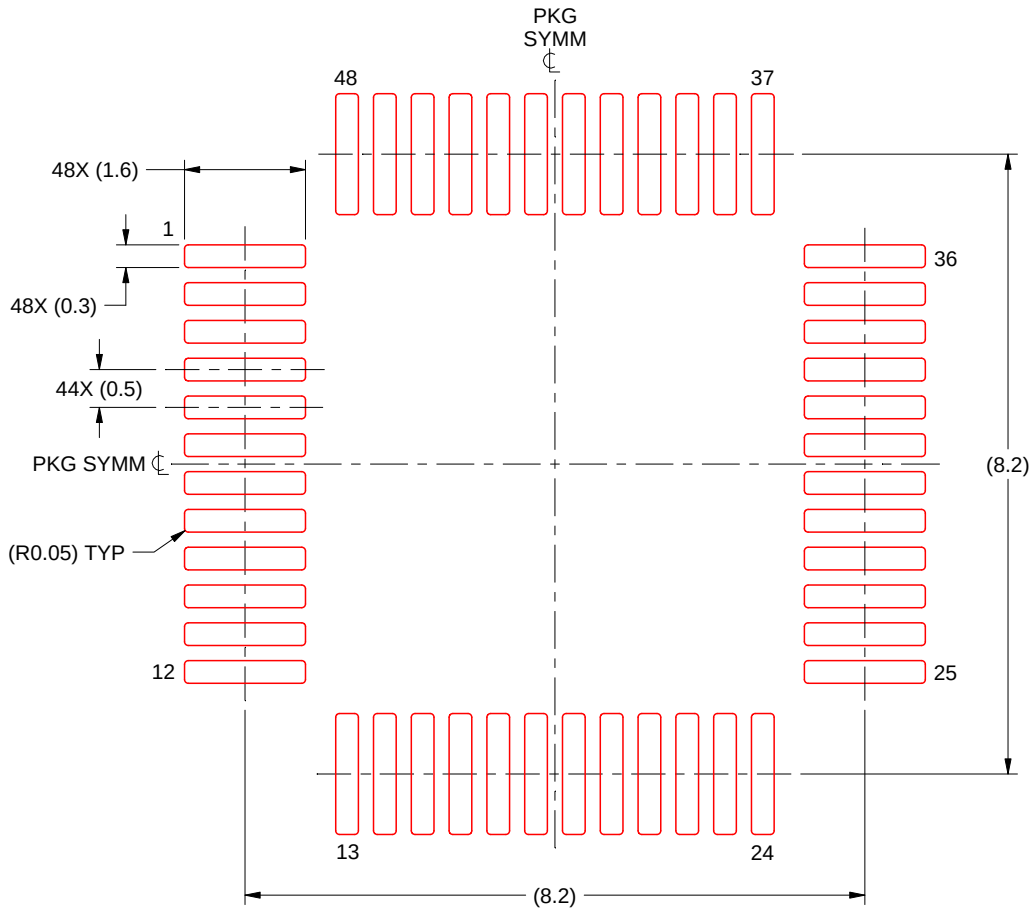


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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