





**DLPC4420** DLPS222A - DECEMBER 2021 - REVISED FEBRUARY 2023

# **DLPC4420 DLP® Display Controller**

#### 1 Features

- Dual DLP controller support for up to 4K ultra high definition (UHD) resolution display using digital micromirror devices (DMD):
  - Up to 4K at 60 Hz
  - Up to 1080p at 240 Hz
  - Up to 1080p at 120 Hz (3D)
- Provides single 30-bit or dual 60-bit input pixel interface:
  - RGB data format
  - 8, 9, or 10 bits per color
  - Pixel clock up to 600 MHz in dual 30-bit mode on dual controllers
- High-speed, low voltage differential signaling (LVDS) DMD interface
- 150-MHz ARM946<sup>™</sup> microprocessor
- Microprocessor peripherals
  - Programmable pulse-width modulation (PWM) and capture timers
  - Three I<sup>2</sup>C ports, three UART ports and three SSP ports
  - One USB 1.1 secondary port
- Image processing
  - Multiple image processing algorithms
  - Frame rate conversion
  - Color coordinate adjustment
  - Programmable color space conversion
  - Programmable degamma and splash
  - Integrated support for 3-D display
  - 1-D keystone correction

- Integrated clock generation circuitry
  - Operates on a single 20-MHz crystal
  - Integrated spread spectrum clocking
- External memory support
  - Parallel flash for microprocessor and PWM sequence
- 516-pin plastic ball grid array package
- Supports LED and laser hybrid illuminations

### 2 Applications

- Laser TV
- **Smart projector**
- Digital signage
- Enterprise projectors

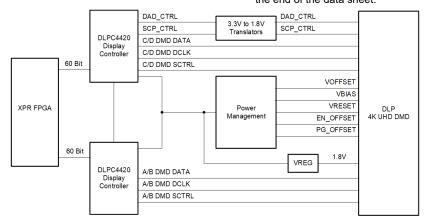
### 3 Description

The DLPC4420 is a digital display controller for the DLP® display chipset. The chipset comprises the DLPC4420 display controller, the DLP digital micromirror device (DMD), the DLPA100 controller power management device, and the DLPA300 DMD micromirror driver (refer to the DMD data sheet). This solution is a great fit for display systems that require high resolution, high brightness, and system simplicity. To ensure reliable operation, the DLPC4420 display controller must always be used with a DLP DMD and respective DLP power management devices.

#### **Device Information**

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE (NOM)
DLPC4420	ZPC (516)	27.00 mm × 27.00 mm

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



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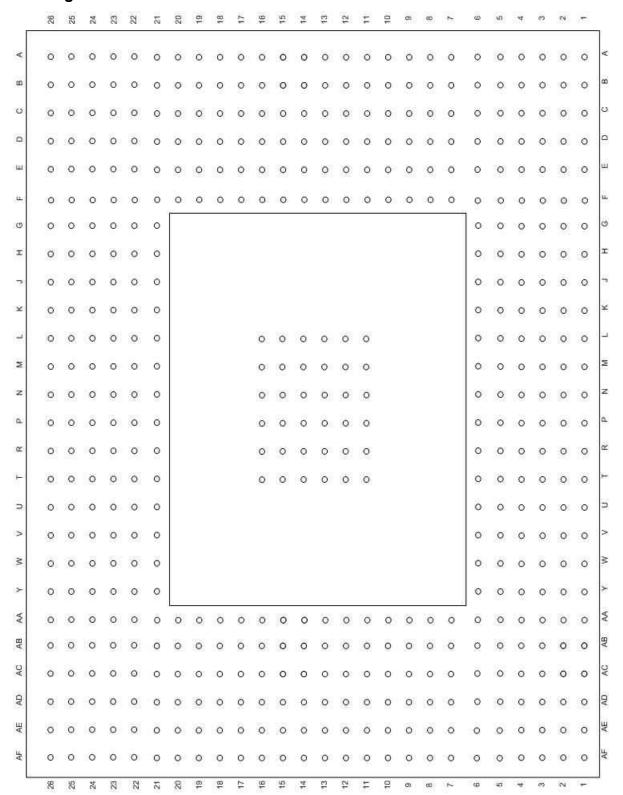
# **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	Changes from Revision * (December 2021) to Revision A (February 2023)				
•	Updated wording in Features for clarity	1			
•	Updated Description	1			
•	Updated Device Nomenclature and Device Marking sections	43			



### **5 Pin Configuration and Functions**





### **Table 5-1. Pin Functions**

PIN <sup>(1)</sup>		(2)	DECODINE		
NAME	NO.	TYPE <sup>(2)</sup>	DESCRIPTION		
POSENSE	P22	14	Power-on sense, high true, signal provided from an external voltage monitor circuit. This signal is driven active (high) when all ASIC supply voltages have reached 90% of their specified minimum voltage. This signal is driven inactive (low) after the falling edge of PWRGOOD as specified.		
PWRGOOD	T26	14	Power good, high true, signal from external power supply or voltage monitor. A high value indicates all power is within operating voltage specs and the system is safe to exit its reset state. A transition from high to low is used to indicate that the controller or DMD supply voltage drops below their rated minimum level. This transition must occur prior to the supply voltage drop as specified. During this interval, POSENSE must remain active high. This is a warning of an imminent power loss condition. This warning is required to enhance long term DMD reliability. A DMD park followed by a full controller reset is performed by the DLPC4420 controller when PWRGOOD goes low for the specified minimum, protecting the DMD. This minimum deassertion time is used to protect the input from glitches. Following this the DLPC4420 controller is held in its reset state as long as PWRGOOD is low. PWRGOOD must be driven high for normal operation. The DLPC4420 controller acknowledges PWRGOOD as active once it has been driven high for a specified minimum time. Uses hysteresis		
EXT_ARTZ	T24	O <sub>2</sub>	General purpose, low true, reset output. This output is asserted low immediately upon asserting power-up reset (POSENSE) low and remains low while POSENSE remains low. EXT_ARSTZ continues to be held low after the release of power-up reset (that is, POSENSE set high) until released by software. EXT_ARSTZ is also asserted low approximately 5 µs after the detection of a PWRGOOD or any internally generated reset. In all cases it remains active for a minimum of 2 ms. Note that the ASIC contains a software register that can be used to independently drive this output.		
MTR_ARTZ	T25	O <sub>2</sub>	Color wheel motor controller, low true, reset output. This output is asserted low immediately upon asserting power-up reset (POSENSE) low and remains low while POSENSE remains low. MTR_ARSTZ continues to be held low after the release of power-up reset (that is, POSENSE is set high) until released by software. MTR_ARSTZ is also optionally asserted low approximately 5 µs after the detection of a PWRGOOD or any internally generated reset. In all cases, it remains active for a minimum of 2 ms. Note that the ASIC contains a software register that can be used to independently drive this output. The ASIC also contains a software register that can be used to motor reset upon a lamp strike reset.		
BOARD LEVEL TEST	T AND INITIALIZAT	ΓΙΟΝ <sup>(3)</sup>			
TDI	N25	I <sub>4</sub>	JTAG serial data in		
TCK	N24	l <sub>4</sub>	JTAG serial data clock		
TMS1	P25	I <sub>4</sub>	JTAG test mode select		
TMS2	P26	l <sub>4</sub>	JTAG test mode select		
TDO1	N23	O <sub>5</sub>	JTAG serial data out		
TDO2	N22	O <sub>5</sub>	JTAG serial data out		
TRSTZ	M23	I <sub>4</sub>	JTAG reset. This signal includes an internal pullup and utilizes hysteresis. This pin is pulled high (or left unconnected) when the JTAG interface is in use for boundary scan or ARM debug. Connect this pin to ground otherwise. Failure to tie this pin low during normal operation causes startup and initialization problems.		
RTCK	E4	O <sub>2</sub>	JTAG return clock		
ETM_PIPESTAT_2	A4	B <sub>2</sub>			
ETM_PIPESTAT_1	B5	B <sub>2</sub>	ETM trace port pipeline status. Indicates the pipeline status of the ARM core. These signals include internal pulldowns.		
ETM_PIPESTAT_0	C6	B <sub>2</sub>			
ETM_TRACESYNC	A5	B <sub>2</sub>	ETM trace port synchronization signal, indicating the start of a branch sequence on the trace packet port. This signal includes an internal pulldown.		
ETM_TRACECLK	D7	B <sub>2</sub>	ETM trace port clock. This signal includes an internal pulldown.		
ICTSEN	M24	I <sub>4</sub>	IC tristate enable (active high). Asserting high tristates all outputs except the JTAG interface. This signal includes an internal pulldown, however an external pulldown is recommended for added protection. Uses hysteresis.		
TSTPT_7	E8	B <sub>2</sub>	Test pin 7. This signal provides internal pulldowns.  Normal use: reserved for test output. Recommended to be left open or unconnected for normal use		
TSTPT_6	B4	B <sub>2</sub>	Test pin 6. This signal provides internal pulldowns.  Normal use: reserved for test output. Recommended to be left open or unconnected for normal use		
TSTPT_5	C4	B <sub>2</sub>	Test pin 5. This signal provides internal pulldowns.  Normal use: reserved for test output. Recommended to be left open or unconnected for normal use		
TSTPT_4	E7	B <sub>2</sub>	Test pin 4. This signal provides internal pulldowns.  Normal use: reserved for test output. Recommended to be left open or unconnected for normal use		
TSTPT_3	D5	B <sub>2</sub>	Test pin 3. This signal provides internal pulldowns.  Normal use: reserved for test output. Recommended to be left open or unconnected for normal use.		
TSTPT_2	E6	B <sub>2</sub>	Test pin 2. This signal provides internal pulldowns. Additionally, it is recommended that jumper options be provided for connecting TSTPT(2:0) to external pullups.		
TSTPT_1	D3	B <sub>2</sub>	Test pin 1. This signal provides internal pulldowns. Additionally, it is recommended that jumper options be provided for connecting TSTPT(2:0) to external pullups.		
TSTPT_0	C2	B <sub>2</sub>	Test pin 0. This signal provides internal pulldowns. Additionally, it is recommended that jumper options be provided for connecting TSTPT(2:0) to external pullups.		
DEVICE TEST					
HW_TEST_EN	M25	I <sub>4</sub>	Device manufacturing test enable. This signal includes an internal pulldown and utilizes hysteresis. It is recommended that this signal be tied to an external ground in normal operation for added protection.		
PORT1 and PORT 2	CHANNEL DATA a	ind CONTROL (4)	5) (6) (7)		
P_CLK1	AE22	I <sub>4</sub>	Input Port Data Pixel Write Clock (selectable as rising or falling edge triggered, and which port it is associated with (A or B or (A and B)). This signal includes an internal pulldown.		



		Table 5-1. Pin Functions (continued)			
PIN <sup>(1)</sup>		TYPE <sup>(2)</sup>	DESCRIPTION		
NAME	NO.				
P_CLK2	W25	14	Input Port Data Pixel Write Clock (selectable as rising or falling edge triggered, and which port it is associated with (A or B or (A and B)). This signal includes an internal pulldown.		
P_CLK3	AF23	l <sub>4</sub>	Input Port Data Pixel Write Clock (selectable as rising or falling edge triggered, and which port it is associated with (A or B or (A and B)). This signal includes an internal pulldown.		
P_DATAEN1	AF22	I <sub>4</sub>	Active High Data Enable. Selectable as to which port it is associated with (A or B or (A and B)). This signal includes an internal pulldown.		
P_DATAEN2	W24	I <sub>4</sub>	Active High Data Enable. Selectable as to which port it is associated with (A or B or (A and B)). This signal includes an internal pulldown.		
P1_A_9	AD15	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 128)		
P1_A_8	AE15	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 64)		
P1_A_7	AE14	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 32)		
P1_A_6	AE13	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 16)		
P1_A_5	AD13	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 8)		
P1_A_4	AC13	14	Port 1 A Channel Input Pixel Data (bit weight 4)		
P1_A_3	AF14	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 2)		
P1_A_2	AF13	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 1)		
P1_A_1	AF12	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 0.5)		
P1_A_0	AE12	I <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 0.25)		
P1_B_9	AF18	14	Port 1 B Channel Input Pixel Data (bit weight 128)		
P1_B_8	AB18	I <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 64)		
P1_B_7	AC15	I <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 32)		
P1_B_6	AC16	I <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 32)		
			· · · · · · · · · · · · · · · · · · ·		
P1_B_5	AD16	l <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 8)		
P1_B_4	AE16	l <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 4)		
P1_B_3	AF16	I <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 2)		
P1_B_2	AF15	I <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 1)		
P1_B_1	AC14	I <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 0.5)		
P1_B_0	AD14	I <sub>4</sub>	Port 1 B Channel Input Pixel Data (bit weight 0.25)		
P1_C_9	AD20	I <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 128)		
P1_C_8	AE20	l <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 64)		
P1_C_7	AE21	l <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 32)		
P1_C_6	AF21	l <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 16)		
P1_C_5	AD19	l <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 8)		
P1_C_4	AE19	I <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 4)		
P1_C_3	AF19	I <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 2)		
P1_C_2	AF20	I <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 1)		
P1_C_1	AC19	I <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 0.5)		
P1_C_0	AE19	I <sub>4</sub>	Port 1 C Channel Input Pixel Data (bit weight 0.25)		
P1_VSYNC	AC20	B <sub>2</sub>	Port 1 Vertical Sync. This signal includes an internal pulldown. While intended to be associated with Port 1, it can be programmed for use with Port 2.		
P1_HSYNC	AD21	B <sub>2</sub>	Port 1 Horizontal Sync. This signal includes an internal pulldown. While intended to be associated with Port 1, it can be programmed for use with Port 2.		
P2_A_9	AD26	I <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 128)		
P2_A_8	AD25	I <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 64)		
P2_A_7	AB21	I <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 32)		
P2_A_6	AC22	I <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 32)  Port 2 A Channel Input Pixel Data (bit weight 16)		
P2_A_5	AD23	l <sub>4</sub>	Port 1 A Channel Input Pixel Data (bit weight 1)		
P2_A_4	AB20	l <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 4)		
P2_A_3	AC21	I <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 4)  Port 2 A Channel Input Pixel Data (bit weight 2)		
P2_A_3 P2_A_2	AD22		· · · · · · · · · · · · · · · · · · ·		
		l <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 1)		
P2_A_1	AE23	I <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 0.5)		
P2_A_0	AB19	l <sub>4</sub>	Port 2 A Channel Input Pixel Data (bit weight 0.25)		
P2_B_9	Y22	l <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 128)		
P2_B_8	AB26	l <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 64)		
P2_B_7	AA23	l <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 32)		
P2_B_6	AB25	I <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 16)		



PIN	<b>N</b> (1)		Table 5-1. Pin Functions (continued)	
NAME	NO.	TYPE <sup>(2)</sup>	DESCRIPTION	
P2_B_5	AA22	14	Port 2 B Channel Input Pixel Data (bit weight 8)	
P2 B 4	AB24	14	Port 2 B Channel Input Pixel Data (bit weight 4)	
P2 B 3	AC26	14	Port 2 B Channel Input Pixel Data (bit weight 2)	
P2 B 2	AB23	I <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 1)	
P2 B 1	AC25	14	Port 2 B Channel Input Pixel Data (bit weight 0.5)	
P2 B 0	AC24	l <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 0.25)	
P2_C_9	W23	l <sub>4</sub>	Port 2 C Channel Input Pixel Data (bit weight 128)	
P2_C_8	V22	l <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 64)	
P2 C 7	Y26	I <sub>4</sub>	Port 2 C Channel Input Pixel Data (bit weight 32)	
P2_C_6	Y25	I <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 16)	
P2 C 5	Y24	I <sub>4</sub>	Port 2 C Channel Input Pixel Data (bit weight 8)	
P2 C 4	Y23	I <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 4)	
P2_C_4	W22	l <sub>4</sub>	Port 2 C Channel Input Pixel Data (bit weight 4)	
P2_C_3 P2_C_2	AA26	I <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 2)	
	AA20		Port 2 C Channel Input Pixel Data (bit weight 1)	
P2_C_1	AA23	I <sub>4</sub>	· · · · · · · · · · · · · · · · · · ·	
P2_C_0	AA24	l <sub>4</sub>	Port 2 B Channel Input Pixel Data (bit weight 0.25)	
P2_VSYNC	U22	B <sub>2</sub>	Port 2 Vertical Sync. This signal includes an internal pulldown. While intended to be associated with Port 2, it can be programmed for use with Port 1.	
P2_HSYNC	W26	B <sub>2</sub>	Port 2 Horizontal Sync. This signal includes an internal pulldown. While intended to be associated with Port 2, it can be programmed for use with Port1.	
ALF INPUT PORT	CONTROL			
ALF_VSYNC	AF11	I <sub>4</sub>	Autolock dedicated vertical sync. This signal includes an internal pulldown and uses hysteresis.	
ALF_HSYNC	AD11	I <sub>4</sub>	Autolock dedicated horizontal sync. This signal includes an internal pulldown and uses hysteresis.	
ALF_CSYNC	AE11	I <sub>4</sub>	Autolock dedicated composite sync (sync on green). This signal includes an internal pulldown and uses hysteresis.	
DMD RESET and B	IAS CONTROL			
DADOEZ	AE7	O <sub>5</sub>	DAD (DLPA200 / DLPA300) Output Enable (active low)	
DADADDR_3	AD6	O <sub>5</sub>		
DADADDR_2	AE5	O <sub>5</sub>		
DADADDR_1	AF4	O <sub>5</sub>	— DAD address	
DADADDR_0	AB8	O <sub>5</sub>	_	
DADMODE_1	AD7	O <sub>5</sub>		
DADMODE_0	AE6	O <sub>5</sub>	— DAD modes	
DADSEL_1	AE4	O <sub>5</sub>		
DADSEL_0	AC7	O <sub>5</sub>	— DAD select	
DADSTRB	AF5	O <sub>5</sub>	DAD strobe	
DAD INTZ	AC8	14	DAD interrupt (active low). This signal typically requires an external pullup and uses hysteresis.	
DMD LVDS INTERF		1 7		
DCKA_P	V4	O <sub>7</sub>		
DCKA N	V3	O <sub>7</sub>	DMD, LVDS I/F channel A, differential clock	
SCA P	V2	O <sub>7</sub>		
SCA N	V1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial control	
DDA P 15	P4	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_I _15	P3	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_N_13	P2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_I _14	P1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_N_14	R1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_N_12 DDA_P_11	T4	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data  DMD, LVDS I/F channel A, differential serial data	
DDA_P_11 DDA_N_11	T3	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data  DMD, LVDS I/F channel A, differential serial data	
DDA_N_11	T2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data  DMD, LVDS I/F channel A, differential serial data	
	T1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data  DMD, LVDS I/F channel A, differential serial data	
DDA_N_10	U4		DMD, LVDS I/F channel A, differential serial data  DMD, LVDS I/F channel A, differential serial data	
DDA_P_9		O <sub>7</sub>		
DDA_N_9	U3	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_P_8	U2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_N_8	U1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	
DDA_P_7	W4	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data	



PIN <sup>(1)</sup>			Table 5-1. Pin Functions (continued)		
		TYPE <sup>(2)</sup>	DESCRIPTION		
NAME	NO.		DMD 1//DO //E shared A ## confidencial data		
DDA_N_7	W3	07	DMD, LVDS I/F channel A, differential serial data		
DDA_P_6	W2	07	DMD, LVDS I/F channel A, differential serial data		
DDA_N_6	W1	07	DMD, LVDS I/F channel A, differential serial data		
DDA_P_5	Y2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_N_5	Y1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_P_4	Y4	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_N_4	Y3	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_P_3	AA2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_N_3	AA1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_P_2	AA4	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_N_2	AA3	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_P_1	AB2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_N_1	AB1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_P_0	AC2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DDA_N_0	AC1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial data		
DCKB_P	J3	O <sub>7</sub>	DMD, LVDS I/F channel A, differential clock		
DCKB_N	J4	O <sub>7</sub>	DMD, LVDS I/F channel A, differential clock		
SCB P	J1	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial control		
SCB_N	J2	O <sub>7</sub>	DMD, LVDS I/F channel A, differential serial control		
DDB_P_15	N1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_15	N2	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB P 14	N3	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_14	N4	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_13	M2	O <sub>7</sub>			
	M1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_13	M3		DMD, LVDS I/F channel B, differential serial data		
DDB_P_12		07	DMD, LVDS I/F channel B, differential serial data		
DDB_N_12	M4	07	DMD, LVDS I/F channel B, differential serial data		
DDB_P_11	L1	07	DMD, LVDS I/F channel B, differential serial data		
DDB_N_11	L2	07	DMD, LVDS I/F channel B, differential serial data		
DDB_P_10	L3	07	DMD, LVDS I/F channel B, differential serial data		
DDB_N_10	L4	07	DMD, LVDS I/F channel B, differential serial data		
DDB_P_9	K1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_9	K2	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_8	K3	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_8	K4	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_7	H1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_7	H2	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_6	Н3	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_6	H4	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_5	G1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_5	G2	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_4	G3	07	DMD, LVDS I/F channel B, differential serial data		
DDB_N_4	G4	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_3	F1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_3	F2	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_2	F3	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_2	F4	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_1	E1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_N_1	E2	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB_P_0	D1	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
DDB N 0	D2	O <sub>7</sub>	DMD, LVDS I/F channel B, differential serial data		
PROGRAM MEMOR					
	1	, T	Input Bus D Data bit 3.		
PM_CSZ_0	D13	O <sub>5</sub>	100-Ω internal LVDS termination		



PIN <sup>(1)</sup>			Table 5-1. Pin Functions (continued)			
NAME	NO.	TYPE(2)	DESCRIPTION			
PM_CSZ_1	E12	O <sub>5</sub>				
			Input Bus D Data bit 5.			
PM_CSZ_2	A13	O <sub>5</sub>	100-Ω internal LVDS termination			
PM_ADDR_22 (GPIO 36)	A12	B <sub>5</sub>				
PM_ADDR_21 (GPIO 35)	E11	B <sub>5</sub>	Input Bus D Data bit 10. 100-Ω internal LVDS termination			
PM_ADDR_20	D12	O <sub>5</sub>				
PM_ADDR_19	C12	O <sub>5</sub>	Input Bus D Data bit 11. 100-Ω internal LVDS termination			
PM_ADDR_18	B11	O <sub>5</sub>				
PM_ADDR_17	A11	O <sub>5</sub>	Input Bus D Data bit 12.			
PM_ADDR_16	D11	O <sub>5</sub>	100-Ω internal LVDS termination			
PM_ADDR_15	C11	O <sub>5</sub>	Input Bus D Data bit 13.			
PM_ADDR_14	E10	O <sub>5</sub>	100-Ω internal LVDS termination			
PM_ADDR_13	D10	O <sub>5</sub>	Input Bus D Data bit 14.			
PM_ADDR_12	C10	O <sub>5</sub>	100-Ω internal LVDS termination			
PM_ADDR_11	B9	O <sub>5</sub>	Input Bus D Data bit 15.			
PM ADDR 10	A9	O <sub>5</sub>	100-Ω internal LVDS termination			
PM ADDR 9	E9	O <sub>5</sub>				
PM ADDR 8	D9	O <sub>5</sub>	Output Bus A Data bit 0 to DMD			
PM_ADDR_7	C9	O <sub>5</sub>				
		+	Output Bus A Data bit 1 to DMD			
PM_ADDR_6	B8	O <sub>5</sub>				
PM_ADDR_5	A8	O <sub>5</sub>	Output Bus A Data bit 2 to DMD			
PM_ADDR_4	D8	O <sub>5</sub>				
PM_ADDR_3	C8	O <sub>5</sub>	Output Bus A Data bit 3 to DMD			
PM_ADDR_2	B7	O <sub>5</sub>				
PM_ADDR_1	A7	O <sub>5</sub>	Output Bus A Data bit 4 to DMD			
PM_ADDR_0	C7	O <sub>5</sub>	· ·			
PM_WEZ	B12	O <sub>5</sub>	Output Bus A Data bit 5 to DMD			
PM_OEZ	C13	O <sub>5</sub>				
PM_BLSZ_1	B6	O <sub>5</sub>	Output Bus A Data bit 6 to DMD			
PM_BLSZ_0	A6	O <sub>5</sub>	Output Buo N Butta Bit 0 to Birib			
PM_DATA_15	C17	B <sub>5</sub>	Output Bus A Data bit 7 to DMD			
PM_DATA_14	B16	B <sub>5</sub>	Output bus A bata sit I to birib			
PM_DATA_13	A16	B <sub>5</sub>	Output Due A Data hit 0 to DMD			
PM_DATA_12	A15	B <sub>5</sub>	Output Bus A Data bit 8 to DMD			
PM_DATA_11	B15	B <sub>5</sub>	0.1.1010.1.10.1.000			
PM_DATA_10	D16	B <sub>5</sub>	Output Bus A Data bit 9 to DMD			
PM_DATA_9	C16	B <sub>5</sub>	S + 12 + 12 + 12 + 12 + 12 + 12 + 12 + 1			
PM_DATA_8	E14	B <sub>5</sub>	Output Bus A Data bit 10 to DMD			
PM_DATA_7	D15	B <sub>5</sub>				
PM_DATA_6	C15	B <sub>5</sub>	Output Bus A Data bit 11 to DMD			
PM_DATA_5	B14	B <sub>5</sub>				
PM_DATA_4	A14	B <sub>5</sub>	Output Bus A Data bit 12 to DMD			
PM_DATA_3	E13	B <sub>5</sub>				
PM_DATA_2	D14	B <sub>5</sub>	Output Bus A Data bit 13 to DMD			
PM_DATA_1	C14	B <sub>5</sub>				
PM_DATA_1 PM_DATA_0			Output Bus A Data bit 14 to DMD			
	B13	B <sub>5</sub>				
PERIPHERAL INTE	RFACE		100 Duy 0 Olysty This has suggested 400 kHz / 1 to 1			
IIC0_SCL	A10	B <sub>8</sub>	I2C Bus 0, Clock. This bus support 400 kHz, fast mode operation. This signal requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ. This input is not 5-V tolerant.			
IIC0_SDA	B10	B <sub>8</sub>	2C Bus 0, Data. This bus support 400 kHz, fast mode operation. This signal requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ. This input is not 5-V tolerant.			
SSP0_CLK	AD4	B <sub>5</sub>	Synchronous Serial Port 0, clock			
SSP0_RXD	AD5	I <sub>4</sub>	Synchronous Serial Port 0, receive data in			



MANE   NO.   NO.   Professional Content   No.   Professional Content   No.   No.   Professional Content   No.   No.	PW(1)			Table 5-1. Pin Functions (continued)			
SSPP_STD_   APT			TYPE <sup>(2)</sup>		DESCRIPTION		
SSP0_CSZ_0   AGS			0-	Synchronous Sorial Port 0, transmit data	nut.		
SSPO_CSE_2   A68							
SSP0_658_2   AG3							
UARTO_RXD							
UARTIC_RYSD			-		active low)		
UARTO CTS2				•			
UARTH CTSZ					val autorité (autòria laur)		
USB_DAT_N   C6   B <sub>B</sub>   USB D-IIO  PRO_NTZ   A68				-			
USB_DAT_P							
PMO_MYZ			-				
CWP_NINDEX         AP7         O <sub>S</sub> Color wheel index. Uses hysteresis           CWI_NIDEX         AP7         O <sub>S</sub> Color wheel index. Uses hysteresis           GENERAL PURPOSE ID (OPPO)®**         ALTERNATE PUNCTION 1         ALTERNATE FUNCTION 2           GPIO_82         E3         B <sub>S</sub> N/A         N/A           GPIO_81         AB10         B <sub>S</sub> IR_ENABLE (O)         N/A           GPIO_78         AE9         B <sub>S</sub> Reserved         N/A           GPIO_79         AE9         B <sub>S</sub> FELD_3D_LR(I)         N/A           GPIO_78         AE9         B <sub>S</sub> FELD_3D_LR(I)         N/A           GPIO_77         AB11         B <sub>S</sub> SAS_INTGITE_EN(O)         SENSE_PMM_OUT (O)           GPIO_78         AC10         B <sub>S</sub> BAS_CSZ (O)         N/A           GPIO_78         AC10         B <sub>S</sub> BAS_DI(I)         SENSE_CRETEQ_IN(I)           GPIO_74         AE10         B <sub>S</sub> SAS_DI(I)         SENSE_COMP_IN (I)           GPIO_72         K24         B <sub>S</sub> SSP2_CLK (B)         N/A           GPIO_71         K24         B <sub>S</sub> SSP2_CSZ_1 (B)         N/A           GPIO_72         K24         <							
CW_NDEX         AF7         O <sub>6</sub> Color wheel index_Uses hysteresis           GENERAL PURPOSE IO (QPIO)****         ALTERNATE PUNCTION 1         ALTERNATE FUNCTION 2           SPIO, S2         E3         B <sub>5</sub> N/A         N/A           GPIO, 81         A810         B <sub>2</sub> Reserved         N/A           GPIO, 78         A69         B <sub>2</sub> Reserved         N/A           GPIO, 78         A79         B <sub>3</sub> FIELD, 3D_LR (I)         N/A           GPIO, 78         A610         B <sub>2</sub> SAS_INTGR, EN (IO)         SINNE_PMM_OUT (IO)           GPIO, 76         AC10         B <sub>2</sub> SAS_DO (IO)         SENSE_FREQ_IN (I)           GPIO, 76         AD10         B <sub>2</sub> SAS_DO (IO)         SENSE_FREQ_IN (I)           GPIO, 73         AF10         B <sub>2</sub> SAS_DUI (I)         SENSE_COMP_IN (I)           GPIO, 72         K24         B <sub>2</sub> SSP2_CLK (B)         N/A           GPIO, 73         AF10         B <sub>2</sub> SSP2_CES_T. (B)         N/A           GPIO, 74         K23         B <sub>2</sub> SSP2_CES_T. (B)         N/A           GPIO, 81         J.26         B <sub>2</sub> SSP2_CES_T. (B)         N/A           GPIO, 79 <td></td> <td></td> <td>-</td> <td></td> <td>signal requires an external pullup. Uses hysteresis</td>			-		signal requires an external pullup. Uses hysteresis		
GENERAL PURPOSE ID (GPIO)   □   ALTERNATE FUNCTION 1							
GPIO_82         E3         B <sub>5</sub> NA         N/A           GPIO_81         A810         B <sub>2</sub> Rosenved         N/A           GPIO_81         A810         B <sub>2</sub> Reserved         N/A           GPIO_78         A69         B <sub>2</sub> Reserved         N/A           GPIO_78         A69         B <sub>2</sub> FIELD_3D_R(I)         N/A           GPIO_78         A611         B <sub>2</sub> SSS_INIGITE_RIN(0)         SENSE_PMM_OUT (0)           GPIO_70         A611         B <sub>2</sub> SAS_DO(0)         SENSE_PMM_OUT (0)           GPIO_73         A610         B <sub>2</sub> SAS_DO(0)         SENSE_COMP_IN (I)           GPIO_74         A610         B <sub>2</sub> SAS_DO(0)         SENSE_COMP_IN (I)           GPIO_73         A610         B <sub>2</sub> SAS_DO(0)         N/A           GPIO_73         A610         B <sub>2</sub> SAS_DO(0)         N/A           GPIO_74         A623         B <sub>2</sub> SSP2_COLK(B)         N/A           GPIO_71         K23         B <sub>2</sub> SSP2_COLK(B)         N/A           GPIO_71         K22         B <sub>2</sub> SSP2_COLK_B)         N/A           GPIO_75         J24         B <sub>2</sub>				· ·			
GPIO_81							
GPIO_80         AD9         B₂         IR_ENABLE (O)         N/A           GPIO_79         AE9         B₂         Reserved         N/A           GPIO_79         AE9         B₂         RESERVED         N/A           GPIO_77         AB11         B₂         SAS_INTGTR_EN (O)         SENSE_PMM_OUT (O)           GPIO_76         AC10         B₂         SAS_CSZ (O)         N/A           GPIO_78         AD10         B₂         SAS_DQ (O)         SENSE_REE_IN (I)           GPIO_73         AP10         B₂         SAS_CLK (O)         N/A           GPIO_73         AP10         B₂         SAS_CLK (O)         N/A           GPIO_71         K23         B₂         SSP2_CES_T (B)         N/A           GPIO_70         K22         B₂         SSP2_CES_T (B)         N/A           GPIO_70         K22         B₂         SSP2_CES_T (B)         N/A           GPIO_88         J25         B₂         SSP2_CES_T (B)         N/A           GPIO_89         J24         B₂         SSP2_DO (O)         N/A           GPIO_80         J22         B₂         SSP_DOB_T (O)         SSP2_CES_T (B)           GPIO_80         J22         B₂         SP_DOB_T							
GPIO_79							
GPIO_76	GPIO_80	AD9	B <sub>2</sub>	IR_ENABLE (O)	N/A		
GPIO_77         AB11         B₂         SAS_INTGTR_EN(O)         SENSE_PWM_OUT(O)           GPIO_76         AC10         B₂         SAS_CSZ (O)         NA           GPIO_76         AC10         B₂         SAS_DO (O)         SENSE_FRO_IN (I)           GPIO_73         AF10         B₂         SAS_DI (I)         SENSE_COMP_IN (I)           GPIO_73         AF10         B₂         SAS_CLK (O)         NA           GPIO_71         K23         B₂         SSP2_CLK (B)         NA           GPIO_71         K23         B₂         SSP2_CLK (B)         NA           GPIO_70         K22         B₂         SSP2_CSZ_1 (B)         NA           GPIO_60         J26         B₂         SSP2_CSZ_0 (B)         NA           GPIO_61         J22         B₂         SSP2_CSZ_0 (B)         NA           GPIO_66         J23         B₂         SSP_Data_6 (O)         SSP2_CSZ_2 (B)           GPIO_68         J23         B₂         SSP_Data_6 (O)         SSP2_CSZ_2 (B)           GPIO_69         J22         B₂         SSP_Data_5 (O)         NA           GPIO_61         J23         B₂         SSP_Data_5 (O)         NA           GPIO_63         J22         B₂	GPIO_79	AE9	B <sub>2</sub>	Reserved	N/A		
GPIO_76         AC10         B₂         SAS_CSZ(O)         N/A           GPIO_76         AD10         B₂         SAS_DO (O)         SENSE_FREQ_IN()           GPIO_74         AF10         B₂         SAS_DI (I)         SENSE_COMP_IN (I)           GPIO_73         AF10         B₂         SAS_CIX (O)         N/A           GPIO_71         K24         B₂         SSP2_DI (I)         N/A           GPIO_71         K23         B₂         SSP2_CSZ_I (B)         N/A           GPIO_70         K22         B₂         SSP2_CSZ_I (B)         N/A           GPIO_69         J.28         B₂         SSP2_CSZ_I (B)         N/A           GPIO_69         J.28         B₂         SSP2_CSZ_I (B)         N/A           GPIO_68         J.25         B₂         SSP2_CSC_I (B)         N/A           GPIO_68         J.21         B₂         SP_Data_T (O)         SSP2_CSZ_2 (B)           GPIO_68         J.23         B₂         SP_Data_A (O)         SSP2_CSZ_2 (B)           GPIO_69         J.22         B₂         SP_Data_A (O)         GV_PMM_2 (O)           GPIO_69         J.22         B₂         SP_Data_A (O)         GV_MNDEX_2 (I)           GPIO_69         H24	GPIO_78	AF9	B <sub>2</sub>	FIELD_3D_LR (I)	N/A		
GPIO_75         AD10         B₂         SAS_DO (O)         SENSE_FREQ_IN (I)           GPIO_74         AE10         B₂         SAS_DI (I)         SENSE_COMP_IN (I)           GPIO_73         AF10         B₂         SAS_CLK (O)         N/A           GPIO_73         K24         B₂         SSP2_DI (I)         N/A           GPIO_71         K23         B₂         SSP2_CLK (B)         N/A           GPIO_70         K22         B₂         SSP2_CSZ_C (B)         N/A           GPIO_68         J25         B₂         SSP2_CSZ_C (B)         N/A           GPIO_68         J25         B₂         SSP2_DO(O)         N/A           GPIO_68         J24         B₂         SSP2_DO(O)         N/A           GPIO_69         J24         B₂         SP_Data_F (O)         SSP2_CSZ_C (B)           GPIO_69         J24         B₂         SP_Data_F (O)         SSP2_CSZ_C (B)           GPIO_61         J23         B₂         SP_Data_F (O)         SSP2_CSZ_C (B)           GPIO_64         H28         B₂         SP_Data_F (O)         SSP2_CSZ_C (B)           GPIO_65         J22         B₂         SP_Data_F (O)         N/A           GPIO_61         H23 <t< td=""><td>GPIO_77</td><td>AB11</td><td>B<sub>2</sub></td><td>SAS_INTGTR_EN (O)</td><td>SENSE_PWM_OUT (0)</td></t<>	GPIO_77	AB11	B <sub>2</sub>	SAS_INTGTR_EN (O)	SENSE_PWM_OUT (0)		
SPIO_74	GPIO_76	AC10	B <sub>2</sub>	SAS_CSZ (O)	N/A		
GPIO_73         AF10         B₂         SAS_CLK (O)         N/A           GPIO_72         K24         B₂         SSP2_DI (I)         N/A           GPIO_71         K23         B₂         SSP2_CSZ_I (B)         N/A           GPIO_70         K22         B₂         SSP2_CSZ_I (B)         N/A           GPIO_69         J26         B₂         SSP2_CSZ_0 (B)         N/A           GPIO_68         J25         B₂         SSP2_CSZ_0 (B)         N/A           GPIO_68         J25         B₂         SSP2_CSZ_0 (B)         N/A           GPIO_68         J25         B₂         SSP2_DO (O)         N/A           GPIO_68         J23         B₂         SSP_Data_6 (O)         SSP2_CSZ_2 (B)           GPIO_69         J24         B₂         SP_Data_6 (O)         SSP2_CSZ_2 (B)           GPIO_69         J22         B₂         SP_Data_6 (O)         SSP2_CSZ_2 (B)           GPIO_69         J22         B₂         SP_Data_5 (O)         N/A           GPIO_69         H26         B₂         SP_Data_5 (O)         N/A           GPIO_61         H25         B₂         SP_Data_2 (O)         N/A           GPIO_61         H23         B₂         SP_D	GPIO_75	AD10	B <sub>2</sub>	SAS_DO (O)	SENSE_FREQ_IN (I)		
GPIO_72   K24	GPIO_74	AE10	B <sub>2</sub>	SAS_DI (I)	SENSE_COMP_IN (I)		
GPIO_71	GPIO_73	AF10	B <sub>2</sub>	SAS_CLK (O)	N/A		
GPIO_70   K22   B2   SSP2_CSZ_1 (B)   N/A	GPIO_72	K24	B <sub>2</sub>	SSP2_DI (I)	N/A		
GPIO_68   J26   B2   SSP2_CSZ_0 (B)   NIA	GPIO_71	K23	B <sub>2</sub>	SSP2_CLK (B)	N/A		
GPIO_68         J25         B2         SSP2_DO (0)         N/A           GPIO_67         J24         B2         SP_Data_7 (0)         SSP2_CSZ_2 (B)           GPIO_68         J23         B2         SP_Data_6 (0)         SSP0_CSZ_5 (B)           GPIO_66         J22         B2         SP_Data_5 (0)         N/A           GPIO_65         J22         B2         SP_Data_5 (0)         CW_PWM_2 (0)           GPIO_68         H26         B2         SP_Data_4 (0)         CW_PWM_2 (0)           GPIO_69         H26         B2         SP_Data_3 (0)         CW_INDEX_2 (I)           GPIO_69         H24         B2         SP_Data_2 (0)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_1 (0)         N/A           GPIO_69         G26         B2         SP_Data_0 (0)         N/A           GPIO_59         G26         B2         SP_VMG_CLK (0)         N/A           GPIO_59         G26         B2         SP_WG_CLK (0)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_58         G24         B2         UART2_RXD (0)         N/A           GPIO_59         G23         B2<	GPIO_70	K22	B <sub>2</sub>	SSP2_CSZ_1 (B)	N/A		
GPIO_67         J24         B2         SP_Data_7 (O)         SSP2_CSZ_2 (B)           GPIO_66         J23         B2         SP_Data_6 (O)         SSP0_CSZ_5 (B)           GPIO_65         J22         B2         SP_Data_5 (O)         N/A           GPIO_64         H26         B2         SP_Data_4 (O)         CW_PWM_2 (O)           GPIO_63         H25         B2         SP_Data_3 (O)         CW_INDEX_2 (I)           GPIO_69         H24         B2         SP_Data_2 (O)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_1 (O)         N/A           GPIO_60         H22         B2         SP_Data_0 (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_59         G26         B2         LED_SENSE_PULSE (O)         N/A           GPIO_59         G26         B2         UART2_RXD (O)         N/A           GPIO_59         G23         B2         UART2_RXD (O)         N/A           GPIO_59         G24         B2         UART2_RXD (O)         N/A           GPIO_50         G23	GPIO_69	J26	B <sub>2</sub>	SSP2_CSZ_0 (B)	N/A		
GPIO_67         J24         B2         SP_Data_7 (O)         SSP2_CSZ_2 (B)           GPIO_68         J23         B2         SP_Data_6 (O)         SSP0_CSZ_5 (B)           GPIO_65         J22         B2         SP_Data_5 (O)         N/A           GPIO_64         H26         B2         SP_Data_4 (O)         CW_PWM_2 (O)           GPIO_63         H25         B2         SP_Data_3 (O)         CW_INDEX_2 (I)           GPIO_62         H24         B2         SP_Data_2 (O)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_2 (O)         N/A           GPIO_69         H22         B2         SP_Data_0 (O)         N/A           GPIO_69         G26         B2         SP_WG_CLK (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_59         G26         B2         LED_SENSE_PULSE (O)         N/A           GPIO_59         G26         B2         UART2_RXD (O)         N/A           GPIO_59         G26         B2         UART2_RXD (O)         N/A           GPIO_59         G26         B2         UART2_RXD (O)         N/A           GPIO_50         G23	GPIO_68	J25	B <sub>2</sub>	SSP2_DO (O)	N/A		
GPIO_66         J23         B2         SP_Data_6 (O)         SSPO_CSZ_5 (B)           GPIO_65         J22         B2         SP_Data_5 (O)         N/A           GPIO_64         H26         B2         SP_Data_4 (O)         CW_PVM_2 (O)           GPIO_63         H25         B2         SP_Data_3 (O)         CW_INDEX_2 (I)           GPIO_62         H24         B2         SP_Data_2 (O)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_0 (O)         N/A           GPIO_61         H22         B2         SP_Data_0 (O)         N/A           GPIO_60         H22         B2         SP_Data_0 (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_56         G24         B2         UART2_RXD (O)         N/A           GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_6 (O)         N/A           GPIO_53         E26         B2	GPIO_67	J24		SP_Data_7 (O)	SSP2_CSZ_2 (B)		
GPIO_65         J22         B2         SP_Data_5 (O)         N/A           GPIO_64         H26         B2         SP_Data_4 (O)         CW_PWM_2 (O)           GPIO_63         H25         B2         SP_Data_3 (O)         CW_INDEX_2 (I)           GPIO_62         H24         B2         SP_Data_2 (O)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_1 (O)         N/A           GPIO_69         G26         B2         SP_WG_CLK (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_56         G24         B2         UART2_RXD (O)         N/A           GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_F (O)         N/A           GPIO_53         E26         B2         PROG_AUX_F (O)         N/A           GPIO_54         F26         B2         PROG_AUX_F (O)         N/A           GPIO_52         AB12         B2         CSP	GPIO_66	J23		SP_Data_6 (O)	SSP0_CSZ_5 (B)		
GPIO_64         H26         B2         SP_Data_4 (O)         CW_PWM_2 (O)           GPIO_63         H25         B2         SP_Data_3 (O)         CW_INDEX_2 (I)           GPIO_62         H24         B2         SP_Data_2 (O)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_1 (O)         N/A           GPIO_60         H22         B2         SP_Data_0 (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_58         G25         B2         Reserved         N/A           GPIO_59         F25         B2         Reserved         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_58         G24         B2         UART2_RXD (O)         N/A           GPIO_59         F25         B2         Reserved         N/A           GPIO_55         G23         B2         UART2_RXD (O)         N/A           GPIO_54         F26         B2         PROG_	GPIO 65	J22		SP Data 5 (O)	N/A		
GPIO_63         H25         B2         SP_Data_3 (O)         CW_INDEX_2 (I)           GPIO_62         H24         B2         SP_Data_2 (O)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_1 (O)         N/A           GPIO_60         H22         B2         SP_Data_0 (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_57         F25         B2         UARTZ_RXD (O)         N/A           GPIO_55         G23         B2         UARTZ_TXD (O)         N/A           GPIO_55         G23         B2         UARTZ_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (O)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (O)         N/A           GPIO_54         F26         B2         PROG_AUX_6 (O)         N/A           GPIO_55         AB12         B2         CSP_Data (O)         ALF_CAMP (O)           GPIO_54         AC1         B2         Rese		H26	1		CW PWM 2 (O)		
GPIO_62         H24         B2         SP_Data_2 (O)         SP_VC_FDBK (I)           GPIO_61         H23         B2         SP_Data_1 (O)         N/A           GPIO_60         H22         B2         SP_Data_0 (O)         N/A           GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_56         G24         B2         UART2_RXD (O)         N/A           GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (O)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (O)         N/A           GPIO_55         AB12         B2         CSP_Data (O)         N/A           GPIO_54         F26         B2         PROG_AUX_6 (O)         N/A           GPIO_55         AB12         B2         CSP_CLK (O)         ALF_CLAMP (O)           GPIO_54         F26         B2         Reserved         HBT_CLKOUT (O)           GPIO_55         AB12         B2         Reserved							
GPIO_61         H23         B2         SP_Data_1 (0)         NIA           GPIO_60         H22         B2         SP_Data_0 (0)         NIA           GPIO_59         G26         B2         SP_WG_CLK (0)         NIA           GPIO_58         G25         B2         LED_SENSE_PULSE (0)         NIA           GPIO_57         F25         B2         Reserved         NIA           GPIO_56         G24         B2         UART2_RXD (0)         NIA           GPIO_55         G23         B2         UART2_RXD (0)         NIA           GPIO_54         F26         B2         PROG_AUX_7 (0)         NIA           GPIO_53         E26         B2         PROG_AUX_7 (0)         NIA           GPIO_55         AB12         B2         CSP_Data (0)         NIA           GPIO_54         F26         B2         PROG_AUX_7 (0)         NIA           GPIO_55         AB12         B2         CSP_Data (0)         ALF_CLAMP (0)           GPIO_50         AB12         B2         CSP_CLK (0)         ALF_CLAMP (0)           GPIO_51         AC11         B2         CSP_CLK (0)         ALF_CLAMP (0)           GPIO_50         V23         B2         Reserve		H24					
GPIO_60         H22         B2         SP_Data_0 (0)         N/A           GPIO_59         G26         B2         SP_WG_CLK (0)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (0)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_56         G24         B2         UART2_RXD (0)         N/A           GPIO_55         G23         B2         UART2_TXD (0)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (0)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (0)         N/A           GPIO_52         AB12         B2         CSP_Data (0)         ALF_CLAMP (0)           GPIO_51         AC11         B2         CSP_CLK (0)         ALF_COAST (0)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (0)           GPIO_49         V24         B2         Reserved         HBT_OL (N)           GPIO_48         V25         B2         Reserved         HBT_OL (I)           GPIO_46         T22         B2         Reserved         HBT_OL (I)           GPIO_45         U23         B2         Reser							
GPIO_59         G26         B2         SP_WG_CLK (O)         N/A           GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_56         G24         B2         UART2_RXD (O)         N/A           GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (O)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (O)         N/A           GPIO_52         AB12         B2         CSP_Data (O)         ALF_CLAMP (O)           GPIO_51         AC11         B2         GSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_58         G25         B2         LED_SENSE_PULSE (O)         N/A           GPIO_57         F25         B2         Reserved         N/A           GPIO_56         G24         B2         UART2_RXD (O)         N/A           GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (O)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (O)         N/A           GPIO_52         AB12         B2         CSP_Data (O)         ALF_CLAMP (O)           GPIO_51         AC11         B2         CSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_DI_2 (I)           GPIO_47         V26         B2         Reserved         HBT_DL_2 (I)           GPIO_45         U23         B2         Reserved         HBT_DL_1 (I)           GPIO_44         U24         B2         Reserved         HBT_DL (KIN_0 (I)							
GPIO_57         F25         B2         Reserved         N/A           GPIO_56         G24         B2         UART2_RXD (O)         N/A           GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (O)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (O)         N/A           GPIO_52         AB12         B2         CSP_Data (O)         ALF_CLAMP (O)           GPIO_51         AC11         B2         CSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_DL2 (I)           GPIO_47         V26         B2         Reserved         HBT_DL2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_56         G24         B2         UART2_RXD (O)         N/A           GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (O)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (O)         N/A           GPIO_52         AB12         B2         CSP_Data (O)         ALF_CLAMP (O)           GPIO_51         AC11         B2         CSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_D_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_55         G23         B2         UART2_TXD (O)         N/A           GPIO_54         F26         B2         PROG_AUX_7 (O)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (O)         N/A           GPIO_52         AB12         B2         CSP_Data (O)         ALF_CLAMP (O)           GPIO_51         AC11         B2         CSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_DL_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DL_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (II)							
GPIO_54         F26         B2         PROG_AUX_7 (0)         N/A           GPIO_53         E26         B2         PROG_AUX_6 (0)         N/A           GPIO_52         AB12         B2         CSP_Data (0)         ALF_CLAMP (0)           GPIO_51         AC11         B2         CSP_CLK (0)         ALF_COAST (0)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (0)           GPIO_49         V24         B2         Reserved         HBT_DO (0)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_DI_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DI_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (II)							
GPIO_53         E26         B2         PROG_AUX_6 (0)         N/A           GPIO_52         AB12         B2         CSP_Data (O)         ALF_CLAMP (O)           GPIO_51         AC11         B2         CSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_DI_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DI_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_52         AB12         B2         CSP_Data (O)         ALF_CLAMP (O)           GPIO_51         AC11         B2         CSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_DL2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DL1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (II)							
GPIO_51         AC11         B2         CSP_CLK (O)         ALF_COAST (O)           GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_D_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_D_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_50         V23         B2         Reserved         HBT_CLKOUT (O)           GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_D1_2 (I)           GPIO_48         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_48         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_D1_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_49         V24         B2         Reserved         HBT_DO (O)           GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_DI_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DI_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_48         V25         B2         Reserved         HBT_CLKIN_2 (I)           GPIO_47         V26         B2         Reserved         HBT_DI_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DI_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)			1				
GPIO_47         V26         B2         Reserved         HBT_DI_2 (I)           GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DI_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_46         T22         B2         Reserved         HBT_CLKIN_1 (I)           GPIO_45         U23         B2         Reserved         HBT_DI_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_45         U23         B2         Reserved         HBT_DI_1 (I)           GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
GPIO_44         U24         B2         Reserved         HBT_CLKIN_0 (I)							
	GPIO_45	U23		Reserved	HBT_DI_1 (I)		
GPIO_43         U25         B2         Reserved         HBT_DI_0 (I)				Reserved	HBT_CLKIN_0 (I)		
	GPIO_43	U25	B <sub>2</sub>	Reserved	HBT_DI_0 (I)		



PIN <sup>(1)</sup>			Table 5-1. Pin Functions (continued)			
NAME NO.	TYPE <sup>(2)</sup>		DESCRIPTION			
GPIO_42	U26	B <sub>2</sub>	Reserved	SSP0_CSZ4 (B)		
GPIO_41	R22	B <sub>2</sub>	Reserved	DASYNC (I)		
GPIO_40	T23	B <sub>2</sub>	Reserved	FSD12 (O)		
GPIO_39	F24	B <sub>2</sub>	SW reserved (Boot Hold)	SW reserved (Boot Hold)		
GPIO_38	E25	B <sub>2</sub>	SW reserved (USB Enumeration Enable)	SW reserved (USB Enumeration Enable)		
GPIO_37	G22	B <sub>2</sub>	N/A	N/A		
GPIO_36	A12	B <sub>2</sub>	PM_ADDR_22 (O)	I2C_2 SDA (B)		
GPIO_35	E11	B <sub>2</sub>	PM_ADDR_21 (O)	I2C_2 SCL (B)		
GPIO_34	F23	B <sub>2</sub>	SSP1_CSZ_1 (B)	N/A		
GPIO_33	D26	B <sub>2</sub>	SSP1_CSZ_0 (B)	N/A		
GPIO_32	E24	B <sub>2</sub>	SSP1_DO (O)	N/A		
GPIO_31	F22	B <sub>2</sub>	SSP1_DI (I)	N/A		
GPIO_30	D25	B <sub>2</sub>	SSP1_CLK (B)	N/A		
GPIO_29	E23	B <sub>2</sub>	IR1 (I)	SSP2 BC CSZ (B)		
GPIO_28	C26	B <sub>2</sub>	IR0 (I)	SSP2 BC CSZ (B)		
GPIO_27	AB4	B <sub>2</sub>	SSP0_CSZ3 (B)	N/A		
GPIO_26	D24	B <sub>2</sub>	Blue LED enable (O)	UART2 TXD (O)		
GPIO_25	C25	B <sub>2</sub>	Green LED enable (O)	LAMPSYNC (O)		
GPIO_24	B26	B <sub>2</sub>	Red LED enable (O)	N/A		
GPIO_23	E21	B <sub>2</sub>	LED Dual Current Control (O)	N/A		
GPIO_22	D22	B <sub>2</sub>	LED Dual Current Control (O)	N/A		
GPIO_21	E20	B <sub>2</sub>	LED Dual Current Control (O)	N/A		
GPIO_20	C23	B <sub>2</sub>	N/A	N/A		
GPIO_19	D21	B <sub>2</sub>	N/A	N/A		
GPIO_18	B24	B <sub>2</sub>	N/A	N/A		
GPIO_17	C22	B <sub>2</sub>	General Purpose Clock 2 (O)	N/A		
GPIO_16	B23	B <sub>2</sub>	General Purpose Clock 1 (O)	N/A		
GPIO_15	E19	B <sub>2</sub>	I2C_1 SDA (B)	N/A		
GPIO_14	D20	B <sub>2</sub>	I2C_1 SCL (B)	N/A		
GPIO_13	C21	B <sub>2</sub>	PWM IN_1 (I)	I2C_2 SDA (B)		
GPIO_12	B22	B <sub>2</sub>	PWM IN_0 (I)	I2C_2 SCL (B)		
GPIO_11	A23	B <sub>2</sub>	PWM STD 7 (O)	N/A		
GPIO_10	A22	B <sub>2</sub>	PWM STD_6 (O)	N/A		
GPIO_10	B21	_	PWM STD_5 (O)	N/A		
GPIO_9	A21	B <sub>2</sub>		N/A		
GPIO_7	A20	B <sub>2</sub>	PWM STD_4 (O) PWM STD_3 (O)	N/A		
GPIO_7	C20	B <sub>2</sub>	PWM STD_3 (0)	N/A		
GPIO_6	B20	B <sub>2</sub>	PWM STD_1 (O)	N/A		
GPIO_5	B19	_	PWM STD_1 (O) PWM STD 0 (O)	N/A		
GPIO_4 GPIO_3	A19	B <sub>2</sub>		N/A N/A		
GPIO_3 GPIO 2		B <sub>2</sub>	UART1_RTSZ (0)	N/A N/A		
GPIO_2 GPIO_1	E18	B <sub>2</sub>	UART1_CTSZ (I)	N/A N/A		
		B <sub>2</sub>	UART1_RXD (I)			
GPIO_0	C19	B <sub>2</sub>	UART1_TXD (O)	N/A		
MOSC	M26	I <sub>10</sub>	System clock oscillator input (3.3-V LVTTL). transitions from low to high.	Note that MOSC must be stable a maximum of 25 ms after POSENSE		
MOSCN	N26	O <sub>10</sub>	MOSC crystal return			
OCLKA	AF6	O <sub>10</sub>	General purpose output clock A. Targeted for driving the CW motor controller. The frequency is software programmable. Power-up default 787 KHz. Note that the output frequency is not affected by non-power-up reset operations (it will hold the last value programmed).			
DUAL CONTROLLI	ER SUPPORT		1 , 3/-			
SEQ_SYNC	AB9	B <sub>3</sub>	Sequence sync. This signal is used in multi-controller configurations only, in which case the SEQSYNC signal from each controller is connected together with an external pullup. This signal is either pulled high or pulled low and not allowed to float for single controller configurations.			
POWER and GROU	POWER and GROUND					

PIN <sup>(1)</sup>				
NAME	NO.	TYPE <sup>(2)</sup>	DESCRIPTION	
VDD33	F20, F17, F11, F8, L21, R21, Y21, AA19, AA16, AA10, AA7	POWER	3.3-V I/O power	
VDD18	C1, F5, G6, K6, M5, P5, T5, W6, AA5, AE1, H5, N6, T6, AA13, U21, P21, H21, F14	POWER	1.8-V internal DRAM and LVDS I/O power	
VDD11	F19, F16, F13, F10, F7, H6, L6, P6, U6, Y6, AA8, AA11, AA14, AA17, AA20, W21, T21, N21, K21, G21, L11, T11, T16, L16	POWER	1.1-V core power	
VDD_PLLD	L22	POWER	1.1-V DMD clock generator PLL digital power	
VSS_PLLD	L23	GROUND	1.1-V DMD clock generator PLL digital ground	
VAD_PLLD	K25	POWER	1.8-V DMD clock generator PLL analog power	
VAS_PLLD	K26	GROUND	1.8-V DMD clock generator PLL analog ground	
VDD_PLLM1	L26	POWER	1.1-V master-LS clock generator PLL digital power	
VSS_PLLM1	M22	GROUND	1.1-V master-LS clock generator PLL digital ground	
VAD_PLLM1	L24	POWER	1.8-V master-LS clock generator PLL analog power	
VAS_PLLM1	L25	GROUND	1.8-V master-LS clock generator PLL analog ground	
VDD_PLLM2	P23	POWER	1.1-V master-HS clock generator PLL digital power	
VSS_PLLM2	P24	GROUND	1.1-V master-HS clock generator PLL digital ground	
VAD_PLLM2	R25	POWER	1.8-V master-HS clock generator PLL analog power	
VAS_PLLM2	R26	GROUND	1.8-V master-HS clock generator PLL analog ground	
VAD_PLLS	R23	POWER	1.1-V video-2X clock generator PLL analog power	
VAS_PLLS	R24	GROUND	1.1-V video-2X clock generator PLL analog ground	
L-VDQPAD_[7:0], R-VDQPAD_[7:0]	B18, D18, B17, E17, A18, C18, A17, D17, AE17, AC17, AF17, AC18, AB16, AD17, AB17, AD18	RESERVED	These pins have to be tied directly to ground for normal operation.	
CFO_VDD33	AE26	RESERVED	This pin has to be tied directly to 3.3 I/O power (VDD33) for normal operation.	
VTEST1, VTEST2, VTEST3, VTEST4	AB14, AB15, E15, E16	RESERVED	These pins have to be tied directly to ground for normal operation.	
LVDS_AVS1, LVDS_AVS2	V5, K5	POWER	These pins have to be tied directly to ground for normal operation.	
VPGM	AC6	POWER	This pin has to be tied directly to ground for normal operation.	



PII	N <sup>(1)</sup>	TYPE(2)	DESCRIPTION
NAME	NO.	ITPE-	DESCRIPTION
GROUND	A26, A25, A24, B25, C24, D23, E22, F21, F18, F15, F12, F9, F6, E5, D4, C3, B3, A3, B2, A2, B1, A1 G5, J5, J6, L5, M6, N5, R5, R6, U5, V6, W5, Y5, AA6, AB5, AC4, AD3, AE3, AF3, AF2, AF1, AA9, AA12, AA15, AA24, AE24, AE24, AE25, AF24, AE25, AF26, AF26, AF26, AF26, AF26, AF27, M21, J21, L15, L14, L13, L12, M16, M15, M14, M13, M12, M11, N16, N15, N14, N13, N12, N11, P16, P15, P14, P13, P12, P11, R16, R15, R14, R13, R12, R11, T15, T14, T13, T12	GROUND	Common ground

- For instructions on handling unused pins, see General Handling Guidelines for Unused CMOS-Type Pins.
- I/O Type: I = Input. O = Output. B = Bidirectional, and H = Hysteresis. See Table 5-2 for subscript explanation. (2)
- All JTAG signals are LVTTL compatible.
- Ports 1 and 2 can each be used to support multiple source options for a given product (for example AFE and HDMI). To do so, the data bus from both source components must be connected to the same port pins (1 or 2) and control given to the DLPC4420 device to tristate the "inactive" source. Tying them together like this causes some signal degradation due to reflections on the tristated path. Given the clock is the most critical signal, three Port clocks (1, 2, and 3) are provided to provide an option to improve the signal integrity.
- Ports 1 and 2 can be used separately as two 30-bit ports, or can be combined into one 60-bit port (typically for high data rate sources) (5) for transmission of two pixels per clock.
- The A, B, C input data channels of Ports 1 and 2 can be internally reconfigured/remapped for optimum board layout.
- Sources feeding less than the full 10-bits per color component channel have to be MSB justified when connected to the DLPC4420 controller and the LSBs tied off to zero. For example an 8-bit per color input has to be connected to bits 9:2 of the corresponding A, B, C input channel.
- GPIO signals must be configured by software for input, output, bidirectional, or open-drain. Some GPIOs have one or more alternate use modes, which are also software configurable. The reset default for all optional GPIOs is as an input signal. However, any alternate function connected to these GPIO pins with the exception of general-purpose clocks and PWM generation, are reset. An external pullup to the 3.3-V supply is required for each signal configured as open-drain. External pullup or pulldown resistors may be required to ensure stable operation before software is able to configure these ports.

### Table 5-2. I/O Type Subscript Definition

SUBSCRIPT	DESCRIPTION	ESD STRUCTURE
2	3.3-V LVTTL I/O buffer with 8-mA drive	
3	3.3-V LVTTL I/O buffer with 12-mA drive	
4	3.3-V LVTTL receiver	
5	3.3-V LVTTL I/O buffer with 8-mA drive, with slew rate control	
6	3.3-V LVTTL I/O buffer, with programmable 4-mA, 8-mA, or 12-mA drive	ESD diode to VDD33 and GROUND
7	1.8-V LVDS (DMD I/F)	
8	3.3-V I <sup>2</sup> C with 3 mA sink	
9	USB Compatible (3.3 V)	
10	OSC 3.3-V I/O Compatible LVTTL	

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# 6 Specifications

### **6.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
ELECTRICAL				
	V <sub>DD11</sub> (Core)	-0.30	1.60	
	V <sub>DD18</sub> (LVDS I/O and Internal DRAM)	-0.30	2.50	
	V <sub>DD33</sub> (I/O)	-0.30	3.90	
	VDD_PLLD (1.1-V DMD clock generator - Digital)	-0.30	1.60	
	VDD_PLLM1 (1.1-V Master - LS clock generator - Digital)	-0.30	1.60	
Supply Voltage <sup>(1)</sup>	VDD_PLLM2 (1.1-V Master - HS clock generator - Digital)	-0.30	1.60	V
	VDD_PLLD (1.8-V DMD clock generator - Analog)	-0.30	2.50	
	VDD_PLLM1 (1.8-V Master - LS clock generator - Analog)	-0.30	2.50	
	VDD_PLLM2 (1.8-V Master - HS clock generator - Analog)	-0.30	2.50	
	VDD_PLLS (1.1-V Video 2X - Analog)	-0.50	1.40	
	USB	-1.0	5.25	
/ <sub>I</sub> Input Voltage <sup>(2)</sup>	OSC	-0.3	V <sub>DD33</sub> + 0.3	
input voltage(=)	3.3-V LVTTL	-0.3	3.6	v
	3.3-V I2C	-0.5	3.8	
	USB	-1.0	5.25	
/ <sub>○</sub> Output Voltage	osc	-0.3	2.2	
0 Output voltage	3.3-V LVTTL	-0.3	3.6	v
	3.3-V I2C	-0.5	3.8	
ENVIRONMENTAL	·			
J operating junction temp	perature	0	111	°C
storage temperature	range	-40	125	°C

<sup>(1)</sup> All voltage values are with respect to GROUND.

### 6.2 ESD Ratings

			VALUE	UNIT
V Electron to the disease	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	± 1000	V
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	+500/–300	V

<sup>(1)</sup> Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### **6.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

	I/O <sup>(1)</sup>	MIN NOM	MAX	UNIT
ELECTRICAL				

<sup>(2)</sup> Applies to external input and bidirectional buffers

<sup>(2)</sup> Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



over operating free-air temperature range (unless otherwise noted)

		I/O <sup>(1)</sup>	MIN	NOM	MAX	UNIT
V <sub>DD33</sub>	3.3-V supply voltage, I/O		3.135	3.3	3.465	V
V <sub>DD18</sub>	1.8-V supply voltage, LVDS and DRAM		1.71	1.8	1.89	V
V <sub>DD11</sub>	1.1-V supply voltage, core logic		1.045	1.1	1.155	V
VDD_PLLD	1.8-V supply voltage, PLL analog		1.71	1.8	1.89	V
VDD_PLLM1	1.8-V supply voltage, PLL analog		1.71	1.8	1.89	V
VDD_PLLM2	1.8-V supply voltage, PLL analog		1.71	1.8	1.89	V
VDD_PLLS	1.8-V supply voltage, PLL Analog		1.050	1.10	1.150	V
VDD_PLLD	1.8-V supply voltage, PLL analog		1.045	1.1	1.155	V
VDD_PLLM1	1.8-V supply voltage, PLL analog		1.045	1.1	1.155	V
VDD_PLLM2	1.8-V supply voltage, PLL analog		1.045	1.1	1.155	V
		USB (9)	0		V <sub>DD33</sub>	
.,	Innut voltage	OSC (10)	0		V <sub>DD33</sub>	V
VI	Input voltage	3.3-V LVTTL (1,2,3,4)	0		V <sub>DD33</sub>	V
		3.3-V I <sup>2</sup> C (8)	0		V <sub>DD33</sub>	
		USB (8)	0		$V_{DD33}$	
.,	Output voltage	3.3-V LVTTL (1,2,3,4)	0		$V_{DD33}$	V
Vo	Output voltage	3.3-V I <sup>2</sup> C (8)	0		V <sub>DD33</sub>	V
		1.8-V LVDS (7)	0		V <sub>DD33</sub>	
T <sub>A</sub>	Operating ambient temperature range	See <sup>(2) (3)</sup>	0		55	°C
T <sub>C</sub>	Operating top center case temperature	See <sup>(3) (4)</sup>	0		109.16	°C
TJ	Operating junction temperature		0		111	°C

- (1) The number inside each parenthesis for the I/O refers to the type defined in the I/O type subscript definition section.
- (2) Assumes minimum 1 m/s airflow along with the JEDEC thermal resistance and associated conditions listed at www.ti.com/packaging. Thus, this is an approximate value that varies with environment and PCB design.
- (3) Maximum thermal values assume max power of 4.6 watts.
- (4) Assume Psi<sub>JT</sub> equals 0.4 C/W

#### 6.4 Thermal Information

		DLPC4420	
	THERMAL METRIC <sup>(1)</sup>	ZPC (BGA)	UNIT
		516 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	14.4	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	4.4	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics Application Report.

#### 6.5 Electrical Characteristics

over recommended operating conditions

	PAF	RAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USB (9)		2.0			
	High-level input	OSC (10)		2.0			] ,,
V <sub>IH</sub>	voltage	3.3-V LVTTL (1,2,3,4)		2.0			] <b>'</b>
		3.3-V I <sup>2</sup> C (8)		2.4		VDD33V <sub>DD33</sub> +0.5	

Product Folder Links: DLPC4420

<sup>(2)</sup> In still air



### **6.5 Electrical Characteristics (continued)**

over recommended operating conditions

	PAF	RAMETER	TEST CONDITIONS	MIN	ТҮР	MA	X UNI
		USB (9)				0	.8
	Low-level input	OSC (10)				0	.8
$V_{IL}$	voltage	3.3-V LVTTL (1,2,3,4)				0	.8 V
		3.3-V I <sup>2</sup> C (8)		-0.5		1	.0
V <sub>DIS</sub>	Differential Input Voltage	USB(9)		200			mV
V <sub>ICM</sub>	Differential cross point voltage	USB(9)		0.8		2	.5 V
		USB(9)		200			
$V_{HYS}$	Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )	3.3-V LVTTL (1,2,3,4)			400		mV
	v  -/	3.3-V I <sup>2</sup> C (8)		300	550	60	00
		USB (9)		2.8			
$V_{OH}$	High-level output	1.8-V LVDS (7)		1.520			
VOH	voltage	3.3-V LVTTL (1,2,3)	I <sub>OH</sub> = Max Rated	2.7			
	Low-level output voltage	USB (9)		0.0		0	.3
		1.8-V LVDS (7)				0.88	80
V <sub>OL</sub>		3.3-V LVTTL (1,2,3)	I <sub>OL</sub> = Max Rated			0	.4 V
		3.3-V I <sup>2</sup> C (8)	I <sub>OL</sub> = 3-mA sink			0	.4
V <sub>OD</sub>	Output differential voltage	1.8-V LVDS (7)		0.065		0.44	10 V
		USB(9)				20	00
		OSC (10)		-10.0		1	0
I <sub>IH</sub>	High-level input current	3.3-V LVTTL (1-4) without internal pulldown	V <sub>IH</sub> = VDD33	-10.0		1	0 μΑ
	ouron	3.3-V LVTTL (1-4) with internal pulldown	V <sub>IH</sub> = VDD33	10.0		200	.0
		3.3-V I <sup>2</sup> C (8)	V <sub>IH</sub> = VDD33			10	.0
		USB(9)		-10.0		10	.0
		OSC (10)		-10.0		10	.0
I <sub>IL</sub>	Low-level input current	3.3-V LVTTL (1–4) without internal pulldown	V <sub>OH</sub> = VDD33	-10.0		10	.0 <sub>µA</sub>
	Current	3.3-V LVTTL (1-4) with internal pulldown	V <sub>OH</sub> = VDD33	-10.0		-20	00
		3.3-V I <sup>2</sup> C (8)	V <sub>OH</sub> = VDD33			-10	.0
		USB(9)			_ 19.1		
	High-level output	1.8-V LVDS (7) (V <sub>OD</sub> = 300 mV)	VO = 1.4 V	6.5	·		
I <sub>OH</sub>	current	3.3-V LVTTL (1)	VO = 2.4 V	-4.0		mA	
		3.3-V LVTTL (2)	VO = 2.4 V	-8.0			
		3.3-V LVTTL (3)	VO = 2.4 V	-12.0			



### **6.5 Electrical Characteristics (continued)**

over recommended operating conditions

	PAR	RAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		USB (9)		19.1		
		1.8-V LVDS (7) (V <sub>OD</sub> = 300 mV)	VO = 1.0 V	6.5		
	Low-level output	3.3-V LVTTL (1)	VO = 0.4 V	4.0		
l <sub>OL</sub>	current	3.3-V LVTTL (2)	VO = 0.4 V	8.0		mA
		3.3-V LVTTL (3)	VO = 0.4 V	12.0		
		3.3-V I <sup>2</sup> C (8)		3.0		
		USB (9)		-10		
	High-impedance	LVDS (7)		-10		
l <sub>OZ</sub>	leakage current	3.3-V LVTTL (1,2,3)		-10		pF
		3.3-V I <sup>2</sup> C (8)		-10		]
		USB (9)		11.84	17.07	
		3.3-V LVTTL (1)		3.75	5.52	
C <sub>I</sub>	Input capacitance	3.3-V LVTTL (2)		3.75	5.52	pF
		3.3-V LVTTL (4)		3.75	5.52	
		3.3-V I <sup>2</sup> C (8)		5.26	6.54	]
I <sub>CC11</sub>	Supply voltage, 1.1	-V core power	Normal Mode		1474	mA
I <sub>CC18</sub>	Supply voltage, 1.8-DRAM)	-V power (LVDS I/O and internal	Normal Mode		1005	mA
I <sub>CC33</sub>	Supply voltage, 3.3	-V I/O power	Normal Mode		33	mA
I <sub>CC11_PLLD</sub>	Supply voltage, DM	D PLL Digital Power ( 1.1V)	Normal Mode	4.4	6.2	mA
I <sub>CC11_PLLM1</sub>	Supply voltage, Mar power ( 1.1V)	ster-LS Clock Generator PLL Digital	Normal Mode	4.4	6.2	mA
I <sub>CC11_PLLM2</sub>	Supply voltage, Mar power ( 1.1V)	ster-HS Clock Generator PLL Digital	Normal Mode	4.4	6.2	mA
I <sub>CC18 PLLD</sub>	Supply voltage, DM	D PLL Analog Power (1.8 V)	Normal Mode	8.0	10.2	mA
I <sub>CC18_PLLM1</sub>	Supply voltage, Mar power (1.8 V)	ster-LS Clock Generator PLL Analog	Normal Mode	8.0	10.2	mA
I <sub>CC18_PLLM2</sub>	Supply voltage, Mar power (1.8 V)	ster-HS Clock Generator PLL Analog	Normal Mode	8.0	10.2	mA
I <sub>CC11_PLLS</sub>	Supply voltage, Vid	eo-2X PLL Analog Power ( 1.1 V)	Normal Mode		2.9	mA
	Total Power		Normal Mode		3.73	W
I <sub>CC11</sub>	Supply voltage, 1.1	V core power	Low Power Mode		21	mA
I <sub>CC18</sub>	Supply voltage, 1.8-DRAM)	-V power (LVDS I/O and internal	Low Power Mode		0	mA
I <sub>CC33</sub>	Supply voltage, 3.3	-V I/O power	Low Power Mode		18	mA
I <sub>CC11_PLLD</sub>	Supply voltage, DM	D PLL Digital Power ( 1.1V)	Low Power Mode		2.03	mA
I <sub>CC11_PLLM1</sub>	Supply voltage, Mar power ( 1.1V)	ster-LS Clock Generator PLL Digital	Low Power Mode		2.03	mA
I <sub>CC11_PLLM2</sub>	Supply voltage, Mapower (1.1V)	ster-HS Clock Generator PLL Digital	Low Power Mode		2.03	mA
I <sub>CC18_PLLD</sub>	Supply voltage, DM	D PLL Analog Power (1.8 V)	Low Power Mode		5.42	mA
I <sub>CC18_PLLM1</sub>	Supply voltage, Mar	ster-LS Clock Generator PLL Analog	Low Power Mode		5.42	mA

### 6.5 Electrical Characteristics (continued)

over recommended operating conditions

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC18_PLLM2</sub>	Supply voltage, Master-HS Clock Generator PLL Analog power (1.8 V)	Low Power Mode			5.42	mA
I <sub>CC11_PLLS</sub>	Supply voltage, Video-2X PLL Analog Power ( 1.1V)	Low Power Mode			.03	mA
	Total Power	Low Power Mode			106	mW

### 6.6 System Oscillators Timing Requirements

over operating free-air temperature range(unless otherwise noted)

PARAM	ETER	TEST CONDITIONS	MIN	MAX	UNIT				
SYSTEM OSCILLATORS									
f <sub>clock</sub>	Clock frequency, MOSC <sup>(1)</sup>		19.998	20.002	MHz				
t <sub>c</sub>	Cycle time, MOSC <sup>(1)</sup>		49.995	50.005	MHz				
t <sub>w(H)</sub>	Pulse duration <sup>(2)</sup> , MOSC, high	50% to 50% reference points (signal)	20		ns				
t <sub>w(L)</sub>	Pulse duration <sup>(2)</sup> , MOSC, low	50% to 50% reference points (signal)	20		ns				
t <sub>t</sub>	Transition time <sup>(2)</sup> , MOSC, tt = tf /tr	20% to 80% reference points (signal)		12	ns				
t <sub>jp</sub>	Period Jitter <sup>(2)</sup> , MOSC (This is the deviation in period from the ideal period due solely to high frequency jitter).			18	ps				

<sup>(1)</sup> The frequency range for MOSC is 20 MHz with +/-100 PPM accuracy (it includes impact to accuracy due to aging, temperature and trim sensitivity). The MOSC input cannot support spread spectrum clock spreading.

### 6.7 Test and Reset Timing Requirements

			MIN	MAX	UNIT
t <sub>W1(L)</sub>	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)	4.0		μs
t <sub>W1(L)</sub>	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)		1000 <sup>(2)</sup>	ms
t <sub>t1</sub>	Transition time, PWRGOOD, $t_{t1} = t_f/t_r$	20% to 80% reference points (signal)		625	μs
t <sub>W2(L)</sub>	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)	500		μs
t <sub>W2(L)</sub>	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)		1000 <sup>(2)</sup>	ms
t <sub>t2</sub>	Transition time, POSENSE, $t_{t1} = t_f/t_r$	20% to 80% reference points (signal)		25 <sup>(1)</sup>	μs
t <sub>PH</sub>	Power Hold time, POSENSE remains active after PWRGOOD is de-asserted	20% to 80% reference points (signal)	500		μs
t <sub>EW</sub>	Early Warning time, PWRGOOD goes inactive low prior to any power supply voltage going below its specification		500		μs
t <sub>W1(L)</sub> +t <sub>W2(L)</sub>	The sum of PWRGOOD and POSENSE inactive time			1050 <sup>(2)</sup>	ms

<sup>(1)</sup> As long as noise on this signal is below the hysteresis threshold.

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<sup>(2)</sup> Applies only when driven via an external digital oscillator.

<sup>(2)</sup> With 1.8 V power applied. If the 1.8 V power is disabled by the controller command (For example – if system is placed in Low Power mode where the controller disables 1.8 V power), these signals can be placed and remain in their inactive state indefinitely.



# 6.8 JTAG Interface: I/O Boundary Scan Application Timing Requirements

			MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency, TCK			10	MHZ
t <sub>C</sub>	Cycle time, TCK		100		ns
t <sub>W(H)</sub>	Pulse duration, high	50% to 50% reference points (signal)	40		ns
t <sub>W(L)</sub>	Pulse duration, low	50% to 50% reference points (signal)	40		ns
t <sub>t</sub>	Transition time, $t_t = t_f/t_r$	20% to 80% reference points (signal)		5	ns
t <sub>SU</sub>	Setup time, TDI valid before TCK↑		8		ns
t <sub>h</sub>	Hold time, TDI valid after TCK↑		2		ns
t <sub>SU</sub>	Setup time, TMS1 valid before TCK↑		8		ns
t <sub>h</sub>	Hold time, TMS1 valid before TCK↑		2		ns

# **6.9 Port 1 Input Pixel Timing Requirements**

	and the same and t	TEST CONDITIONS	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (30-bit bus)		12	175	MHz
f <sub>clock</sub>	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (60-bit bus)		12	160	MHz
t <sub>C</sub>	Cycle Time, P_CLK1, P_CLK2, P_CLK3		5.714	83.33	ns
$t_{W(H)}$	Pulse Duration, high	50% to 50% reference points (signal)	2.3		ns
t <sub>W(L)</sub>	Pulse Duration, low	50% to 50% reference points (signal)	2.3		ns
t <sub>jp</sub>	Clock period jitter, P_CLK1, P_CLK2, P_CLK3	Max f <sub>clock</sub>		See (2)	ps
t <sub>t</sub>	Transition time, t <sub>t</sub> =t <sub>t</sub> /t <sub>r</sub> , P_CLK1, P_CLK2, P_CLK3	20% to 80% reference points (signal)	0.6	2.0	ns
t <sub>t</sub>	Transition time, $t_t=t_f/t_r$ , P1_A(9-0), P1_B(9-0), P1_C(9-0), P1_HSYNC, P1_VSYNC, P1_DATAEN	20% to 80% reference points (signal)	0.6	3.0	ns
t <sub>t</sub>	Transition time, t <sub>i</sub> =t <sub>i</sub> /t <sub>r</sub> , ALF_HSYNC, ALF_VSYNC, ALF_CSYNC <sup>(1)</sup>	20% to 80% reference points (signal)	0.6	3.0	ns
SETUP	AND HOLD TIMES			'	
t <sub>su</sub>	Setup time, P1_A(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P1_A(9-0), valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P1_B(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P1_B(9-0), valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P1_C(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P1_C(9-0), valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P1_VSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P1_VSYNC valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P1_HSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P1_HSYNC valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns

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### **6.9 Port 1 Input Pixel Timing Requirements (continued)**

		TEST CONDITIONS	MIN	MAX	UNIT
t <sub>su</sub>	Setup time, P2_A(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P2_A(9-0), valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P2_B(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P2_B(9-0), valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P2_C(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P2_C(9-0), valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P2_VSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P2_VSYNC valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P2_HSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P2_HSYNC valid before P_CLK1 $\uparrow\downarrow$ , P_CLK2 $\uparrow\downarrow$ , or P_CLK3 $\uparrow\downarrow$		0.8		ns
t <sub>su</sub>	Setup time, P_DATAEN1, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P_DATAEN1 valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>su</sub>	Setup time, P_DATAEN2, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>h</sub>	Hold time, P_DATAEN2 valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t <sub>w(A)</sub>	VSYNC Active Pulse Width		1		Video Line
t <sub>w(A)</sub>	HSYNC Active Pulse Width		16		Pixel Clocks

- (1) ALF\_CSYNC, ALF\_VSYNC and ALF\_HSYNC are Asynchronous signals.
   (2) For frequencies (fclock) less than 175 MHZ, use following formula to obtain the jitter: Max Clock Jitter = +/- [ (1/f<sub>clock</sub>) 5414 ps]

# 6.10 Port 3 Input Pixel Interface (via GPIO) Timing Requirements

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f <sub>clock</sub>	Clock Frequency, P3_CLK		27	54	MHz
t <sub>c</sub>	Cycle time, P3_CLK		18.5	37.1	ns
t <sub>W(H)</sub>	Pulse Duration, high	50% to 50% reference points (signal)	7.4		ns
t <sub>W(L)</sub>	Pulse Duration, low	50% to 50% reference points (signal)	7.4		ns
t <sub>jp</sub>	Clock period jitter, P3_CLK	$Max\ f_{clock}$	See (1)	See (1)	ps
t <sub>t</sub>	Transition time, t <sub>t</sub> = t <sub>f</sub> /t <sub>r</sub> , P3_CLK	20% to 80% reference points (signal)	1.0	5.0	ns
t <sub>t</sub>	Transition time, t <sub>t</sub> = t <sub>t</sub> /t <sub>r</sub> , P3_DATA(9-0)	20% to 80% reference points (signal)	1.0	5.0	ns
t <sub>su</sub>	Setup time, P3_DATA(9-0) valid before P3_CLK↑↓		2.0		ns
t <sub>h</sub>	Hold time, P3_DATA(9-0) valid after P3_CLK↑↓		2.0		ns

(1) For frequencies less than 54 MHZ, use following formula to obtain the jitter: Jitter = [(1/F) - 5414 ps].



### **6.11 DMD LVDS Interface Timing Requirements**

		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency, DCK_A	N/A	DCK_A	100	400	MHz
t <sub>C</sub>	Cycle time, DCK_A <sup>(1)</sup>	N/A	DCK_A	2475.3		ps
t <sub>W(H)</sub>	Pulse duration, high	N/A	DCK_A	1093		ps
t <sub>W(L)</sub>	Pulse duration, low	N/A	DCK_A	1093		ps
t <sub>t</sub>	Transition time, t <sub>t</sub> = t <sub>f</sub> /t <sub>r</sub>	N/A	DCK_A	100	400	ps
t <sub>osu</sub>	Output Setup time at max clock rate <sup>(2)</sup>	DCK_A↑↓	SCA, DDA(15:0)	438		ps
t <sub>oh</sub>	Output hold time at max clock rate <sup>(2)</sup>	DCK_A↑↓	SCA, DDA(15:0)	438		ps
f <sub>clock</sub>	Clock frequency, DCK_B	N/A	DCK_B	100	400	MHz
t <sub>C</sub>	Cycle time, DCK_B <sup>(1)</sup>	N/A	DCK_B	2475.3		ps
t <sub>W(H)</sub>	Pulse duration, high	N/A	DCK_B	1093		ps
t <sub>W(L)</sub>	Pulse duration, low	N/A	DCK_B	1093		ps
t <sub>t</sub>	Transition time, t <sub>t</sub> = t <sub>f</sub> /t <sub>r</sub>	N/A	DCK_B	100	400	ps
t <sub>osu</sub>	Output Setup time at max clock rate <sup>(2)</sup>	DCK_B↑↓	SCA, DDB(15:0)	438		ps
t <sub>oh</sub>	Output hold time at max clock rate <sup>(2)</sup>	DCK_B↑↓	SCA, DDB(15:0)	438		ps
t <sub>sk</sub>	Output Skew, Channel A to Channel B	DCK_A↑	DCK_B↑		250	ps

<sup>(1)</sup> The minimum cycle time (t<sub>c</sub>) for DCK\_A and DCL\_B includes 1.0% spread spectrum modulation. User must verify that DMD can support this rate.

## 6.12 Synchronous Serial Port (SSP) Interface Timing Requirements

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT		
SSP Primary							
t <sub>su</sub>	Setup time, SSPx_DI valid before SSPx_CLK		15		ns		
t <sub>su</sub>	Setup time, SSPx_DI valid before SSPx_CLK		15		ns		
t <sub>h</sub>	Hold time, SSPx_DI valid after SSPx_CLK		0		ns		
t <sub>h</sub>	Hold time, SSPx_DI valid after SSPx_CLK		0		ns		
t <sub>t</sub>	Transition time, SSPx_DI, $t_t$ = $t_f/t_r$	20% to 80% reference points (signal)		1.5	ns		
SSP S	econdary						
t <sub>su</sub>	Setup time, SSPx_DI valid before SSPx_CLK		12		ns		
t <sub>su</sub>	Setup time, SSPx_DI valid before SSPx_CLK		12		ns		
t <sub>h</sub>	Hold time, SSPx_DI valid after SSPx_CLK		12		ns		
t <sub>h</sub>	Hold time, SSPx_DI valid after SSPx_CLK		12		ns		
t <sub>t</sub>	Transition time, SSPx_DI, $t_t$ = $t_f/t_r$	20% to 80% reference points (signal)		1.5	ns		

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<sup>(2)</sup> Output Setup and Hold times for DMD clock frequencies below the maximum can be calculated as follows:  $t_{osu}(fclock) = t_{osu}(fmax) + 250000 \times (1/fclock - 1/400)$  and  $t_{oh}(fclock) = t_{oh}(fmax) + 250000 \times (1/fclock - 1/400)$  where fclock is in MHz.



### 6.13 Programmable Output Clocks Switching Characteristics

over operating free air temperature range, C<sub>L</sub>(min timing) = 5 pF, C<sub>L</sub>(max timing) = 50 pF (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency, OCLKA <sup>(1)</sup>		OCLKA	0.787	50	MHz
t <sub>C</sub>	Cycle Time, OCLKA		OCLKA	20	1270.6	ns
t <sub>W(H)</sub>	Pulse Duration, high <sup>(2)</sup>	50% to 50% reference points (signal)	OCLKA	(t <sub>C</sub> /22)		ns
t <sub>W(L)</sub>	Pulse Duration, low <sup>(2)</sup>	50% to 50% reference points (signal)	OCLKA	(t <sub>C</sub> /22)		ns
	Jitter		OCLKA		350	ps
f <sub>clock</sub>	Clock frequency, OCLKB <sup>(1)</sup>		OCLKB	0.787	50	MHz
t <sub>C</sub>	Cycle Time, OCLKB		OCLKB	20	1270.6	ns
t <sub>W(H)</sub>	Pulse Duration, high <sup>(2)</sup>	50% to 50% reference points (signal)	OCLKB	(t <sub>C</sub> /22)		ns
t <sub>W(L)</sub>	Pulse Duration, low <sup>(2)</sup>	50% to 50% reference points (signal)	OCLKB	(t <sub>C</sub> /22)		ns
	Jitter		OCLKB		350	ps
f <sub>clock</sub>	Clock frequency, OCLKC <sup>(1)</sup>		OCLKC	0.787	50	MHz
t <sub>C</sub>	Cycle Time, OCLKC <sup>(2)</sup>		OCLKC	20	1270.6	ns
t <sub>W(H)</sub>	Pulse Duration, high	50% to 50% reference points (signal)	OCLKC	(t <sub>C</sub> /22)		ns
$t_{W(L)}$	Pulse Duration, low <sup>(2)</sup>	50% to 50% reference points (signal)	OCLKC	(t <sub>C</sub> /22)		ns
	Jitter		OCLKC		350	ps

- (1) The frequency of OCLKA thru OCLKC is programmable.
- (2) The Duty Cycle of OCLKA thru OCLKC is within +/- 2 ns of 50%.

### 6.14 Synchronous Serial Port Interface (SSP) Switching Characteristics

over operating free-air temperature range, C<sub>L</sub>(min timing) = 5 pF, C<sub>L</sub>(max timing) = 50 pF (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>clock</sub>	Clock Frequency, SSPx_CLK		N/A	SSPx_CLK	73	25000	kHz
t <sub>c</sub>	Cycle time, SSPx_CLK		N/A	SSPx_CLK	0.040	13.6	μs
t <sub>W(H)</sub>	Pulse Duration, high	50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
t <sub>W(L)</sub>	Pulse Duration, low	50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
SSP P	rimary (1)						
t <sub>pd</sub>	Output Propagation, Clock to Q, SSPx_DO <sup>(2)</sup>		SSPx_CLK↓	SSPx_DO	-5	5	ns
t <sub>pd</sub>	Output Propagation, Clock to Q, SSPx_DO <sup>(2)</sup>		SSPx_CLK↑	SSPx_DO	-5	5	ns
SSP S	econdary <sup>(1)</sup>						
t <sub>pd</sub>	Output Propagation, Clock to Q, SSPx_DO <sup>(2)</sup>		SSPx_CLK↓	SSPx_DO	0	34	ns
t <sub>pd</sub>	Output Propagation, Clock to Q, SSPx_DO <sup>(2)</sup>		SSPx_CLK↑	SSPx_DO	0	34	ns

<sup>(1)</sup> The SSP can be used as an SSP Primary, or as an SSP Secondary. When used as a Primary, the SSP can be configured to sample DI with the same internal clock edge used to transmit the next DO, which provides a full cycle rather than a half cycle timing path, allowing operation at higher SPI clock frequencies.

<sup>(2)</sup> The SSP can be configured into four different operational modes/configurations.

SPI Clocking Mode	SPI Clock Polarity (CPOL)	SPI Clock Phase (CPHA)
0	0	0
1	0	1
2	1	0
3	1	1

### 6.15 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

over operating free-air temperature range,  $C_L$ (min timing) = 5 pF,  $C_L$ (max timing) = 85 pF (unless otherwise noted)

	PARAMETER		FROM INPUT	TO OUTPUT	MIN	MAX	UNIT
t <sub>pd</sub>	Output Propagation, Clock to Q	TCK↓		TDO1	3	12	ns

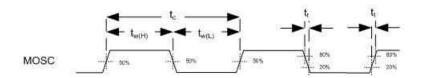


Figure 6-1. System Oscillators

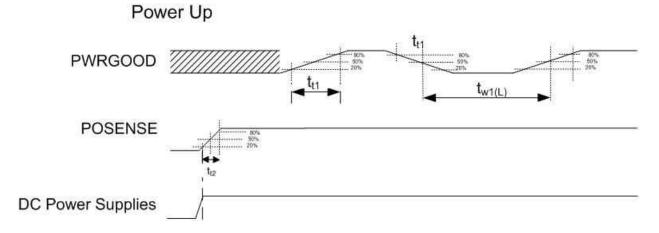


Figure 6-2. Power Up

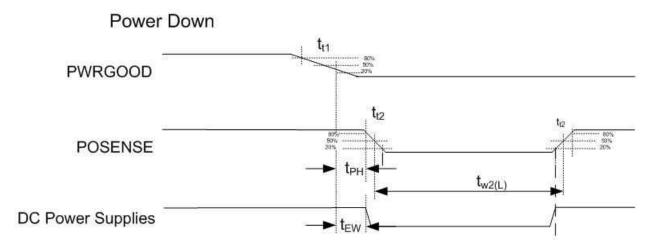


Figure 6-3. Power Down

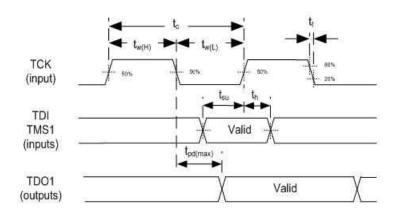


Figure 6-4. I/O Boundary Scan

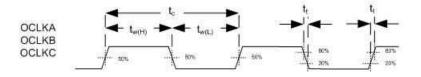


Figure 6-5. Programmable Output Clocks

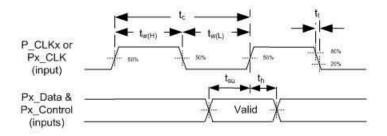


Figure 6-6. Port1, Port2, and Port3 Input Interface



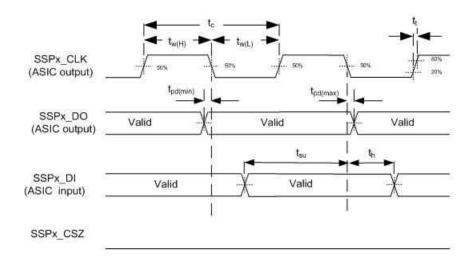


Figure 6-7. Synchronous Serial Port Interface—Primary

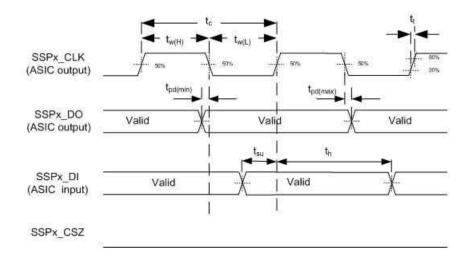


Figure 6-8. Synchronous Serial Port Interface—Secondary

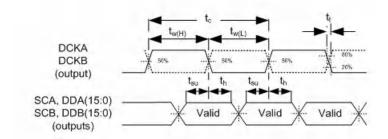


Figure 6-9. DMD LVDS Interface

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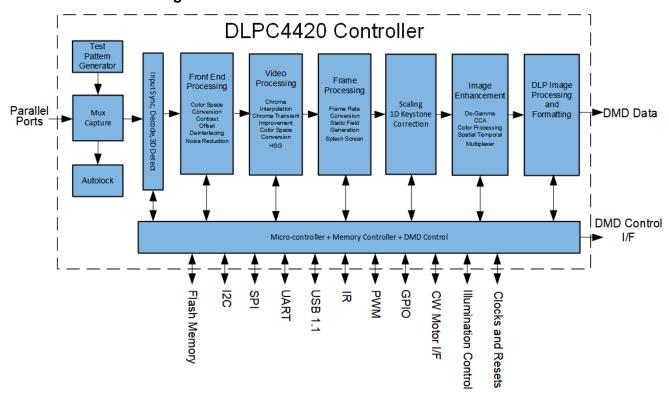


### 7 Detailed Description

#### 7.1 Overview

As with prior DLP electronics solutions, image data is 100% digital from the DLPC4420 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC4420 processes the digital input image and converts the data into bit-plane format as needed by the DMD. The DLPC4420 display controller is optimized for high-resolution and high-brightness display applications. Applications include 4K ultra high definition (UHD) display, home theatre, smart display, digital signage, and laser TV.

### 7.2 Functional Block Diagram



#### 7.3 Feature Description

#### 7.3.1 System Reset Operation

#### 7.3.1.1 Power-Up Reset Operation

Immediately following a power-up event, the DLPC4420 hardware automatically brings up the primary PLL and places the controller in normal power mode. Then, the hardware follows the standard system reset procedure (see Section 7.3.1.2).

#### 7.3.1.2 System Reset Operation

Immediately following any type of system reset (power-up reset, PWRGOOD reset, watchdog timer timeout, lamp-strike reset), the DLPC4420 device automatically returns to NORMAL power mode in the following state:

- All GPIO are tristated.
- The primary PLL remains active (it is reset only after a power-up reset sequence) and most of the derived clocks are active. However, only those resets associated with the ARM9 processor and its peripherals are released (the ARM9 is responsible for releasing all other resets).
- ARM9 associated clocks default to their full clock rates. (Boot-up is a full speed.)
- All front-end clocks derived are disabled.



- The PLL feeding the LVDS DMD I/F (PLLD) defaults to its power-down mode and all derived clocks are inactive with corresponding resets asserted. (The ARM9 is responsible for enabling these clocks and releasing associated resets.)
- LVDS I/O defaults to its power-down mode with outputs tristated.
- All resets output by the DLPC4420 device remain asserted until released by the ARM9 (after boot-up).
- The ARM9 processor boots-up from external flash.

When the ARM9 boots-up, the ARM9 API:

- Configures the programmable DDR Clock Generator (DCG) clock rates (that is, the DMD LVDS I/F rate)
- Enables the DCG PLL (PLLD) while holding divider logic in reset
- When the DCG PLL locks, ARM9 software sets DMD clock rates
- API software then releases DCG divider logic resets, which in turn, enable all derived DCG clocks
- Release external resets

Application software then typically waits for a wake-up command (through the soft power switch on the projector) from the end user. When the projector is requested to wake-up, the software places the ASIC back in normal mode, re-initialize clocks, and resets as required.

#### 7.3.2 Spread Spectrum Clock Generator Support

The DLPC4420 controller supports limited, internally-controlled, spread spectrum clock spreading on the DMD interface. The purpose of this is to frequency spread all signals on this high-speed, external interface to reduce EMI emissions. Clock spreading is limited to triangular waveforms. The DLPC4420 controller provides modulation options of 0%, +/-0.5% and +/-1.0% (center-spread modulation).

#### 7.3.3 GPIO Interface

The DLPC4420 controller provides 83 software-programmable, general-purpose I/O pins. Each GPIO pin is individually configurable as either input or output. In addition, each GPIO output can be either configured as push-pull or open-drain. Some GPIO have one or more alternate-use modes, which are also software configurable. The reset default for all GPIO is as an input signal. However, any alternate function connected to these GPIO pins, with the exception of general purpose clocks and PWM generation, stay in reset. When configured as open-drain, the outputs must be externally pulled-up (to the 3.3-V supply). External pull-up or pulldown resistors may be required to ensure stable operation before software is able to configure these ports.

#### 7.3.4 Source Input Blanking

Vertical and horizontal blanking requirements for both input ports are defined as follows (See *Video Timing Parameter Definitions*).

- Minimum port 1 and port 2 vertical blanking
  - Vertical back porch (VBP): 370 us
  - Vertical front porch (VFP): 1 line
  - Total vertical blanking (TVB): 370 µs + 2 lines
- Minimum port1 and port 2 horizontal blanking
  - Horizontal back porch (HBP): 10 pixels
  - Horizontal front porch (HFP): 0 pixels
  - Total horizontal blanking (THB): 80 pixels

#### 7.3.5 Video Graphics Processing Delay

The DLPC4420 controller introduces a variable number of field/ frame delays dependent on the source type and selected processing steps performed on the source. For optimum audio/ video synchronization this delay must be matched in the audio path. The following tables define various video delay scenarios to aid in audio matching.

Frame and Fields in table refer to source frames and fields.

- For 2-D sources, "N" is defined to be the ratio of the primary channel source frame rate (or field rate for interlaced video) to the display frame/ field rate.
- For 3-D sources, "M" is defined to be the ratio of the primary channel source frame rate (or field rate for interlaced video) required to obtain both the left and right image, to the display frame/field rate (The rate at which each eye is displayed).

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Instruments

<b>Table 7-1.</b>	Primar	/ Channel/\	Video-Gra	phics Pr	ocessina [	Delav

Source	Frame Rate Conversion	FRC Type	Formatter Buffer	Total Delay
48 Hz Graphics	1 Frame	Sync (1:1)	N Frames	1 + N Frames
50 Hz Graphics	1 Frame	Sync (1:1)	N Frames	1 + N Frames
60 Hz Graphics	1 Frame	Sync (1:1)	N Frames	1 + N Frames
100 and 120 Hz Graphics	1 Frame	Sync (1:1)	N Frames	1 + N Frames
100 and 120 Hz Graphics (3D)	1 Frame	Sync (1:2)	M Frames	1 + M Frames
240 Hz Graphics (2xDLPC4420)	1 Frame	Sync (1:1)	N Frames	1 + N Frames

### 7.3.6 Program Memory Flash/SRAM Interface

The DLPC4420 controller provides three external program memory chip selects:

- PM CSZ 0 available for optional SRAM or flash device (≤ 128 Mb)
- PM CSZ 1 dedicated CS for boot flash device (ie. Standard NOR-type flash, ≤ 128 Mb)
- PM CSZ 2 available for optional SRAM or flash device (≤ 128 Mb)

Flash and SRAM access timing is software programmable up to 31 wait states. Wait state resolution is 6.7 ns in normal mode and 53.33 ns in low power modes. Wait state program values for typical flash access times are shown in the Table 7-2.

Table 7-2. Wait State Program Values for Typical Flash Access Times

	Normal Mode <sup>(1)</sup>	Low Power Mode <sup>(1)</sup>		
Formula to Calculate the Required Wait State Value	= Roundup (Device_Access_Time / 6.7 ns)	= Roundup (Device_Access_Time / 53.33 ns)		
Max Supported Device Access Time	207 ns	1660 ns		

<sup>(1)</sup> Assumes a maximum single direction trace length of 75 mm.

Note that when another device such as an SRAM or additional flash is used in conjunction with the boot flash, care must be taken to keep stub length short and located as close as possible to the flash end of the route.

The DLPC4420 controller provides enough Program Memory Address pins to support a flash or SRAM device up to 128 Mb. For systems not requiring this capacity, up to two address pins can be used as GPIO instead. Specifically, the two most significant address bits (i.e. PM ADDR 22 and PM ADDR 21) are shared on pins GPIO 36 and GPIO 35 respectively. Like other GPIO pins, these pins float in a high-impedance input state following reset; therefore, if these GPIO pins are to be reconfigured as Program Memory Address pins, they require board-level pull-down resistors to prevent any flash address bits from floating until software is able to reconfigure the pins from GPIO to Program Memory Address. Also note that until software reconfigures the pins from GPIO to Program Memory Address, upper portions of flash memory are not accessible.

Table 7-3 shows typical GPIO 35 and GPIO36 pin configuration for various flash sizes.

Table 7-3. Typical GPIO\_35 and GPIO\_36 Pin Configurations for Various Flash Sizes

FLASH SIZE	GPIO_36 Pin Configuration	GPIO_35 Pin Configuration
32 Mb or less	GPIO_36	GPIO_35
64 Mb	GPIO_36	PM_ADDR_21 <sup>(1)</sup>
128 Mb	PM_ADDR_22 <sup>(1)</sup>	PM_ADDR_21 <sup>(1)</sup>

<sup>(1)</sup> Board-level pulldown resistor required.

#### 7.3.7 Calibration and Debug Support

The DLPC4420 controller contains a test point output port, TSTPT\_(7:0), which provides selected system calibration support as well as ASIC debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes

an internal pull-down resistor and thus external pull-ups are used to modify the default test configuration. The default configuration (x00) corresponds to the TSTPT\_(7:0) outputs being driven low for reduce switching activity during normal operation. For maximum flexibility, an option to jumper to an external pull-up is recommended for TSTPT\_(3:0). Note that adding pull-up to TSTPT\_(7:4) may have adverse affects for normal operation and are not recommended. Note that these external pull-ups are only sampled upon a zero to one transition on POSENSE and thus changing their configuration after reset has been released does not have any effect until the next time reset is asserted and released. Table 7-4 defines the test mode selection for 3 of the 16 programmable scenarios defined by TSTPT\_(3:0):

Table 7-4. Test Mode Selection

	No Switching Activity	System Calibration	ARM Debug Signal Set
TSTPT(3:0) Capture Value	х0	х8	x1
TSTPT(0)	0	Vertical Sync	ARM9_Debug (0)
TSTPT(1)	0	Delayed CW Index	ARM9_Debug (1)
TSTPT(2)	0	Sequence Index	ARM9_Debug (2)
TSTPT(3)	0	CW Spoke Test Pt	ARM9_Debug (3)
TSTPT(4)	0	CW Revolution Test Pt	ARM9_Debug (4)
TSTPT(5)	0	Reset Seq. Aux Bit 0	ARM9_Debug (5)
TSTPT(6)	0	Reset Seq. Aux Bit 1	ARM9_Debug (6)
TSTPT(7)	0	Reset Seq. Aux Bit 2	ARM9_Debug (7)

#### 7.3.8 Board Level Test Support

The in-circuit tristate enable signal (ICTSEN) is a board level test control signal. By driving ICTSEN to a logic high state, all controller outputs (except TDO1 and TDO2) are tristated.

The DLPC4420 controller also provides JTAG boundary scan support on all I/O except non-digital I/O and a few special signals. Table 7-5 defines these exceptions.

**SIGNAL NAME PKG BALL** HW TEST EN M25 MOSC M26 MOSCN N26 USB\_DAT\_N C5 USB DAT P D6 TCK N24 TDI N25 **TRSTZ** M23 TDO1 N23 TDO2 N22 TMS1 P25 TMS2 P26

Table 7-5. DLPC4420 —Signals Not Covered by JTAG

#### 7.4 Device Functional Modes

The DLPC4420 has two functional modes which are enabled via software command via the Host control interface. These modes are Standby and Active.

#### 7.4.1 Standby Mode

The system is powered up and active, however, some blocks within the controller have been shut down to conserve power. Only the  $\mu$ Processor and its peripherals are active (supporting a dormant projector waiting to be woken up). In this mode the DMD is parked and no image can be displayed.

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### 7.4.2 Active Mode

The system is powered up and fully operational, capable of projecting internal or external video sources.

### 7.4.2.1 Normal Configuration

This configuration enables the full functionality of the DLPC4420.



### 8 Application and Implementation

#### **Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The DLPC4420 display controller coupled with supported DMDs comprise the chipset. The controller integrates all system image processing, DMD control and data formatting onto a single integrated circuit (IC), as well as LED or LPCW illumination systems and multiple image processing algorithms. Applications include 4K Ultra High Definition (UHD) Display, Home Theatre, Smart Display, Digital Signage, and Laser TV.

#### 8.2 Typical Application

The DLPC4420 controller is ideal for applications requiring high brightness and high resolution displays. When two DLPC4420 display controllers are combined with the DLP 4K DMD, an FPGA, a power management and motor driver device (DLPA100), and other electrical, optical and mechanical components the chipset enables bright, affordable, 4K UHD display solutions. A typical DLP system application using the DLPC4420 controller and supported DLP DMD is shown below.

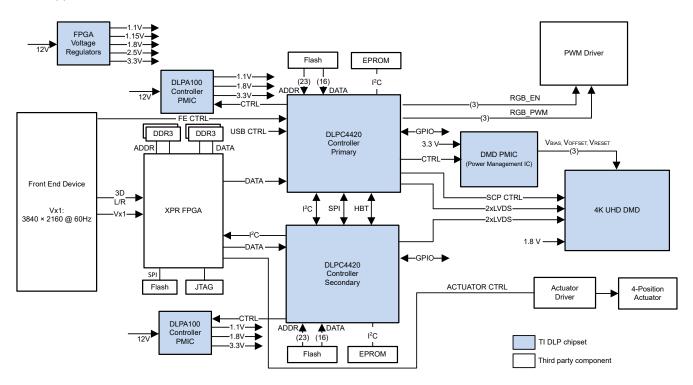


Figure 8-1. Typical 4K UHD LED Display Application

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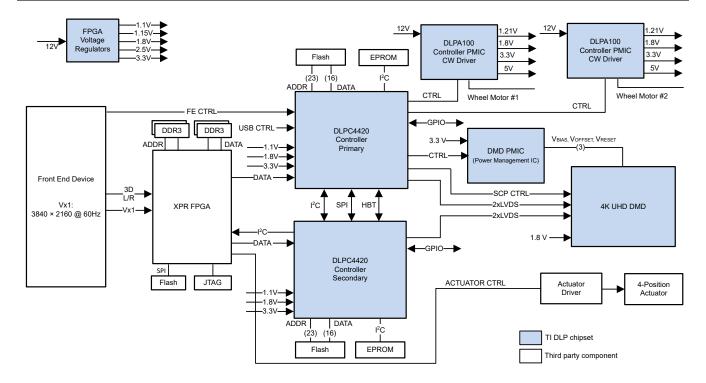


Figure 8-2. Typical 4K UHD LPCW Display Application

### 8.2.1 Design Requirements

The display controller is the digital interface between the DMD and the rest of the system. The display controller takes digital input from front end digital receivers and drives the DMD over a high speed interface. The display controller also generates the necessary signals (data, protocols, timings) required to display images on the DMD. Some systems require a dual controller to format the incoming data before sending it to the DMD. Reliable operation of the DMD is only insured when the DMD and the controller are used together in a system. In addition to the DLP devices included in the chipset, other devices may be needed such as a flash part to store the software and firmware.

#### 8.2.1.1 Recommended MOSC Crystal Oscillator Configuration

**Table 8-1. Crystal Port Characteristics** 

Table of the Crystal Fort of the Color of th				
PARAMETER	NOMINAL	UNIT		
MOSC TO GROUND Capacitance	1.5	pF		
MOSCZ TO GROUND Capacitance	1.5	pF		

**Table 8-2. Recommended Crystal Configuration** 

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (1st harmonic)	
Crystal nominal frequency	20	MHz
Crystal frequency temperature stability	+/- 30	PPM
Overall crystal frequency tolerance (including accuracy, stability, aging, and trim sensitivity)	+/- 100	PPM
Crystal Equivalent Series Resistor (ESR)	50 max	Ω
Crystal load	20	pF
Crystal shunt load	7 max	pF
RS drive resistor (nominal)	100	Ω
RFB feedback resistor (nominal)	1	ΜΩ

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<b>Table 8-2.</b>	Recommended	Crystal	Configuration	(continued)	)

PARAMETER	RECOMMENDED	UNIT
CL1 external crystal load capacitor (MOSC)	See <sup>(1)</sup> .	pF
CL2 external crystal load capacitor (MOSCN)	See <sup>(1)</sup> .	pF
PCB layout	A ground isolation ring around the crystal is recommended.	

(1) Typical drive level with the XSA020000FK1H-OCX Crystal (ESRmax =  $40 \Omega$ ) =  $50 \mu W$ .

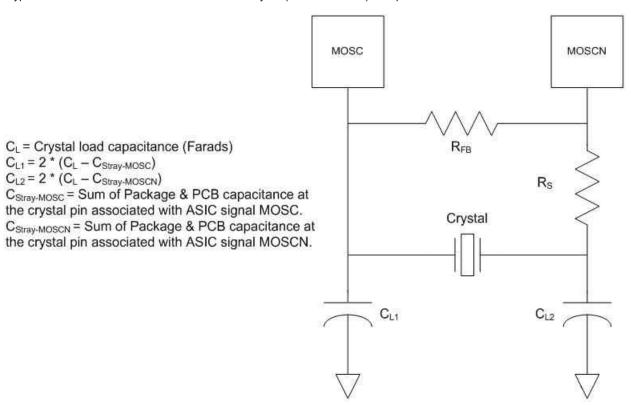


Figure 8-3. Recommended Crystal Oscillator Configuration

Typically, the external crystal oscillator stabilizes within 50 ms after stable power is applied.

#### 8.2.2 Detailed Design Procedure

For connecting the DLPC4420 controller and the DLP DMD together, see the reference design schematic. The layout guidelines must be followed to achieve a reliable system. To complete the DLP system, an optical module or light engine is required that contains the DLP DMD, associated illumination sources, optical elements, and necessary mechanical components.

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# 9 Power Supply Recommendations

### 9.1 System Power Regulations

It is strongly recommended that the VDD18\_PLLD, VDD18\_PLLM1, and VDD18\_PLLM2 power feeding internal PLLs be derived from an isolated linear regulator in order to minimize the AC Noise component. The VDD11\_PLLD, VDD11\_PLLM1, VDD11\_PLLM2, and VDD11\_PLLS can be derived from the same regulator as the core VDD11, but they have to be filtered.

### 9.2 System Power-Up Sequence

Although the DLPC4420 controller requires an array of power supply voltages (1.1V, 1.8V, 3.3V), there are no restrictions regarding the relative order of power supply sequencing for both power-up and power-down scenarios. Similarly, there is no minimum time between powering-up or powering-down the different supplies feeding the DLP controller. However, note that it is not uncommon for there to be power sequencing requirements for the devices that share the supplies with the DLP controller.

- 1.1V core power is applied whenever any I/O power is applied to ensures the state of the associated I/O
  that are powered are controlled to a known state. Thus, it is recommended to apply core power first. Other
  supplies are applied only after the 1.1V core has ramped up.
- All DLPC4420 device power must be applied before POSENSE is asserted to ensure proper power-up initialization.

Typically the DLPC4420 controller power-up sequencing is handled by external hardware. An external power monitor will hold the controller in system reset during power-up (i.e. POSENSE = 0). During this time all DLP controller I/Os are tri-stated. The primary PLL (PLLM1) is released from reset upon the low to high transition of POSENSE but the controller keeps the rest of the device in reset for an additional 60 ms to allow the PLL to lock and stabilize its outputs. After this 60 ms delay the ARM-9 related internal resets are de-asserted causing the microprocessor to begin its boot-up routine.

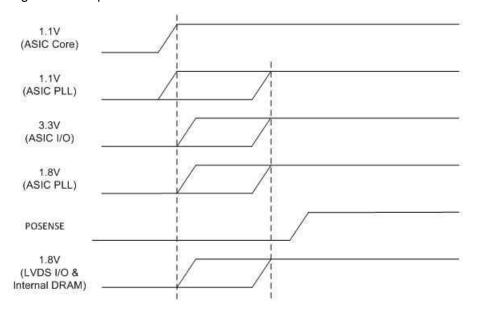


Figure 9-1. System Power-Up Sequence

#### 9.3 Power-On Sense (POSENSE) Support

In order to set up the power monitor to trip within the DLPC4420 controller minimum supply voltage specifications, it is recommended that the external power monitor generating POSENSE targets its threshold to 90% of the minimum supply voltage specifications and ensures that POSENSE remains low a sufficient amount of time for all supply voltages to reach minimum device requirements and stabilize. Note that the trip

voltage for detecting the loss of power, as well as the reaction time to respond to a low voltage condition is not critical for POSENSE as PWRGOOD is used for this purpose. As such, PWRGOOD has critical requirements in these areas.

#### 9.4 System Environment and Defaults

#### 9.4.1 DLPC4420 System Power-Up and Reset Default Conditions

Following system power-up, the DLPC4420 controller performs a power-up initialization routine that defaults the device to a normal power mode, in which ARM9-related clocks are enabled at their full rate and associated resets are released. Most other clocks default to disabled state with associated resets asserted until released by the processor. In addition, the default for system power gating enables all power. These same defaults are also applied as part of all system reset events (Watch Dog timer timeout etc.) that occur without removing or cycling power, with the possible exception of power for the LVDS I/O and internal DRAM. For an extended reset condition, the OEM is expected to place the controller in Low Power mode prior to reset, in which case the 1.8V power for the LVDS I/O and internal DRAM are disabled. When this reset is released, the 1.8V power does not get enabled until the ARM9 has been initialized and is executing the system initialization routines.

Following power-up or system reset initialization, the ARM9 boots from an external flash memory after which it enables the 1.8V power (from the DLPA100), enables the rest of the controller clocks, and initializes the internal DRAM. Once system initialization is complete the Application software determines if and when to enter low power mode.

#### 9.4.2 1.1V System Power

The DLPC4420 controller can support a low cost power delivery system with a single 1.1V power source derived from a switching regulator. To enable this approach, appropriate filtering must be provided for the 1.1V power pins of the PLLs.

#### 9.4.3 1.8V System Power

It is recommended that the DLPC4420 controller power delivery system provides two independent 1.8V power sources. One of the 1.8V power sources is used to supply 1.8V power to the controller LVDS I/O and internal DRAM. Power for these functions is fed from a common source which is recommended to be a linear regulator. The second 1.8V power source is used (along with appropriate filtering as discussed in the PCB layout guidelines for internal ASIC PLL power section of this document) to supply all of the DLPC4420 controller internal PLLs. In order to keep this power as clean as possible, a dedicated linear regulator for the 1.8V power to the PLLs is recommended.

#### 9.4.4 3.3V System Power

The DLPC4420 controller can support a low cost power delivery system with a single 3.3V power source derived from a switching regulator. This 3.3V source supplies power to all LVTTL I/O and the Crystal Oscillator cell. The 3.3V power must remain active in all power modes for which 1.1V core power is applied.

### 9.4.5 Power Good (PWRGOOD) Support

The PWRGOOD signal is defined as an early warning signal that alerts the DLPC4420 controller a specified amount of time before the DC supply voltages drop below specifications, which allows the controller to park the DMD and to place the system into reset, ensuring the integrity of future operation. For practical reasons, it is recommended that the monitor sensing PWRGOOD be on the input side of supply regulators.

#### 9.4.6 5V Tolerant Support

With the exception of USB\_DAT, the DLPC4420 controller does not support any other 5V tolerant I/Os. However, note that source signals ALF\_HSYNC, ALF\_VSYNC and I2C typically have 5V requirements and special measures must be taken to support them. Also, 5V to 3.3V level shifter is recommended.

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### 10 Layout

### 10.1 Layout Guidelines

To achieve the needed thermal connectivity, 2-ounce copper planes in the PCB design are recommended.

#### 10.1.1 PCB Layout Guidelines for Internal DLPC4420 Power

The following guidelines to achieve desired controller performance relative to internal PLLs are recommended:

- The DLPC4420 controller contains four PLLs (PLLM1, PLLM2, PLLD and PLLS), each of which have a dedicated 1.1V digital supply, and three (PLLM1, PLLM2 and PLLD) which have a dedicated 1.8-V analog supply. It is important to have filtering on the supply pins that covers a broad frequency range. Each 1.1V PLL supply pin must have individual high frequency filtering in the form of a ferrite bead and a 0.1µF ceramic capacitor. These components must be located very close to the individual PLL supply balls. The impedance of the ferrite bead must be greater than that of the capacitor at frequencies above 10MHz. The 1.1V to the PLL supply pins must also have low frequency filtering in the form of an RC filter. This filter can be common to all the PLLs. The voltage drop across the resistor is limited by the 1.1V regulator tolerance and the DLPC4420 device voltage tolerance. A resistance of 0.36 Ω and a 100 µF ceramic are recommended.
- The analog 1.8V PLL power pins must have a similar filter topology as the 1.1V. In addition, it is recommended that the 1.8V be generated with a dedicated linear regulator.
- When designing the overall supply filter network, care must be taken to ensure no resonance occurs.
   Particular care must be taken around the 1 to 2MHz band, as this coincides with the PLL natural loop frequency.



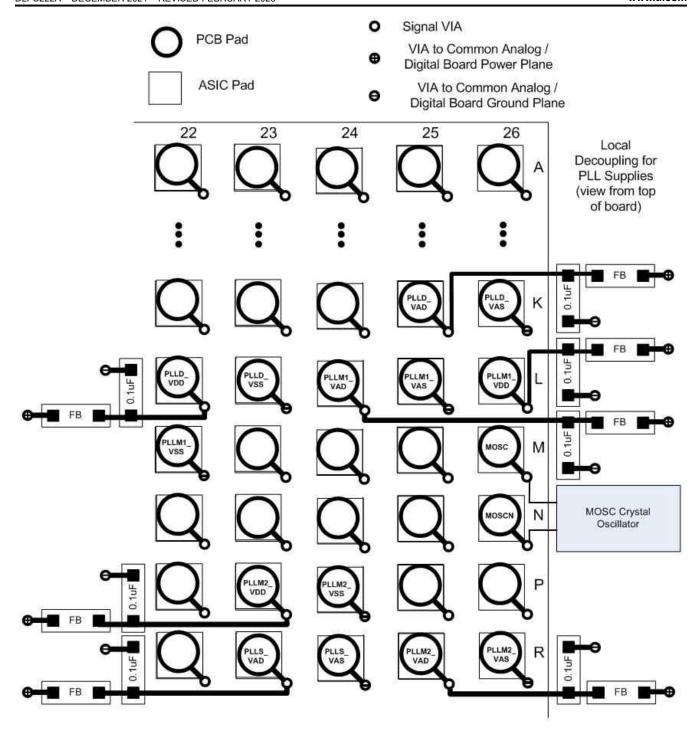


Figure 10-1. PLL Filter Layout

High frequency decoupling is required for both 1.1V and 1.8V PLL supplies and must be provided as close as possible to each of the PLL supply package pins. It is recommended to place decoupling capacitors under the package on the opposite side of the board. Use high quality, low-ESR, monolithic, surface mount capacitors. Typically 0.1µF for each PLL supply is sufficient. The length of a connecting trace increases the parasitic inductance of the mounting and thus, tracing should be avoided, allowing the via to butt up against the land itself. Additionally, the connecting trace has to be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design.

## 10.1.2 PCB Layout Guidelines for Auto-Lock Performance

One of the most important factors in getting good performance from Auto-Lock is to design the PCB with the highest signal integrity possible by following the recommendations below:

- Place the ADC chip as close to the VESA/Video connectors as possible.
- Avoid crosstalk to the analog signals by keeping them away from digital signals
- Do not place the digital ground or power planes under the analog area between the VESA connector to the ADC chip.
- Avoid crosstalk onto the RGB analog signals, by separating them from the VESA Hsync and Vsync signals.
- · Analog power must not be shared with the digital power directly.
- Try to keep the trace lengths of the RGB as equal as possible.
- Use good quality (1%) termination resistors for the RGB inputs to the ADC
- If the green channel must be connected to more than the ADC green input and ADC sync-on-green input, provide a good quality high impendence buffer to avoid adding noise to the green channel.

#### 10.1.3 DMD Interface Considerations

High speed interface waveform quality and timing on the DLPC4420 controller (that is, the LVDS DMD Interface) is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus ensuring positive timing margin requires attention to many factors.

As an example, DMD Interface system timing margin can be calculated as follows:

- Setup Margin = (DLPC4420 output setup) (DMD input setup) (PCB routing mismatch) (PCB SI degradation)
- Hold-time Margin = (DLPC4420 output hold) (DMD input hold) (PCB routing mismatch) (PCB SI degradation)

Where *PCB SI degradation* is signal integrity degradation due to PCB effects, which include simultaneously switching output (SSO) noise, cross-talk and inter-symbol interference (ISI) noise. The controller I/O timing parameters as well as DMD I/O timing parameters can be easily found in their corresponding data sheets. Similarly, *PCB routing mismatch* can be budgeted and met through controlled PCB routing. However, PCB SI degradation is not so straight forward.

In an attempt to minimize the signal integrity analysis, the following PCB design guidelines are provided as a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but have to be confirmed with PCB signal integrity analysis or lab measurements

#### PDB Design:

Configuration
 Etch Thickness
 Flex Etch Thickness
 Single Ended Signal Impedance
 Differential Signal Impedance
 Differential Signal Impedance
 Differential Signal Impedance
 Differential Signal Impedance

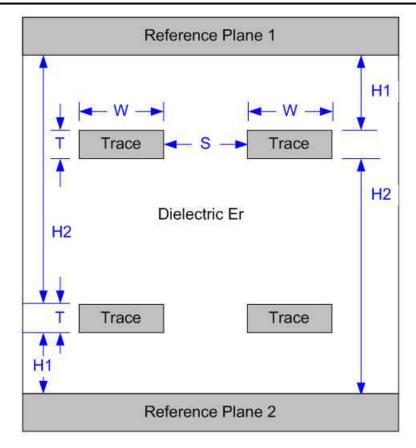
• Differential Signal Impedance 100 ohms differential (+/– 10%)

#### PCB Stackup:

- Reference plane 1 is assumed to be a ground plane for proper return path
- Reference plane 2 is assumed to be the I/O power plane or ground

Dielectric FR4, (Er):
Signal trace distance to reference plane 1 (H1)
Signal trace distance to reference plane 2 (H2)
34.2 mil (nominal)





**PCB Stackup Geometries** 

Figure 10-2. PCB Stackup Geometries

Table 10-1. General PCB Routing (Applies to All Corresponding PCB Signals)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNAL	DIFFERENTIAL PAIRS	UNIT	
Line width (W) <sup>(1)</sup>	Escape Routing in Ball Field	4 (0.1)	4 (0.1)	mil (mm)	
	PCB Etch Data or Control	7 (0.18)	4.25 (0.11)	mil (mm)	
	PCB Etch Clocks	7 (0.18)	4.25 (0.11)	mil (mm)	
Minimum Line spacing to other signals (S)	Escape Routing in Ball Field	4 (0.1)	4 (0.1)	mil (mm)	
	PCB Etch Data or Control	10 (0.25)	20 (0.51)	mil (mm)	
	PCB Etch Clocks	20 (0.51)	20 (0.51)	mil (mm)	

(1) Line width is expected to be adjusted to achieve impedance requirements.

Table 10-2. DMD I/F, PCB Interconnect Length Matching Requirements

SIGNAL GROUP LENGTH MATCHING							
I/F	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT			
DMD (LVDS)	SCA_P,SCA_N, DDA_P(15:0), DDA_N(15:0)	DCKA_P, DCKA_N	+/-150 (+/-3.81)	mil (mm)			
DMD (LVDS)	SCB_P,SCB_N, DDB_P(15:0), DDB_N(15:0)	DCKB_P, DCKB_N	+/-150 (+/-3.81)	mil (mm)			

Number of layer changes:

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- · Single ended signals: Minimize
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair typically does not change layers.

#### Termination requirements:

- DMD Interface—None, the DMD receiver is differentially terminated to 100 ohms internally
   Connector (DMD-LVDS I/F bus only)—High Speed Connectors that meet the following requirements must be used:
  - Differential Crosstalk

<5 %

• Differential Impedance

75 ohms-125 ohms

Routing requirements for right angle connectors:

When using right angle connectors, P-N pairs have to be routed in same row to minimize delay mismatch and propagation delay difference for each row has to be accounted for on associated PCB etch lengths.

#### 10.1.4 Layout Example

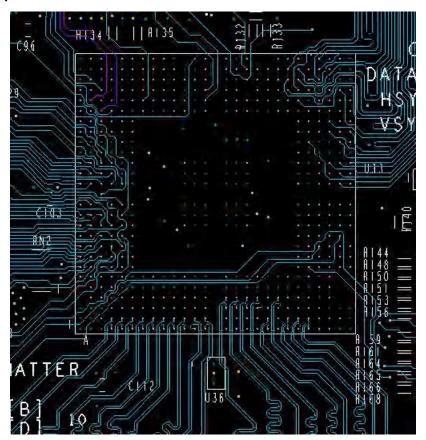


Figure 10-3. Layer 3



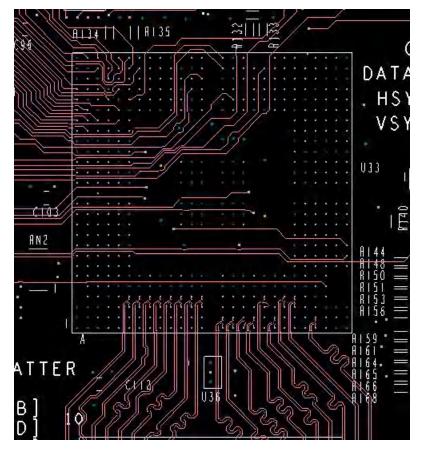


Figure 10-4. Layer 4

#### 10.1.5 Thermal Considerations

The underlying thermal limitation for the DLPC4420 controller is that the maximum operating junction temperature (T<sub>J</sub>) not be exceeded (this is defined in the Section 6.3). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC6421 device and power dissipation of surrounding components. The DLPC4420 package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature  $(T_A)$  is provided primarily as a design target and is based on maximum DLPC4420 power dissipation and  $R_{\theta JA}$  at 1 m/s of forced airflow, where  $R_{\theta JA}$  is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC4420 PCB, and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, it is highly recommended that thermal performance be measured and validated.

To do this, the top center case temperature has to be measured under the worst case product scenario (max power dissipation, max voltage, max ambient temp) and validated not to exceed the maximum recommended case temperature ( $T_C$ ). This specification is based on the measured  $\phi_{JT}$  for the DLPC4420 package and provides a relatively accurate correlation to junction temperature. Note that care must be taken when measuring this case temperature to prevent accidental cooling of the package surface. A small (approximately 40 gauge) thermocouple is recommended. The bead and the thermocouple wire must contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires must be routed closely along the package and the board surface to avoid cooling the bead through the wires.

# 11 Device and Documentation Support

## 11.1 Third-Party Products Disclaimer

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### 11.2 Device Support

#### 11.2.1 Video Timing Parameter Definitions

- Active Lines Per Frame (ALPF)—Defines the number of lines in a Frame containing displayable data: ALPF
  is a subset of the TLPF.
- Active Pixels Per Line (APPL)—Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL
- **Horizontal Back Porch Blanking (HBP)**—Number of blank pixel clocks after Horizontal Sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal
- Horizontal Front Porch Blanking (HFP)—Number of blank pixel clocks after the last active pixel but before Horizontal Sync.
- Horizontal Sync (HS)—Timing reference point that defines the start of each horizontal interval (line). The
  absolute reference point is defined by the "active" edge of the HS signal. The "active" edge (either rising or
  falling edge as defined by the source) is the reference from which all Horizontal Blanking parameters are
  measured.
- **Total Lines Per Frame (TLPF)**—Defines the Vertical Period (or Frame Time) in lines: TLPF = Total number of lines per frame (active and inactive).
- **Total Pixel Per Line (TPPL)**—Defines the Horizontal Line Period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).
- Vertical Back Porch Blanking (VBP)—Number of blank lines after Vertical Sync but before the first active line
- Vertical Front Porch Blanking (VFP)—Number of blank lines after the last active line but before Vertical Sync.
- **Vertical Sync (VS)**—Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the "active" edge of the VS signal. The "active" edge (either rising or falling edge as defined by the source) is the reference from which all Vertical Blanking parameters are measured.

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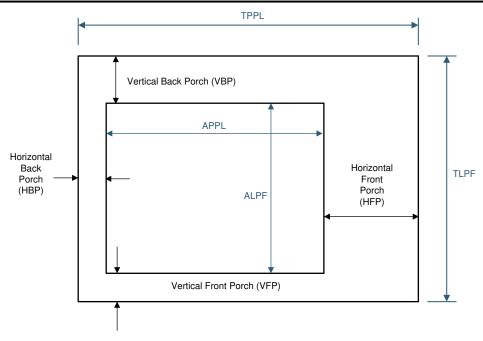


Figure 11-1. Timing Parameter Diagram

#### 11.2.2 Device Nomenclature

## Table 11-1. Part Number Description

TI PART NUMBER	DESCRIPTION		
DLPC4420	DLPC4420 Digital Controller		

# 11.2.3 Device Markings 11.2.3.1 Device Marking

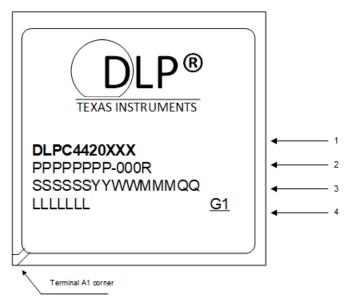


Figure 11-2. DLPC4420 Device Markings

#### Marking Definitions:

Line 1: DLP Device Name followed by TI Part Number

XXX: ZPC Package designator

Line 2: Vendor Information

Line 3: SSSSSYYWWMMM-QQ Package Assembly information

- SSSSS: Vendor Country
- YYWW: Vendor Year and Week Code (YY = Year :: WW = Week)
- MMM: Vendor Manufacturing code (ex. HAL, HBL, HAF)
- QQ: Qualification level (optional)

Line 4: LLLLLLe1 Manufacturing Information

- · LLLLLL: Manufacturing Lot code
- · G1: Green package designator

#### 11.3 Documentation Support

#### 11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLPC4420:

- DLPA100 Controller Power Management and Motor Driver Data Sheet
- DLPA300 DMD Power Management and Motor Driver Data Sheet



#### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 11.6 Trademarks

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TI E2E<sup>™</sup> is a trademark of Texas Instruments.

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#### 11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.8 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.



# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
DLPC4420ZPC	Active	Production	BGA (ZPC)   516	40   JEDEC TRAY (5+1)	Yes	Call TI	Call TI	0 to 55	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

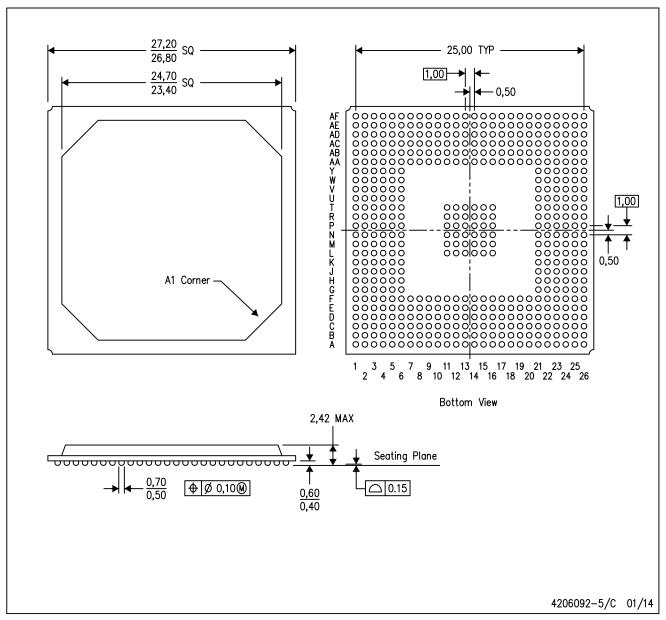
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# ZPC (S-PBGA-N516)

## PLASTIC BALL GRID ARRAY



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is Pb-free.



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