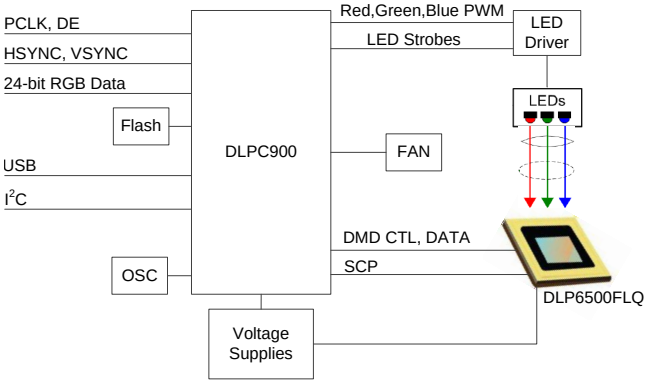
DLP6500 0.65 1080p MVSP Type A DMD

1 Features

- High Resolution 1080p (1920×1080) Array With >2 Million Micromirrors
  - 0.65-Inch Micromirror Array Diagonal
  - 7.56 µm Micromirror Pitch
  - ±12° Micromirror Tilt Angle (Relative to Flat State)
  - Designed for Corner Illumination
- Designed for Use With Broadband Visible Light (400 nm – 700 nm)
  - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
  - Micromirror Reflectivity 88%
  - Array Diffraction Efficiency 86%
  - Array Fill Factor 92%
- Two 16-Bit, Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR) Buses
- Two Dedicated Controller Options at 400 MHz Input Data Clock Rate
- DLPC900 Digital Controller
  - Up to 9523 Hz (1-Bit Binary Patterns)
  - Up to 19.7 Giga-bits Per Second (1-Bit Binary Patterns)
  - Up to 1031 Hz (8-Bit Gray Patterns Pre-Loaded With Illumination Modulation), External Input Up to 360 Hz
- DLPC910 Digital Controller
  - Up to 11574 Hz (1-Bit Binary Patterns)
  - Up to 24 Giga-bits Per Second (1-Bit Binary Patterns)
  - Up to 1446 Hz (8-Bit Gray Patterns With Illumination Modulation)
- Integrated Micromirror Driver Circuitry
- Hermetic Package

DLPC900 Simplified Diagram



2 Applications

- Industrial
  - 3D Scanners for Machine Vision and Quality Control
  - 3D Printing
  - Direct Imaging Lithography
  - Laser Marking and Repair
- Medical
  - Ophthalmology
  - 3D Scanners for Limb and Skin Measurement
  - Hyper-spectral Imaging
- Displays
  - 3D Imaging Microscopes
  - Intelligent and Adaptive Lighting

3 Description

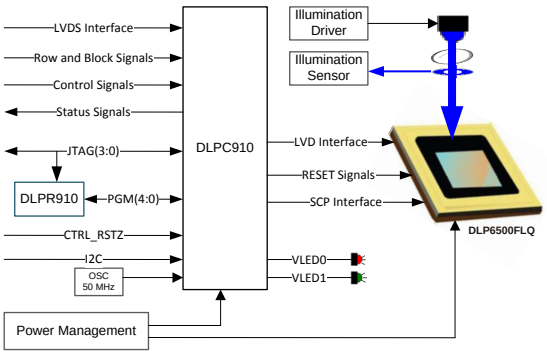
Featuring over 2 million micromirrors in a hermetic package, the high resolution 0.65 1080p digital micromirror device (DMD) is a spatial light modulator (SLM) that modulates the amplitude, direction, and/or phase of incoming light. The unique capability and value offered by the DLP6500, including operation at 405nm, makes it well suited to support a wide variety of industrial, medical, and advanced imaging applications. Reliable function and operation of the DLP6500 requires that it be used in conjunction with the DLPC900 or the DLPC910 digital controllers. This dedicated chipset provides full HD resolution at high speeds and can be easily integrated into a variety of end equipment solutions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP6500	FLQ (203)	40.6 mm × 31.8 mm × 6 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

DLPC910 Simplified Diagram



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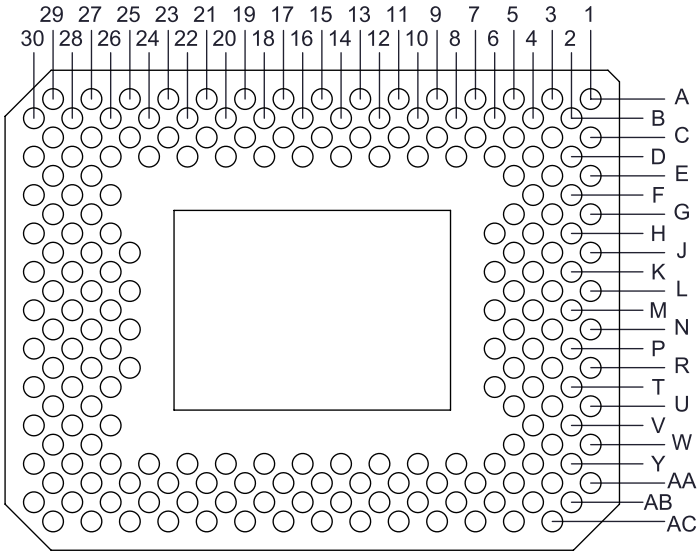
Changes from Original (October 2014) to Revision A **Page**

- Updated features to include additional digital controller. ... 1
- Added additional symplified diagram. ... 1
- Removed DLKC_C and DCLK_D, separated TCASE into TARRAY and TWINDOW, added TDELTA, and reduced fclock in *Absolute Maximum Ratings*. ... 8
- Separated handling ratings into *Storage Conditions* and *ESD Ratings*. ... 8
- Changed TDMD to TARRAY, TGRADIENT to TDELTA, and added short term operational values in *Recommended Operating Conditions* ... 9
- Updated Micromirror Derating Curve. ... 11
- Added typical characteristics when DMD is controlled with the DLPC910. ... 17
- Update CL2W constant in *Micromirror Array Termperature Calculation*. ... 28
- Added recommended idle mode operation for maximizing mirror useful life. ... 29
- Added additional typical application schematic. ... 31
- Added *DMD Mirror Park Sequence* requirements. ... 33
- Added cross reference to *DMD Mirror Park Sequence* requirements. ... 34
- Updated part number description and device markings. ... 42

5 Pin Configuration and Functions

FLQ Package
203-Pin CLGA
Bottom View



Pin Functions

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	DESCRIPTION	TRACE (mils)[4]
NAME	NO.						
DATA BUS A							
D_AN(0)	B10	Input	LVDS	DDR	Differential	Data, Negative	557.27
D_AN(1)	A13	Input	LVDS	DDR	Differential	Data, Negative	558.46
D_AN(2)	D16	Input	LVDS	DDR	Differential	Data, Negative	556.87
D_AN(3)	C17	Input	LVDS	DDR	Differential	Data, Negative	555.6
D_AN(4)	B18	Input	LVDS	DDR	Differential	Data, Negative	555.33
D_AN(5)	A17	Input	LVDS	DDR	Differential	Data, Negative	555.76
D_AN(6)	A25	Input	LVDS	DDR	Differential	Data, Negative	556.47
D_AN(7)	D22	Input	LVDS	DDR	Differential	Data, Negative	555.79
D_AN(8)	C29	Input	LVDS	DDR	Differential	Data, Negative	556.54
D_AN(9)	D28	Input	LVDS	DDR	Differential	Data, Negative	555.23
D_AN(10)	E27	Input	LVDS	DDR	Differential	Data, Negative	555.55
D_AN(11)	F26	Input	LVDS	DDR	Differential	Data, Negative	556.48
D_AN(12)	G29	Input	LVDS	DDR	Differential	Data, Negative	555.91
D_AN(13)	H28	Input	LVDS	DDR	Differential	Data, Negative	556.38
D_AN(14)	J27	Input	LVDS	DDR	Differential	Data, Negative	559.01
D_AN(15)	K26	Input	LVDS	DDR	Differential	Data, Negative	556.11
D_AP(0)	B12	Input	LVDS	DDR	Differential	Data, Positive	555.99
D_AP(1)	A11	Input	LVDS	DDR	Differential	Data, Positive	556.02
D_AP(2)	D14	Input	LVDS	DDR	Differential	Data, Positive	556.31
D_AP(3)	C15	Input	LVDS	DDR	Differential	Data, Positive	555.88
D_AP(4)	B16	Input	LVDS	DDR	Differential	Data, Positive	556.08
D_AP(5)	A19	Input	LVDS	DDR	Differential	Data, Positive	556.33
D_AP(6)	A23	Input	LVDS	DDR	Differential	Data, Positive	556.13
D_AP(7)	D20	Input	LVDS	DDR	Differential	Data, Positive	555.21
D_AP(8)	A29	Input	LVDS	DDR	Differential	Data, Positive	555.58
D_AP(9)	B28	Input	LVDS	DDR	Differential	Data, Positive	555.39
D_AP(10)	C27	Input	LVDS	DDR	Differential	Data, Positive	556.11
D_AP(11)	D26	Input	LVDS	DDR	Differential	Data, Positive	555.88
D_AP(12)	F30	Input	LVDS	DDR	Differential	Data, Positive	556.58
D_AP(13)	H30	Input	LVDS	DDR	Differential	Data, Positive	556.3
D_AP(14)	J29	Input	LVDS	DDR	Differential	Data, Positive	557.67
D_AP(15)	K28	Input	LVDS	DDR	Differential	Data, Positive	555.32
DATA BUS B							
D_BN(0)	AB10	Input	LVDS	DDR	Differential	Data, Negative	552.46
D_BN(1)	AC13	Input	LVDS	DDR	Differential	Data, Negative	556.99
D_BN(2)	Y16	Input	LVDS	DDR	Differential	Data, Negative	545.06
D_BN(3)	AA17	Input	LVDS	DDR	Differential	Data, Negative	555.44
D_BN(4)	AB18	Input	LVDS	DDR	Differential	Data, Negative	556.34
D_BN(5)	AC17	Input	LVDS	DDR	Differential	Data, Negative	547.1
D_BN(6)	AC25	Input	LVDS	DDR	Differential	Data, Negative	557.92
D_BN(7)	Y22	Input	LVDS	DDR	Differential	Data, Negative	544.03

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.
(2) DDR = Double Data Rate.
SDR = Single Data Rate.
Refer to the *Timing Requirements* for specifications and relationships.
(3) Internal term = CMOS level internal termination.
Refer to *Recommended Operating Conditions* for differential termination specification.
(4) Dielectric Constant for the DMD Type A ceramic package is approximately 9.6.
For the package trace lengths shown:
Propagation Speed = 11.8 / sqrt(9.6) = 3.808 in/ns.
Propagation Delay = 0.262 ns/in = 262 ps/in = 10.315 ps/mm.

Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	DESCRIPTION	TRACE (mils)[4]
NAME	NO.						
D_BN(8)	AA29	Input	LVDS	DDR	Differential	Data, Negative	555.9
D_BN(9)	Y28	Input	LVDS	DDR	Differential	Data, Negative	555.42
D_BN(10)	W27	Input	LVDS	DDR	Differential	Data, Negative	556.26
D_BN(11)	V26	Input	LVDS	DDR	Differential	Data, Negative	555.52
D_BN(12)	T30	Input	LVDS	DDR	Differential	Data, Negative	556
D_BN(13)	R29	Input	LVDS	DDR	Differential	Data, Negative	557.17
D_BN(14)	R27	Input	LVDS	DDR	Differential	Data, Negative	555.25
D_BN(15)	N27	Input	LVDS	DDR	Differential	Data, Negative	555.19
D_BP(0)	AB12	Input	LVDS	DDR	Differential	Data, Positive	551.93
D_BP(1)	AC11	Input	LVDS	DDR	Differential	Data, Positive	557.1
D_BP(2)	Y14	Input	LVDS	DDR	Differential	Data, Positive	544.38
D_BP(3)	AA15	Input	LVDS	DDR	Differential	Data, Positive	555.98
D_BP(4)	AB16	Input	LVDS	DDR	Differential	Data, Positive	555.56
D_BP(5)	AC19	Input	LVDS	DDR	Differential	Data, Positive	547.17
D_BP(6)	AC23	Input	LVDS	DDR	Differential	Data, Positive	556.47
D_BP(7)	Y20	Input	LVDS	DDR	Differential	Data, Positive	543.25
D_BP(8)	AC29	Input	LVDS	DDR	Differential	Data, Positive	555.71
D_BP(9)	AB28	Input	LVDS	DDR	Differential	Data, Positive	556.32
D_BP(10)	AA27	Input	LVDS	DDR	Differential	Data, Positive	555.35
D_BP(11)	Y26	Input	LVDS	DDR	Differential	Data, Positive	555.65
D_BP(12)	U29	Input	LVDS	DDR	Differential	Data, Positive	555.28
D_BP(13)	T28	Input	LVDS	DDR	Differential	Data, Positive	557.25
D_BP(14)	P28	Input	LVDS	DDR	Differential	Data, Positive	555.83
D_BP(15)	P26	Input	LVDS	DDR	Differential	Data, Positive	556.67
SERIAL CONTROL							
SCTRL_AN	C21	Input	LVDS	DDR	Differential	Serial Control, Negative	555.14
SCTRL_BN	AA21	Input	LVDS	DDR	Differential	Serial Control, Negative	555.14
SCTRL_AP	C23	Input	LVDS	DDR	Differential	Serial Control, Positive	555.13
SCTRL_BP	AA23	Input	LVDS	DDR	Differential	Serial Control, Positive	555.13
CLOCKS							
DCLK_AN	B22	Input	LVDS		Differential	Clock Negative	555.12
DCLK_BN	AB22	Input	LVDS		Differential	Clock Negative	555.12
DCLK_AP	B24	Input	LVDS		Differential	Clock Positive	555.13
DCLK_BP	AB24	Input	LVDS		Differential	Clock Positive	555.12
SERIAL COMMUNICATIONS PORT (SCP)							
SCP_DO	B2	Output	LVCMOS	SDR		Serial Communications Port Output	525.78
SCP_DI	F4	Input	LVCMOS	SDR	Pull-Down	Serial Communications Port Data Input	509.96
SCP_CLK	E3	Input	LVCMOS		Pull-Down	Serial Communications Port Clock	403.93
SCP_ENZ	D4	Input	LVCMOS		Pull-Down	Active-low Serial Communications Port Enable	464.17
MICROMIRROR RESET CONTROL							
RESET_ADDR(0)	C5	Input	LVCMOS		Pull-Down	Reset Driver Address Select	1088.3
RESET_ADDR(1)	E5	Input	LVCMOS		Pull-Down	Reset Driver Address Select	979.26
RESET_ADDR(2)	G5	Input	LVCMOS		Pull-Down	Reset Driver Address Select	900.45
RESET_ADDR(3)	AC3	Input	LVCMOS		Pull-Down	Reset Driver Address Select	658.56
RESET_MODE(0)	D8	Input	LVCMOS		Pull-Down	Reset Driver Mode Select	1012.52
RESET_MODE(1)	C11	Input	LVCMOS		Pull-Down	Reset Driver Mode Select	789.83
RESET_SEL(0)	T4	Input	LVCMOS		Pull-Down	Reset Driver Level Select	539.64
RESET_SEL(1)	U5	Input	LVCMOS		Pull-Down	Reset Driver Level Select	400.3
RESET_STROBE	V2	Input	LVCMOS		Pull-Down	Reset Address, Mode, & Level latched on rising-edge	446.34

Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	DESCRIPTION	TRACE (mils)[4]
NAME	NO.						
ENABLES & INTERRUPTS							
PWRDNZ	C3	Input	LVCMOS		Pull-Down	Active-low Device Reset	390.76
RESET_OEZ	W1	Input	LVCMOS		Pull-Down	Active-low output enable for DMD reset driver circuits	513.87
RESETZ	G3	Input	LVCMOS		Pull-Down	Active-low sets Reset circuits in known VOFFSET state	941.63
RESET_IRQZ	T6	Output	LVCMOS			Active-low, output interrupt to ASIC	403.34
VOLTAGE REGULATOR MONITORING							
PG_BIAS	AA11	Input	LVCMOS		Pull-Up	Active-low fault from external VBIAS regulator	858.86
PG_OFFSET	Y10	Input	LVCMOS		Pull-Up	Active-low fault from external VOFFSET regulator	822.06
PG_RESET	V4	Input	LVCMOS		Pull-Up	Active-low fault from external VRESET regulator	1186.98
EN_BIAS	D12	Output	LVCMOS			Active-high enable for external VBIAS regulator	167.53
EN_OFFSET	AB8	Output	LVCMOS			Active-high enable for external VOFFSET regulator	961.04
EN_RESET	H2	Output	LVCMOS			Active-high enable for external VRESET regulator	566.05
LEAVE PIN UNCONNECTED							
MBRST(0)	P2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1167.69
MBRST(1)	AB4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1348.04
MBRST(2)	AA7	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1240.35
MBRST(3)	N3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1030.51
MBRST(4)	M4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	870.63
MBRST(5)	AB6	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1267.73
MBRST(6)	AA5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1391.22
MBRST(7)	L3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1064.01
MBRST(8)	Y6	Output	Analog		Pull-Down	For proper DMD operation, do not connect	552.89
MBRST(9)	K4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	992.63
MBRST(10)	L5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1063.13
MBRST(11)	AC5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	641.44
MBRST(12)	Y8	Output	Analog		Pull-Down	For proper DMD operation, do not connect	428.07
MBRST(13)	J5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	962.91
MBRST(14)	K6	Output	Analog		Pull-Down	For proper DMD operation, do not connect	1093.63
MBRST(15)	AC7	Output	Analog		Pull-Down	For proper DMD operation, do not connect	577.13
LEAVE PIN UNCONNECTED							
RESERVED_PFE	AA1	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	1293.6
RESERVED_TM	B6	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	365.64
RESERVED_XI1	D2	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	689.96
RESERVED_TP0	Y2	Input	Analog			For proper DMD operation, do not connect	667.66
RESERVED_TP1	P6	Input	Analog			For proper DMD operation, do not connect	623.99
RESERVED_TP2	W3	Input	Analog			For proper DMD operation, do not connect	564.35
LEAVE PIN UNCONNECTED							
RESERVED_BA	U3	Output	LVCMOS			For proper DMD operation, do not connect	684.44
RESERVED_BB	C9	Output	LVCMOS			For proper DMD operation, do not connect	223.73
RESERVED_TS	D10	Output	LVCMOS			For proper DMD operation, do not connect	90.87
LEAVE PIN UNCONNECTED							
NO CONNECT	H6					For proper DMD operation, do not connect	

PIN		TYPE (I/O/P)	SIGNAL	DESCRIPTION
NAME(1)	NO.			
VBIAS	N5, P4, R3, R5	Power	Analog	Supply voltage for positive Bias level of Micromirror reset signal.
VOFFSET	G1, J1, L1, N1, R1	Power	Analog	Supply voltage for HVCMOS logic. Supply voltage for stepped high voltage at Micromirror address electrodes. Supply voltage positive Offset level of Micromirror reset signal.
VRESET	A3, A5, B4, C7	Power	Analog	Power supply for negative reset level of mirror reset signal
VCC	A7, A15, C1	Power	Analog	Supply voltage for LVCMOS core logic.
	E1, U1, AB2	Power	Analog	Supply voltage for normal high level at Micromirror address electrodes.
	AC9, AC15	Power	Analog	Supply voltage for positive Offset level of Micromirror reset signal during Power Down sequence.
VCCI	A21, A27, D30, M30, Y30, AC21, AC27	Power	Analog	Power supply for LVDS Interface
VSS	A1, A9, B8, B14, B20, B26, B30, C13, C19, C25, D6, D18, D24, E29, F2, F28, G27, H4, H26, J3, J25, K2, K30, L25, L27, L29, M2, M6, M26, M28, N25, N29, P30, R25, T2, T26, U27, V28, V30, W5, W29, Y4, Y12, Y18, Y24, AA3, AA9, AA13, AA19, AA25, AB14, AB20, AB26, AB30	Power	Analog	Device Ground. Common return for all power.

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

SUPPLY VOLTAGES		MIN	MAX	UNIT
VCC	Supply voltage for LVCMOS core logic (2)	–0.5	4	V
VCCI	Supply voltage for LVDS receivers (2)	–0.5	4	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (2) (3)	–0.5	9	V
VBIAS	Supply voltage for micromirror electrode (2)	–0.5	17	V
VRESET	Supply voltage for micromirror electrode (2)	–11	0.5	V
| VCC – VCCI |	Supply voltage delta (absolute value) (4)		0.3	V
| VBIAS – VOFFSET |	Supply voltage delta (absolute value) (5)		8.75	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins (2)	–0.5	VCC + 0.3	V
	Input voltage for all other LVDS input pins (2)	–0.5	VCCI + 0.3	V
$\|V_{ID}\|$	Input differential voltage (absolute value) (2) (6)		700	mV
I_{ID}	Input differential current (7)		7	mA
CLOCKS				
f_{clock}	Clock frequency for LVDS interface, DCLK_A		440	MHz
	Clock frequency for LVDS interface, DCLK_B		440	
ENVIRONMENTAL				
T_{ARRAY}	Array temperature: operational (8) (9)	0	90	°C
	Array temperature: non-operational (8) (9)	-40	90	
T_{WINDOW}	Window temperature: operational	0	65	°C
	Window temperature: non–operational	-40	90	
$\|T_{DELTA}\|$	Absolute termperature delta between the window test point and the ceramic test point TP1 (10)		10	°C
RH	Relative Humidity, operating and non–operating		95	%

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(3) VOFFSET supply transients must fall within specified voltages.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. Refer to *Power Supply Requirements* for additional information.
(6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) Exposure of the DMD simultaneously to any combination of the maximum operating conditions for case temperature, differential temperature, or illumination power density will reduce device lifetime. Refer to *ESD Ratings*.
(9) The highest temperature of the active array as calculated by the *Micromirror Array Temperature Calculation* using ceramic test point 1 (TP1) in Figure 15.
(10) Temperature delta is the highest difference between the ceramic test point TP1 and window test points TP2 and TP3 in Figure 15.

6.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T_{DMD}	Storage temperature range (non-operating)	–40	80	°C
RH	Relative Humidity (non-condensing)		95%	

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES(1)(2)					
VCC	Supply voltage for LVCMOS core logic	3.0	3.3	3.6	V
VCCI	Supply voltage for LVDS receivers	3.0	3.3	3.6	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrodes(3)	8.25	8.5	8.75	V
VBIAS	Supply voltage for micromirror electrodes	15.5	16	16.5	V
VRESET	Mirror electrode voltage	–9.5	–10	–10.5	V
| VCCI–VCC |	Supply voltage delta (absolute value) (4)			0.3	V
| VBIAS–VOFFSET |	Supply voltage delta (absolute value) (5)			8.75	V
LVCMOS PINS					
V_{IH}	High level Input voltage(6)	1.7	2.5	VCC + 0.3	V
V_{IL}	Low level Input voltage(6)	–0.3		0.7	V
I_{OH}	High level output current at VOH = 2.4 V			–20	mA
I_{OL}	Low level output current at VOL = 0.4 V			15	mA
T_{PWRDNZ}	PWRDNZ pulse width(7)	10			ns
SCP INTERFACE(5)					
f_{clock}	SCP clock frequency(8)			500	kHz
t_{SCP_SKEW}	Time between valid SCPDI and rising edge of SCPCLK(9)	–800		800	ns
t_{SCP_DELAY}	Time between valid SCPDO and rising edge of SCPCLK(9)			700	ns
$t_{SCP\_BYTE\_INTERVAL\_}$	Time between consecutive bytes	1			µs
$t_{SCP\_NEG\_ENZ}$	Time between falling edge of SCPENZ and the first rising edge of SCPCLK	30			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			µs
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)			1.5	ns
f_{clock}	SCP circuit clock oscillator frequency(10)	9.6		11.1	MHz
LVDS INTERFACE					
f_{clock}	Clock frequency DCLK			400	MHz
$\| V_{ID} \|$	Input differential voltage (absolute value)(11)	100	400	600	mV
V_{CM}	Common mode(11)		1200		mV

(1) Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) All voltages are referenced to common ground VSS.
(3) VOFFSET supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. Refer to *Power Supply Requirements* for additional information.
(6) Tester Conditions for VIH and VIL:
Frequency = 60 MHz. Maximum Rise Time = 2.5 ns @ (20% to 80%)
Frequency = 60 MHz. Maximum Fall Time = 2.5 ns @ (80% to 20%)
(7) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(8) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(9) Refer to Figure 3.
(10) SCP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.
(11) Refer to Figure 4, Figure 5, and Figure 6.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{LVDS}	LVDS voltage (11)	0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL (12)	**For Illumination Source Between 420 nm and 700 nm**				
T_{ARRAY}	Array temperature, Long-term operational (13)(14)(15)	10		40 to 65 (16)	°C
	Array temperature, Short-term operational (13)(14)(17)	0		10	°C
T_{WINDOW}	Window Temperature test points TP2 and TP3, Long-term operational. (15)	10		65	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1 (18)			10	°C
ILL_{VIS}	Illumination, wavelengths between 420 nm and 700 nm			Thermally Limited (19)	mW/cm^2
RH	Relative Humidity (non-condensing)			95%	
ENVIRONMENTAL (12)	**For Illumination Source Between 400 nm and 420 nm**				
T_{ARRAY}	Array temperature, Long-term operational (13)(14)(15)	20		30 (16)	°C
	Array temperature, Short-term operational (13)(14)(17)	0		20	°C
T_{WINDOW}	Window Temperature test points TP2 and TP3, Long-term operational. (15)			30	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1 (18)			10	°C
ILL_{VIS}	Illumination, wavelengths between 400 and 420 nm			10	W/cm^2
RH	Relative Humidity (non-condensing)			95%	
ENVIRONMENTAL (12)	**For Illumination Source <400 nm and >700 nm**				
T_{ARRAY}	Array temperature, Long-term operational (13)(14)(15)	10		40 to 65 (16)	°C
	Array temperature, Short-term operational (13)(14)(17)	0		10	°C
T_{WINDOW}	Window Temperature test points TP2 and TP3, Long-term operational. (15)	10		65	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1 (18)			10	°C
ILL_{UV}	Illumination, wavelength < 400 nm			0.68	mW/cm^2
ILL_{IR}	Illumination, wavelength > 700 nm			10	mW/cm^2
RH	Relative Humidity (non-condensing)			95%	

(12) Optimal, long-term performance and optical effciency of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(13) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(14) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 15 and the package thermal resistance *Thermal Information* using *Micromirror Array Temperature Calculation*.
(15) Long-term is defined as the usable life of the device.
(16) Per Figure 1, the maximum operational case temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-on/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(17) Array and Window temperatures beyond those specified as long-term are recommended for short-term conditions only (power- up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(18) Temperature delta is the highest difference between the ceramic test point (TP1) and window test points (TP2) and (TP3) in Figure 15.
(19) Refer to *Thermal Information* and *Micromirror Array Temperature Calculation*.

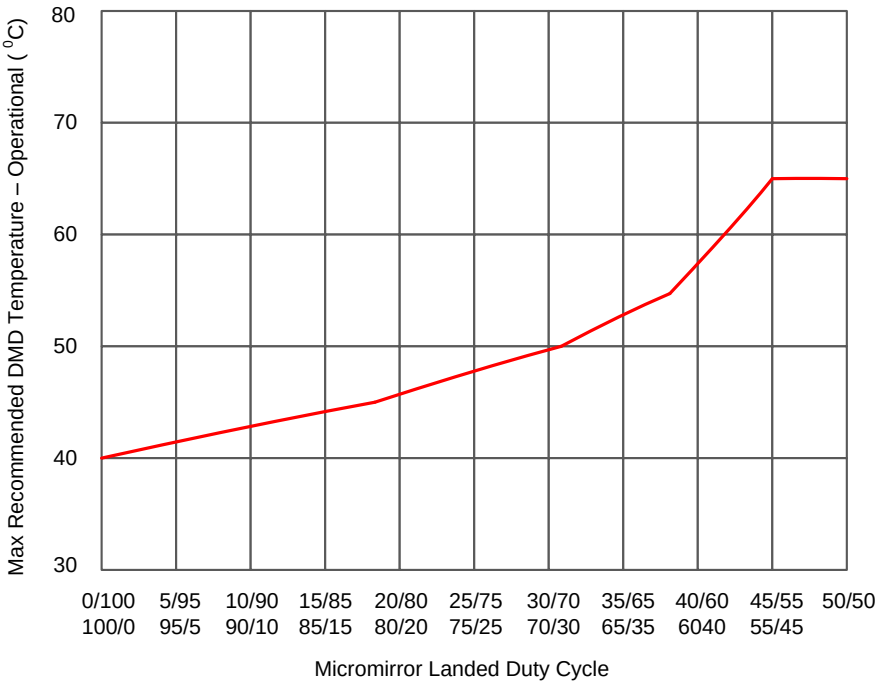


Figure 1. Max Recommended DMD Temperature – Derating Curve

6.5 Thermal Information

THERMAL METRIC (1)	DLP6500 FLQ (CLGA) 203 PINS	UNIT
Active Area to Case Ceramic Thermal resistance (1)	0.7	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	VCC = 3 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low level output voltage	VCC = 3.6 V, I_{OL} = 15 mA			0.4	V
I_{IH}	High–level input current(2)(3)	VCC = 3.6 V, VI = VCC			250	µA
IIL	Low level input current	VCC = 3.6 V, V_I = 0	–250			µA
I_{OZ}	High–impedance output current	VCC = 3.6 V			10	µA
CURRENT						
I_{CC}	Supply current(4)	VCC = 3.6 V			1076	mA
I_{CCI}	Supply current(4)	VCCI = 3.6 V			518	
I_{OFFSET}	Supply current(5)	V_{OFFSET} = 8.75 V			4	mA
I_{BIAS}	Supply current(5)	V_{BIAS} = 16.5 V			14	
I_{RESET}	Supply current	V_{RESET} = –10.5 V			11	mA
I_{TOTAL}	Supply current	Total Sum			1623	
POWER						
P_{CC}	Supply power dissipation	VCC = 3.6 V			3874	mW
P_{CCI}		VCCI = 3.6 V			1865	
P_{OFFSET}		V_{OFFSET} = 8.75 V			35	
P_{BIAS}		V_{BIAS} = 16.5 V			231	
P_{RESET}		V_{RESET} = –10.5 V			116	
P_{TOTAL}	Supply power dissipation(6)	Total Sum			6300	
CAPACITANCE						
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Output capacitance	f = 1 MHz			10	pF
C_M	Reset group capacitance MBRST(14:0)	f = 1 MHz; 1920 × 72 micromirrors	330		390	pF

(1) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) Applies to LVCMOS input pins only. Does not apply to LVDS pins and MBRST pins.
(3) LVCMOS input pins utilize an internal 18000 Ω passive resistor for pull-up and pull-down configurations. Refer to *Pin Configuration and Functions* to determine pull-up or pull-down configuration used.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(6) Total power on the active micromirror array is the sum of the electrical power dissipation and the absorbed power from the illumination source. See the *Micromirror Array Temperature Calculation*.

6.7 Timing Requirements

Over *Recommended Operating Conditions* unless otherwise noted.

DESCRIPTION[1]				MIN	TYP	MAX	UNIT
SCP INTERFACE[2]							
t_r	Rise time	20% to 80%				200	ns
t_f	Fall time	80% to 20%				200	ns
LVDS INTERFACE[2]							
t_r	Rise time	20% to 80%		100		400	ps
t_f	Fall time	80% to 20%		100		400	ps
LVDS CLOCKS[3]							
t_c	Cycle time	DCLK_A, 50% to 50%		2.5			ns
		DCLK_B, 50% to 50%		2.5			
t_w	Pulse duration	DCLK_A, 50% to 50%		1.19	1.25		ns
		DCLK_B, 50% to 50%		1.19	1.25		
LVDS INTERFACE[3]							
t_{su}	Setup time	D_A(15:0) before rising or falling edge of DCLK_A		0.2			ns
		D_B(15:0) before rising or falling edge of DCLK_B		0.2			
t_{su}	Setup time	SCTRL_A before rising or falling edge of DCLK_A		0.2			ns
		SCTRL_B before rising or falling edge of DCLK_B		0.2			
t_h	Hold time	D_A(15:0) after rising or falling edge of DCLK_A		0.5			ns
		D_B(15:0) after rising or falling edge of DCLK_B		0.5			
t_h	Hold time	SCTRL_A after rising or falling edge of DCLK_A		0.5			ns
		SCTRL_B after rising or falling edge of DCLK_B		0.5			
LVDS INTERFACE[4]							
t_{skew}	Skew time	Channel B relative to Channel A	Channel A includes the following LVDS pairs: DCLK_AP and DCLK_AN SCTRL_AP and SCTRL_AN D_AP(15:0) and D_AN(15:0)	–1.25		1.25	ns
			Channel B includes the following LVDS pairs: DCLK_BP and DCLK_BN SCTRL_BP and SCTRL_BN D_BP(15:0) and D_BN(15:0)				

(1) Refer to *Pin Configuration and Functions* for pin details.
(2) Refer to Figure 7.
(3) Refer to Figure 8.
(4) Refer to Figure 9.

Timing Diagrams

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 2 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Refer to the *Application and Implementation* section.

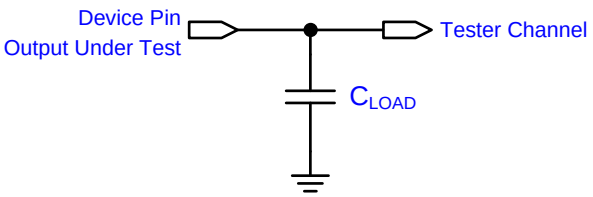
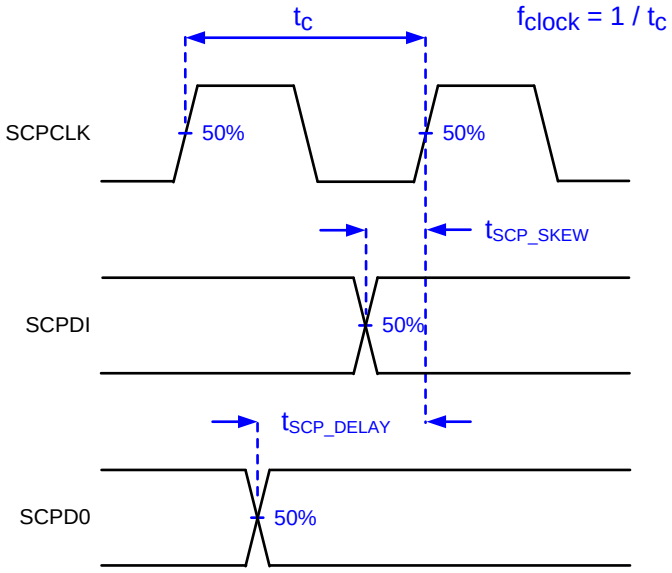


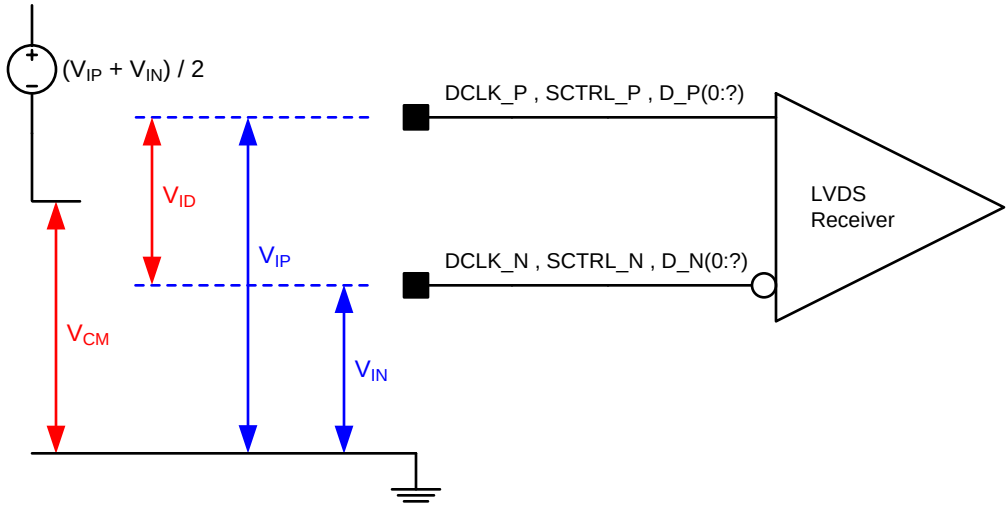
Figure 2. Test Load Circuit



Not to scale.

Refer to SCP Interface section of the *Recommended Operating Conditions* table.

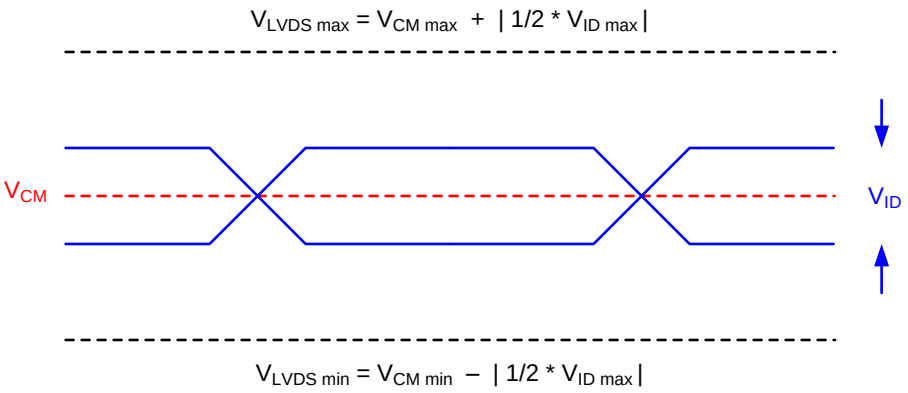
Figure 3. SCP Timing Parameters



Refer to the LVDS Interface section of the *Recommended Operating Conditions* table.

Refer to *Pin Configuration and Functions* for a list of LVDS pins.

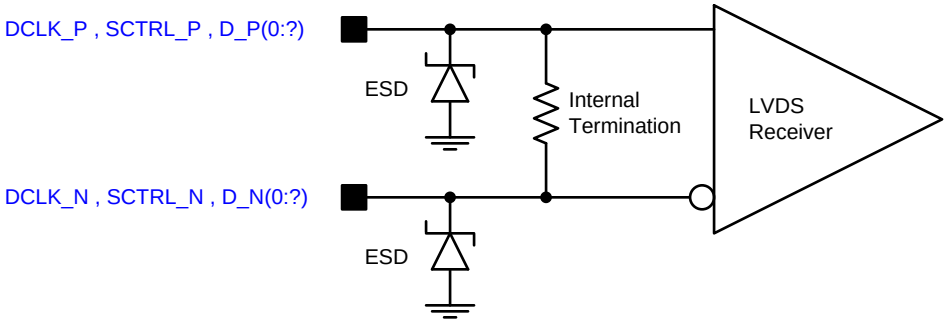
Figure 4. LVDS Voltage Definitions (References)



Not to scale.

Refer to the LVDS Interface section of the *Recommended Operating Conditions* table.

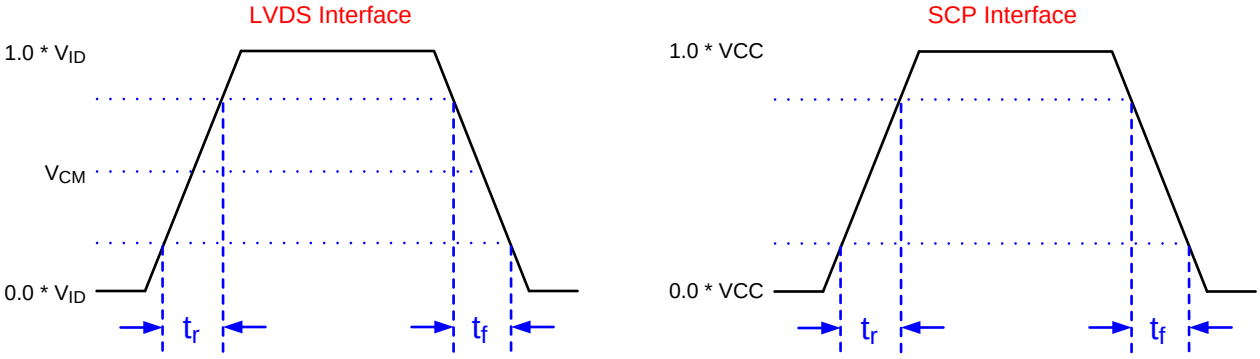
Figure 5. LVDS Voltage Parameters



Refer to LVDS Interface section of the *Recommended Operating Conditions* table

Refer to *Pin Configuration and Functions* for list of LVDS pins.

Figure 6. LVDS Equivalent Input Circuit

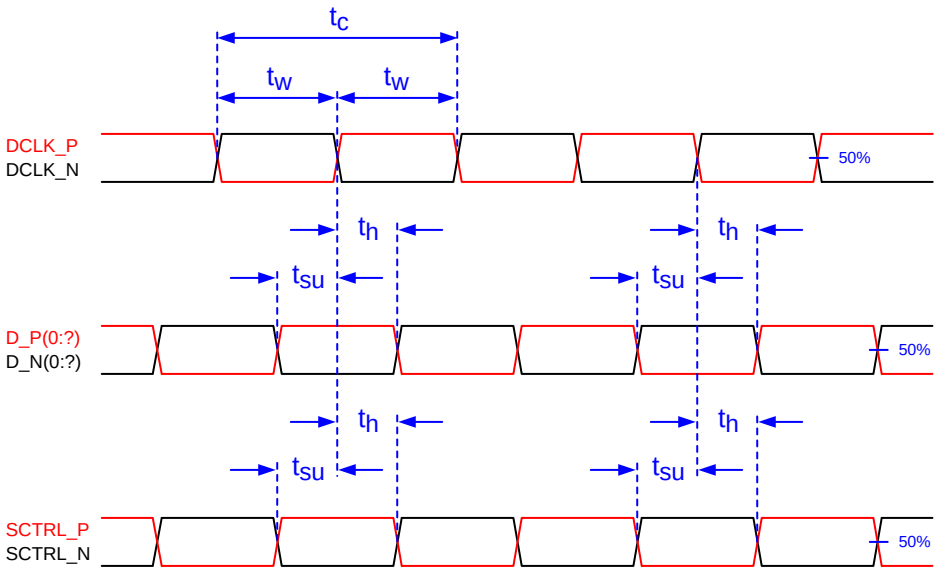


Not to scale.

Refer to the *Timing Requirements* table.

Refer to *Pin Configuration and Functions* for list of LVDS pins and SCP pins.

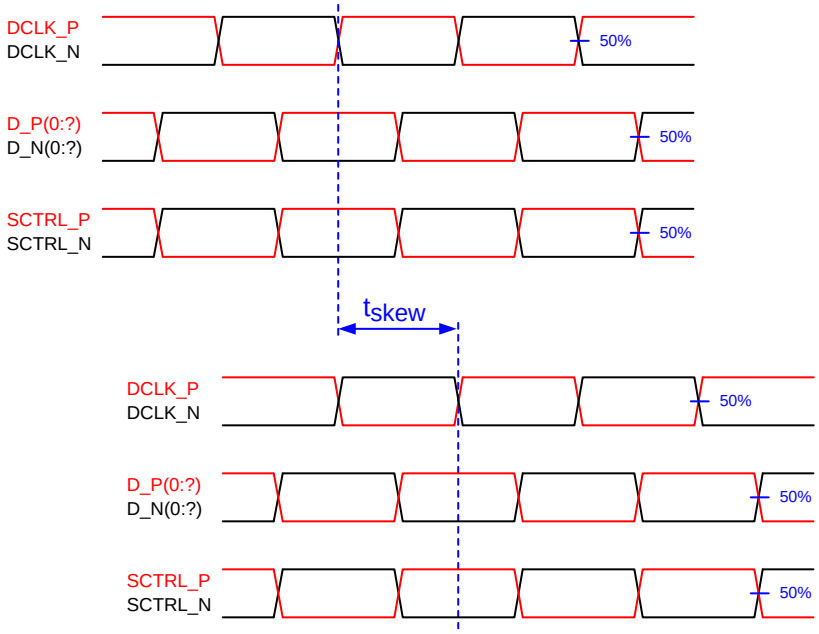
Figure 7. Rise Time and Fall Time



Not to scale.

Refer to LVDS INTERFACE section in the *Timing Requirements* table.

Figure 8. Timing Requirement Parameter Definitions



Not to scale.

Refer to LVDS INTERFACE in the *Timing Requirements* table.

Figure 9. LVDS Interface Channel Skew Definition

6.8 Typical Characteristics

When the DMD is controlled by the DLPC900, the digital controller has four modes of operation.

1. Video Mode
2. Video Pattern Mode
3. Pre-Stored Pattern Mode
4. Pattern On-The-Fly Mode

In video mode, the video source is displayed on the DMD at the rate of the incoming video source.

In modes 2, 3, and 4, the pattern rates depend on the bit depth as shown in Table 1.

Table 1. DLPC900 with DLP6500 Pattern Rate versus Bit Depth

BIT DEPTH	VIDEO PATTERN MODE (Hz)	PRE-STORED or PATTERN ON-THE-FLY MODE (Hz)
1	2880	9523
2	1440	3289
3	960	2638
4	720	1364
5	480	823
6	480	672
7	360	500
8	247	247

When the DLP6500 DMD is controlled by the DLPC910, the controller operates in pattern mode only. With proper illumination modulation, bit depths greater than 1 can be achieved. Table Table 2 shows the pattern rates for each bit depth.

Table 2. DLPC910 with DLP6500 Pattern Rate versus Bit Depth

BIT DEPTH	PATTERN RATE (Hz)
1	11574
2	5787
3	3858
4	2893
5	2315
6	1929
7	1653
8	1446

6.9 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal Interface area (See Figure 10)			25	lbs
	Electrical Interface area			95	lbs
	Datum “A” Interface area(1)			90	lbs

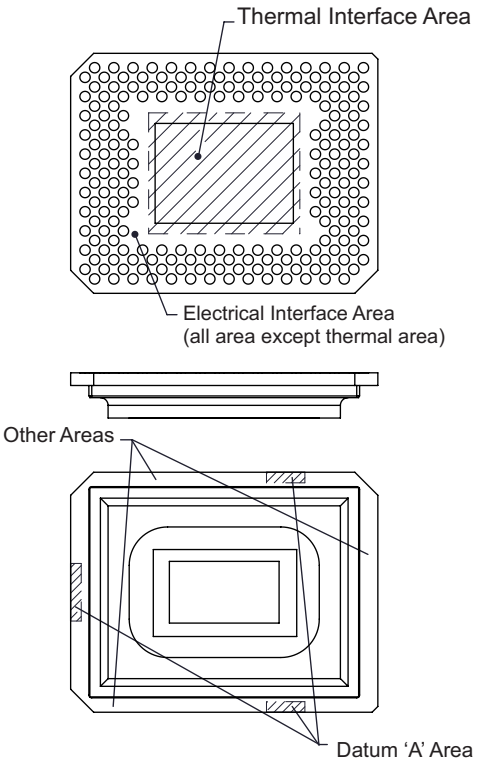


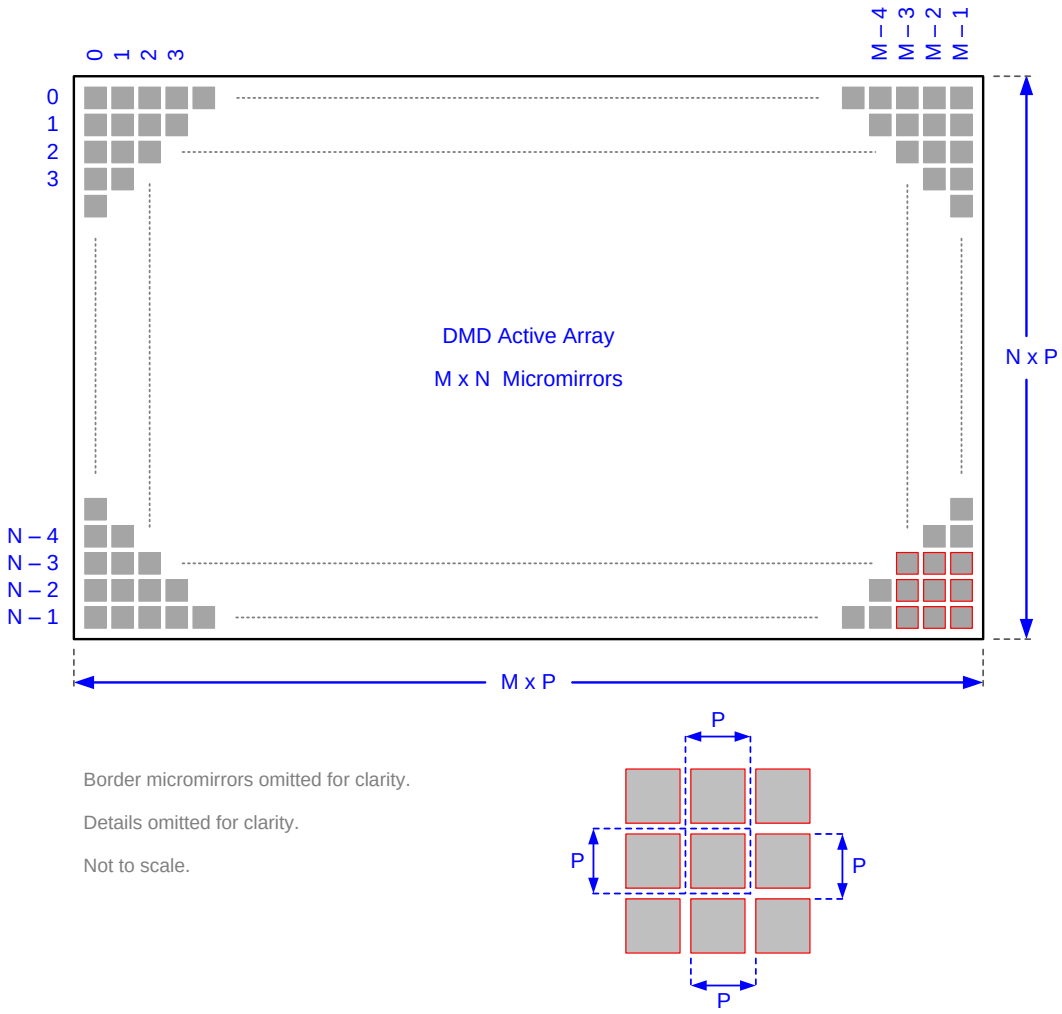
Figure 10. System Mounting Interface Loads

(1) Combined loads of the thermal and electrical interface areas in excess of Datum “A” load shall be evenly distributed outside the Datum “A” area (95 + 25 – Datum “A).

6.10 Micromirror Array Physical Characteristics

PARAMETER				VALUE	UNIT
M	Number of active columns		See Figure 11	1920	micromirrors
N	Number of active rows			1080	micromirrors
P	Micromirror (pixel) pitch			7.56	µm
	Micromirror active array width	M × P		14.5152	mm
	Micromirror active array height	N × P		8.1648	mm
	Micromirror active border	Pond of micromirror (POM)(1)		14	micromirrors /side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

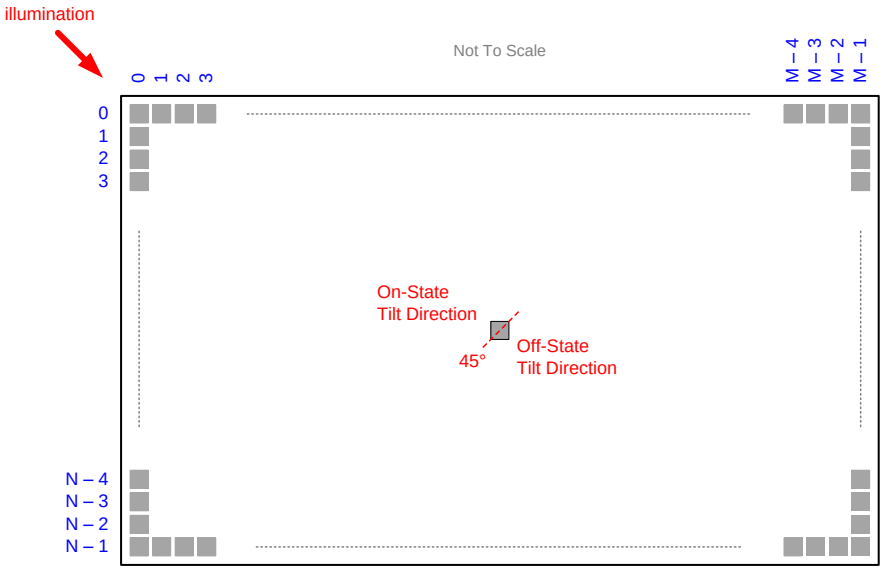
Figure 11. Micromirror Array Physical Characteristics

6.11 Micromirror Array Optical Characteristics

See *Optical Interface and System Image Quality* for important information.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD landed state (1)		12		°
β	Micromirror tilt angle tolerance (1) (2)(3)(4)(5)		–1		1	°
	Micromirror tilt direction (5)(6) (7)	Figure 12	44	45	46	°
	Number of out-of-specification micromirrors (7)	Adjacent micromirrors			0	micromirrors
		Non-adjacent micromirrors			10	
	Micromirror crossover time (8)(9)	Typical performance		2.5		µs
	DMD efficiency within the wavelength range 400 nm to 420 nm (10)			68%		
	DMD photopic efficiency within the wavelength range 420 nm to 700 nm (10)			66%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.
(8) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.
(9) Performance as measured at the start of life.
(10) Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 12. Micromirror Landed Orientation and Tilt

6.12 Window Characteristics

PARAMETER(1)	CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation	Corning 7056				
Window refractive index	at wavelength 589 nm		1.487		
Window aperture(2)	See(2)				
Illumination overfill(3)	See(3)				
Window transmittance, single–pass through both surfaces and glass (4)	At wavelength 405 nm. Applies to 0° and 24° AOI only.	95%			
	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Window Characteristics and Optics* for more information.
(2) For details regarding the size and location of the window aperture, see the package mechanical characteristics listed in the Mechanical ICD in section Mechanical, Packaging, and Orderable Information.
(3) Refer to *Illumination Overfill*.
(4) See the TI application report DLPA031, *Wavelength Transmittance Considerations for DLP® DMD Window*.

6.13 Chipset Component Usage Specification

The DLP6500 is a component of one or more DLP chipsets. Reliable function and operation of the DLP6500 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

7 Detailed Description

7.1 Overview

DLP6500 DMD is a 0.65 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in Figure 11.

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR).

DLP6500 DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the *Functional Block Diagram*.

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

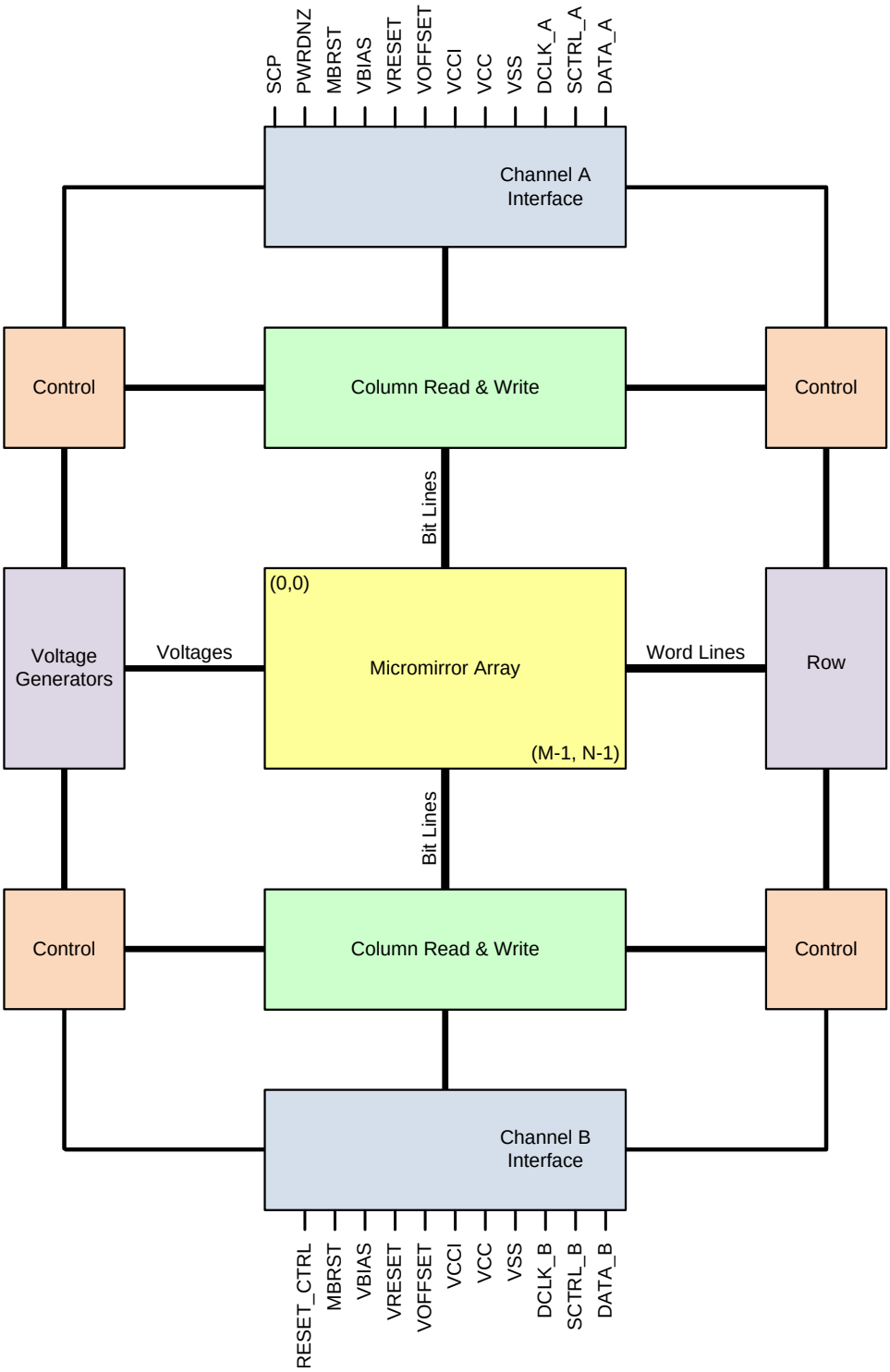
Each cell of the *M* × *N* memory array drives its true and complement ('Q' and 'QB') data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. Refer to *Micromirror Array Optical Characteristics*. The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to *Pin Configuration and Functions* for more information on micromirror reset control.

7.2 Functional Block Diagram

Not to Scale. Details Omitted for Clarity. See Accompanying Notes in this Section.



For pin details on Channels A, and B, refer to *Pin Configuration and Functions* and *Timing Requirements* notes 5 through 8.

Refer to *Micromirror Array Physical Characteristics* for dimensions, orientation, and tilt angle.

7.3 Feature Description

DLP6500 device consists of highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional orthogonal pixel array. Refer to Figure 11 and Figure 13.

Each aluminum micromirror is switchable between two discrete angular positions, –α and +α. The angular positions are measured relative to the micromirror array plane, which is parallel to the silicon substrate. Refer to *Micromirror Array Optical Characteristics* and Figure 14.

The parked position of the micromirror is not a latched position and is therefore not necessarily perfectly parallel to the array plane. Individual micromirror flat state angular positions may vary. Tilt direction of the micromirror is perpendicular to the hinge-axis. The on-state landed position is directed toward the left-top edge of the package, as shown in Figure 13.

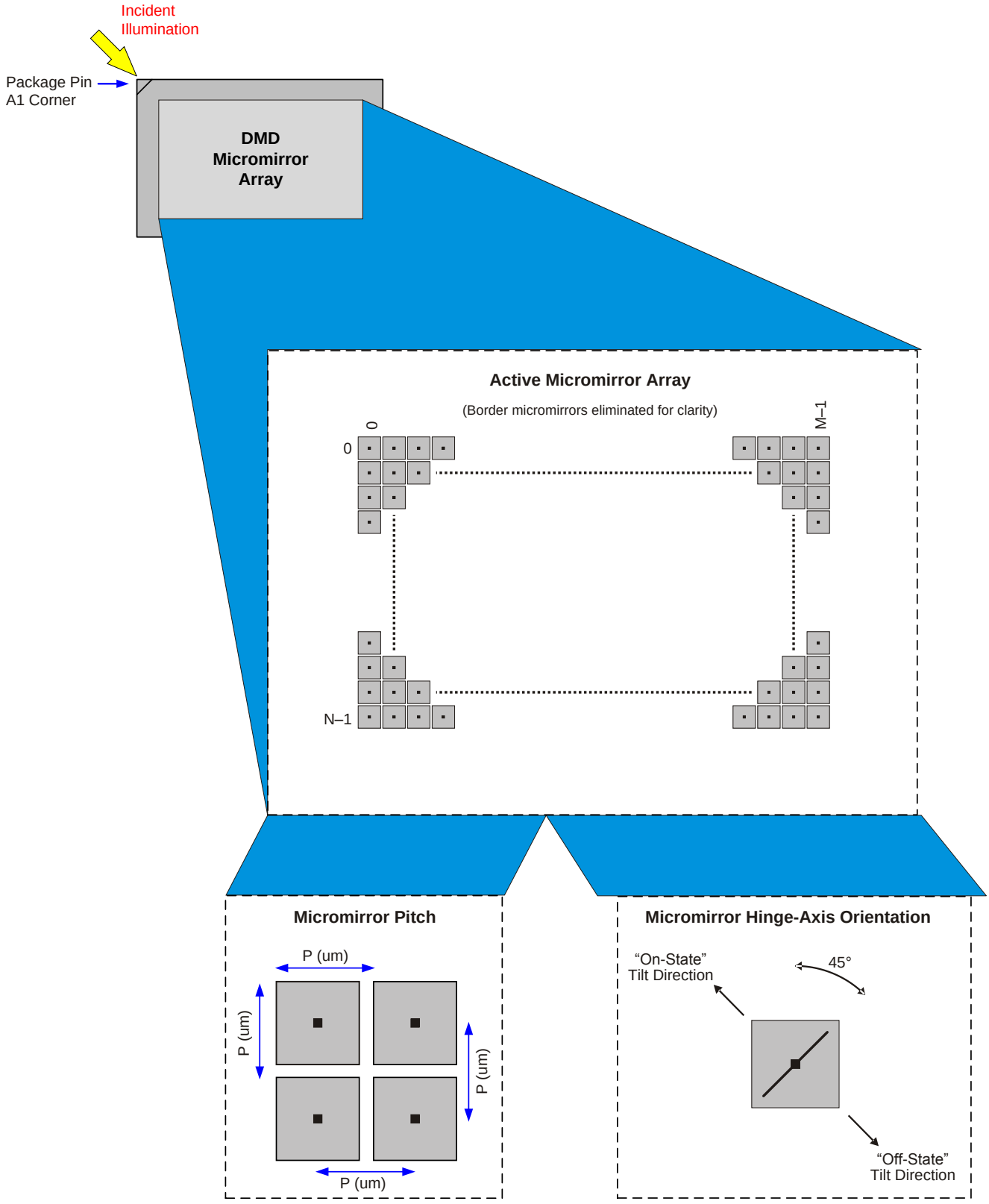
Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror clocking pulse is applied. The angular position (–α and +α) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update.

Writing logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a +α position. Writing logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a – α position.

Updating the angular position of the micromirror array consists of two steps. First, update the contents of the CMOS memory. Second, apply a micromirror reset to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror reset pulses are generated internally by the DLP6500 DMD with application of the pulses being coordinated by the digital controller.

For more information, see the TI application report DLPA008A, *DMD101: Introduction to Digital Micromirror Device (DMD) Technology*.

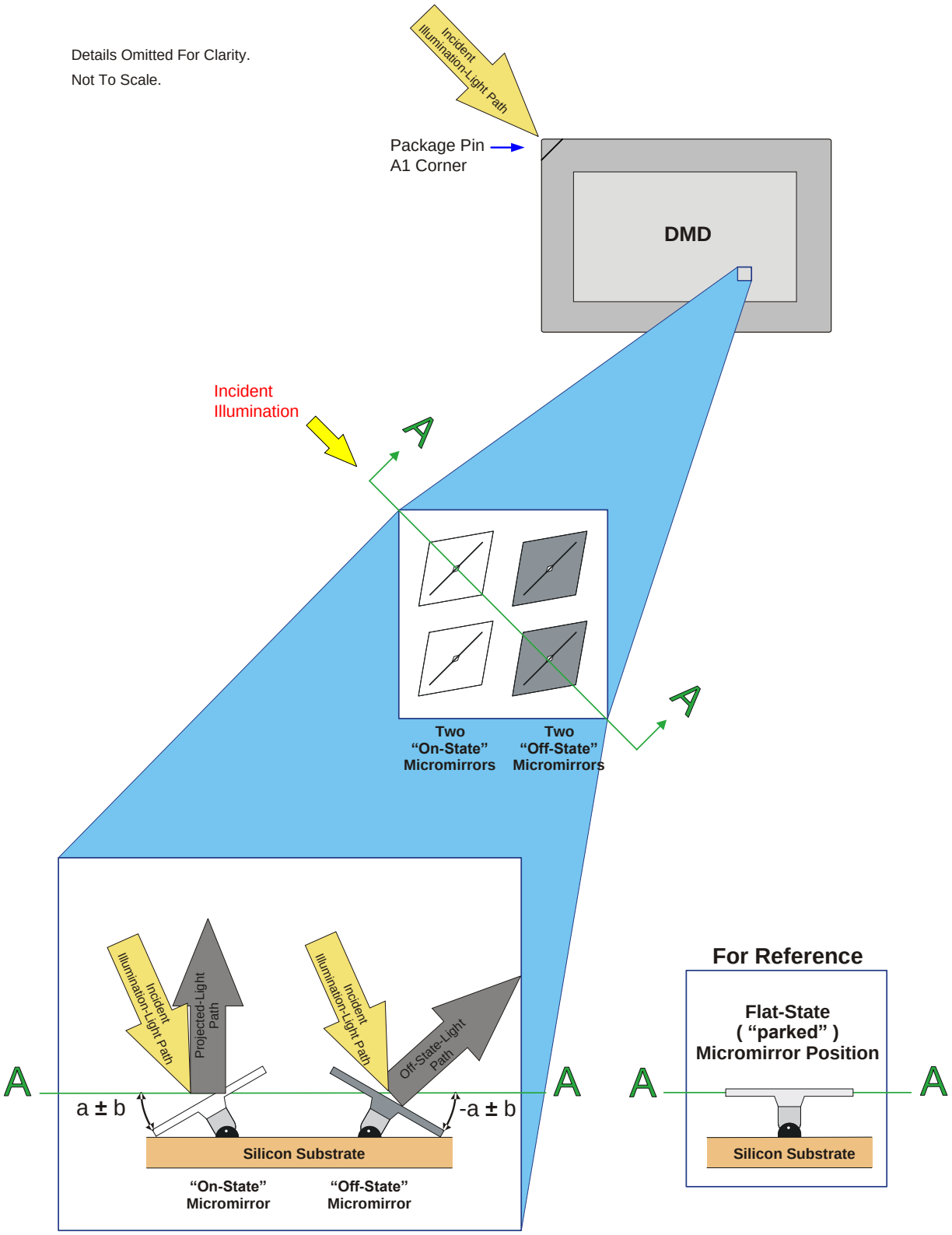
Feature Description (continued)



Refer to *Micromirror Array Physical Characteristics*, Figure 11, and Figure 12.

Figure 13. Micromirror Array, Pitch, Hinge Axis Orientation

Feature Description (continued)



Refer to *Micromirror Array Optical Characteristics* and Figure 12.

Figure 14. Micromirror States: On, Off, Flat

7.4 Device Functional Modes

DLP6500 is part of the chipset comprising of the DLP6500 DMD and a DLPC900 or a DLC910 digitial controller. To ensure reliable operation, the DLP6500 must always be used with one of these digital controllers.

DMD functional modes are controlled by the digital controller. See the digital controller datasheet listed in Related Documentation. Contact a TI applications engineer for more information.

7.5 Window Characteristics and Optics

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.5.3 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

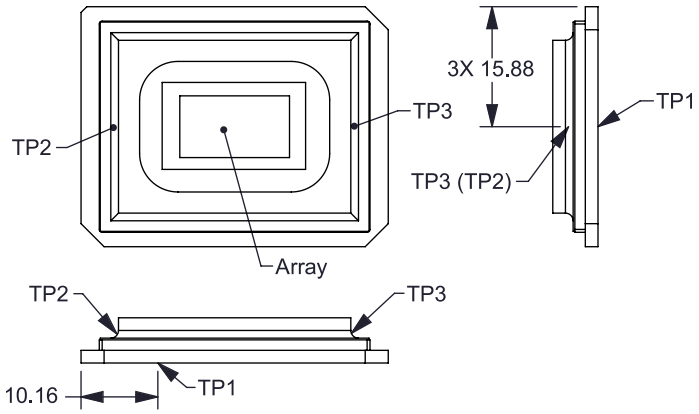


Figure 15. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (3)$$

Where:

T_{ARRAY} = Computed micromirror array temperature (°C)
$T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 15
$R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from micromirror array to outside ceramic (°C/W) specified in *Thermal Information*
Q_{ARRAY} = Total DMD power; electrical, specified in *Electrical Characteristics*, plus absorbed (calculated) (W)
$Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W), specified in *Electrical Characteristics*
C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
SL = Measured ANSI screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation to use when calculating array temperature is 2.9 Watts. Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00274 W/lm.

Sample Calculation for typical projection application:

$T_{CERAMIC}$ = 55°C, assumed system measurement; see *Recommended Operating Conditions* for specific limits
SL = 2000 lm
$Q_{ELECTRICAL}$ = 2.9 W (see the maximum power specifications in *Electrical Characteristics*)
C_{L2W} = 0.00274 W/lm
Q_{ARRAY} = 2.9 W + (0.00274 W/lm × 2000 lm) = 8.38 W
T_{ARRAY} = 55°C + (8.38 W × 0.7 × C/W) = 60.87°C

7.7 Micromirror Landed-on/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On–state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On–state 100% of the time (and in the Off–state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off–state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Individual DMD mirror duty cycles vary by application as well as the mirror location on the DMD within any specific application. DMD mirror useful life are maximized when every individual mirror within a DMD approaches 50/50 (or 1/1) duty cycle. Therefore, for the DLPC900 and DLP6500 chipset, it is recommended that DMD Idle Mode be enabled as often as possible. Examples are whenever the system is idle, the illumination is disabled, between sequential pattern exposures (if possible), or when the exposure pattern sequence is stopped for any reason. This software mode provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the on and off states. Refer to the DLPC900 Software Programmer's Guide DLPU018 for a description of the DMD Idle Mode command. For the DLPC910 and DLP6500 chipset, it is recommended the controlling applications processor provide a 50/50 pattern sequence to the DLPC910 for display on the DLP6500 as often as possible, similar to the above examples stated for the DLPC900. The pattern provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the on and off states.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a give long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Micromirror Landed-on/Landed-Off Duty Cycle (continued)

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 3.

Table 3. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle =(Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where:

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 4.

Table 4. Example Landed Duty Cycle for Full-Color

Red Cycle Percentage 50%	Green Cycle Percentage 20%	Blue Cycle Percentage 30%	Landed Duty Cycle
Red Scale Value	Green Scale Value	Blue Scale Value	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLP6500 along with a DLPC900 or a DLPC910 digital controller provide solutions for many applications including structured light and video projection. The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the digitial controller. Applications of interest include machine vision, 3D printing, and lithography.

8.2 Typical Application

A typical embedded system application using the DLPC900 digital controller and a DLP6500 is shown in Figure 16. In this configuration, the DLPC900 digital controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. This system configuration supports still and motion video sources plus sequential pattern mode. Refer to Related Documents for the DLPC900 digital controller datasheet.

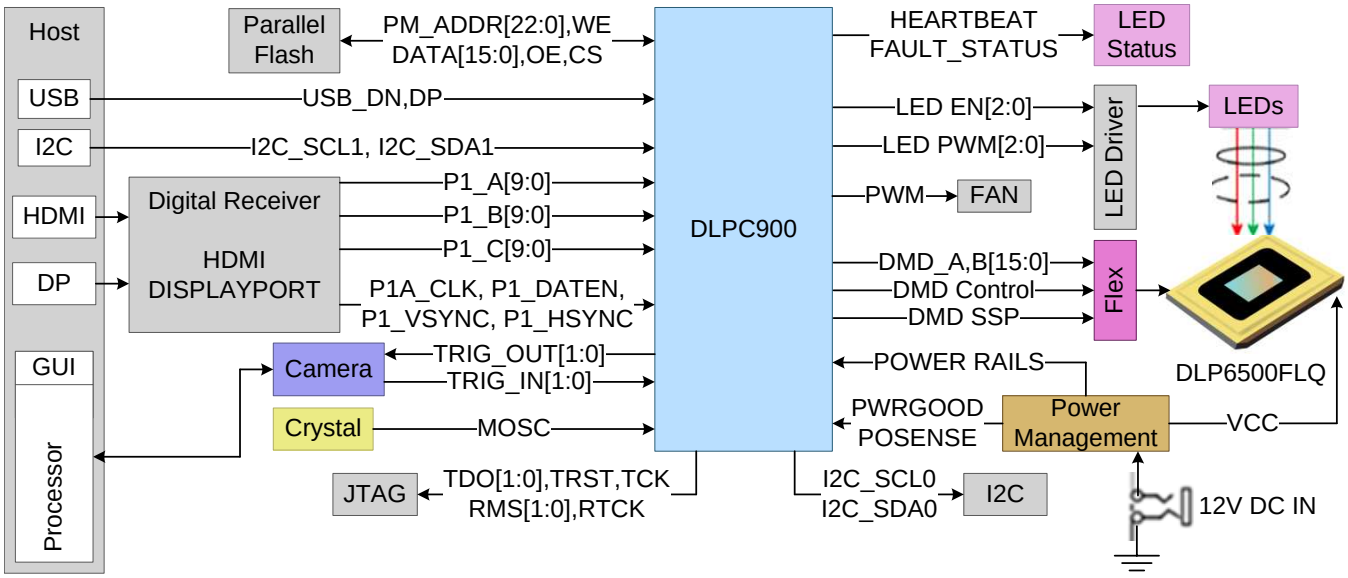


Figure 16. DLPC900 and DLP6500 Typical Application Schematic

A typical embedded system application using the DLPC910 digital controller and a DLP6500 is shown in Figure 17. In this configuration, the DLPC910 digital controller accepts streaming binary patterns from an external source or processor. This system configuration supports high speed pattern mode. Refer to Related Documents for the DLPC910 digital controller datasheet.

Typical Application (continued)

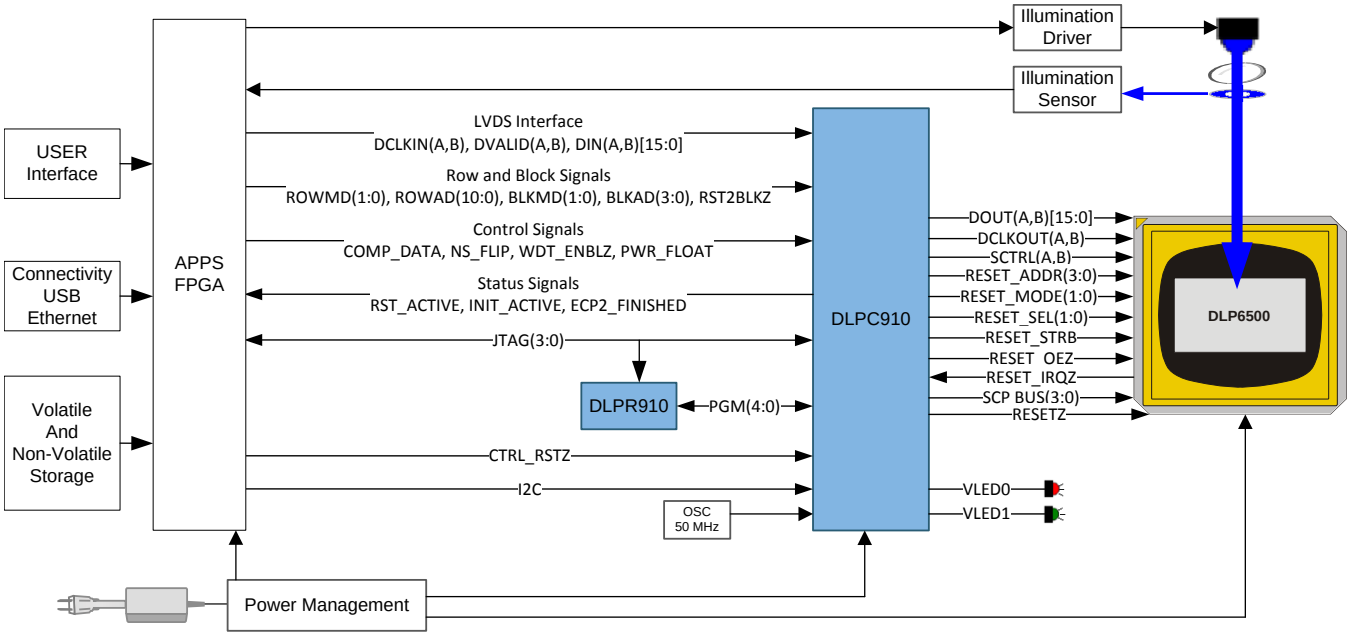


Figure 17. DLPC910 and DLP6500 Typical Application Schematic

8.2.1 Design Requirements

Detailed design requirements are located in the digital controller datasheet. Refer to Related Documents.

8.2.2 Detailed Design Procedure

See the reference design schematic for connecting together the DLPC900 controller and the DLP6500 DMD. An example board layout is included in the reference design data base. Layout guidelines should be followed for reliability.

See the reference design schematic for connecting together the DLPC910 controller and the DLP6500 DMD. An example board layout is included in the reference design data base. Layout guidelines should be followed for reliability.

9 Power Supply Requirements

9.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the digital controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VCC, VCCI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 18.

9.2 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. During power-up, VBIAS does not have to start after VOFFSET.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 18.
- During power-up, LVCMOS input pins shall not be driven high until after VCC and VCCI have settled at operating voltages listed in *Recommended Operating Conditions*.

9.3 DMD Mirror Park Sequence Requirements

9.3.1 DLPC900

For correct power down operation of the DLP6500 DMD with the DLPC900, the following power down procedure must be executed.

Prior to an anticipated power removal, the controlling applications processor must command the DLPC900 to enter Standby mode by using the Power Mode command and then wait for a minimum of 20 ms to allow the DLPC900 to complete the power down procedure. This procedure will assure the mirrors are in a flat state. Following this procedure, the power can be safely removed.

In the event of an unanticipated power loss, the power management system must detect the input power loss, command the DLPC900 to enter Standby mode by using the Power Mode command, and then maintain all operating power levels of the DLPC900 and the DLP6500 DMD for a minimum of 20 ms to allow the DLPC900 to complete the power down procedure. Following this procedure, the power can be allowed to fall below safe operating levels. Refer to the DLPC900 datasheet for more details on power down requirements.

In both anticipated power down and unanticipated power loss, the DLPC900 is commanded over the USB/I2C interface, and then the DLPC900 loades the correct power down sequence to the DMD. Communicating over the USB/I2C and loading the power down sequence accounts for most of the 20 ms. Compared to the DLPC910, the controlling processor only needs to assert the PWR_FLOAT pin and wait for a minimum of 500 µs.

The controlling applications processor can resume normal operations by commanding the DLPC900 to enter Normal mode. See Power Mode command in the DLPC900 Software Programmer's Guide DLPU018 for a description of this command.

DMD Mirror Park Sequence Requirements (continued)

9.3.2 DLPC910

For correct power down operation of the DLP6500 DMD with the DLPC910, the following power down procedure must be executed.

Prior to an anticipated power removal, assert PWR_FLOAT to the DLPC910 for a minimum of 500 μs to allow the DLPC910 to complete the power down procedure. This procedure will assure the DMD mirrors are in a flat state. Following this procedure, the power can be safely removed.

In the event of an unanticipated power loss, the power management system must detect the input power loss, assert PWR_FLOAT to the DLPC910, and maintain all operating power levels of the DLPC910 and the DLP6500 DMD for a minimum of 500 μs to allow the DLPC910 to complete the power down procedure. Refer to the DLPC910 datasheet for more details on power down requirements.

To restart after assertion of PWR_FLOAT without removing power, the DLPC910 must be reset by setting CTRL_RSTZ low (logic 0) for 50 ms, and then back to high (logic 1), or power to the DLPC910 must be cycled.

9.4 DMD Power Supply Power-Down Procedure

Refer to DMD Mirror Park Sequence Requirements for the power down procedure.

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. Refer to Table 5.
- During power-down, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 18.
- During power-down, LVCMOS input pins must be less than specified in *Recommended Operating Conditions*.

DMD Power Supply Power-Down Procedure (continued)

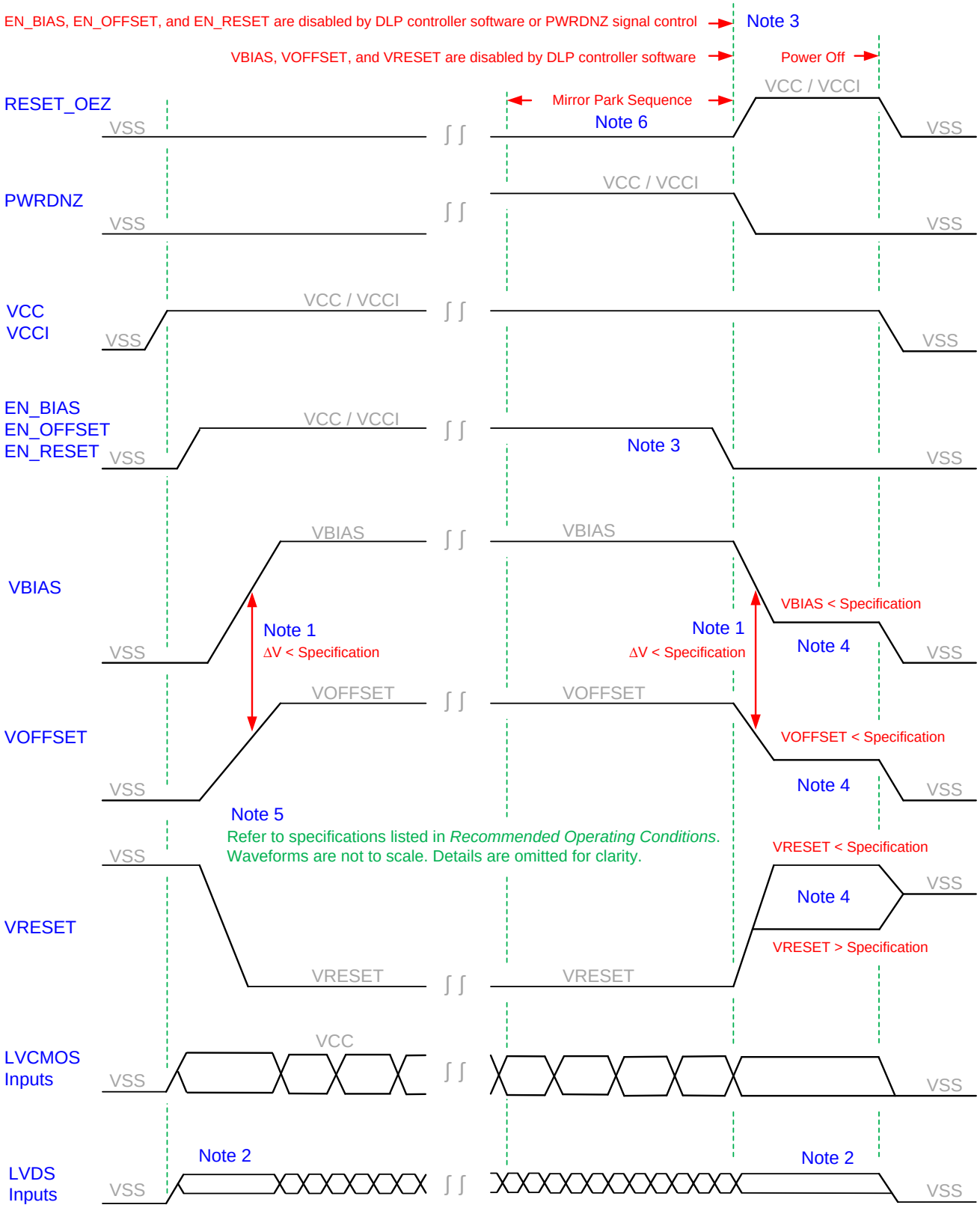


Figure 18. DMD Power Supply Sequencing Requirements

DMD Power Supply Power-Down Procedure (continued)

1. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in *Recommended Operating Conditions*. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down.
2. LVDS signals are less than the input differential voltage (VID) maximum specified in *Recommended Operating Conditions*. During power-down, LVDS signals are less than the high level input voltage (VIH) maximum specified in *Recommended Operating Conditions*.
3. When system power is interrupted, the DLP digital controller initiates a power-down sequence that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET after the micromirror park sequence. Software power-down disables VBIAS, VRESET, and VOFFSET after the micromirror park sequence through software control. For either case, enable signals EN_BIAS, EN_OFFSET, and EN_RESET are used to disable VBIAS, VOFFSET, and VRESET, respectfully.
4. Refer to DMD Power Down Sequence Requirements.
5. Figure not to scale. Details have been omitted for clarity. Refer *Recommended Operating Conditions*.
6. Refer to *DMD Mirror Park Sequence Requirements* for details on powering down the DMD.

Table 5. DMD Power-Down Sequence Requirements

PARAMETER		MIN	MAX	UNIT
VBIAS	Supply voltage level during power–down sequence		4.0	V
VOFFSET	Supply voltage level during power–down sequence		4.0	V
VRESET	Supply voltage level during power–down sequence	–4.0	0.5	V

10 Layout

10.1 Layout Guidelines

The DLP6500 along with its dedicated digital controller provides a solution for many applications including structured light and video projection. This section provides layout guidelines for the DLP6500.

10.1.1 General PCB Recommendations

The PCB shall be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, class 2. The PCB board thickness to be 0.062 inches +/- 10%, using standard FR-4 material, and applies after all lamination and plating processes, measured from copper to copper.

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity. Refer to Related Documents for the digital controller datasheet for related information on the DMD Interface Considerations.

High-speed interface waveform quality and timing on the digital controller (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors. As an example, DMD interface system timing margin can be calculated as follows:

- Setup Margin = (controller output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)
- Hold-time Margin = (controller output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

The PCB SI degradation is the signal integrity degradation due to PCB affects which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol-interference (ISI) noise.

The I/O timing parameters can be found in the digital controller datasheet. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy to determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations should be confirmed with PCB signal integrity analysis or lab measurements.

10.2 Layout Example

10.2.1 Board Stack and Impedance Requirements

Refer to Figure 19 for guidance on the parameters.

PCB design:

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0-oz copper (1.2 mil)
Flex etch thickness (T):	0.5-oz copper (0.6 mil)
Single-ended signal impedance:	50 Ω (±10%)
Differential signal impedance:	100 Ω (±10%)

Layout Example (continued)

PCB stack-up:

Reference plane 1 is assumed to be a ground plane for proper return path.	Asymmetric dual stripline
Reference plane 2 is assumed to be the I/O power plane or ground.	1.0-oz copper (1.2 mil)
Dielectric FR4, (Er):	4.2 (nominal)
Signal trace distance to reference plane 1 (H1):	5.0 mil (nominal)
Signal trace distance to reference plane 2 (H2):	34.2 mil (nominal)

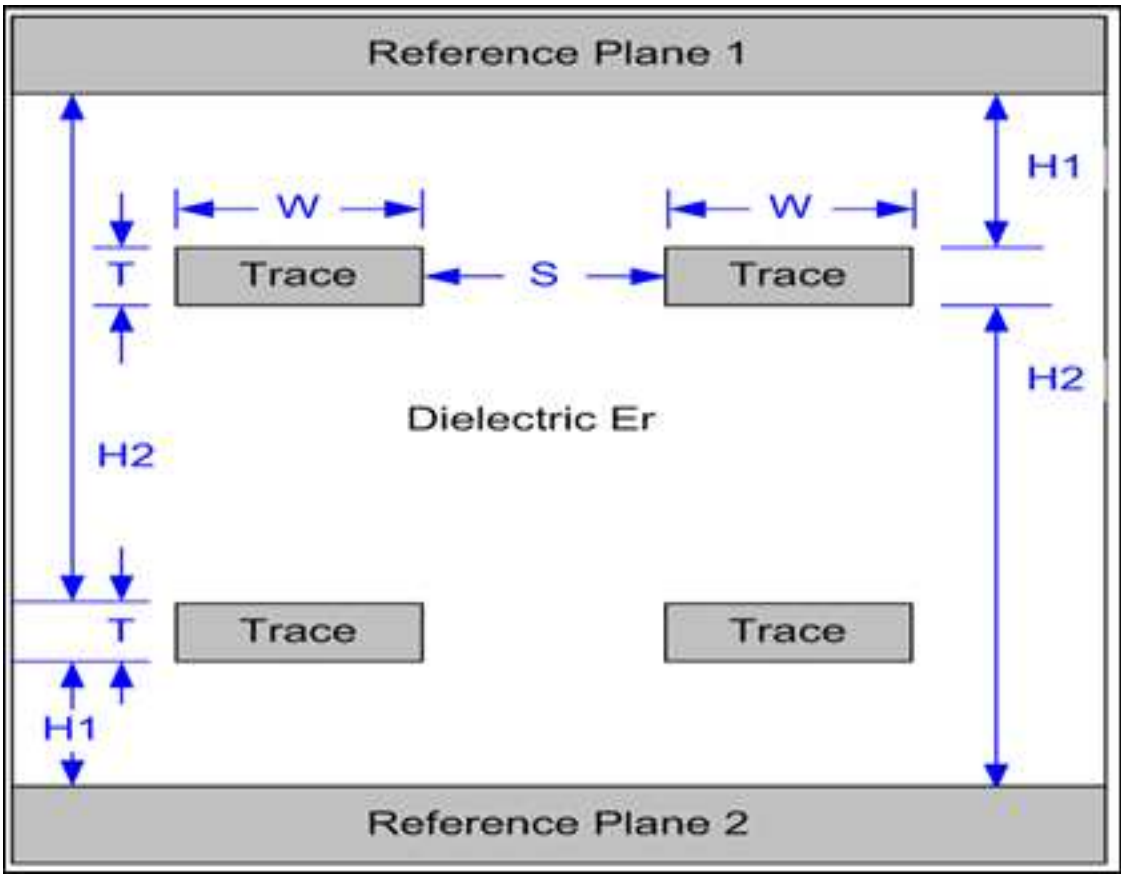


Figure 19. PCB Stack Geometries

Table 6. General PCB Routing (Applies to All Corresponding PCB Signals)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)

Layout Example (continued)

Table 6. General PCB Routing (Applies to All Corresponding PCB Signals) (continued)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75 (1) –0.15	mil (mm)
	PCB etch clocks	N/A	5.75 (1) –0.15	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
Minimum line spacing to other signals (S)	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)
Maximum differential pair P-to-N length mismatch	Total data	N/A	12 –0.3	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements

Table 7. DMD Interface Specific Routing

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (LVDS)	SCTRL_AN, SCTRL_AP D_AP(15:0), D_AN(15:0)	DCK_AP/ DCKA_AN	± 150 (± 3.81)	mil (mm)
DMD (LVDS)	SCTRL_BN, SCTRL_BP D_BP(15:0), D_BN(15:0)	DCK_BP/ DCK_BN	± 150 (± 3.81)	mil (mm)

Number of layer changes:

- Single-ended signals: Minimize
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Table 8. DMD Signal Routing Length (1)

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Max signal routing length includes escape routing.

Stubs: Stubs should be avoided.

Termination Requirements: DMD interface: None – The DMD receiver is differentially terminated to 100 Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements should be used:

- Differential crosstalk: <5%
- Differential impedance: 75 to 125 Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs should be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths. Voltage or low frequency signals should be routed on the outer layers. Signal trace corners shall be no sharper than 45 degrees. Adjacent signal layers shall have the predominant traces routed orthogonal to each other.

These guidelines will produce a maximum PCB routing mismatch of 4.41 mm (0.174 inch) or approximately 30.4 ps, assuming 175 ps/inch FR4 propagation delay.

These PCB routing guidelines will result in approximately 25-ps system setup margin and 25-ps system hold margin for the DMD interface after accounting for signal integrity degradation as well as routing mismatch.

Both the digital controller output timing parameters and the DLP6500 DMD input timing parameters include timing budget to account for their respective internal package routing skew.

10.2.1.1 Power Planes

Signal routing is NOT allowed on the power and ground planes. All device pin and via connections to this plane shall use a thermal relief with a minimum of four spokes. The power plane shall clear the edge of the PCB by 0.2”.

Prior to routing, vias connecting all digital ground layers (GND) should be placed around the edge of the rigid PWB regions 0.025” from the board edges with a 0.100” spacing. It is also desirable to have all internal digital ground (GND) planes connected together in as many places as possible. If possible, all internal ground planes should be connected together with a minimum distance between connections of 0.5”. Extra vias are not required if there are sufficient ground vias due to normal ground connections of devices. NOTE: All signal routing and signal vias should be inside the perimeter ring of ground vias.

Power and Ground pins of each component shall be connected to the power and ground planes with one via for each pin. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100”). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. Ground plane slots are NOT allowed.

Route VOFFSET, VBIAS, and VRESET as a wide trace >20mils (wider if space allows) with 20 mils spacing.

10.2.1.2 LVDS Signals

The LVDS signals shall be first. Each pair of differential signals must be routed together at a constant separation such that constant differential impedance (as in section Board Stack and Impedance Requirements) is maintained throughout the length. Avoid sharp turns and layer switching while keeping lengths to a minimum. The distance from one pair of differential signals to another shall be at least 2 times the distance within the pair.

10.2.1.3 Critical Signals

The critical signals on the board must be hand routed in the order specified below. In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long trace all around the PCB.

Table 9. Timing Critical Signals

GROUP	SIGNAL	CONSTRAINTS	ROUTING LAYERS
1	D_AP(0:15), D_AN(0:15), DCLK_AP, DCLK_AN, SCTRL_AN, SCTRL_AP, D_BP(0:15), D_BN (0:15), DCLK_BP, DCLK_BN, SCTRL_BN, SCTRL_BP	Refer to Table 6 and Table 7	Internal signal layers. Avoid layer switching when routing these signals.
2	RESET_ADDR(0:3), RESET_MODE(0:1), RESET_OEZ, RESET_SEL(0:1) RESET_STROBE, RESET_IRQZ.		Internal signal layers. Top and bottom as required.
3	SCP_CLK, SCP_DO, SCP_DI, SCP_ENZ.		Any
4	Others	No matching/length requirement	Any

10.2.1.4 Flex Connector Plating

Plate all the pad area on top layer of flex connection with a minimum of 35 and maximum 50 micro-inches of electrolytic hard gold over a minimum of 150 micro-inches of electrolytic nickel.

10.2.1.5 Device Placement

Unless otherwise specified, all major components should be placed on top layer. Small components such as ceramic, non-polarized capacitors, resistors and resistor networks can be placed on bottom layer. All high frequency de-coupling capacitors for the ICs shall be placed near the parts. Distribute the capacitors evenly around the IC and locate them as close to the device's power pins as possible (preferably with no vias). In the case where an IC has multiple de-coupling capacitors with different values, alternate the values of those that are side by side as much as possible and place the smaller value capacitor closer to the device.

10.2.1.6 Device Orientation

It is desirable to have all polarized capacitors oriented with their positive terminals in the same direction. If polarized capacitors are oriented both horizontally and vertically, then all horizontal capacitors should be oriented with the "+" terminal the same direction and likewise for the vertically oriented ones.

10.2.1.7 Fiducials

Fiducials for automatic component insertion should be placed on the board according to the following guidelines or on recommendation from manufacturer:

- Fiducials for optical auto insertion alignment shall be placed on three corners of both sides of the PWB.
- Fiducials shall also be placed in the center of the land patterns for fine pitch components (lead spacing <0.05").
- Fiducials should be 0.050 inch copper with 0.100 inch cutout (antipad).

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 10. Package Specific Information

PACKAGE TYPE	PINS	CONNECTOR
FLQ	203	LGA

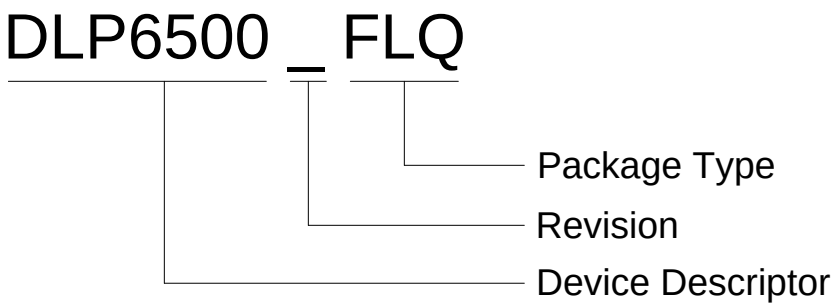


Figure 20. Part Number Description

11.1.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 21. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

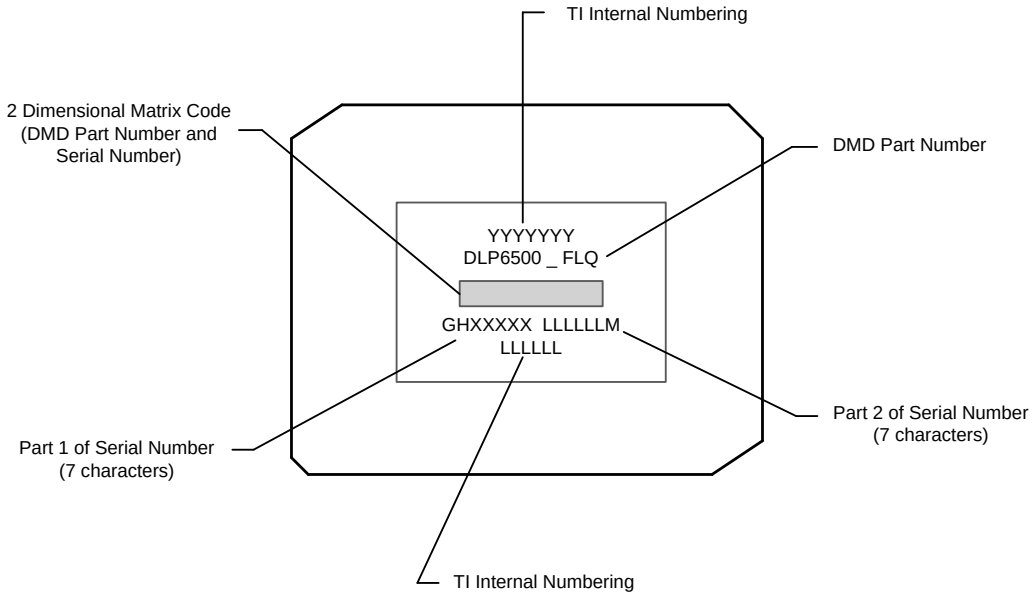


Figure 21. DMD Marking Locations

11.2 Documentation Support

11.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP6500 device.

Table 11. Related Documents

DOCUMENT	
DLPC900 Digital Controller Datasheet	DLPS037
DLPC900 Software Programmer's Guide	DLPU018
DLPC910 Digital Controller Datasheet	DLPS064
DMD101: Introduction to Digital Micromirror Device (DMD) Technology	DLPA008

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP6500BFLQ	Active	Production	CLGA (FLQ) | 203	18 | JEDEC TRAY (5+1)	Yes	NI-PD-AU	N/A for Pkg Type	0 to 65	
DLP6500BFLQ.B	Active	Production	CLGA (FLQ) | 203	18 | JEDEC TRAY (5+1)	Yes	NI-PD-AU	N/A for Pkg Type	0 to 65	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

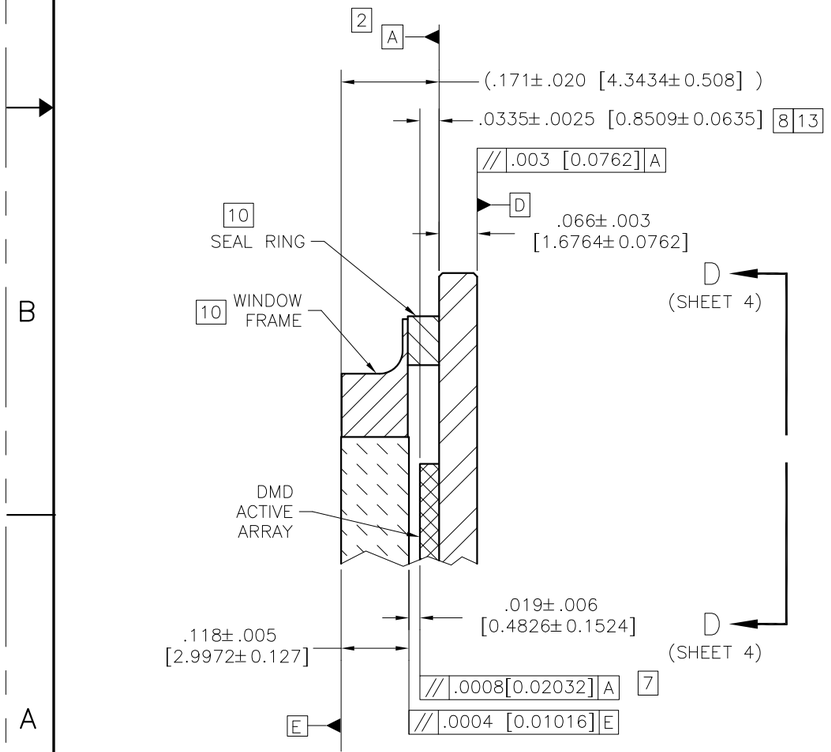
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

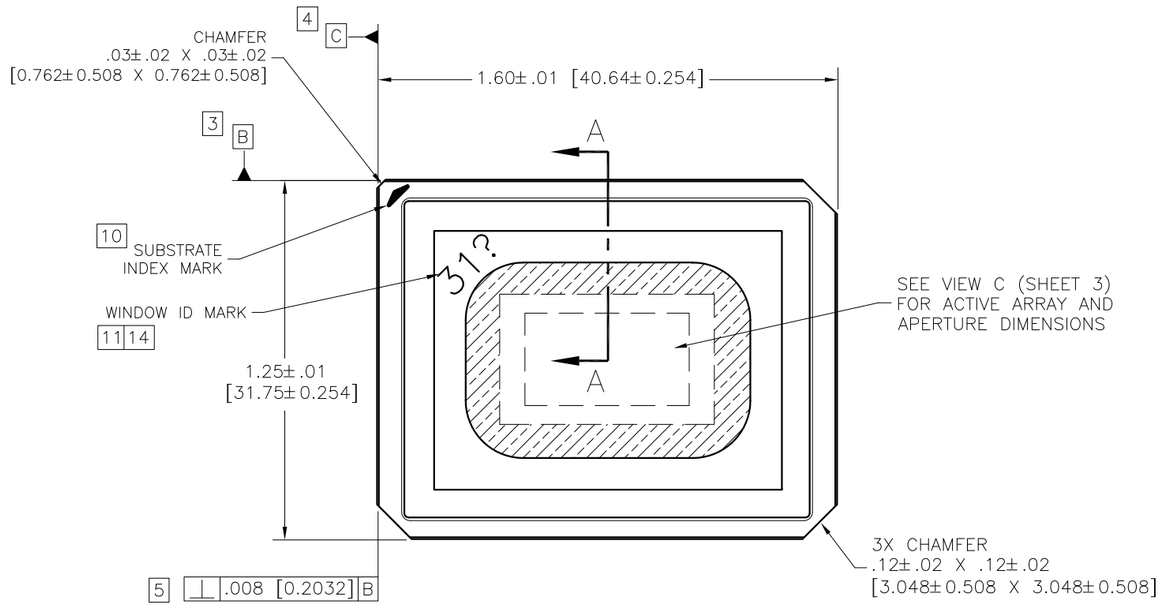
NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M–1994.
2. DATUM A (SYSTEM INTERFACE PLANE) ESTABLISHED BY THREE DATUM AREAS SHOWN IN VIEW B (SHEET 2).
3. DATUM B ESTABLISHED BY TWO DATUM AREAS SHOWN IN VIEW B (SHEET 2).
4. DATUM C ESTABLISHED BY DATUM AREA SHOWN IN VIEW B (SHEET 2).
5. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
6. LOCALIZED BACKSIDE SURFACE FLATNESS APPLIES TO ENTIRE CERAMIC SURFACE.
7. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
8. DIE HEIGHT TOLERANCE APPLIES TO CENTER OF DMD ACTIVE ARRAY ONLY.
9. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND IS THE MAXIMUM VALUE ALLOWED.
10. SUBSTRATE INDEX MARK, SYMBOLIZATION PAD, SEAL RING, AND WINDOW FRAME TO BE ELECTRICALLY CONNECTED TO VSS PLANE IN SUBSTRATE.
11. WINDOW SHALL BE ORIENTED SUCH THAT WINDOW ID MARK ALIGNS WITH SUBSTRATE INDEX MARK AS SHOWN.
12. (DELETED)
13. DMD ACTIVE ARRAY DIMENSIONS ARE RELATED TO DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY).
14. ? IS A WILD CARD CHARACTER AND CAN BE ANY LETTER.
15. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING AS SHOWN ABOVE THE SYMBOLIZATION PAD. SUBSTRATES WITH Ni/Pd/Au SHALL HAVE MARKING IN THE ALTERNATE LOCATION BELOW THE SYMBOLIZATION PAD.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2086120, INITIAL RELEASE	01/14/08	MAA
B	ECO 2086464, CHG INDEX MARK TOP	01/21/08	MAA
C	ECO 2087635, CHG GDT SYM PARALLEL FROM .001 TO .0008 IN SECTION A–A	03/03/08	MAA
D	ECO 2088011, CORRECTED PARALLELISM TYPO FROM [.0254] TO [.02032]	03/17/08	MAA
E	ECO 2150557, ADD NOTE 15, UPDATE VIEW D–D SHEET 4.	05/06/15	MAA
F	ECO 2179888, DELETE NOTE 12	02/27/19	BMH



SECTION A–A
SCALE 6/1



–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES [MILLIMETERS]
- TOLERANCES: ANGLES ± 1°
  3 PLACE DECIMALS ±.005 [0.127]
  2 PLACE DECIMALS ±.01 [0.254]
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- ~~CONCENTRICITY MACHINED DIAMETERS .010 FIM~~
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 ± .004 .001	.126 THRU .250 ± .005 .001	.251 THRU .500 ± .006 .001
.501 THRU .750 ± .008 .001	.751 THRU 1.000 ± .010 .001	1.001 THRU 2.000 ± .012 .001

THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

DWN M. AVERY	DATE 01/01/08	
ENGR M. AVERY	01/01/08	
QA P. KONRAD	01/01/08	
APVD		

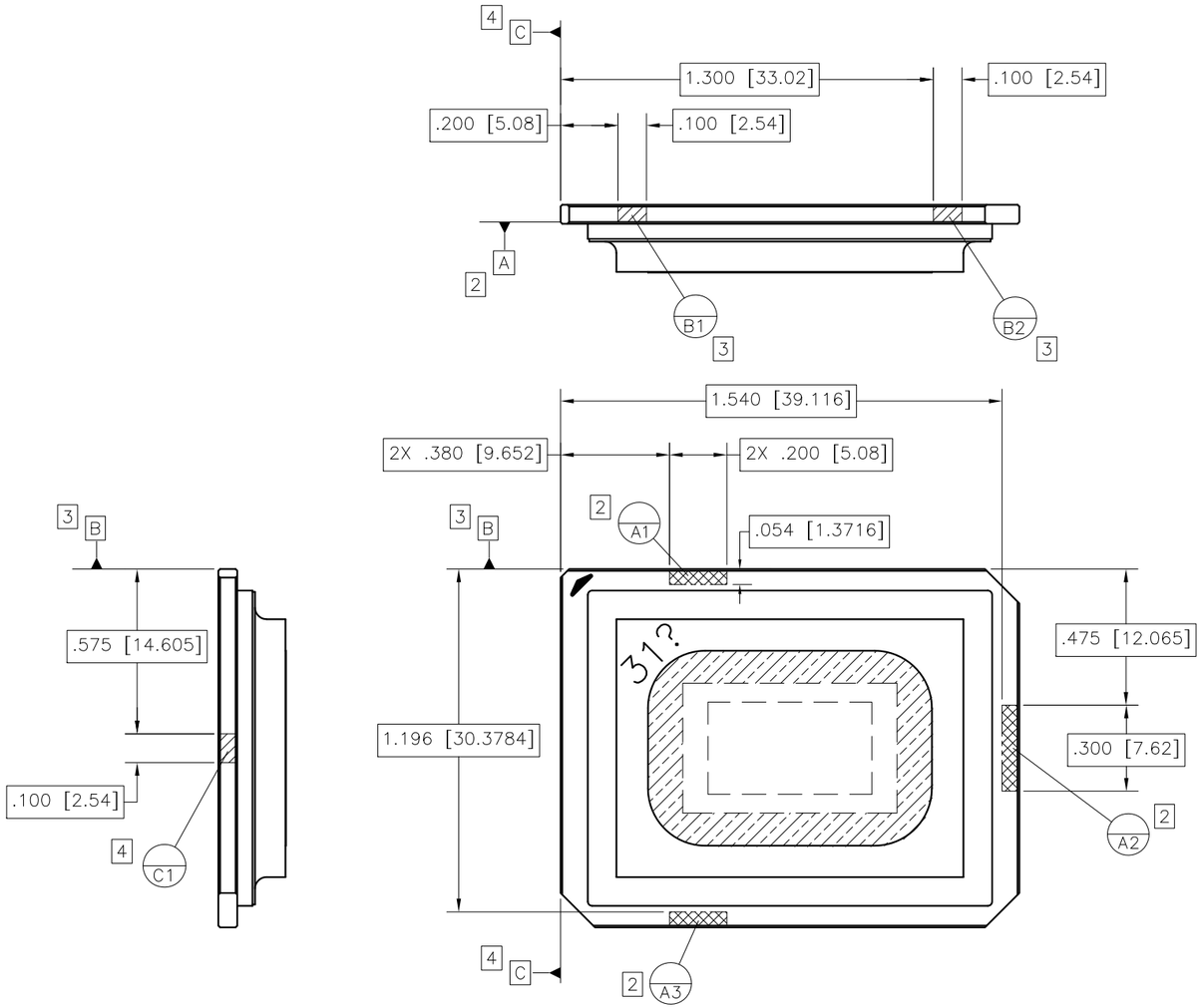
TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD
.65" 1080P TYPE A (FLQ PKG)

SIZE	DRAWING NO	REV
C	2509321	F
SCALE 3/1	SHEET 1 OF 4	

SH 1
DWG NO 2509321

ACEC1g

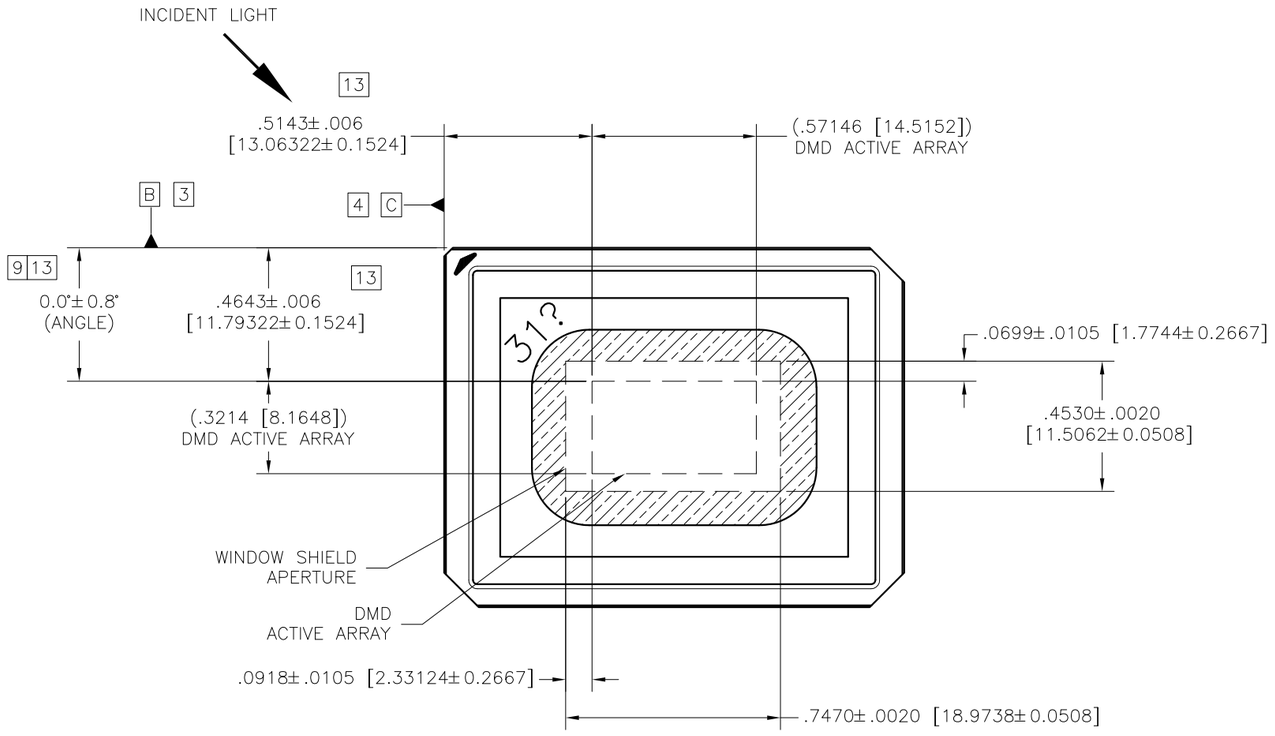


VIEW B (SHEET 1 NOTES)
DATUMS A, B, AND C

ACEC2c

Texas Instruments, Dallas, Texas	DWN DATE	SIZE C		DRAWING NO 2509321	REV F
	ISSUE DATE	SCALE 3/1		SHEET 2	

SH 2
DWG NO 2509321

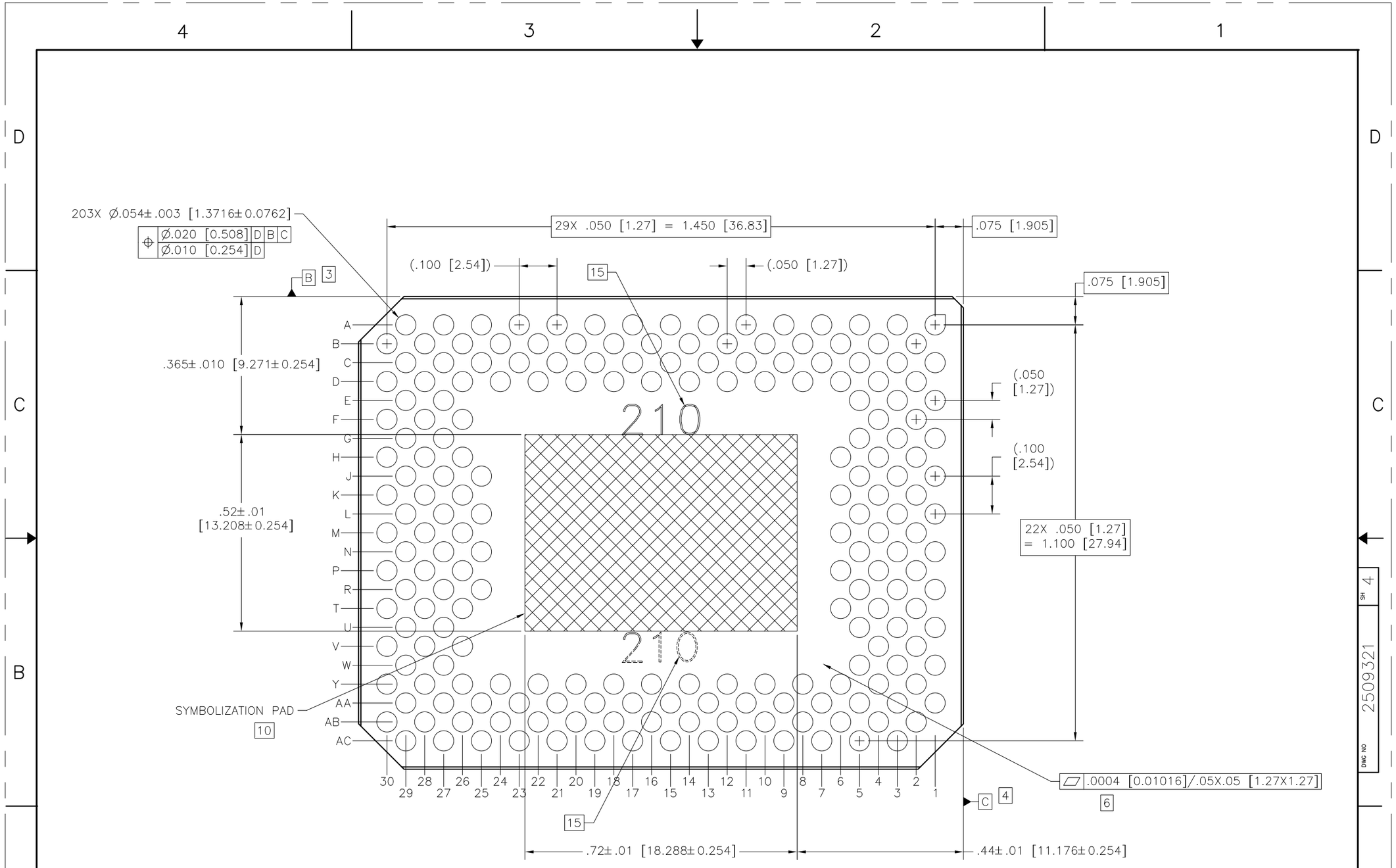


VIEW C (SHEET 1)
DMD ACTIVE ARRAY AND
WINDOW SHIELD APERTURE

SH 3
DWG NO 2509321

Texas Instruments, Dallas, Texas	DWN DATE	SIZE C		DRAWING NO 2509321	REV F
	ISSUE DATE	SCALE 3/1		SHEET 3	

ACEC2c



VIEW D–D (SHEET 1)
SCALE 6/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE	SIZE C	DRAWING NO 2509321	REV F
	ISSUE DATE	SCALE 3/1	SHEET 4	

DWG NO 2509321 SH 4

ACEC2c

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