

SBAS032A - JULY 1997 - REVISED NOVEMBER 2005

# 16-Bit DIGITAL-TO-ANALOG CONVERTER With Serial Data Interface

## **FEATURES:**

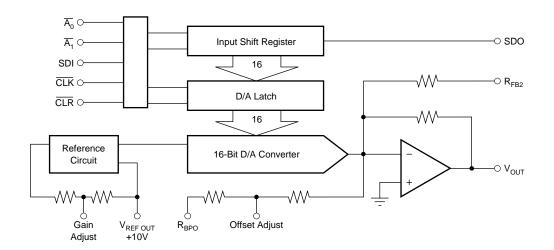
- SERIAL DIGITAL INTERFACE
- VOLTAGE OUTPUT: ±10V, ±5V, 0 to +10V
- ±1 LSB INTEGRAL LINEARITY
- 16-BIT MONOTONIC OVER TEMPERATURE
- PRECISION INTERNAL REFERENCE
- LOW NOISE: 120nV/√Hz Including Reference
- 16-LEAD PLASTIC AND CERAMIC SKINNY DIP AND PLASTIC SO PACKAGES

## DESCRIPTION

The DAC714 is a complete monolithic digital-toanalog (D/A) converter including a +10V temperature compensated reference, current-to-voltage amplifier, a high-speed synchronous serial interface, a serial output which allows cascading multiple converters, and an asynchronous clear function which immediately sets the output voltage to midscale.

The output voltage range is  $\pm 10V$ ,  $\pm 5V$ , or 0 to  $\pm 10V$  while operating from  $\pm 12V$  or  $\pm 15V$  supplies. The gain and bipolar offset adjustments are designed so that they can be set via external potentiometers or external D/A converters. The output amplifier is protected against short circuit to ground.

The 16-pin DAC714 is available in a plastic 0.3" DIP, ceramic 0.3" CERDIP, and wide-body plastic SO package. The DAC714P, U, HB, and HC are specified over the -40°C to +85°C temperature range while the DAC714HL is specified over the 0°C to +70°C range.





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## ABSOLUTE MAXIMUM RATINGS(1)

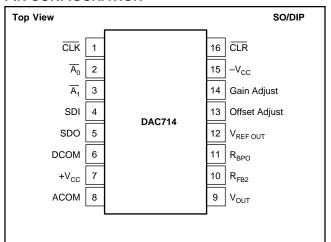
+V <sub>CC</sub> to Common 0V to +1	7V
−V <sub>CC</sub> to Common	7V
+V <sub>CC</sub> to -V <sub>CC</sub>	34V
ACOM to DCOM±0.	.5V
Digital Inputs to Common	7V)
External Voltage Applied to BPO and Range Resistors ±\	$I_{CC}$
V <sub>REF OUT</sub> Indefinite Short to Comm	non
V <sub>OUT</sub> Indefinite Short to Comm	non
SDO Indefinite Short to Comm	non
Power Dissipation	nW
Storage Temperature60°C to +150	)°C
Lead Temperature (soldering, 10s)+300	)°C

NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## **PACKAGE/ORDERING INFORMATION**

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## **PIN CONFIGURATION**





## **ELECTROSTATIC DISCHARGE SENSITIVITY**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	CLK	Serial Data Clock
2	$\overline{A_0}$	Enable for Input Register (Active Low)
3	$\overline{A_1}$	Enable for D/A Latch (Active Low)
4	SDI	Serial Data Input
5	SDO	Serial Data Output
6	DCOM	Digital Ground
7	+V <sub>CC</sub>	Positive Power Supply
8	ACOM	Analog Ground
9	V <sub>OUT</sub>	D/A Output
10	R <sub>FB2</sub>	±10V Range Feedback Output
11	$R_{BPO}$	Bipolar Offset
12	V <sub>REF OUT</sub>	Voltage Reference Output
13	Offset Adjust	Offset Adjust
14	Gain Adjust	Gain Adjust
15	-V <sub>CC</sub>	Negative Power Supply
16	CLR	Clear

## **ELECTRICAL CHARACTERISTICS**

At  $T_A$  = +25°C, +V<sub>CC</sub> = +12V and +15V, -V<sub>CC</sub> = -12V, and -15V, unless otherwise noted.

		DAC714P,	J		DAC714HE	3		DAC714HC	;		DAC714HL	-	
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error			±4			±2			±1			±1	LSB
T <sub>MIN</sub> to T <sub>MAX</sub>			±8			±4			±2			±2	LSB
Differential Linearity Error			±4			±2			±1			±1	LSB
$T_{MIN}$ to $T_{MAX}$	l		±8	l		±4			±2	l		±1	LSB
Monotonicity	14			15			16			16			Bits
Monotonicity Over Spec Temp Range Gain Error <sup>(3)</sup>	13		±0.1	14		±0.1	15		±0.1	16		<b>⊥0.1</b>	Bits %
T <sub>MIN</sub> to T <sub>MAX</sub>			±0.1 ±0.25			±0.1 ±0.25			±0.1 ±0.25			±0.1 ±0.25	% %
Unipolar/Bipolar Zero Error <sup>(3)</sup>			±0.23			±0.23			±0.23			±0.23	% of FSR <sup>(2)</sup>
T <sub>MIN</sub> to T <sub>MAX</sub>			±0.2			±0.2			±0.2			±0.2	% of FSR
Power Supply Sensitivity of Gain			±0.003			±0.003			±0.003			±0.003	%FSR/%V <sub>CC</sub>
			±30			±30			±30			±30	ppm FSR/%V <sub>CC</sub>
DYNAMIC PERFORMANCE													
Settling Time (to $\pm 0.003\%$ FSR, $5k\Omega \parallel 500$ pF Load) <sup>(4)</sup>													
20V Output Step		6	10		6	10		6	10		6	10	μs
1LSB Output Step <sup>(5)</sup>		4	10		4	10		4	'0		4	10	μS
Output Slew Rate		10			10			10			10		V/μs
Total Harmonic Distortion													
0dB, 1001Hz, $f_S = 100kHz$		0.005			0.005			0.005			0.005		%
$-20$ dB, 1001Hz, $f_S = 100$ kHz		0.03			0.03			0.03			0.03		%
$-60$ dB, $100$ 1Hz, $f_S = 100$ kHz		3.0			3.0			3.0			3.0		%
SINAD: 1001Hz, f <sub>S</sub> = 100kHz		87			87			87			87		dB
Digital Feedthrough <sup>(5)</sup> Digital-to-Analog Glitch Impulse <sup>(5)</sup>		2 15			2 15			2 15			2 15		nV–s nV–s
Output Noise Voltage (includes reference)		120			120			120			120		nV/√Hz
ANALOG OUTPUT		1.20			1.20			.20			120		,
Output Voltage Range													
$+V_{CC}$ , $-V_{CC} = \pm 11.4V$	±10			±10			±10			±10			V
Output Current	±5			±5			±5			±5			mA
Output Impedance		0.1			0.1			0.1			0.1		Ω
Short Circuit to ACOM Duration		Indefinite			Indefinite			Indefinite			Indefinite		
REFERENCE VOLTAGE	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	٧
Voltage T <sub>MIN</sub> to T <sub>MAX</sub>	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	V
Output Resistance	+3.300	1	+10.040	+3.300	1	+10.040	+3.300	1	10.040	+3.300	1	+10.040	Ω
Source Current	2			2			2	i i		2			mA
Short Circuit to ACOM Duration		Indefinite			Indefinite			Indefinite			Indefinite		
INTERFACE													
RESOLUTION		16			16			16			16		Bits
DIGITAL INPUTS Serial Data Input Code													
Logic Levels <sup>(1)</sup>		l	l	l	l Ri	l inary Two's	Compleme	 nt	l	l	I	ļ	
V <sub>IH</sub>	+2.0	I	(V <sub>CC</sub> -1.4)	+2.0		(V <sub>CC</sub> –1.4)			(V <sub>CC</sub> -1.4)	+2.0	I	(V <sub>CC</sub> -1.4)	V
V <sub>IL</sub>	0		+0.8	0		+0.8	0		+0.8	0		+0.8	V
	"		±10	ľ		±10	"		±10	ľ		±10	μA
$I_{IH} (V_I = +2.7V)$			±10										· ·
I <sub>IL</sub> (V <sub>I</sub> = +0.4V)  DIGITAL OUTPUT			±10			±10			±10			±10	μА
Serial Data													
V <sub>OL</sub> (I <sub>SINK</sub> = 1.6mA)	0		+0.4	0		+0.4	0		+0.4	0		+0.4	V
$V_{OH}$ ( $I_{SOURCE} = 500\mu A$ ), $T_{MIN}$ to $T_{MAX}$	+2.4		+5	+2.4		+5	+2.4		+5	+2.4		+5	V
POWER SUPPLY REQUIREMENTS				1									
Voltage				1						1			
+V <sub>CC</sub>	+11.4	+15	+16.5	+11.4	+15	+16.5	+11.4	+15	+16.5	+11.4	+15	+16.5	V
-V <sub>CC</sub>	-11.4	-15	-16.5	-11.4	-15	-16.5	-11.4	-15	-16.5	-11.4	-15	-16.5	V
Current (No Load, ±15V Supplies) <sup>(6)</sup>		4.2	,_		4.5	4.5		1	4.0		,_	4.5	
+V <sub>CC</sub>		13	16		13	16		13	16		13	16	mA
-V <sub>CC</sub> Power Dissipation <sup>(7)</sup>		22	26 625		22	26 625		22	26 625		22	26 625	mA mW
TEMPERATURE RANGES			525			020			020			020	11/44
Specification			]										
All Grades	-40		+85	-40		+85	-40		+85	0		+70	°C
Storage	-60		+150	-60		+150	-60		+150	-60		+150	°C
Thermal Coefficient, $\theta_{JA}$		75		1	75			75			75		°C/W

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for  $\pm 10V$  output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the  $3\sigma$  limit. Not 100% tested for this parameter. (5) For the worst-case Binary Two's Complement code changes: FFFF<sub>H</sub> to  $0000_H$  and  $0000_H$  to FFFF<sub>H</sub>. (6) During power supply turn on, the transient supply current may approach  $3x_{\underline{t}}$  he maximum quiescent specification. (7) Typical (i.e. rated) supply voltages times maximum currents.

TEXAS INSTRUMENTS

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## **TIMING SPECIFICATIONS**

 $T_A = -40^{\circ}\text{C}$  to +85°C, + $V_{CC} = +12\text{V}$  or +15V, - $V_{CC} = -12\text{V}$  or -15V.

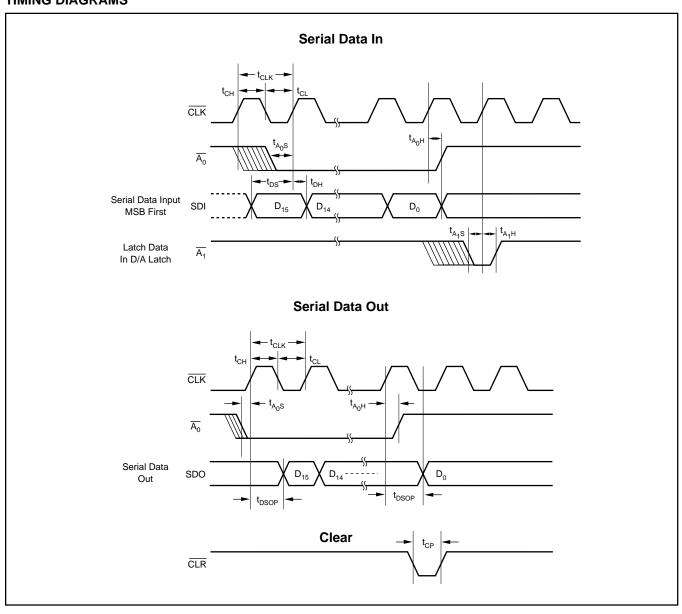
	10 +83 C, +V <sub>CC</sub> = +12 V OI +13 V, -V			
SYMBOL	PARAMETER	MIN	MAX	UNITS
t <sub>CLK</sub>	Data Clock Period	100		ns
t <sub>CL</sub>	Clock LOW	50		ns
t <sub>CH</sub>	Clock HIGH	50		ns
t <sub>AOS</sub>	Setup Time for $\overline{A_0}$	50		ns
t <sub>A1S</sub>	Setup Time for $\overline{A_1}$	50		ns
t <sub>AOH</sub>	Hold Time for $\overline{A_0}$	0		ns
t <sub>A1H</sub>	Hold Time for $\overline{A_1}$	0		ns
t <sub>DS</sub>	Setup Time for DATA	50		ns
t <sub>DH</sub>	Hold Time for DATA	10		ns
t <sub>DSOP</sub>	Output Propagation Delay		140	ns
t <sub>CP</sub>	Clear Pulsewidth	200		ns

## **TRUTH TABLE**

$\overline{A_0}$	$\overline{\mathbf{A}_{1}}$	CLK	CLR	DESCRIPTION
0	1	$1 \rightarrow 0 \rightarrow 1$	1	Shift Serial Data into SDI
1	0	$1 \to 0 \to 1$	1	Load D/A Latch
1	1	$1 \rightarrow 0 \rightarrow 1$	1	No Change
0	0	$1 \rightarrow 0 \rightarrow 1$	1	Two Wire Operation <sup>(1)</sup>
Х	Х	1	1	No Change
Х	Х	Х	0	Reset D/A Latch
NOTES	: X = Dor	n't Care. (1) All	digital inpu	t changes will appear at the

NOTES: X = Don't Care. (1) All digital input changes will appear at the output.

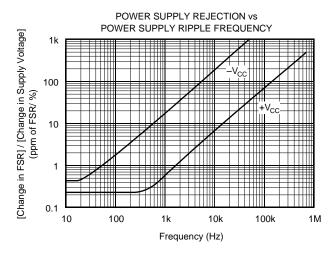
## **TIMING DIAGRAMS**

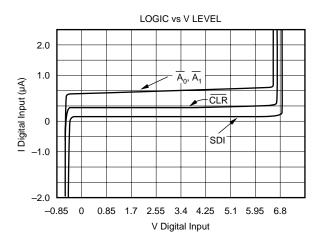


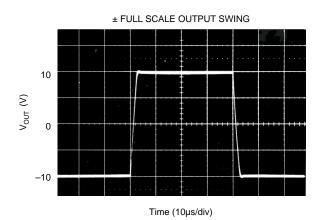


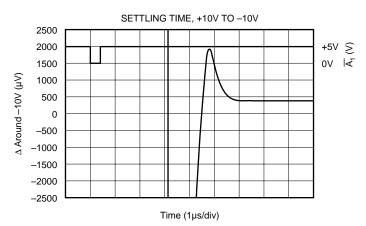
## TYPICAL CHARACTERISTICS

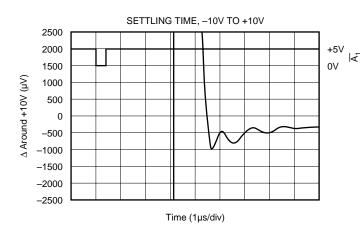
At  $T_A$  = +25°C,  $V_{CC}$  = ±15V, unless otherwise noted.

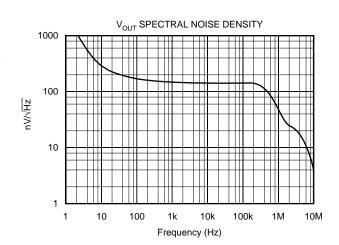












## DISCUSSION OF SPECIFICATIONS

#### LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

#### **DIFFERENTIAL LINEARITY ERROR**

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of  $\pm 1/2$ LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than -1LSB, the D/A is said to be monotonic.

## MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of the C and L grades is assured over the specification temperature range to 16 bits.

## **SETTLING TIME**

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within  $\pm 0.003\%$  of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry (FFFFH to  $0000_H$ , and  $0000_H$  to FFFFH: BTC codes), the input transition at which worst-case settling time occurs.

## **TOTAL HARMONIC DISTORTION**

Total harmonic distortion is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate  $f_S$ .

## SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate,  $f_s$ .

## **DIGITAL-TO-ANALOG GLITCH IMPULSE**

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from  $0000_{\rm H}$  to FFFF<sub>H</sub>.

## **DIGITAL FEEDTHROUGH**

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

## **OPERATION**

The DAC714 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and a serial interface.

## **INTERFACE LOGIC**

The DAC714 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to the block diagram shown in Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic "0" will enter the latch. When the enable inputs return to logic "1", the data is latched.

The  $\overline{CLR}$  input resets both the input latch and the D/A latch to  $0000_H$  (midscale).

## LOGIC INPUT COMPATIBILITY

The DAC714 digital inputs are TTL compatible (1.4V switching level), low leakage, and high impedance. Thus, the inputs are suitable for being driven by any type of 5V logic family, such as CMOS. An equivalent circuit for the digital inputs is shown in Figure 2.

The inputs will float to logic "0" if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

## **INPUT CODING**

The DAC714 is designed to accept binary two's complement (BTC) input codes with the MSB first which are compatible with bipolar analog output operation. For this configuration, a digital input of  $7FFF_H$  produces a plus full scale output,  $8000_H$  produces a minus full scale output, and  $0000_H$  produces bipolar zero output.

#### INTERNAL REFERENCE

The DAC714 contains a +10V reference. The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant; otherwise, the gain and bipolar offset of the converter will vary.



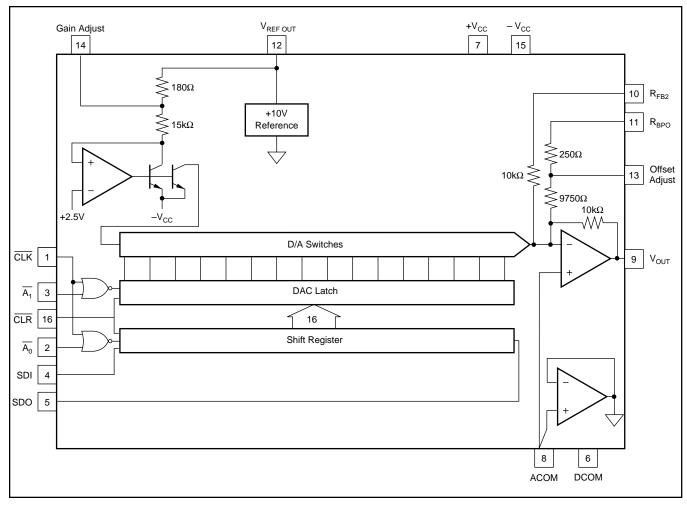


FIGURE 1. DAC714 Block Diagram.

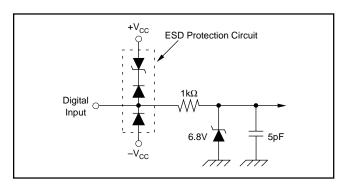


FIGURE 2. Equivalent Circuit of Digital Inputs.

## **OUTPUT VOLTAGE SWING**

The output amplifier of the DAC714 is designed to achieve a  $\pm 10V$  output range while operating on  $\pm 11.4V$  or higher power supplies.

## **GAIN AND OFFSET ADJUSTMENTS**

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of  $\pm 0.3\%$ .

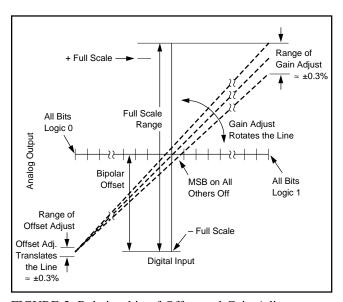


FIGURE 3. Relationship of Offset and Gain Adjustments.

## **Offset Adjustment**

Apply the digital input code,  $8000_H$ , that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for -10V (or 0V unipolar).





DAC	DAC714 CALIBRATION VALUES										
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG O BIPOLAR 20V RANGE	UTPUT (V) UNIPOLAR 10V RANGE	DESCRIPTION								
7FFF <sub>H</sub>	+9.999695	+9.999847	+ Full Scale -1LSB								
4000 <sub>H</sub>	+5.000000	+7.500000	3/4 Scale								
0001 <sub>H</sub>	+0.000305	+5.000153	BPZ + 1LSB								
0000 <sub>H</sub>	0.000000	+5.000000	Bipolar Zero (BPZ)								
FFFF <sub>H</sub>	-0.000305	+4.999847	BPZ – 1LSB								
C000 <sub>H</sub>	-5.000000	+2.500000	1/4 Scale								
8000 <sub>H</sub>	-10.00000	0.000000	Minus Full Scale								

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

## **Gain Adjustment**

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

## **INSTALLATION**

#### **GENERAL CONSIDERATIONS**

Due to the high accuracy of the DAC714 system design, problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305 $\mu$ V. With a load current of 5mA, series wiring and connector resistance of only 60m $\Omega$  will cause a voltage drop of 300 $\mu$ V. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 m $\Omega$  per square. For a 5mA load, a 10 milliinch wide printed circuit conductor 60 milliinches long will result in a voltage drop of 150 $\mu$ V.

The analog output of DAC714 has an LSB size of  $305\mu V$  (-96dB) in the bipolar mode. The rms noise floor of the D/A should remain below this level in the frequency range of interest. The DAC714's output noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Characteristic section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

## POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to  $10\mu F$  tantalum capacitor at  $-V_{CC}$ . Applications with less

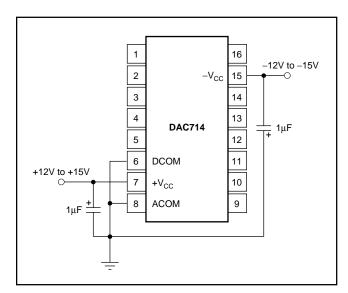


FIGURE 4. Power Supply Connections.

critical settling time may be able to use  $0.01\mu F$  at  $-V_{CC}$  as well as at  $+V_{CC}.$  The capacitors should be located close to the package.

The DAC714 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC714s are used or if DAC714 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

## LOAD CONNECTIONS

Since the reference point for  $V_{OUT}$  and  $V_{REF\ OUT}$  is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by  $R_1$  through  $R_3$ . As long as the load resistance  $R_L$  is constant,  $R_1$  simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration.  $R_2$  is part of  $R_L$  if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because there is no change in DAC714 ACOM current, provided that R<sub>3</sub> is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.



## **GAIN AND OFFSET ADJUST**

## **Connections Using Potentiometers**

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least  $\pm 0.3\%$  of Full Scale Range. Refer to Figure 6.

## **Using D/A Converters**

The GAIN ADJUST and OFFSET ADJUST circuits of the DAC714 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of  $30\mu V$  to  $50\mu V$  per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, +5V.

#### **OUTPUT VOLTAGE RANGE CONNECTIONS**

The DAC714 output amplifier is connected internally to provide a 20V output range. For other ranges and configurations, see Figures 6 and 7.

## **DIGITAL INTERFACE**

## SERIAL INTERFACE

The DAC714 has a serial interface with two data buffers which can be used for either synchronous or asynchronous updating of multiple D/A converters.  $\overline{A0}$  is the enable control for the input shift register.  $\overline{A1}$  is the enable for the D/A Latch.  $\overline{CLK}$  is used to strobe data into the latches enabled by  $\overline{A0}$  and  $\overline{A1}$ . A  $\overline{CLR}$  function is also provided and when enabled it sets the shift register and the D/A Latch to  $0000_H$  (output voltage is midscale).

Multiple DAC714s can be connected to the same  $\overline{\text{CLK}}$  and data lines in two ways. The output of the serial shift register is available as SDO so that any number of DAC714s can be cascaded on the same input bit stream as shown in Figures 8 and 9. This configuration allows all D/A converters to be updated simultaneously and requires a minimum number of control signals. These configurations do require 16N  $\overline{\text{CLK}}$  cycles to load any given D/A converter, where N is the number of D/A converters.

The DAC714 can also be connected in parallel as shown in Figure 10. This configuration allows any D/A converter in the system to be updated in a maximum of 16 CLK cycles.

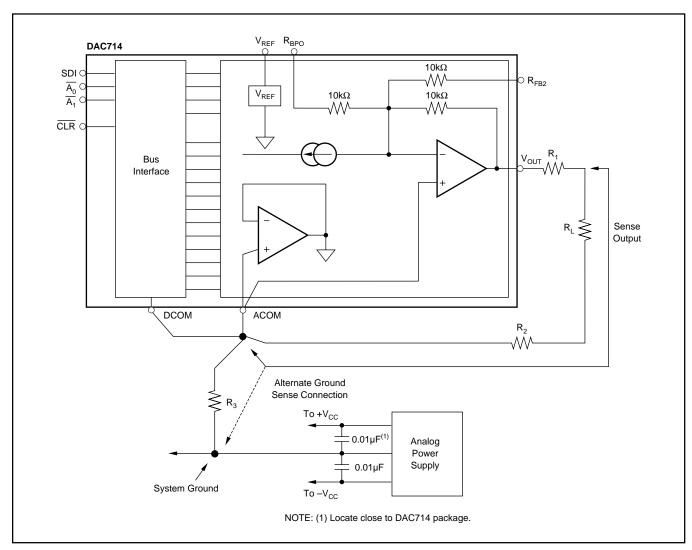


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.



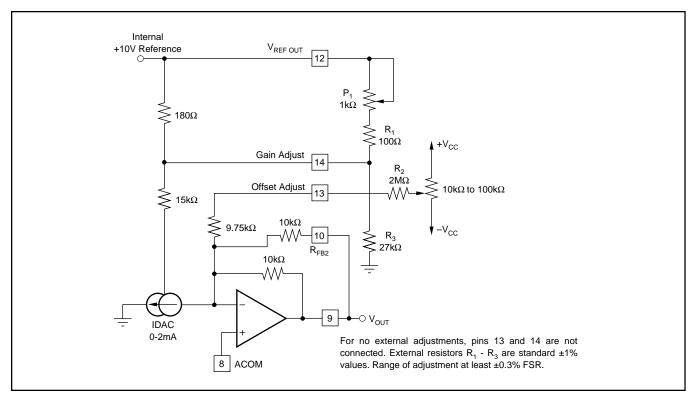


FIGURE 6a. Manual Offset and Gain Adjust Circuits; Unipolar Mode (0V to +10V output range).

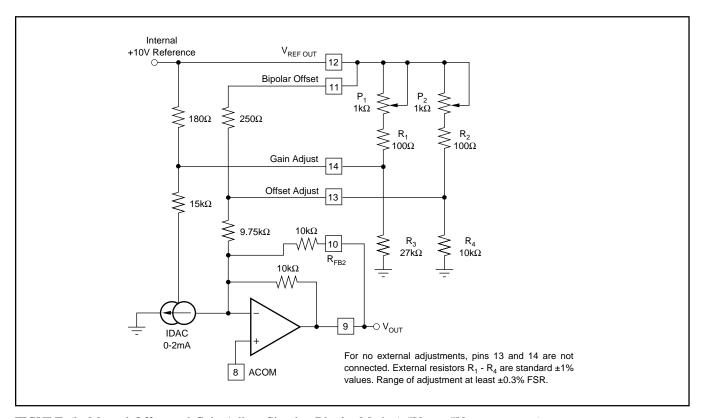


FIGURE 6b. Manual Offset and Gain Adjust Circuits; Bipolar Mode (-5V to +5V output range).

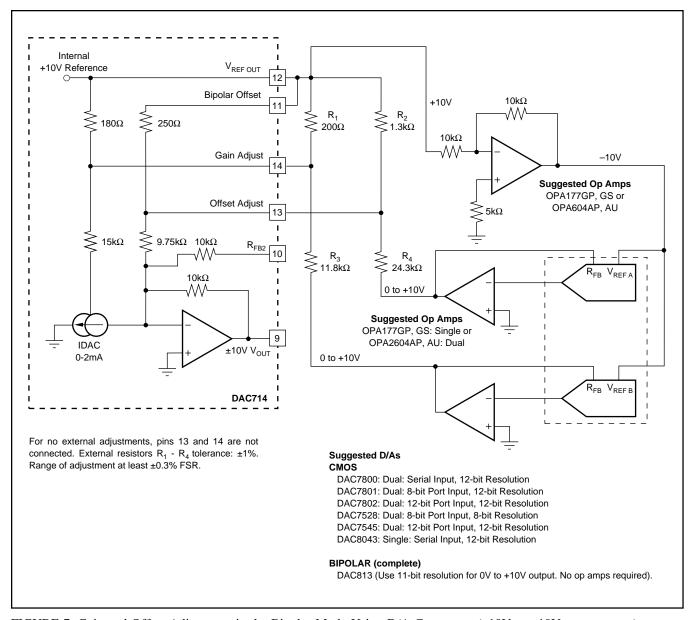


FIGURE 7. Gain and Offset Adjustment in the Bipolar Mode Using D/A Converters (-10V to +10V output range).



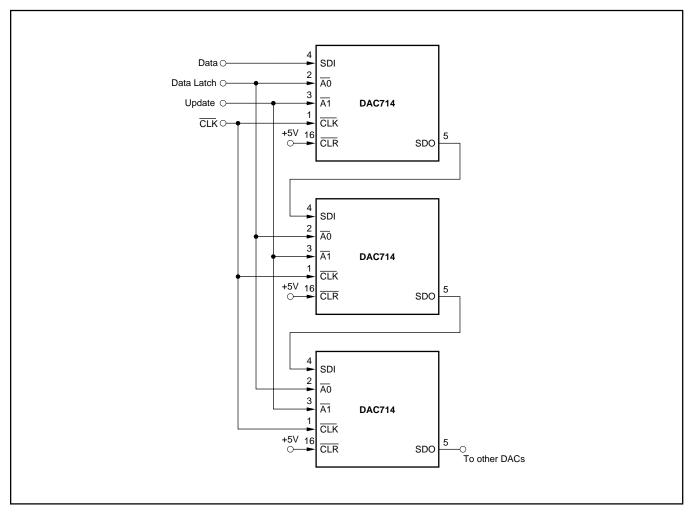


FIGURE 8a. Cascaded Serial Bus Connection with Synchronous Update.

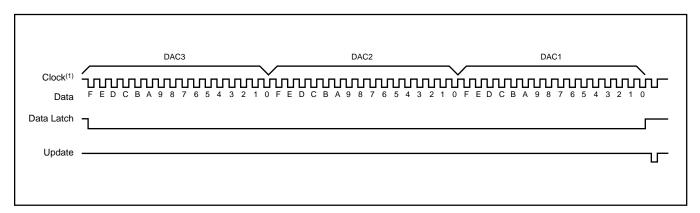


FIGURE 8b. Timing Diagram For Figure 8a.

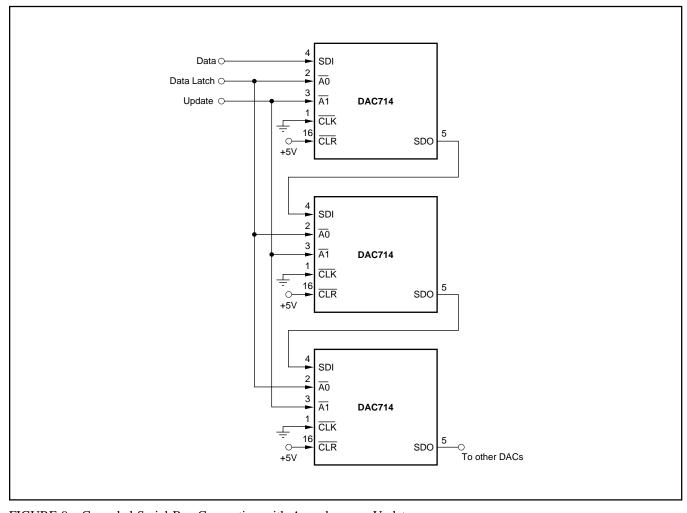


FIGURE 9a. Cascaded Serial Bus Connection with Asynchronous Update.

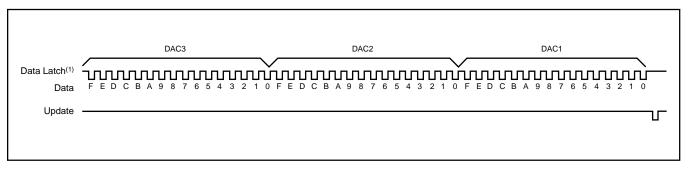


FIGURE 9b. Timing Diagram For Figure 9a.



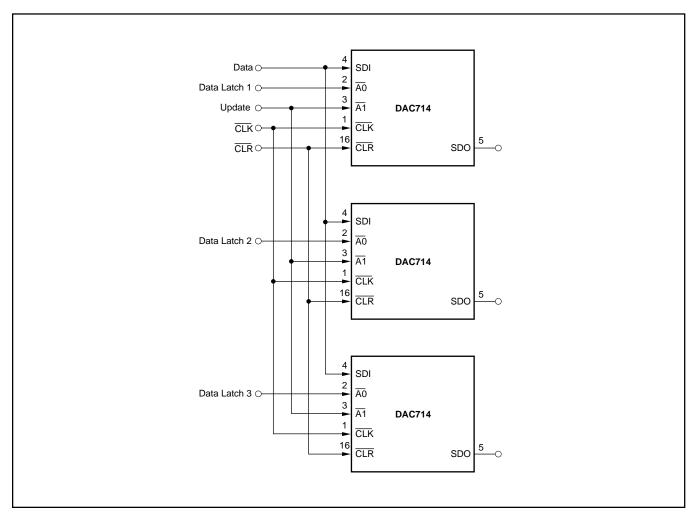


FIGURE 10a. Parallel Bus Connection.

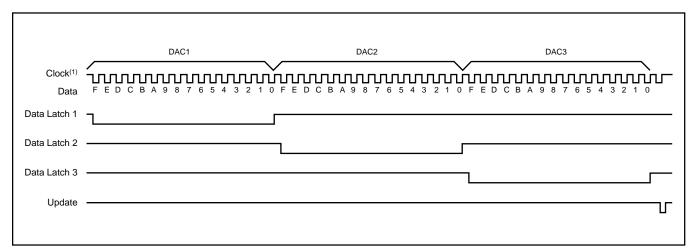


FIGURE 10b. Timing Diagram For Figure 10a.

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## PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
DAC714P	NRND	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DAC714P
DAC714P.A	NRND	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DAC714P
DAC714U	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC714U
DAC714U.A	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC714U
DAC714U/1K	Active	Production	SOIC (DW)   16	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC714U
DAC714U/1K.A	Active	Production	SOIC (DW)   16	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC714U
DAC714U/1KG4	Active	Production	SOIC (DW)   16	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC714U

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

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## **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC714U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

## **PACKAGE MATERIALS INFORMATION**

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## \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	DAC714U/1K	SOIC	DW	16	1000	353.0	353.0	32.0	

## **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC714P	N	PDIP	16	25	506	13.97	11230	4.32
DAC714P.A	N	PDIP	16	25	506	13.97	11230	4.32
DAC714U	DW	SOIC	16	40	507	12.83	5080	6.6
DAC714U.A	DW	SOIC	16	40	507	12.83	5080	6.6

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





SOIC



## NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- 5. Reference JEDEC registration MS-013.



SOIC



## NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



## NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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