DAC539E4W 10-Bit Smart DAC for LUT-Based Standalone Fault-Management With Auto-Detected I²C or SPI

1 Features

- Quad comparator inputs
- 10-bit independent comparator thresholds
  - 1 LSB DNL
  - Gains of 1 ×, 1.5 ×, 2 ×, 3 ×, and 4 ×
- Quad general-purpose output (GPO)
- Look-up table (LUT) based comparator-to-GPO mapping
- Automatically detected SPI and I²C interface
  - 1.62V V_{IH} with V_{DD} = 5.5V
- MODE pin to select between programming and standalone modes
- User-programmable nonvolatile memory (NVM)
- Reference: internal, external, VDD
- Wide operating range
  - Power supply: 1.8V to 5.5V
  - Temperature: –40˚C to +125˚C
- Tiny package:
  - 16-pin DSBGA: 1.76mm × 1.76mm, nominal

2 Applications

- Cordless power tool
- Vacuum robot
- Air purifier and humidifier

3 Description

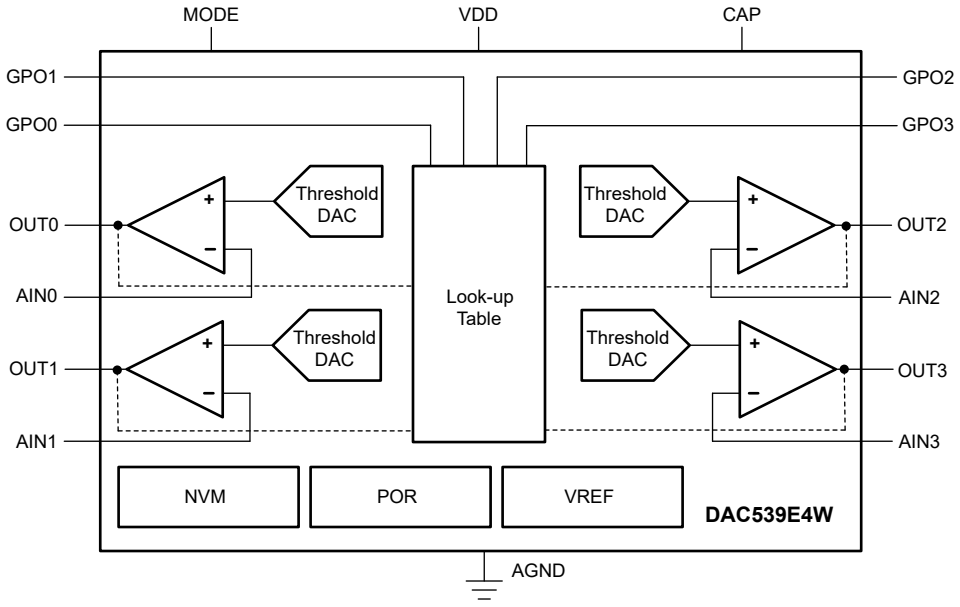
The DAC539E4W is 10-bit smart digital-to-analog converters (DACs) with quad programmable comparator inputs and quad general-purpose outputs. A look-up table maps the comparator inputs to the GPOs. The DAC539E4W also supports a programmable delay to allow the input transitions to settle. These devices provide NVM for storing the configurations. This smart DAC functions without the need for a processor (*processor-less* operation) using LUT and NVM.

This device has an automatically detected SPI and I²C interface and an internal reference. The feature set combined with the tiny package and low power make the smart DAC an excellent choice for applications in fault management.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DAC539E4W	YBH (DSBGA, 16)	1.76mm × 1.76mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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4 Pin Configuration and Functions

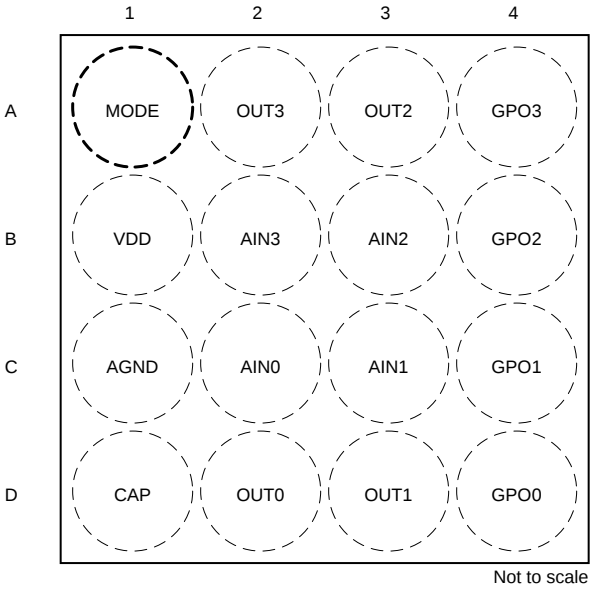


Figure 4-1. YBH Package, 16-pin DSBGA (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	MODE	Power	External reference (VREF) or MODE input. Connect a capacitor (approximately 0.1 µF) between MODE and AGND. Use a pullup resistor to VDD when the external reference is not used. Do not ramp up this pin before VDD. In case an external reference is used, make sure the reference ramps up after VDD. For programming mode, pull this pin low. For standalone mode, pull this pin high or connect to external reference.
A2	OUT3	Output	Comparator output 3. For easy PCB routing, make this pin Hi-Z using register settings and short AIN3 and OUT3.
A3	OUT2	Output	Comparator output 2. For easy PCB routing, make this pin Hi-Z using register settings and short AIN2 and OUT2.
A4	GPO3	Output	Programming mode: This pin is configurable as SDO. For SDO function, connect the pin to the I/O voltage with an external pullup resistor. If unused, connect this pin to VDD or AGND using an external resistor. This pin can ramp up before VDD. Standalone mode: General-purpose output 3. Connect this pin to the I/O voltage using an external pullup resistor.
B1	VDD	Power	Supply voltage.
B2	AIN3	Input	Analog input pin for channel 3.
B3	AIN2	Input	Analog input pin for channel 2.
B4	GPO2	Input/Output	Programming mode (SCL/$\overline{\text{SYNC}}$): I^2C serial interface clock or SPI chip select input. Connect this to the I/O voltage using an external pullup resistor. This pin can ramp up before VDD. Standalone mode: General-purpose output 2. Connect this pin to the I/O voltage using an external pullup resistor.
C1	AGND	Ground	Ground reference point for all circuitry on the device.
C2	AIN0	Input	Analog input pin for channel 0.
C3	AIN1	Input	Analog input pin for channel 1.

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
C4	GPO1	Input/Output	Programming mode (A0/SDI): Address configuration pin for I^2C or serial data input for SPI. For A0, connect this pin to VDD, AGND, SDA, or SCL for address configuration. For SDI, this pin need not be pulled up or pulled down. This pin can ramp up before VDD. Standalone mode: General-purpose output 1. Connect this pin to the I/O voltage using an external pullup resistor.
D1	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
D2	OUT0	Output	Comparator output 0. For easy PCB routing, make this pin Hi-Z using register settings and short AIN0 and OUT0.
D3	OUT1	Output	Comparator output 1. For easy PCB routing, make this pin Hi-Z using register settings and short AIN1 and OUT1.
D4	GPO0	Input/Output	Programming mode (SDA/SCLK): Bidirectional I^2C serial data bus or SPI clock input. Connect this pin to the I/O voltage using an external pullup resistor in I^2C mode. This pin can ramp up before VDD. Standalone mode: General-purpose output 0. Connect this pin to the I/O voltage using an external pullup resistor.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to AGND	–0.3	6	V
	Digital inputs to AGND	–0.3	V_{DD} + 0.3	V
	V_{AINX} to AGND	–0.3	V_{DD} + 0.3	V
	V_{OUTX} to AGND	–0.3	V_{DD} + 0.3	V
V_{REF}	External reference, V_{REF} to AGND	–0.3	V_{DD} + 0.3	V
	Current into any pin except the OUTx, VDD, and AGND pins	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (AGND)	1.7		5.5	V
V_{REF}	External reference to ground (AGND)	1.7		V_{DD}	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
C_{CAP}	External capacitor on CAP pin	0.5		15	µF
T_A	Ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		DAC539E4W YBH (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.3	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

5.5 Electrical Characteristics: Threshold DAC

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		10			Bits
INL	Integral nonlinearity(1)		–1.25		1.25	LSB
DNL	Differential nonlinearity(1)		–1		1	LSB
	Offset error(3)	1.7 V ≤ V_{DD} < 2.7 V, AINx pin shorted to OUTx, DAC code: 8d	–0.75	0.3	0.75	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, AINx pin shorted to V_{OUT}, DAC code: 8d	–0.5	0.25	0.5	
	Offset-error temperature coefficient(3)	AINx pin shorted to OUTx, DAC code: 8d		±0.0003		%FSR/°C
	Gain error(3)	Between end-point codes: 8d to 1016d	–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(3)	Between end-point codes: 8d to 1016d		±0.0008		%FSR/°C
OUTPUT						
Z_O	V_{AIN} dc output impedance(3)	DAC output enabled, internal reference (gain = 1.5 × or 2 ×) or external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	400	500	600	kΩ
		DAC output enabled, internal V_{REF}, gain = 3 × or 4 ×	325	400	485	

(1) Measured with output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 × gain + 0.2 V, between end-point codes: 8d to 1016d.
(2) Specified with 200-mV headroom with respect to reference value when internal reference is used.
(3) Measured with output unloaded.

5.6 Electrical Characteristics: Comparator

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 × in voltage output mode, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Offset error(1) (2)	1.7 V ≤ V_{DD} ≤ 5.5 V; DAC at midscale, comparator input at Hi-Z, and DAC operating with external reference.	–6	0	6	mV
	Offset error time drift(1)	V_{DD} = 5.5 V, external reference, T_A = 125°C, AINx in Hi-Z mode, DAC at full scale and V_{AINX} at 0 V or DAC at zero scale and V_{AINX} at 1.84 V, drift specified for 10 years of continuous operation		4		mV
OUTPUT						
	Input voltage	V_{REF} connected to V_{DD}, AINx resistor network connected to ground	0		V_{DD}	V
		V_{REF} connected to V_{DD}, AINx resistor network disconnected from ground	0		V_{DD} × (1/3 – 1/100)	
V_{OL}	Logic low output voltage	I_{LOAD} = 100 µA, output in open-drain mode		0.1		V
DYNAMIC PERFORMANCE						
t_{resp}	Output response time	DAC at midscale with 10-bit resolution, AINx input at Hi-Z, and transition step at AINx node is (V_{DAC} – 2 LSB) to (V_{DAC} + 2 LSB), transition time measured between 10% and 90% of output, output current of 100 µA, comparator output configured in push-pull mode, load capacitor at comparator output is 25 pF		10		µs

(1) Specified by design and characterization, not production tested.
(2) This specification does not include the total unadjusted error (TUE) of the DAC.

5.7 Electrical Characteristics: General

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×,and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	T_A = 25°C for all measurements	1.1979	1.212	1.224	V
	Reference output temperature coefficient(1) (2)				50	ppm/°C
EXTERNAL REFERENCE						
	V_{REF} input impedance(1) (3)			192		kΩ-ch
EEPROM						
	Endurance(1)	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A = 125°C		1000		
	Data retention(1)			50		Years
	EEPROM programming write cycle time(1)				200	ms
	Device boot-up time(1)	Time taken from power valid (V_{DD} ≥ 1.7 V) to output valid state (output state as programmed in EEPROM), 0.5-µF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Current flowing into VDD	DAC in sleep mode, internal reference powered down, external reference at 5.5 V			28	µA
	Current flowing into VDD(1)	DAC in sleep mode, internal reference enabled, additional current through internal reference		10		
		DAC channels enabled, internal reference enabled, additional current through internal reference per DAC channel in voltage-output mode		12.5		µA-ch
		Normal operation, state machine enabled		1.53		mA
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into OUTx and AINx	DAC in Hi-Z output mode, 1.7 V ≤ V_{DD} ≤ 5.5 V		10		nA

(1) Specified by design and characterization, not production tested.
(2) Measured at –40°C and +125°C and calculated the slope.
(3) Impedances for the DAC channels are connected in parallel.

5.8 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCL}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs

5.9 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCL}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs

5.10 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCL}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs

5.11 Timing Requirements: SPI Write Operation

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			ns
$t_{SCLKLOW}$	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	10			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time (time between subsequent $\overline{SYNC}$ falling edges) for same channel	2			µs

5.12 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 0

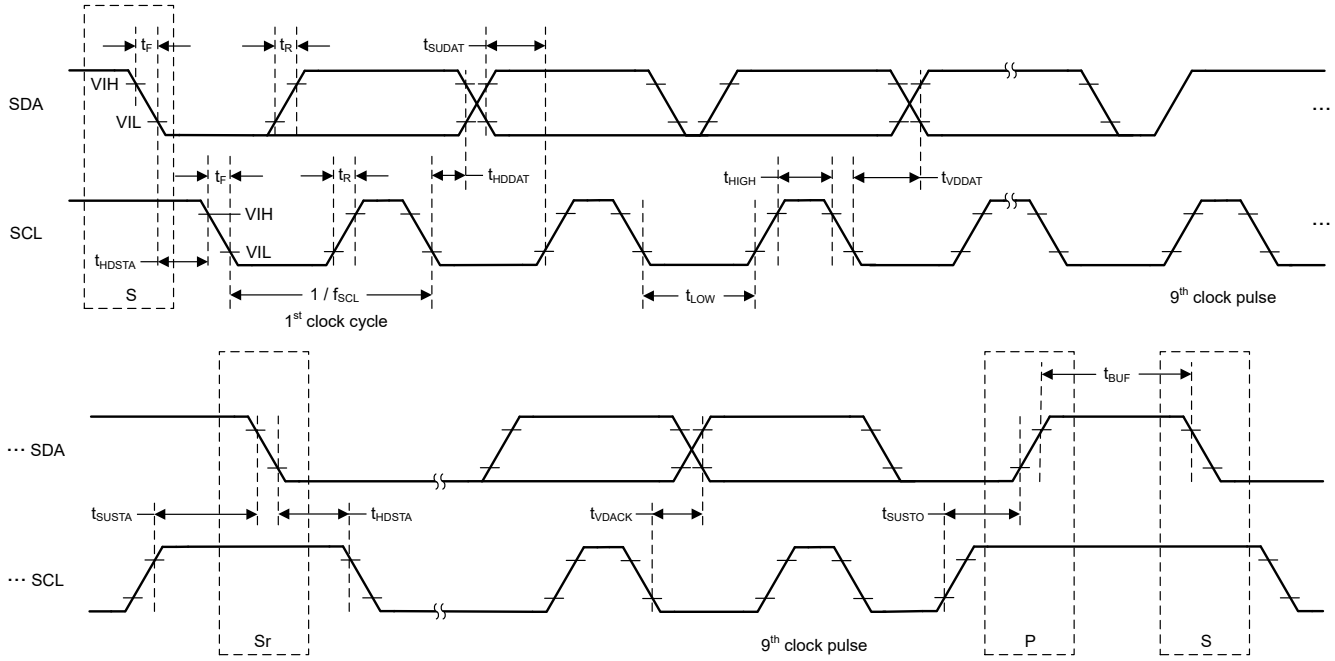
		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			1.25	MHz
$t_{SCLKHIGH}$	SCLK high time	350			ns
$t_{SCLKLOW}$	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	400			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

5.13 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 1

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			2.5	MHz
$t_{SCLKHIGH}$	SCLK high time	175			ns
$t_{SCLKLOW}$	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	300			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

5.14 Timing Diagrams



S: Start bit, **Sr**: Repeated start bit, **P**: Stop bit

Figure 5-1. I²C Timing Diagram

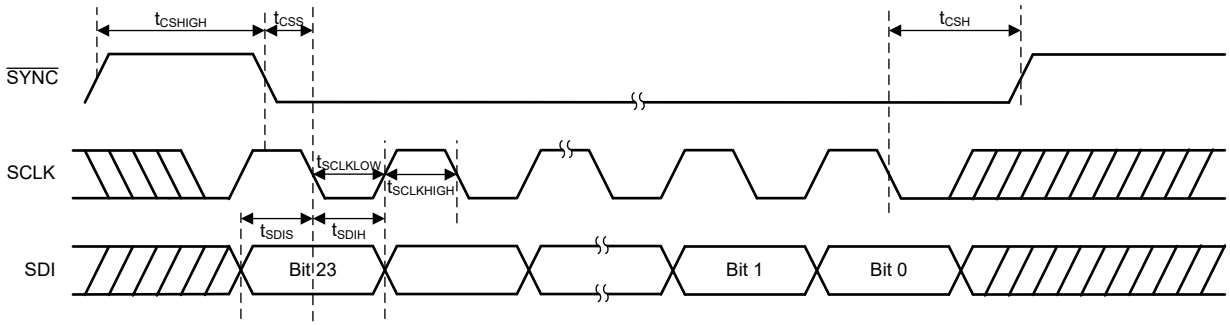


Figure 5-2. SPI Write Timing Diagram

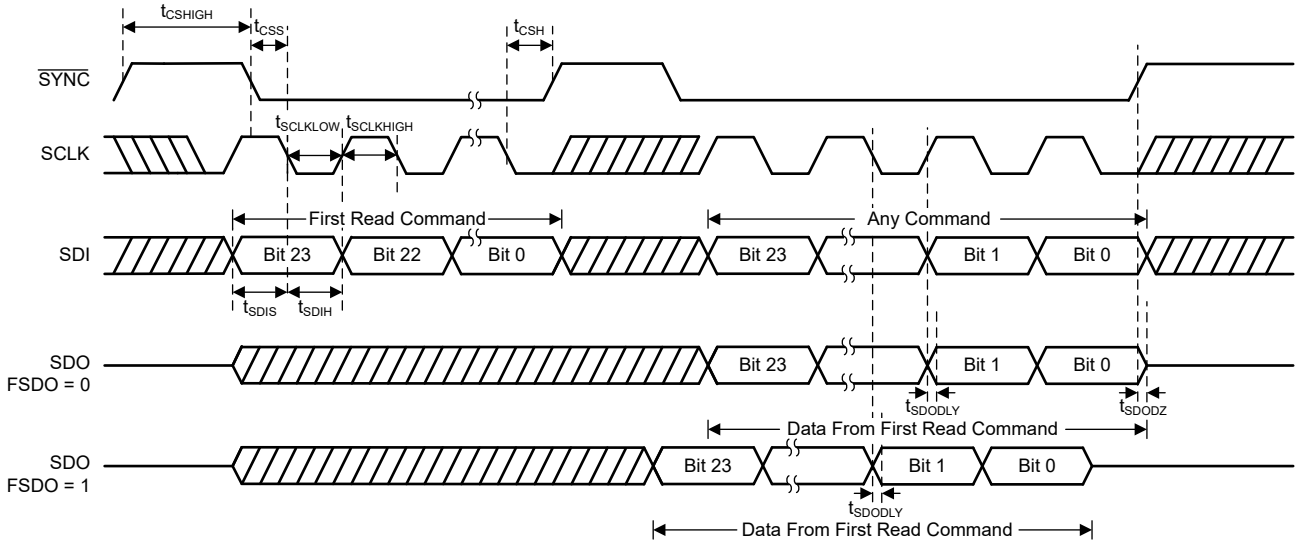


Figure 5-3. SPI Read Timing Diagram

5.15 Typical Characteristics

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, AINx pins in Hi-Z mode, and the outputs unloaded (unless otherwise noted)

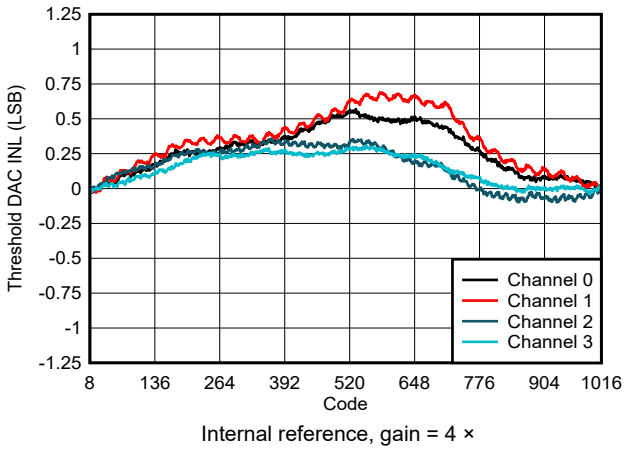


Figure 5-4. Threshold DAC INL vs Digital Input Code

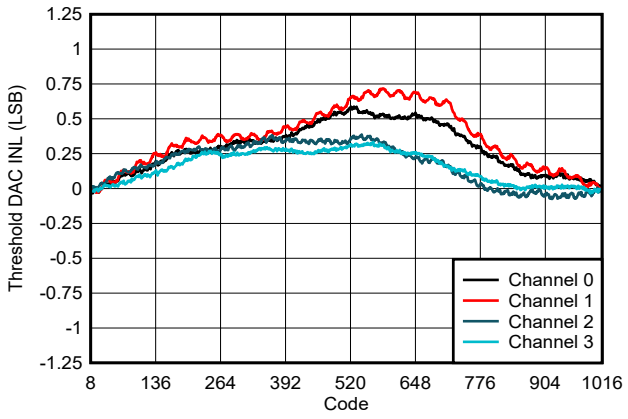


Figure 5-5. Threshold DAC INL vs Digital Input Code

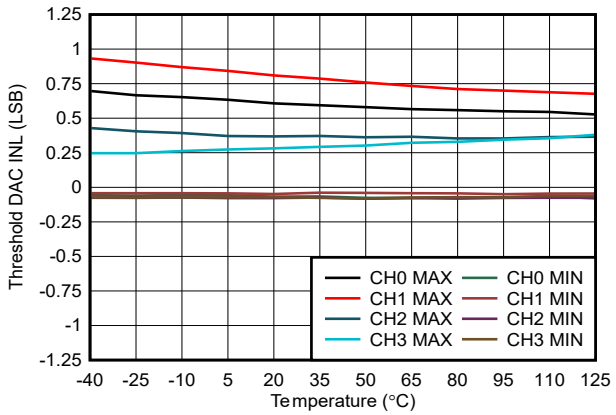


Figure 5-6. Threshold DAC INL vs Temperature

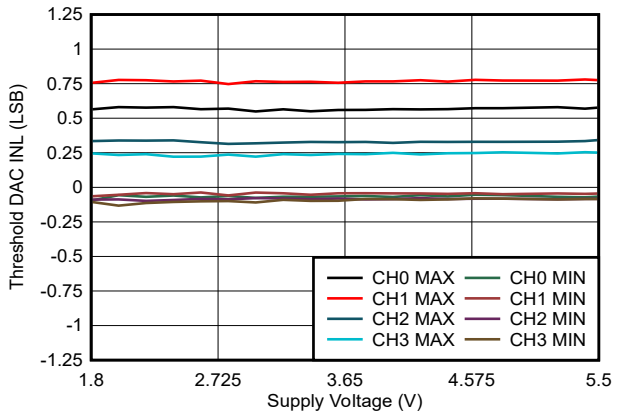


Figure 5-7. Threshold DAC INL vs Supply Voltage

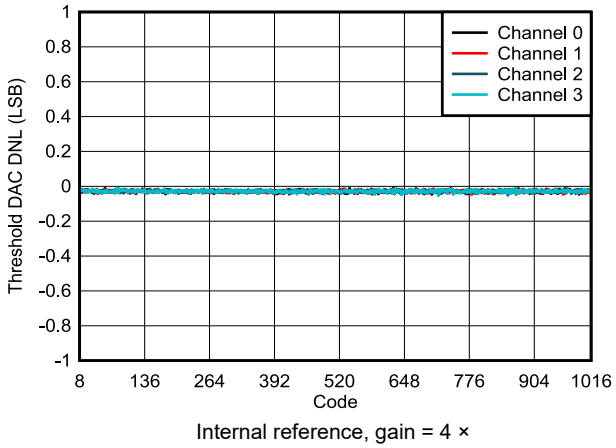


Figure 5-8. Threshold DAC DNL vs Digital Input Code

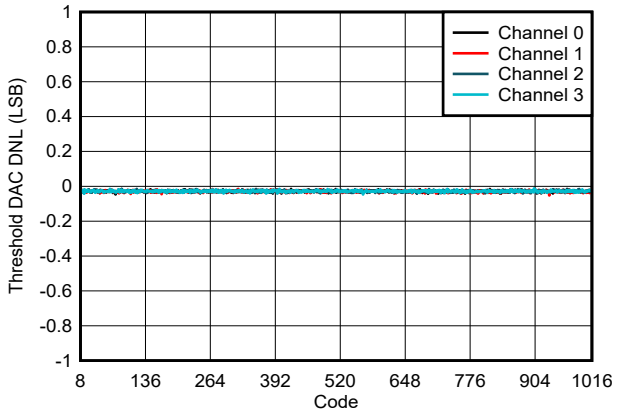


Figure 5-9. Threshold DAC DNL vs Digital Input Code

5.15 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, AINx pins in Hi-Z mode, and the outputs unloaded (unless otherwise noted)

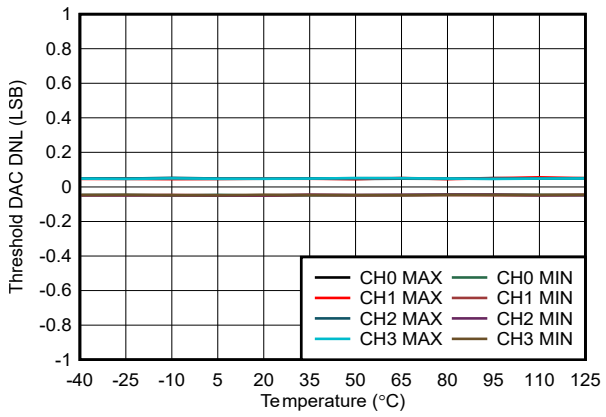


Figure 5-10. Threshold DAC DNL vs Temperature

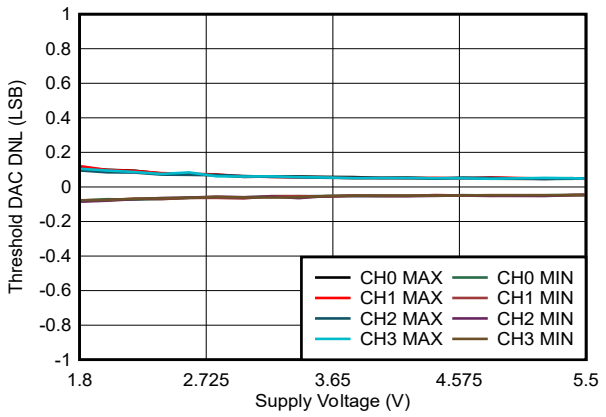


Figure 5-11. Threshold DAC DNL vs Supply Voltage

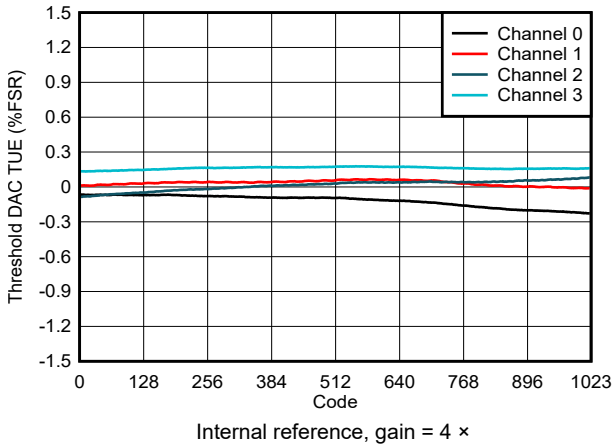


Figure 5-12. Threshold DAC Total Unadjusted Error (TUE) vs Digital Input Code

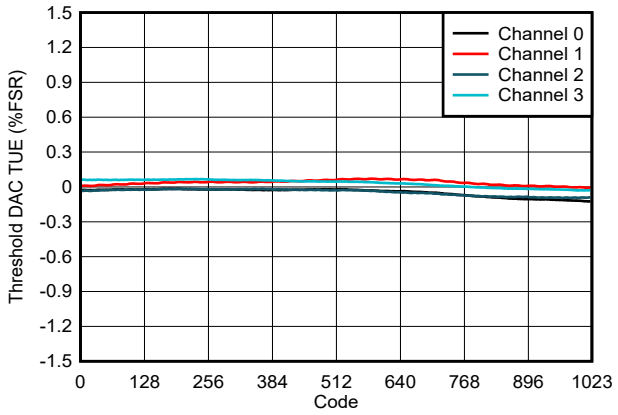


Figure 5-13. Threshold DAC Total Unadjusted Error (TUE) vs Digital Input Code

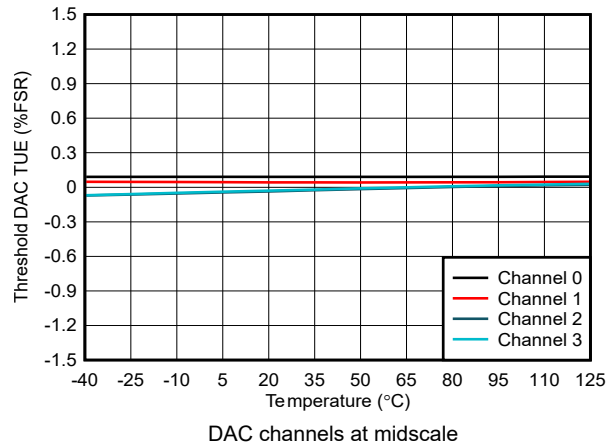


Figure 5-14. Threshold DAC Total Unadjusted Error (TUE) vs Temperature

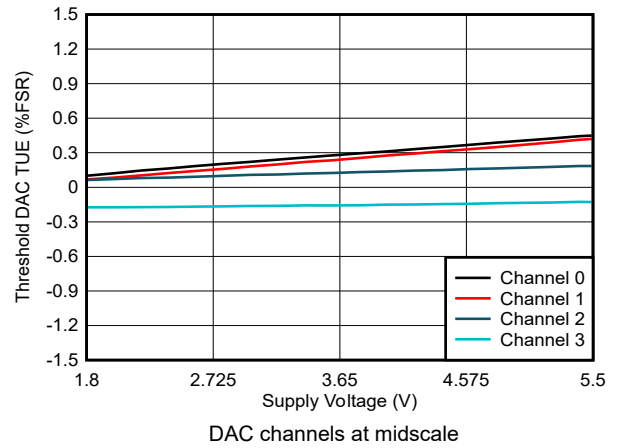


Figure 5-15. Threshold DAC Total Unadjusted Error (TUE) vs Supply Voltage

5.15 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, AINx pins in Hi-Z mode, and the outputs unloaded (unless otherwise noted)

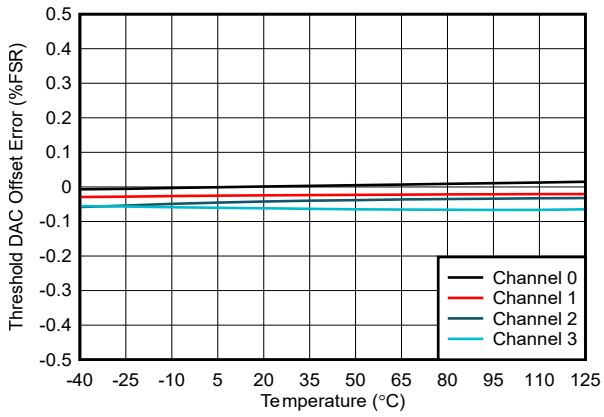


Figure 5-16. Threshold DAC Offset Error vs Temperature

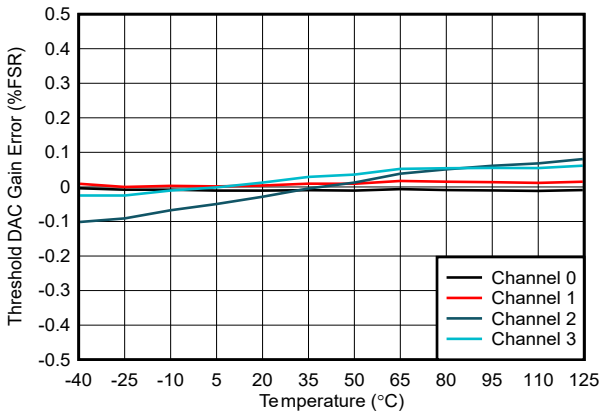
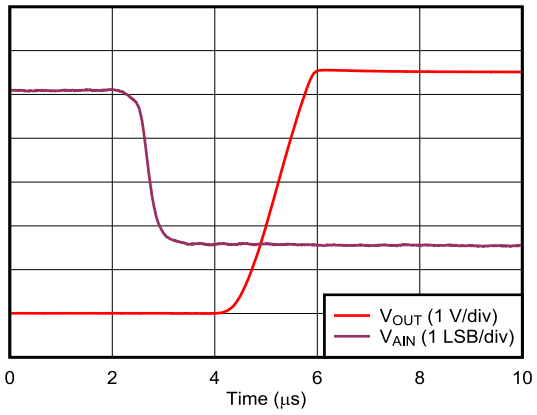
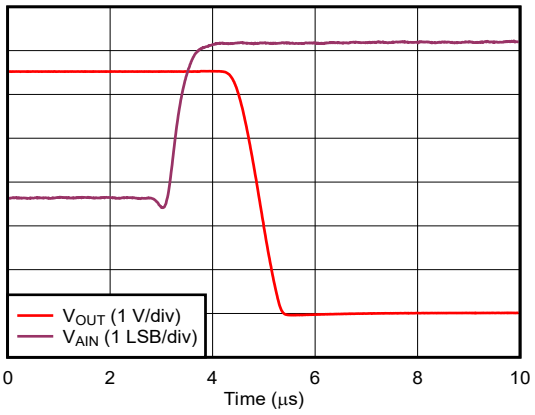


Figure 5-17. Threshold DAC Gain Error vs Temperature



Comparator output in push-pull mode

Figure 5-18. Comparator Response Time: Low-to-High Transition



Comparator output in push-pull mode

Figure 5-19. Comparator Response Time: High-to-Low Transition

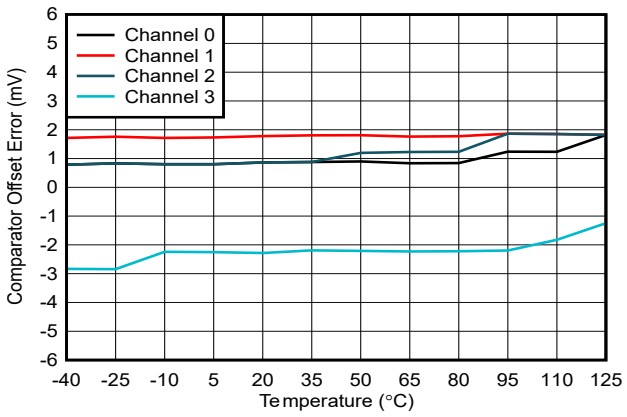
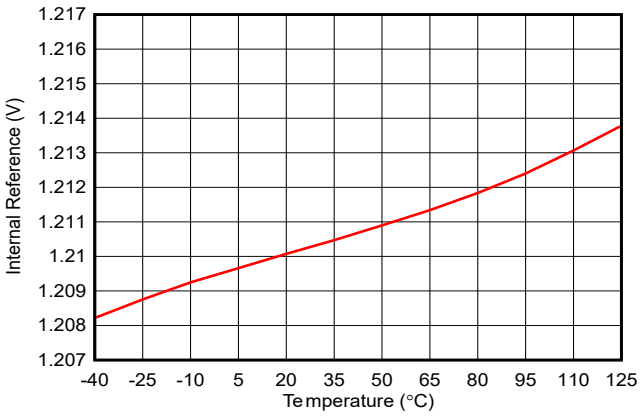


Figure 5-20. Comparator Offset Error vs Temperature



Internal reference

Figure 5-21. Internal Reference vs Temperature

5.15 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, AINx pins in Hi-Z mode, and the outputs unloaded (unless otherwise noted)

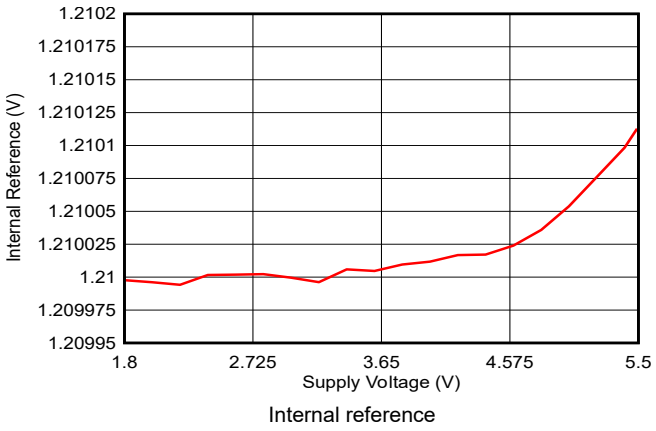


Figure 5-22. Internal Reference vs Supply Voltage

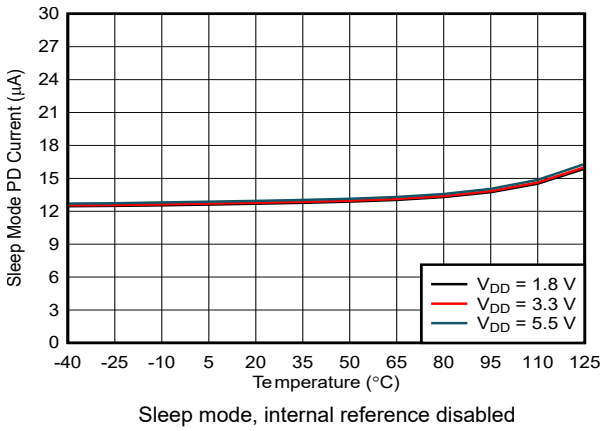


Figure 5-23. Power-Down Current vs Temperature

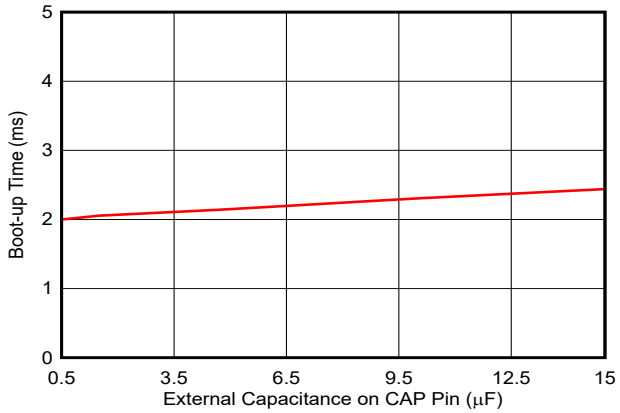


Figure 5-24. Boot-up Time vs Capacitance on CAP pin

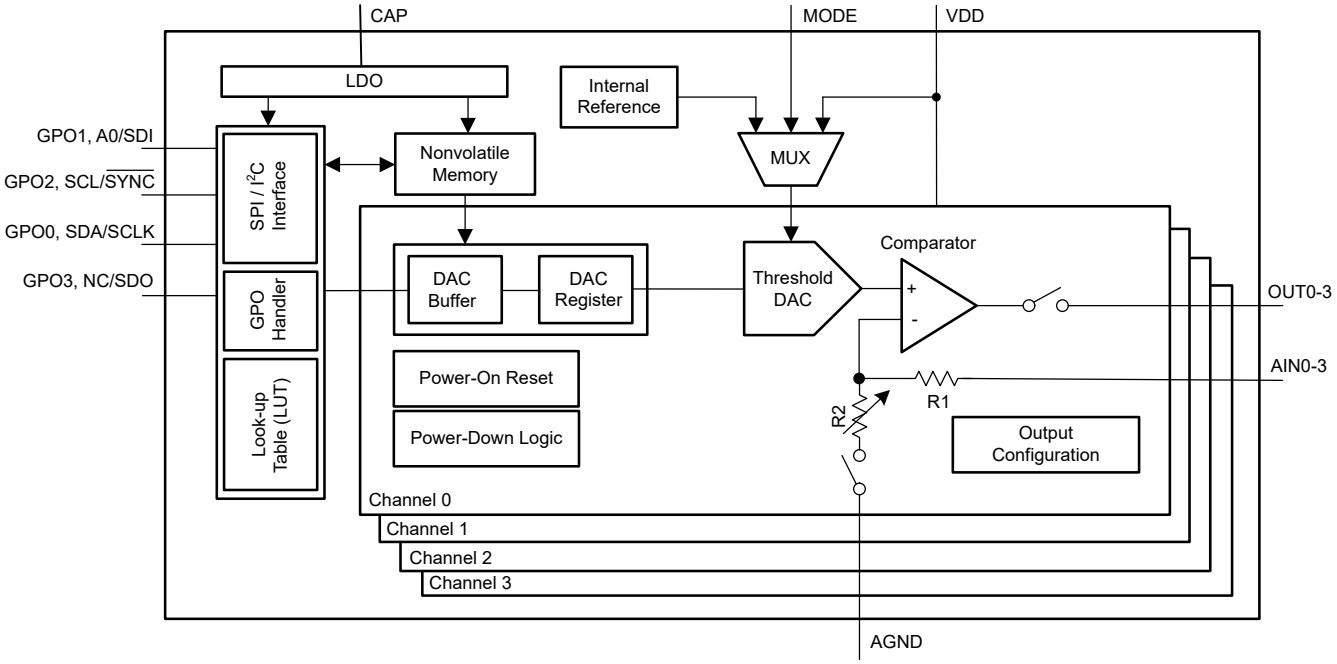
6 Detailed Description

6.1 Overview

The DAC539E4W is a 10-bit, quad smart digital-to-analog converter (DAC) with programmable comparators and look-up table based general-purpose outputs. The comparator outputs are available directly as an option. The comparator inputs can be configured as Hi-Z for an input range of VDD/3 or as finite resistance for the full input range. The comparators use four threshold DACs as reference. All the threshold DACs can be configured independently and the settings can be stored in the NVM.

The DAC539E4W uses the MODE pin to select between programming mode (I^2C or SPI) and standalone mode. This device provides nonvolatile memory (NVM) to store the register settings at factory using the SPI or I^2C interface. After being programmed, this device functions autonomously without the need for a processor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Smart Digital-to-Analog Converter (DAC) Architecture

The DAC539E4W uses a string architecture for the threshold DACs, followed by comparators. Section 6.2 shows the DAC architecture within the block diagram, which operates from a 1.8-V to 5.5-V power supply.

The threshold DAC uses one of the following three reference options: the internal voltage reference of 1.21 V, an external reference on the MODE pin, or the power supply. The threshold DACs support multiple programmable output ranges.

The comparator outputs can be inverted using register settings. The comparator outputs can be push-pull or open-drain. The analog inputs can be configured as Hi-Z or finite impedance to support different input ranges. The comparators supports programmable hysteresis using the *margin-high* and *margin-low* register fields, and latching comparator although the *margin-high* and *margin-low* register field are not stored in the NVM. The comparator outputs are accessible internally by the device.

The DAC539E4W features a programmable state machine supporting arithmetic, logic, and timing operations, as shown in Figure 6-1. This state machine is preprogrammed as a look-up table that maps the comparator outputs to the GPOs for the DAC539E4W. The state machine is configured using the register map, and the parameters can be stored in the NVM. The state machine can be operated in standalone mode without interfacing to a processor (*processor-less* operation).

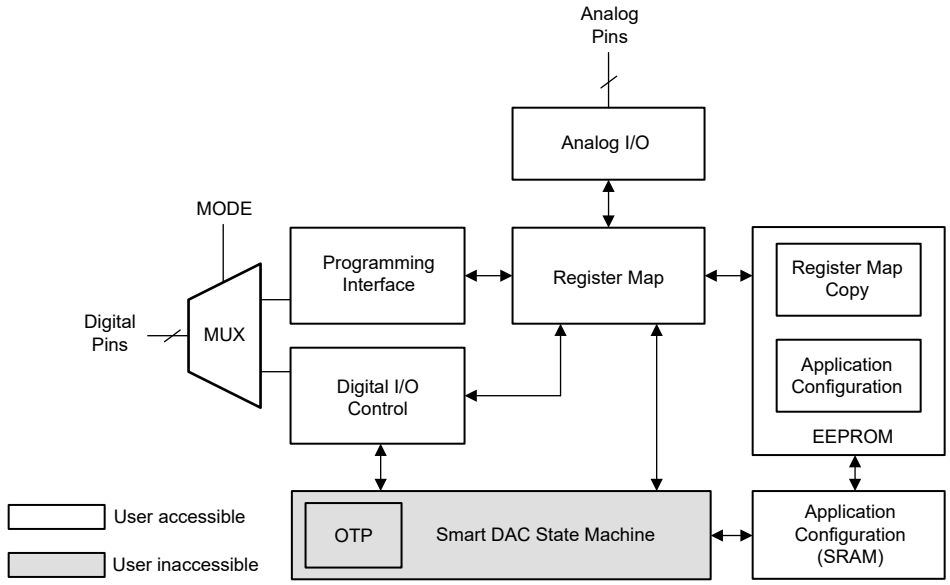


Figure 6-1. Smart DAC Architecture

6.3.2 Threshold DAC

The threshold DAC for each channel can be enabled by selecting the power-up option in the VOUT-PDN-x fields in the COMMON-CONFIG register. To achieve the desired threshold voltage, select the correct reference option, select the gain for the required output range, and program the DAC code in the DAC-x-DATA register of the respective channels.

6.3.2.1 Voltage Reference and DAC Transfer Function

There are three voltage reference options possible with the DAC539E4W: internal reference, external reference, and the power supply as reference, as shown in Figure 6-2. The transfer function for the threshold DAC changes based on the voltage reference selection.

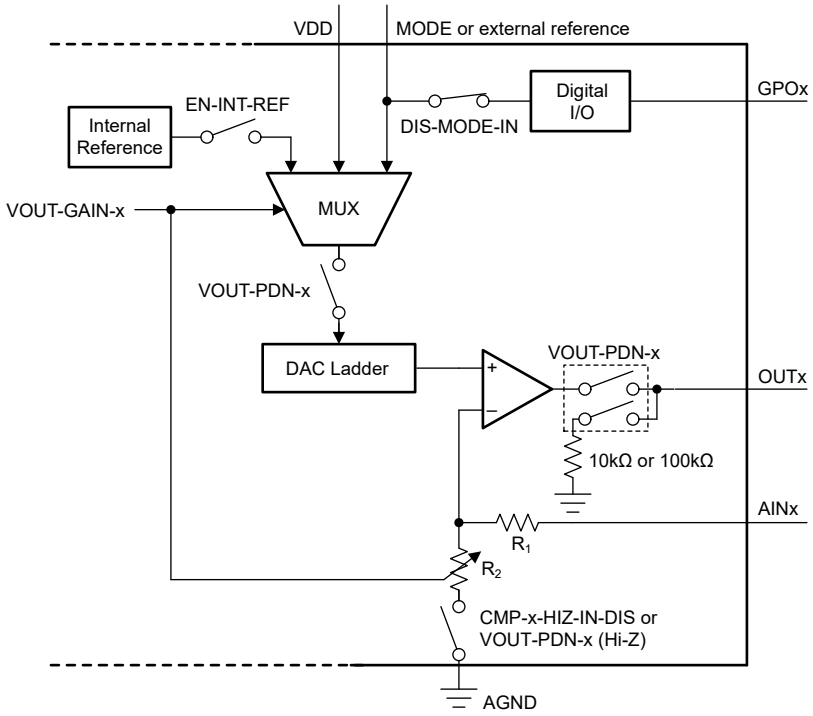


Figure 6-2. Voltage Reference Selection and Power-Down Logic

6.3.2.1.1 Power-Supply as Reference

By default, the DAC539E4W operates with the power-supply pin (VDD) as a reference. Equation 1 shows the transfer function of the threshold DAC when the power-supply pin is used as reference. The gain at the output stage is always 1 ×.

$$V_{THLD} = \frac{DAC\_DATA}{2^N} \times V_{DD} \quad (1)$$

where:

- N is the resolution in bits, 10 bits for DAC539E4W.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-x-DATA field in the DAC-x-DATA register.
- DAC_DATA ranges from 0 to $2^N - 1$.
- V_{DD} is used as the DAC reference voltage.

6.3.2.1.2 Internal Reference

The DAC539E4W contains an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage (V_{THLD}). Equation 2 shows DAC transfer function using the internal reference.

$$V_{THLD} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \quad (2)$$

where:

- N is the resolution in bits, 10 bits for DAC539E4W
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-x-DATA field in the DAC-x-DATA register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on VOUT-GAIN-x bits.

6.3.2.1.3 External Reference

The DAC539E4W provides an external reference input (MODE pin). Select the external reference option by configuring the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register appropriately. In case the MODE pin functionality is not used, write 1 to the DIS-MODE-IN bit in the DEVICE-MODE-CONFIG register to minimize quiescent current. The external reference can be between 1.8 V and VDD. Equation 3 shows the transfer function of the threshold DAC when the external reference is used.

Note

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{THLD} = \frac{DAC\_DATA}{2^N} \times V_{REF} \quad (3)$$

where:

- N is the resolution in bits, 10 bits for DAC539E4W.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-x-DATA field in the DAC-x-DATA register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the external reference voltage.

6.3.3 Look-Up Table (LUT)

The DAC539E4W provides a user-programmable look-up table that maps the comparator inputs to the GPOs. This LUT can be stored in the NVM for standalone operation. Table 6-1 and Table 6-2 show the user-programmable LUT with different settings of the CMP-x-INV-EN bit in the DAC-x-VOUT-CMP-CONFIG register. Table 6-3 shows the pin mapping between the programming and standalone modes.

Table 6-1. Comparator Input to GPO Map (CMP-x-INV-EN = 0, default)

COMPARATOR INPUTS				USER-PROGRAMMABLE OUTPUTS (DEFAULT VALUES)				SRAM LOCATION	NAME
AIN3	AIN2	AIN1	AIN0	GPO3	GPO2	GPO1	GPO0		
0	0	0	0	1	1	1	1	0x25[3:0]	LUT-0-DATA
0	0	0	1	1	1	1	0	0x26[3:0]	LUT-1-DATA
0	0	1	0	1	1	0	1	0x27[3:0]	LUT-2-DATA
0	0	1	1	1	1	0	0	0x28[3:0]	LUT-3-DATA
0	1	0	0	1	0	1	1	0x29[3:0]	LUT-4-DATA
0	1	0	1	1	0	1	0	0x2A[3:0]	LUT-5-DATA
0	1	1	0	1	0	0	1	0x2B[3:0]	LUT-6-DATA
0	1	1	1	1	0	0	0	0x2C[3:0]	LUT-7-DATA
1	0	0	0	0	1	1	1	0x2D[3:0]	LUT-8-DATA
1	0	0	1	0	1	1	0	0x2E[3:0]	LUT-9-DATA
1	0	1	0	0	1	0	1	0x2F[3:0]	LUT-10-DATA
1	0	1	1	0	1	0	0	0x30[3:0]	LUT-11-DATA
1	1	0	0	0	0	1	1	0x31[3:0]	LUT-12-DATA
1	1	0	1	0	0	1	0	0x32[3:0]	LUT-13-DATA
1	1	1	0	0	0	0	1	0x33[3:0]	LUT-14-DATA
1	1	1	1	0	0	0	0	0x34[3:0]	LUT-15-DATA

Table 6-2. Comparator Input to GPO Map (CMP-x-INV-EN = 1)

COMPARATOR INPUTS				USER-PROGRAMMABLE OUTPUTS (DEFAULT VALUES)				SRAM LOCATION	NAME
AIN3	AIN2	AIN1	AIN0	GPO3	GPO2	GPO1	GPO0		
0	0	0	0	0	0	0	0	0x25[3:0]	LUT-0-DATA
0	0	0	1	0	0	0	1	0x26[3:0]	LUT-1-DATA
0	0	1	0	0	0	1	0	0x27[3:0]	LUT-2-DATA
0	0	1	1	0	0	1	1	0x28[3:0]	LUT-3-DATA
0	1	0	0	0	1	0	0	0x29[3:0]	LUT-4-DATA
0	1	0	1	0	1	0	1	0x2A[3:0]	LUT-5-DATA
0	1	1	0	0	1	1	0	0x2B[3:0]	LUT-6-DATA
0	1	1	1	0	1	1	1	0x2C[3:0]	LUT-7-DATA
1	0	0	0	1	0	0	0	0x2D[3:0]	LUT-8-DATA
1	0	0	1	1	0	0	1	0x2E[3:0]	LUT-9-DATA
1	0	1	0	1	0	1	0	0x2F[3:0]	LUT-10-DATA
1	0	1	1	1	0	1	1	0x30[3:0]	LUT-11-DATA
1	1	0	0	1	1	0	0	0x31[3:0]	LUT-12-DATA
1	1	0	1	1	1	0	1	0x32[3:0]	LUT-13-DATA
1	1	1	0	1	1	1	0	0x33[3:0]	LUT-14-DATA
1	1	1	1	1	1	1	1	0x34[3:0]	LUT-15-DATA

Table 6-3. GPO Pin Mapping

STANDALONE MODE (MODE PIN IS HIGH)	PROGRAMMING MODE (MODE PIN IS LOW)	PIN NUMBER
GPO0	SDA/SCLK	8
GPO1	A0/SDI	7
GPO2	SCL/$\overline{\text{SYNC}}$	6
GPO3	NC/SDO	5

The DAC539E4W provides a programmable delay between the comparator outputs and the GPOs to allow the analog inputs to settle the transitions. This delay is specified using the LOOP-REFRESH field in the LOOP-WAIT register. Equation 4 calculates the total delay in seconds using the decimal value of the LOOP-REFRESH field.

$$\text{DELAY\_TIME} = \frac{2^{\text{LOOP\_REFRESH}} + 1}{25.6 \times 10^{6}} \quad (4)$$

6.3.4 Programming Interface

The DAC539E4W has four digital I/O pins that include I^2C and SPI. These devices automatically detect I^2C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I^2C interface uses the A0 pin to select from among four address options. The SPI is a 3-wire interface by default. No readback capability is available in this mode. The NC/SDO pin can be configured in the register map and then programmed in to the NVM as the SDO output. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I^2C: SCL, SDA, A0
- SPI: SCLK, SDI, $\overline{\text{SYNC}}$, NC/SDO

All the digital pins are open-drain when used as outputs. Therefore, all the output pins must be pulled up to the desired I/O voltage using external registers.

6.3.5 Nonvolatile Memory (NVM)

The DAC539E4W contains nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, as shown in the highlighted gray cells in the *Register Map* section, can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. This is an autoresetting bit. The NVM-BUSY bit in the GENERAL-STATUS register is set to 1 by the device when an NVM write or reload operation is ongoing. During this time, the device blocks all read/write operations to the device. The NVM-BUSY bit is set to 0 after the write or reload operation is complete; at this point, all read/write operations to the device are allowed. The default value for all the registers in the DAC539E4W is loaded from NVM as soon as a POR event is issued.

The DAC539E4W also implements a NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. The NVM-reload operation overwrites the register map with the stored data from the NVM. After completion, the device autoresets this bit to 0. During the NVM-RELOAD operation, the NVM-BUSY bit is set to 1.

6.3.5.1 NVM Cyclic Redundancy Check (CRC)

The DAC539E4W implements a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in DAC539E4W:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits The CRC feature is implemented by storing a 16-Bit CRC (CRC-16-CCITT) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM.

Note

The alarm bits are set only at boot-up.

6.3.5.1.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any device registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see *Section 6.3.7*) command, or cycle power to the device. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

6.3.5.1.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any device registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see *Section 6.3.7*) command or cycle power to the device. A permanent failure in the NVM makes the device unusable.

6.3.6 Power-On Reset (POR)

The DAC539E4W includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the DAC539E4W is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in Figure 6-3, to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device reset is not deterministic under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

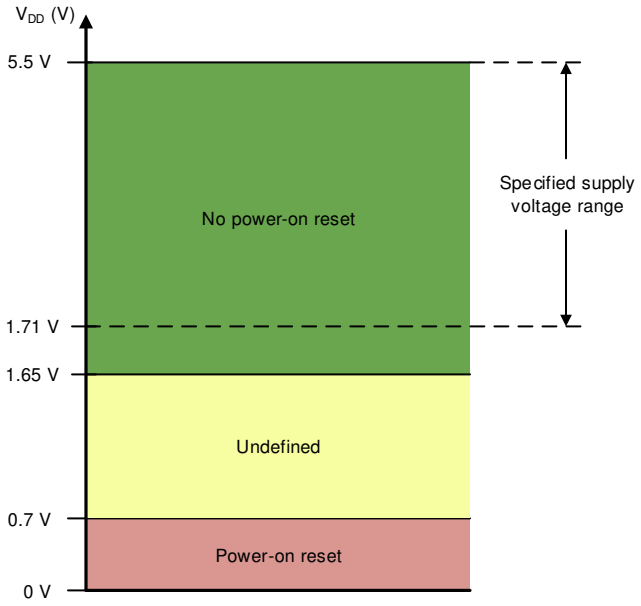


Figure 6-3. Threshold Levels for V_{DD} POR Circuit

6.3.7 External Reset

An external reset to the device can be triggered through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event.

6.3.8 Register-Map Lock

The DAC539E4W implements a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

6.4 Device Functional Modes

6.4.1 Comparator Mode

To enable the comparator for a channel, write 1 to the CMP-x-EN and the CMP-x-OUT-EN bits in the respective DAC-x-VOUT-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-x-OD-EN bit. To invert the comparator output, write 1 to the CMP-x-INV-EN bit. The AINx pin has a finite impedance. To disable high-impedance on the AINx pin, write 1 to the CMP-x-HIZ-IN-DIS bit. Table 6-4 shows the comparator output at the pin for different bit settings. Table 6-5 shows the full scale analog input settings for the comparator. Any higher input voltage is clipped.

Table 6-4. Comparator Output Configuration

CMP-x-EN	CMP-x-OUT-EN	CMP-x-OD-EN	CMP-x-INV-EN	OUTx PIN(1)
0	X	X	X	Comparator not enabled.
1	0	X	X	Hi-Z output.
1	1	0	0	Push-pull output.
1	1	0	1	Push-pull and inverted output.
1	1	1	0	Open-drain output.
1	1	1	1	Open-drain and inverted output.

(1) When the comparator is enabled, the comparator output value is accessible to the LUT irrespective of the output pin (OUTx) setting.

Table 6-5. Full Scale Analog Input (V_{FS})

REFERENCE (VREF)	GAIN	V_{FS} (Hi-Z INPUT MODE)	V_{FS} (FINITE IMPEDANCE INPUT MODE)
Power supply	1 ×	VDD / 3	VDD
External	1 ×	VREF / 3	VREF
Internal	1.5 ×	(VREF × GAIN) / 3	VREF × GAIN
	2 ×	(VREF × GAIN) / 3	VREF × GAIN
	3 ×	(VREF × GAIN) / 6	(VREF × GAIN) / 2
	4 ×	(VREF × GAIN) / 6	(VREF × GAIN) / 2

Individual comparator channels can be configured in no-hysteresis, with-hysteresis, or latching-comparator mode using the CMP-x-MODE field in the respective DAC-x-CMP-MODE-CONFIG register.

Note

Only the no-hysteresis mode is supported in the NVM. The hysteresis or latching comparator modes can be operated from the register map only.

Figure 6-4 shows the interface circuit for the comparators. The programmable comparator operation is as shown in Figure 6-5. Individual comparator channels can be configured in no-hysteresis or with-hysteresis mode using the CMP-x-MODE bit in the respective DAC-x-CMP-MODE-CONFIG register, as shown in Table 6-6.

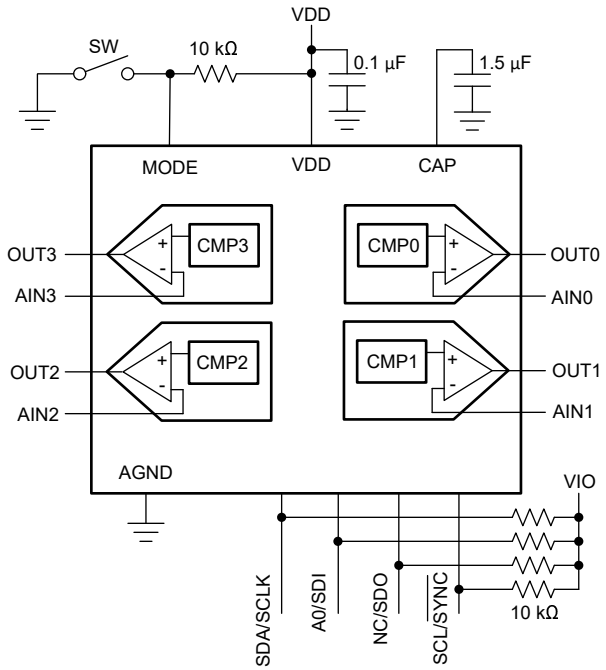


Figure 6-4. Comparator Interface

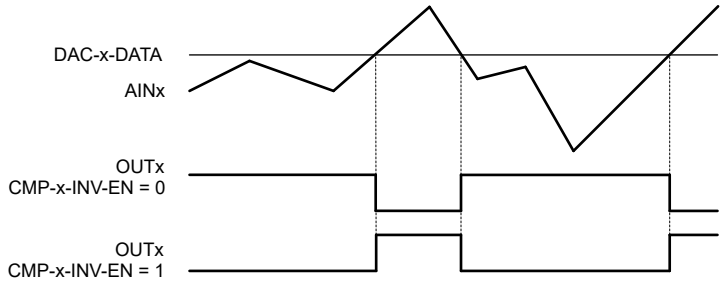


Figure 6-5. Programmable Comparator Operation

Table 6-6. Comparator Mode Selection

CMP-x-MODE BIT FIELD	COMPARATOR CONFIGURATION
00	Normal comparator mode. No hysteresis operation.
01	Hysteresis comparator mode (not supported in NVM). DAC-x-MARGIN-HIGH and DAC-x-MARGIN-LOW registers set the hysteresis.
10	Invalid setting.
11	Invalid setting.

6.4.1.1 Programmable Hysteresis Comparator

The comparator provides hysteresis when the CMP-x-MODE bit is set to 01b, as shown in Table 6-6. The hysteresis is provided by the DAC-x-MARGIN-HIGH and DAC-x-MARGIN-LOW registers, as shown in Figure 6-6.

When the DAC-x-MARGIN-HIGH is set to full-code or the DAC-x-MARGIN-LOW is set to zero-code, the comparator works as a latching comparator that is, the output is latched after the threshold is crossed. The latched output can be reset by writing to the corresponding RST-CMP-FLAG-x bit in the COMMON-DAC-TRIG register. Figure 6-7 shows the behavior of a latching comparator with active low output and Figure 6-8 shows the behavior of a latching comparator with active high output.

Note

The value of the DAC-x-MARGIN-HIGH register must be greater than the value of the DAC-x-MARGIN-LOW register. The comparator output in the hysteresis mode can only be noninverting that is, the CMP-x-INV-EN bit in the DAC-x-VOUT-CMP-CONFIG register must be set to 0. In latching mode, for the reset to take effect, the input voltage must be within DAC-x-MARGIN-HIGH and DAC-x-MARGIN-LOW.

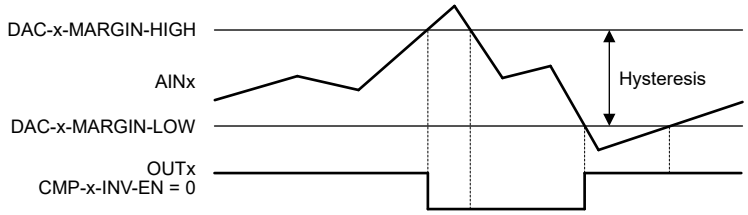


Figure 6-6. Programmable Hysteresis Without Latching Output

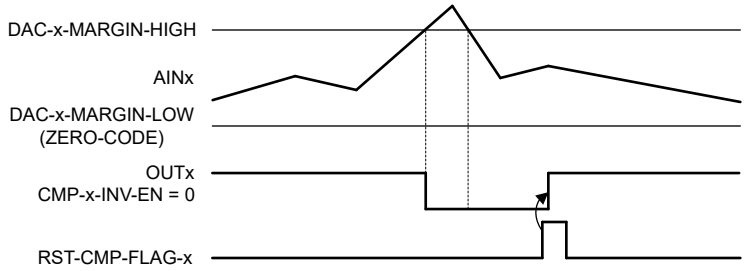


Figure 6-7. Latching Comparator With Active-Low Output

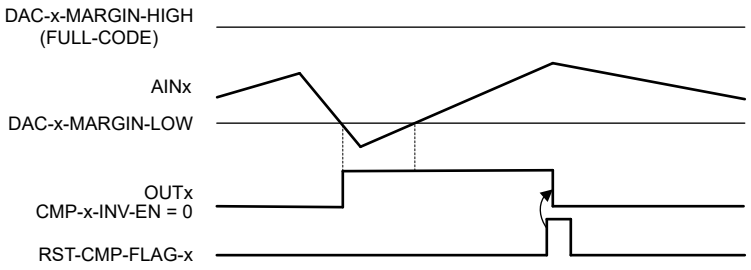


Figure 6-8. Latching Comparator With Active-High Output

6.4.2 Power-Down Mode

The comparators and the internal reference in DAC539E4W can be independently powered down through the EN-INT-REF and VOUT-PDN-x bits in the COMMON-CONFIG register, as shown in Figure 6-2. At power up, the DAC output and the internal reference are disabled by default. In power-down mode, the comparator outputs (OUTx pins) are in a high-impedance state. To change this state to 10 kΩ-A_{GND} or 100 kΩ-A_{GND} (at power up), use the VOUT-PDN-x bits.

The comparator power-up state can be programmed to any state (power-down or normal mode) using the NVM. Table 6-7 shows the comparator power-down bits.

Table 6-7. Comparator Power-Down Bits

REGISTER	VOUT-PDN-x[1]	VOUT-PDN-x[0]	DESCRIPTION
COMMON-CONFIG	0	0	Power up channel x.
	0	1	Power down channel x with 10 kΩ to AGND.
	1	0	Power down channel x with 100 kΩ to AGND.
	1	1	Power down channel x to Hi-Z. (default).

6.5 Programming

6.5.1 SPI Programming Mode

To initiate an SPI access cycle for the DAC539E4W, assert the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, is a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for the DAC539E4W is 24 bits long. Therefore, ensure that the $\overline{\text{SYNC}}$ pin stays low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In the three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

Table 6-8 and Figure 6-9 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

Table 6-8. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Identifies the communication as a read or write command to the address register: R/$\overline{\text{W}}$ = 0 sets a write operation. R/$\overline{\text{W}}$ = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are *don't care* values.

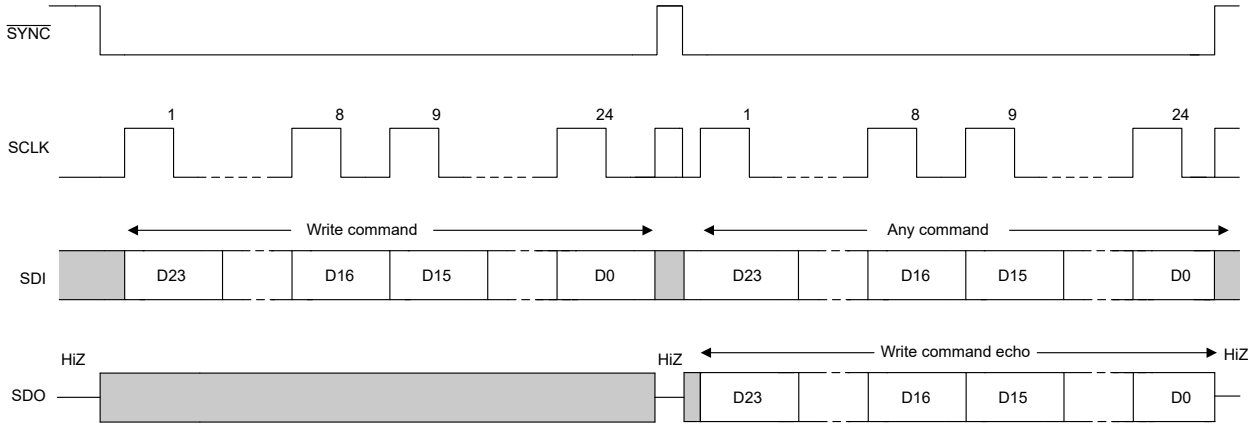


Figure 6-9. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. Table 6-9 and Figure 6-10 show the output data format. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit; see Figure 5-3.

Table 6-9. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Echo R/$\overline{\text{W}}$ from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle

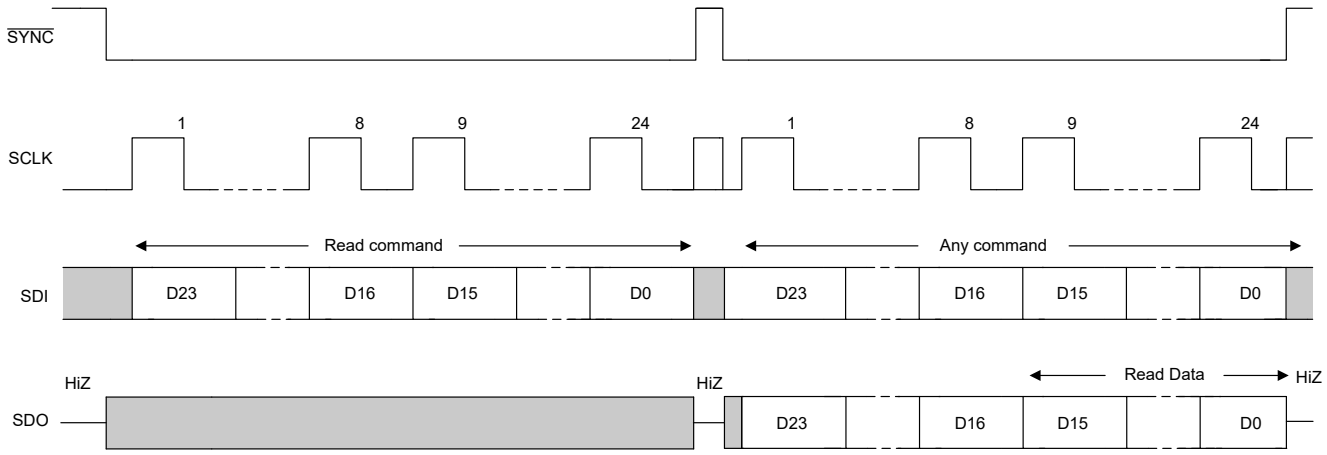


Figure 6-10. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. In daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device, as shown in Figure 6-11. The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. Figure 6-12 describes the packet format for the daisy-chain write cycle.

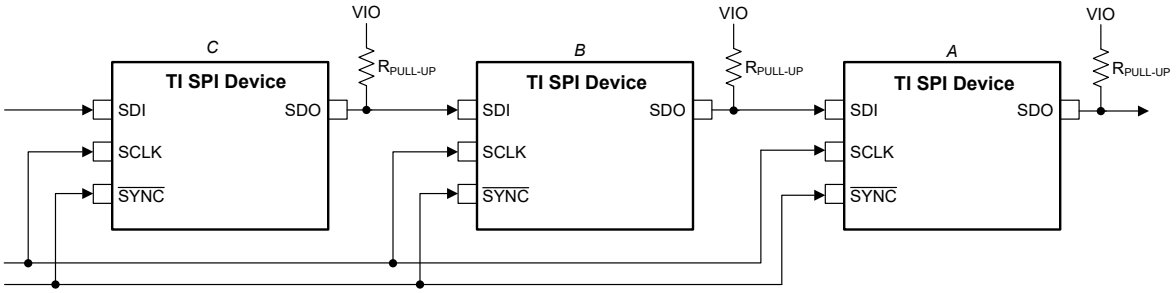


Figure 6-11. SPI Daisy-Chain Connection

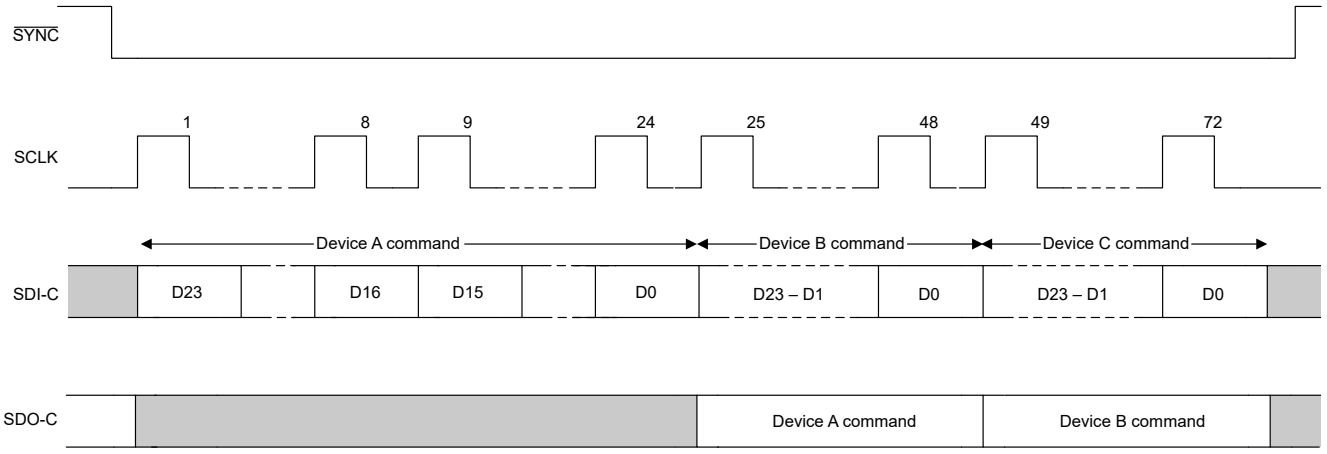


Figure 6-12. SPI Daisy-Chain Write Cycle

6.5.2 I²C Programming Mode

The DAC539E4W has a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram in the *Pin Configuration and Functions* section. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I²C bus is typically a microcontroller or digital signal processor (DSP). The DAC539E4W operates as a target on the I²C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the DAC539E4W operates as a target receiver. A controller writes to the DAC539E4W, a target receiver. However, if a controller requires the DAC539E4W internal register data, the DAC539E4W operates as a target transmitter. In this case, the controller reads from the DAC539E4W. According to I²C terminology, read and write refer to the controller.

The DAC539E4W supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The DAC539E4W supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in Figure 6-13.

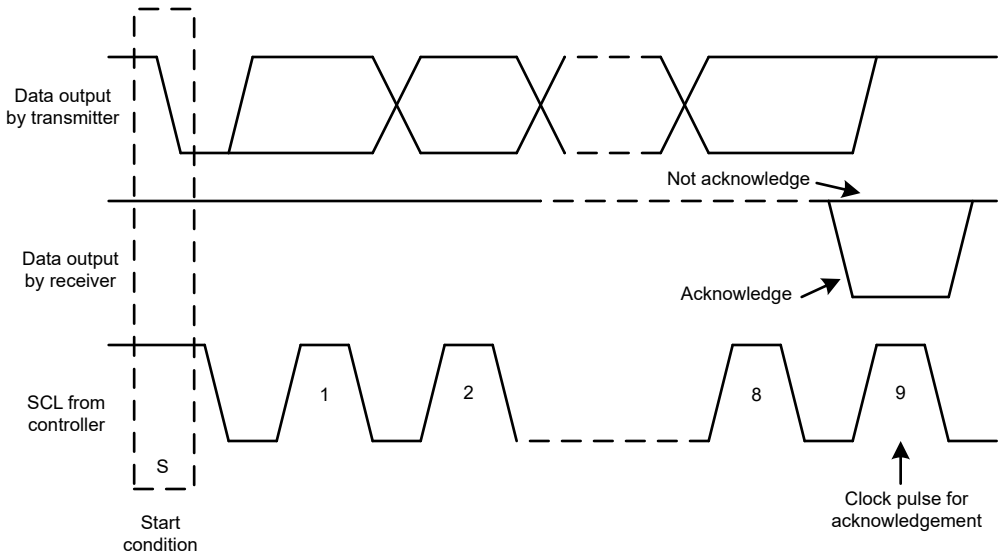


Figure 6-13. Acknowledge and Not Acknowledge on the I²C Bus

6.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 6-14. All I^2C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the controller makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 6-15. All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in Figure 6-13. When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high, as shown in Figure 6-14. This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

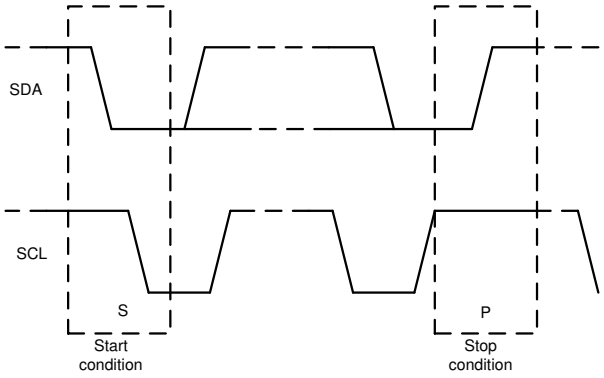


Figure 6-14. Start and Stop Conditions

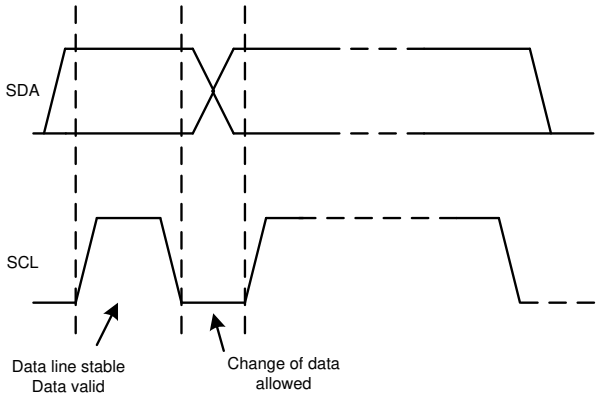


Figure 6-15. Bit Transfer on the I^2C Bus

6.5.2.2 I²C Update Sequence

For a single update, the DAC539E4W requires a start condition, a valid I²C address byte, a command byte, and two data bytes, as listed in Table 6-10.

Table 6-10. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 6.5.2.2.1				Command byte Section 6.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the DAC539E4W acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 6-16. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the DAC539E4W.

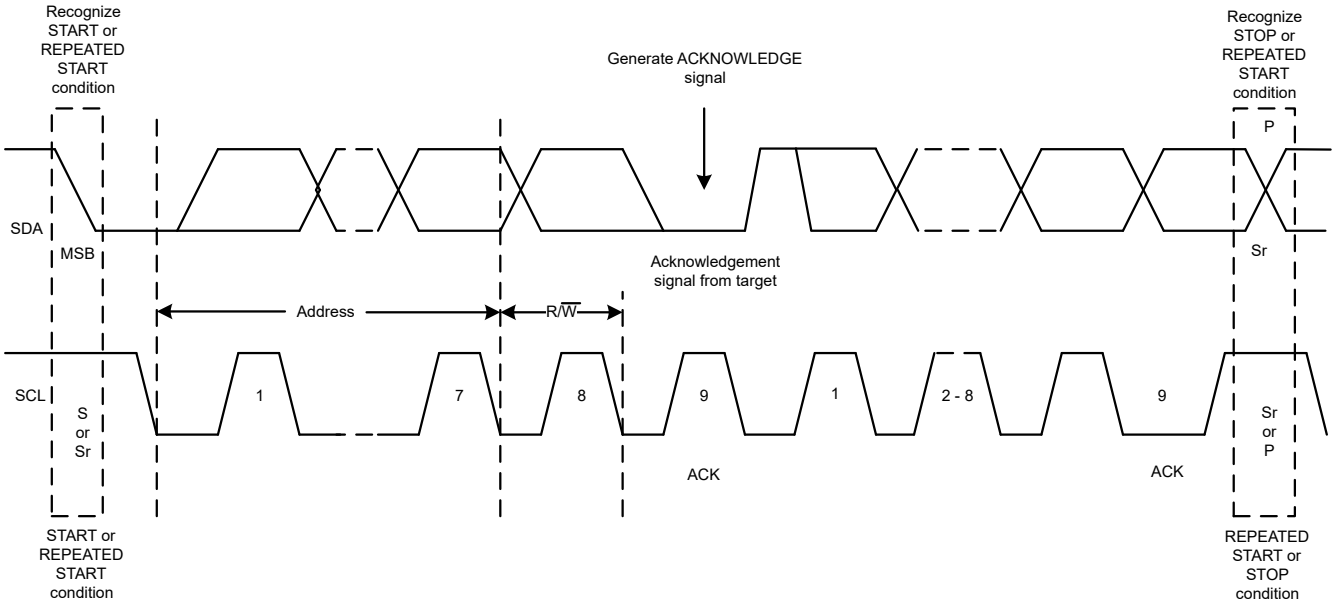


Figure 6-16. I²C Bus Protocol

The command byte sets the operating mode of the selected DAC539E4W device. For a data update to occur when the operating mode is selected by this byte, the DAC539E4W device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The DAC539E4W device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the DAC539E4W device releases the I²C bus and awaits a new start condition.

6.5.2.2.1 Address Byte

The address byte, as shown in Table 6-11, is the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001b. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to Table 6-12.

Table 6-11. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/$\overline{W}$
General address	1	0	0	1	See Table 6-12 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

Table 6-12. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The DAC539E4W supports broadcast addressing, which is used for synchronously updating or powering down multiple DAC539E4W devices. When the broadcast address is used, the DAC539E4W responds regardless of the address pin state. Broadcast is supported only in write mode.

6.5.2.2.2 Command Byte

The *Register Names* table in the *Register Map* section lists the command byte in the ADDRESS column.

6.5.2.3 I²C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/$\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/$\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

Table 6-13. Read Sequence

S	MSB	…	R/$\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/$\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	ADDRESS BYTE Section 6.5.2.2.1				COMMAND BYTE Section 6.5.2.2.2				Sr	ADDRESS BYTE Section 6.5.2.2.1				MSDB				LSDB			
From Controller				Target	From Controller			Target	From Controller				Target	From Target			Controller	From Target			Controller

6.6 Register Maps

Table 6-14. Register Map

REGISTER	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
DAC-x-MARGIN-HIGH	DAC-x-MARGIN-HIGH												X			
DAC-x-MARGIN-LOW	DAC-x-MARGIN-LOW												X			
DAC-x-VOUT-CMP-CONFIG	X			VOUT-GAIN-x			X					CMP-x-OD-EN	CMP-x-OUT-EN	CMP-x-HIZ-IN-DIS	CMP-x-INV-EN	CMP-x-EN
DAC-x-CMP-MODE-CONFIG	X				CMP-x-MODE		X									
COMMON-CONFIG	RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-3		RESERVED	VOUT-PDN-2		RESERVED	VOUT-PDN-1		RESERVED	VOUT-PDN-0		RESERVED
COMMON-TRIGGER	DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
COMMON-DAC-TRIG	RST-CMP-FLAG-0	RESERVED			RST-CMP-FLAG-1	RESERVED			RST-CMP-FLAG-2	RESERVED			RST-CMP-FLAG-3	RESERVED		
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-3-BUSY	DAC-2-BUSY	DAC-1-BUSY	DAC-0-BUSY	NVM-BUSY	DEVICE-ID						VERSION-ID	
CMP-STATUS	X												CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0
DEVICE-MODE-CONFIG	RESERVED		DIS-MODE-IN	RESERVED								X				
INTERFACE-CONFIG	X			TIMEOUT-EN	X									FSDO-EN	X	SDO-EN
STATE-MACHINE-CONFIG0	RESERVED													SM-ABORT	SM-START	SM-EN
SRAM-CONFIG	X								SRAM-ADDR							
SRAM-DATA	SRAM-DATA															
DAC-x-DATA	DAC-x-DATA												X			
LUT-x-DATA	RESERVED												LUT-x-DATA			
LOOP-WAIT	RESERVED											LOOP-WAIT				

Note: Shaded cells indicate the register bits or fields that are stored in NVM.

Note: X = Don't care.

Table 6-15. Register Names

I²C/SPI ADDRESS	SRAM ADDRESS	REGISTER NAME	SECTION
00h	—	NOP	Section 6.6.1
01h	—	DAC-0-MARGIN-HIGH	Section 6.6.2
02h	—	DAC-0-MARGIN_LOW	Section 6.6.3
03h	—	DAC-0-VOUT-CMP-CONFIG	Section 6.6.4
05h	—	DAC-0-CMP-MODE-CONFIG	Section 6.6.5
07h	—	DAC-1-MARGIN-HIGH	Section 6.6.2
08h	—	DAC-1-MARGIN_LOW	Section 6.6.3
09h	—	DAC-1-VOUT-CMP-CONFIG	Section 6.6.4
0Bh	—	DAC-1-CMP-MODE-CONFIG	Section 6.6.5
0Dh	—	DAC-2-MARGIN-HIGH	Section 6.6.2
0Eh	—	DAC-2-MARGIN_LOW	Section 6.6.3
0Fh	—	DAC-2-VOUT-CMP-CONFIG	Section 6.6.4
11h	—	DAC-2-CMP-MODE-CONFIG	Section 6.6.5
13h	—	DAC-3-MARGIN-HIGH	Section 6.6.2
14h	—	DAC-3-MARGIN_LOW	Section 6.6.3
15h	—	DAC-3-VOUT-CMP-CONFIG	Section 6.6.4
17h	—	DAC-3-CMP-MODE-CONFIG	Section 6.6.5
1Fh	—	COMMON-CONFIG	Section 6.6.6
20h	—	COMMON-TRIGGER	Section 6.6.7
21h	—	COMMON-DAC-TRIG	Section 6.6.8
22h	—	GENERAL-STATUS	Section 6.6.9
23h	—	CMP-STATUS	Section 6.6.10
25h	—	DEVICE-MODE-CONFIG	Section 6.6.11
26h	—	INTERFACE-CONFIG	Section 6.6.12
27h	—	STATE-MACHINE-CONFIG0	Section 6.6.13
2Bh	—	SRAM-CONFIG	Section 6.6.14
2Ch	—	SRAM-DATA	Section 6.6.15
—	0x21	DAC-0-DATA	Section 6.6.16
—	0x22	DAC-1-DATA	Section 6.6.16
—	0x23	DAC-2-DATA	Section 6.6.16
—	0x24	DAC-3-DATA	Section 6.6.16
—	0x25	LUT-0-DATA	Section 6.6.17

Table 6-15. Register Names (continued)

I²C/SPI ADDRESS	SRAM ADDRESS	REGISTER NAME	SECTION
—	0x26	LUT-1-DATA	Section 6.6.17
—	0x27	LUT-2-DATA	Section 6.6.17
—	0x28	LUT-3-DATA	Section 6.6.17
—	0x29	LUT-4-DATA	Section 6.6.17
—	0x2A	LUT-5-DATA	Section 6.6.17
—	0x2B	LUT-6-DATA	Section 6.6.17
—	0x2C	LUT-7-DATA	Section 6.6.17
—	0x2D	LUT-8-DATA	Section 6.6.17
—	0x2E	LUT-9-DATA	Section 6.6.17
—	0x2F	LUT-10-DATA	Section 6.6.17
—	0x30	LUT-11-DATA	Section 6.6.17
—	0x31	LUT-12-DATA	Section 6.6.17
—	0x32	LUT-13-DATA	Section 6.6.17
—	0x33	LUT-14-DATA	Section 6.6.17
—	0x34	LUT-15-DATA	Section 6.6.17
—	0x35	LOOP-WAIT	Section 6.6.18

6.6.1 NOP Register (address = 00h) [reset = 0000h]

Figure 6-17. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R/W-0h															

Table 6-16. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R/W	0000h	No operation

6.6.2 DAC-x-MARGIN-HIGH Register (address = 01h, 07h, 0Dh, 13h) [reset = 0000h]

Figure 6-18. DAC-x-MARGIN-HIGH Register (x = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-x-MARGIN-HIGH[9:0]												X			
R/W-0h												X-0h			

Table 6-17. DAC-x-MARGIN-HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-x-MARGIN-HIGH[9:0]	R/W	000h	Margin-high code for threshold DAC. Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: {DAC-x-MARGIN-HIGH[9:0], X, X} X = Don't care bits.
3-0	X	X	0	Don't care

6.6.3 DAC-x-MARGIN-LOW Register (address = 02h, 08h, 0Eh, 14h) [reset = 0000h]

Figure 6-19. DAC-x-MARGIN-LOW Register (x = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-x-MARGIN-LOW[9:0]												X			
R/W-0h												X-0h			

Table 6-18. DAC-x-MARGIN-LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-x-MARGIN-LOW[9:0]	R/W	000h	Margin-low code for threshold DAC. Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: {DAC-x-MARGIN-LOW[9:0], X, X} X = Don't care bits.
3-0	X	X	0	Don't care

6.6.4 DAC-x-VOUT-CMP-CONFIG Register (address = 03h, 09h, 0Fh, 15h) [reset = 0401h]

Figure 6-20. DAC-x-VOUT-CMP-CONFIG Register (x = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			VOUT-GAIN-x			X					CMP-x-OD-EN	CMP-x-OUT-EN	CMP-x-HIZ-IN-DIS	CMP-x-INV-EN	CMP-x-EN
X-0h			R/W-001			X-0h					R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1

Table 6-19. DAC-X-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12-10	VOUT-GAIN-x	R/W	001	000: Gain = 1 ×, external reference on MODE pin. 001: Gain = 1 ×, VDD as reference. 010: Gain = 1.5 ×, internal reference. 011: Gain = 2 ×, internal reference. 100: Gain = 3 ×, internal reference. 101: Gain = 4 ×, internal reference. Others: NA.
9-5	X	X	0h	Don't care.
4	CMP-x-OD-EN	R/W	0	1: Set OUTx pin as open-drain in comparator mode (CMP-x-EN = 1 and CMP-x-OUT-EN = 1). 0: Set OUTx pin as push-pull.
3	CMP-x-OUT-EN	R/W	0	1: Bring comparator output to the respective OUTx pin. 0: Generate comparator output but consume internally.
2	CMP-x-HIZ-IN-DIS	R/W	0	0: AINx input has high-impedance. Input voltage range is limited. 1: AINx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-x-INV-EN	R/W	0	1: Invert the comparator output. 0: Don't invert the comparator output.
0	CMP-x-EN	R/W	1	1: Enable comparator. 0: Disable comparator.

6.6.5 DAC-x-CMP-MODE-CONFIG Register (address = 05h, 0Bh, 11h, 17h) [reset = 0000h]

Figure 6-21. DAC-x-CMP-MODE-CONFIG Register (x = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				CMP-x-MODE		X									
X-0h				R/W-0h		X-0h									

Table 6-20. DAC-x-CMP-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	00h	Don't care.
11-10	CMP-x-MODE	R/W	00	00: No hysteresis function. 01: Hysteresis provided using DAC-x-MARGIN-HIGH and DAC-x-MARGIN-LOW registers. Others: Invalid setting.
9-0	X	X	000h	Don't care.

6.6.6 COMMON-CONFIG Register (address = 1Fh) [reset = 1249h]

Figure 6-22. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-3		RESERVED	VOUT-PDN-2		RESERVED	VOUT-PDN-1		RESERVED	VOUT-PDN-0		RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h

Table 6-21. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0	Always write 0.
14	DEV-LOCK	R/W	0	0: Device not locked 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	RESERVED	R/W	0	Always write 0.
12	EN-INT-REF	R/W	000	0: Disable internal reference 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10, 8-7, 5-4, 2-1	VOUT-PDN-x	R/W	00	00: Power-up VOUT-x. 01: Power-down VOUT-x with 10 KΩ to AGND. 10: Power-down VOUT-x with 100 KΩ to AGND. 11: Power-down VOUT-x with Hi-Z to AGND.
9, 6, 3, 0	RESERVED	R/W	1	Always write 1.

6.6.7 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

Figure 6-23. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
R/W-0h				R/W-0h				R/W-0h						R/W-0h	R/W-0h

Table 6-22. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0000	0101: Device unlocking password. Others: Don't care.
11-8	RESET	W	0000	1010: POR reset triggered. This field is self-resetting. Others: Don't care.
7-2	RESERVED	R/W	0	Always write 0.
1	NVM-PROG	R/W	0	0: NVM write not triggered. 1: NVM write triggered. This bit is self-resetting.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered. 1: Reload data from NVM to register map. This bit is self-resetting.

6.6.8 COMMON-DAC-TRIG Register (address = 21h) [reset = 0000h]

Figure 6-24. COMMON-DAC-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST-CMP-FLAG-0	RESERVED			RST-CMP-FLAG-1	RESERVED			RST-CMP-FLAG-2	RESERVED			RST-CMP-FLAG-3	RESERVED		
W-0h	W-0h			W-0h	W-0h			W-0h	W-0h			W-0h	W-0h		

Table 6-23. COMMON-DAC-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15, 11, 7, 3	RST-CMP-FLAG-x	W	0	0: Latching-comparator output unaffected. 1: Reset latching-comparator output. This bit is self-resetting.
14, 13, 10, 9, 8, 6, 5, 4, 2, 1, 0	RESERVED	W	0	Always write 0.

6.6.9 GENERAL-STATUS Register (address = 22h) [reset = 00h, DEVICE-ID, VERSION-ID]

Figure 6-25. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-3-BUSY	DAC-2-BUSY	DAC-1-BUSY	DAC-0-BUSY	NVM-BUSY	DEVICE-ID						VERSION-ID	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R						R-0h	

Table 6-24. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this temporary error condition.
13	X	R	0	Don't care
12	DAC-3-BUSY	R	0	0: DAC-3 channel can accept commands 1: DAC-3 channel does not accept commands
11	DAC-2-BUSY	R	0	0: DAC-2 channel can accept commands 1: DAC-2 channel does not accept commands
10	DAC-1-BUSY	R	0	0: DAC-1 channel can accept commands 1: DAC-1 channel does not accept commands
9	DAC-0-BUSY	R	0	0: DAC-0 channel can accept commands 1: DAC-0 channel does not accept commands
8	NVM-BUSY	R	0	0: NVM is available for read and write. 1: NVM is not available for read or write.
7-2	DEVICE-ID	R	DAC539E4W: 1Bh	Device identifier.
1-0	VERSION-ID	R	00	Version identifier.

6.6.10 CMP-STATUS Register (address = 23h) [reset = 0000h]

Figure 6-26. CMP-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X												CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0
X-0h												R-0h	R-0h	R-0h	R-0h

Table 6-25. CMP-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	X	X	0	Don't care.
3, 2, 1, 0	CMP-FLAG-x	R	0	Synchronized comparator output from respective channels.

6.6.11 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 8040h]

Figure 6-27. DEVICE-MODE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DIS-MODE-IN	RESERVED										X		
R/W-10		R/W-0h	R/W-02h										X-0h		

Table 6-26. DEVICE-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	10	Always write 10b
13	DIS-MODE-IN	R/W	0	0: MODE function enabled. 1: MODE function disabled.
12-5	RESERVED	R/W	02h	Always write 02h.
4-0	X	R/W	00h	Don't care.

6.6.12 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

Figure 6-28. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			TIMEOUT-EN	X									FSDO-EN	X	SDO-EN
X-0h			R/W-0h	X-0h									R/W-0h	X-0h	R/W-0h

Table 6-27. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12	TIMEOUT-EN	R/W	0	0: I^2C timeout disabled. 1: I^2C timeout enabled.
11-3	X	X	0h	Don't care.
2	FSDO-EN	R/W	0	0: Fast SDO disabled. 1: Fast SDO enabled.
1	X	X	0	Don't care.
0	SDO-EN	R/W	0	0: SDO disabled. 1: SDO enabled.

6.6.13 STATE-MACHINE-CONFIG0 Register (address = 27h) [reset = 0003h]

Figure 6-29. STATE-MACHINE-CONFIG0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SM-ABORT	SM-START	SM-EN
R/W-0h													R/W-0h	R/W-0h	R/W-0h

Table 6-28. STATE-MACHINE-CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0000h	Always write 0.
2	SM-ABORT	R/W	0	0: State machine not aborted. 1: State machine aborted.
1	SM-START	R/W	0	0: State machine stopped. 1: State machine started. The state machine must be enabled using the SM-EN bit.
0	SM-EN	R/W	0	0: State machine disabled. 1: State machine enabled.

6.6.14 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

Figure 6-30. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/W-00h							

Table 6-29. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care.
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

6.6.15 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

Figure 6-31. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/W-0h															

Table 6-30. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0h	16-bit SRAM data. This data is written to or read from the address configured in the SRAM-CONFIG register.

6.6.16 DAC-x-DATA Register (SRAM address = 21h, 22h, 23h, 24h) [reset = 8000h]

Note

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

Figure 6-32. DAC-x-DATA Register (x = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-x-DATA[9:0]												X			
R/W-800h												X-0h			

Table 6-31. DAC-x-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-x-DATA[9:0]	R/W	800h	Data for threshold DAC Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: {DAC-x-DATA[9:0], X, X} X = Don't care bits.
3-0	X	X	0h	Don't care.

6.6.17 LUT-x-DATA Register (SRAM address = 25h through 34h) [reset = (see register description)]

Note

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

Figure 6-33. LUT-x-DATA Register (x = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 12, 13, 14, 15)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												LUT-x-DATA			
R/W-0h												R/W			

Table 6-32. LUT-X-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	000h	Always write 000h.
3-0	LUT-0-DATA	R/W	0h	Look-up table data 0.
3-0	LUT-1-DATA	R/W	1h	Look-up table data 1.
3-0	LUT-2-DATA	R/W	2h	Look-up table data 2.
3-0	LUT-3-DATA	R/W	3h	Look-up table data 3.
3-0	LUT-4-DATA	R/W	4h	Look-up table data 4.
3-0	LUT-5-DATA	R/W	5h	Look-up table data 5.
3-0	LUT-6-DATA	R/W	6h	Look-up table data 6.
3-0	LUT-7-DATA	R/W	7h	Look-up table data 7.
3-0	LUT-8-DATA	R/W	8h	Look-up table data 8.
3-0	LUT-9-DATA	R/W	9h	Look-up table data 9.
3-0	LUT-10-DATA	R/W	Ah	Look-up table data 10.
3-0	LUT-11-DATA	R/W	Bh	Look-up table data 11.
3-0	LUT-12-DATA	R/W	Ch	Look-up table data 12.
3-0	LUT-13-DATA	R/W	Dh	Look-up table data 13.
3-0	LUT-14-DATA	R/W	Eh	Look-up table data 14.
3-0	LUT-15-DATA	R/W	Fh	Look-up table data 15.

6.6.18 LOOP-WAIT Register (SRAM address = 35h) [reset = 0000h]

Note

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

Figure 6-34. LOOP-WAIT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											LOOP-REFRESH				
R/W-000h											R/W-00h				

Table 6-33. LOOP-WAIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	000h	Always write 000h.
4-0	LOOP-REFRESH	R/W	00h	Additional delay between the comparator output and the GPO change, as calculated by Equation 4 in seconds.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The DAC539E4W is a quad-channel, buffered, force-sense output, voltage-output smart DAC that includes an NVM and internal reference, and is available in a tiny 1.76-mm × 1.76-mm package. The device is configured as an application-specific, LUT based standalone fault-management controller. The four DAC channels are configured as programmable comparators (CMPx), each with an independently configured 10-bit threshold. The four comparator outputs control an internal LUT to configure four GPOs. The LUT values and comparator thresholds are programed using I^2C or SPI and stored in the NVM. The GPOs are multiplexed with the digital communication pins. The MODE pin determines whether the device is in programming or standalone mode.

7.2 Typical Application

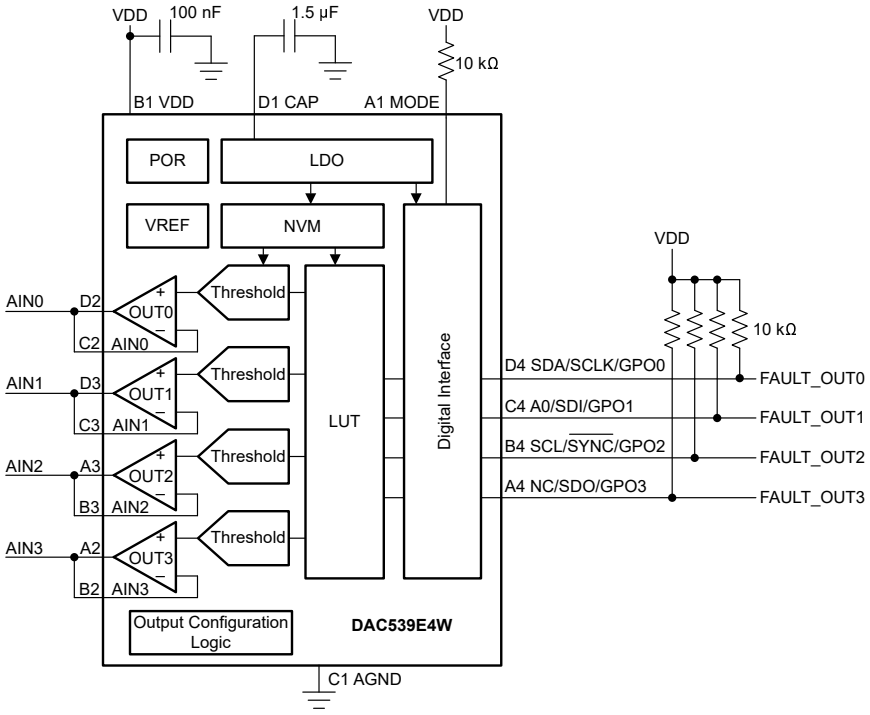


Figure 7-1. LUT-Based Standalone Fault-Management Circuit

This design uses the DAC539E4W to monitor four analog input voltages and output a 4-bit fault code on the GPO pins based on a 16-position LUT. The DAC539E4W output buffers have an exposed feedback path through the analog input (AINx) pins which act as the voltage input to the comparators. The DAC outputs are connected to the non-inverting inputs of the output buffers and set the user programmable comparator thresholds. Use this circuit to communicate faults in applications such as cordless power tools, vacuum robots, air purifiers, and humidifiers. Figure 7-1 shows an example schematic for this application. This schematic connects the AINx and OUTx pins so that the layout can be routed as shown in Figure 7-3. This layout strategy removes the need for vias-in-pad and a multilayer board, thereby reducing manufacturing costs; an excellent feature for cost-sensitive applications.

7.2.1 Design Requirements

Table 7-1. Design Parameters

PARAMETER	VALUE
Threshold 0	1 V
Threshold 1	2 V
Threshold 2	3 V
Threshold 3	4 V
Loop refresh	41 ms
Fault outputs	See look-up table (Table 7-3)

7.2.2 Detailed Design Procedure

The GPO pins are open drain outputs. These pins must be pulled up to the desired IO voltage using external resistors.

This example connects the AINx and OUTx pins to simplify routing. The OUTx pins must be disabled as the comparator outputs by setting the CMP-x-OUT-EN bit to 0 in the DAC-x-VOUT-CMP-CONFIG register, which is the default setting.

Use Equation 5 to calculate the threshold codes stored in DAC-x-DATA.

$$\text{THRESHOLD} = \frac{V_{THLD} \times 2^{N}}{V_{REF} \times \text{GAIN}} \tag{5}$$

The DAC539E4W is a 10-bit device, which means the maximum DAC code is 1023d. For a 1-V V_{THLD}, DAC-0-DATA is calculated by Equation 6.

$$\text{THRESHOLD} = \frac{1\,\text{V} \times 2^{10}}{5\,\text{V}} = 204.8\text{d} \tag{6}$$

This result is rounded up to 205d (0x0CD). Table 7-2 lists the codes for the remaining threshold values.

Table 7-2. Threshold Codes

THRESHOLD VOLTAGE	DAC-x-DATA[9:0]
1 V	0x0CD
2 V	0x19A
3 V	0x266
4 V	0x333

The AINx inputs are connected to the inverting input of the output buffer, and the threshold voltage is connected to the non-inverting input. By default, the comparator output is high when the voltage on AINx is lower than the threshold voltage. This example inverts the comparator outputs by setting the CMP-x-INV-EN bit in the DAC-x-VOUT-CMP-CONFIG register to 1.

By default the AINx inputs are high-impedance and the input voltage range is limited. This example sets the CMP-x-HIZ-IN-DIS bit in the DAC-x-VOUT-CMP-CONFIG register to 1 to connect the AINx inputs to a finite impedance. The input voltage range is 0 to V_{REF}×Gain.

Table 6-1 shows the LUT configuration used in this example. This example application uses four different error codes, including 0b0000 representing no error. When the CMP0 and CMP1 outputs are high, the GPOs output 0b0011. When CMP2 is high, the GPOs output 0b0100. When all comparator outputs are high, the GPOs output 0b1111. All other conditions output 0b0000. Table 7-3 shows the LUT settings for this example.

Table 7-3. Comparator Input to GPO LUT

COMPARATOR OUTPUT STATUS CMP3, CMP2, CMP1, CMP0	OUTPUTS GPO3, GPO2, GPO1, GPO0
0b0000	LUT-0-DATA: 0b0000
0b0001	LUT-1-DATA: 0b0000
0b0010	LUT-2-DATA: 0b0000
0b0011	LUT-3-DATA: 0b0011
0b0100	LUT-4-DATA: 0b0100
0b0101	LUT-5-DATA: 0b0100
0b0110	LUT-6-DATA: 0b0100
0b0111	LUT-7-DATA: 0b0100
0b1000	LUT-8-DATA: 0b0000
0b1001	LUT-9-DATA: 0b0000
0b1010	LUT-10-DATA: 0b0000
0b1011	LUT-11-DATA: 0b0000
0b1100	LUT-12-DATA: 0b0100
0b1101	LUT-13-DATA: 0b0100
0b1110	LUT-14-DATA: 0b0100
0b1111	LUT-15-DATA: 0b1111

The CMPx outputs are read and the GPOs updated in a continuous loop. A loop refresh delay can be used to decrease the frequency of the loop to avoid any switching noise on the outputs as the voltage on the AINx pins settle. The timer is 5 bits and is stored in the LOOP-WAIT SRAM register. Use Equation 4 to calculate the delay. Set the LOOP-REFRESH code to 19d for a 41-ms delay.

Follow these guidelines to set up the registers on the DAC539E4W:

- Stop the state machine before updating the application parameters by writing 0 to the STATE-MACHINE-CONFIG0 register.
- Set all of the application parameters shown in Table 7-4. These locations must be used to save the settings in the NVM.
- LUT locations LUT-0-DATA, LUT-1-DATA, and LUT-15-DATA correspond to CMP3, CMP2, CMP1, and CMP0 equaling 0b0000, 0b0001, and 0b1111, respectively.
- Configure the reference for all channels in the DAC-x-VOUT-CMP-CONFIG register. Configure each channel to operate in comparator mode by setting the CMP-x-EN bit to 1 in the same register.
- Power on the comparator outputs using the COMMON-CONFIG register.
- Set the DEVICE-MODE-CONFIG register to 0x8040.
- Start the state machine by writing 0003h to the STATE-MACHINE-CONFIG0.
- Trigger an NVM write by setting the NVM-PROG bit in the COMMON-TRIGGER register (0x20) to 1.

Table 7-4. Application Parameters

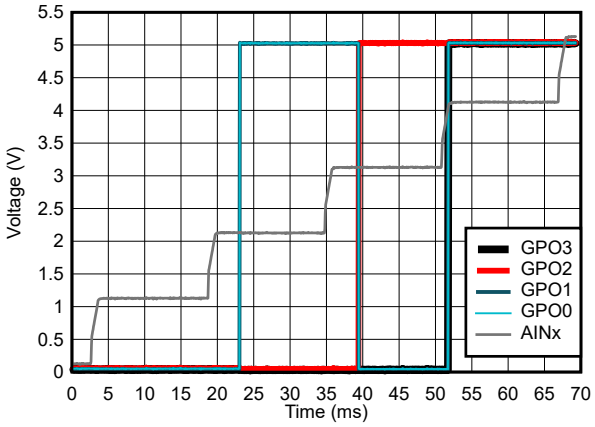
REGISTER NAME	ADDRESS [BITS]	ADDRESS LOCATION
DAC-0-DATA	0x21[15:6]	SRAM
DAC-1-DATA	0x22[15:6]	SRAM
DAC-2-DATA	0x23[15:0]	SRAM
DAC-3-DATA	0x24[15:6]	SRAM
LUT-0-DATA	0x25[3:0]	SRAM
LUT-1-DATA	0x26[3:0]	SRAM
LUT-2-DATA	0x27[3:0]	SRAM
LUT-3-DATA	0x28[3:0]	SRAM
LUT-4-DATA	0x29[3:0]	SRAM
LUT-5-DATA	0x2A[3:0]	SRAM
LUT-6-DATA	0x2B[3:0]	SRAM
LUT-7-DATA	0x2C[3:0]	SRAM
LUT-8-DATA	0x2D[3:0]	SRAM
LUT-9-DATA	0x2E[3:0]	SRAM
LUT-10-DATA	0x2F[3:0]	SRAM
LUT-11-DATA	0x30[3:0]	SRAM
LUT-12-DATA	0x31[3:0]	SRAM
LUT-13-DATA	0x32[3:0]	SRAM
LUT-14-DATA	0x33[3:0]	SRAM
LUT-15-DATA	0x34[3:0]	SRAM
LOOP-WAIT	0x35[3:0]	SRAM
DAC-0-VOUT-CMP-CONFIG	0x03[12:10][4:0]	Register
DAC-1-VOUT-CMP-CONFIG	0x09[12:10][4:0]	Register
DAC-2-VOUT-CMP-CONFIG	0x0F[12:10][4:0]	Register
DAC-3-VOUT-CMP-CONFIG	0x15[12:10][4:0]	Register
COMMON-CONFIG	0x1F[15:0]	Register
DEVICE-MODE-CONFIG	0x25[15:0]	Register
STATE-MACHINE-CONFIG0	0x27[2:0]	Register

Only the bits listed in the address column of Table 7-4 are saved in NVM and used in the state machine. For example, only bits 12 to 10, and 4 to 0 are saved in NVM for the DAC-X-VOUT-CMP-CONFIG registers.

The pseudocode for this application example is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (REGISTER ADDRESS)>, <MSB DATA>, <LSB DATA>
//Pull MODE pin low to enter programming mode//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <MSB DATA>,
<LSB DATA>
//Stop the state machine
WRITE STATE-MACHINE-CONFIG(0x27), 0x00, 0x03
//Set the comparator thresholds
WRITE DAC-0-DATA(SRAM 0x21), 0x33, 0x40
WRITE DAC-1-DATA(SRAM 0x22), 0x66, 0x80
WRITE DAC-2-DATA(SRAM 0x23), 0x99, 0x80
WRITE DAC-3-DATA(SRAM 0x24), 0xCC, 0xC0
//Set the LUT values
WRITE LUT-0-DATA(SRAM 0x25), 0x00, 0x00
WRITE LUT-1-DATA(SRAM 0x26), 0x00, 0x00
WRITE LUT-2-DATA(SRAM 0x27), 0x00, 0x00
WRITE LUT-3-DATA(SRAM 0x28), 0x00, 0x03
WRITE LUT-4-DATA(SRAM 0x29), 0x00, 0x04
WRITE LUT-5-DATA(SRAM 0x2A), 0x00, 0x04
WRITE LUT-6-DATA(SRAM 0x2B), 0x00, 0x04
WRITE LUT-7-DATA(SRAM 0x2C), 0x00, 0x04
WRITE LUT-8-DATA(SRAM 0x2D), 0x00, 0x00
WRITE LUT-9-DATA(SRAM 0x2E), 0x00, 0x00
WRITE LUT-10-DATA(SRAM 0x2F), 0x00, 0x00
WRITE LUT-11-DATA(SRAM 0x30), 0x00, 0x03
WRITE LUT-12-DATA(SRAM 0x31), 0x00, 0x04
WRITE LUT-13-DATA(SRAM 0x32), 0x00, 0x04
WRITE LUT-14-DATA(SRAM 0x33), 0x00, 0x04
WRITE LUT-15-DATA(SRAM 0x34), 0x00, 0x0F
//Set the loop refresh setting for 41 ms
WRITE LOOP-WAIT(SRAM 0x35), 0x00, 0x13
//Set the channel 0 reference to VDD and enable comparator mode
WRITE DAC-0-VOUT-CMP-CONFIG(0x03), 0x04, 0x07
//Set channel 1 reference to VDD and enable comparator mode
WRITE DAC-1-VOUT-CMP-CONFIG(0x09), 0x04, 0x07
//Set channel 2 reference to VDD and enable comparator mode
WRITE DAC-2-VOUT-CMP-CONFIG(0x0F), 0x04, 0x07
//Set channel 3 reference to VDD and enable comparator mode
WRITE DAC-3-VOUT-CMP-CONFIG(0x15), 0x04, 0x07
//Power on the DAC channels
WRITE COMMON-CONFIG(0x1F), 0x02, 0x49
//Set the device mode (this is the device default)
WRITE DEVICE-MODE-CONFIG(0x25), 0x80, 0x40
//Start the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
//Pull the MODE pin high to enter standalone mode
```

7.2.3 Application Curve



AINx steps: 100 mV, 1.1 V, 2.1 V, 3.1 V, 4.1 V, and 5.1 V.

Figure 7-2. LUT Output

7.3 Power Supply Recommendations

The DAC539E4W family of devices does not require specific power-supply sequencing. These devices require a single power supply, V_{DD}. However, make sure the external voltage reference is applied after VDD. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 µF for the CAP pin.

7.4 Layout

7.4.1 Layout Guidelines

The DAC539E4W pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

7.4.2 Layout Example

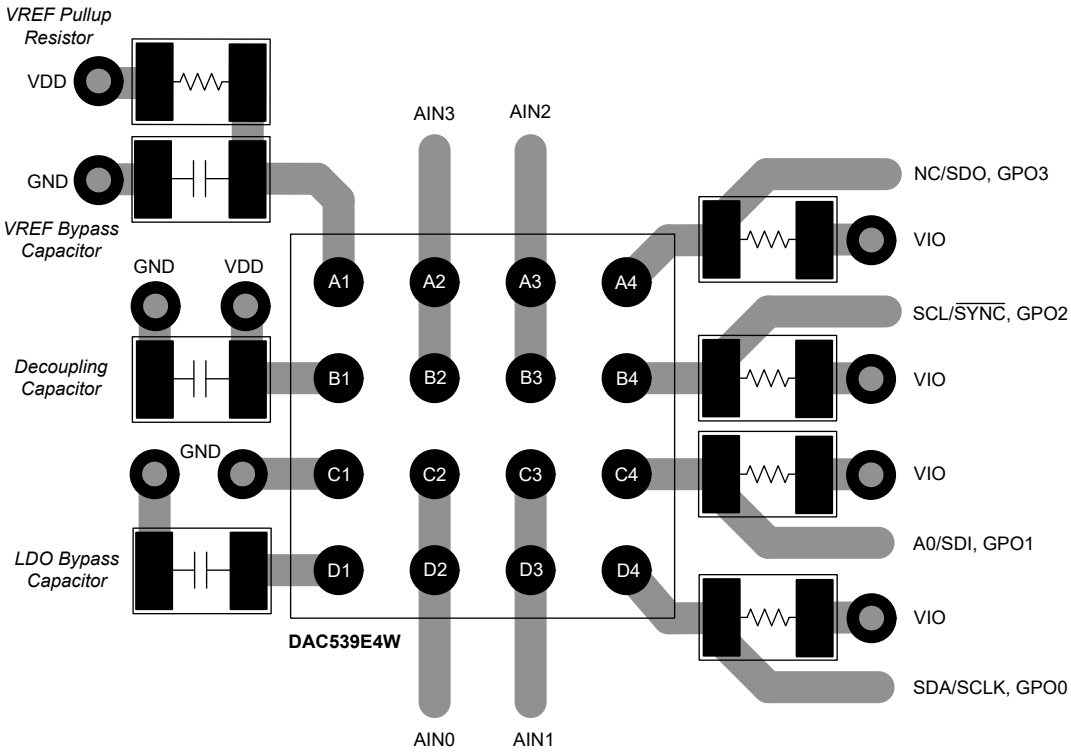


Figure 7-3. Layout Example

Note: The ground and power planes have been omitted for clarity.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2023) to Revision A (July 2025)	Page
• Changed package dimensions from 1.72mm × 1.72mm to 1.76mm × 1.76mm in last bullet in *Features*	1
• Changed package dimensions from 1.72mm × 1.72mm to 1.76mm × 1.76mm in *Package Information* table.	1
• Changed package dimensions from 1.75-mm × 1.75-mm to 1.76-mm × 1.76-mm in *Application Information*	46
• Updated YBH package outline with corrected dimensions	53

10 Mechanical, Packaging, and Orderable Information

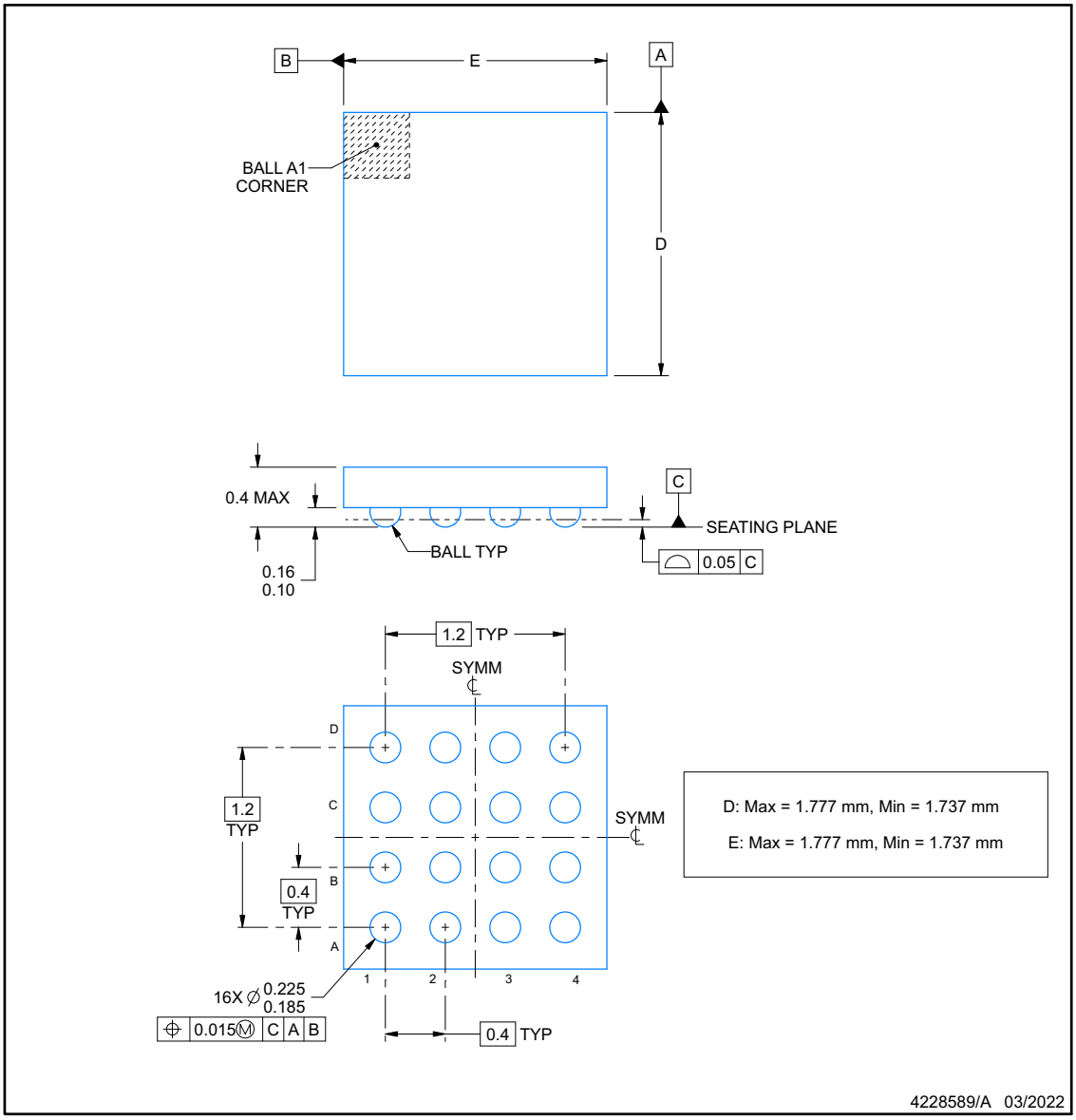
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YBH0016-C03

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

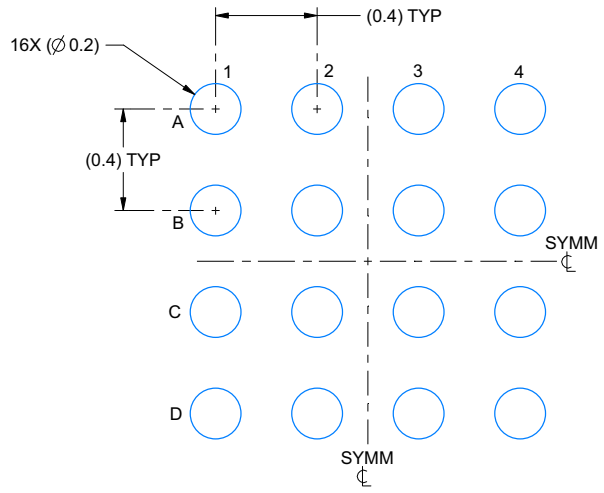
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

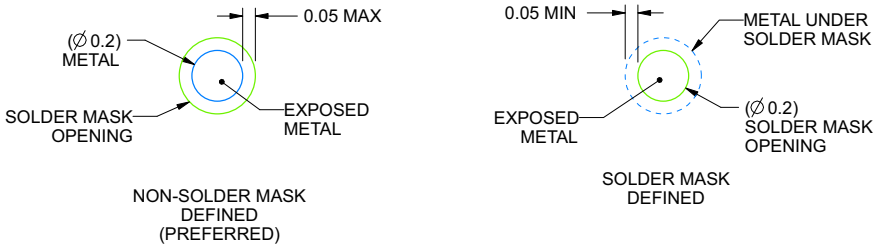
YBH0016-C03

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4228589/A 03/2022

NOTES: (continued)

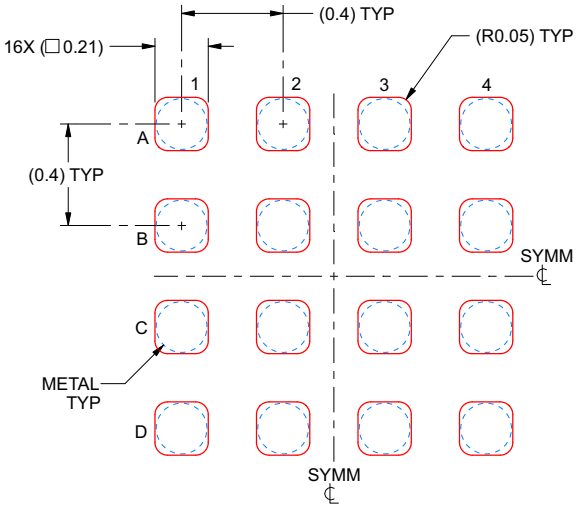
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBH0016-C03

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4228589/A 03/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC539E4YBHR	Active	Production	DSBGA (YBH) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DAC 539E4
DAC539E4YBHR.A	Active	Production	DSBGA (YBH) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DAC 539E4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

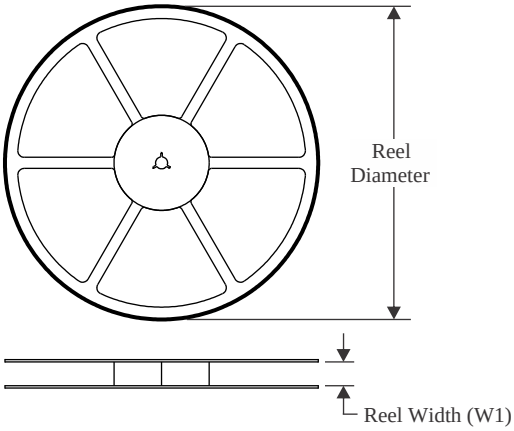
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

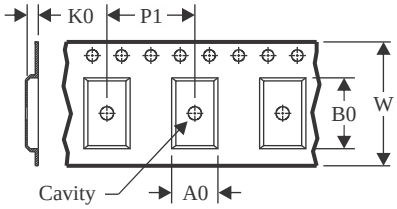
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

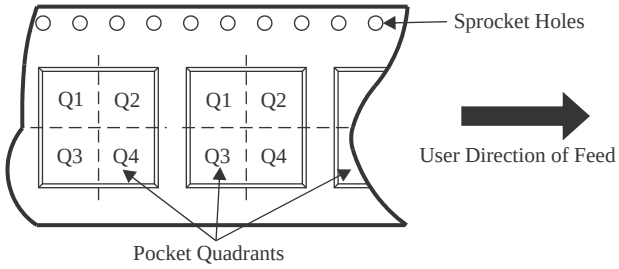


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

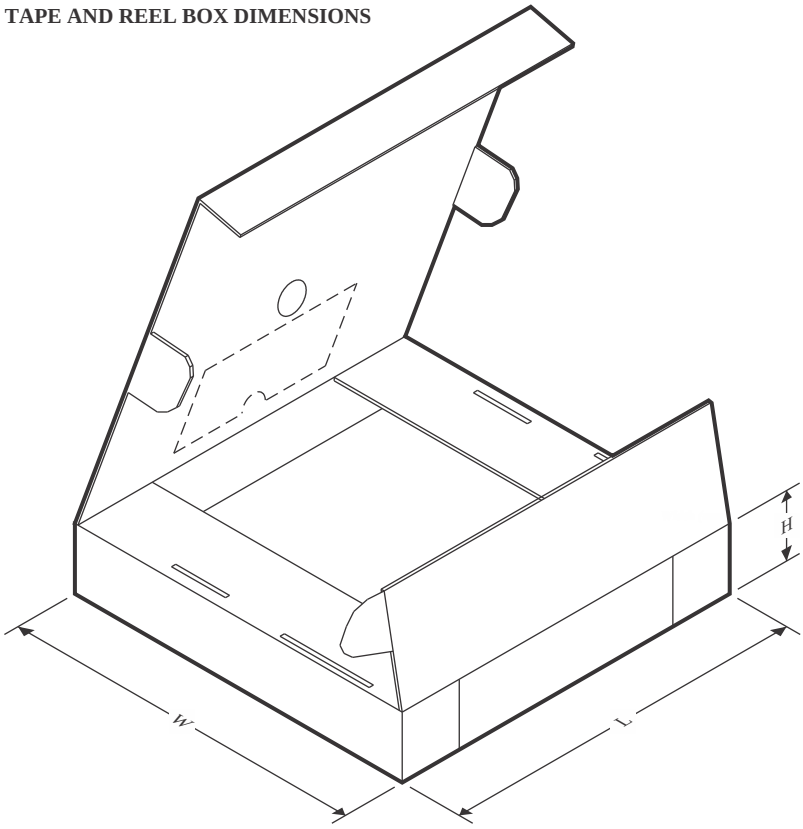
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC539E4YBHR	DSBGA	YBH	16	3000	180.0	8.4	1.94	1.94	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC539E4YBHR	DSBGA	YBH	16	3000	182.0	182.0	20.0

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