DAC39RF20: 22GSPS or 44GSPS, 16-bit, Single and Dual Channel, Multi-Nyquist Digital-to-Analog Converter (DAC) with JESD204C Interface

ADVANCE INFORMATION

1 Features

- 16-bit Multi-Nyquist DAC core
- DAC sample rate:
  - NRZ, RF Modes: 22GSPS
  - DES2xL, DES2xH modes: 44GSPS
- Maximum input data rate:
  - 12-bit, Dual channel: 21GSPS/ch
  - 16-bit, Dual channel: 15.75GSPS/ch
  - 16-bit, Single channel: 22GSPS
- Output frequency range: >18GHz
- Performance at f_{OUT} = 10GHz, DES2xL mode
  - Noise floor (small signal): –170dBFS/Hz
  - SFDR (-0.1dBFS) : –55dBc
  - IMD3 (-7dBFS each tone) : –60dBc
  - Additive phase noise, 10kHz offset: -132dBc/Hz
- Optional PLL/VCO for DAC clock generation
- Four integrated digital up-converters (DUC)
  - Interpolation: 1x, 4x, 6x, 8x to 256x
  - Complex baseband DUC for I/Q output
  - Complex to real upconversion for direct RF sampling
  - 64-bit frequency resolution NCOs
  - Phase continuous, synchronous and reset options with frequency hopping
- Programmable FIR equalizer at DUC input or DAC input
- Direct digital synthesis (DDS) functions
  - Four piecewise linear waveform generators
    - 16 Prestored waveforms
    - 256 Total vectors
    - Automatic or synchronous external triggers
  - Frequency, amplitude, phase interface streaming
- JESD204C Interface
  - 16 Lanes at up to 32.5Gbps
  - Class C-S, subclass-1 compatible
- Automatic clock and SYSREF calibration and tracking

2 Applications

- Satellite Communications (SATCOM)
- Phased Array Antenna Systems
- Synthetic Aperture Radar (SAR) Exciter
- Wireless Communications Testers
- Arbitrary Waveform Generator (AWG)

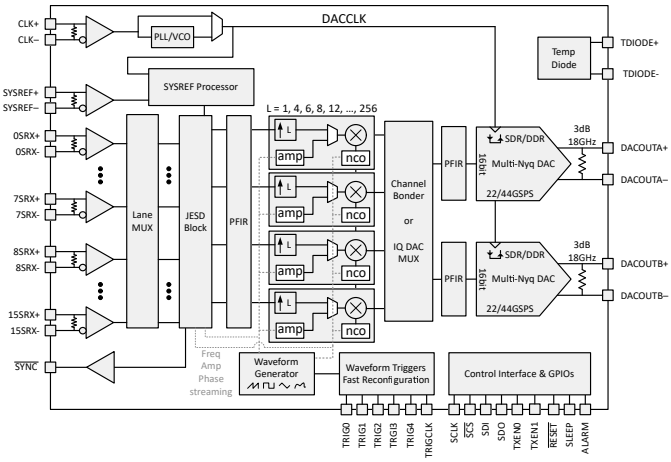
3 Description

The DAC39RF20 is a single and dual channel digital-to-analog converter (DAC) with 16-bit resolution. With an external full rate clock, the devices support 22GSPS with single edge sampling modes (NRZ and RF) and 44GSPS in dual edge sampling modes (DES2XL, DES2XH). When using the internal PLL/VCO, the devices support 17GSPS with single edge sampling modes (NRZ and RF) and 34GSPS in dual edge sampling modes (DES2XL, DES2XH). The devices can be used as noninterpolating or interpolating DACs for either direct RF sampling or complex baseband signal generation. The maximum input data rate for two channels is 21GSPS (12-bit resolution) or 15.75GSPS (16-bit resolution). The maximum rate for one channel is 22GSPS (16-bit resolution). The device can generate signals greater than 10GHz bandwidth at frequencies exceeding 20GHz, enabling direct sampling through Ku band.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DAC39RF20	FCCSP (289 balls)	13.8mm × 13.8mm, 0.8mm pitch

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

4 Device Comparison

Feature/Specification		DAC39RF20 Generation 1	DAC39RF2x Generation 2
PLL/VCO	F_{DACCLK}	8.125GHz ≤ F_{DACCLK} ≤ 17GHz	0.8GHz ≤ F_{DACCLK} ≤ 22GHz
	PLL Output Divider	1x only	1, 2, 4, 8 or 16x
	CPLL_MPY	8 to 99	6 to 256
	Phase Noise		5dB better between 100kHz≤F_{OFFSET}≤10MHz
	Multi-device Synchronization	No	Yes
SYSREF Windowing for F_{DACCLK}<10GHz		No	Yes
Timestamp Output		No	Yes
SPI readable temp sensor		No (temp diode is available)	Yes
SerDes Loss of Signal Detector		No	Yes
Maximum SPI Clock Frequency		15MHz	>50MHz (target)
DDS Streaming Trigger		AMP = 0	AMP = 0 and PHASE[0]=1
SOFT_RESET		does not properly clear registers in an address range of 0x0080 to 0x00FE. Use external $\overline{\text{RESET}}$.	Fixed
HD2			improved by 10 to 20dB

ADVANCE INFORMATION

Table of Contents

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Pin Configuration and Functions

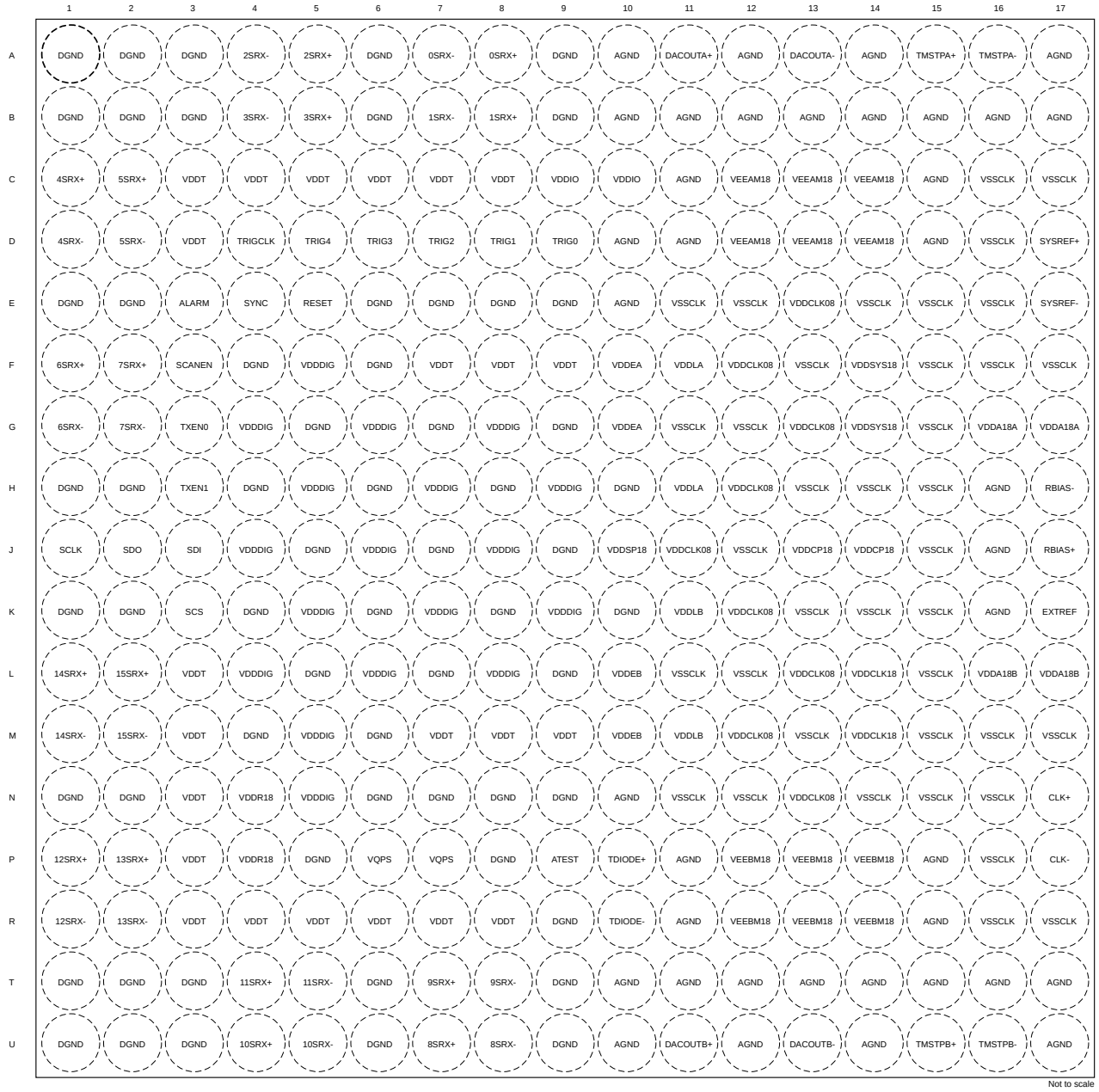


Figure 5-1. ANH0289A Package, 289-Ball Flip Chip CSP with 0.8mm pitch (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO		
DAC Outputs			
DACOUTA-	A13	O	DAC channel A analog output negative terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.
DACOUTA+	A11	O	DAC channel A analog output positive terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.
DACOUTB-	U13	O	DAC channel B analog output negative terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.
DACOUTB+	U11	O	DAC channel B analog output positive terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.
Differential Clock and SYSREF Inputs			
CLK-	P17	I	Device clock input negative terminal. There is an internal 100Ω differential termination between CLK+ and CLK–. This input is self-biased and should be AC coupled to the clock source.
CLK+	N17	I	Device clock input positive terminal. There is an internal 100Ω differential termination between CLK+ and CLK–. This input is self-biased and should be AC coupled to the clock source.
SYSREF-	E17	I	Differential JESD204C SYSREF input negative terminal. There is an internal 100Ω differential termination between SYSREF+ and SYSREF–. This input is self-biased if AC coupled. If DC coupled, the input common mode must meet the V_{CMI} specification in Recommended Operating Conditions.
SYSREF+	D17	I	Differential JESD204C SYSREF input negative terminal. There is an internal 100Ω differential termination between SYSREF+ and SYSREF–.
SerDes Interface			
0SRX-	A7	I	Serdes Lane 0 negative input. Includes 100Ω internal termination to 0SRX+.
0SRX+	A8	I	Serdes Lane 0 positive input. Includes 100Ω internal termination to 0SRX-.
1SRX-	B7	I	Serdes Lane 1 negative input. Includes 100Ω internal termination to 1SRX+.
1SRX+	B8	I	Serdes Lane 1 positive input. Includes 100Ω internal termination to 1SRX-.
2SRX-	A4	I	Serdes Lane 2 negative input. Includes 100Ω internal termination to 2SRX+.
2SRX+	A5	I	Serdes Lane 2 positive input. Includes 100Ω internal termination to 2SRX-.
3SRX-	B4	I	Serdes Lane 3 negative input. Includes 100Ω internal termination to 3SRX+.
3SRX+	B5	I	Serdes Lane 3 positive input. Includes 100Ω internal termination to 3SRX-.
4SRX-	D1	I	Serdes Lane 4 negative input. Includes 100Ω internal termination to 4SRX+.
4SRX+	C1	I	Serdes Lane 4 positive input. Includes 100Ω internal termination to 4SRX-.
5SRX-	D2	I	Serdes Lane 5 negative input. Includes 100Ω internal termination to 5SRX+.
5SRX+	C2	I	Serdes Lane 5 positive input. Includes 100Ω internal termination to 5SRX-.
6SRX-	G1	I	Serdes Lane 6 negative input. Includes 100Ω internal termination to 6SRX+.
6SRX+	F1	I	Serdes Lane 6 positive input. Includes 100Ω internal termination to 6SRX-.
7SRX-	G2	I	Serdes Lane 7 negative input. Includes 100Ω internal termination to 7SRX+.
7SRX+	F2	I	Serdes Lane 7 positive input. Includes 100Ω internal termination to 7SRX-.
8SRX-	U8	I	Serdes Lane 8 negative input. Includes 100Ω internal termination to 8SRX+.
8SRX+	U7	I	Serdes Lane 8 positive input. Includes 100Ω internal termination to 8SRX-.
9SRX-	T8	I	Serdes Lane 9 negative input. Includes 100Ω internal termination to 9SRX+.
9SRX+	T7	I	Serdes Lane 9 positive input. Includes 100Ω internal termination to 9SRX-.
10SRX-	U5	I	Serdes Lane 10 negative input. Includes 100Ω internal termination to 10SRX+.
10SRX+	U4	I	Serdes Lane 10 positive input. Includes 100Ω internal termination to 10SRX-.
11SRX-	T5	I	Serdes Lane 11 negative input. Includes 100Ω internal termination to 11SRX+.
11SRX+	T4	I	Serdes Lane 11 positive input. Includes 100Ω internal termination to 11SRX-.
12SRX-	R1	I	Serdes Lane 12 negative input. Includes 100Ω internal termination to 12SRX+.
12SRX+	P1	I	Serdes Lane 12 positive input. Includes 100Ω internal termination to 12SRX-.
13SRX-	R2	I	Serdes Lane 13 negative input. Includes 100Ω internal termination to 13SRX+.
13SRX+	P2	I	Serdes Lane 13 positive input. Includes 100Ω internal termination to 13SRX-.
14SRX-	M1	I	Serdes Lane 14 negative input. Includes 100Ω internal termination to 14SRX+.
14SRX+	L1	I	Serdes Lane 14 positive input. Includes 100Ω internal termination to 14SRX-.
15SRX-	M2	I	Serdes Lane 15 negative input. Includes 100Ω internal termination to 15SRX+.
15SRX+	L2	I	Serdes Lane 15 positive input. Includes 100Ω internal termination to 15SRX-.

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO		
GPIO Functions			
ALARM	E3	O	ALARM pin is asserted when an internal unmasked alarm is detected. Alarm mask is set by ALM_MASK register. No pullup or pulldown.
$\overline{\text{RESET}}$	E5	I	Device reset input, active low. Must be toggled after power up. Internal pullup.
SCANEN	F3	I	TI use only, can be left unconnected. Internal pulldown.
SCLK	J1	I	Serial programming interface (SPI) clock input. No pullup or pulldown.
$\overline{\text{SCS}}$	K3	I	Serial programming interface (SPI) device select input, active low. Internal pullup.
SDI	J3	I	Serial programming interface (SPI) data input. No pullup or pulldown.
SDO	J2	O	Serial programming interface (SPI) data output. High impedance when not reading out SPI data. No pullup or pulldown.
$\overline{\text{SYNC}}$	E4	I/O	JESD204C SYNC output, active low. Pullup active when used as an input.
TRIG0	D9	I	Trigger interface ball 0. Also used as data input 0 for FR Interface. Internal pulldown.
TRIG1	D8	I	Trigger interface ball 1. Also used as data input 1 for FR Interface. Internal pulldown.
TRIG2	D7	I	Trigger interface ball 2. Also used as data input 2 for FR Interface. Internal pulldown.
TRIG3	D6	I	Trigger interface ball 3. Also used as data input 3 for FR Interface. Internal pulldown.
TRIG4	D5	I	Trigger interface ball 4. Also used as chip select input for FR Interface. Internal pulldown.
TRIGCLK	D4	I/O	Trigger interface clock. Used as an input clock for FR Interface or output clock for trigger interface. Internal pulldown.
TXEN0	G3	I	Pin control for muting DAC outputs or entering APP Sleep (see TX_EN_SEL). See also Transmit Enables. Internal pullup.
TXEN1	H3	I	Pin control for muting DAC outputs or entering APP Sleep (see TX_EN_SEL). See also Transmit Enables. Internal pullup.
Analog functions			
ATEST	P9	O	Analog test pin. Can be left disconnected if not used.
EXTREF	K17	I/O	Reference voltage output or input, determined by the EXTREF_EN register field. If the internal reference is used, the ball should be tied through 0.1uF to AGND.
RBIAS-	H17	O	Full-scale output current bias is set by the resistor tied from this terminal to RBIAS+.
RBIAS+	J17	O	Full-scale output current bias is set by the resistor tied from this terminal to RBIAS-.
TDIODE+	P10	I	Temperature diode positive terminal (to be sensed by an external circuit)
TDIODE-	R10	I	Temperature diode negative terminal (to be sensed by an external circuit)
TMSTPA+	A15	O	Reserved.
TMSTPA-	A16	O	Reserved.
TMSTPB+	U15	O	Reserved.
TMSTPB-	U16	O	Reserved.
Power Supplies			
Note one low ESL 0.1µF decoupling capacitor per power supply pin is recommended			
VDDA18A	G16, G17	I	1.8V supply voltage for DAC channel A. Can be combined with VDDA18B, but may degrade channel-to-channel crosstalk (XTALK).
VDDA18B	L16, L17	I	1.8V supply voltage for DAC channel B. Can be combined with VDDA18A, but may degrade channel-to-channel crosstalk (XTALK).
VDDCLK08	J11, F12, H12, K12, M12, E13, G13, L13, N13	I	0.8V supply voltage for internal sampling clock distribution path. Noise or spurs on this supply may degrade phase noise performance. Recommended to separate from VDDDIG and VDDLA/B for best performance.
VDDCLK18	L14, M14	I	1.8V supply voltage for clock (CLK+/–) input buffer. Noise or spurs on this supply may degrade phase noise performance.
VDDCP18	J13, J14	I	Data converter PLL 1.8V supply.
VDDDIG	G4, J4, L4, F5, H5, K5, M5, N5, G6, J6, L6, H7, K7, G8, J8, L8, H9, K9	I	0.8V supply voltage for digital block. Recommended to separate from VDDLA/B and VDDCLK for best performance.
VDDEA	F10, G10	I	0.8V supply voltage for channel A DAC encoder. Recommended to separate from VDDDIG for best performance. Can be combined with VDDEB.

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO		
VDDEB	L10, M10	I	0.8V supply voltage for channel B DAC encoder. Recommended to separate from VDDDIG for best performance. Can be combined with VDDEA.
VDDIO	C9, C10	I	1.8V supply for CMOS input and output terminals.
VDDLA	F11, H11	I	0.8V supply for DAC analog latch for channel A. Separate from VDDLB for best channel-to-channel crosstalk (XTALK). Must be separated from VDDDIG for best performance.
VDDLB	K11, M11	I	0.8V supply for DAC analog latch for channel B. Separate from VDDLA for best channel-to-channel crosstalk (XTALK). Must be separated from VDDDIG for best performance.
VDDR18	N4, P4	I	1.8V Supply voltage for SerDes receivers.
VDDSP18	J10	I	Serdes PLL 1.8V supply.
VDDSYS18	F14, G14	I	1.8V supply voltage for SYSREF (SYSREF+/–) input buffer. Can be combined with VDDCLK18 when SYSREF is disabled during normal operation. This supply should be separate from VDDCLK18 when SYSREF is run continuously during operation to avoid noise and spur coupling and reduced phase noise performance.
VDDT	C3, D3, L3, M3, N3, P3, R3, C4, R4, C5, R5, C6, R6, C7, F7, M7, R7, C8, F8, M8, R8, F9, M9	I	0.8V Supply voltage for SerDes termination.
VEEAM18	C12, D12, C13, D13, C14, D14	I	–1.8V supply voltage for DAC current source bias for channel A. Can be combined with VEEBM18, but may degrade channel-to-channel crosstalk (XTALK).
VEEBM18	P12, R12, P13, R13, P14, R14	I	–1.8V supply voltage for DAC current source bias for channel B. Can be combined with VEEAM18, but may degrade channel-to-channel crosstalk (XTALK).
VQPS	P6, P7	I	TI use only. Can be tied to DGND during normal operation.
Grounds			
AGND	A10, B10, D10, E10, N10, T10, U10, B11, C11, D11, P11, R11, T11, B12, A12, T12, U12, B13, T13, A14, B14, T14, U14, B15, C15, D15, P15, R15, T15, B16, H16, J16, K16, T16, A17, B17, T17, U17	-	Analog ground.
DGND	A1, B1, E1, H1, K1, N1, T1, U1, A2, B2, E2, H2, K2, N2, T2, U2 , A3, B3, T3, U3, F4, H4, K4, M4, G5, J5, L5, P5, A6, B6, E6, F6, H6, K6, M6, N6, T6, U6, E7, G7, J7, L7, N7, E8, H8, K8, N8 , P8, A9, B9, E9, G9, J9, L9, N9, R9, T9, U9, H10, K10	-	Digital ground.
VSSCLK	E11, G11, L11, N11, E12, G12, J12, L12, N12, F13, H13, K13, M13, E14, H14, K14, N14, E15, F15, G15, H15, J15, K15, L15, M15, N15, C16, D16, E16, F16, M16, N16, P16, R16, C17, F17, M17, R17	-	Clock ground.

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range	Supply voltage range, VDDA18A, VDDA18B(2)	-0.3	2.45	V
	Supply voltage range, VEEAM18, VEEBM18(2)	-2.0	0.3	V
	Supply voltage range, VDDCLK18, VDDSYS18, VDDSP18, VDDCP18(3)	-0.3	2.45	V
	Supply voltage range, VDDLB, VDDLA, VDDCLK08(3)	-0.3	1.0	V
	Supply voltage range, VDDIO, VQPS, VDDR18(4)	-0.3	2.45	V
	Supply voltage range, VDDDIG, VDDEB, VDDEA, VDDT(4)	-0.3	1.0	V
Voltage between any combination of AGND, DGND and VSSCLK	Voltage between any combination of AGND, DGND and VSSCLK	-0.1	0.1	V
Voltage applied to input pins	CLK+, CLK–(3)	-0.3	VDDCLK18+0.3	V
	SYSREF+, SYSREF-(3)	-0.3	VDDSYS18+0.3	
	[0:15]SRX-/+(4)	-0.3	VDDT + 0.2	
	SCLK, $\overline{\text{SCS}}$, SDI, $\overline{\text{RESET}}$, SYNC, SCANEN, TXEN[0:1], FRDI[0:3], FRCLK, $\overline{\text{FRCS}}$, $\overline{\text{SYNC}}$ (4)	-0.3	VDDIO+0.3	
	EXTREF(2)	-0.3	VDDA18A + 0.3	
Voltage at output pins	DACOUTA+, DACOUTA-(2)	-0.3	VDDA18A + 0.5	V
	DACOUTB+, DACOUTB-(2)	-0.3	VDDA18B + 0.5	
	ATEST(2)	-0.3	VDDA18B + 0.3	
	RBIAS-/+(2)	-0.3	VDDA18A + 0.3	
	SDI, SDO, ALARM(4)	-0.3	VDDIO + 0.3	
Peak input current (any input)		-20	20	mA
Peak total input current (sum of absolute value of all currents forced in or out, not including power supply current and DACOUTA+, DACOUTA–, DACOUTB+ and DACOUTB–)			30	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured to AGND.
(3) Measured to VSSCLK.
(4) Measured to DGND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage range		VDDA18A, VDDA18B(1)	1.71	1.8	1.89	V
		VEEAM18, VEEBM18(1)	-1.89	-1.8	-1.71	V
		VDDCLK18, VDDSYS18, VDDSP18, VDDCP18(2)	1.71	1.8	1.89	V
		VDDLB, VDDLA, VDDCLK08(2)	0.76	0.8	0.84	V
		VDDIO, VDDR18(3)	1.71	1.8	1.89	V
		VQPS(3)	0	0	1.89	V
		VDDDIG, VDDEB, VDDEA, VDDT(3)	0.76	0.8	0.84	V
V_{CMI}	Input common mode voltage	CLK+, CLK–(2) (4)		0.4		V
		SYSREF+, SYSREF–(2) (4)	0.4	0.5	0.6	V
V_{ID}	Input differential peak-to-peak voltage	SYSREF+ to SYSREF–	400	1000	2000	$mV_{PP-DIFF}$
		CLK+ to CLK–, f_{CLK} < 3GHz(6)	800	1000	2000	$mV_{PP-DIFF}$
		CLK+ to CLK–, 3GHz < f_{CLK} < 12GHz(6)	800	1000	1400	$mV_{PP-DIFF}$
		CLK+ to CLK–, 12GHz < f_{CLK} < 17GHz(6)	800	1000	1800	$mV_{PP-DIFF}$
		CLK+ to CLK–, f_{CLK} > 17GHz(6)	800	1000	2000	$mV_{PP-DIFF}$
DC_{MIN}	DACCLK+/– duty cycle minimum	CLK+/– duty cycle minimum		45		%
DC_{MAX}	DACCLK+/– duty cycle maximum	CLK+/– duty cycle maximum		55		%
T_A	Operating free-air temperature		-40		85	°C
T_J	Recommended operating junction temperature				105(5)	°C
T_{J-MAX}	Maximum rated operating junction temperature	Maximum rated operating junction temperature	125			°C

(1) Measured to AGND.
(2) Measured to VSSCLK.
(3) Measured to DGND.
(4) CLK+/- and SYSREF+/- are weakly self-biased to the optimal common mode voltage. CLK+/- should always be AC coupled to the clock source. SYSREF+/- is recommended to be AC coupled to the clock source when possible.
(5) Die is designed for Tj = 150 °C operation and for device and die metallization degradation up to 150,000POH continuous operation at Tj = 113°C (118°C for 100,000POH). Prolonged use above a junction temperature of Tj =105 °C may, however, increase the package failure-in-time (FIT) rate.
(6) For optimum phase noise, the clock amplitude should be near the high end of the range.

6.4 Thermal Information

THERMAL METRIC(1)		13.8mm x 13.8mm FCCSP 289 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	15.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

6.5 Electrical Characteristics - DC Specifications

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz, external clock mode, I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, f_{OUT} = 2897MHz, NRZ mode, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
BITS	DAC core resolution		16		16	bits
DNL	Differential nonlinearity			±4		LSB
INL	Integral nonlinearity			±6		LSB
RT_{DRIFT}	Internal termination resistance drift over temperature			.02		Ω/°C
DAC ANALOG OUTPUT (DACOUTA+, DACOUTA–, DACOUTB+, DACOUTB–)						
I_{FS_SWITCH}	Switched full scale output current	3.6kΩ resistor from RBIAS+ to RBIAS-, COARSE_CUR_A / COARSE_CUR_B= 0xF and FINE_CUR_A / FINE_CUR_B = 0x10 (default), Current_2x = 1		40		mA
I_{FS_SWITCH}	Switched full scale output current	3.6kΩ resistor from RBIAS+ to RBIAS-, COARSE_CUR_A / COARSE_CUR_B= 0xF and FINE_CUR_A / FINE_CUR_B = 0x10 (default), Current_2x = 0		20		mA
		3.6kΩ resistor from RBIAS+ to RBIAS-, COARSE_CUR_A / COARSE_CUR_B = 0x0 and FINE_CUR_A / FINE_CUR_B = 0x10 (default), Current_2x = 0		2		
I_{STATIC}	Static output current per pin	3.6kΩ resistor from RBIAS+ to RBIAS-, COARSE_CUR_A / COARSE_CUR_B = 0xF and FINE_CUR_A / FINE_CUR_B = 0x10 (default)		4.7		mA
$I_{FSDRIFT}$	Full scale output current temperature drift	3.6kΩ resistor from RBIAS+ to RBIAS-, COARSE_CUR_A / COARSE_CUR_B = 0xF and FINE_CUR_A / FINE_CUR_B = 0x10 (default)		1		uA/°C
				65		PPM/°C
$I_{FSERROR}$	Full scale current error	3.6kΩ resistor from RBIAS+ to RBIAS-, COARSE_CUR_A / COARSE_CUR_B = 0xF and FINE_CUR_A / FINE_CUR_B = 0x10 (default)		±1		%
V_{COMP}	Output compliance voltage range	Measured from DACOUTA+, DACOUTA–, DACOUTB+ or DACOUTB– to AGND	1.3		2.3	V
R_{TERM}	Output differential termination resistance			100		Ω
$R_{TERMDRIFT}$	Output differential termination resistance temperature coeff			-5		mΩ/°C
				-50		PPM/°C
CLOCK AND SYSREF INPUTS (CLK+, CLK-, SYSREF+, SYSREF-)						
R_T	Internal differential termination resistance			100		Ω
C_{IN}	Internal differential input capacitance			0.5		pF
REFERENCE VOLTAGE						
V_{REF}	Reference output voltage			0.9		V
$V_{REF-DRIFT}$	Reference output voltage drift over temperature			45		ppm/°C
I_{REF}	Maximum reference output current sourcing capability			100		nA

ADVANCE INFORMATION

6.5 Electrical Characteristics - DC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz, external clock mode, I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, f_{OUT} = 2897MHz, NRZ mode, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
JESD204C SERDES INTERFACE ([15:0]SRX+/-)						
V_{SRDIFF}	SerDes Receiver Input Amplitude		50		1200	mVppdiff
V_{SRCOM}	SerDes Input Common Mode(2)			450		mV
Z_{SRdiff}	SerDes Internal Differential Termination		80	100	120	Ω
CMOS INTERFACE (SCLK, $\overline{SCS}$, SDI, SDO, $\overline{RESET}$, TRIG[0:4], TRIGCLK, $\overline{SYNC}$, TXENABLE[0:1])						
I_{IH}	High level input current (with pulldowns)	TRIG[0..4](3), TRIGCLK(3), SCANEN(1)			200	uA
I_{IH}	High level input current (without pulldowns)	$\overline{SDS}$, $\overline{RESET}$, $\overline{SYNC}$, TXEN[0:1], SDI, SCLK(1)			2	uA
I_{IL}	Low level input current (with pullups)	$\overline{SDS}$, $\overline{RESET}$, $\overline{SYNC}$, TXEN[0:1](1)	-100			uA
I_{IL}	Low level input current (without pullups)	SCANEN, SDI, SCLK(1)	-20			uA
C_I	Input capacitance	Input capacitance		3		pF
V_{IH}	High level input voltage	SCLK, $\overline{SCS}$, SDI, $\overline{RESET}$, SCANEN, TXEN[0:1], $\overline{SYNC}$, TRIG[0..4], TRIGCLK	0.7 x VDDIO18			V
V_{IL}	Low level input voltage			0.3 x VDDIO18		V
V_{OH}	High level output voltage	I_{LOAD} = –400uA	1.55			V
V_{OL}	Low level output voltage	I_{LOAD} = 400uA			0.2	V
TEMPERATURE DIODE CHARACTERISTICS (TDIODE+, TDIODE–)						
ΔV_{BE}	Temperature diode voltage slope	Forced forward current of 100µA. Offset voltage (approximately 0.792V at 0°C) varies with process and must be measured for each part. Offset measurement must be done with the device unpowered or with the PD pin asserted to minimize device self-heating.		–1.45		mV/°C

(1) With no IO supply voltage offset in connecting device.
(2) AC coupling from the Serdes transmitter is recommended.
(3) TRIG[0..3] and TRIGCLK have a pulldown when used as inputs. When used as outputs, the pulldown is disabled.

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MODE INDEPENDENT PARAMETERS						
f_{DACCLK}	DAC clock rate = f_{SAMPLE} in NRZ and RF mode = f_{SAMPLE}/2 in DES2XL/H modes			22		GHz
BW	Analog output bandwidth (–3dB)	Excluding sinx/x response. Useable frequency range may exceed the –3 dB point.		18		GHz
Crosstalk	Isolation between channel A (DACOUTA+/–) and channel B (DACOUTB+/-), f_{OUT} = -25MHz offset on victim channel, dual channel device only	f_{OUT} = 97MHz, NRZ mode		90		dBc
		f_{OUT} = 2897MHz, NRZ mode		75		dBc
		f_{OUT} = 5897MHz, NRZ mode		70		dBc
		f_{OUT} = 8897MHz, NRZ mode		66		dBc
		f_{OUT} = 13103MHz, RF mode		60		dBc
		f_{OUT} = 16103MHz, RF mode		55		dBc
		f_{OUT} = 19103MHz, RF mode		50		dBc
DAC OUTPUT TIME DOMAIN CHARACTERISTICS						
t_{RISE}	10% to 90%(1)	JMODE 0, 1x Interpolation		18		ps
t_{FALL}	90% to 10%(1)	JMODE 0, 1x Interpolation		18		ps
f_{CLK} fixed spur	Relative to fullscale sinewave at 1 GHz	NRZ Mode, f_{OUT} = DC (mid-code), DEM/Dither off		50		dBc
		NRZ Mode, f_{OUT} = DC (mid-code), DEM/Dither on		50		dBc
		DES2XL Mode, f_{OUT} = DC (mid-code), DEM/Dither off		50		dBc
		DES2XL Mode, f_{OUT} = DC (mid-code), DEM/Dither on		50		dBc
2*f_{CLK} fixed spur	Relative to fullscale sinewave at 1 GHz	DES2XL Mode, f_{OUT} = DC (mid-code), DEM/Dither off		50		dBc
		DES2XL Mode, f_{OUT} = DC (mid-code), DEM/Dither on		50		dBc

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
22GSPS GSPS, JMODE 2, 4x Int, NRZ MODE						
P_{OUT}	Output power into 100Ω load(2)	f_{OUT} = 97MHz		1.0		dBm
		f_{OUT} = 2897MHz		0.6		dBm
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		6.6		dBm
		f_{OUT} = 5897MHz		-0.5		dBm
		f_{OUT} = 8897MHz		-3.5		dBm
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		2.5		dBm
SFDR	Spurious free dynamic range (SFDR) across 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		–74		dBc
		f_{OUT} = 2897MHz		-56		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		-53		dBc
		f_{OUT} = 5897MHz		-44		dBc
		f_{OUT} = 8897MHz		-36		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		-45		dBc
HD2	Second harmonic (HD2), 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		–81		dBc
		f_{OUT} = 2897MHz		-56		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		-55		dBc
		f_{OUT} = 5897MHz		-44		dBc
		f_{OUT} = 8897MHz		-36		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		-38		dBc
HD3	Third harmonic (HD3), 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		–74		dBc
		f_{OUT} = 2897MHz		-75		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		-60		dBc
		f_{OUT} = 5897MHz		-70		dBc
		f_{OUT} = 8897MHz		-54		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		-60		dBc
$SFDR_{NONHD23}$	non-HD2/3 SFDR, 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		–98		dBc
		f_{OUT} = 2897MHz		–94		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		–94		dBc
		f_{OUT} = 5897MHz		–71		dBc
		f_{OUT} = 8897MHz		–74		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		–74		dBc
IMD3	Third-order two tone intermodulation distortion	f_{OUT} = 97 +/- 10MHz, -7dBFS/tone		–80		dBc
		f_{OUT} = 2897 +/- 10MHz, -7dBFS/tone		-75		dBc
		f_{OUT} = 2897 +/- 10MHz, -7dBFS/tone, I_{FS_SWITCH} = 40mA		-65		dBc
		f_{OUT} = 5897 +/- 10MHz, -7dBFS/tone		-75		dBc
		f_{OUT} = 8897 +/- 10MHz, -7dBFS/tone		-65		dBc
		f_{OUT} = 8897 +/- 10MHz, -7dBFS/tone, I_{FS_SWITCH} = 40mA		-70		dBc

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither on	f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–160		dBc/Hz
		f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–158		dBc/Hz
		v= 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–158		dBc/Hz
		f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–156		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–152		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–152		dBc/Hz
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither disabled	f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–170		dBc/Hz
		f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–168		dBc/Hz
		f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–168		dBc/Hz
		f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–166		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–160		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–160		dBc/Hz
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither on	AOUT = -20 dBFS, f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–163		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–162		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–162		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–160		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–160		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–160		dBFS/Hz
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither disabled	A_{OUT} = -20dBFS, f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–170		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–169		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–169		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–168		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–167		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–167		dBFS/Hz

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NPR	Noise power ratio, peak	Signal spanning C-Band, 200MHz notch in center, I_{FS_SWITCH} = 40mA		53		dBc
ENOB	Effective number of bits	Calculated from peak NPR, I_{FS_SWITCH} = 40mA		8.5		bits
PN	Additive DAC phase noise, external clock contribution subtracted out	f_{OUT} = 10GHz, 100Hz offset				dBc/Hz
		f_{OUT} = 10GHz, 1kHz offset		-120		dBc/Hz
		f_{OUT} = 10GHz, 10kHz offset		-132		dBc/Hz
		f_{OUT} = 10GHz, 100kHz offset		-140		dBc/Hz
		f_{OUT} = 10GHz, 1MHz offset		-142		dBc/Hz
		f_{OUT} = 10GHz, 10MHz offset		-143		dBc/Hz
PN	Additive DAC phase noise, external clock contribution subtracted out, DEM/Dither disabled	f_{OUT} = 10GHz, 100Hz offset				dBc/Hz
		f_{OUT} = 10GHz, 1kHz offset		-120		dBc/Hz
		f_{OUT} = 10GHz, 10kHz offset		-132		dBc/Hz
		f_{OUT} = 10GHz, 100kHz offset		-140		dBc/Hz
		f_{OUT} = 10GHz, 1MHz offset		-147		dBc/Hz
		f_{OUT} = 10GHz, 10MHz offset		-149		dBc/Hz

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
22GSPS GSPS, JMODE 2, 4x Int, DES2xL MODE						
P_{OUT}	Output power into 100Ω load[2]	f_{OUT} = 97MHz		1.0		dBm
		f_{OUT} = 2897MHz		0.8		dBm
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		6.8		dBm
		f_{OUT} = 5897MHz		0.4		dBm
		f_{OUT} = 8897MHz		-1.5		dBm
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		4.5		dBm
SFDR	Spurious free dynamic range (SFDR) across 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		-58		dBc
		f_{OUT} = 2897MHz		-59		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		-76		dBc
		f_{OUT} = 5897MHz		-66		dBc
		f_{OUT} = 8897MHz		-66		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		-60		dBc
HD2	Second harmonic (HD2), 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		–80		dBc
		f_{OUT} = 2897MHz		-58		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		-59		dBc
		f_{OUT} = 5897MHz		-76		dBc
		f_{OUT} = 8897MHz		-66		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		-66		dBc
HD3	Third harmonic (HD3), 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		–74		dBc
		f_{OUT} = 2897MHz		-71		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		-60		dBc
		f_{OUT} = 5897MHz		-80		dBc
		f_{OUT} = 8897MHz		-71		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		-80		dBc
$SFDR_{NONHD23}$	non-HD2/3 SFDR, 0 - F_{DACCLK}/2	f_{OUT} = 97MHz		–92		dBc
		f_{OUT} = 2897MHz		–87		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		–87		dBc
		f_{OUT} = 5897MHz		–73		dBc
		f_{OUT} = 8897MHz		–74		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		–74		dBc
IMG_{DES}	F_{DACCLK} - F_{OUT} DES Image	f_{OUT} = 97MHz		-66		dBc
		f_{OUT} = 2897MHz		-62		dBc
		f_{OUT} = 2897MHz, I_{FS_SWITCH} = 40mA		-62		dBc
		f_{OUT} = 5897MHz		-59		dBc
		f_{OUT} = 8897MHz		-51		dBc
		f_{OUT} = 8897MHz, I_{FS_SWITCH} = 40mA		-51		dBc

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	Third-order two tone intermodulation distortion	f_{OUT} = 97 +/- 10MHz, -7dBFS/tone		–80		dBc
		f_{OUT} = 2897 +/- 10MHz, -7dBFS/tone		-83		dBc
		f_{OUT} = 2897 +/- 10MHz, -7dBFS/tone, I_{FS_SWITCH} = 40mA		-63		dBc
		f_{OUT} = 5897 +/- 10MHz, -7dBFS/tone		-72		dBc
		f_{OUT} = 8897 +/- 10MHz, -7dBFS/tone		-65		dBc
		f_{OUT} = 8897 +/- 10MHz, -7dBFS/tone, I_{FS_SWITCH} = 40mA		-67		dBc
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither off	f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–170		dBc/Hz
		f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–168		dBc/Hz
		f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–168		dBc/Hz
		f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–166		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–160		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–160		dBc/Hz
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither on	f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–160		dBc/Hz
		f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–158		dBc/Hz
		f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–158		dBc/Hz
		f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–156		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–152		dBc/Hz
		f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–152		dBc/Hz
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither off	AOUT = -20 dBFS, f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–170		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–169		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–169		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–168		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–167		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–167		dBFS/Hz

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither on	A_{OUT} = -20dBFS, f_{OUT} = 97MHz, 70MHz offset from f_{OUT}		–163		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}		–162		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 2897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–162		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 5897MHz, 70MHz offset from f_{OUT}		–160		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}		–160		dBFS/Hz
		A_{OUT} = -20dBFS, f_{OUT} = 8897MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		–160		dBFS/Hz
NPR	Noise power ratio, peak	Signal spanning C-Band, 200MHz notch in center, I_{FS_SWITCH} = 40mA		53		dBc
ENOB	Effective number of bits	Calculated from peak NPR		8.5		bits
PN	Additive DAC phase noise, external clock contribution subtracted out, DEM/Dither off	f_{OUT} = 10GHz, 100Hz offset				dBc/Hz
		f_{OUT} = 10GHz, 1kHz offset		-120		dBc/Hz
		f_{OUT} = 10GHz, 10kHz offset		-132		dBc/Hz
		f_{OUT} = 10GHz, 100kHz offset		-140		dBc/Hz
		f_{OUT} = 10GHz, 1MHz offset		-147		dBc/Hz
		f_{OUT} = 10GHz, 10MHz offset		-149		dBc/Hz

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
22GSPS GSPS, JMODE 2, 4x Int, RF MODE						
P_{OUT}	Output power into 100Ω load(2)	f_{OUT} = 13103MHz		-3.5		dBm
		f_{OUT} = 16103MHz		-4.0		dBm
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		2.0		dBm
		f_{OUT} = 19103MHz		-5.0		dBm
SFDR	Spurious free dynamic range (SFDR) across $F_{DACCLK}/2$ - F_{DACCLK}	f_{OUT} = 13103MHz		–45		dBc
		f_{OUT} = 16103MHz		-45		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-45		dBc
		f_{OUT} = 19103MHz		-45		dBc
HD2	2nd Harmonic Distortion in $F_{DACCLK}/2$ - F_{DACCLK}	f_{OUT} = 13103MHz		–40		dBc
		f_{OUT} = 16103MHz		-35		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-35		dBc
		f_{OUT} = 19103MHz		-46		dBc
HD3	3rd Harmonic Distortion in $F_{DACCLK}/2$ - F_{DACCLK}	f_{OUT} = 13103MHz		–51		dBc
		f_{OUT} = 16103MHz		-75		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-55		dBc
		f_{OUT} = 19103MHz		-56		dBc
$SFDR_{NONHD23}$	non-HD2/3 SFDR across $F_{DACCLK}/2$ - F_{DACCLK}	f_{OUT} = 13103MHz		-72		dBc
		f_{OUT} = 16103MHz		-67		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-65		dBc
		f_{OUT} = 19103MHz		-69		dBc
IMD3	Third-order two tone intermodulation distortion	f_{OUT} = 13103 +/- 10MHz, -7dBFS/tone		-55		dBc
		f_{OUT} = 16103 +/- 10MHz, -7dBFS/tone		-55		dBc
		f_{OUT} = 16103 +/- 10MHz, -7dBFS/tone, I_{FS_SWITCH} = 40mA		-60		dBc
		f_{OUT} = 19103 +/- 10MHz, -7dBFS/tone		-70		dBc
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither off	f_{OUT} = 13103MHz, 70MHz offset from f_{OUT}		-158		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}		-155		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-155		dBc/Hz
		f_{OUT} = 19103MHz, 70MHz offset from f_{OUT}		-154		dBc/Hz
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither on	f_{OUT} = 13103MHz, 70MHz offset from f_{OUT}		-154		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}		-152		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-152		dBc/Hz
		f_{OUT} = 19103MHz, 70MHz offset from f_{OUT}		-151		dBc/Hz

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither off	f_{OUT} = 13103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-165		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-164		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-164		dBFS/Hz
		f_{OUT} = 19103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-164		dBFS/Hz
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither on	f_{OUT} = 13103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-160		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-159		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-159		dBFS/Hz
		f_{OUT} = 19103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-158		dBFS/Hz
NPR	Noise power ratio, peak	Signal spanning Ku-Band, 300MHz notch in center, I_{FS_SWITCH} = 40mA		48		dBc
ENOB	Effective number of bits	Calculated from peak NPR		7.8		bits
PN	Additive DAC phase noise, external clock contribution subtracted out, DEM/Dither off	f_{OUT} = 17.8GHz, 100Hz offset		-103		dBc/Hz
		f_{OUT} = 17.8GHz, 1kHz offset		-115		dBc/Hz
		f_{OUT} = 17.8GHz, 10kHz offset		-126		dBc/Hz
		f_{OUT} = 17.8GHz, 100kHz offset		-135		dBc/Hz
		f_{OUT} = 17.8GHz, 1MHz offset		-144		dBc/Hz
		f_{OUT} = 17.8GHz, 10MHz offset		-148		dBc/Hz

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
22GSPS GSPS, JMODE 2, 4x Int, DES2xH MODE						
P_{OUT}	Output power into 100Ω load[2]	f_{OUT} = 13103MHz		-1.2		dBm
		f_{OUT} = 16103MHz		-2.0		dBm
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		4.0		dBm
		f_{OUT} = 19103MHz		-2.5		dBm
SFDR	Spurious free dynamic range (SFDR) across F_{DACCLK}/2- F_{DACCLK}	f_{OUT} = 13103MHz		–47		dBc
		f_{OUT} = 16103MHz		-35		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-30		dBc
		f_{OUT} = 19103MHz		-58		dBc
HD2	2nd Harmonic Distortion in F_{DACCLK}/2- F_{DACCLK}	f_{OUT} = 13103MHz		–47		dBc
		f_{OUT} = 16103MHz		-35		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-30		dBc
		f_{OUT} = 19103MHz		-58		dBc
HD3	3rd Harmonic Distortion in F_{DACCLK}/2- F_{DACCLK}	f_{OUT} = 13103MHz		–72		dBc
		f_{OUT} = 16103MHz		-69		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-70		dBc
		f_{OUT} = 19103MHz		-67		dBc
$SFDR_{NONHD23}$	non-HD2/3 SFDR across F_{DACCLK}/2- F_{DACCLK}	f_{OUT} = 13103MHz		-72		dBc
		f_{OUT} = 16103MHz		-73		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-65		dBc
		f_{OUT} = 19103MHz		-69		dBc
IMG_{DES}	F_{DACCLK} - F_{OUT} DES Image	f_{OUT} = 13103MHz		-43		dBc
		f_{OUT} = 16103MHz		-48		dBc
		f_{OUT} = 16103MHz, I_{FS_SWITCH} = 40mA		-48		dBc
		f_{OUT} = 19103MHz		-39		dBc
IMD3	Third-order two tone intermodulation distortion	f_{OUT} = 13103 +/- 10MHz, -7dBFS/tone		-66		dBc
		f_{OUT} = 16103 +/- 10MHz, -7dBFS/tone		-68		dBc
		f_{OUT} = 16103 +/- 10MHz, -7dBFS/tone, I_{FS_SWITCH} = 40mA		-58		dBc
		f_{OUT} = 19103 +/- 10MHz, -7dBFS/tone		-70		dBc
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither off	f_{OUT} = 13103MHz, 70MHz offset from f_{OUT}		-158		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}		-155		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-155		dBc/Hz
		f_{OUT} = 19103MHz, 70MHz offset from f_{OUT}		-154		dBc/Hz

ADVANCE INFORMATION

6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating junction temperature range, typical supply voltages, f_{CLK} = 22GHz (external clock mode), I_{FS_SWITCH} = 20mA, single tone amplitude = -0.1dBFS, Dither and DEM enabled, 64b/66b encoding, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise spectral density, large signal, sinusoidal output, DEM/Dither on	f_{OUT} = 13103MHz, 70MHz offset from f_{OUT}		-154		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}		-152		dBc/Hz
		f_{OUT} = 16103MHz, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-152		dBc/Hz
		f_{OUT} = 19103MHz, 70MHz offset from f_{OUT}		-151		dBc/Hz
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither off	f_{OUT} = 13103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-165		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-164		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-164		dBFS/Hz
		f_{OUT} = 19103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-164		dBFS/Hz
NSD	Noise spectral density, small signal, sinusoidal output, DEM/Dither on	f_{OUT} = 13103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-160		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-159		dBFS/Hz
		f_{OUT} = 16103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}, I_{FS_SWITCH} = 40mA		-159		dBFS/Hz
		f_{OUT} = 19103MHz, A_{OUT} = -20dBFS, 70MHz offset from f_{OUT}		-158		dBFS/Hz
NPR	Noise power ratio, peak	Signal spanning Ku-Band, 300MHz notch in center, I_{FS_SWITCH} = 40mA		48		dBc
ENOB	Effective number of bits	Calculated from peak NPR		7.8		bits
PN	Additive DAC phase noise, external clock contribution subtracted out, DEM/Dither off	f_{OUT} = 17.8GHz, 100Hz offset				dBc/Hz
		f_{OUT} = 17.8GHz, 1kHz offset		-115		dBc/Hz
		f_{OUT} = 17.8GHz, 10kHz offset		-127		dBc/Hz
		f_{OUT} = 17.8GHz, 100kHz offset		-135		dBc/Hz
		f_{OUT} = 17.8GHz, 1MHz offset		-144		dBc/Hz
		f_{OUT} = 17.8GHz, 10MHz offset		-148		dBc/Hz

(1) Measured single ended into 50Ω load
(2) A 100Ω load is equivalent to a 2:1 with 50Ω single ended load. Includes device die and package parasitics and output response. PCB and external component losses removed.

ADVANCE INFORMATION

6.7 Electrical Characteristics - Power Consumption

Typical values at T_A = +105°C and fast process, minimum and maximum values over operating free-air temperature range, typical supply voltages, 2 channels,external clock mode, f_{CLK} = 22GHz, f_{OUT} = 2997MHz, NRZ mode, I_{FS_SWITCH} = 20mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDDA18}	1.8V combined supply current for VDDA18A and VDDA18B	Power Mode 1: Single DAC, JMODE 0 with 1 real stream, f_{INPUT} = 22GSPS, 1x Interpolation, f_{SERDES} = 22.6875Gbps, 66b/64b encoding, NRZ mode, f_{OUT} = 8797 MHz		60		mA
I_{VDDIO}	1.8V supply current for VDDIO			1		
I_{VDDCSR}	1.8V combined supply current for VDDCLK18, VDDSYS18, VDDR18 and VDDSP18			344		
$I_{VDDCP18}$	1.8V supply for data converter PLL/VCO			2		
I_{VDDL}	0.8V combined supply current for VDDLB, VDDLA			340		
I_{VDDCLK}	0.8V supply current for VDDCLK08			656		
I_{DVDD}	0.8V supply current for VDDDIG, VDDT, VDDEB and VDDEA			2320		
I_{VEE}	–1.8V combined supply current for VEEAM18 and VEEBM18			57		
P_{DIS}	Total power dissipation			3483		mW
I_{VDDA18}	1.8V combined supply current for VDDA18A and VDDA18B	Power Mode 2: Dual DACs, JMODE 2 with 2 IQ streams, f_{INPUT} = 5.5GSPS, 4x Interpolation, f_{SERDES} = 22.6875Gbps, 66b/64b encoding, NRZ mode, f_{OUT} = 2897MHz		114		mA
I_{VDDIO}	1.8V supply current for VDDIO			0		
I_{VDDCSR}	1.8V combined supply current for VDDCLK18, VDDSYS18, VDDR18 and VDDSP18			350		
$I_{VDDCP18}$	1.8V supply for data converter PLL/VCO			0		
I_{VDDL}	0.8V combined supply current for VDDLB, VDDLA			710		
I_{VDDCLK}	0.8V supply current for VDDCLK08			687		
I_{DVDD}	0.8V supply current for VDDDIG, VDDT, VDDEB and VDDEA			4198		
I_{VEE}	–1.8V combined supply current for VEEAM18 and VEEBM18			114		
P_{DIS}	Total power dissipation			5517		mW
I_{VDDA18}	1.8V combined supply current for VDDA18A and VDDA18B	Power Mode 3: Dual DACs, JMODE 3 with 4 IQ streams, f_{INPUT} = 2.75GSPS, 8x Interpolation, f_{SERDES} =30.9375Gbps, 66b/64b encoding, NRZ mode, f_{OUT} = 2897MHz, 5897MHz		114		mA
I_{VDDIO}	1.8V supply current for VDDIO			1		
I_{VDDCSR}	1.8V combined supply current for VDDCLK18, VDDSYS18, VDDR18 and VDDSP18			388		
$I_{VDDCP18}$	1.8V supply for data converter PLL/VCO			0		
I_{VDDL}	0.8V combined supply current for VDDLB, VDDLA			710		
I_{VDDCLK}	0.8V supply current for VDDCLK08			687		
I_{DVDD}	0.8V supply current for VDDDIG, VDDT, VDDEB and VDDEA			5262		
I_{VEE}	–1.8V combined supply current for VEEAM18 and VEEBM18			114		
P_{DIS}	Total power dissipation			6437		mW

ADVANCE INFORMATION

6.7 Electrical Characteristics - Power Consumption (continued)

Typical values at T_A = +105°C and fast process, minimum and maximum values over operating free-air temperature range, typical supply voltages, 2 channels,external clock mode, f_{CLK} = 22GHz, f_{OUT} = 2997MHz, NRZ mode, I_{FS_SWITCH} = 20mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDDA18}	1.8V combined supply current for VDDA18A and VDDA18B	Power Mode 4: Dual DACs, JMODE 6 with 4 IQ streams, f_{INPUT} = 458.3MSPS, 48x Interpolation, f_{SERDES} =30.25Gbps, 66b/64b encoding, NRZ mode, f_{OUT} = 2897MHz, 5897MHz		114		mA
I_{VDDIO}	1.8V supply current for VDDIO			1		
I_{VDDCSR}	1.8V combined supply current for VDDCLK18, VDDSYS18, VDDR18 and VDDSP18			388		
$I_{VDDCP18}$	1.8V supply for data converter PLL/VCO			0		
I_{VDDL}	0.8V combined supply current for VDDLB, VDDLA			710		
I_{VDDCLK}	0.8V supply current for VDDCLK08			687		
I_{DVDD}	0.8V supply current for VDDDIG, VDDT, VDDEB and VDDEA			4602		
I_{VEE}	–1.8V combined supply current for VEEAM18 and VEEBM18			114		
P_{DIS}	Total power dissipation			5909		mW
I_{VDDA18}	1.8V combined supply current for VDDA18A and VDDA18B	Power Mode 5: Dual DACs, JMODE 17 with 2 real streams, f_{INPUT} = 21GSPS, 1x Interpolation, f_{SERDES} = 32.48Gbps, 66b/64b encoding, NRZ mode, f_{OUT} = 8797MHz		114		mA
I_{VDDIO}	1.8V supply current for VDDIO			1		
I_{VDDCSR}	1.8V combined supply current for VDDCLK18, VDDSYS18, VDDR18 and VDDSP18			395		
$I_{VDDCP18}$	1.8V supply for data converter PLL/VCO			0		
I_{VDDL}	0.8V combined supply current for VDDLB, VDDLA			710		
I_{VDDCLK}	0.8V supply current for VDDCLK08			687		
I_{DVDD}	0.8V supply current for VDDDIG, VDDT, VDDEB and VDDEA			3665		
I_{VEE}	–1.8V combined supply current for VEEAM18 and VEEBM18			114		
P_{DIS}	Total power dissipation	Power Mode 5: Dual DACs, JMODE 17 with 2 real streams, f_{INPUT} = 21GSPS, 1x Interpolation, f_{SERDES} = 32.48Gbps, 66b/64b encoding, NRZ mode, f_{OUT} = 8797MHz		5172		mW
P_{DIS}	Total power dissipation	Power Mode 6: Power Down				mW
I_{VDDDIG}	Additional Current DES enabled	scales with f_{CLK} and # DAC		150		mA
	Additional Current with PFIR enabled at DUC output	scales with f_{CLK} and fraction non-zero taps (of 24)		2100		mA
$I_{VDDCP18}$	Additional Current with PLLVCO enabled	scales with f_{CLK}		132		mA
I_{VEE}	Additional Current with 40mA compared to 20mA	per DAC		57		mA

ADVANCE INFORMATION

6.8 Timing Requirements

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, f_{CLK} = 22GHz, external clock mode, I_{FS_SWITCH} = 20mA, single tone amplitude = 0.1dBFS, Dither and DEM enabled, unless otherwise noted.

			MIN	NOM	MAX	UNIT
INPUT CLOCK (CLK+, CLK-)						
f_{CLK}	Input clock frequency	External clock mode	0.8		22	GHz
f_{CLK}	Input clock frequency	PLL/VCO clock mode	0.1		3	GHz
SYSREF and Clock Path Delays						
t_{SYSREF_LOW}	SYSREF Low Time Requirement		5*t_{DEVLK} + 1ns			
t_{SYSREF_HIGH}	SYSREF High Time Requirement		5*t_{DEVLK} + 1ns			
$t_{ADJRANGEMIN}$	Minimum range for clock delay t_{ADJ}			130		ps
$t_{ADJRANGEMAX}$	Maximum range for clock delay t_{ADJ}			280		ps
$t_{SYSRANGEMIN}$	Minimum SYSREF system delay range			130		ps
$t_{SYSRANGEMAX}$	Maximum SYSREF system delay range			280		ps
$t_{xSTEPCOARSEMAX}$	t_{ADJ} and t_{SYS} delay maximum coarse step size	setting bits 18:14		9500		fs
$t_{xSTEPCOARSEMIN}$	t_{ADJ} and t_{SYS} delay minimum coarse step size	setting bits 18:14		3200		fs
$t_{xSTEPMEDMAX}$	t_{ADJ} and t_{SYS} delay maximum medium step size	setting bits 13:10		4000		fs
$t_{xSTEPMEDMIN}$	t_{ADJ} and t_{SYS} delay minimum medium step size	setting bits 13:10		270		fs
$t_{xSTEPFINEMAX}$	t_{ADJ} and t_{SYS} delay maximum fine step size	setting bits 9:0		16.7		fs
$t_{xSTEPFINEMIN}$	t_{ADJ} and t_{SYS} delay minimum fine step size	setting bits 9:0		2.2		fs
$t_{xSETTLE}$	t_{ADJ} and t_{SYS} delay settling time	settle to within 5% of the added delay		42		ns
RESET						
t_{RESET}	Minimum $\overline{\text{RESET}}$ pulse width			25		ns

ADVANCE INFORMATION

6.9 Switching Characteristics

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, f_{CLK} = 16GHz, external clock mode, I_{FS_SWITCH} = 41mA, single tone amplitude = 0dBFS, Dither and DEM enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
JESD204C SERDES INTERFACE [15:0]SRX-/+						
$f_{SERDESMAX}$	SERDES bit rate maximum		32.5			Gbps
$f_{SERDESMIN}$	SERDES bit rate minimum				1.5	Gbps
f_{REFMAX}	Serdes PLL reference frequency maximum		2040			MHz
f_{REFMIN}	Serdes PLL reference frequency minimum				82	MHz
f_{VCOMAX}	Serdes PLL frequency maximum		16.25			GHz
f_{VCOMIN}	Serdes PLL Frequency minimum				8.125	GHz
SJ_{LF}	Low frequency sinusoidal jitter tolerance	20kHz			5	UI
SJ_{HF}	High frequency sinusoidal jitter tolerance	20MHz			0.05	UI
BHPUJ	Bounded high-probability uncorrelated jitter tolerance				0.25	UI
BHPCJ	Bounded high-probability correlated jitter tolerance				0.2	UI
TUJ	Total jitter tolerance(2)				0.7	UI
$BOOST_{CTLE}$	CTLE Boost at data rate Nyquist frequency with respect to DC		9			dB
R_{LDIFF}	Differential return loss	f_{IN} = 0.275 - 0.75*f_{SERDES}			-9.7	dB
LATENCY						
T_{DACCLK}	DAC clock period			1 / f_{CLK}		
$t_{PD(RX)}$	Serdes RX analog propagation delay	Serdes RX analog propagation delay		250		ps
t_{PDI}	Input clock rising edge cross-over to output sample cross-over	Input clock rising edge cross-over to output sample cross-over		250		ps
t_{DAC_LAT}	Digital path latency from SYSREF rising edge to DAC output			See XLS Calculator		
$t_{RELEASE}$	Latency from SYSREF rising edge to elastic buffer release			See XLS Calculator		
t_{RXIN}	Latency from SERDES Input to elastic buffer release			See XLS Calculator		
SERIAL PROGRAMMING INTERFACE						
f_{S_C}	serial clock frequency				15	MHz
t_P	serial clock period		33			ns
t_{PH}	serial clock pulse width high		16			ns
t_{PL}	serial clock pulse width low		16			ns
t_{SU}	SDI setup		8			ns
t_H	SDI hold		1.5			ns
t_{IZ}	SDI TRI-STATE				3	ns
t_{ODZ}	SDO driven to TRI-STATE	200fF load	0		6	ns
t_{OZD}	SDO TRI-STATE to driven	200fF load	0		6	ns
t_{OD}	SDO output delay	200fF load	0		6	ns
t_{CSS}	$\overline{SCS}$ setup		8			ns
t_{CSH}	$\overline{SCS}$ hold		1.5			ns

ADVANCE INFORMATION

6.9 Switching Characteristics (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, f_{CLK} = 16GHz, external clock mode, I_{FS_SWITCH} = 41mA, single tone amplitude = 0dBFS, Dither and DEM enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{IAG}	Inter-access gap		16			ns
t_{CRS}	$\overline{SCS}$ setup to $\overline{RESET}$	$\overline{RESET}$ rising edge	0			ns
t_{CSH}	$\overline{SCS}$ hold to $\overline{RESET}$	$\overline{RESET}$ rising edge	30			ns
FAST RECONFIGURATION (FR) AND TRIGGER INTERFACE						
$F_{TRIGCLK}$	FRCLK frequency				200	MHz
$t_{TRIGCLK\_P}$	FRCLK period		5			ns
$t_{TRIGCLK\_PH}$	FRCLK pulse width high		2.4			ns
t_{FRCLK_PL}	FRCLK pulse width low		2.4			ns
$t_{TRIG0\_3\_SU}$	TRIG[3:0] setup	relative to TRIGCLK output rising edge(3)	2.6			ns
$t_{TRIG0\_3\_H}$	TRIG[3:0] hold	relative to TRIGCLK output rising edge(3)	0.5			ns
t_{TRIG4_SU}	TRIG4 setup	relative to TRIGCLK output rising edge(3)	2.5			ns
t_{TRIG4_H}	TRIG4 hold	relative to TRIGCLK output rising edge(3)	0.6			ns
t_{FR_IAG}	Inter-access gap		5			ns
$t_{FR\_PFIRWAIT}$	Wait time after setting FR_PFIR_PROG = 1		1024			DACCLKs
PLL/VCO Characteristics						
f_{REF}	Reference clock frequency		0.1		3	GHz
f_{DACCLK}	DAC sample clock with converter PLL/VCO		8.125		17	GHz
PLL_{RATIO}	Ratio of reference clock to VCO frequency(4)		6		255	
PLL_{DIV}	Ratio of VCO frequency to DAC sample clock		1		1	
PN_{PLL}	PLL/VCO Phase Noise, f_{REF} = 2GHz(1)	f_{VCO} = 16GHz, 100Hz offset		-102		dBc/Hz
		f_{VCO} = 16GHz, 1KHz offset		-112		dBc/Hz
		f_{VCO} = 16GHz, 10kHz offset		-122		dBc/Hz
		f_{VCO} = 16GHz, 100kHz offset		-129		dBc/Hz
		f_{VCO} = 16GHz, 1MHz offset		-132		dBc/Hz
		f_{VCO} = 16GHz, 10MHz offset		-130		dBc/Hz
		f_{VCO} = 16GHz, 100MHz offset		-139		dBc/Hz
PN_{PLLINT}	1kHz to 100MHz, f_{REF} = 2GHz(1)	f_{VCO} = 20GHz		-55		dBc

(1) Measured at DAC output at 1GHz, normalized to VCO frequency.
(2) Includes high-frequency sinusoidal jitter; the Gaussian jitter (GJ) portion is defined with respect to a BER of 10^{-15}.
(3) with 4pF load on TRIGCLK
(4) Device supports 2^N*3^M, where N = 1 - 16 and M = 0 or 1

ADVANCE INFORMATION

6.10 SPI Interface Timing Diagrams

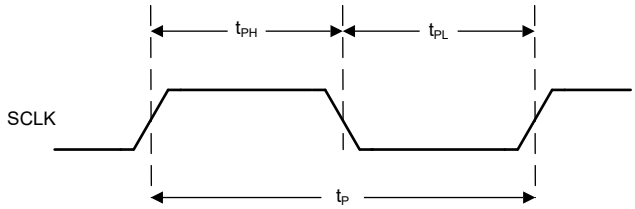


Figure 6-1. SPI Clock Timing Diagram

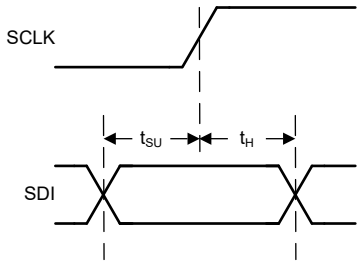


Figure 6-2. SPI Data Input Timing Diagram

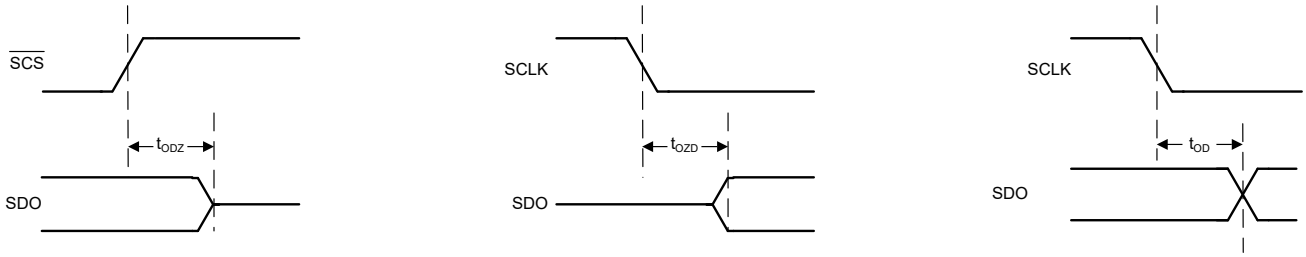


Figure 6-3. SPI Data Output Timing Diagram

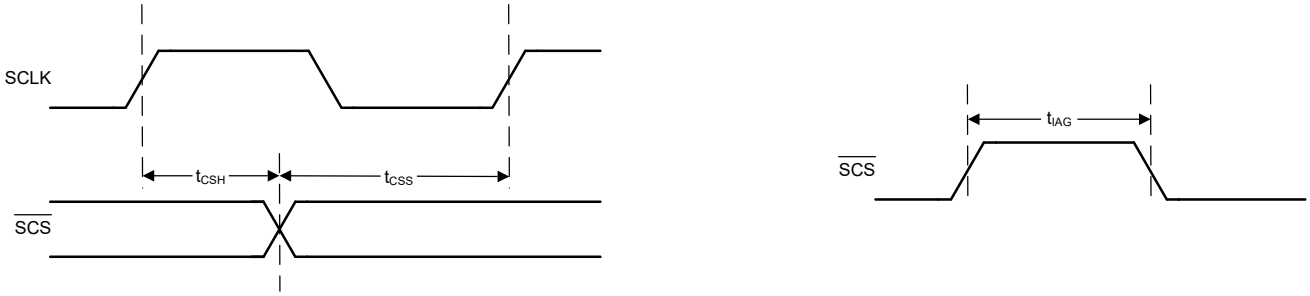


Figure 6-4. SPI Chip Select Timing Diagram

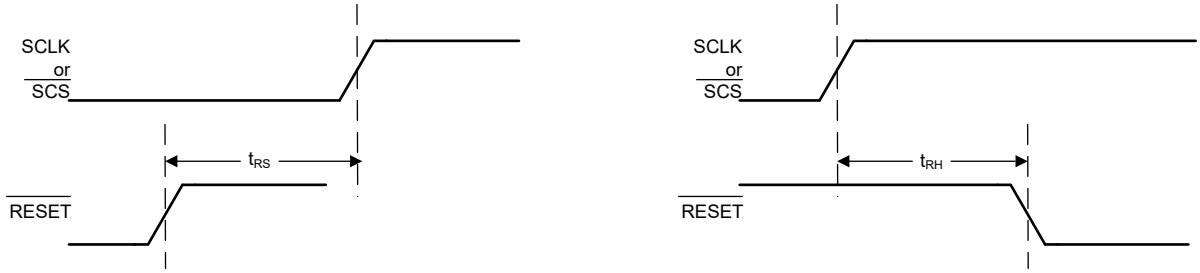


Figure 6-5. $\overline{\text{RESET}}$ Timing Diagram

7 Detailed Description

7.1 Overview

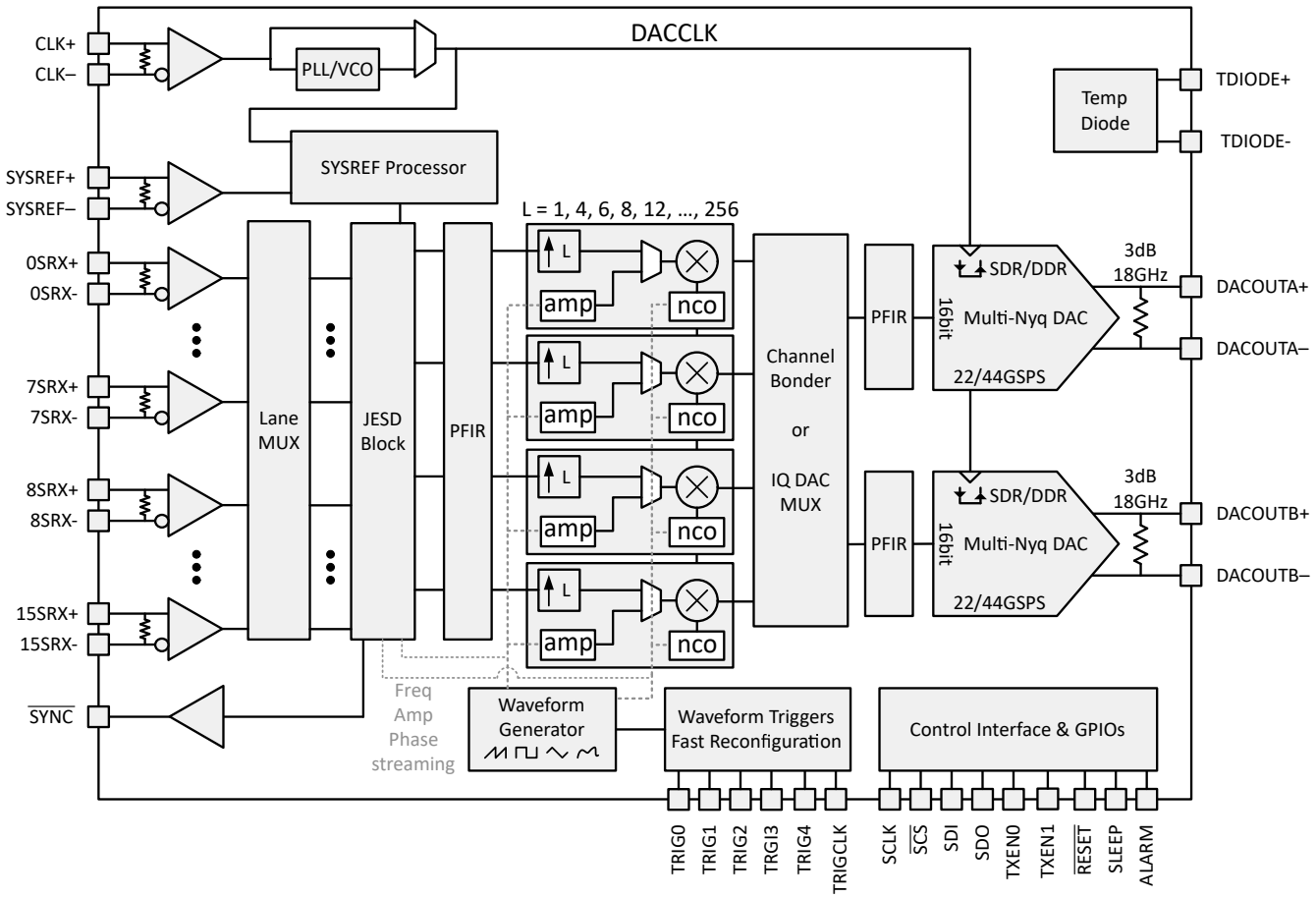
The DAC39RF20 is a single and dual channel digital-to-analog converter (DAC) with 16-bit resolution. With external clock, the devices support 22GSPS with single edge sampling modes (NRZ and RF) and 44GSPS in dual edge sampling modes (DES2XL, DES2XH). When using the internal PLL/VCO, the devices support 17GSPS with single edge sampling modes (NRZ and RF) and 34GSPS in dual edge sampling modes (DES2XL, DES2XH). The devices can be used as noninterpolating or interpolating DACs for either direct RF sampling or complex baseband signal generation. The maximum input data rate for two channels is 21GSPS (12-bit resolution) or 15.75GSPS (16-bit resolution). The maximum rate for one channel is 22GSPS (16-bit resolution). The device can generate signals greater than 10GHz bandwidth at frequencies exceeding 20GHz, enabling direct sampling through Ku band.

The high sampling rate, output frequency range, 64-bit NCO frequency resolution and infinite frequency hopping with phase coherence also makes DAC39RF20 capable of arbitrary waveform generation (AWG) and direct digital synthesis (DDS). Four built in piecewise linear waveform generators can be used to synthesize complex waveforms, for example for non-linear frequency modulation (NLFM), Frank or Barker phase coded radar pulses, or derivative removal by adiabatic gate (DRAG) pulses for quantum computing controllers.

An optional high performance PLL/VCO can be used to generate the DAC sample clock from a lower frequency reference clock.

A JESD204C compatible interface has 16 receiver pairs capable of up to 32.5Gbps. The interface is subclass-1 compliant for deterministic latency and multi-device synchronization through the use of SYSREF (external clock mode only).

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

This section describes the analog and digital features of the device.

7.3.1 DAC Output Modes

The DAC39RF20 contains two multi-Nyquist DAC cores capable of direct transmission in 1st and 2nd Nyquist zone. The high output frequency capabilities are enabled by specific output switching waveforms that alter the frequency response of the DAC output to enhance the DAC images in higher Nyquist zones. The desired output mode can be selected independently for each DAC by programming the MXMODE0/1 registers. A list of DAC output modes along with their properties and uses are provided in Table 7-1. The responses shown in this section do not consider the effect of the DAC analog bandwidth or external passive or active signal chain components.

Table 7-1. Summary of Multi-Nyquist Output Modes and Uses

DAC OUTPUT MODE	PASSES DC	OPTIMAL FREQUENCY RANGE(2)	PEAK OUTPUT POWER (1)	OTHER
Non-return-to-zero (NRZ)	Yes	0 - $F_{CLK}/2$	0dBFS	
Radio Frequency (RF)	No	$F_{CLK}/2$ - F_{CLK}	–2.8dBFS	
Dual Edge Sampling Low Band (DES2XL)	Yes	0 - 0.4*$F_{CLK}/2$	0dBFS	Duty cycle image at F_{CLK} - F_{OUT}
Dual Edge Sampling High Band (DES2XH)	No	0.6*F_{CLK} - F_{CLK}	0dBFS	Duty cycle image at F_{CLK} - F_{OUT}

(1) Peak power here does not include the effect of analog output bandwidth due to parasitic passive components or external components
(2) F_{CLK} is the frequency of the CLK+/- input

ADVANCE INFORMATION

7.3.1.1 NRZ Mode

Non-return-to-zero (NRZ) mode is the standard zero-order hold mode. The timing diagram for NRZ mode is given in Figure 7-1. The sample is output from the DAC on the rising edge of the clock provided to the DAC core (either from the PLL/VCO or externally) and held until the rising edge. This output waveform can be thought of as a rectangular filter in time domain resulting in a sinc response in the frequency domain. The result is a frequency response that has significant power loss in the 2nd and 3rd Nyquist zones and a null at the sampling rate and is meant for 1st Nyquist zone operation only. A plot of the frequency response of NRZ mode is shown in Figure 7-2.

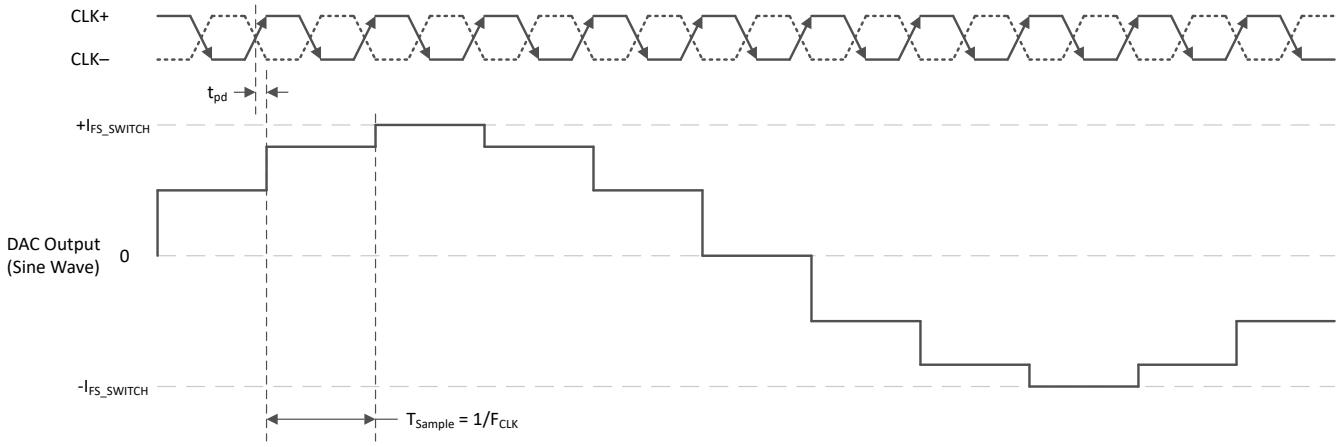


Figure 7-1. NRZ Mode Timing Diagram

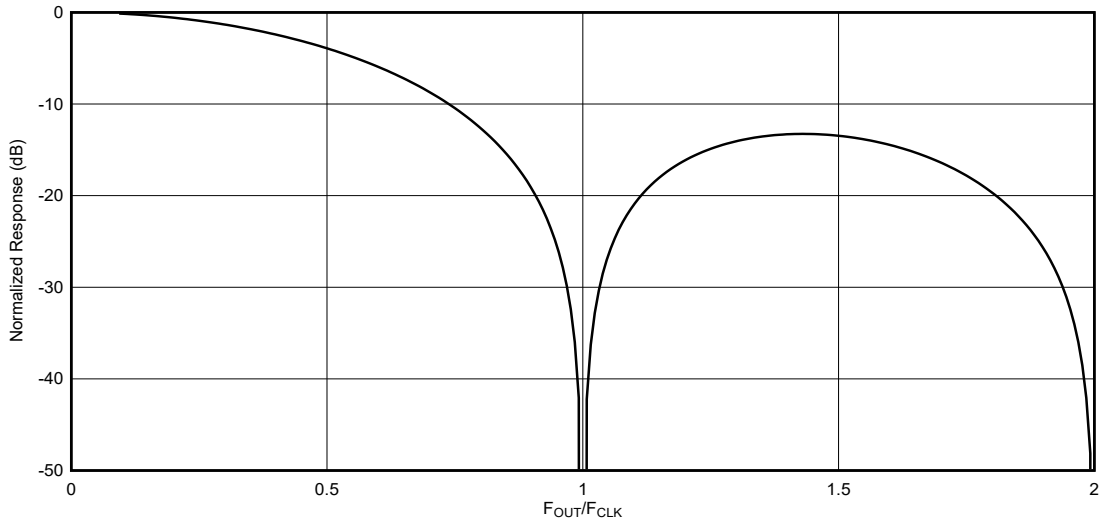


Figure 7-2. NRZ Mode Output Frequency Response

7.3.1.2 RF Mode

RF mode adds a mixing function to the DAC output by inverting the sample halfway through the sample period. The result is a frequency response that peaks and provides maximum flatness in the 2nd Nyquist zone. The timing diagram for RF mode is given in Figure 7-3. A plot of the frequency response of RF mode is shown in Figure 7-4.

ADVANCE INFORMATION

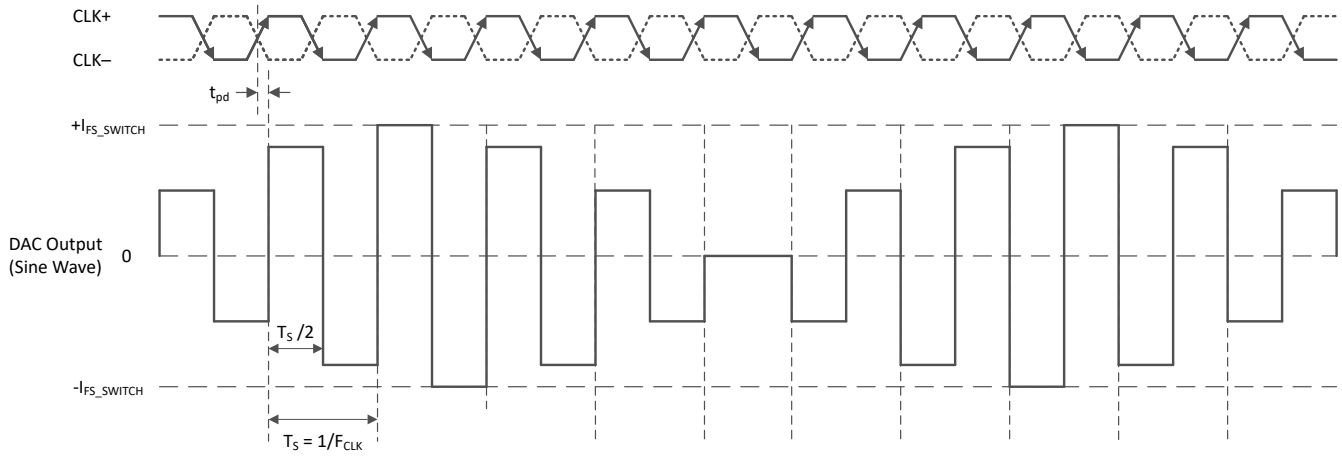


Figure 7-3. RF Mode Timing Diagram

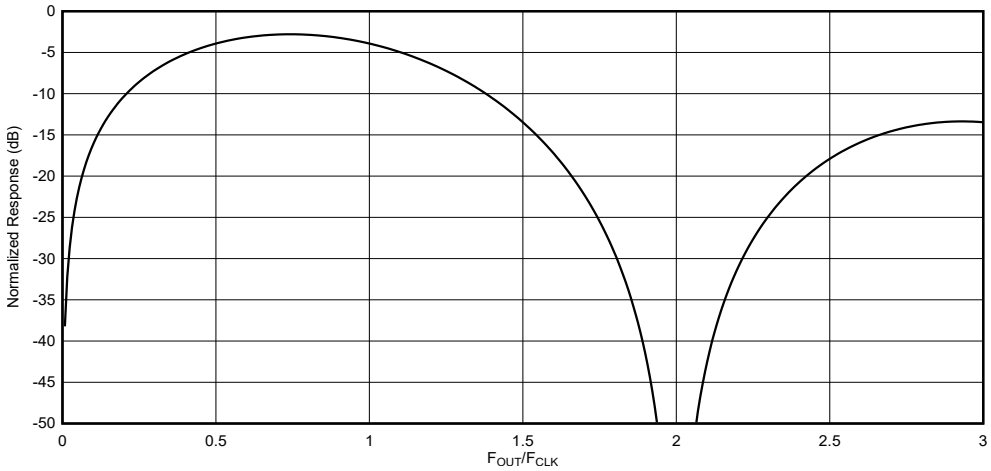


Figure 7-4. RF Mode Output Frequency Response

7.3.1.3 DES Modes

Dual edge sampling (DES) mode outputs unique samples on both the rising and falling edge of the DACCLK provided to the DAC core (either from the PLL/VCO or provided externally), doubling the sample rate for the same clock frequency. An extra digital interpolate by 2 stage is included in the device to enable a double sample rate. In DES2XL mode the interpolation filter is low pass (passing 0 - 0.4*F_{DACCLK}) and in DES2XH mode the interpolation filter is high pass (passing 0.6*F_{DACCLK} - F_{DACCLK}). The DES2XL and DES2XH interpolation filter combined with the Sin(x)/x response is shown in Figure 7-5.

A non-50% CLK duty cycle results in an image of the signal at F_{CLK} - F_{OUT}. Compared to NRZ or RF modes with the same DACCLK, DES2XL and DES2XH modes provide significant reduction in the image amplitude, reducing filter requirements.

ADVANCE INFORMATION

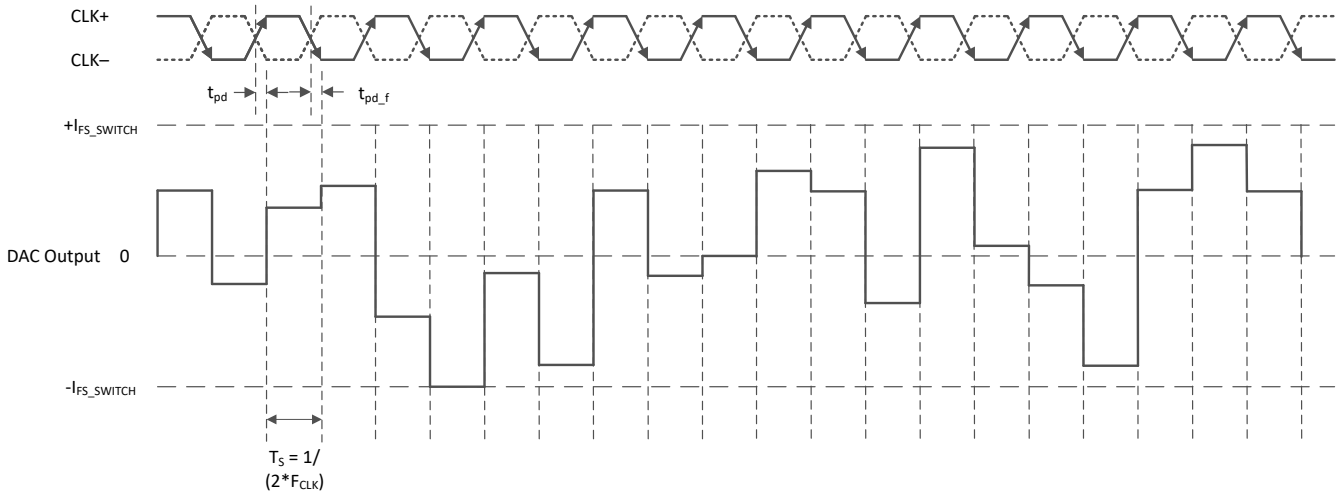


Figure 7-5. DES Mode Timing Diagram

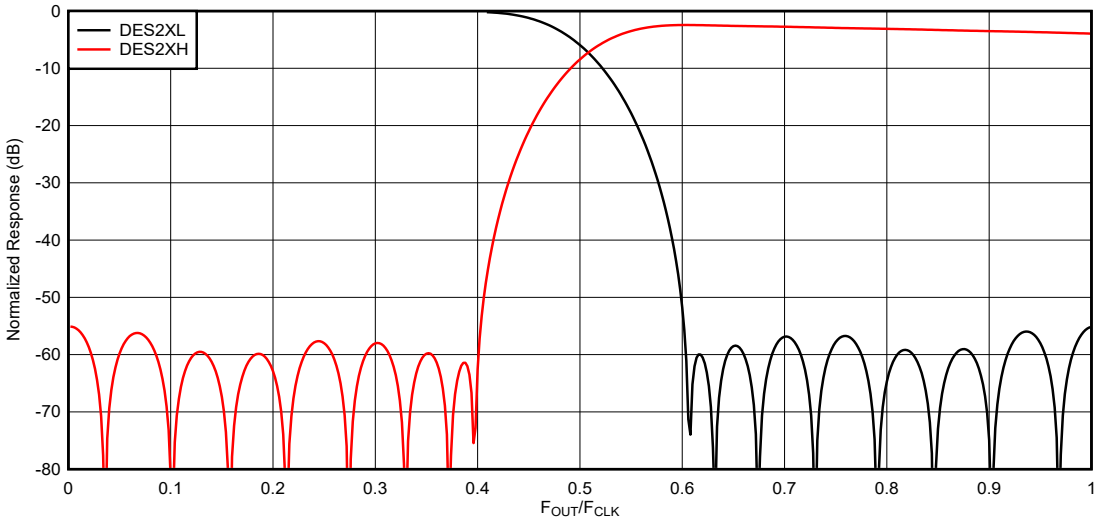


Figure 7-6. DES Modes Output Frequency Response

7.3.2 DAC Core

The device has two 16-bit DAC cores.

7.3.2.1 DAC Output Structure

The DAC core analog output structure is shown in Figure 7-7 for one DAC channel. There is a differential termination resistance between the two current output pins, DACOUTx±. The current steering switch array connects to the output pins and steers current between the output pins based on the digital code. A constant DC current bias, I_{FS_STATIC}, draws current from both outputs regardless of the digital code. An internal resistor R_{TERM} with nominal 100Ohm resistance terminates the output differentially.

ADVANCE INFORMATION

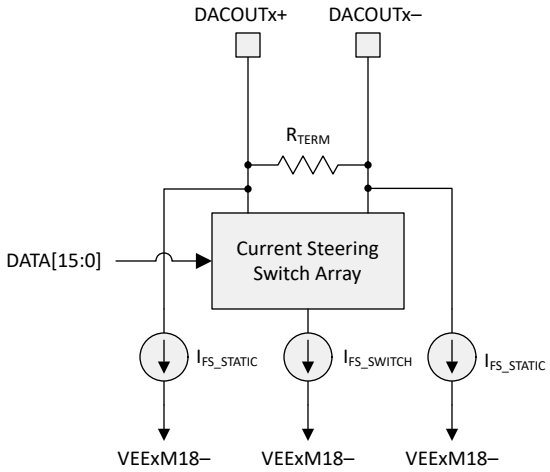


Figure 7-7. Analog Output Structure

Examples of conversions from digital codes to currents on the DACOUTx± outputs are given in Table 7-2. The currents shown in Table 7-2 include both the current steered portion and the bias currents on each leg.

ADVANCE INFORMATION

Table 7-2. Example Digital Code to Analog Current Conversions

DIGITAL CODE	2'S COMPLEMENT	OFFSET BINARY	$I_{DACOUTx+}$	$I_{DACOUTx-}$	$I_{DACOUTx+} - I_{DACOUTx-}$
32767	0111 1111 1111 1111	1111 1111 1111 1111	0.9999847 × I_{FS_SWITCH} + I_{FS_STATIC}	0.0000153 × I_{FS_SWITCH} + I_{FS_STATIC}	0.9999694 × I_{FS_SWITCH}
16384	0100 0000 0000 0000	1100 0000 0000 0000	¾ × I_{FS_SWITCH} + I_{FS_STATIC}	¼ × I_{FS_SWITCH} + I_{FS_STATIC}	½ × I_{FS_SWITCH}
0	0000 0000 0000 0000	0000 0000 0000 0000	½ × I_{FS_SWITCH} + I_{FS_STATIC}	½ × I_{FS_SWITCH} + I_{FS_STATIC}	0
–16384	1100 0000 0000 0000	0100 0000 0000 0000	¼ × I I_{FS_SWITCH} + I_{FS_STATIC}	¾ × I I_{FS_SWITCH} + I_{FS_STATIC}	–½ × I_{FS_SWITCH}
–32768	1000 0000 0000 0000	0000 0000 0000 0000	I_{FS_STATIC}	I I_{FS_SWITCH} + I_{FS_STATIC}	–I_{FS_SWITCH}

7.3.2.2 Full-Scale Current Adjustment

The total DAC output current is set through the external R_{BIAS} resistor and the COARSE_CUR_A or COARSE_CUR_B, the FINE_CUR_A or FINE_CUR_B and CURRENT_2X_EN registers. There is a switched fullscale current and a static fullscale current. The switched current is divided between DACOUTA/B+ and DACOUTA/B- in proportion to the digital signal value at the DAC. The static current is fixed at the output of each ball DACOUTA/B+ and DACOUTA/B-.

The equation for the total DAC switched output current is

$$I_{FSSWITCH} = \frac{3.6k\Omega}{R_{BIAS}} \times (1.2mA + 1.2mA{*}COARSE + 0.025mA{*}FINE) \times 2^{CUR\_2X\_EN} \quad (1)$$

where

- R_{bias} is the external bias resistor
- COARSE is the value of the register COARSE_CUR_A or COARSE_CUR_B (0 to 15)
- FINE is the value of register FINE_CUR_A or FINE_CUR_B (0 to 63)
- CUR_2X_EN is the value of register CURRENT_2X_EN (0 or 1)

The static current is a fixed fraction of the switched current

$$I_{FS\_STATIC} = 0.23 \times I_{FS\_SWITCH} \quad (2)$$

With a 3.6kΩ bias resistor, at the default values of COARSE_CUR_A or COARSE_CUR_B = 15, FINE_CUR_A or FINE_CUR_B = 32 and CURRENT_2X_EN = 0, $I_{FS\_SWITCHED}$ is approximately 20mA and I_{FS_STATIC} approximately 4.6mA (on each ball + and -).

7.3.3 DEM and Dither

The device contains two optional features to improve non-linearity due to current segment and switch timing mismatch: dynamic element mixing (DEM) and dither.

The DAC core consists of

1. Thermometer encoded current sources/switches representing the MSBs
2. Binary weighted current sources/switches representing the LSBs.
3. Additional current sources/switches for dithering

DEM randomizes which MSB current sources/switches are used to generate the output, which whitens the non-linearity due to mismatches between the current sources and switch timing. The DEM_DITH and DEM_ADJ registers control the frequency and amplitude of the shift in current sources/segments.

Dither add or subtracts different digital code values to the digital data which are then canceled by switching additional current sources with the same amplitude. The digital data path is expanded so the full 16-bit range is maintained. The DITH0/1 register fields control the frequency of the dither.

ADVANCE INFORMATION

Using DEM generally improves low order harmonics near fullscale. Dither generally improves higher order harmonics near fullscale and all harmonics at lower digital amplitudes. Both DEM and dither increase the noise floor (both amplitude and phase) of the output due to the whitening of the non-linearity. This is reduced by DEM and dither settings with lower switching activity.

7.3.4 Offset Adjustment

The device allows an offset adjustment to the signal at the DAC output. The offset adjustment does NOT take away from the full 16-bit digital range of the DAC data.

The offset is set by the DAC_OFS[0] or DAC_OFS[1] register values for DACA and DACB, respectively. If dithering is enabled (see register DEM_DITH), the value is saturated to the range of ±128. If dithering is disabled, the value is saturated to the range ±3968. This makes sure that the primary DAC range never is exceeded.

7.3.5 Clocking Subsystem

The device requires a clock (called DACCLK) running at a frequency equal to the DAC core sampling rate in NRZ, RTZ and RF modes, or at half of the DAC core sampling rate in DES mode. The clocking subsystem is shown in Figure 7-8. The input clock can be directly at DACCLK frequency or alternatively at a reference frequency when the internal PLL/VCO (CPLL) is used to generate DACCLK. Multi-device synchronization is not possible when using the internal PLL/VCO.

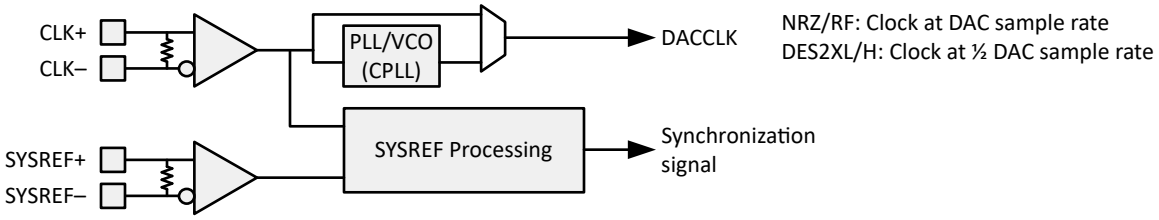


Figure 7-8. Device Clocking Subsystem

7.3.5.1 Converter Phase Locked Loop (CPLL)

The CPLL supports a continuous range of frequencies up to the maximum DACCLK frequency. When using the CPLL, the user must program various parameters for proper operation before setting CPLL_EN, subject to the constraints:

1. $F_{DACCLK} = F_{CPLL} = F_{CLK} * CPLL\_MPY$
2. $8GHz <= F_{CPLL} <= 17GHz$
3. $8 <= CPLL\_MPY <= 99$

7.3.5.2 Clock and SYSREF Delay

The device has several available delays on the clock and SYSREF paths that can be used for device and SYSREF alignment (see Figure 7-9). In the clock path there is a programmable inversion and a fine delay adjustment D_{ADJ}, which is controlled by T_{ADJ} register (when SRCAL_EN = 0) or by the automatic SYSREF calibration engine (when SRCAL_EN = 1). In the SYSREF path there is a fine delay adjustment D_{SYS} controlled by T_{SYS}. An initial value for T_{SYS} is controlled by the T_{SYS} register (SRCAL_EN=0 or SRTRK_EN=0) and then by the automatic SYSREF calibration engine (when SRCAL_EN=1 and SRTRK_EN=1). When SRCAL_EN=1, the Automatic SYSREF Calibration and Tracking values can be read via the TADJ_CAL and TSYS_CAL registers.

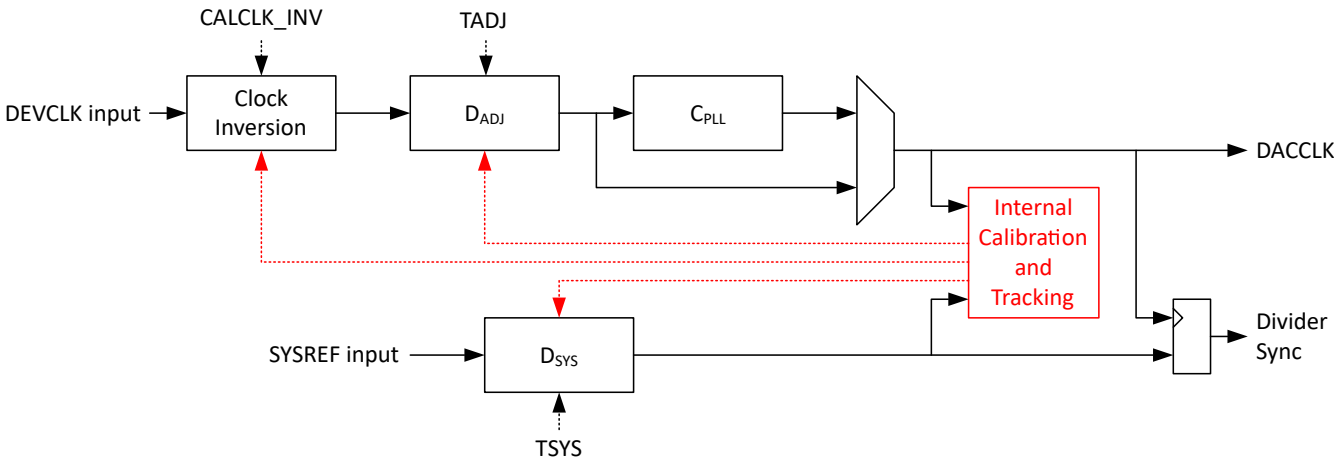


Figure 7-9. Clock and SYSREF Delay Diagram

The delay registers consist of 3 delay fields: coarse, medium and fine. For each field, a value of zero produces minimum delay. The specifications for the delay range and step are given in Section 6.8.

Table 7-3. Timing Adjust Block Register Delay Encoding

Register Bits	Description
18:14	32 step coarse delay
13:10	13 step medium delay – Values >12 are not allowed
9:0	1024 step fine delay

7.3.5.3 SYSREF Capture and Monitoring

7.3.5.3.1 SYSREF Frequency Requirements

The SYSREF input period must be an integer multiple of all clocks in the part, including the LMFC/LEMC. The following table depicts the requirements for the SYSREF period:

Table 7-4. Requirements for SYSREF period

Requirements on SYSREF Period
SYSREF period must be a multiple of 32 DACCLK cycles.
SYSREF period must be a multiple of LT DACCLK cycles. This requirement only applies when the JESD204C interface is enabled. [1]
SYSREF period must be a multiple of 8*LT*S/GCD(8*LT*S,F) DACCLK cycles. This requirement only applies when the JESD204C interface is enabled. [1]
SYSREF period must be a multiple of LT*S*K DACCLK cycles. This requirement only applies when the JESD204C interface is enabled [1] and (SUBCLASS = 1)
SYSREF period must be a multiple of 32*(TRIGC_DIV+1) DACCLK cycles. This requirement only applies when TRIG_TYPE*n* = 4 or 6 (for any *n*).

1. The JESD204C interface is enabled when JESD_M is greater than 0 and SYS_EN=1
2. GCD(*x*,*y*) is the greatest common divisor of *x* and *y*, the largest integer that can evenly divide both *x* and *y*.

SYSREF_ALIGN_EN must be set for any clocks to realign to SYSREF edges.

7.3.5.3.2 SYSREF Pulses for Full Alignment

The device contains a cascade of clock dividers that are aligned by SYSREF. Multiple SYSREF pulses are necessary to fully align all clock dividers and set the CLK_ALIGNED register bit. A total of 15 SYSREF pulses are required to fully align the device.

ADVANCE INFORMATION

7.3.5.3.3 Automatic SYSREF Calibration and Tracking

When configured for automatic SYSREF Calibration and Tracking (CPLL_EN = 0 and SRCAL_EN = 1), the system begins calibration when the SYSREF_RX_EN = 1 and SRCAL_EN = 1. If either of these goes low, the calibration engine resets and SYSREF_CAL_DONE, SYSREF_CAL_FAIL, and SYSREF_TRACK_FAIL are be cleared.

7.3.5.3.3.1 SYSREF Automatic Calibration Procedure

Use the following procedure to run the automatic calibration:

1. Set SRCAL_AVG and SRTRK_AVG to appropriate settings
2. Set SYSREF_RX_EN=1
3. Set SYSREF_PROC_EN=1
4. Wait for the SYSREF receiver to settle before setting SRCAL_EN=1
5. Wait for SYSREF_CAL_DONE=1

For calibration to produce the best results, the delays need to be consistent throughout the calibration process. Even small changes in supply voltage or temperature of any portion of the clock and SYSREF paths can have a significant impact on the quality of the calibration results waiting for the device temperature to stabilize can help the calibration process. The system designer must make sure that the paths are stable from the time that SRCAL_EN is set until SYSREF_CAL_DONE = 1.

For the best alignment of multiple devices, all devices must be calibrated at the same time so the common SYSREF circuitry is at the same temperature and voltage.

7.3.5.3.3.2 Multi-device Alignment

When using internal calibration, T_{SYS} can be initially set to tune the alignment between multiple calibrated devices. To do this, perform a binary search of each of the coarse, medium, and fine delay settings for T_{SYS}. For each test, calibration must be rerun on all chips and then the timing difference of the outputs must be measured to determine the next step.

7.3.5.3.3.3 Calibration Failure

If calibration fails because the edge is not found within the range of the delay, SYSREF_CAL_FAIL is set to 1, TADJ_CAL is set to 0, and CALCLK_INV_CAL is set so the rising edge of the CALCLK is at least the entire range of DADJ before the rising edge of SYSREF. While this provides the most margin possible for sampling SYSREF, the device does not use SYSREF as the low-skew alignment reference. SYSREF tracking is not performed in this case.

7.3.5.3.3.4 SYSREF Tracking

SYSREF tracking runs whenever SYSREF_CAL_DONE=1 and SYSREF_CAL_FAIL=0, and automatically adjusts TSYS_CAL to maintain alignment of SYSREF to the clock falling edge.

To maintain tracking, changes in timing between SYSREF and the clock internal or external to the device cannot change too quickly. The user must avoid any abrupt voltage changes as these can cause tracking to switch to a different clock edge.

7.3.5.4 Trigger Clocking

The synchronous trigger clock is generated by dividing the DAC clock according to register TRIGC_DIV. The divider is reset on each rising edge of SYSREF. If a SYSREF edge is detected that realigns the trigger clock divider, CLK_REALIGNED is set. Trigger clock is used to latch the synchronous trigger interface.

For the trigger clock to be active, you must set SYS_EN = 1 and at least one of the TRIG_TYPE*n* values must be 4 or 6. The trigger clock is driven on the TRIGCLK output if TRIGC_OUT_EN = 1 and FR_EN = 0. Alternatively, the user can use ALARM_SEL to output the trigger clock on the ALARM pin (this is helpful if the TRIGCLK pin is unavailable because the pin is allocated to the FRI interface). If FR_EN = 1, TRIGCLK becomes an input to latch FR data.

When TRIGC_DIV is even and greater than zero (TRIGC_DIV+1 is odd), the high time of the output clock is 32 DACCLK cycles less than the low time.

7.3.6 Digital Signal Processing Blocks

The digital signal processing blocks are shown in Figure 7-10. The device includes four digital up-converter (DUC) blocks supporting four complex (IQ) input streams that can be combined at different RF frequencies. The four DUCs can be flexibly assigned and summed together for either DAC output in the channel bonder. A programmable FIR filter can be used either at the input to the DUC's or at the DAC sample rate. The final signal processing block is a extra interpolate by 2 filter for use with DES mode.

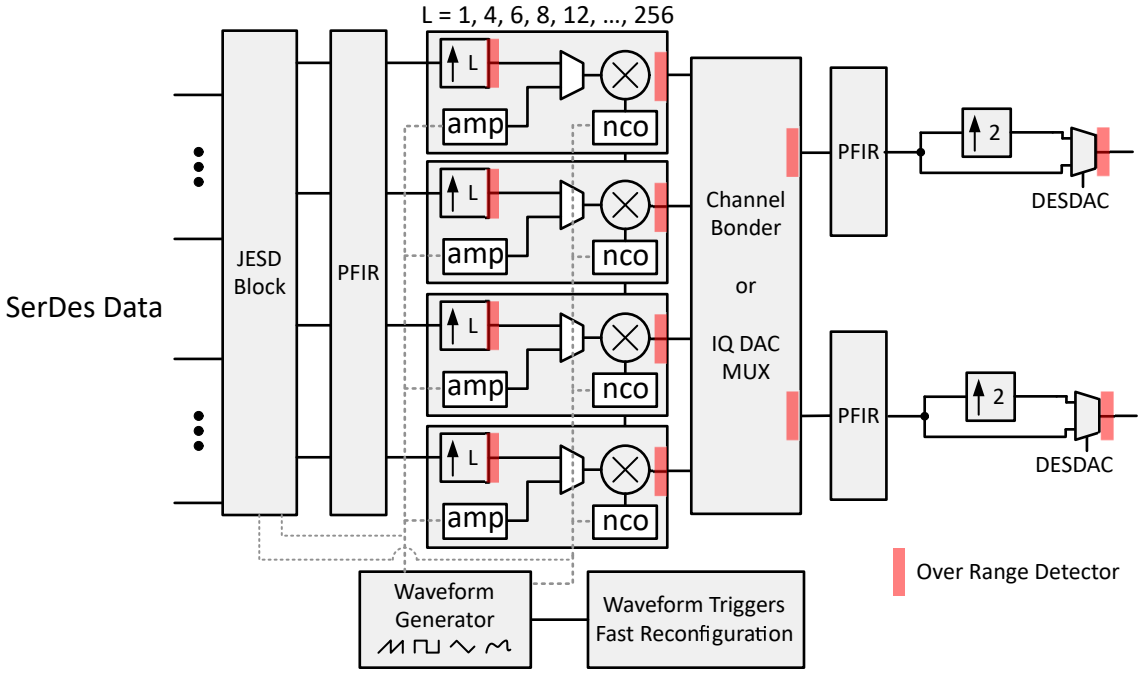


Figure 7-10. Digital Signal Processing Blocks

The DSPs can operate in several different modes, which are summarized below. Each mode is covered more fully in its own sub-section. The mode for each DSP block is selected by the DSP_MODE*n* register, *n* = 0 to 3

1. Bypass Mode: Bypass mode disables the DUC/DDS signal processing and sends data to the IQ DAC MUX. The signal can then be inverted (DAC_INV), equalized using the PFIR and interpolated by 2x for DES2XL/H modes.
2. DUC Mode: This mode accepts I/Q samples from the JESD204C interface, interpolates the sampling rate using FIR filters, and then uses an NCO/Mixer to translate the signals to a carrier frequency.
3. DDS SPI Mode: This mode uses the AMP, FREQ, and PHASE registers to define the amplitude, frequency, and phase of a cosine signal. Samples from the JESD204C interface are not used by the DSP.
4. DDS Vector Mode: This mode uses a table of vectors (programmed via SPI) to generate DDS waveforms. Frequency and amplitude ramping are supported, as well as auto/manual triggering. Samples from the JESD204C interface are not used by the DSP.
5. DDS Streaming Mode This mode uses the JESD204C interface to stream frequency, phase, and amplitude values to the DDS. The STREAM_MODE register can be used to restrict the streaming to frequency-only, or phase+amplitude only.

Table 7-5 summarizes key features of the NCO/Mixer and how they operate in the various DSP modes.

ADVANCE INFORMATION

Table 7-5. NCO/Mixer Features vs. DSP Mode

Features	DSP Mode (DSP_MODE*n*)			
	DUC Mode	DDS SPI Mode	DDS Vector Mode	DDS Streaming Mode
Amplitude Control	Determined by I/Q samples (via JESD)	AMP Register	Set by vectors (DDS_VEC)	AMP register or JESD stream (see STREAM_MODE)
Frequency Control	FREQ Register (64 bits)	FREQ Register (64 bits)	Set by vectors (DDS_VEC) (48 bits)	FREQ register or JESD stream (see STREAM_MODE)
Phase Control	PHASE Register	PHASE Register	Set by vectors (DDS_VEC)	PHASE register or JESD stream (see STREAM_MODE)
JESD Interface	Yes (two 16-bit streams per DSP) (I/Q data)	No	No	Yes (two 16-bit streams per DSP)
Trigger Actions	FREQ/PHASE update. Accumulator reset if NCO_AR = 1.	FREQ/PHASE/AMP update. Accumulator reset if NCO_AR = 1.	Advance to next vector if waiting for trigger.	Update non-streamed parameter(s). Accumulator reset if NCO_AR = 1
Other Features	Phase-coherent frequency change. Phase-continuous frequency change.	Phase-coherent frequency change. Phase-continuous frequency change.	FREQ/AMP ramping via vector table	Streaming a zero amplitude can generate a trigger
Mixer Used for:	Multiply IQ data with NCO	Amplitude control	Amplitude control	Amplitude control

7.3.6.1 Bypass Mode

Bypass mode disables the DUC/DDS and sends data directly from the JESD204C transport layer to the Encoder. The routing is controlled by the Channel Bonder.

7.3.6.2 DUC Mode

7.3.6.2.1 Digital Upconverter (DUC)

Each DUC interpolates the I and Q signals by factors ranging from L = 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128, 192 and 256. The resulting up-converted baseband I/Q signal is then multiplied by a complex sinusoid generated by the numerically controlled oscillator (NCO) to mix the signal to the desired carrier frequency for output from the DAC. The interpolation factors supported vs the number of DUCs enabled is listed in Table 7-6.

Table 7-6. Supported Interpolation Factors vs Number of DUCs Enabled

Interpolation Factors Supported (L)	DSP Channels that support DUC Mode
4x, 6x	Only DSP channel 0 and 1 can use DUC mode. Channel 2 and 3 must be disabled or placed into a non-DUC mode.
8x - 256x	Any DSP channel can be placed into DUC mode.

The NCOs and mixer can be bypassed, essentially setting the frequency and phase to 0, in which case the I input passes to the I output and the Q input passes to the Q output.

7.3.6.2.1.1 Interpolation Filters

The first operation of the DUC is to interpolate the input signal to a higher data rate. The available interpolation options are summarized in Table 7-7. The sampling rate of the input signal is multiplied by the specified interpolation amount to determine the DAC output rate, subject to the maximum sample rate for the DAC39RF20. These rates do not include the optional 2x interpolation for DES mode. For interpolations rates 6x and below, a reduced number of DUC channels are available.

Table 7-7. Summary of Interpolation Options

INTERPOLATION	Maximum Number of DUC channels
4x	2 (only DUC0 and DUC1)
6x	2 (only DUC0 and DUC1)
8x	4

Table 7-7. Summary of Interpolation Options (continued)

INTERPOLATION	Maximum Number of DUC channels
12x	4
16x	4
24x	4
32x	4
48x	4
64x	4
96x	4
128x	4
192x	4
256x	4

Each DUC contains multiple 2x or 3x interpolating filters. The composite interpolation filter responses are given in Figure 7-11 to Figure 7-35. The filters are designed to provide a passband bandwidth of 81.4% on the input bandwidth and passband ripple less than 0.001dB. The stopband attenuation is greater than 90dB for any signal within the passband.

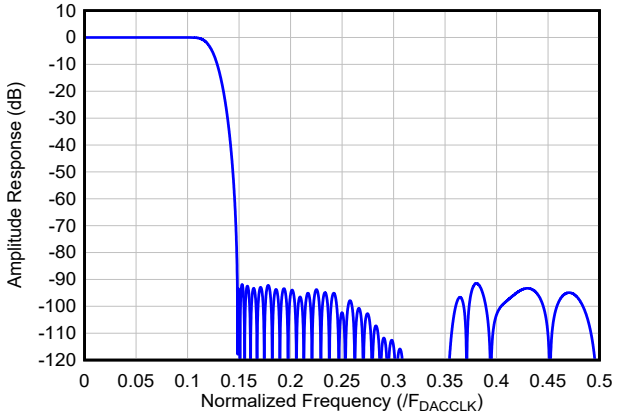


Figure 7-11. 4x Interpolation Filter Response

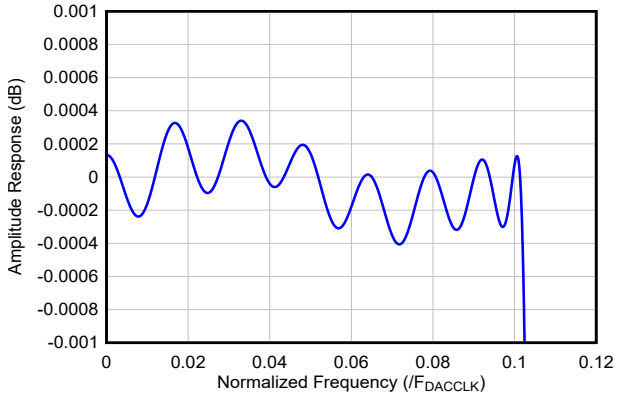


Figure 7-12. 4x Interpolation Filter Passband Response

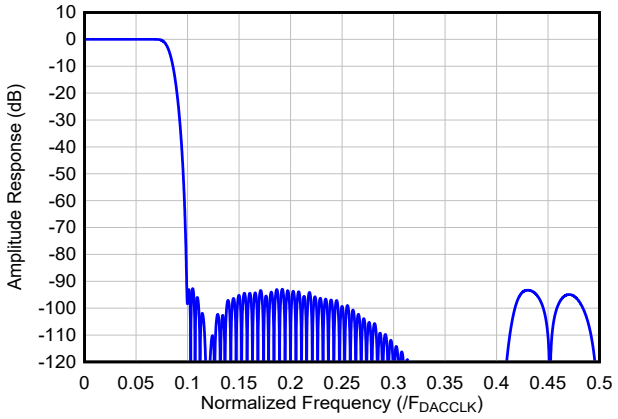


Figure 7-13. 6x Interpolation Filter Response

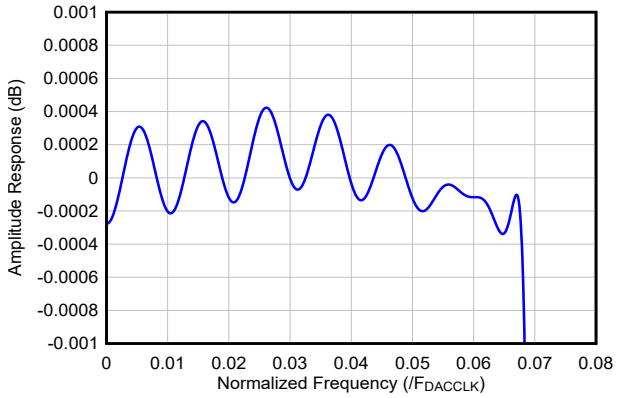


Figure 7-14. 6x Interpolation Filter Passband Response

ADVANCE INFORMATION

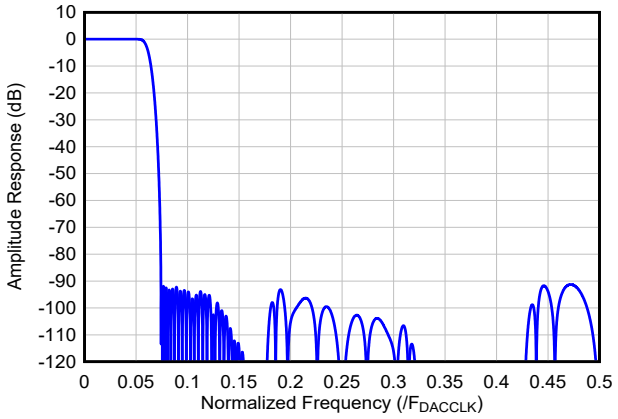


Figure 7-15. 8x Interpolation Filter Response

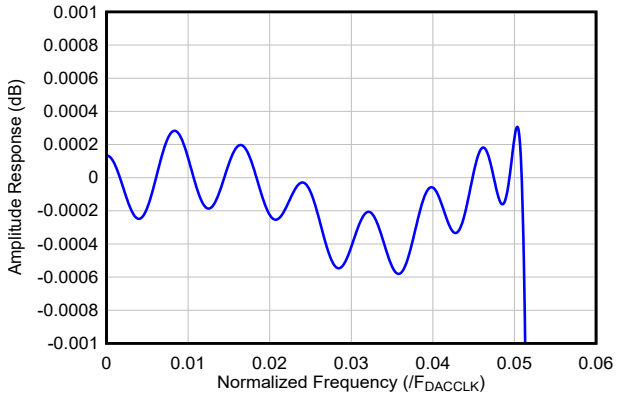


Figure 7-16. 8x Interpolation Filter Passband Response

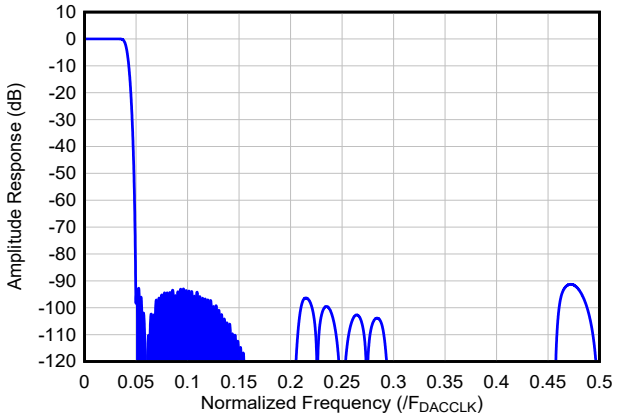


Figure 7-17. 12x Interpolation Filter Response

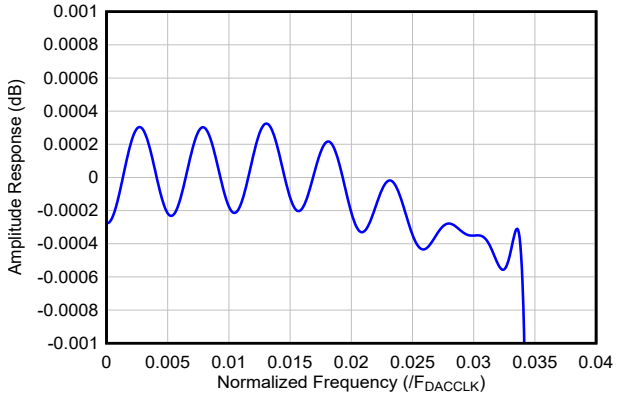


Figure 7-18. 12x Interpolation Filter Passband Response

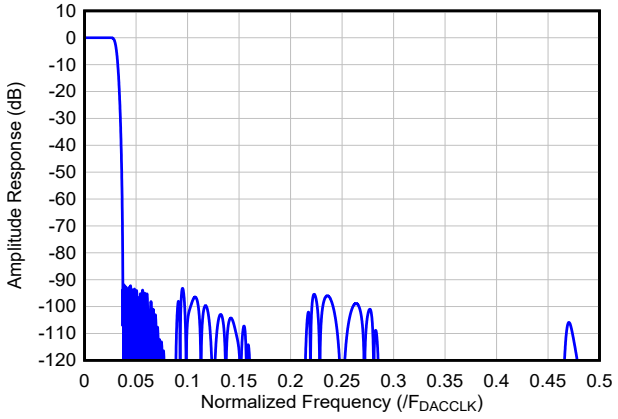


Figure 7-19. 16x Interpolation Filter Response

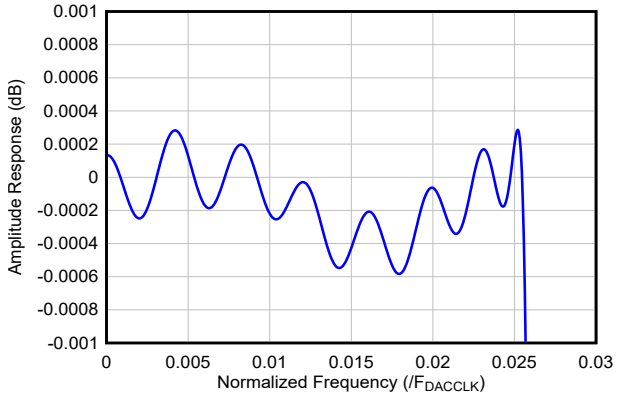


Figure 7-20. 16x Interpolation Filter Passband Response

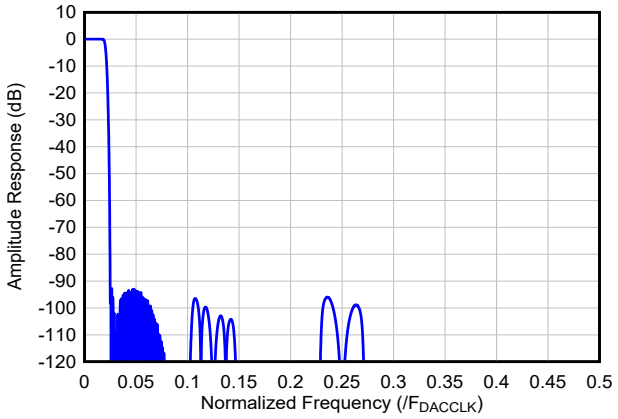


Figure 7-21. 24x Interpolation Filter Response

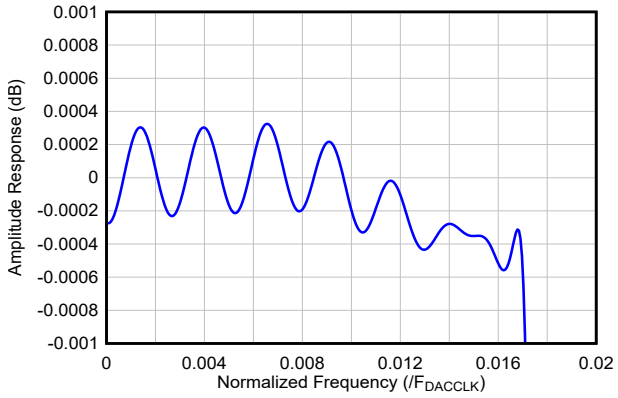


Figure 7-22. 24x Interpolation Filter Passband Response

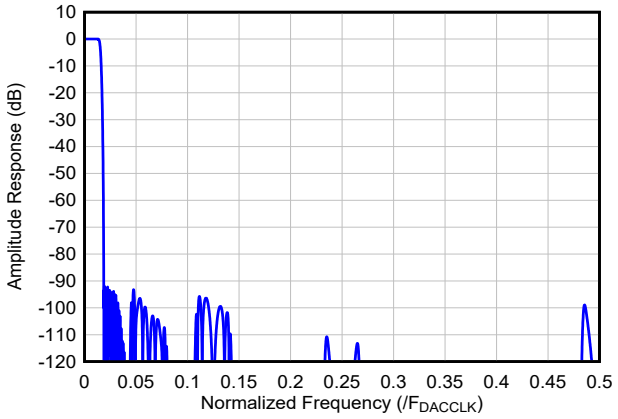


Figure 7-23. 32x Interpolation Filter Response

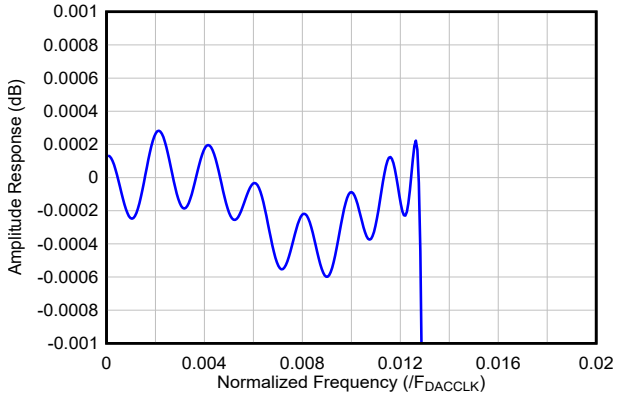


Figure 7-24. 32x Interpolation Filter Passband Response

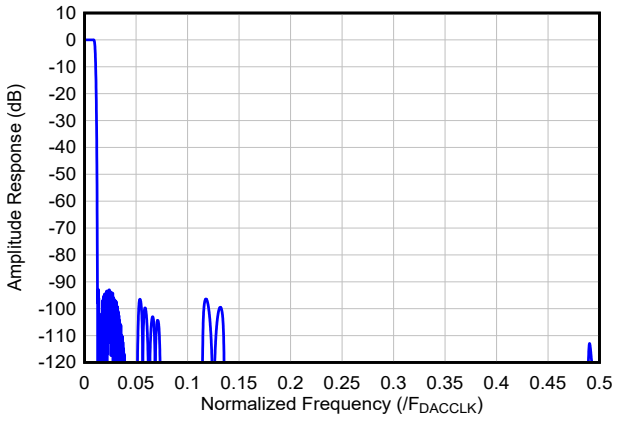


Figure 7-25. 48x Interpolation Filter Response

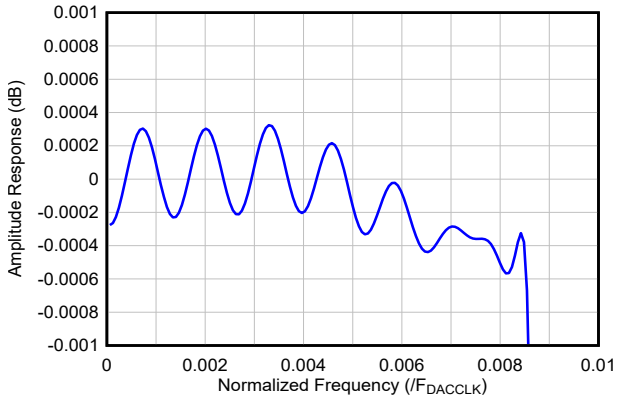


Figure 7-26. 48x Interpolation Filter Passband Response

ADVANCE INFORMATION

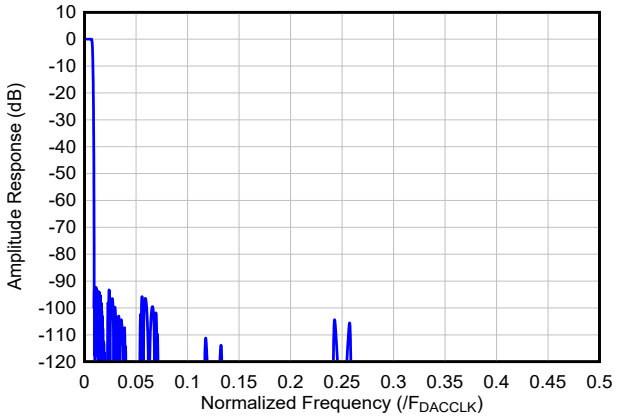


Figure 7-27. 64x Interpolation Filter Response

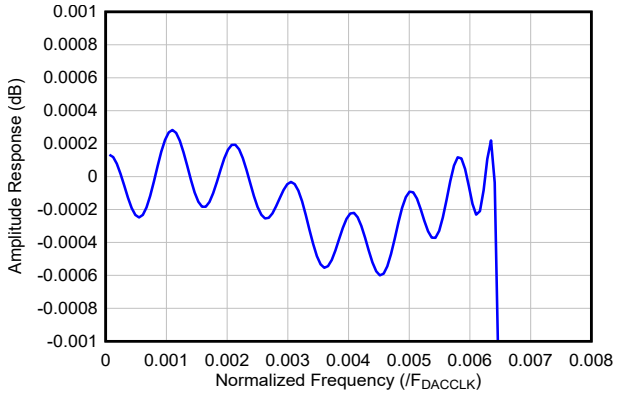


Figure 7-28. 64x Interpolation Filter Passband Response

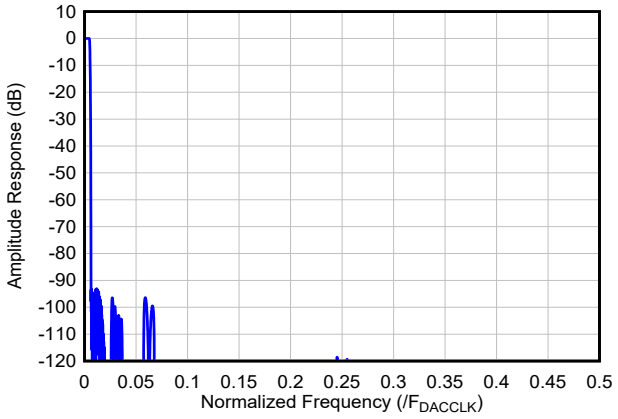


Figure 7-29. 96x Interpolation Filter Response

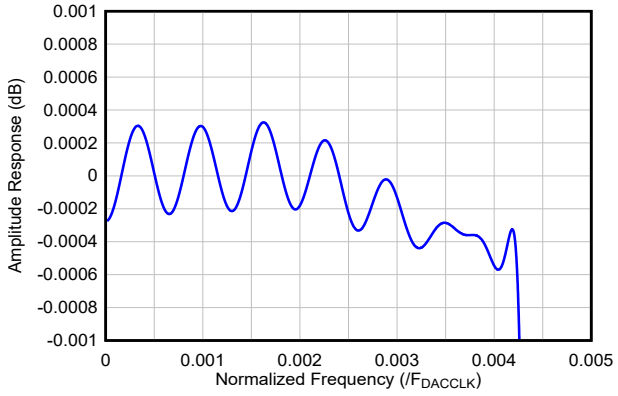


Figure 7-30. 96x Interpolation Filter Passband Response

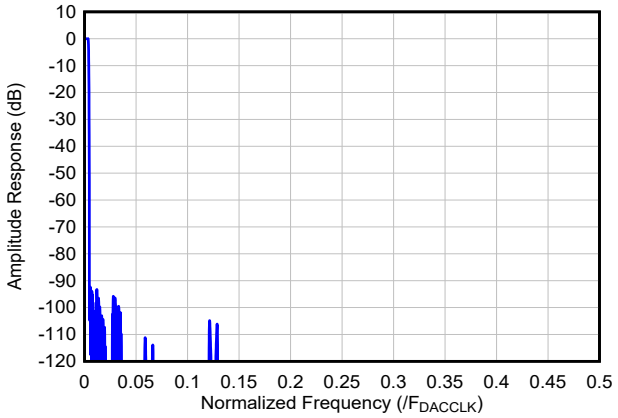


Figure 7-31. 128x Interpolation Filter Response

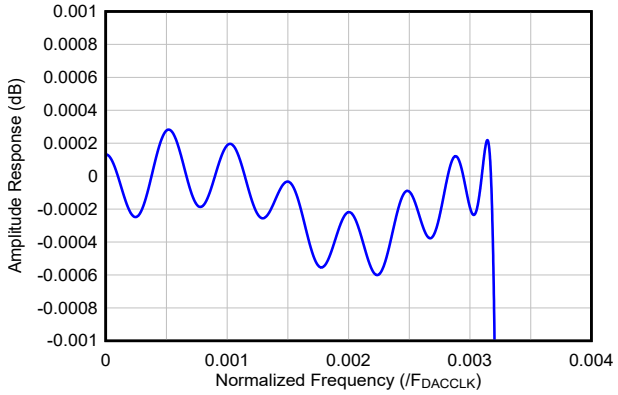


Figure 7-32. 128x Interpolation Filter Passband Response

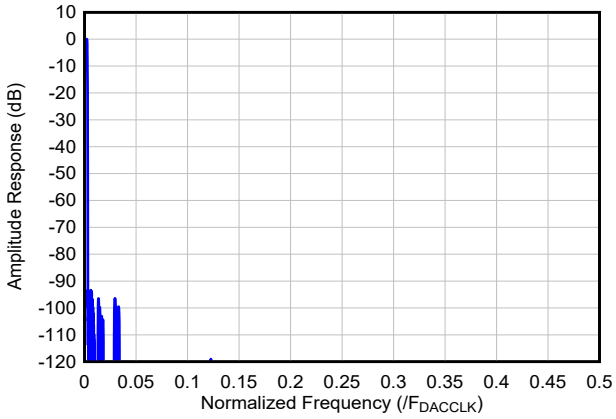


Figure 7-33. 192x Interpolation Filter Response

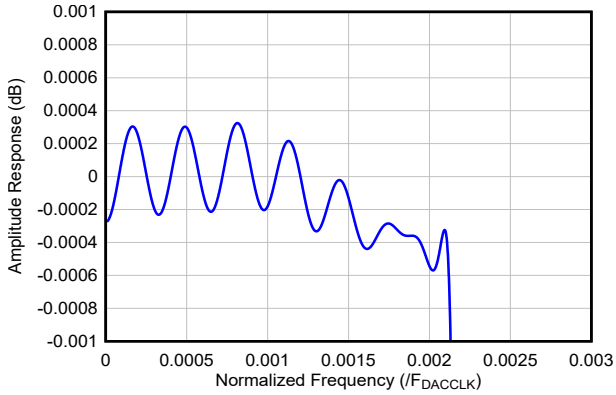


Figure 7-34. 192x Interpolation Filter Passband Response

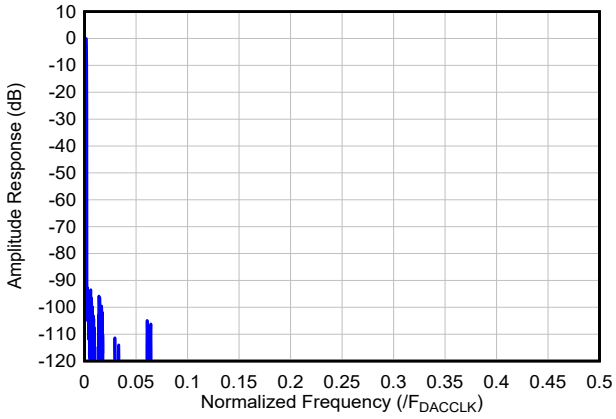


Figure 7-35. 256x Interpolation Filter Response

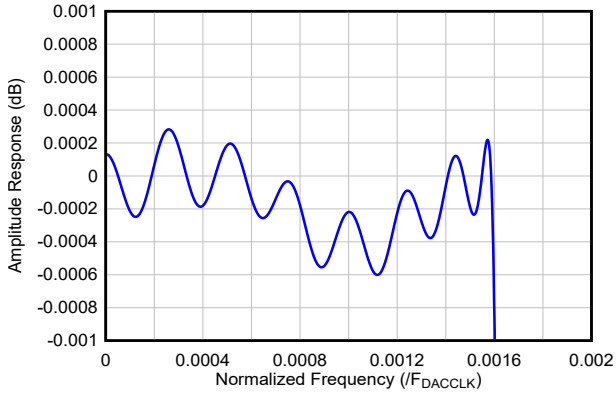


Figure 7-36. 256x Interpolation Filter Passband Response

ADVANCE INFORMATION

7.3.6.2.1.2 Numerically Controlled Oscillator (NCO)

Each DUC has its own NCO block that is capable of phase continuous frequency hopping and phase coherent frequency hopping through a NCO with 64-bit frequency and 16-bit phase words. The NCO provides the complex continuous wave signal that is used for the complex mixing operation. The NCOs can also be used in DDS SPI mode with a constant input to generate tones.

The NCO has a worst case SFDR < -96dBc when the frequency is set exactly to (2*N - 1)/32 or (2*N+1)/64 (N is an integer). For other frequencies the worst case SFDR is < -105dBc.

The NCO update modes are either Phase-continuous (see Phase-continuous NCO Update Mode), Phase-coherent (see Phase-coherent NCO Update Mode or Phase-sync (see Phase-sync NCO Update Mode). If only a single NCO frequency is required (no frequency hopping) then select the Phase Continuous NCO.

The NCO frequency is written to the NCO frequency word register setting through the standard SPI interface or through the fast reconfiguration interface (FRI). The frequency update occurs once triggered by the chosen trigger source selected by TRIG_TYPEn. Available trigger sources are a SPI register, the SYSREF signal, replacing the LSB of the I input signal with a sync signal, a TRIG pin or the rising edge of $\overline{\text{FRCS}}$ when the FRI is used.

7.3.6.2.1.2.1 Phase-continuous NCO Update Mode

In phase-continuous NCO update mode, the phase and/or frequency is updated without reset of the phase accumulator, which maintains the current sinusoid phase when changing frequency to reduce discontinuities in the output response. Phase Continuous NCO Mode operation is demonstrated in Figure 7-37.

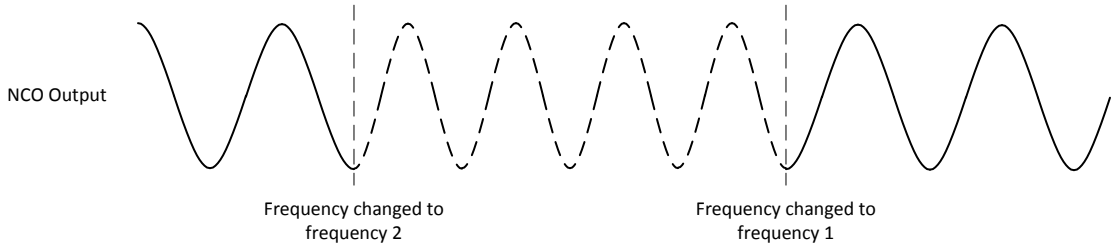


Figure 7-37. Example of Phase Continuous NCO Mode Operation

7.3.6.2.1.2.2 Phase-coherent NCO Update Mode

The phase-coherent NCO update mode, the frequency word is updated and is multiplied by a counter to update the accumulator. This allows the phase for a particular frequency to be "coherent" with the previous usage of the frequency as if the NCO had never been tuned away from that frequency. Since the phase information is maintained by the counter, any frequency can be phase coherent. Phase Coherent NCO Mode operation is demonstrated in Figure 7-38.

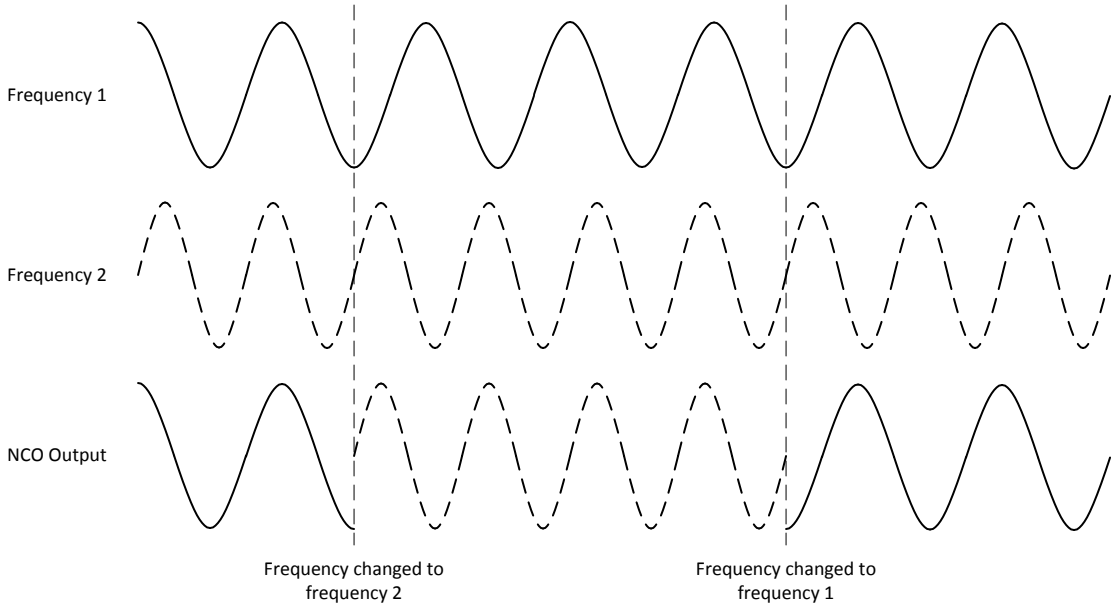


Figure 7-38. Example Phase Coherent NCO Mode Operation

7.3.6.2.1.2.3 Phase-sync NCO Update Mode

In Phase-sync NCO update mode, the frequency word is updated (if it changed) and the accumulator is reset to the initial phase value. This mode can be used to align the NCOs across multiple devices by providing a synchronization signal simultaneously across all devices.

ADVANCE INFORMATION

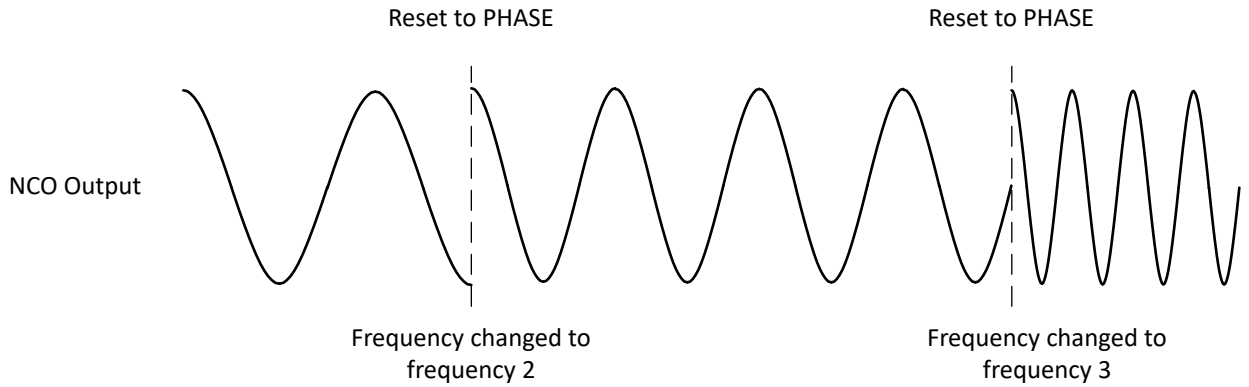


Figure 7-39. Phase-sync NCO Update Mode

7.3.6.2.1.2.4 NCO Synchronization

Many systems require synchronization between DAC channels including the phase of the internal NCOs when using digital up-conversion features. Further, frequency hopping systems may have additional requirements for synchronized frequency hopping to maintain NCO synchronization during changes in NCO frequency. The device has a number of ways to update NCO changes. These include:

- Synchronization through the LSB of the "I" input of DUC0 in the JESD204C input data stream
- Synchronization through SYSREF
- Synchronization through rising edge of TRIG[3:0] pins
- Update by the rising edge of $\overline{\text{FRCS}}$ when FR interface is used
- Update through SPI_SYNC register bit

The method used for NCO synchronization is controlled through the register setting of TRIG_TYPE.

The JESD204C LSB approach allows the synchronization information to be embedded in the input data, and therefore; can be easily controlled by the data source (that is, FPGA). By controlling the timing of the synchronization bit across multiple devices, multi-device synchronization can be achieved. LSB synchronization is covered in detail in JESD204C LSB Synchronization.

Synchronization by issuing a SYSREF pulse requires a DC coupled SYSREF interface and the ability to issue a single SYSREF pulse unless the NCO frequency is an integer multiple of the SYSREF frequency. Many systems will use AC coupled SYSREF signals which eliminates the ability to reliably issue a single SYSREF pulse. Careful timing of the SPI interface, especially for slow SYSREF signals (< 10 MHz), may make masking and unmasking of SYSREF at multiple devices possible. However, it is not characterized since the SPI path is asynchronous.

For synchronization using the synchronous trigger interface, a rising edge on TRIG pin latched by TRIGCLK immediately triggers DSPn actions. The register TRIG_SEL determines which external trigger pin is bound to each DSP channel. If the trigger interface is configured as the FRI interface, either TXEN0/1 (when assigned by TX_PIN_FUNC0/1 registers) or $\overline{\text{SYNC}}$ (when assigned by SYNCB_PIN_FUNC register) can be programmed as trigger pins.

With SPI_SYNC synchronization, The register TRIG_SEL determines which TRIG_SPI bit is bound to each DSP channel.

7.3.6.2.1.2.4.1 JESD204C LSB Synchronization

The DSP blocks , for example the NCO, can be synchronized using the LSB of the "I" input of the DUC0 channel on the JESD204C interface in complex input JMODES. Control bits that replace the LSB of the data bits are used as a trigger event for synchronization. Table 7-8 shows how the SYNC bit replace the I sample LSB when using LSB replacement. The LSB replacement mode is enabled when the SPI_SYNC register bit is high. To trigger the event, the LSB must be low for 4 or more consecutive samples, and then high for 4 consecutive samples. When using the SPI interface to update the NCO frequency word, the user must set SPI_SYNC back

ADVANCE INFORMATION

to 0 to change back to the LSB representing I sample data. When using the FR interface to update the NCO, the LSB changes back to representing the I sample data after the synchronization event is triggered.

Table 7-8. Bit Assignment using LSB Replacement

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I Sample	I[15:1]															Sync
Q Sample	Q[15:0]															

7.3.6.3 DDS SPI Mode

In DDS SPI mode (see Figure 7-40), the NCO is controlled using the FREQ and PHASE registers. Samples from the JESD204C interface are not used by the DSP, and the mixer is used to scale the amplitude of the NCO output using the AMP register. This mode is useful for generating cosine tones with indefinite duration. The user can change the amplitude, frequency, and phase at any time by updating the AMP, FREQ, and PHASE registers and then generating a DSP trigger event (see DSP Triggering).

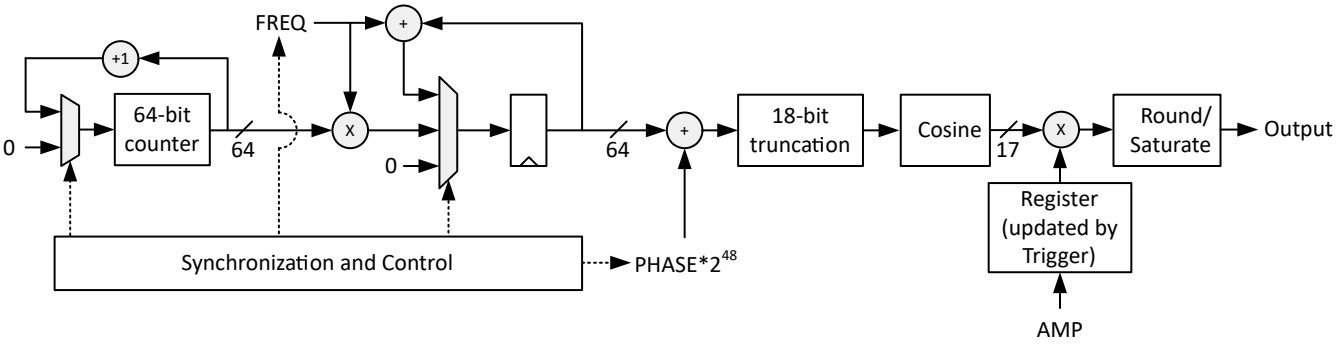


Figure 7-40. DDS SPI Mode Block Diagram

DDS SPI Mode supports the same NCO trigger features as the DUC mode:

- Phase-Continuous mode: Trigger event updates frequency, but phase accumulator is not reset (NCO_CONT=1, NCO_AR=0).
- Phase-Sync mode: Trigger event updates frequency and resets phase accumulator (NCO_AR=1)
- Phase-Coherent mode: Trigger event updates frequency and phase accumulator is seeded from counter (NCO_CONT=0, NCO_AR=0)

7.3.6.4 DDS Vector Mode

Any DSP channel can operate in DDS Vector mode (see DSP_MODE*n*). In this mode, the interpolation filters are disabled and the NCO/Mixer logic is repurposed to generate user-defined waveforms (defined by DDS_VEC). The DSP does not require any input samples from the JESD interface.

Table 7-9. Terms and Definitions for DDS Vector Mode

Term	Definition
Vector Field	Each DDS Vector is made up of several fields that define signal attributes to produce a waveform segment. Example fields are PHASE_START and FREQ_START.
Vector	A vector is one entry in the vector table and contains fields which define a waveform segment (see DDS_VEC)
Vector Table	A table of vectors that are used by the DDS (see DDS_VEC).
Vector Block	A portion of the vector table assigned to a DDS channel (a subset of DDS_VEC)
Waveform Segment	A signal that the DDS produces based on a single vector in the vector table.
Waveform	A signal that is produced by playing a sequence of waveform segments
Stalled	The vector processor is stalled when waiting for a trigger event. This always occurs at startup. Stalling also occurs if a vector is loaded that has the vector's VTRIG_MODE field set and no trigger is active or already queued in the trigger queue. In general, the DDS output is muted while the vector processor is stalled; however, Hold mode defines an exception to this.

The DDS Vector mode synthesizer is shown in Figure 7-41. Key features are:

- Generates waveforms by playing a sequence of waveform segments.
- Each waveform segment is defined by a vector in the vector table (DDS_VEC).
- Four DDS channels can each produce independent waveforms.
- DDS channels can be disabled to allow more vectors to be used by the remaining channels.
- Each vector contains fields to define the initial amplitude, frequency, and phase of the waveform segment. Amplitude and frequency can also be ramped up or down, and the duration of the waveform segment can be defined (see DDS_VEC).
- Second order amplitude ramping is possible (DDS_AMP2).
- Up to 256 vectors are available.
- Upon startup, playback does not begin until a trigger event occurs.
- Playback can be stalled at the start of specific vectors and the DDS waits for a trigger to continue (output is muted during the waiting period, unless Hold Mode is active) (see VTRIG_MODE)
- A single trigger input event can play a waveform multiple times (DDS_BURST).
- A 'Symmetric Mode' can instruct the DDS to play vectors in ascending order and then again in descending order (for symmetric Frank codes) (DDS_SYM)
- The Indexing Mode allows the TRIG[4:1] inputs to instruct the DDS to jump to specific sections of vector memory. When Indexing Mode is enabled, only one DSP channel is used for DDS Vector mode.

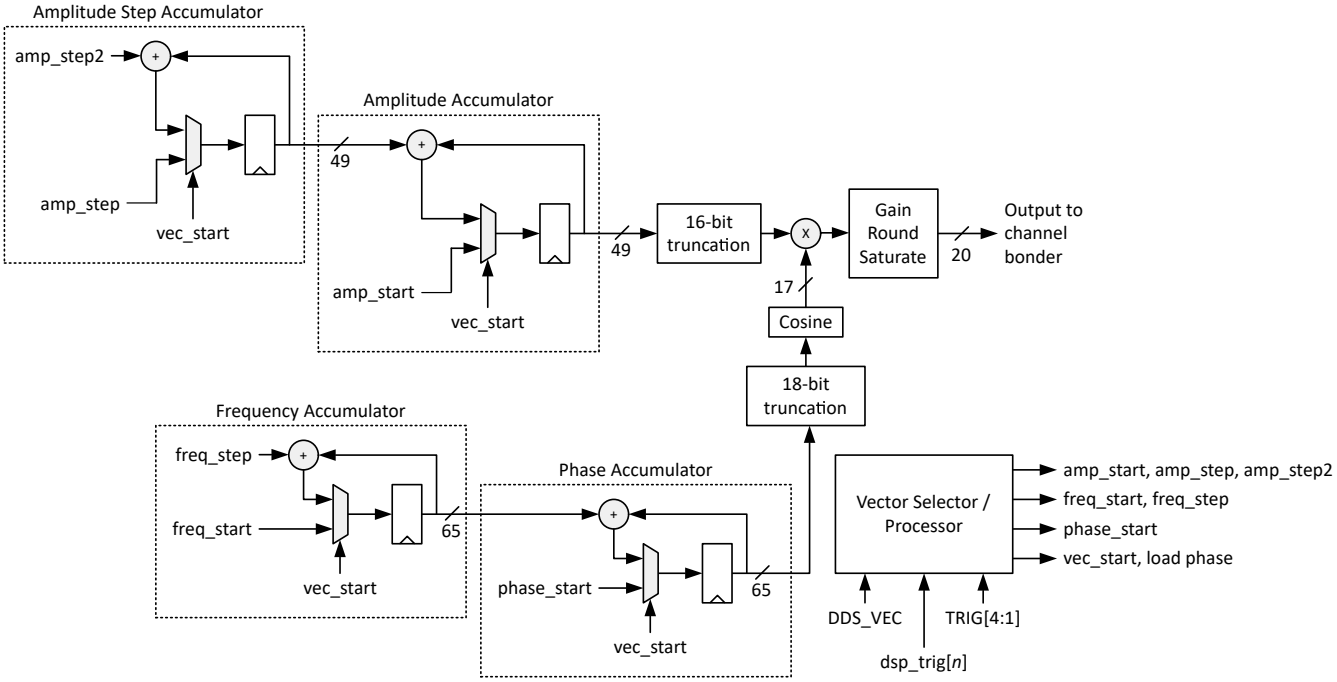


Figure 7-41. DDS Vector Waveform Generator

The vector table (defined by DDS_VEC) is divided into blocks and assigned to the DSP channels. The DSP channels are grouped into channel sets (channel 0 and 2 are grouped and channel 1 and 3 are grouped). When both DSP channels in a group are in DDS-Vector mode, the memory is shared between the two channels. This is depicted in Table 7-10. Each DDS channel executes the vectors in the channel's assigned vector block in ascending order, starting with the lowest index. When a DDS channel finishes playing a vector, the channel inspects the LAST_VEC field of that vector. If LAST_VEC=1, the channel starts over at the beginning of the channels assigned vector block.

ADVANCE INFORMATION

Table 7-10. Vector Blocks Assigned to Channels for DSP0/2 Configurations

Vector Range	If channel 2 is NOT in DDS-Vector Mode	If channel 0 is NOT in DDS-Vector Mode	If channel 0 and 2 are both in DDS-Vector Mode
DDS_VEC[0:63]	Channel 0	Channel 2	Channel 0
DDS_VEC[64:127]			Channel 2

Table 7-11. Vector Blocks Assigned to Channels for DSP1/3 Configurations

Vector Range	If channel 3 is NOT in DDS-Vector Mode	If channel 1 is NOT in DDS-Vector Mode	If channel 1 and 3 are both in DDS-Vector Mode
DDS_VEC[128:191]	Channel 1	Channel 3	Channel 1
DDS_VEC[192:255]			
DDS_VEC[256:319]			Channel 3
DDS_VEC[320:383]			

The mapping in the above tables allows channel 0 and 2 to share resources. Similarly, channel 1 and 3 share resources.

More memory is allocated to channels 1 and 3. This maximizes the available memory when combining DDS-Vector mode with DUC or DDS-Stream modes. In those mixed configurations, the DDS-Vector mode applies to channels 1, 2, and/or 3, but not channel 0.

The Vector Processor is responsible for reading each vector, formatting and scaling the parameters, and applying them to the DDS accumulators for the proper duration of time.

Table 7-12 defines how the parameters produced by the Vector Processor. All references to DDS vector fields refer to the field of the specific vector being played.

Table 7-12. DDS Vector Fields

Signal	Format	Description
step_exp	Integer	Step exponent. Ranges from -4 to -32. The purpose of this value is to apply a scaling factor to the amplitude and frequency step that is appropriate for the duration of the vector. Longer vectors use a smaller scaling factor (larger STEP_EXP value). step_exp = -STEP_EXP - 1 The recommended value for the STEP_EXP field of each vector is: STEP_EXP = floor(log2(NUM_SAMP_M32+32)) - 1
amp_start	49-bit signed	Initial value for amplitude accumulator. Applied when a vector begins. amp_start = AMP_START * 2^{33} amp_start can be set to zero to mute the DDS output while waiting for a trigger.
amp_step	49-bit signed	Initial value for amplitude step accumulator. amp_step =AMP_STEP * 2^{33} * 2^{step_exp} + amp_step/2 Note: The “amp_step2/2” term makes sure that the sequence of amplitude values follows a simpler quadradic equation.
amp_step2	49-bit signed	Step for amplitude step accumulator (2nd order term). Applied during the entire vector. This term only applies when 2nd-order amplitude is enabled (see DDS_AMP2) amp_step2 = AMP_STEP2 * 2^{33} * 4^{step_exp}
freq_start	65-bit	Initial value for frequency accumulator. Applied when a vector begins. freq_start =FREQ_START * 2^{17} + freq_step/2 Note: The “freq_step/2” term makes sure that the sequence of phase values follows a simpler quadradic equation. Note: When 2^{nd}-order amplitude is enabled (see DDS_AMP2), the lower 16-bits of FREQ_START are used for amplitude control, and the formula above for freq_start assumes those 16-bits are zero.

Table 7-12. DDS Vector Fields (continued)

Signal	Format	Description
freq_step	65-bit	Step value for frequency accumulator. Applied during the entire vector. freq_step = FREQ_STEP * 2^{33} * 2^{step_exp}
phase_start	65-bit	Initial value for phase accumulator. Applied when a vector begins. phase_start = PHASE_START * 2^{49}
vec_start	1-bit	Control signal indicating the start of a vector. Causes the accumulators to initialize. Asserted for one sample period. If the Vector Processor encounters a vector that requires a trigger (and no trigger is in the queue), the vec_start signal is asserted, but amp_start and amp_step are set to zero to mute the DDS output. Once the trigger occurs, vec_start is asserted again but this time with amp_start and amp_step configured normally to start the vector. If Hold Mode is active, no mute is generated. The amp_start and amp_step signals are not set to zero and vec_start is not pulsed a second time in response to the trigger event (because the vector is already playing).
load_phase	1-bit	When Hold Mode is disabled, the load_phase signal matches the vec_start signal (the phase accumulator loads phase_start). When Hold Mode is enabled, load_phase remains low to achieve phase-continuous operation.

7.3.6.4.1 Second Order Amplitude Support

By default, the vector engine does not support second-order amplitude ramping. However, this mode can be enabled using the DDS_AMP2 register. This mode allows smooth and accurate amplitude curves to be generated. When this mode is enabled, a few important changes occur:

1. The maximum length of each vector is 65536 samples (NUM_SAMP_M32 must be 65504 or less).
2. The lower 16-bits of the FREQ_START field of every vector are re-purposed to define the 2nd order amplitude step value which is a 16-bit signed value (AMP_STEP2). This reduces the resolution of the initial frequency to 32-bits (the lower 16-bits of FREQ_START are assumed to be zero for the purposes of defining the initial frequency).
3. The maximum supported value of STEP_EXP becomes 15 (step_exp = -16).

7.3.6.4.2 Vector Order and Symmetric Vector Mode

Each DDS channel has a local vector pointer that is updated after each vector is completed. The local vector pointer is added to a channel offset to index into DDS_VEC. The channel offset for each channel depends on how many channels are enabled, and is listed in Table 7-13.

Table 7-13. Channel Offset for DDS_VEC

Channel	Channel Offset
0	0
1	128
2	0 (or 64 if DSP channel 0 is also in vector mode)
3	128 (or 256 if DSP channel 1 is also in vector mode)

When symmetric mode is disabled (DDS_SYM=0), the local pointer starts at channel offset value and increments after each vector is completed. Once a vector is completed that has the LAST_VEC field set (=1), the pointer returns to the channel offset value and the incrementing sequence repeats.

Here is an example sequence for the local vector pointer (DDS_SYM=0, vector 5 has LAST_VEC=1) with channel offset = 0:

0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5, …

ADVANCE INFORMATION

When symmetric mode is enabled by setting DDS_SYM, the pointer does not reset to the channel offset value after playing a vector with LAST_VEC set. Instead, the pointer begins decrementing until reaching the channel offset value, then begins incrementing again (the channel offset vector is played twice).

Here is an example sequence for the local vector pointer (DDS_SYM=1, vector 5 has LAST_VEC=1) with channel offset = 0:

0, 1, 2, 3, 4, 5, 4, 3, 2, 1, 0, 0, 1, 2, 3, 4, 5, 4, 3, 2, 1, 0, 0, 1, 2, 3, 4, 5, …

Note that vector 5 is played ***once,*** but vector 0 is played ***twice*** (to support symmetric Frank codes). The vectors in the decrement phase are underlined above. During the decrement phase, the VTRIG_MODE field of the vectors are ignored and vectors are processed as if VTRIG_MODE was 0. This makes sure a complete symmetric waveform is played without requiring a trigger during the second half of the waveform.

Note that symmetric mode is intended for Frank codes (phase modulation with a symmetric phase sequence). While the waveform segments are played in reverse order, the actual samples that make up the waveform segments are not reversed in time (not played backwards).

7.3.6.4.3 Initial Startup

The vector processor is enabled whenever SYS_EN=1 and the datapath is not in APP Sleep. Once enabled, the processor waits for a trigger to begin operation. Some important notes about the startup:

1. Upon startup, the vector processor fetches the first vector from the Vector Block.
2. If Hold Mode is disabled (DDS_HOLD[n]=0) the processor behaves as if the first vector has VTRIG_MODE set. The DDS output remains muted until the first trigger occurs. When returning to the first vector later, VTRIG_MODE is honored normally.
3. If Hold Mode is enabled (DDS_HOLD[n]=1) the DDS output is muted upon startup. Once a trigger is received, the first vector begins playback, but the processor remains stalled if VTRIG_MODE=1 and a second trigger is required to complete the first vector.
4. Assuming the processor is waiting for a trigger, the latency for all trigger events to the DAC output are the same, regardless of whether the trigger initializes playback or resumes playback.

7.3.6.4.4 Trigger Queuing

If a DDS channel is not stalled, but a trigger event is received anyway, the event is queued and consumed at a later time. This is implemented with an event counter. A received trigger event increments the counter. Playing a vector that requires a trigger decrements the counter. If the counter is zero and a vector requires a trigger, playback is stalled until a trigger event is received. Up to 65535 trigger events can be queued. Triggers beyond that limit are discarded (the counter saturates at 65535).

7.3.6.4.5 Trigger Burst

The DDS_BURST registers can be programmed (one per DDS channel) to enable burst triggering. Burst triggering allows each received trigger event to add DDS_BURST+1 events to the trigger queue (see Trigger Queuing) (one event is consumed immediately if the DDS is stalled). This is useful for radar applications that need to send a series of identical waveforms in a burst.

7.3.6.4.6 Hold Mode

The DDS_HOLD[n] register can be set to enable Hold Mode on DDS channel n. This allows the DDS to hold on a vector to generate a tone with an indefinite length (and constant frequency and amplitude), and then use the trigger to initiate a frequency or amplitude ramp, and then hold again at a different frequency and/or amplitude. When Hold Mode is activated, the following changes apply:

1. The initial trigger that enables the DDS output does not also satisfy the trigger condition of the first vector. See Initial Startup for full details.
2. After the initial trigger, whenever the vector processor is stalled, the DDS output is not muted. Instead, the vector is started, but runs indefinitely (waiting for a trigger event). Once a trigger event occurs, the DDS plays NUM_SAMP_M32+32 additional samples of the current vector before continuing to the next vector.

3. The phase accumulator operates in phase-continuous mode. This makes sure phase continuous behavior when starting each vector. The PHASE_START value of the first vector is applied once when the first trigger occurs after startup, but then the PHASE_START values are ignored for all subsequent operations.
4. The length of each vector must be a multiple of 32 (the NUM_SAMP_M32 field of all vectors must be a multiple of 32).
5. Indexing-Mode must be disabled (DDS_IMODE=0).
6. Symmetric mode must be disabled (DDS_SYM[n] must be 0 when DDS_HOLD[n] is 1).

(move to typical application example) Below is an example use case for a smooth transition between arbitrary frequencies and/or amplitudes. In this description, vector numbers are offsets within the channel vector block.

1. **Set up initial frequency/amplitude:**
   a. Enable Hold Mode (DDS_HOLD) and program vector 0 (DDS_VEC) to the initial desired frequency and amplitude:
      i. FREQ_START = desired frequency;
      ii. AMP_START = desired amplitude;
      iii. NUM_SAMP_M32 = 0; FREQ_STEP = 0; AMP_STEP = 0; STEP_EXP = 0; VTRIG_MODE = 1; LAST_VEC = 0;
   b. Start the DDS (SYS_EN=1).
   c. The DDS plays vector 0 indefinitely, and waits for a trigger.
2. **Ramp to a new frequency/amplitude:**
   a. Once a new frequency or amplitude is desired, program vector 1 to generate a frequency or amplitude ramp that starts at the initial frequency/amplitude (from step 1), and ends at the new frequency and amplitude. Set VTRIG_MODE to 0. The duration of the ramp is set by NUM_SAMP_M32. Program appropriate values for FREQ_STEP, AMP_STEP and STEP_EXP. Program VTRIG_MODE = 0 and LAST_VEC = 1.
   b. Update vector 0 with the new frequency/amplitude (it does not have any effect yet). Other fields of vector 0 can remain unchanged (same as step 1).
   c. Trigger the DDS using any triggering method. This causes the DDS to play vector 1 (the ramp) and then return to vector 0 (which is the new frequency and/or amplitude). The DDS then holds indefinitely on vector 0.
3. **Once a new frequency or amplitude is desired, repeat step 2.**

7.3.6.4.7 Indexing Mode

Indexing Mode is enabled by setting DDS_IMODE=1. Indexing Mode allows the TRIG[4:1] pins to select one of 16 locations in the vector memory to jump to when the DDS is triggered by TRIG[0]. This allows the user to have random access to 16 sections of vector memory (triggering one of several different waveforms).

Any DSP channel can operate in indexing mode, but the user must configure the DSP channel to be triggered by TRIG[0] by programming TRIG_TYPE*n*=4 and TRIG_SEL*n*=0. Multiple DSP channels can simultaneously operate in indexing mode, but the DSP channels all share the TRIG[4:0] pins, so the user cannot uniquely index the channels. Note that DSP channel 0 and 2 do not have access to as many vectors and are therefore not good choices for the indexing mode. Channel 3 is recommended for indexing mode so that 16 unique locations can be indexed. If the user attempts to jump to a vector number that is larger than the number of vectors allocated to the channel, the address is aliased back into the channel's allocation.

In Indexing-Mode, vectors are processed normally, but with the following changes:

1. Each time the DDS receives a trigger, the current value of TRIG[4:1] is multiplied by 16 and stored in an internal register named VINDEX.
2. If the DSP channel only has access to 128 vectors, then bit 7 of VINDEX is ignored (address aliasing). If only 64 vectors are available, then bit 7 and 6 are both ignored.
3. If a trigger is received *while the processor is waiting for a trigger*, the VINDEX register is updated, and then the processor jumps to the vector specified by VINDEX and immediately plays that vector. The trigger is

consumed if the new vector has VTRIG_MODE=1, otherwise the trigger is placed into the trigger queue. If DDS_SYM=1, VINDEX is copied to VSYM (the vector processor memorizes the starting index of symmetric playback so to decrement the index later).
4. If a trigger is received while the processor is *not waiting for a trigger*, the VINDEX register is updated, and the trigger is placed into the queue, but playback is not interrupted. The new value of VINDEX can be consumed later (see following items).
5. When DDS_SYM=0 (non-symmetric mode), and the processor completes a vector with LAST_VEC=1, the processor jumps to the vector specified by VINDEX (instead of setting the vector pointer to 0).
6. 5. When DDS_SYM=1 (symmetric mode), and the vector pointer is in the decrement phase, the vector pointer does not decrement to VINDEX, but instead decrements to VSYM. Once the vector specified by VSYM is completed, the symmetric sequence is complete, so the processor jumps to the vector specified by VINDEX and sets VSYM=VINDEX (This definition allows one symmetric sequence to be queued while another one is being executed).

7.3.6.4.8 Queued or Burst Triggers in Indexing-Mode

There is only one VINDEX register and the value is overwritten each time a trigger is received. This means the user cannot queue up multiple trigger events with *unique* VINDEX values. However, the stored VINDEX value can be re-used by the DDS multiple times. For example, if DDS_BURST=3, a single trigger event plays a specific waveform 4 times. Operation for this example is detailed below:

1. Assume the DDS is waiting for a trigger and DDS_SYM[0]=0 (non-symmetric mode).
2. Assume DDS_VEC[80].VTRIG_MODE=1.
3. TRIG[0] rises with TRIG[4:1]=5. The DDS sets VINDEX=5*16=80. The DDS begins playback of vector 80 (one trigger is consumed and 3 trigger events are queued since DDS_BURST=3).
4. The DDS plays vector 80 through 83.
5. DDS_VEC[83].LAST_VEC=1, so the DDS jumps to DDS_VEC[VINDEX] (this is vector 80 since VINDEX has not been changed). Since DDS_VEC[80].VTRIG_MODE=1, one trigger event is removed from the queue.
6. Vectors 80 through 83 are played a total of 4 times (with zero gaps in the playback). After the fourth playback, the trigger queue is empty, so the DDS stops (mutes) and waits for a trigger again.

7.3.6.4.9 Writing Vectors While DDS is Enabled

The user can write to the DDS Vectors (DDS_VEC) while the DDS is enabled (SYS_EN=1); however, the user *must make sure* the DDS never attempts to read any vectors while the vectors are being written. This can be accomplished using one of several methods:

1. If a DDS channel is idle (waiting for a trigger), the user can write to any vector that is allocated to that channel. However, the user must not change the VTRIG_MODE field of the vector that the DDS is idling on.
2. In Indexing Mode, the user can write to vectors in sections of the vector table that are not currently being played (because the TRIG[4:1] inputs are not activating them).
3. If the DDS is active, but eventually stops to wait for a trigger, the user can write vectors that are beyond the stop point if the user can make sure the vectors are written before the DDS is triggered to read them.

7.3.6.5 DDS Streaming Mode

DDS Stream mode allows to user to send a continuous stream of frequency/phase/amplitude values to the DDS using the JESD204C Interface. This mode is useful for frequency/phase/amplitude modulation/keying. Frequency streaming can also be used to generate complex chirp signals over a wide frequency range while using less JESD204C bandwidth compared to DUC mode.

To put a DSP channel into DDS Stream mode, program DSP_MODE*n* to DDS Stream mode. DDS Stream mode supports input sample rates of $F_{DACCLK}/16$, $F_{DACCLK}/32$, or $F_{DACCLK}/64$. This is configured by programming the DSP_L register to set the DDS Upsampling factor to 16, 32, or 64. The user must select a JMODE that supports 16-bit samples and supports an LT value that matches the DDS Upsampling factor (16, 32, or 64).

Table 7-14 summarizes some key features of DDS Stream mode.

Table 7-14. Summary of DDS Streaming Mode

Property/Feature	Details
Supported JMODEs:	Any 16-bit JMODE that supports the desired setting for JESD_M and DSP_L
Number of JESD204C Converters (streams) allocated to each DDS channel:	2 (32-bits)
Supported Values for JESD_M:	2, 4, 6, 8
Supported Upsampling Factor (DSP_L):	16, 32, 64
Streaming Options	Stream frequency, phase, and amplitude (STREAM_MODE[*n*]=0) Stream frequency only (STREAM_MODE[*n*]=1) Stream phase and amplitude only (STREAM_MODE[*n*]=2)
Can trigger the DDS by streaming zero amplitude:	Yes
Actions that occur when DDS is triggered:	Update non-streamed parameters from FREQ/PHASE/AMP registers. Reset phase accumulator if NCO_AR is set.

Two 16-bit JESD204C converters (streams) are allocated to each DSP channel according to Table 7-15. The user must program JESD_M to make sure that each DSP channel (that is configured in DDS Stream mode) receives two 16-bit streams. The two 16-bit streams are concatenated to produce a single 32-bit stream (referred to as sdata). The lower stream is the lower 16-bits (sdata[15:0]). The upper stream is the upper 16-bits (sdata[31:16]).

Table 7-15. Allocation of JESD204C Converters to DSP Channels (DDS-Stream Mode)

JESD204C Converter (Stream)	DSP Channel Associated with the converter	Contribution to the 32-bit DDS stream (sdata)
C0	DSP0	sdata[15:0]
C1	DSP0	sdata[31:16]
C2	DSP1	sdata[15:0]
C3	DSP1	sdata[31:16]
C4	DSP2	sdata[15:0]
C5	DSP2	sdata[31:16]
C6	DSP3	sdata[15:0]
C7	DSP3	sdata[31:16]

If FPA-Stream mode is enabled (STREAM_MODE[n]=0), the DDS interprets sdata[31:1] as frequency or phase+amplitude depending the value of sdata[0]. This is shown in Table 7-16 and Table 7-17. This allows the stream to control all parameters (frequency, phase, amplitude). The phase/amplitude samples are internally delayed by one input sample period (compared to frequency samples). This allows the user to simultaneously change all parameters by sending a phase+amplitude sample immediately followed by a frequency sample.

Table 7-16. Format of Frequency Sample (STREAM_MODE[*n*]=0)

sdata[31:1]	sdata[0]
31-bit frequency value (LSB weight is $2^{-31} * F_{DAC}$)	1'b0

Table 7-17. Format of a Phase+Amplitude Sample (STREAM_MODE[*n*]=0)

sdata[31:16]	sdata[15:1]	sdata[0]
16-bit phase value (LSB weight is $2^{-16} * 2\pi$ radians)	15-bit amplitude value (unsigned) (LSB weight is 2^{-15} * full scale)	1'b1

ADVANCE INFORMATION

When frequency data is received, the previous phase and amplitude are held. When phase/amplitude data is received, the previous frequency is held. The initial frequency, phase, and amplitude are all zero when the DDS is first enabled (by SYS_EN).

The user can also trigger the DDS by streaming a zero-value amplitude and setting thephase LSB bit PHASE[0] = 1. If NCO_AR[n] is set, this resets the phase accumulator (it resumes accumulation once the signal amplitude is non-zero). This provides a convenient way to generate frequency chirps with a consistent initial phase.

In Frequency/Phase/Amplitude or Phase/Amplitude stream modes (STREAM_MODE[*n*] = 2), the frequency is determined by the FREQ registers.

In Frequency/Phase/Amplitude or Phase/Amplitude stream modes (STREAM_MODE[*n*] = 0 or 2), streaming a zero-value amplitude causes the DDS to start using any new value in the FREQ[n] register. This trigger is decoded internally by the DDS and operates independently from the trigger sources defined in DSP Triggering.

Since the JESD204C link can experience bit errors, this can corrupt the sdata[0] bit causing the frequency, phase, or amplitude to be corrupted. The user can periodically toggle sdata[0] to stream all parameters and make sure that any corruption is overwritten periodically. If the user prefers to always send frequency data or always send phase/amplitude data, use the STREAM_MODE register to instruct the DDS to ignore the sdata[0] bit entirely. The options are listed in Table 7-18.

Table 7-18. Stream Modes Description

STREAM_MODE *n*	Description
0	FPA-Stream: Dynamically stream frequency/phase/amplitude using the sdata[0] bit.
1	F-Stream: Only stream frequency samples. The sdata[0] bit is the LSB of the frequency value, allowing 32-bit frequencies. Phase and amplitude are set by the PHASE[*n*] and AMP[*n*] registers.
2	PA-Stream: Only stream phase/amplitude samples (sdata[0] is ignored). Frequency is set by the FREQ[*n*] register.

Table 7-19. Format of Frequency Sample (STREAM_MODE[*n*]=1)

sdata[31:0]
32-bit frequency value (LSB weight is $2^{-32} * F_{DAC}$)

Table 7-20. Format of a Phase+Amplitude Sample (STREAM_MODE[*n*]=2)

sdata[31:16]	sdata[15:1]	sdata[0]
16-bit phase value (LSB weight is $2^{-16} * 2\pi$ radians)	15-bit amplitude value (unsigned) (LSB weight is 2^{-15} * full scale)	don't care

7.3.6.6 DSP Triggering

Each DSP channel can receive a trigger event from a variety of sources (see Figure 7-42 and Table 7-21). When a DSP channel receives a trigger, a number of different actions can occur depending on the DSP mode (DSP_MODE*n*), and other DSP settings. Trigger actions are summarized in Figure 7-42 and Table 7-22.

By default, all DSP channels can be triggered by changing TRIG_SPI[0] from 0 to 1 (SPI-immediate mode with all DSP channels bound to TRIG_SPI[0]).

ADVANCE INFORMATION

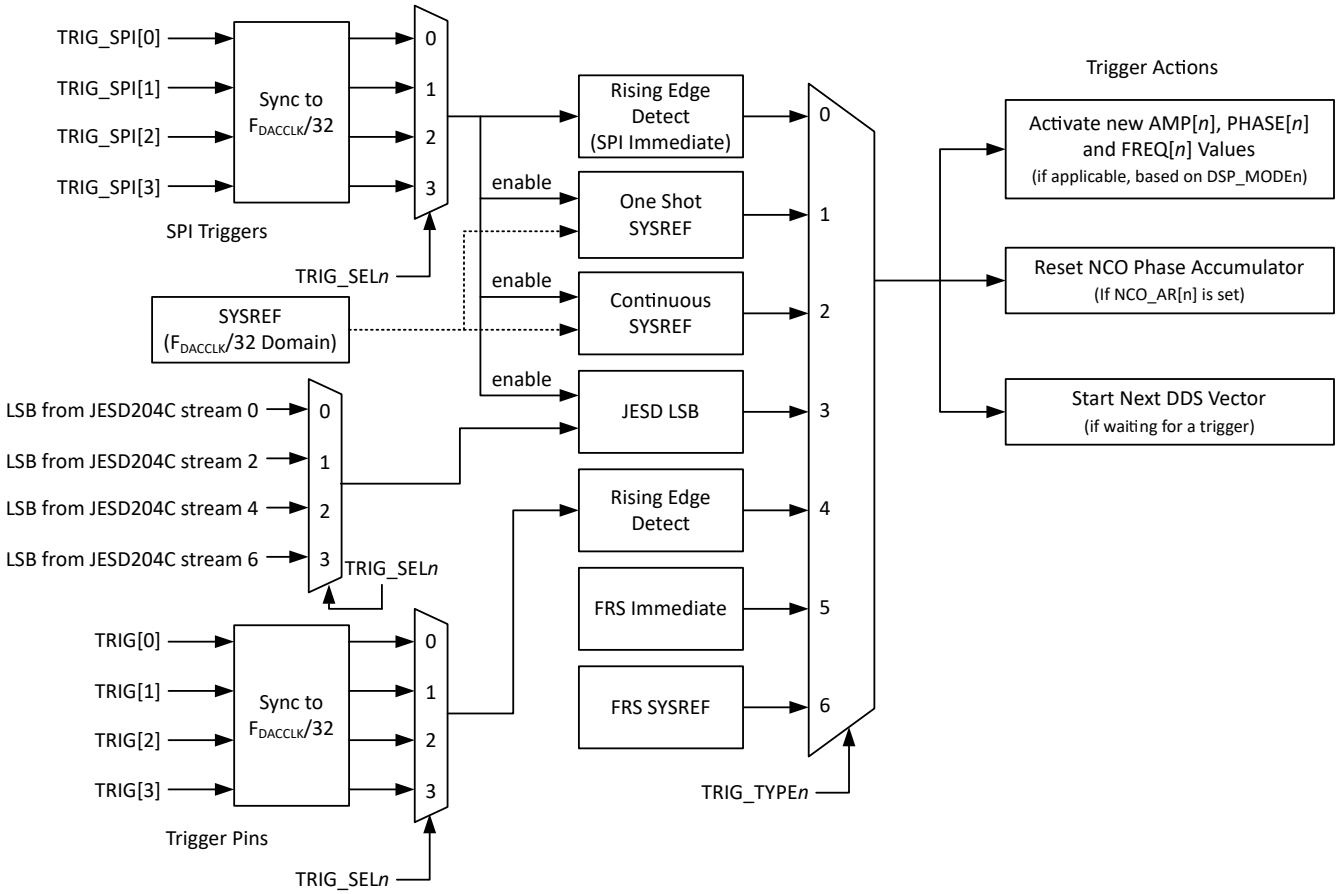


Figure 7-42. Trigger Sources and Actions for DSP*n* (one DSP channel shown)

Table 7-21. Trigger Sources / Modes

TRIG_TYPE[n] Value [2]	Trigger Source / Mode	Description
0	SPI-Immediate (default)	A rising edge on the TRIG_SPI bit that is bound [1] to DSP**n** triggers DSP**n**. *To trigger multiple DSP channels simultaneously, you must bind them to the same TRIG_SPI bit using TRIG_SEL.* . This trigger type is not designed for aligning multiple parts, since the SPI interface is asynchronous to the DSP clock.
1	SYSREF One-Shot	A rising edge on the TRIG_SPI bit that is bound [1] to DSP**n** causes the next SYSREF rising edge to trigger DSP**n**. *SYSREF can not trigger a DSP if the SYSREF timing is inconsistent with internal clocks (i.e. this causes* CLK_ALIGNED *to be low).* This trigger type can be used to align all DSPs across multiple parts, provided that all parts receive a deterministic SYSREF.
2	SYSREF Continuous	Every SYSREF rising edge triggers DSP ***n*** as long as the TRIG_SPI bit that is bound [1] to DSP ***n*** is high. *SYSREF can not trigger a DSP if the SYSREF timing is inconsistent with internal clocks (i.e. this causes CLK_ALIGNED to be low).* This trigger type can be used to align all DSPs across multiple parts, provided that all parts receive a deterministic SYSREF.
3	JESD204C LSB	The LSB of stream 0 from the JESD204C interface triggers DSP ***n*** whenever the TRIG_SPI bit that is bound [1] to DSP ***n*** is high. The LSb must be low for four consecutive samples then go high for four consecutive samples to initiate a trigger event. This trigger type can be used to align all DSPs across multiple parts, provided that all parts operate in subclass 1 mode.
4	Trigger Pin [3]	A rising edge on an external trigger pin (TRIG) that is bound [1] to DSP ***n*** triggers DSP ***n*** . *To trigger multiple DSP channels simultaneously, you must either meet setup/hold to the trigger clock or bind them to the same TRIG bit using TRIG_SEL.* See also Trigger Clock. This trigger type can be used to align all DSPs across multiple parts, provided that all parts have aligned trigger clock to a common SYSREF, and the TRIG signas meet setup/hold to the trigger clocks.

ADVANCE INFORMATION

Table 7-21. Trigger Sources / Modes (continued)

TRIG_TYPE[n] Value [2]	Trigger Source / Mode	Description
5	FRS Immediate	If FRS is set, then DSPn is triggered by the rising edge of $\overline{FRCS}$ (pin TRIG[4] when used as a FR interface) at the end of the FRI transaction. This trigger type is not designed for aligning multiple parts, since the FRI interface is asynchronous to the DSP clock. However, the trigger type can align multiple DSP channels in a single part.
6	FRS-TRIGCLK	If FRS is set, then DSPn is triggered by the rising edge of TRIGCLK that follows the rising edge of $\overline{FRCS}$ (pin TRIG[4] when used as a FR interface). If frcs_n meets setup/hold to trig_c, this method can deterministically align DSPs across multiple parts.

1. Use TRIG_SEL to choose which TRIG_SPI or TRIG bit is bound to each DSP.
2. See TRIG_TYPE for additional information.
3. When any TRIG_TYPE[n] is set to 4, the TRIG pins are used by default, but the user can substitute different pins in place of the TRIG[0], TRIG[1] or TRIG[2] pins. This is done using the TX_PIN_FUNC or SYNCB_PIN_FUNC registers. For example, if SYNCB_PIN_FUNC=10, then the SYNCB pin is used instead of the TRIG[0] pin. The user must also verify that TRIG_SELn=0 to bind DSPn to the SYNCB pin (which is standing in for TRIG[0]).

Table 7-22. DSP Trigger Actions vs. DSP Mode

DSP_MODE*n*	New FREQ[n] value applied to NCO	New PHASE[n] value applied to NCO	New AMP[n] value applied to Mixer	Phase Accumulator Reset	Advance to next DDS Vector
DUC Mode	Yes	Yes	n/a	If NCO_ARn[]=1	n/a
DDS SPI Mode	Yes	Yes	Yes	If NCO_AR[n]=1	n/a
DDS Vector Mode	n/a	n/a	n/a	Reset whenever a vector begins (auto or manually triggered) unless in Hold Mode	Yes, if the vector processor is waiting for a trigger (see VTRIG_MODE)
DDS Streaming Modes	Only if STREAM_MODE *n*=2	Only if STREAM_MODE *n*=1	Only if STREAM_MODE *n*=1	If NCO_AR[n]=1	n/a

Do not write the AMP, FREQ and PHASE registers around the same time that a trigger is occurring, otherwise the NCO can receive a corrupted AMP, FREQ or PHASE value.

7.3.6.6.1 Trigger Latency

There are several deterministic methods for triggering DSP blocks: through an LSB of the JESD204C interface, trigger pins or via SYSREF. The latency parameters for each triggering method are listed in Table 7-23. The values for T_{SYSREF_NCO}, T_{SYSREF_VEC},T_{TRIG_NCO} and T_{TRIG_VEC} depend on the device configuration and are provided in a latency calculator spreadsheet available from Texas Instruments. The value for T_{JSYNC_NCO} is provided in Table 7-24.

Table 7-23. NCO Synchronization Latency Parameters

Latency Parameter	Description
T_{SYSREF_NCO}	Latency from SYSREF sampled high (by DACCLK) to DAC output reacting to an NCO synchronization event (that was triggered by SYSREF).
T_{SYSREF_VEC}	Delay from SYSREF sampled high (to trigger NCO) to DAC output (vector mode) (DACCLK cycles)
T_{TRIG_NCO}	Delay from TRIGn sampled high to DAC output (DUC/Streaming/DDS-SPI) (DACCLK cycles)
T_{TRIG_VEC}	Delay from TRIGn sampled high to DAC output (vector mode) (DACCLK cycles)
T_{JSYNC_NCO}	The latency through the interpolation filter to the NCO minus the latency of the LSB that synchronizes the NCO. Applies only when using the LSB of the input data to synchronize the NCO. To make input sample **n** be the first sample to be mixed with a new NCO frequency or phase, the LSB can be brought high on sample **n'** = **n**+T_{JSYNC_NCO}/LT. Note that **n'** can be a non-integer value as the synchronization path is not always a whole number of input sample periods. See Table 7-24

ADVANCE INFORMATION

Table 7-24. T_{JSYNC_NCO} vs. LT

Interpolation Factor (LT)	T_{JSYNC_NCO} [DACCLK cycles](1)
4	-148, -152, -156, -160, -164, -168, -172, -176
6	-70, -76, -82, -86, -88, -92, -94, -98, -100, -104, -106, -110, -112, -116, -122, -128
8	10, 18, 26, 34
12	90, 102, 106, 114, 118, 126, 130, 142
16	262, 278
24	406, 422, 430, 446
32	624
48	896, 912
64	1404
96	2036
128	2932
192	4212
256	6004

(1) Multiple values listed indicates that T_{JSYNC_NCO} depends on when the LSB rises with respect to the multiframe boundary.

7.3.6.7 NCO Square Wave Mode

The NCO inside each DSP channel can be configured to produce a square waveform instead of sine/cosine waveforms. This feature is designed for systems that want to synthesize a clock signal using the DAC with programmable frequency, phase, amplitude, slew time and duty cycle. Enable this feature on DSP*n* by setting NCO_SQ_MODE[*n*]. This mode is compatible with all the DDS modes, but is not supported for DUC mode (see the DSP_MODE*n*). The DDS-SPI mode is the primary use case for this feature. But if frequency ramping is necessary, DDS-Vector mode or DDS-Streaming mode can be useful.

The slew time and duty cycle are adjustable using the SLEW and DUTY_CYCLE registers. The slew time is programmed as a proportion of the period, so when the NCO frequency is changed, the period; therefore, the slew time also changes.

The frequency, phase, and amplitude are controlled in the same fashion as if the NCO was producing sine/cosine waveforms. This is summarized in Table 7-25.

Table 7-25. NCO Parameter Control Method vs DSP Mode

NCO Parameter	Control Method for the NCO Parameter depends on DSP mode		
	DDS SPI Mode	DDS Streaming Mode	DDS Vector Mode
Frequency	FREQ register	Depends on STREAM_MODE	Vector Engine
Phase	PHASE register	Depends on STREAM_MODE	Vector Engine
Amplitude	AMP register	Depends on STREAM_MODE	Vector Engine
Slew	SLEW register	SLEW register	SLEW register
Duty Cycle	DUTY_CYCLE register	DUTY_CYCLE register	DUTY_CYCLE register

The square waveform produced by the NCO is depicted in Figure 7-43.

ADVANCE INFORMATION

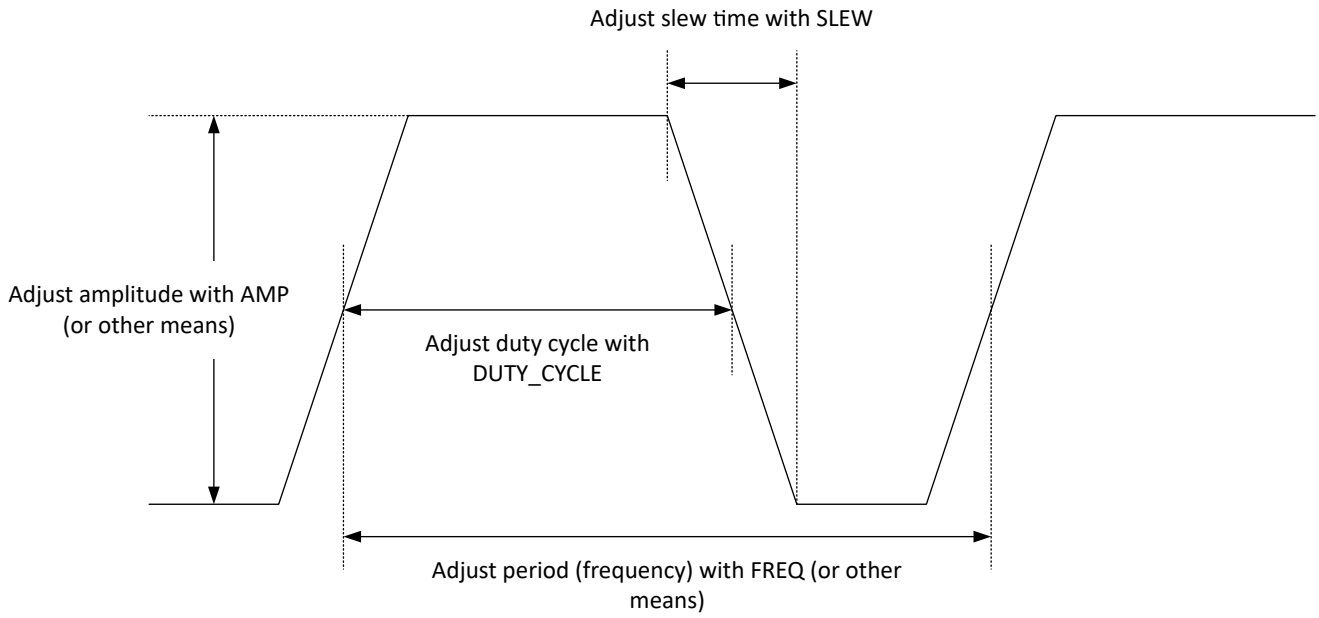


Figure 7-43. NCO Square Waveform Properties

The duty cycle is adjustable over a wide range, but the user must never adjust the duty cycle to extreme values that cause the falling edge of the signal to “collide” with the rising edge. The supported duty cycle range depends on the SLEW setting and is listed in Table 7-26.

Table 7-26. Supported Duty Cycle Range vs Slew Time

SLEW Setting	Slew time as a percentage of the period (25% * 2^{-SLEW})	Acceptable duty cycle range [percent]	Supported range of DUTY_CYCLE register (decimal)
0	25%	25% - 75%	1024 to 3072
1	12.5%	12.5% - 87.5%	512 to 3584
2	6.25%	6.25% - 93.75%	256 to 3840
3	3.125%	3.125% - 96.875%	128 to 3968
4	1.5625%	1.5625% - 98.4375%	64 to 4032
5	0.78125%	0.78125% - 99.21875%	32 to 4064
6	0.390625%	0.390625% - 99.60938%	16 to 4080
7	0.195313%	0.195313% - 99.80469%	8 to 4088
8	0.097656%	0.097656% - 99.90234%	4 to 4092
9	0.048828%	0.048828% - 99.95117%	2 to 4094

Notes about the square wave generator:

1. Square wave mode only makes sense to use in NRZ or DES2XL DAC output modes (1st Nyquist modes) and with a frequency < 1/10th the DAC clock rate, otherwise there are not enough data points during the cycle to define the transition periods.
2. The SLEW and DUTY_CYCLE parameters can be changed while the NCO is producing an output, but the parameters do not go into effect until the DSP receives a trigger event. Updating these parameters in this way is not clean as the waveform can glitch to the new waveform. To prevent glitches, the waveform can be gated low to update the SLEW and DUTY_CYCLE parameters using NCO_SQ_EN.
3. When using the square waveform with DDS Vector mode, use the DDS_HOLD feature so that the vector engine holds on a vector and keeps producing a waveform when waiting for a trigger. If you do not use this mode, the output mutes by going to mid-code and does not gate the square wave into the low state.

ADVANCE INFORMATION

4. Internally, the square wave swings from -32768 to +32767 and then is scaled by the mixer. When the DDS amplitude (AMP) is full scale (32767), this scales the waveform down slightly, so the output swings from 32767 to +32766.
5. Setting the DDS amplituide to 0 is not the same as gating the waveform. Setting the amplitude to 0 causes the swing to be 0 at mid-code. Gating the waveform low keeps the waveform at the “logic low” or “minimum level” (for example -32767 if the DDS amplitude is set to 32767).
6. The square wave mode is not compatible with DSP_FORMAT=1.
7. In square wave mode, do not set the NCO frequency higher than $F_{DAC}/4$.
8. The user must take care that the SLEW setting is not too high. If the setting is too high, the NCO can fail to produce output samples during the transition period. As a result, the jitter of the resulting signal can be poor as every edge is rounded off to the nearest sampling period. Better jitter performance occurs when the the slew time consists of multiple sample periods. The number of sample periods in the slew time is equal to $0.25 * 2^{-SLEW[n]} * 2^{64} / FREQ[n]$ (assuming DDS SPI mode). A low-pass anti-imaging filter on the DAC output can help smooth out the transitions to produce a smoother clock signal.
9. DES2XL mode is advantageous to use as DES2XL increases the number of points in the transition period. However, as the DES2x digital filter limits the digital bandwidth, the filter produces ripple near the transition period that is larger than the square wave amplitude. Therefore, the square wave amplitude must be backed off by 2-3% to prevent saturating the digital signal.
10. See Bandwidth Optimization for Square Wave Mode on optimization of the DAC output bandwidth for square wave mode.

7.3.6.7.1 Square Wave Enable

In square wave mode, the NCO has the ability to synchronously disable the waveform output by gating the waveform low. This is similar to how a digital clock signal is typically gated. The user can decide how to provide the waveform-enable signal (see NCO_SQ_SEL). When the provided enable signal changes state, the NCO does not immediately respond, but waits for the waveform to be in a low state so that no truncated pulses occur on the output. This is depicted in Figure 7-44. The phase of the waveform is not altered when the waveform is disabled and re-enabled. The waveform returns to the same phase the waveform as if the waveform had never been disabled.

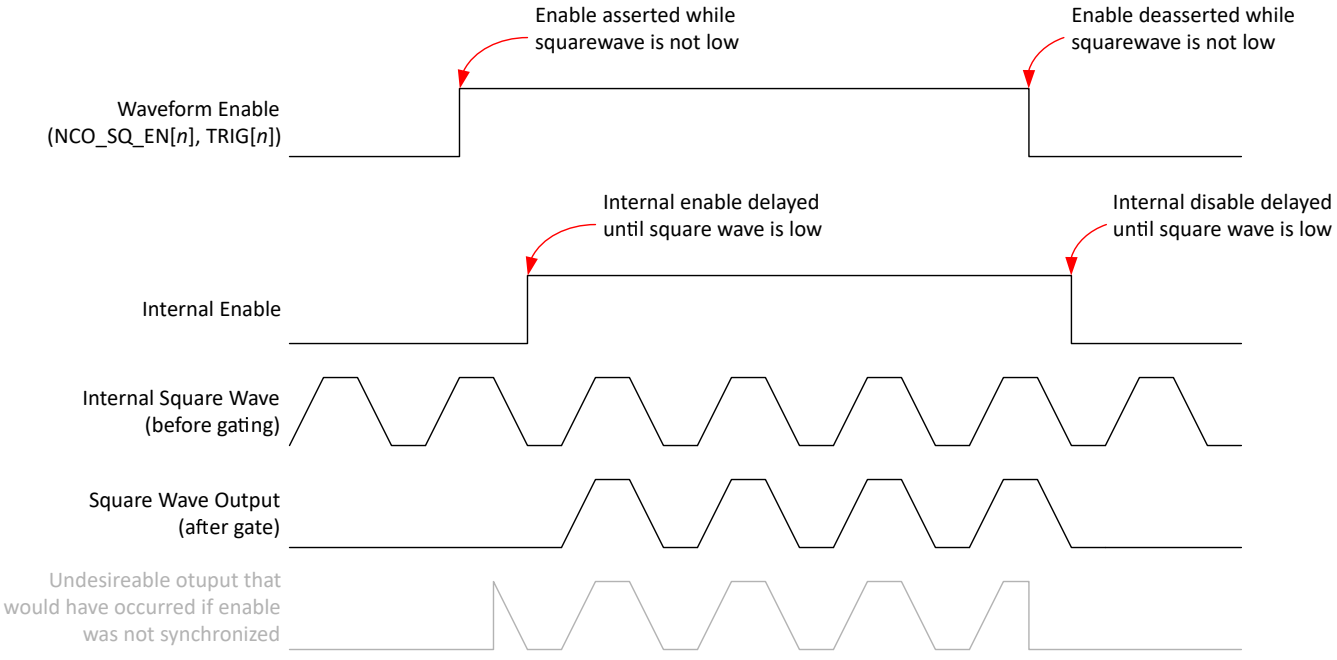


Figure 7-44. Waveform Enable/Disable Example

While the waveform is disabled, the NCO applies any new values programmed into the SLEW or DUTY_CYCLE registers. The new settings are observable once the waveform is re-enabled. New values for FREQ, PHASE,

ADVANCE INFORMATION

AMP are not applied while the waveform is disabled. The user must provide a trigger to the DSP to update those parameters.

Some latency occurs when the enable signal changes state. The NCO must first wait for the waveform to be low. In addition to that delay, there is an additional delay of 448 DAC clock cycles for the NCO to process the event. If the user changes the enable signal again while the NCO is still processing the previous change, then additional delay can occur as the NCO must fully process the previous change before the NCO inspects the current state of the enable signal and process another change (if necessary).

7.3.6.8 DSP Mute Function

Each DSP channel contains a mute function that makes sure the DSP output is zero during startup or when waking from a sleep condition. The output transitions directly from a valid sample to zero when muting or directly from zero to a valid sample when unmuting. The mute is applied at the DSP output (just before the channel bonder input).

The DSP output is muted in the following conditions:

- SY_EN transitions from 0 to 1
- The device is in APP Sleep
- The DSP channel is asleep based on APP_SLEEP0/1

Once the DSP channel is awake, the mute is extended by a counter. The duration of the counter is a function of DSP_MODE*n*, DSP_L, and PFIR_MODE. The mute extension makes sure that unknown or old samples stored in the DUC, DDS, or PFIR signal paths are flushed out (and these samples never reach the channel bonder). The extension roughly scales based on the memory depth of the DSP signal path.

The mute extension (in DAC cycles) is given by

$$\text{Total Mute Extension (in DAC cycles)} = 512 \times (D_{DSP} + D_{PFIR}) \quad (3)$$

where Table 7-27 and Table 7-28 and define the values of D_{DSP} and D_{PFIR}. Note that D_{DSP} and D_{PFIR} are channel-specific (each DSP channel can have a unique value based on DSP_MODE*n* and PFIR_EN).

Table 7-27. Mute Extension for DSP*n* associated with DSP latency (D_{DSP})

DSP_MODE*n*	DSP_L	LT (shown for reference)	D_{DSP}
DSP is NOT in DUC mode	any	any	2
DSP is in DUC mode	0 to 2	RESERVED	2
	3	4x	2
	4	6x	3
	5	8x	3
	6	12x	4
	7	16x	4
	8	24x	6
	9	32x	8
	10	48x	10
	11	64x	13
	12	96x	20
	13	128x	26
	14	192x	38
	15	256x	50

ADVANCE INFORMATION

Table 7-28. Mute Extension for DSP*n* when PFIR is enabled (D_{PFIR})

DSP_MODE*n*	PFIR_EN[*n*]	PFIR_MODE	Mute Extension (D_{PFIR})							
			Interpolation Factor (LT)							
			4	6	8	12	16	24	32	All others
non-DUC mode	any value	any value	0	0	0	0	0	0	0	0
DUC Mode	0	any value	0	0	0	0	0	0	0	0
DUC Mode	1	0	0	0	0	0	0	0	0	0
DUC Mode	1	1	2	2	3	4	8	11	26	undefined
DUC Mode	1	2	1	2	2	3	4	6	14	undefined
DUC Mode	1	3	0	0	2	2	3	4	7	undefined

If DSP_FORMAT=1, then DSP2/3 uses the mute extension from DSP0/1 respectively. This makes sure DSP2/3 use the same duration as the partner channel.

7.3.6.9 DSP Output Gain

At the DSP output, there is a 'Gain / Round / Saturate' function. This function performs these steps (in order):

1. Receives the output of the mixer (32-bits)
2. Rounds the mixer output (19-bits)
3. Implement a mux that can bypass the mixer (applies to DUC mode when NCO_EN=0).
4. Perform the gain function from DSP_GAINn (output is 24-bits).Note that gain is still applied when the mixer is bypassed.
5. Round and saturate the result to 20-bits and send the result to the channel bonder.

Note that the mixer output has enough range to support samples up to about 2.0. This extra range is maintained through the gain block and then removed after the gain block. This extra range allows the datapath to mix I/Q values with a magnitude greater than 1.0 and never saturate if the gain setting provides adequate attenuation. For example, if the I and Q samples are both full scale (1.0), the complex magnitude is about 1.414. If the gain (DSP_GAINn) is -3dB or less, the signal can not saturate. This can be useful if the DUC input is a baseband QAM signal with zero frequency offset and nearly at full scale (the corners of the QAM constellation have a magnitude greater than 1.0). For other signals, the distribution of the baseband I/Q samples is not very rectangular, so this extra range provides only a little benefit (fewer peak samples saturate depending on where the peaks fall in the I/Q plane).

7.3.6.10 Complex Output Support

Each DSP channel can only produce one real output signal. If the user prefers a complex signal, the DSP_FORMAT register can be used to enable the mixers in DSP2 and DSP3 to generate imaginary (Q) samples for DSP0 and DSP1 respectively (reducing the number of available DSP channels from 4 to 2). To accomplish this, signals are routed from DSP0 and DSP1 to DSP2 and DSP3 respectively. The routed NCO outputs are multiplied by -j so that DSP2/DSP3 produce the imaginary output (instead of a real output).

7.3.6.11 Channel Bonder

When the DSPs are used, the Channel Bonder allows each DAC channel to receive a summation of any combination of DSP channel outputs (see Figure 7-45). To avoid saturation when summing DSP signals, the DSP gain should be adjusted (see DSP_GAINn). The gain is applied within each DSP before the signals reach the channel bonder (see DSP Output Gain).

DSP outputs are bound to DAC channels using the DAC_SRC register, then all bound DSP signals are summed together to produce a signal for the DAC channel (which is sent to the PFIR, DES2X interpolator or Encoder).

When the DSPs are bypassed (see Bypass Mode), the channel bonder simply allows the user to route either of the bypass sample streams to either DAC channel using DAC_SRC. No scaling or summing is supported in bypass mode.

Finally, the channel bonder can optionally invert the output based on DAC_INVn.

ADVANCE INFORMATION

The input resolution of the channel bonder is 20-bits and the output resolution is 16-bits.

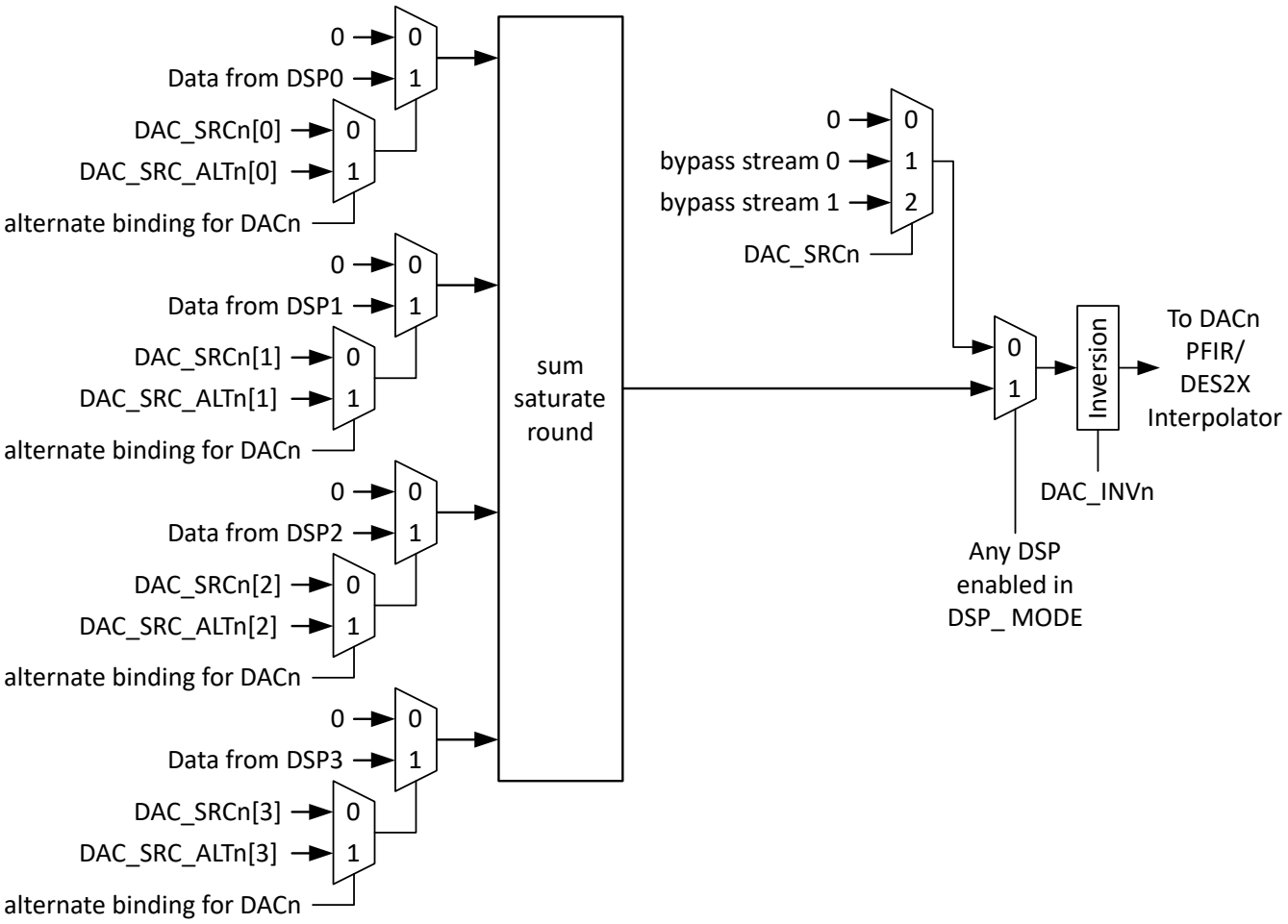


Figure 7-45. Channel Bonder Block Diagram for DAC Channel n

ADVANCE INFORMATION

7.3.6.12 Programmable FIR Filter

The device contains a programmable FIR filter (PFIR), placed either after the channel bonder and before the DES interpolator (when used, alternatively the DAC encoder), or at the input to the DUC. When place at the output of the channel bonder, the PFIR can equalize the full DAC Nyquist zone (single edge clock). When placed at the input to the DUC, the PFIR can be split to provide separate filters for each DUC input, and can equalize within the signal bandwidth. Since the sample rate is lower at the input to the DUC, the PFIR has more filter taps available. Also, the filter covers a longer time span (more taps at a lower sample rate), improving the frequency resolution of the filter.

Table 7-29. PFIR Features

PFIR Behavior / Feature	Placement of PFIR	
	PFIR Placed after Channel bonder (Real Mode) (PFIR_MODE=0)	PFIR Placed before DUC Channels (Complex Mode) (PFIR_MODE>0)
Number of Supported Channels	Up to 2 real channels	1, 2, or 4 complex channels, depending on PFIR_MODE
Complex Support	PFIR inputs, outputs and coefficients are all real (not complex)	PFIR inputs, outputs, and coefficients are all complex
Sample Rate	F_{DACCLK}	F_{DACCLK}/LT
Number of Coefficients (taps)	24 real coefficients	Depends on LT and PFIR_MODE
Reflection Mode Support	Yes, see PFIR Reflection Cancellation Section	No
DSP_MODE*n* settings supported	Any DSP_MODE*n* supported	Only DUC mode supported
Interpolation values supported (LT)	All interpolation factors supported	Only 4x – 32x supported
Broadcast support	Yes, channel 0 can be broadcast to DAC1 (see PFIR_BC)	No
Reduced taps count	No, always uses 24 taps	Yes, see PFIR_LEN

ADVANCE INFORMATION

The PFIR coefficient resolution is 16 bits. Table 7-30 provides the maximum # of filter taps depending on PFIR location and modes.

Table 7-30. PFIR Modes

PFIR_MODE Setting	PFIR Position	Max # of Channels	Interpolation	Max # of Taps/Channel
0	Channel bonder output	2 Real DAC Channels	(1x - 256x)	24
1	Before DUC0	1 complex DUC channel	4x	48
			6x	48
			8x	96
			12x	96
			16x	192
			24x	192
			32x	384
2	Before DUC0 and DUC1	2 complex DUC channels	4x	24
			6x	24
			8x	48
			12x	48
			16x	96
			24x	96
			32x	192
3	Before DUC0, DUC1, DUC2 and DUC3	4 complex DUC channels	8x	24
			12x	24
			16x	48
			24x	48
			32x	96

7.3.6.12.1 PFIR Coefficients

The coefficients for the PFIR taps are defined by the PFIR_H or FR_PFIR_H register arrays. The arrays supports a total of 768 coefficients. Each coefficient is a signed 16-bit value with an LSB weight of 2^{-15}. Real and imaginary coefficients are allocated to separate locations in the array. The locations are assigned to PFIR channels differently depending on PFIR_MODE (see Table 7-31). In complex mode (PFIR_MODE>0), the number of coefficients increases as the interpolation factor increases. Also note, the DUC channels are out of order (0,2,1,3) when PFIR_MODE=3.

Table 7-31. PFIR Coefficient Allocation vs. PFIR_MODE and LT

	PFIR_MODE											
	0	1				2				3		
	LT	Interpolation Factor (LT)				Interpolation Factor (LT)				Interpolation Factor (LT)		
Offset[1] into PFIR_H[n]	*Any*	4x, 6x	8x,12x	16x,24x	32x	4x, 6x	8x, 12x	16x,24x	32x	8x, 12x	16x,24x	32x
0	DAC0	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real	DUC0, Real
24												
48												
72												
96										DUC0, Imag	DUC0, Imag	DUC0, Imag
120												
144												
168												
192						DUC0, Imag	DUC0, Imag	DUC0, Imag	DUC0, Imag	DUC2, Real	DUC2, Real	DUC2, Real
216												
240												
264												
288										DUC2, Imag	DUC2, Imag	DUC2, Imag
312												
336												
360												
384	DAC1	DUC0, Imag	DUC0, Imag	DUC0, Imag	DUC0, Imag	DUC1, Real	DUC1, Real	DUC1, Real	DUC1, Real	DUC1, Real	DUC1, Real	DUC1, Real
408												
432												
456												
480										DUC1, Imag	DUC1, Imag	DUC1, Imag
504												
528												
552												
576						DUC1, Imag	DUC1, Imag	DUC1, Imag	DUC1, Imag	DUC3, Real	DUC3, Real	DUC3, Real
600												
624												
648												
672										DUC3, Imag	DUC3, Imag	DUC3, Imag
696												
720												
744												

(1) Each row represents a group of 24 coefficients. Only the index of the first coefficient within the group is listed.

ADVANCE INFORMATION

7.3.6.12.2 PFIR Reflection Cancellation Mode

The PFIR filter in real mode can be split into two PFIR filters with a delay in between to cancel reflections that occur on the DAC output network, cables, etc. The PFIR_DLY register is provided to facilitate this. PFIR_DLY adjusts the delay of taps 12 thru 23 of the PFIR by inserting zero-valued coefficients between coefficient 11 and 12. Up to 255 zero-valued coefficients can be added.

For example, if PFIR_DLY[0] = 103, then PFIR0 inserts 103 zeros in the impulse response. The impulse response for PFIR0 is therefore:

- h[n] = PFIR_H[n] for n =0..11
- h[n] = 0 for n =12..114
- h[n] = PFIR_H[n -103] for n =115..126

7.3.6.12.3 PFIR Power Savings

The PFIR filter is a large digital block that can dissipate as much power as the rest of the digital logic circuits. There are three main ways the user can reduce the power consumption of the PFIR:

1. Program unneeded coefficients to zero. This provides a modest power savings (as compared to using all non-zero coefficients)
2. Set PFIR_EN to enable fewer than the maximum number of supported channels afforded by the PFIR_MODE setting. Example: Set PFIR_MODE=3 (up to 4 DUCs can be filtered), but set PFIR_EN[3:0]=0b0001 (only DUC0 is filtered)
3. Set PFIR_LEN=0 to halve the number of active coefficients. Example: With PFIR_MODE=3 and LT=32x, 96 taps are supported, but if PFIR_LEN=0, the tap count is reduced by half (to 48). Note that this feature is not available for any modes that use 24 coefficients.

7.3.6.12.4 PFIR Usage

1. Configure the JESD204C subsystem, DSP and other components for your desired mode of operation. Do not set SYS_EN.
2. Program PFIR_MODE (consult PFIR Modes):
   a. If using DUC mode (see DSP_MODE*n*), then the user has the option to place the PFIR after the DUCs (PFIR_MODE=0) or before the DUCs (PFIR_MODE>0). If using any other mode (DDS, Bypass, etc.), the user must use PFIR_MODE=0 to run the PFIR at full sample rate.
   b. If using PFIR_MODE>0, select a mode that supports the number of channels the user wishes to filter. Selecting a mode that supports more channels than needed reduces tap count and power consumption.
3. Program PFIR_EN to specify which channels are be filtered.
4. Program FR_EN based on which interface is used for updating PFIR coefficients. If FR_EN=1, use FR_PFIR_H and FR_PFIR_PROG instead of PFIR_H and PFIR_PROG below.
5. Consult Table 7-31 and program the proper elements of PFIR_H (based on PFIR_MODE and LT).
6. Set other possible options like PFIR_LEN or PFIR_DLY.
7. Set SYS_EN to start up the system. The PFIR now runs with the specified configuration.
8. To change the coefficients on the fly (while SYS_EN=1), first set PFIR_PROG=1, then wait 1024 DACCLK cycles before modifying PFIR_H. Once the user has completed the changes, set PFIR_PROG=0 to put the changes into effect.

7.3.6.13 DES Interpolator

The output of the summation block can optionally be interpolated by 2x by the DES interpolator to double the sample rate for DES2XL and DES2XH output modes. The DES interpolator has a passband bandwidth of 80%, stopband attenuation of 54dB and ripple less than ±0.02dB. The DES interpolator can operate as high pass (DES2XH) or low pass (DES2XL) with an inverted spectrum. The filter taps for the DES interpolator are

[-9 0 19 0 -39 0 70 0 -122 0 211 0 -403 0 1293 2048 1293 0 -403 0 211 0 -122 0 70 0 -39 0 19 0 -9]*2^{-11}

The responses are shown in Figure 7-46, with the passband ripple for DES2XL shown in Figure 7-47.

The sample rate after interpolation is 2*f_{DACCLK} due to having samples on both the rising and falling edges, so the x-axis in Figure 7-46 covers the Nyquist zone.

Due to the filter gain of 0.1dB in passband at some frequencies, the user may need to backoff the input to avoid clipping.

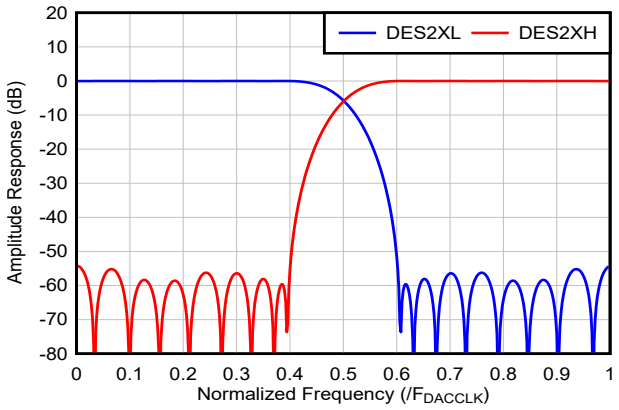


Figure 7-46. DES Interpolator Frequency Response

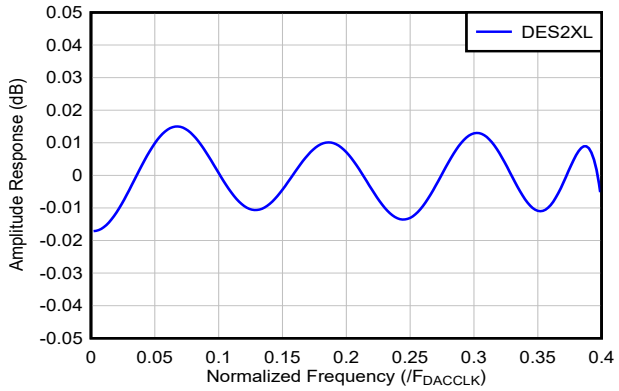


Figure 7-47. DES Interpolator Frequency Response (Passband)

7.3.6.13.1 DAC Mute Function

The DAC mute function is used to quiet the output data in various conditions described below. The output transitions directly from valid sample to mid-scale (0) when muting or directly from mid-scale (0) to a valid sample when unmuting.

The DAC output is muted in the following conditions:

- SYS_EN=0
- MODE>0
- the device is in APP Sleep

Once the mute condition ceases, the mute is extended by a counter. The duration of the counter is a function of MXMODE, PFIR_EN, and PFIR_MODE. The mute extension makes sure that unknown or old samples stored in the PFIR, DES2X filter, or encoder signal paths are flushed out whenever the encoder is started up or resumed (and these samples never reach the DACs). The extension roughly scales based on the memory depth of the signal path.

The extension (in DAC cycles) is defined by this equation with three terms:

$$\text{Total Mute Extension}\left(\text{in DAC cycles}\right) = 512 \times \left(2 + D_{PFIR\_ENC} + D_{DES2X}\right) \quad (4)$$

The value of the terms are given in Table 7-32 and Table 7-33, and can be unique for each encoder channel *n*:

Table 7-32. Mute Extension for PFIR Operation in full rate mode (D_{PFIR_ENC})

Condition	Value of D_{PFIR_ENC}
PFIR_EN[*n*] && PFIR_MODE==0	2
All other conditions	0

Table 7-33. Mute Extension for DES2X operation (D_{DES2X})

MXMODE*n*	D_{DES2X}
DES2X or DES2XH	1
All others	0

ADVANCE INFORMATION

This mute function is also triggered when the transmit enable signal for the DAC is low and IDLE_STATIC=0. This provides a mute with dynamic switching that provides more balanced aging. No mute extension occurs due to exiting this condition.

7.3.7 Serdes Physical Layer

The device contains 16 SerDes lanes. Each SerDes lane has a CTLE for channel loss equalization.

7.3.7.1 Serdes PLL

The Serdes PHY includes a PLL and power supply regulator to provide the required high quality, high speed internal clocks. The PLL uses a reference clock which derived from the DACCLK. PLL lock status is provided via the PLL_LOCK bit.

7.3.7.1.1 Enabling the Serdes PLL

To enable the internal Serdes PLL, PLL_EN must be set high. The VCO calibration will then run if VCAL_EN=1. At the end of a successful calibration, the VCAL_DONE field goes high. Shortly after calibration, the PLL should achieve lock. Lock is indicated by the LOCK field.

When PLL_EN is low, the PLL and regulator are fully powered down.

7.3.7.1.2 Reference Clock

During normal operation, the integrated PLL uses a reference clock from the device clock tree to generate a higher frequency clock from which the bit rate can be derived. The reference clock frequency (F_{REF}) can be in the range specified in Switching Characteristics. The clock frequency generated by the PLL VCO (F_{VCO}) is determined by the multiplication factor MPY setting according to:

$$F_{VCO} = MPY \times F_{REF} \quad (5)$$

The VCO output frequency (F_{VCO}) must be within the range specified in Switching Characteristics.

The relationship between line rate (F_{BIT}) and PLL output clock frequency (F_{VCO}) depends on the user-defined RATE setting:

$$F_{BIT} = \frac{2 \times F_{VCO}}{2^{RATE}} \quad (6)$$

Separate from the PLL, the JESD PHY includes additional frequency translation to support a variety of line rates. See Table 7-34.

7.3.7.1.3 PLL VCO Calibration

The Serdes PLL output frequency is realized using multiple VCO cores. The LC tanks provide good phase noise performance. The entire range of 8.125GHz to 16.25GHz, an octave, is covered with 4 different VCO cores. VCO calibration is required to obtain the correct frequency of interest.

A stable reference clock is required for calibration. Calibration begins after the PLL is enabled. During calibration, the PLL loop is disabled, and the VCO control voltage is driven to mid-scale. The calibration algorithm uses the frequency detector to determine if the VCO frequency is too high or too low.

When VCO calibration is completed (or skipped), and lock is detected, the PLL_LOCKED field is asserted.

7.3.7.1.4 Serdes PLL Loop Bandwidth

The SPLL loop bandwidth is a function of the VCO gain, phase detector gain and the loop filter passives (resistor and capacitor). The loop filter bandwidth can be adjusted depending on the PLL multiplication factor for better noise. The device has a lookup table for loop filter settings according to the VCO calibration settings and MPY. For lower values of MPY (<33) where the refclk is relatively high (≥400MHz) a fixed loop filter setting can be used.

The loop bandwidth varies between 1MHz and 12MHz.

7.3.7.2 Serdes Receiver

7.3.7.2.1 Serdes Data Rate Selection

The PLL output frequency is determined by the reference clock frequency ($F_{RX} = F_{VCO}/2$) and PLL multiplication factor, as detailed in Reference Clock. However, the PLL output frequency operates only over a limited range, so the RATE setting is provided to support a wide range of line rates.

The relationship between line rate (F_{BIT}) and VCO frequency (F_{VCO}) depends on the user-defined RATE setting, as listed in Table 7-34.

Table 7-34. Line Rate vs. RATE setting

RATE Field	Description	Line Rate	Supported Line Rate
0	Full Rate	2 * F_{VCO}	16.25Gbps – 32.5Gbps
1	Half Rate	1 * F_{VCO}	8.125Gbps – 16.25Gbps
2	Quarter Rate	0.5 * F_{VCO}	4.0625Gbps – 8.125Gbps
3	Eight Rate	0.25 * F_{VCO}	2.03125Gbps – 4.0625Gbps
4	Sixteenth Rate	0.125 * F_{VCO}	1.015625Gbps – 2.03125Gbps

7.3.7.2.2 Serdes Receiver Termination

The nSRX+ and nSRX- (n = 0:15) differential inputs are each internally terminated to a common point via 50Ω, as shown Figure 7-48. The Serdes inputs are only intended for AC coupled operation.

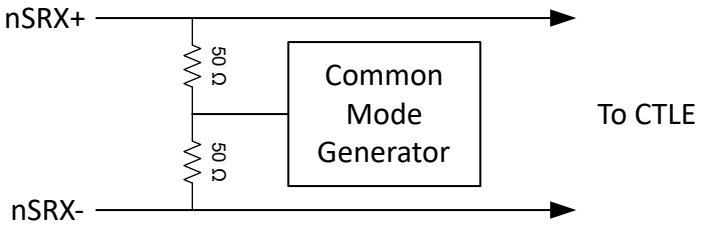


Figure 7-48. Serdes Receiver Input Termination

7.3.7.2.3 Serdes Receiver Polarity

The polarity of nSRX+ and nSRX- can be inverted by setting the LANE_INV register. This can potentially simplify PCB layout and improve signal integrity by avoiding the need to swap differential signal traces.

7.3.7.2.4 Serdes Clock Data Recovery

The clock recovery algorithms operate to adjust the clocks used to sample nSRX+ and nSRX- so that the data samples are taken midway between data transitions.

The algorithm uses a basic technique to determine whether the sampling clock is correctly placed, and if not whether the sampling clock needs to be moved earlier or later. When two contiguous data samples are different, the edge sample between the two is examined. The sampling clock can be considered early or late depending on whether the edge sample matches the first or second data sample respectively.

Every 32 UI, 32 such comparisons are made, with each result counted as a vote to move the sample point either earlier or later (positions where no transition occurred produce no vote). If the majority are early or late votes, an internal counter is incremented or decremented respectively. When the internal counter overflows or underflows, the sampling instant of the clock is adjusted later or earlier respectively (by 1/64 UI).

Each time the sampling instant of the clock is adjusted, the internal counter returns to mid-code, and a blanking interval occurs (also called “settling time”). During the blanking interval, no votes are counted. This is necessary to make sure that the incoming data and edge samples have reflected the new sampling instant. This can prevent the algorithm from overshooting. The blanking interval (settling time) is defined by the CDRSTL register field. The largest setting can provide power savings.

The size of the internal counter (and therefore the number of increments or decrements required to adjust the sampling instant) is programmable (see CRDVOTE register field).

Note that the clock recovery algorithm continues to operate even if the SIG_DET[n] status bit is low (loss of signal).

7.3.7.2.5 Serdes Equalizer

The equalizer operates in several different modes by setting the EQMODE field. The available settings are depicted in Table 7-35.

Table 7-35. Equalizer Modes

EQMODE	Description	Details
0	No Equalization	The equalizer provides a flat response at the maximum gain. This setting is appropriate if jitter at the receiver occurs predominantly as a result of crosstalk rather than frequency dependent loss.
1	Adaptive or Fixed Equalization	The zero position is determined by the selected operating rate, and the low frequency gain of the equalizer is determined algorithmically by analyzing the data patterns and transition positions in the received data. (See Adaptive Equalization). This setting is also used for fixed equalization by setting EQ_OVR=1 and a fixed equalization level using EQLEVEL. (See Fixed Equalization)
2	Pre-cursor Equalization Analysis	The data patterns and transition positions in the received data are analyzed to determine whether the transmit link partner is applying more or less precursor equalization than necessary. See Pre and Post Cursor Analysis for further details.
3	Post-cursor Equalization Analysis	The data patterns and transition positions in the received data are analyzed to determine whether the transmit link partner is applying more or less post-cursor equalization than necessary. See Pre and Post Cursor Analysis for further details.

7.3.7.2.5.1 Adaptive Equalization

The serdes receivers incorporate an adaptive equalizer, which compensates for channel insertion loss by attenuating the low frequency components with respect to the high frequency components of the signal, thereby reducing inter-symbol interference.

When enabled, the receiver equalization logic analyzes data patterns and transition times to determine whether the low frequency gain of the equalizer is increased or decreased.

The decision logic is implemented as a voting algorithm with a relatively long analysis interval. The slow time constant that results reduces the probability of incorrect decisions, but allows the equalizer to compensate for the relatively stable response of the channel.

The lock time for the adaptive equalizer is data dependent and therefore not possible to specify a generally applicable absolute limit. However, assuming random data, the maximum lock time is approximately 6×10^6 UI divided by the CDR activity level.

To enable adaptive equalization:

1. Set EQMODE = 1prior to setting SYS_EN=1.
2. Once the equalizer is enabled, read EQLEVEL_S to get the current state of the adaptive equalizer. Before reading EQLEVEL_S, set EQHOLD=1 to freeze the EQ loop to make sure a coherent value is returned by EQLEVEL_S. Multiple reads are recommended to verify the adaptation loop has settled (set EQHOLD low and then high again between each read to let the loop operate).

7.3.7.2.5.2 Fixed Equalization

For fixed (non-adaptive equalization), program EQMODE=1, EQ_OVR=1, EQZ_OVR=0 prior to setting SYS_EN=1. Program EQLEVEL to the desired equalization level.

7.3.7.2.5.3 Pre and Post Cursor Analysis

Pre and Post Cursor Analysis can be used to determine an optimized setting for pre-emphasis in the transmitter. The usage model is as follows:

1. Program SYS_EN=0 if necessary. Program a mode that uses the JESD interface (JESD_M>0).
2. Program EQMODE=1. Program SYS_EN=1 and allow sufficient time for the equalizer to adapt and settle. You can read EQLEVEL_S multiple times to verify the value is stable or toggling between adjacent values (set EQHOLD=1 before reading EQLEVEL_S, then return EQHOLD back to 0. Then repeat as necessary).
3. Set EQHOLD=1 to lock the equalizer (disable adaptation). This also causes EQOVER and EQUNDER fields to become low.
4. Wait at least 48UI, and proportionally longer if the CDR activity is less than 100% to make sure the 1 on EQHOLD is sampled and acted upon. The SPI is slow enough that no explicit delay is be necessary.
5. Set EQMODE to 2 or 3 to select pre or post cursor analysis respectively. With a separate SPI transaction, set EQHOLD=0. The equalization characteristics of the received signal are analyzed (the equalizer response continues to be locked).
6. Wait at least 150,000UI to allow time for the analysis to occur, proportionately longer if the CDR activity is less than 100%.
7. Examine EQOVER and EQUNDER for results of analysis.
   a. If EQOVER is high the signal is over equalized
   b. If EQUNDER is high the signal is under equalized
8. Set EQHOLD = 1
9. Adjust the transmitter. Repeat items 3 to 7 if required.
10. Set EQMODE=1, and with a separate SPI transaction, set EQHOLD=0 to exit analysis mode and return to normal adaptive equalization.

7.3.7.2.6 Serdes Receiver Eyescan

All receive channels provide features which facilitate mapping the received data eye. A variety of different modes are supported (see ES register for list of modes). The following sections describe how to get eye-scan data from the part and some approaches for building an eye-diagram. The process of transforming this data into a map of the eye must then be performed externally, typically in software.

The basic principle used is as follows:

- Enable dedicated eye scan input sampler, and generate an error when the value sampled differs from the normal data sample.
- Apply a voltage offset to the dedicated eye scan sampler.
- Apply a phase offset to adjust the sampling instant of the eye scan sampler.
- Reset the error counter
- Specify a scan duration and initiate the scan process. When the scan completes, check how many errors have occurred.
- Change voltage and/or phase offset, and repeat.

Alternatively, the algorithm can be configured to optimize the voltage offset at a specified phase offset, over a specified time interval.

Eye scan can be used while receiving normal data traffic.

The register fields used to directly control eye-scan and symbol response extraction are ES, ESBSEL, ESPO, ESVO, ESVO_OVR, ESLEN, ESRUN and ESDONE. Eye-scan errors are accumulated in the ECOUNT field of the PHY_STATUS register (see Serdes PHY Status). The required eye-scan mode is selected via the ES field, as shown below. All ES settings use the ESLEN field to determine the duration of the scan process.

Table 7-36. Eye-scan Modes

ES Field	Effect
0000	*Disabled:* Eye scan is disabled (eye-scan sampler powered down)
0X01	*Compare:* Counts mismatches between the normal sample and the eye-scan sample if ES[2] = 0, and matches otherwise.
0X10	*Compare zeros:* As ES = 0X01, but only analyses zeros, and ignores ones.
0X11	*Compare ones:* As ES = 0X01, but only analyses ones, and ignores zeroes.
0100	*Count ones:* Increments ECOUNT when the eye-scan sample is a 1.

ADVANCE INFORMATION

Table 7-36. Eye-scan Modes (continued)

ES Field	Effect
1X00	*Average:* Adjusts ESVO_S to the average eye opening. Analyses zeroes when ES[2] = 0, and ones when ES[2] = 1.
1X01	*Outer:* Adjusts ESVO_S to the outer eye opening (lowest voltage zero, highest voltage 1). Analyses zeroes when ES[2] = 0, and ones when ES[2] = 1.
1X10	*Inner:* Adjusts ESVO_S to the inner eye opening (highest voltage zero, lowest voltage 1). Analyses zeroes when ES[2] = 0, and ones when ES[2] = 1.

All the eye-scan options apart from setting 0X01 analyze only ones or zeroes. Note that the value of INVPAIR is applied before deciding whether a bit is a one or a zero.

Eye-Scan only analyzes every 32nd received bit, the position of which is set by register field ESBSEL.

To build a complete eye, superimpose data from all positions within the word and of both polarities. Alternately, assembling eyes based on every second or fourth bit can establish whether there is any duty cycle or quadrature distortion present in the data stream.

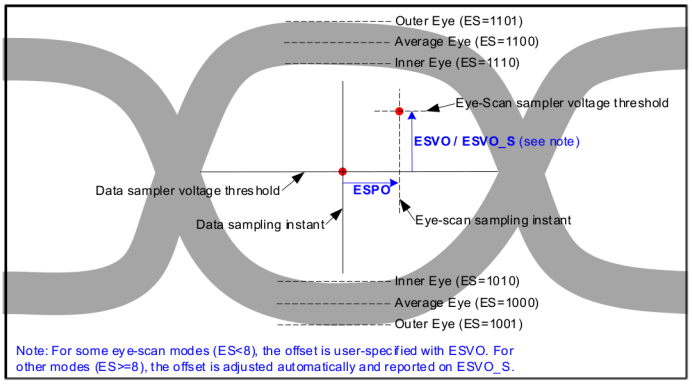


Figure 7-49. Eye-Scan Terminology

7.3.7.2.6.1 Eyescan Procedure

Use the following procedure to use eye-scan.

1. Configure the part for JESD204C operation by following the steps in the JESD204C Usage Model. Return here after setting SYS_EN=1. Eye-scan can be run with JESD204C bitstreams, but can also work with general PRBS input stimulus. Eye-scan runs on all enabled physical lanes simultaneously.
2. Program ES to the desired eye-scan mode.
3. If ES is less than 8, you must program ESVO to the desired voltage offset. For other modes, the eye-scan logic automatically adjusts the voltage offset of the eye-scan sampler.
4. Program ESPO to the desired phase offset.
5. Program ESBSEL to a value from 0 to 31. Eye-scan analyzes every 32th received bit (decimate-by-32). ESBSEL adjusts this decimation phase. For random stimulus, this does not impact the results. If the input has repeating patterns, this can affect the results.
6. Program ESLEN to the desired number of samples. Higher settings gives more consistent results.
7. Set ECOUNT_CLR = 1 then set ECOUNT_CLR = 0 to clear the error counter. This step is recommended, but can be skipped if desired (e.g. to add up counts from multiple eye scan runs). This can also be skipped if ECOUNT won't be used (for modes with ES of 8 or greater)
8. Program ESRUN = 1 to start the scan.
9. Poll ESDONE until ESDONE returns 1 for each of the lanes you want to run eye-scan on.
10. If the selected eye-scan mode modified the eye-scan voltage offset (inner/outer/average modes), read ESVO_S to get the inner/outer/average eye boundary. For other eye-scan modes, read ECOUNT to return the number of mismatches (or matches) recorded.
11. Program ESRUN = 0.

ADVANCE INFORMATION

12. Return to step 2 to run another eye-scan data collection process. The receiver can remain enabled during multiple iterations of steps 2 to 12.

7.3.7.2.6.2 Building an Eye Diagram

There are two basic approaches to build an eye diagram using the eye-scan feature.

1. Fast approach using ESVO_S:
   a. Repeat the procedure outlined in Eyescan Procedure for each valid value of ESPO. For each value of ESPO, run an inner-eye analysis of zeros and ones. This locates the maximum zero ($ESVO_{max0}$) and minimum one ($ESVO_{min1}$) for each value of ESPO.
   b. Each value of ESPO is associated with a column of cells in the eye. All the cells in a column between $ESVO_{max0}$ and $ESVO_{min1}$ (inclusive) can be colored black, and all other cells colored white.
   c. Additional detail can be added to the eye-diagram by including outer and/or average analysis (see ES). For example, the ESVO_S values produced from average analysis can be colored red, while all other values between and including the inner and outer values colored white.
2. Detailed approach using ECOUNT:
   a. Select an eye-scan mode that counts mismatches. Repeat the procedure outlined in Eyescan Procedure for each valid value of ESVO and ESPO.
   b. After each run, record the value of ECOUNT in the PHY_STATUS register (resetting ECOUNT before each run).
   c. Each eye-scan run corresponds to one cell of the eye-diagram. ESPO is the x-coordinate of the cell. ESVO is the y-coordinate of the cell. The intensity of the cell is proportional to $ECOUNT/N_{samples}$, where $N_{samples}$ is the number of analyzed samples per run (determined by ESLEN).
   d. This approach takes much more time to run, but can provide a more granular eye-diagram.

7.3.7.3 Serdes PHY Status

The PHY_LANE register determines which PHY lane is selected for reading status data back via the PHY_STATUS register. The PHY_SSEL register specifies which status field is returned in the PHY_STATUS register.

Table 7-37. Status Values Returned by PHY_STATUS Register

PHY_SSEL	Data returned on PHY_STATUS (reserved bits are omitted)		
0x00	[5]	EQOVER	EQOVER status pre/post cursor analysis. See Pre/Post Cursor Analysis Usage Model
	[4]	EQUNDER	EQUNDER status for pre/post cursor analysis. See Pre/Post Cursor Analysis Usage Model.
	[3:0]	EQLEVEL_S	Returns the equalizer level currently in effect (0 to 14).
0x01	[0]	ESDONE	Returns a 1 to indicate that the eye-scan procedure is completed.
0x02	[5:0]	ESVO_S	Returns the voltage offset result from eye-scan. Applies to eye-scan modes that compute the voltage offset automatically. Only valid when ESDONE returns 1.
0x03	[15:0]	ECOUNT	Returns the mismatch count (applies to eye-scan modes that count mismatches). Only valid when ESDONE returns 1.
0x04-0x05		RESERVED	
0x06	[0]	OCIP	Returns 1 if offset calibration is currently running, or is enabled but has not started yet.
0x10-0x19		RESERVED	

7.3.8 JESD204C Interface

The devices uses a JESD204C high-speed serial interface to transfer data from the logic device to the receiving DAC. The device serialized lanes are capable of operating with both 8b/10b encoding and 64b/66b encoding. The JESD204C formats using 8B/10B encoding are backwards compatible with existing JESD204B receivers.

ADVANCE INFORMATION

A maximum of 16 lanes can be used to lower lane rates for interfacing with speed limited logic devices. There are a few differences between 8b/10b and 64B/66B encoded JESD204C, which is highlighted throughout this section. Figure 7-50 shows a simplified block diagram of the 8b/10b encoded JESD204C interface and Figure 7-51 shows a simplified block diagram of the 64b/66b encoded JESD204C interface.

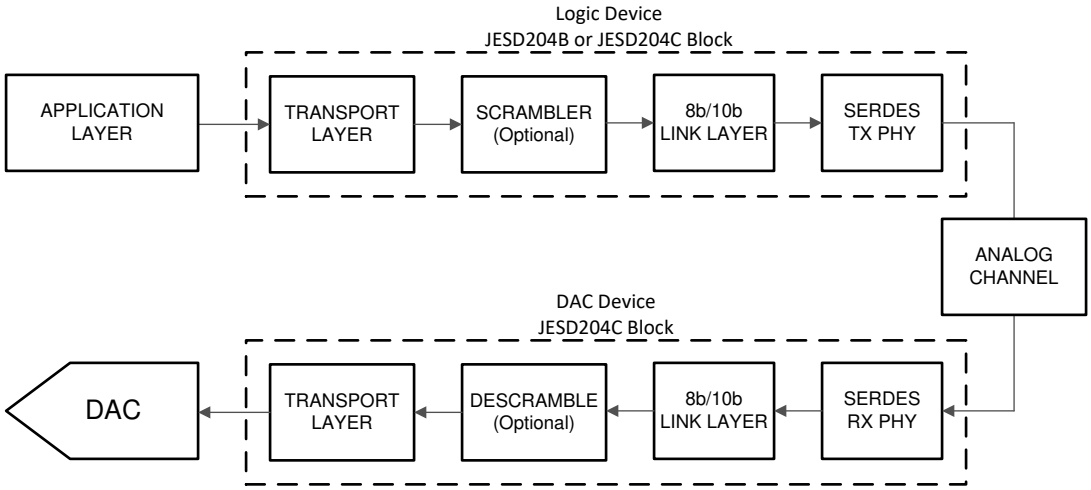


Figure 7-50. Simplified JESD204C Interface Diagram with 8b/10b Encoding

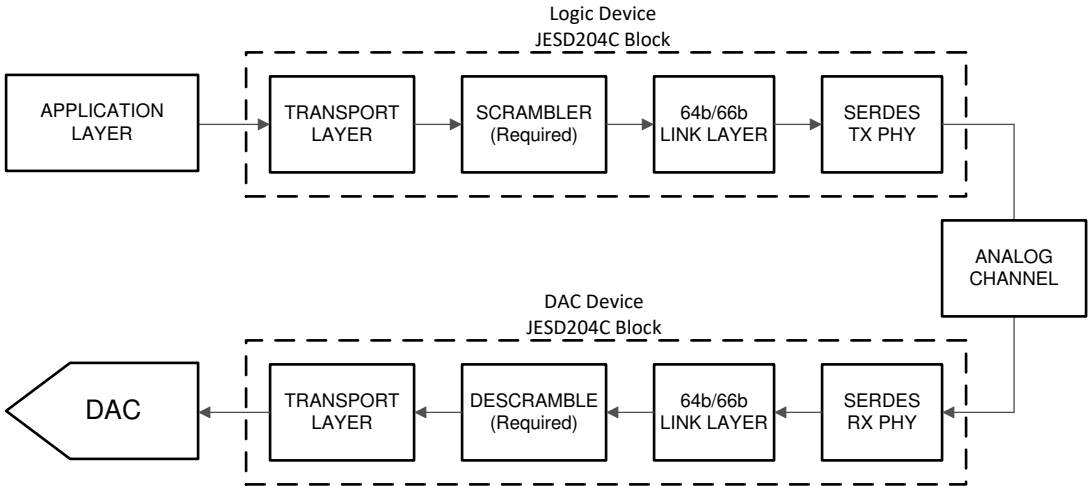


Figure 7-51. Simplified JESD204C Interface Diagram with 64b/66b Encoding

Not all optional features of JESD204C are supported by the device. The list of features that are supported and the features that are not supported is provided in Table 7-38

Table 7-38. Declaration of Supported JESD204C Features

LETTER IDENTIFIER	FEATURE	SUPPORTED BY DEVICE?
a	8b/10b link layer	Yes
b	64b/66b link layer	Yes
c	64b/80b link layer	No
d	The command channel when using 64b/66b or 64b/80b link layer	No
e	Forward error correction (FEC) when using the 64b/66b or 64b/80b link layer	Yes
f	CRC3 when using the 64b/66b or 64b/80b link layer	No

Table 7-38. Declaration of Supported JESD204C Features (continued)

LETTER IDENTIFIER	FEATURE	SUPPORTED BY DEVICE?
g	A physical $\overline{\text{SYNC}}$ pin when using the 8b/10b link layer	Yes
h	Subclass 0	Yes
i	Subclass 1	Yes
j	Subclass 2	No
k	Lane alignment within a single link	Yes
l	Subclass 1 with support for lane alignment on a multipoint link by means of the MULTIREF signal	No
m	$\overline{\text{SYNC}}$ interface timing compatible with JESD204A	Yes
n	$\overline{\text{SYNC}}$ interface timing compatible with JESD204B	Yes

The various signals used in the JESD204C interface and the associated device pin names are summarized briefly in Table 7-39 for reference.

Table 7-39. Summary of JESD204C Signals

SIGNAL NAME	DEVICE PIN NAMES	DESCRIPTION
Data	[15:0]SRX±	High-speed serialized data after 8b/10b or 64b/66b encoding that is received by the SerDes receivers.
$\overline{\text{SYNC}}$	$\overline{\text{SYNC}}$	Link initialization signal (handshake), toggles low to start code group synchronization (CGS) process. Not used for 64B/66B encoding modes.
Device clock	DACCLK+, DACCLK–	DAC sampling clock, also used for clocking digital logic and SerDes receivers.
SYSREF	SYSREF+, SYSREF–	System timing reference used to deterministically reset the internal local multiframe clock (LMFC) or local extended multiblock clock (LEMC) counters in each JESD204C device

7.3.8.1 Deviation from JESD204C Standard

JESD204C section 4.3.4 requires subclass 1 devices to be able to measure the amount of device clock cycles by which the detected active edge of the SYSREF signal deviates from its expected position and not to re-align the LMFC/LEMC if the deviation from the expected position is less than a programmable number of device clock cycles. This design does not contain this feature, but is compliant with JESD204B. The LMFC and other supporting clocks are aligned to the detected SYSREF if the JESD204C subsystem and SYSREF processor are enabled (and SYSREF_ALIGN_EN=1). Implementing the new requirement from JESD204C would severely complicate the clock generation logic. The phase measurements must be processed and passed through the ripple-clock divider architecture, and then phase adjustments must be rippled back toward the root divider.

7.3.8.2 Link Layer

The link layer serves multiple purposes in JESD204C for both 8b/10b and 64b/66b encoding schemes, however there are some differences in implementation for each encoding scheme. In general, the link layer responsibilities include mapping Serdes PHY to JESD "lanes", scrambling of the data (see Scrambler and Descrambler), establishing the code (8b/10b) or block (64b/66b) boundaries and the multiframe (8b/10b) or multiblock (64b/66b) boundaries to de-skew the Serdes lanes, initializing the link, encoding the data, and monitoring the health of the link.

ADVANCE INFORMATION

7.3.8.2.1 Serdes Crossbar

The device includes a crossbar immediately after coming out of the Serdes PHY that allows mapping of signals between lanes to simplify PCB routing between the Tx and Rx which could save PCB complexity or shorten the traces (reduce loss). See LANE_SEL[n].

The physical layer lanes (0SRX± to 15SRX±) must be routed to the appropriate JESD204C lanes (JESD0 to JESD15) based on the lanes defined in the bit packing diagrams shown in JESD204C Format Diagrams.

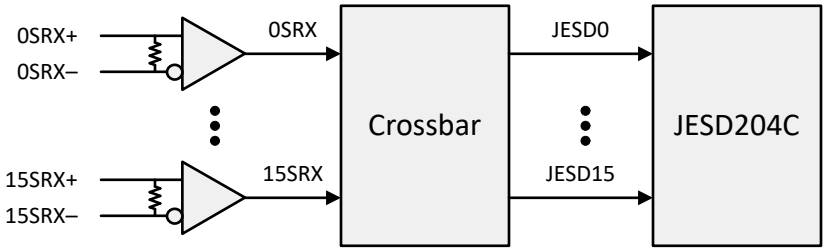


Figure 7-52. Crossbar Block Diagram

7.3.8.2.2 Bit Error Rate Tester

The user can perform bit-error-rate (BER) testing using an error counter that is placed after the crossbar.

BER testing is a PHY level test and the JESD204C link layer encoding (8b/10b or 64b/66b) is not applicable, however JENC still influences the serial bit rate relative to DACCLK.

The user programs JTEST to select which PRBS sequence the receiver expects on all active lanes. When performing BER testing, the serial bit rate (F_{BIT}) is determined in the same fashion as normal modes. The expected PRBS sequences are defined in the following table:

Table 7-40. PRBS Test Modes

PRBS Test Mode	Sequence	Sequence Length (bits)	Notes
PRBS7	y[n] = y[n-6] ^ y[n-7]	127	
PRBS9	y[n] = y[n-5] ^ y[n-9]	511	See JESD204C, Annex K
PRBS15	y[n] = y[n-14] ^ y[n-15]	32767	See JESD204C, Annex K
PRBS31	y[n] = y[n-28] ^ y[n-31]	2,147,483,647	See JESD204C, Annex K

The steps to use the BER tester are

1. Set up the chip and operational parameters according to JESD204C Usage, however do not set SYS_EN.
   a. Program parameters that affect the physical layer such as: JMODE, JESD_M, DSP_L, JENC, LANE_SEL, LANE_INV, REFDIV, MPY and RATE.
   b. You must enable at least one DSP using DSP_MODE*n* if you want LT to be greater than 1 (which affects the link rate). For LT=1, leave all DSPs disabled.
   c. There is no need to program parameters that only impact the link or transport layers, such as SUBCLASS, SFORMAT, SCR, KM1, JESD_M, or RBD.
   d. There is no need to use SYSREF or program SYSREF related parameters.
2. Program JTEST to select the PRBS sequence to verify.
3. Enable the transmitter to send the PRBS sequence on all active lanes.
4. Program SYS_EN=1.
5. Poll the PLL_LOCKED register and wait for PLL_LOCKED to return 1.
6. Wait 4 microseconds (for the PHY to fully initialize and provide valid data to the BER tester).
7. Program BER_EN=1 and LEC_CNT_SEL=0.
8. Read LEC_CNT[n] to get the error count for logical lane n.
9. Program BER_EN=0 and then BER_EN=1 to reset the LEC_CNT values for all lanes and begin counting again.

7.3.8.2.3 Scrambler and Descrambler

A data descrambler is available in the DAC device to descramble the data after reception. Scrambling is used to remove the possibility of spectral peaks in the transmitted data due to repetitive data streams. The scrambler is optional for 8b/10b encoded modes. However it is mandatory for 64b/66b encoded modes to have sufficient spectral content for clock recovery and adaptive equalization. The scrambler operates on the data before encoding, such that the 8b/10b scrambler scrambles the 8-bit octets before 10-bit encoding and the 64b/66b scrambler scrambles the 64-bit block before the sync header insertion (66-bit encoding). The JESD204C receiver automatically synchronizes the descrambler to the incoming scrambled data stream. For 8b/10b encoding, the initial lane alignment sequence (ILA) is never scrambled. The descrambler can be enabled by setting SCR for 8b/10b encoding modes, but it is automatically enabled in 64b/66b modes. The scrambling polynomial is different for 8b/10b encoding and 64b/66b encoding schemes as defined by the JESD204C standard.

7.3.8.2.4 64b and 66b Decoding Link Layer

This section covers the link layer for the 64b/66b decoding operating modes including initialization of the character, frame and multiframe boundaries, alignment of the lanes, 64b/66b encoding and monitoring of the frame and multiframe alignment during operation.

7.3.8.2.4.1 Sync Header Alignment

The device does not use the sync header alignment algorithm that is recommended in the JESD204C standard. The recommended algorithm requires 16 *consecutive* invalid sync headers to lose lock. Since random data looks like a valid sync header 50% of the time, the time to receive 16 *consecutive* invalid sync headers is long.

The device uses an up/down counter scheme to monitor for loss-of-lock:

- Upon initial lock, the device sets a counter = 0.
- When an invalid sync header is received, the counter increments by 16.
- When a valid sync header is received, the counter decrements by 1 (do not decrement below 0).
- If the counter is greater than or equal to 256, detect loss-of-lock.
- Once the elastic buffer is released (LINK_UP=1), a loss-of-lock on one lane resets the gearboxes and the device attempts to reacquire alignment on all lanes.

Since the standard allows for alternate algorithms, this scheme is compliant with the standard.

7.3.8.2.4.2 Extended Multiblock Alignment

Extended Multiblock Alignment is performed as shown in the JESD204C standard in Figure 84. The threshold for the number of consecutive, erroneous sequences to return to the EMB_INIT state is fixed at 8.

7.3.8.2.4.3 Data Integrity

Data integrity is verified by using either CRC or FEC (see SHMODE). Data integrity errors are detected when a multiblock has either a CRC check failure (SHMODE=0) or FEC is unable to correct a detected error (SHMODE=2).

For each lane, the internal signal, DI_FAULT, is set if the number of multi-blocks with CRC or uncorrectable FEC errors exceeds the threshold set by DI_ERR_TH without a run of contiguous, error-free multi-blocks specified by DI_ERR_REC. DI_FAULT is cleared when a run of contiguous, error-free multi-blocks specified by DI_ERR_REC is detected.

Error rate counters are provided for FEC only. CRC error rates can be estimated from PHY level BER testing.

The use FEC error rate testing:

1. Set up the device and operational parameters according to JESD204C Usage, however do not set SYS_EN.
   a. FEC must be enabled (JENC=1 & SHMODE=2).
2. Program FEC_EM_EN=1.
3. Program SYS_EN=1 to start the error counters.
4. Program LEC_CNT_SEL to select the FEC counters to read.
5. Read LEC_CNT[n] to get the error count for logical lane n.

ADVANCE INFORMATION

6. Program FEC_EM_EN=0 and then FEC_EM_EN=1 to reset the LEC_CNT values for all lanes and begin counting again.

Note that FEC is not as effective as CRC at detecting an uncorrectable error and errors that exceed the correction capability can still be reported as correctable. Details about the FEC algorithm can be found in the JESD204C specification.

7.3.8.2.5 8B and 10B Encoding Link Layer

The data link layer converts the 10-bit characters received across the Serdes link into 8-bit octets for the transport layer using 8b/10b decoding. 8b/10b encoding makes sure the DC balance to allow use of AC-coupling between the SerDes transmitter and receiver and specifies a sufficient number of edge transitions for the receiver to reliably recover the data clock. 8b/10b encoding also provides some error detection since a single bit error in a character likely results in either not being able to find the 10-bit character in the 8b/10b decoder lookup table or an incorrect character disparity.

7.3.8.2.5.1 Code Group Synchronization (CGS)

The first step in initializing the JESD204B link, after the LMFC is deterministically reset by SYSREF, is for the receiver to find the boundaries of the encoded 10-bit characters sent across each SerDes lane. This process is called code group synchronization (CGS). The receiver first asserts the $\overline{\text{SYNC}}$ signal (set to logic '0') when ready to initialize the link. The transmitter responds to the request by sending a stream of K28.5 comma characters. The receiver aligns its character clock to the K28.5 character sequence and CGS is achieved after successfully receiving four consecutive K28.5 characters. The receiver deasserts $\overline{\text{SYNC}}$ (set to logic '1') on the next LMFC edge after CGS is achieved and waits for the transmitter to start the initial lane alignment sequence (ILAS).

7.3.8.2.5.2 Initial Lane Alignment Sequence (ILAS)

After the transmitter detects the $\overline{\text{SYNC}}$ signal deassert (logic '0' to logic '1' transition), the transmitter waits until its next LMFC edge to start sending the initial lane alignment sequence (ILAS). The ILAS consists of four multiframes each containing a predetermined sequence. The device receiver searches for the start of the ILAS to determine the frame and multiframe boundaries. Each multiframe of the ILAS starts with a /R/ character (K28.0) and ends with a /A/ character (K28.3) and either can be used to detect the boundary of a multiframe. Each lane starts buffering its data in the elastic buffer once the ILAS reaches the receiver, starting with the /R/ character, until all receivers have received the ILAS and subsequently release the ILAS from all lanes at the same time to align the lanes. The elastic buffer release point is chosen to avoid ambiguity in the release of the data caused by variation in the data delay (arrival of the ILAS at the receiver for each lane). The second multiframe of the ILAS contains configuration parameters for the JESD204B link configuration that can be used by the receiver to verify that the transmitter and receiver configurations match.

7.3.8.2.5.3 Multi-frames and the Local Multiframe Clock (LMFC)

The frames from the transport layer are combined into multiframes which are used in the process of achieving deterministic latency in subclass 1 implementations. The length of a multiframe is set by the K parameter which defines the number of frames in a multiframe. The maximum allowed number of frames per multiframe (K) is 32. The total allowed range of K is defined by the inequality ceil(17/F) ≤ K ≤ min (32, floor (1024/F)) where ceil() and floor() are the ceiling and floor function, respectively. The local multiframe clock (LMFC) keeps track of the start and end of a multiframe for deterministic latency and data synchronization purposes. The LMFC is reset by the SYSREF signal to a deterministic phase in both the transmitter and receiver to act as a timing reference for deterministic latency. The LMFC clock frequency is given in Equation 7 where f_{BIT} is the serialized bit rate (line rate) of the SerDes interface and F and K are as defined above. The frequency of SYSREF must equal to or an integer division of f_{LMFC} if SYSREF is a continuous signal.

$$f_{LMFC} = f_{BIT} / (10 \times F \times K) \quad (7)$$

7.3.8.2.5.4 Frame and Multiframe Monitoring

When a frame alignment character (/F/) or multi-frame alignment character (/A/) is detected in an unexpected location, LANE_ERR[7] is set. No monitoring is performed for missing alignment characters.

The frame alignment monitor inspects both /F/ and /A/ characters to determine if they aligned to the frame boundary. If two characters (either two /F/, two /A/, or one of each) are received in an unexpected location with respect to the frame boundary without receiving an alignment character at an expected frame boundary location, LANE_ERR[5] is set and $\overline{\text{SYNC}}$ is asserted to restart the link.

The multi-frame alignment monitor inspects only /A/ characters to determine if they are aligned to the multi-frame boundary. If two multi-frame alignment characters are received at an unexpected location with respect to the multi-frame boundary without receiving a multi-frame alignment character at an expected multi-frame boundary location, LANE_ERR[6] is set and $\overline{\text{SYNC}}$ is asserted to restart the link.

If the transmitter sends 4 successive /K/ characters after the start of the ILAS, both LANE_ERR[5] and LANE_ERR[6] is set and $\overline{\text{SYNC}}$ is asserted to restart the link.

Frame and multiframe alignment correction is not supported. Two consecutive frame or multiframe alignment errors causes the link to restart.

7.3.8.2.5.5 Link Restart

If any enabled lane detects one of the following conditions, the JESD controller asserts $\overline{\text{SYNC}}$ to restart the link.

- JESD_RST = 1
- The rising edge of SYS_EN
- Transmitter sends 4 successive /K/ characters after the start of the ILAS.
- Gearbox overflow/underflow occurs and GBRST_EN=1
- Code group synchronization is lost as specified in 8.6.1 of the JESD204C spec.
- Two frame/multi-frame alignment characters in unexpected position as specified in Frame & Multi-frame Monitoring
- The JESD204C link layer exits any sleep mode (via changes to MODE)
- SYSREF causes clock or LMFC realignment
- An elastic buffer error is detected

7.3.8.2.5.6 Link Error Reports

Error reporting on $\overline{\text{SYNC}}$ is enabled by setting SYNC_EPW>0. Error reports are issued on $\overline{\text{SYNC}}$ if any enabled lane detects:

- A not-in-table error or unexpected control character error (also reported in LANE_ERR[2]).
  - An unexpected control character error is generated if any control character occurs after the ILAS and is not either /A/ or /F/. The ILAS is not monitored for unexpected control characters.
- A disparity error (also reported in LANE_ERR[1]). A disparity error is generated when:
  - There are more than 6 ones or less than 4 ones in the 10-bit symbol
  - The input disparity is negative and there are less than 5 ones in the 10-bit symbol
  - The input disparity is positive and there are more than 5 ones in the 10-bit symbol
  - The input disparity is negative but the 10-bit symbol only exists for positive disparity
  - The input disparity is positive but the 10-bit symbol only exists for negative disparity
- An alignment character (/A/ or /F/) at an unexpected location (also reported in LANE_ERR[7])

Errors detected while an error report is being sent are not be reported separately.

7.3.8.2.5.7 Watchdog Timer (JTIMER)

The JESD204C receiver includes a watchdog timer to improve reliability. The purpose of the watchdog timer is to reset the PHY layer if the link spends too much time in the “down” state or if the link is up but is generating consistent CRC or uncorrectable FEC errors.

- The watchdog timer consists of an up/down counter that is clocked at F_{DACCLK}/2048. The counter increments/decrements on the rising edge of the clock.
- The counter is initialized to 0 whenever SYS_EN=0 or MODE>1, and begins operating once SYS_EN_EN=1 && MODE<=1 if the JESD interface is enabled (see JESD_M).

ADVANCE INFORMATION

- The counter decrements by a programmable amount (see JTR) if the link is up and the number of FEC or CRC errors does not exceed a threshold (LINK_UP&!DI_FAULT=1). The counter saturates at 0.
- The DI_FAULT signal for this function is extended to so the signal is caught by at least clock edge when a fault is detected.
- The counter increments by 128 if LINK_UP&!DI_FAULT=0.
  - Incrementing the counter never causes overflow.
  - If the counter reaches the threshold defined by JTT, the PHY layer for all lanes are disabled for one $F_{DACCLK}/2048$ cycle. The PHY PLL and reference divider are also disabled for one $F_{DACCLK}/2048$ cycle if and only if JTPLL=1. The counter returns to 0 when the PHY is reset.

7.3.8.3 SYSREF Alignment Required in Subclass 1 Mode

When SUBCLASS=1, the receiver waits for JESD_ALIGNED=1 before measuring lane arrival times (LANE_ARR) or releasing the elastic buffer. This is not prescribed by the JESD204C standard, but is appropriate for these reasons:

1. Waiting makes sure that the reference counter (LMFC/LEMC) used for lane arrival measurements is properly aligned by SYSREF before measuring the lane arrival times. This is important because lane arrival times are only measured once and the user cannot re-measure them unless SYS_EN is cycled (thus resetting the reference counter).
2. Waiting avoids a situation where the link starts up briefly with an arbitrary LMFC/LEMC phase (and arbitrary latency) and then goes back down once SYSREF pulses are processed (this can occur if the SYSREF period is very long).

Additionally, in 8b/10b mode (and SUBCLASS=1), the receiver waits for JESD_ALIGNED=1 before de-asserting $\overline{\text{SYNC}}$.

The JESD_ALIGNED signal is generated according to these rules:

1. JESD_ALIGNED is 0 when SYS_EN is initially set.
2. JESD_ALIGNED is cleared if a SYSREF pulse causes a realignment of any clock that supports the LMFC/LEMC.
3. JESD_ALIGNED is cleared if a SYSREF pulse causes any adjustment of the LMFC/LEMC.
4. JESD_ALIGNED is set if the LMFC/LEMC counter processes two SYSREF alignment events (sysref_align_jctrl pulses) and the second event did not require the LMFC/LEMC phase to be adjusted.
   - The LMFC/LEMC counter may not receive any SYSREF events until all supporting clocks are aligned. Therefore,up to 15 valid SYSREF pulses may be required (while SYSREF_ALIGN_EN=1) to set JESD_ALIGNED.
   - Requiring two SYSREF alignment events to reach the LMFC/LEMC counter makes sure that the link won't come up unless the SYSREF period is valid (avoids false link startups).
5. Any time JESD_ALIGNED is cleared, the counter that counts two SYSREF events (for item #4) is also reset.
6. Note that SYSREF_ALIGN_EN must be set for SYSREF alignment events to reach the LMFC/LEMC counter. If JESD_ALIGNED is already set, and then SYSREF_ALIGN_EN is cleared, and then misaligned SYSREF pulses occur, the JESD_ALIGNED register is unaffected (remains set). This is the intended behavior. To monitor for misaligned SYSREF pulses while SYSREF_ALIGN_EN=0, use the CLK_ALIGNED or SYSREF_ALM registers.

7.3.8.4 Transport Layer

The transport layer decodes the data from the link layer and presents samples to the DSPs or DAC Encoder.

The transport layer takes octets from the link layer and maps them into data streams. The mapping of octets into frames and frames onto lanes is defined by the transport layer settings such as L, M, F, S, N and N'. A frame consists of F octets and the frames are mapped onto L lanes. Samples are N bits, but sent as N' bits across the link. The samples come from M data streams and there are S samples per converter per frame cycle.

There are a number of predefined transport layer modes in the device that are defined in JESD204C Interface Modes. The various configuration parameters for JESD204C block are defined in JESD204C Interface Parameter Definitions.

The link layer further maps the frames into multiframes.

7.3.8.5 JESD204C Debug Capture (JCAP)

7.3.8.5.1 Physical Layer Debug Capture

The JCAP registers can be used to capture the output of the physical layer for general debugging.

The following procedure is used:

1. Set up the part for JESD204C operation (see Startup Procedure, but return here before setting SYS_EN=1).
   a. Some steps are not necessary for a PHY level test. For example, if applying DC or PHY test patterns, there is no need to configure SYSREF, SUBCLASS, RBD, KM1, and so on. The user must still program registers such as: REFDIV, MPY, RATE, and LANE_SEL_x (if applicable).
   b. You must program DSP_L, JESD_M, and JENC because these registers affect the PHY rate and number of lanes.
2. Program JCAP_MODE=0 to capture the PHY output.
3. Apply the desired stimulus to the PHY inputs (DC, PHY test pattern, or JESD204C data).
4. Once registers are configured, set SYS_EN=1.
5. Set JCAP_ARM=1
6. For each logical lane n from 0 to L-1:
   a. Program JCAP_PAGE = n. This allows access to data from lane n.
   b. Read JCAP_STATUS and confirm JCAP_STATUS returns 1 to indicate that lane n has captured data. If JCAP_STATUS returns 0, wait longer for the lane to capture data, and timeout after 100us if no data is captured. If this occurs, verify the PLL is locked (see PLL_LOCKED), and all chip programming is correct.
   c. Read JCAP[0-15] to return up to 16 bytes of data per lane. If doing DC testing, only JCAP[0] needs to be read and verified to return 0x00 or 0xFF depending on the differential input voltage applied to the PHY lane.
   d. If applying a test pattern or JESD204C data, please note that no synchronization is performed. The alignment of the pattern with respect to the byte boundaries of the JCAP registers is arbitrary. Software needs to consider all possible alignments of the data.
   e. Repeat steps (a) thru (c) to inspect data from each lane.
7. If another DC level or pattern is to be tested:
   a. Apply the new DC level or pattern to the PHY inputs.
   b. Program JCAP_ARM=0
   c. Return to step 5.

7.3.8.5.2 Link Layer Debug Capture

The JCAP registers can be used to capture the output of the link layer for general debugging.

The following procedure can be used:

1. Set up the part for JESD204C operation (see Startup Procedure, but return here before setting SYS_EN=1).
2. Program JCAP_MODE=1 to capture the link layer output.
3. Apply JESD204C compliant data to the PHY inputs.
4. Program JCAP_ARM=1.
5. Program JCAP_OFFSET to the desired capture offset. This is especially useful for capturing link configuration octets in the ILAS. See JCAP_OFFSET description.
6. Once registers are configured, set SYS_EN=1.
7. For each logical lane n from 0 to L-1:
   a. Program JCAP_PAGE = n. This allows access to data from lane n.

b. Read JCAP_STATUS and confirm JCAP_STATUS returns 1 to indicate that lane n has captured data. If JCAP_STATUS returns 0, wait longer for the lane to capture data, and timeout if no data is captured. If this occurs, verify the PLL is locked (see PLL_LOCKED), and all chip programming is correct. If the PLL is locked, but no capture is performed, the link layer can have trouble to identifying the multiframe or EMB boundary. Check the transmitter or perform a PHY capture to debug the problem.
c. Read JCAP[0-15] to return up to 16 bytes of data per lane.
d. Repeat steps (a) thru (c) to inspect data from each lane.

8. Another capture (of non-ILAS or payload data) can be performed simply by clearing and then setting JCAP_ARM again. Return to step 7 to read the results of the new capture. To capture the ILAS again, set SYS_EN=0, then return to step 5.

7.3.8.5.3 Transport Layer Debug Capture

The JCAP registers can be used to capture the output of the transport layer for general debugging. Configure the JESD204C transmitter to generate a fixed, repeating sample sequence with a length of one frame (e.g. short transport layer test pattern). The capture is NOT synchronized to a frame boundary. The capture is only synchronized to the application layer clock (depending on JMODE and LT, this does not necessarily correspond to a frame boundary).

To perform a transport layer capture, configure JCAP_MODE=2. Then program JCAP_ARM=1 while the link is up to perform a capture. See also JCAP_STATUS.

After a capture is completed, the data can be read from the JCAP registers. The JCAP_PAGE register must be programmed to access all the pages of data. The organization of the data depends on LT (interpolation factor) and is defined in the following table.

Table 7-41. Transport Layer Capture Map

JCAP_PAGE	Transport Layer Sample Returned from {JCAP[2n+1], JCAP[2n]}				
	LT = 1 (*n*=0..4)	LT = 4 or 6 (*n*=0..7)	LT = 8 or 12 (*n*=0..7)	LT = 16 or 24 (*n*=0..7)	LT = 32 or higher (*n*=0..7)
0	C0[16 ***n***]	C0[8 ***n***]	C0[4 ***n***]	C0[2 ***n***]	C0[***n***]
1	C0[16 ***n*** +1]	C0[8 ***n*** +2]	C0[4 ***n*** +1]	-	-
2	C0[16 ***n*** +2]	C0[8 ***n*** +4]	C0[4 ***n*** +2]	C0[2 ***n*** +1]	-
3	C0[16 ***n*** +3]	C0[8 ***n*** +6]	C0[4 ***n*** +3]	-	-
4	C0[16 ***n*** +4]	C1[8 ***n***]	C1[4 ***n***]	C1[2 ***n***]	C1[***n***]
5	C0[16 ***n*** +5]	C1[8 ***n*** +2]	C1[4 ***n*** +1]	-	-
6	C0[16 ***n*** +6]	C1[8 ***n*** +4]	C1[4 ***n*** +2]	C1[2 ***n*** +1]	-
7	C0[16 ***n*** +7]	C1[8 ***n*** +6]	C1[4 ***n*** +3]	-	-
8	C0[16 ***n*** +8]	C2[8 ***n***]	C2[4 ***n***]	C2[2 ***n***]	C2[***n***]
9	C0[16 ***n*** +9]	C2[8 ***n*** +2]	C2[4 ***n*** +1]	-	-
10	C0[16 ***n*** +10]	C2[8 ***n*** +4]	C2[4 ***n*** +2]	C2[2 ***n*** +1]	-
11	C0[16 ***n*** +11]	C2[8 ***n*** +6]	C2[4 ***n*** +3]	-	-
12	C0[16 ***n*** +12]	C3[8 ***n***]	C3[4 ***n***]	C3[2 ***n***]	C3[***n***]
13	C0[16 ***n*** +13]	C3[8 ***n*** +2]	C3[4 ***n*** +1]	-	-
14	C0[16 ***n*** +14]	C3[8 ***n*** +4]	C3[4 ***n*** +2]	C3[2 ***n*** +1]	-
15	C0[16 ***n*** +15]	C3[8 ***n*** +6]	C3[4 ***n*** +3]	-	-
16	C1[16 ***n***]	C0[8 ***n*** +1]	C4[4 ***n***]	C4[2 ***n***]	C4[***n***]
17	C1[16 ***n*** +1]	C0[8 ***n*** +3]	C4[4 ***n*** +1]	-	
18	C1[16 ***n*** +2]	C0[8 ***n*** +5]	C4[4 ***n*** +2]	C4[2 ***n*** +1]	
19	C1[16 ***n*** +3]	C0[8 ***n*** +7]	C4[4 ***n*** +3]	-	
20	C1[16 ***n*** +4]	C1[8 ***n*** +1]	C5[4 ***n***]	C5[2 ***n***]	C5[***n***]
21	C1[16 ***n*** +5]	C1[8 ***n*** +3]	C5[4 ***n*** +1]	-	-

Table 7-41. Transport Layer Capture Map (continued)

JCAP_PAGE	Transport Layer Sample Returned from {JCAP[2n+1], JCAP[2n]}				
	LT = 1 (*n*=0..4)	LT = 4 or 6 (*n*=0..7)	LT = 8 or 12 (*n*=0..7)	LT = 16 or 24 (*n*=0..7)	LT = 32 or higher (*n*=0..7)
22	C1[16 ***n*** +6]	C1[8 ***n*** +5]	C5[4 ***n*** +2]	C5[2 ***n*** +1]	-
23	C1[16 ***n*** +7]	C1[8 ***n*** +7]	C5[4 ***n*** +3]	-	-
24	C1[16 ***n*** +8]	C2[8 ***n*** +1]	C6[4 ***n***]	C6[2 ***n***]	C6[***n***]
25	C1[16 ***n*** +9]	C2[8 ***n*** +3]	C6[4 ***n*** +1]	-	-
26	C1[16 ***n*** +10]	C2[8 ***n*** +5]	C6[4 ***n*** +2]	C6[2 ***n*** +1]	-
27	C1[16 ***n*** +11]	C2[8 ***n*** +7]	C6[4 ***n*** +3]	-	-
28	C1[16 ***n*** +12]	C3[8 ***n*** +1]	C7[4 ***n***]	C7[2 ***n***]	C7[***n***]
29	C1[16 ***n*** +13]	C3[8 ***n*** +3]	C7[4 ***n*** +1]	-	-
30	C1[16 ***n*** +14]	C3[8 ***n*** +5]	C7[4 ***n*** +2]	C7[2 ***n*** +1]	-
31	C1[16 ***n*** +15]	C3[8 ***n*** +7]	C7[4 ***n*** +3]	-	-

Note

1. All sample fields are 16-bits (two bytes). The most significant byte is read from the higher address (JCAP[2n+1]).
2. For 8 and 12-bit JESD204C modes, the samples are left justified into the 16-bit fields.
3. Cells containing "-" are unused and return undefined data.
4. Sample fields that correspond to disabled streams (that is. converters) return undefined data (that is if JESD_M is programmed to a value that is less than the maximum allowed value).

7.3.8.6 JESD204C Interface Modes

The device JESD204C modes are configured with the parameters defined in Table 7-42, Table 7-43 and Table 7-44.

Table 7-42. JESD204C Interface Parameter Definitions

Parameter	Description
JMODE	JESD204C mode number. The user configures this parameter to choose a supported mode. Most other parameters are derived from this setting. See Table 7-45.
LS	Lanes per sample stream. This is derived from JMODE. See Table 7-45.
LT	Ratio of input sample rate to clock. LT = F_{CLK} / F_{S_IN}. Note that DES2X mode does not affect the value of LT. DSP_MODE*n* = Bypasss (all DSPs disabled, LT = 1. Any DSP Enabled (and JESD_M > 0), LT is set by DSP_L Any DSP Enabled (and JESD_M = 0), LT is not applicable
Lx	Maximum number of lanes used for a given JMODE. The link will scale down the number of active lanes (L) depending on how many channels are enabled. See JESD_M
Mx	Maximum number of streams for a given JMODE. Mx is computed automatically according to Table 7-45. The user can specify the actual number of streams (M) using the JESD_M register.
R	Number of bits transmitted per lane per DACCLK cycle. Derived from JMODE and LT (see Table 7-46). Based on R, the user must program REFDIV, MPY, and RATE registers. Additionally, the maximum DACCLK frequency is a function of R.
SI	Sample Interleaving/Increment Factor. A value of 1 indicates that the standard transport layer mapping from the JESD204C standard is used (samples are mapped linearly from 0 to S-1). A value greater than 1 indicates that an alternate mapping is used as follows: Map samples starting with sample 0, incrementing the index by SI. Repeat this as many times as necessary to map all S samples, starting each repetition at an index that is one larger than the previous repetition. See JESD204C Format Diagrams.

ADVANCE INFORMATION

Table 7-42. JESD204C Interface Parameter Definitions (continued)

Parameter	Description
KR	For 8b/10b operation, KR defines the legal values of K (frames per multiframe). The legal values are restricted to facilitate upset immunity of the elastic buffer. The multiframe length is restricted to a multiple of the elastic buffer depth of 128 characters (buffer depth is reduced to 32 or 64 characters if K*F is 32 or 64). Additionally, having less legal values for K minimizes verification burden. For 8b/10b modes, K is programmed via the KM1 register.

Table 7-43. JESD204C Link Parameters

Parameter	Description	ILAS Field Name	Value for this device see (1)
ADJCNT	DAC LMFC adjustment	ADJCNT[3:0]	n/a
ADJDIR	DAC LMFC adjustment direction	ADJDIR[0]	n/a
BID	Bank ID	BID[3:0]	n/a
CF	Number of control words per frame	CF[4:0]	0
CS	Number. of control bits per sample	CS[1:0]	0
DID	Device identification number	DID[7:0]	n/a
F	Number of octets per frame (per lane)	F[7:0]	See Table 7-45
HD	High Density Format	HD[0]	See Table 7-45
JESDV	JESD204 Version	JESDV[2:0]	n/a
K	Number of frames per multiframe	K[7:0]	Set by KM1 register (2)
L	Number of lanes per link	L[4:0]	ceiling(M/Mx*Lx)
LID	Lane identification no.	LID[4:0]	n/a
M	Number of sample streams per link (see (1))	M[7:0]	Set by JESD_M register
N	Bits per sample (before adding control or tail bits)	N[4:0]	See Table 7-45
N'	Total number of bits per sample (including control and tail bits)	N'[4:0]	See Table 7-45
PHADJ	Phase adjustment request to DAC	PHADJ[0]	n/a
S	Number of samples per stream per frame	S[4:0]	See Table 7-45
SCR	Scrambling enabled	SCR[0]	Set by SCR register
SUBCLASSV	Device Subclass Version	SUBCLASSV[2:0]	n/a
RES1	Reserved field 1	RES1[7:0]	n/a
RES2	Reserved field 2	RES2[7:0]	n/a
CHKSUM	Checksum (sum of all above fields, modulo 256)	FCHK[7:0]	n/a

(1) In 8b and 10b modes, the transmitter may send link configuration octets during the ILAS. The values sent by the transmitter are not checked by this receiver, and they do not need to match the operational values of the receiver. For debugging purposes, specific ILAS octets can be captured and reported via SPI. See JCAP_PAGE and JCAP_OFFSET.
(2) In 8b/10b modes, K is controlled by the KM1 register. In 64b/66b modes, K = 256 x E/F (determined by JMODE).

Table 7-44. Link Parameters (applicable in 64b and 66b encoding only)

Parameter	Description	Value for this device see (1)
E	Number of multi-blocks per extended multi-block (64b and 66b encoding only)	All modes use E=1, except when F=3, then E=3. (E is set automatically based on JMODE).

Each supported mode is assigned a mode number which can be programmed into the JMODE register with the parameters listed in Table 7-45.

Table 7-45. JESD Interface Modes

JMODE	Encoding	Max Input Sample Rate per Stream (GSPS) [1, 2]	MAX Serdes Baud Rate (Gbps)	R = F_{BIT}/ F_{DACCLK} [3]	N	Mx = Max # Streams	Ls = Lanes/ Stream	Lx = Max # Lanes	LT = Interpolation		JESD Format				KR
									MIN	MAX	F	S	HD	SI	
0	8b/10b	22	27.5	1.25	16	1	16	16	1	1	2	16	0	1	32, 64, 128
	64b/66b	22	22.69	1.03125											
1	8b/10b	13	32.5	2.5/LT	16	2	8	16	1	8	2	8	0	1	32, 64, 128
	64b/66b	15.76	32.5	2.0625/LT											
2	8b/10b	6.5	32.5	5/LT	16	4	4	16	1	16	2	4	0	1	32, 64, 128
	64b/66b	7.88	32.5	4.125/LT											
3	8b/10b	3.25	32.5	10/LT	16	8	2	16	4	32	2	2	0	1	32, 64, 128
	64b/66b	3.94	32.5	8.25/LT											
4	8b/10b	1.625	32.5	20/LT	16	8	1	8	4	64	2	1	0	1	32, 64, 128
	64b/66b	1.97	32.5	16.5/LT											
5	8b/10b	0.81	32.5	40/LT	16	8	½	4	8	128	4	1	0	1	16,32,64
	64b/66b	0.98	32.5	33/LT											
6	8b/10b	0.41	32.5	80/LT	16	8	¼	2	16	256	8	1	0	1	8,16,32
	64b/66b	0.49	32.5	66/LT											
7	8b/10b	0.2	32.5	160/LT	16	8	⅛	1	32	256	16	1	0	1	4,8,16
	64b/66b	0.25	32.5	132/LT											
8	8b/10b	22	22	1	12	1	16	16	1	1	8	80	0	16	8,16,32
	64b/66b	22	18.15	0.825											
9	8b/10b	22	27.5	1.25	12	1	12	12	1	1	2	16	1	1	32,64, 128
	64b/66b	22	22.69	1.03125											
10	8b/10b	17.33	32.5	2	12	2	8	16	1	1	8	40	0	8	8,16,32
	64b/66b	21.01	32.5	1.65											
11	8b/10b	13	32.5	2.5	12	2	6	12	1	1	2	8	1	1	32,64, 128
	64b/66b	15.76	32.5	2.0625											
12	8b/10b	8.67	32.5	4	12	2	4	8	1	1	8	20	0	4	8,16,32
	64b/66b	10.51	32.5	3.3											
13	8b/10b	6.5	32.5	5	12	2	3	6	1	1	2	4	1	1	32,64, 128
	64b/66b	7.88	32.5	4.125											
14	8b/10b	22	13.75	0.625	8	1	16	16	1	1	1	16	0	1	64, 128,256
	64b/66b	22	11.34	0.5156											
15	8b/10b	22	27.5	1.25	8	2	8	16	1	1	1	8	0	1	64, 128,256
	64b/66b	22	22.69	1.03125											
16	8b/10b	13	32.5	2.5	8	2	4	8	1	1	1	4	0	1	64, 128,256
	64b/66b	15.76	32.5	2.0625											
17	8b/10b [4]	n/a	n/a	n/a	12	2	8	16	1	1	3	16	0	1	n/a
	64b/66b	21.01	32.5	1.546875											

1. At minimum interpolation rate
2. The encoding (8b/10b or 64b/66b) is restricted for certain combinations of JMODE and LT. See Table 7-46 for details.
3. See Table 7-47 (8b/10b) or Table 7-48 (64b/66b) to program the PHY PLL based on the value of R.
4. This mode does not support 8b/10b encoding.

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 7-46. Interpolation/Upsampling Factors (LT) supported vs. JMODE

User Specified Parameters		Derived Parameters	
JMODE	LT	R [1] (JENC=0) (8b/10b)	R [2] (JENC=1) (64b/66b)
0	1	1.25	1.03125
1	1	2.5	2.0625
	4	0.625	0.515625
	6	0.41667	-
	8	0.3125	-
2	1	5	4.125
	4	1.25	1.03125
	6	0.833	0.6875
	8	0.625	0.515625
	12	0.41667	-
	16	0.3125	-
3	4	2.5	2.0625
	6	1.667	1.375
	8	1.25	1.03125
	12	0.833	0.6875
	16	0.625	0.515625
	24	0.41667	-
	32	0.3125	-
4	4	5	4.125
	6	3.333	2.75
	8	2.5	2.0625
	12	1.667	1.375
	16	1.25	1.03125
	24	0.833	0.6875
	32	0.625	0.515625
	48	0.41667	-
	64	0.3125	-
5	8	5	4.125
	12	3.333	2.75
	16	2.5	2.0625
	24	1.667	1.375
	32	1.25	1.03125
	48	0.833	0.6875
	64	0.625	0.515625
	96	0.41667	-
	128	0.3125	-

Table 7-46. Interpolation/Upsampling Factors (LT) supported vs. JMODE (continued)

User Specified Parameters		Derived Parameters	
JMODE	LT	R [1] (JENC=0) (8b/10b)	R [2] (JENC=1) (64b/66b)
6	16	5	4.125
	24	3.333	2.75
	32	2.5	2.0625
	48	1.667	1.375
	64	1.25	1.03125
	96	0.833	0.6875
	128	0.625	0.515625
	192	0.41667	-
	256	0.3125	-
7	32	5	4.125
	48	3.333	2.75
	64	2.5	2.0625
	96	1.667	1.375
	128	1.25	1.03125
	192	0.833	0.6875
	256	0.625	0.515625
8	1	1	0.825
9	1	1.25	1.031255
10	125	2	1.65
11	1	2.5	2.0625
12	1	4	3.3
13	1	5	4.125
14	1	0.625	0.515625
15	1	1.25	1.03125
16	1	2.5	2.0625
17	1	-	1.546875

1. See Table 7-47 (8b/10b) or Table 7-48 (64b/66b) to program the PHY PLL based on the value of R.
2. If the value of R is unspecified, the associated lane encoding (8b/10b or 64b/66b) is not supported for that particular JMODE and LT settings.

Table 7-47. Parameters derived from R Parameter for 8b/10b Modes (JENC = 0)

R Parameter	Maximum DAC Clock Rate (F_{DACCLK})	Maximum Lane Rate (F_{BIT} = R x F_{DACCLK})
0.3125 (40/128)	25.6GHz	8Gbps
0.416667 (40/96)	25.6GHz	10.667Gbps
0.625 (40/64)	25.6GHz	16Gbps
0.833333 (40/48)	19.2GHz	16Gbps
1 (40/40)	16GHz	16Gbps
1.25 (40/32)	12.8GHz	16Gbps
1.666667 (40/24)	9.6GHz	16Gbps
2 (40/20)	8GHz	16Gbps
2.5 (40/16)	6.4GHz	16Gbps
3.333333 (40/12)	4.8GHz	16Gbps

ADVANCE INFORMATION

Table 7-47. Parameters derived from R Parameter for 8b/10b Modes (JENC = 0) (continued)

R Parameter	Maximum DAC Clock Rate (F_{DACCLK})	Maximum Lane Rate (F_{BIT} = R x F_{DACCLK})
4 (40/10)	4GHz	16Gbps
5 (40/8)	3.2GHz	16Gbps

Table 7-48. Parameters derived from R Parameter for 64b/66b Modes (JENC = 0)

R Parameter	Maximum DAC Clock Rate (F_{DACCLK})	Maximum Lane Rate (F_{BIT} = R x F_{DACCLK})
0.515625 (33/64)	25.6GHz	13.2Gbps
0.6875 (33/48)	25.6GHz	17.6Gbps
0.825 (33/40)	25.6GHz	21.12Gbps
1.03125 (33/32)	25.6GHz	26.4Gbps
1.375 (33/24)	23.636GHz	32.5Gbps
1.546875 (99/64)	21.010GHz	32.5Gbps
1.65 (33/20)	19.697GHz	32.5Gbps
2.0625 (33/16)	15.758GHz	32.5Gbps
2.75 (33/12)	11.818GHz	32.5Gbps
3.3 (33/10)	9.848GHz	32.5Gbps
4.125 (33/8)	7.87GHz	32.5Gbps

7.3.8.6.1 JESD204C Format Diagrams

The following sub-sections depict each JESD204C frame format, showing how samples and tail bits are mapped to the lanes. Any lanes that are not shown in the output format tables are unused. Each table depicts exactly one frame. Tail bits are discarded and ignored by the transport layer. All diagrams are with respect to the logical lane numbers which can be arbitrarily mapped to the external physical lanes using LANE_SELn. Each depiction shows the maximum number of streams (converters) that the mode supports, but the user can configure a smaller number (see JESD_M), which may result in fewer lanes being active.

Table 7-49. JESD Mode Diagram Notation

		Meaning to the Application Layer		
Notation	**Description**	**Bypass Mode**	**DUC Mode**	**DDS-Stream Mode**
T	Tail bits (zeros)	-	-	-
C0[n]	Sample for stream 0	see DAC_SRC	DSP0 (I)	DSP0 (sdata[15:0])
C1[n]	Sample for stream 1	see DAC_SRC	DSP0 (Q)	DSP0 (sdata[31:16])
C2[n]	Sample for stream 2	-	DSP1 (I)	DSP1 (sdata[15:0])
C3[n]	Sample for stream 3	-	DSP1 (Q)	DSP1 (sdata[31:16])
C4[n]	Sample for stream 4	-	DSP2 (I)	DSP2 (sdata[15:0])
C5[n]	Sample for stream 5	-	DSP2 (Q)	DSP2 (sdata[31:16])
C6[n]	Sample for stream 6	-	DSP3 (I)	DSP3 (sdata[15:0])
C7[n]	Sample for stream 7	-	DSP3 (Q)	DSP3 (sdata[31:16])
In all of the above notations, n indicates the sample number (0 to S-1). Some JESD204C modes have S=1 (one sample per stream per frame). In those cases, “[n]” is omitted in the descriptions.				

7.3.8.6.1.1 16-bit Formats

Table 7-50. JMODE 0 (16-bit, 16 lanes per stream, 1 stream)

Octet	0		1	
Nibble	**0**	**1**	**2**	**3**
Lane 0	C0[0]			
Lane 1	C0[1]			

Table 7-50. JMODE 0 (16-bit, 16 lanes per stream, 1 stream) (continued)

Octet	0		1	
Nibble	0	1	2	3
Lane 2	C0[2]			
Lane 3	C0[3]			
Lane 4	C0[4]			
Lane 5	C0[5]			
Lane 6	C0[6]			
Lane 7	C0[7]			
Lane 8	C0[8]			
Lane 9	C0[9]			
Lane 10	C0[10]			
Lane 11	C0[11]			
Lane 12	C0[12]			
Lane 13	C0[13]			
Lane 14	C0[14]			
Lane 15	C0[15]			

Table 7-51. JMODE 1 (16-bit, 8 lanes per stream, 2 streams maximum)

Octet	0		1	
Nibble	0	1	2	3
Lane 0	C0[0]			
Lane 1	C0[1]			
Lane 2	C0[2]			
Lane 3	C0[3]			
Lane 4	C0[4]			
Lane 5	C0[5]			
Lane 6	C0[6]			
Lane 7	C0[7]			
Lane 8	C1[0]			
Lane 9	C1[1]			
Lane 10	C1[2]			
Lane 11	C1[3]			
Lane 12	C1[4]			
Lane 13	C1[5]			
Lane 14	C1[6]			
Lane 15	C1[7]			

Table 7-52. JMODE 2 (16-bit, 4 lanes per stream, 4 streams maximum)

Octet	0		1	
Nibble	0	1	2	3
Lane 0	C0[0]			
Lane 1	C0[1]			
Lane 2	C0[2]			
Lane 3	C0[3]			
Lane 4	C1[0]			
Lane 5	C1[1]			
Lane 6	C1[2]			

ADVANCE INFORMATION

Table 7-52. JMODE 2 (16-bit, 4 lanes per stream, 4 streams maximum) (continued)

Octet	0		1	
Nibble	0	1	2	3
Lane 7	C1[3]			
Lane 8	C2[0]			
Lane 9	C2[1]			
Lane 10	C2[2]			
Lane 11	C2[3]			
Lane 12	C3[0]			
Lane 13	C3[1]			
Lane 14	C3[2]			
Lane 15	C3[3]			

Table 7-53. JMODE 3 (16-bit, 2 lanes per stream, 8 streams maximum)

Octet	0		1	
Nibble	0	1	2	3
Lane 0	C0[0]			
Lane 1	C0[1]			
Lane 2	C1[0]			
Lane 3	C1[1]			
Lane 4	C2[0]			
Lane 5	C2[1]			
Lane 6	C3[0]			
Lane 7	C3[1]			
Lane 8	C4[0]			
Lane 9	C4[1]			
Lane 10	C5[0]			
Lane 11	C5[1]			
Lane 12	C6[0]			
Lane 13	C6[1]			
Lane 14	C7[0]			
Lane 15	C7[1]			

Table 7-54. JMODE 4 (16-bit, 1 lane per stream, 8 streams maximum)

Octet	0		1	
Nibble	0	1	2	3
Lane 0	C0			
Lane 1	C1			
Lane 2	C2			
Lane 3	C3			
Lane 4	C4			
Lane 5	C5			
Lane 6	C6			
Lane 7	C7			

Table 7-55. JMODE 5 (16-bit, 1/2 lane per stream, 8 streams maximum)

Octet	0		1		2		3	
Nibble	0	1	2	3	4	5	6	7
Lane 0	C0				C1			

ADVANCE INFORMATION

Table 7-55. JMODE 5 (16-bit, 1/2 lane per stream, 8 streams maximum) (continued)

Octet	0		1		2		3	
Nibble	0	1	2	3	4	5	6	7
Lane 1	C2				C3			
Lane 2	C4				C5			
Lane 3	C6				C7			

Table 7-56. JMODE 6 (16-bit, 1/4 lane per stream, 8 streams maximum)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lane 0	C0				C1				C2				C3			
Lane 1	C4				C5				C6				C7			

Table 7-57. JMODE 7 (16-bit, 1/8 lane per stream, 8 streams maximum)

Octet	0		1		2		3		4		5		6		7		8		9		10		11		12		13		14		15	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Lane 0	C0				C1				C2				C3				C4				C5				C6				C7			

7.3.8.6.1.2 12-bit Formats

Table 7-58. JMODE 8 (12-bit, 16 lanes per stream, 1 stream)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lane 0	C0[0]		C0[16]				C0[32]		C0[48]				C0[64]			T
Lane 1	C0[1]		C0[17]				C0[33]		C0[49]				C0[65]			T
Lane 2	C0[2]		C0[18]				C0[34]		C0[50]				C0[66]			T
Lane 3	C0[3]		C0[19]				C0[35]		C0[51]				C0[67]			T
Lane 4	C0[4]		C0[20]				C0[36]		C0[52]				C0[68]			T
Lane 5	C0[5]		C0[21]				C0[37]		C0[53]				C0[69]			T
Lane 6	C0[6]		C0[22]				C0[38]		C0[54]				C0[70]			T
Lane 7	C0[7]		C0[23]				C0[39]		C0[55]				C0[71]			T
Lane 8	C0[8]		C0[24]				C0[40]		C0[56]				C0[72]			T
Lane 9	C0[9]		C0[25]				C0[41]		C0[57]				C0[73]			T
Lane 10	C0[10]		C0[26]				C0[42]		C0[58]				C0[74]			T
Lane 11	C0[11]		C0[27]				C0[43]		C0[59]				C0[75]			T
Lane 12	C0[12]		C0[28]				C0[44]		C0[60]				C0[76]			T
Lane 13	C0[13]		C0[29]				C0[45]		C0[61]				C0[77]			T
Lane 14	C0[14]		C0[30]				C0[46]		C0[62]				C0[78]			T
Lane 15	C0[15]		C0[31]				C0[47]		C0[63]				C0[79]			T

Table 7-59. JMODE 9 (12-bit, 12 lanes per stream, 1 stream)

Octet	0		1	
Nibble	0	1	2	3
Lane 0	C0[0]			C0[1][11:8]
Lane 1	C0[1][7:0]		C0[2] [11:4]	
Lane 2	C0[2] [3:0]	C0[3]		
Lane 3	C0[4]			C0[5][11:8]
Lane 4	C0[5][7:0]		C0[6] [11:4]	
Lane 5	C0[6] [3:0]	C0[7]		
Lane 6	C0[8]			C0[9][11:8]

ADVANCE INFORMATION

Table 7-59. JMODE 9 (12-bit, 12 lanes per stream, 1 stream) (continued)

Octet	0		1	
Nibble	0	1	2	3
Lane 7	C0[9][7:0]		C0[10] [11:4]	
Lane 8	C0[10] [3:0]	C0[11]		
Lane 9	C0[12]			C0[13][11:8]
Lane 10	C0[13][7:0]		C0[14] [11:4]	
Lane 11	C0[14] [3:0]	C0[15]		

Table 7-60. JMODE 10 (12-bit, 8 lanes per stream, 2 streams maximum)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lane 0	C0[0]		C0[8]				C0[16]		C0[24]				C0[32]			T
Lane 1	C0[1]		C0[9]				C0[17]		C0[25]				C0[33]			T
Lane 2	C0[2]		C0[10]				C0[18]		C0[26]				C0[34]			T
Lane 3	C0[3]		C0[11]				C0[19]		C0[27]				C0[35]			T
Lane 4	C0[4]		C0[12]				C0[20]		C0[28]				C0[36]			T
Lane 5	C0[5]		C0[13]				C0[21]		C0[29]				C0[37]			T
Lane 6	C0[6]		C0[14]				C0[22]		C0[30]				C0[38]			T
Lane 7	C0[7]		C0[15]				C0[23]		C0[31]				C0[39]			T
Lane 8	C1[0]		C1[8]				C1[16]		C1[24]				C1[32]			T
Lane 9	C1[1]		C1[9]				C1[17]		C1[25]				C1[33]			T
Lane 10	C1[2]		C1[10]				C1[18]		C1[26]				C1[34]			T
Lane 11	C1[3]		C1[11]				C1[19]		C1[27]				C1[35]			T
Lane 12	C1[4]		C1[12]				C1[20]		C1[28]				C1[36]			T
Lane 13	C1[5]		C1[13]				C1[21]		C1[29]				C1[37]			T
Lane 14	C1[6]		C1[14]				C1[22]		C1[30]				C1[38]			T
Lane 15	C1[7]		C1[15]				C1[23]		C1[31]				C1[39]			T

Table 7-61. JMODE 11 (12-bit, 6 lanes per stream, 2 streams maximum)

Octet	0		1	
Nibble	0	1	2	3
Lane 0	C0[0]			C0[1][11:8]
Lane 1	C0[1][7:0]		C0[2] [11:4]	
Lane 2	C0[2] [3:0]	C0[3]		
Lane 3	C0[4]			C0[5][11:8]
Lane 4	C0[5][7:0]		C0[6] [11:4]	
Lane 5	C0[6] [3:0]	C0[7]		
Lane 6	C1[0]			C1[1][11:8]
Lane 7	C1[1][7:0]		C1[2] [11:4]	
Lane 8	C1[2] [3:0]	C1[3]		
Lane 9	C1[4]			C1[5][11:8]
Lane 10	C1[5][7:0]		C1[6] [11:4]	
Lane 11	C1[6] [3:0]	C1[7]		

Table 7-62. JMODE 12 (12-bit, 4 lanes per stream, 2 streams maximum)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lane 0	C0[0]		C0[4]				C0[8]		C0[12]				C0[16]			T

ADVANCE INFORMATION

Table 7-62. JMODE 12 (12-bit, 4 lanes per stream, 2 streams maximum) (continued)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lane 1	C0[1]		C0[5]				C0[9]				C0[13]			C0[17]		T
Lane 2	C0[2]		C0[6]				C0[10]				C0[14]			C0[18]		T
Lane 3	C0[3]		C0[7]				C0[11]				C0[15]			C0[19]		T
Lane 4	C1[0]		C1[4]				C1[8]				C1[12]			C1[16]		T
Lane 5	C1[1]		C1[5]				C1[9]				C1[13]			C1[17]		T
Lane 6	C1[2]		C1[6]				C1[10]				C1[14]			C1[18]		T
Lane 7	C1[3]		C1[7]				C1[11]				C1[15]			C1[19]		T

Table 7-63. JMODE 13 (12-bit, 3 lanes per stream, 2 streams maximum)

Octet	0		1	
Nibble	0	1	2	3
Lane 0	C0[0]			C0[1][11:8]
Lane 1	C0[1][7:0]		C0[2] [11:4]	
Lane 2	C0[2] [3:0]	C0[3]		
Lane 3	C0[4]			C0[5][11:8]
Lane 4	C0[5][7:0]		C0[6] [11:4]	
Lane 5	C0[6] [3:0]	C0[7]		

Table 7-64. JMODE 17 (12-bit, 8 lanes per stream, 2 streams maximum)

Octet	0		1		2	
Nibble	0	1	2	3	4	5
Lane 0	C0[0]			C0[1]		
Lane 1	C0[2]			C0[3]		
Lane 2	C0[4]			C0[10]		
Lane 3	C0[6]			C0[11]		
Lane 4	C0[8]			C0[12]		
Lane 5	C0[10]			C0[13]		
Lane 6	C0[12]			C0[14]		
Lane 7	C0[14]			C0[15]		
Lane 8	C1[0]			C1[1]		
Lane 9	C1[2]			C1[3]		
Lane 10	C1[4]			C1[5]		
Lane 11	C1[6]			C1[7]		
Lane 12	C1[8]			C1[9]		
Lane 13	C1[10]			C1[11]		
Lane 14	C1[12]			C1[13]		
Lane 15	C1[14]			C1[15]		

7.3.8.6.1.3 8-bit Formats

Table 7-65. JMODE 14 (8-bit, 16 lanes per stream, 1 stream)

Octet	0	
Nibble	0	1
Lane 0	C0[0]	
Lane 1	C0[1]	
Lane 2	C0[2]	

ADVANCE INFORMATION

Table 7-65. JMODE 14 (8-bit, 16 lanes per stream, 1 stream) (continued)

Octet	0	
Nibble	0	1
Lane 3	C0[3]	
Lane 4	C0[4]	
Lane 5	C0[5]	
Lane 6	C0[6]	
Lane 7	C0[7]	
Lane 8	C0[8]	
Lane 9	C0[9]	
Lane 10	C0[10]	
Lane 11	C0[11]	
Lane 12	C0[12]	
Lane 13	C0[13]	
Lane 14	C0[14]	
Lane 15	C0[15]	

Table 7-66. JMODE 15 (8-bit, 8 lanes per stream, 2 streams maximum)

Octet	0	
Nibble	0	1
Lane 0	C0[0]	
Lane 1	C0[1]	
Lane 2	C0[2]	
Lane 3	C0[3]	
Lane 4	C0[4]	
Lane 5	C0[5]	
Lane 6	C0[6]	
Lane 7	C0[7]	
Lane 8	C1[0]	
Lane 9	C1[1]	
Lane 10	C1[2]	
Lane 11	C1[3]	
Lane 12	C1[4]	
Lane 13	C1[5]	
Lane 14	C1[6]	
Lane 15	C1[7]	

Table 7-67. JMODE 16 (8-bit, 4 lanes per stream, 2 streams maximum)

Octet	0	
Nibble	0	1
Lane 0	C0[0]	
Lane 1	C0[1]	
Lane 2	C0[2]	
Lane 3	C0[3]	
Lane 4	C1[0]	
Lane 5	C1[1]	
Lane 6	C1[2]	

Table 7-67. JMODE 16 (8-bit, 4 lanes per stream, 2 streams maximum) (continued)

Octet	0	
Nibble	0	1
Lane 7	C1[3]	

7.3.8.6.2 DUC and DDS Modes

The device contains a DUC mode and a direct digital synthesis (DDS) mode. The data path mode uses complex (I and Q) data from the JESD interface, interpolate and upconverts the data in the DUCs, sums the DUC outputs and generates the analog signal in the DAC. In DDS mode, the DUC NCOs are used directly to generate tones without requiring input data.

The list below summarized how DDS mode differs from DUC mode:

1. Interpolation filters are not enabled
2. JESD204C interface is not enabled
3. NCOs use less power (no complex mixing)
4. AMP register supplies unique amplitudes for each DUC (DDS) channel, allowing DDS channels to generate tones to cancel harmonic tones in the DAC output. For example, if DDS channel 0 produces a fundamental tone, channel 1 can produce a tone to cancel HD2, and channel 2 can produce a tone to cancel HD3.
5. The JMODE and DUC_L registers are ignored and the SYSREF period constraints imposed by the JESD204C system and interpolation filters are removed.

7.3.9 Data Path Latency

There are several difference latencies defined for the device as shown in Figure 7-53 and listed in Table 7-68. Many of these parameters depend on the chip configuration (JMODE, LT, JENC, RBD, NCO_EN, MXMODE (DES2X), PFIR_EN, PFIR_MODE). An Excel spreadsheet calculator is provided by TI to calculate the device latency in different modes of operation.

In JESD204C subclass 0 operation, the latency from Serdes input to DAC output is called T_{DAC_LAT0} and is not deterministic and a minimum and maximum range is provided in the Excel spreadsheet calculator.

In JESD204C subclass 1 operation, the latency T_{DAC_LAT} from the SYSREF input to DAC output is deterministic and is provided in the Excel spreadsheet calculator. The JESD204C link from JESD204C transmitter to output from the RxFIFO output can also has deterministic latency as long as the RBD value is set properly (the proper conditions depend in the latency of the SYSREF and link paths and are shown in Figure 7-53).

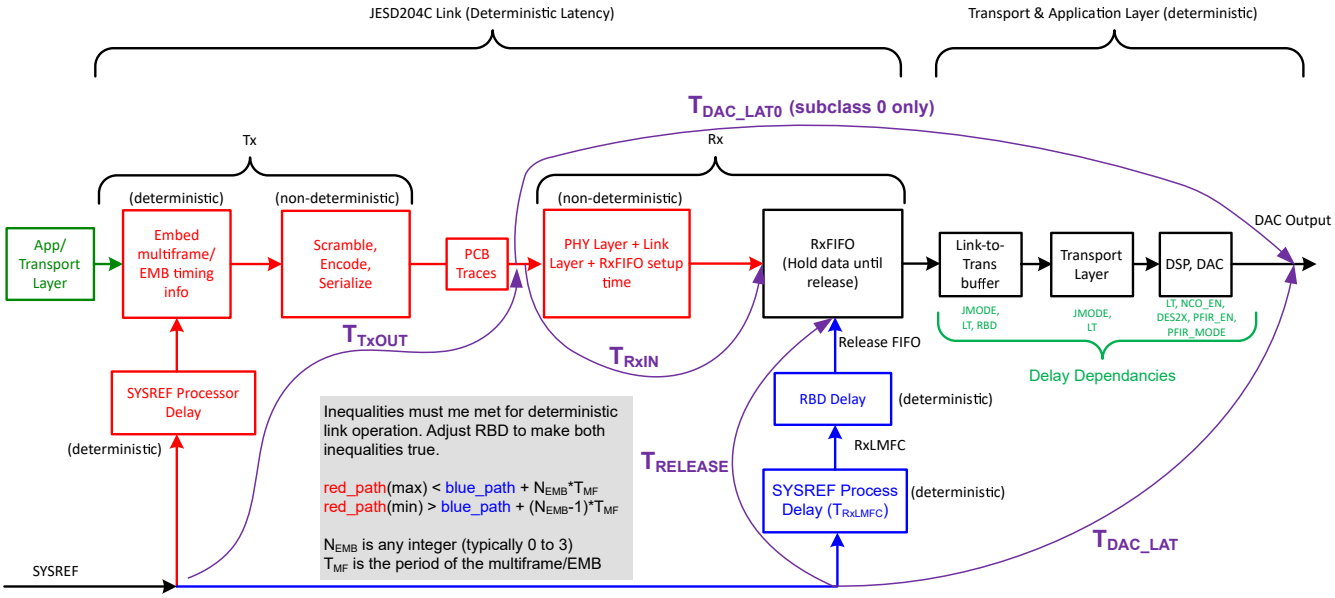


Figure 7-53. Definition of Device Latencies

Table 7-68. Latency Definitions

Latency Parameter	Definition
$T_{RELEASE}$	Latency from the rising edge of DACCLK that follows the rising edge of SYSREF to release event for elastic buffer. (subclass 1 only).
T_{DAC_LAT}	Latency from he rising edge of DACCLK that follows the rising edge of SYSREF to the time of the first sample at the DAC output of the multiframe/extended multiblock launched by SYSREF (subclass 1 only).
T_{RxIN}	Latency from the receiver data inputs to the elastic buffer input, including the minimum setup time of the elastic buffer. This is non-deterministic, so a minimum and maximum limit are provided.
T_{TxOUT}	Latency from transmitter device SYSREF input to the multiframe or EMB boundary coming out of the transmitter (Tx) and arriving at the receiver (Rx).
T_{DAC_LAT0}	Latency from receiver data inputs (multiframe/EMB boundary) to first sample of a multiframe launched on DAC output. This is non-deterministic, so a minimum and maximum limit are provided (subclass 0 only).

7.3.10 Multi-Device Synchronization and Deterministic Latency

JESD204C subclass 1 outlines a method to achieve deterministic latency across the serial link. Multi-device synchronization is not possible when using the PLL/VCO. If two devices achieve the same deterministic latency then they can be considered synchronized. This latency must be achieved from system startup to startup to be deterministic. There are two key requirements to achieve deterministic latency. The first is proper capture of SYSREF. SYSREF resets the LMFC counter in each device to act as a known timing reference.

The second requirement is to choose a proper elastic buffer release point in the receiver. The converter device is the receiver (RX) in the JESD204C link and the logic device is the transmitter (TX). The elastic buffer is the key block for achieving deterministic latency and does so by absorbing variations in the propagation delays of the serialized data as the data travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against delay variations. An incorrect release point results in a latency variation of one LMFC period, or in some cases result in a buffer overflow that prevents the link from establishing. Only when the multiframe is short can the user get a bad release point and when that happens. The lanes are usually deskewed incorrectly resulting in bad data. Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer, referenced to an LMFC edge, and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must makes sure that the data for all lanes arrives at all devices after the previous release point occurs and before the next release point occurs. The invalid region can also be found experimentally, see Programming RBD.

Figure 7-54 provides a simplified timing diagram that demonstrates this requirement. In this figure, the data for two transmitters (ADC or logic device) is shown. The second transmitter (TX 2) has a longer routing distance (t_{PCB}) and results in a longer link delay than the first transmitter (TX 1). First, the invalid region of the LMFC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of quad-octet steps from the LMFC edge so that the release point occurs within the valid region of the LMFC cycle. For Figure 7-54, the LMFC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side of the valid region.

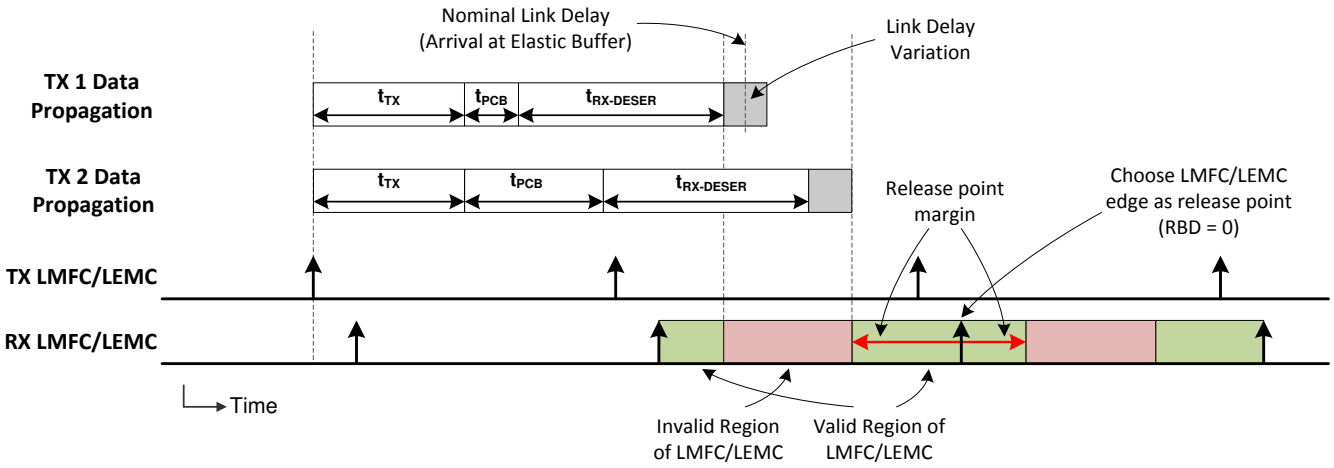


Figure 7-54. LMFC Valid Region Definition for Elastic Buffer Release Point Selection

The TX and RX LMFC do not necessarily need to be phase aligned, but knowledge of their phase is important for proper elastic buffer release point selection. Also, the elastic buffer release point occurs within every LMFC cycle, but the buffers only release when all lanes have arrived. Therefore, the total link delay can exceed a single LMFC period; see *JESD204B multi-device synchronization: Breaking down the requirements* for more information.

7.3.10.1 Programming RBD

In subclass 1 operation, the RBD register must be programmed properly to prevent overflow of the elastic buffer

The range of valid values for RBD depends on the phase delta between the RX and TX LMFC/LEMC, as well as link latencies in the SerDes transmitter, channel, and SerDes receiver. Therefore a pre-determined RBD value that is valid for all systems cannot be provided. The LANE_ARR registers are provided to help the user measure lane arrival times and select an appropriate RBD value for the system. To makes sure deterministic latency, the RBD value can be selected during system prototyping and stored in system firmware. Calculating RBD each time the system is turned on can result in non-deterministic latency.

The arrival times are reported in units of octa-bytes (8 bytes) and are measured with respect to a reference counter that increments for each octo-byte received (per lane). The reference counter is aligned (reset) by SYSREF and operates with a modulus of 32 octa-bytes (256 bytes) regardless of the value of K for 8b/10b modes. The modulus is 32*E octa-bytes (256*E bytes) for 64b/66b modes. The depth of the elastic buffer is denoted as EBD, and depends on the length of the multiframe/EMB.

Table 7-69. Modulus used for Reference Counter and LANE_ARR values

Link Encoding	AM (Modulus for Reference Counter and LANE_ARR) [octa-bytes]
8b/10b (JENC = 0)	32
64b/66b (JENC = 1)	32*E

Since the lane arrival times are modulo-values, using arithmetic that accounts for the modulus (the *latest* arriving lane can actually have a *smaller* LANE_ARR value than the earliest arriving lane) is important. Figure 7-55 and Figure 7-56 depict the RBD calculation graphically to emphasize this. The lane arrival times are mapped onto a circle with a circumference of 64 quad-bytes which corresponds to the modulo-64 counter used to measure lane arrival times.

The earliest usable RBD value is equal to the latest LANE_ARR value plus 1 (modulo AM). The latest usable RBD value is equal to the earliest LANE_ARR value plus the buffer depth (modulo AM) (the buffer depth is denoted by EBD). Note that the latest, usable RBD value causes the earliest arriving lane to overwrite buffer data on the same clock cycle that the data is being read out (this is acceptable and does not cause overflow).

ADVANCE INFORMATION

Choosing an RBD value in the middle of the usable range maximizes the skew tolerance, however the user can choose a value closer to the latest arriving lane if lower latency is desired.

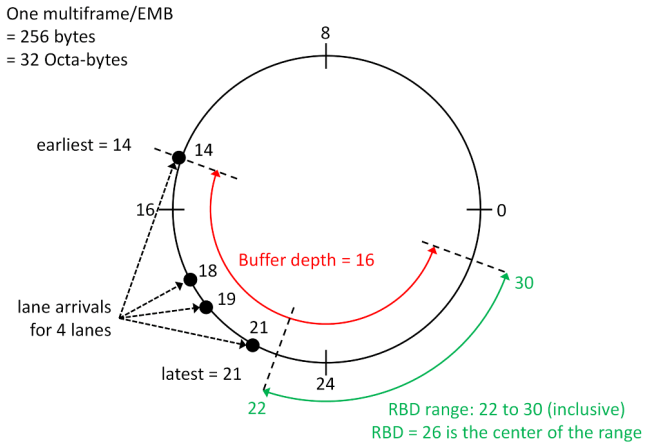


Figure 7-55. RBD Example (lane arrivals do not straddle zero)

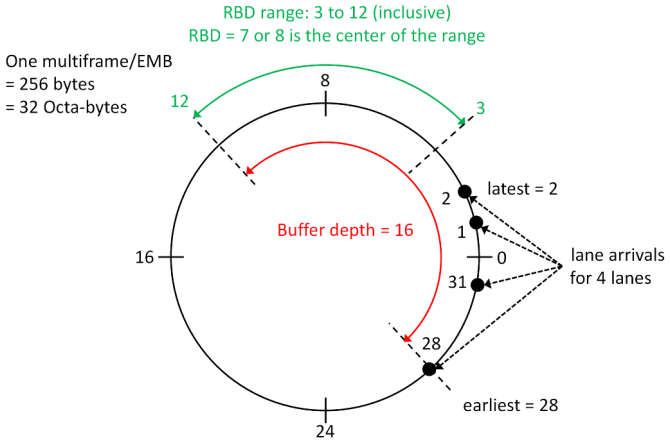


Figure 7-56. RBD Example (lane arrivals straddle zero)

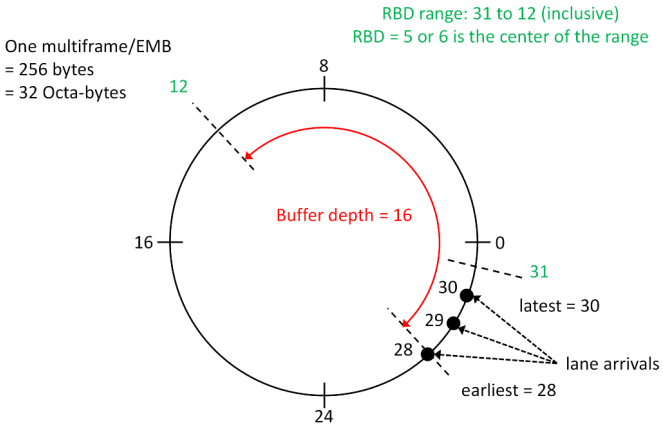


Figure 7-57. RBD Example (valid RBD range straddle zero)

7.3.10.2 Multiframe Lengths less than 32 Octa-Bytes (256 Bytes)

For 8b/10b modes, the lane arrival times are always measured using a 5-bit, modulo-32 counter, regardless of the actual multiframe length.

When the multiframe length is also 32 octa-bytes, the entire 5-bit counter is aligned by SYSREF. When the multiframe length is 16, or 8 octa-bytes, only the lower 4 or 3 bits (respectively) of the counter are aligned by SYSREF, and the upper bits are left to free-run. This arrangement allows the user to unambiguously determine which lanes are the earliest and latest lanes, even when lane skew is as high as 15 octa-bytes (there is a large, unambiguous empty space on the 32 octa-byte circle that separates the latest lane from the earliest lane).

When the multiframe length is less than 32 octa-bytes, the LANE_ARR values can significantly change from one link startup to the next, however this does not interfere with the RBD calculation as long as the user does not mix LANE_ARR data from multiple link startups.

7.3.10.3 Recommended Algorithm to Determine the RBD Value

```
initial begin
int tries;
int arrival [];

// Start the link according to Startup Procedure. Any value of RBD is okay.
// Note that LINK_UP may not be set since RBD can be invalid.

startup_link();
// Wait for LANE_ARR_RDY to go high
// Give up after 1000 tries.
tries = 0;
while(read_reg(LANE_ARR_RDY)==0 && tries<1000)
tries++;

// Read LANE_ARR for all lanes
arrival = new [L];

foreach(arrival[i]) arrival[i] = read_reg(LANE_ARR[i]);

RBD = determine_RBD(arrival, K*F/8);
// Use this RBD value to restart the link
end

// This function computes RBD from an array of arrival times
function determine_RBD(
int arrival [], // A dynamic array of arrival times from LANE_ARR
int oneMF // Number of octa-bytes per multiframe/EMB
);
int spacing, max_spacing;
int latest, earliest;
int L, early_overwrite;
```

ADVANCE INFORMATION

```
int AM, EB_size;

// Buffer size is up to 16 octa-bytes, but never more than oneMF
EB_size = oneMF > 16 ? 16 : oneMF;

// Modulo-value for LANE_ARR
AM = JENC ? 32*E : 32;

// Number of lanes is the size of the arrival array
L = arrival.size;
// Sort arrival list in ascending numeric order
arrival.sort;

// Find the largest spacing between arrival times (on a circle)
max_spacing = 0;
for(int i = 0; i<L; i++) begin
spacing = arrival[(i+1)%L] – arrival[i] + (i==L-1)*AM;
if(spacing>max_spacing) begin
max_spacing = spacing;
latest = arrival[i];
earliest = arrival[(i+1)%L];
end
end

// Check that lane skew is not too large for the elastic buffer
if ( (latest-earliest+AM)%AM >= EB_size ) begin
$display(“ERROR: Lane skew too large for elastic buffer”);
$display(“ Earliest=%0d Latest=%0d”);
return 0;
end

// Choose RBD to be halfway between the latest arriving lane (+1) and the moment
// the earliest lane begins to over-write the elastic buffer.
early_overwrite = (earliest+EB_size)%AM;
if(early_overwrite < latest+1) early_overwrite += AM;
return (latest+1+early_overwrite)/2 % oneMF;

endfunction
```

7.3.10.4 Operation in Subclass 0 Systems

The device can operate with subclass 0 compatibility provided that multi-DAC synchronization and deterministic latency are not required. With these limitations, the device can operate without the application of SYSREF. The

internal LMFC is automatically self-generated with unknown starting phase. $\overline{\text{SYNC}}$ is used as normal to initiate the CGS and ILAS.

7.3.11 Link Reset

The entire link layer for all lanes is reset any time:

- There is a gearbox FIFO underflow/overflow detected (LANE_ERR) on a lane used by the JESD link
- There is an elastic buffer overflow detected (EB_ERR) on a lane used by the JESD link
- The JESD link goes down (JESD_LINK_DOWN_ALM)
- SYSREF causes clock divider or LMFC/LEMC realignment (CLK_REALIGNED)
- The JTimer expires (JTIMER_EXPIRED_ALM, JTIMER)
- SYS_EN=0
- JESD_RST=0
- MODE≥2

7.3.12 Alarm Generation

The alarm pin is useful for notifying the host controller of events that may require intervention. Any active alarms in the SYS_ALM register asserts the alarm output if they are not masked in the ALM_MASK register.

In addition to the mission mode operation, the alarm pin can also be used as a test output. See ALARM_SEL.

7.3.12.1 Over Range Detection

The datapath has the ability to detect an over-range condition and record the event in the OVR_STATUS register.

The OVR_STATUS register has a bit for each DSP channel and DAC channel. If any bit of OVR_STATUS is set, then the OVR_ALM bit is also set, and if OVR_MASK=0, then the alarm output is asserted. The user can choose to clear the alarm by writing a '1' to the OVR_ALM bit, which also clears all bits of the OVR_STATUS register. The user can also choose to clear all the bits of the OVR_STATUS register directly by writing a '1' to the register.

For some components of the datapath, an over-range condition is defined as a full-scale sample. For other components, saturation must occur. The distinction is minor and does not impact the usefulness of this feature. The location of the detectors is depicted in Figure 7-10.

An OVR_DSP*n* bit is set if any of the following events occur in DSP*n*:

1. In DUC mode, the interpolation filter produced an interpolated sample that is equal to full scale. This can occur even if all the DUC input samples are below full-scale.
2. The user inputs a full-scale sample to the DUC via the JESD204C interface (attenuation by the PFIR when enabled before the DUC can prevent this detection).
3. The PFIR is enabled before the DUC and the PFIR produced a full-scale sample due to PFIR gain greater than unity.
4. Saturation occurred in the mixer. This can occur if the mixer rotated the I/Q sample and saturation was the result. This can occur if the absolute value of the I/Q input samples is greater than full scale and the DSP_GAIN*n* is large enough.

An OVR_DAC*n* bit is set if any of the following events occur on DAC channel *n*:

1. Saturation occurred in the channel bonder.
   a. This can be the result of summing multiple DSP channels together, or the result of one DSP channel producing a 20-bit output sample that is slightly saturated to the 16-bit full scale output of the channel bonder.
   b. Saturation in the channel bonder can be detected even if the PFIR subsequently attenuates the sample before the sample reaches the DAC.
2. The DES2X filter for DACn produced a full-scale sample (even if the DES2X filter has no full-scale input samples).

ADVANCE INFORMATION

3. The PFIR is configured to filter the channel bonder output, and the PFIR applied gain to produce a full-scale sample.

Any datapath component that is disabled shall never detect an over-range condition (full-scale sample and/or saturation). For example:

1. If DSP0 was configured in DUC mode, filled with full-scale samples, and then SYS_EN is cleared to reconfigure DSP0 into a non-DUC mode (or disabled), the full scale sample inside the disabled DUC shall not be detected anymore (even after setting SYS_EN=1 again).
2. If a PFIR or DES2X filter was filled with full-scale samples, but then SYS_EN is cleared and the part is reconfigured to not use the PFIR or DES2X filter, then the full-scale samples inside the PFIR or DES2X filter are not detected when the datapath is re-enabled with SYS_EN.

7.3.12.2 Over Range Masking

If the user does not want over-range events to impact the alarm output, set OVR_MASK=1. The events are still detected and reported in OVR_STATUS and OVR_ALM, but do not impact the alarm output.

Additionally, the user can instruct the part to temporarily stop detecting and recording over-range events (mask the events). The user can choose to do this when inputting a signal that is expected to cause over-range and do not want the event reported. The user can choose one of several input pins to act as the mask signal. These are detailed in the following Table 7-70. If no pin is configured as a mask signal, then all events are detected and recorded.

Table 7-70. Over Range Masking Programming and Behavior

Pin	Programming to use the pin as an over-range mask	When are over-range (full-scale) events masked
TRIG[4]	OVR_MASK_SEL=1	Events are ignored while TRIG[4] is high.
SYNCB	SYNCB_PIN_FUNC=14	Events are ignored while SYNCB is low.
TXENABLE[0]	TX_PIN_FUNC0=14	Events are ignored while TXENABLE[0] is low.
TXENABLE[1]	TX_PIN_FUNC1=14	Events are ignored while TXENABLE[1] is low.

7.3.13 Mute Function

The mute function quiets the output data in various conditions described below. The output transitions directly from valid sample to mid-scale (0) when muting or directly from mid-scale (0) to a valid sample when unmuting.

The DAC output is muted in the following conditions:

- SYS_EN=0
- MODE>0
- the device is in APP Sleep

Once the mute condition ceases, the mute is extended by a counter. The duration of the counter is a function of MXMODE, PFIR_EN, and PFIR_MODE. The mute extension makes sure that unknown or old samples stored in the PFIR, DES2X filter, or encoder signal paths are flushed out whenever the encoder is started up or resumed (and these samples never reach the DACs). The extension roughly scales based on the memory depth of the signal path.

The extension (in DAC cycles) is defined by this equation with three terms:

Total Mute Extension (in DAC cycles) = 512 * (2 + D_{PFIR_ENC} + D_{DES2X})

The value of the terms is defined in the following tables, and can be unique for each encoder channel *n*:

Table 7-71. Mute Extension for PFIR Operation in full rate mode (D_{PFIR_ENC})

Condition	Value of D_{PFIR_ENC}
PFIR_EN[*n*]&&PFIR_MODE==0	2

Table 7-71. Mute Extension for PFIR Operation in full rate mode (D_{PFIR_ENC}) (continued)

Condition	Value of D_{PFIR_ENC}
All other conditions	0

Table 7-72. Mute Extension for DES2X operation (D_{DES2X})

MXMODE	D_{DES2X}
DES2X or DES2XH	1
All others	0

This mute function is also triggered when the transmit enable signal for the DAC is low (transmit_enn) and IDLE_STATIC=0. No mute extension occurs due to exiting this condition.

7.3.13.1 Alarm Data Path Muting

Some alarm conditions cause the JESD204C transport layout output to mute. The transport layout output is muted when:

1. JESD is enabled, but the JESD link is down.
   a. The JESD interface is enabled (see JESD_M) and SYS_EN=1 & LINK_UP=0
2. The device is configured to not automatically recover from JESD link down alarms and a link down alarm is currently reported.
   a. JESD_LINK_DOWN_REC=0 & JESD_LINK_DOWN_ALM=1
3. The device is currently detecting a data integrity fault in an enabled lane.
   a. JESD_DI_MUTE_MASK=0 & an enabled lane has DI_FAULT=1
4. The device is configured to not automatically recover from data integrity alarms and an unmasked data integrity alarm is currently reported.
   a. JESD_DI_REC=0 & JESD_DI_MUTE_MASK=0 & JESD_DI_ALM=1
5. The chip is configured to mute on SYSREF alarms and a SYSREF alarm is currently reported.
   a. SYSREF_MUTE_MASK=0 & SYSREF_ALM=1

7.3.13.2 Transmit Enables

The two transmit enable pins TXEN0/1 or $\overline{\text{SYNC}}$ can optionally be configured via TX_PIN_FUNC and SYNCBPIN_FUNC registers to quickly mute and unmute the DAC outputs. Alternately, the TX_EN register can be used for this purpose.

Ramping down the input data prior to disabling transmission is recommended to avoid an abrupt change in output. When transmission is re-enabled, the output remains muted until new data is available to output. There are no glitches or old data output during this time.

7.4 Device Functional Modes

This section describes the functional modes of the device. Some of the features in this section have been discussed in further detail in Feature Description.

7.4.1 Power Modes

The part has a variety of power modes that are primarily controlled via the MODE register. This section outlines which subsystems are enabled in each mode. These power modes only apply when SYS_EN=1.

Table 7-73. Summary of Power Modes

	State of System Components			
Power Mode	**Application Layer (DSPs, Encoder)**	**Link Layer**	**PHY Layer**	**SYSREF Subsystem, LMFC, LEMC, NCO Accumulators, DAC Cores, Regulators**
Normal Operation	on	on	on	on
APP Sleep	off	on	on	on
Link Sleep	off	off	on	on
PHY Sleep	off	off	off	on
Power Down	off	off	off	off

Table 7-74. Power Modes

Power Mode	Description	Condition to Enter this Mode
Normal Operation	• All systems functional • Individual application layer components can be put to sleep using the APP_SLEEP0/APP_SLEEP1 feature.	MODE==0 && !SLEEP (pin)
APP Sleep	• Both DACs are muted according to IDLE_STATIC register • Most DSP and Encoder clocks are turned off. • SYSREF synchronization is maintained, so the LMFC/LEMC counters, trigger clock counter, and NCO accumulators continue to operate as configured. • DSP trigger events configured with TRIG_TYPE cannot be processed in this mode. (1)	MODE==1 || (MODE==0 && SLEEP (pin)
Link Sleep	Identical to APP Sleep, except the JESD link layer clocks are turned off (but LMFC/LEMC phase is maintained).	MODE=2
PHY Sleep	Identical to Link Sleep, except the JESD PHY layer is also turned off.	MODE=3
Power Down	• JESD, DSP, and Encoder subsystems are off (and held in reset). • LMFC/LEMC, trigger clock counter, and NCO accumulators are off (alignment to SYSREF is lost). • DACCLK and SYSREF receivers (and LDOs) are off • CPLL is off • Both DAC cores off and muted using the aging safe static code. • These subsystems remain functional (independent of MODE register): – SPI (including any sticky status bits) – Analog Test Bus (if enabled) – XOR test tree (if enabled)	MODE=7

(1) Avoid generating any DSP trigger events while the APP layer is asleep, or for 1000 DACCLK cycles before putting the device to sleep. Doing so can produce unpredictable behavior. When waking the APP layer, verify PWR_IDLE returns 1 before generating a trigger event. If this recommendation is not followed, the user can generate a trigger after the APP layer is fully awake to re-establish predictable NCO parameters.

Note

Regardless of the current power mode, if SYS_EN is low, various components are disabled. See SYS_EN for details.

Note

Regardless of the power mode, the link and PHY layers are powered down if JESD_M=0

Note

When transitioning from Normal Operation to any of the other modes in Table 7-74, the output mutes within 1000 DACCLK cycle.

The TXEN0/1 or $\overline{\text{SYNC}}$ pins can be assigned to place the part into APP_SLEEP (if the part is already in a deeper sleep state, this has no effect) when any of TX_PIN_FUNC0, TX_PIN_FUNC1 or SYNCB_PIN_FUNC are set to 4.

ADVANCE INFORMATION

8 Programming

The device contains two programming interfaces. The standard SPI interface to program the registers, while the PFIR coefficients can be optionally configured through the Fast Reconfiguration (FR) interface.

8.1 Using the Standard SPI Interface

The standard SPI interface is accessed using the following four pins: serial clock (SCLK), serial data in (SDI), serial data out (SDO), and serial interface chip-select ($\overline{SCS}$). Register access is enabled through the $\overline{SCS}$ pin.

8.1.1 $\overline{SCS}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

8.1.2 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

8.1.3 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data are shifted in MSB first and multi-byte registers are always in little-endian format (least significant byte stored at the lowest address). Setup and hold times with respect to the SCLK must be observed (see Switching Characteristics).

8.1.4 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

8.1.5 Serial Interface Protocol

As shown in Figure 8-1, each register access consists of 24 bits. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last eight bits are the data written to the addressed register. During read operations, the last eight bits on SDI are ignored and, during this time, the SDO outputs the data from the addressed register. Figure 8-1 shows the serial protocol details.

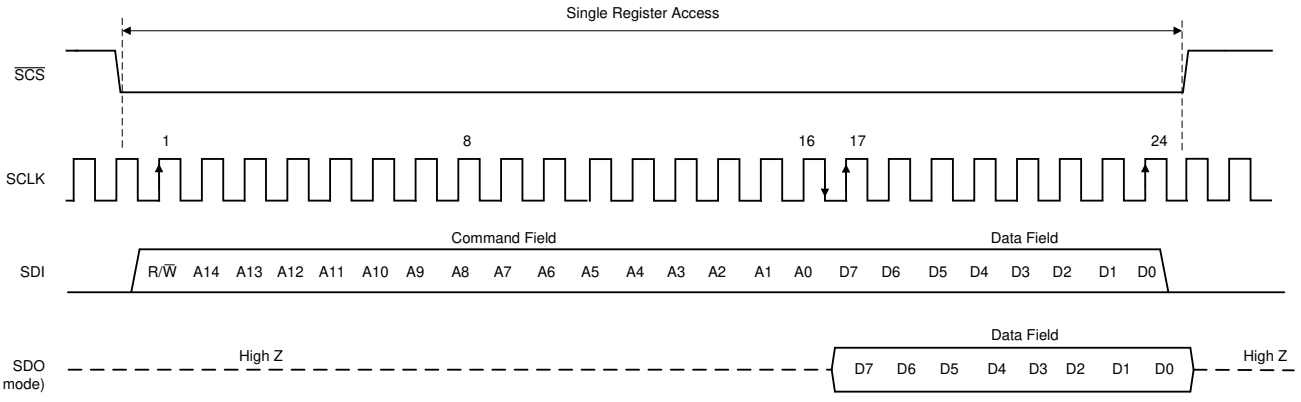


Figure 8-1. Serial Interface Protocol: Single Read and Write

ADVANCE INFORMATION

8.1.6 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{SCS}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8-bit transfer of the streaming transaction. The ADDR_ASC bit (register 000h, bits 5 and 2) controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_HOLD bit (see the SPI Configuration register). Figure 8-2 shows the streaming mode transaction details.

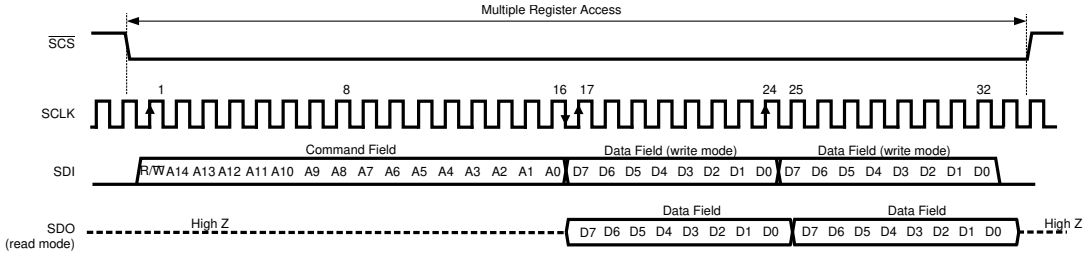


Figure 8-2. Serial Interface Protocol: Streaming Read and Write

8.2 Using the Fast Reconfiguration Interface

The Fast Reconfiguration (FR) interface provides fast write-only access to configure PFIR coefficients and NCO frequency and phase. The FR interface is similar to the SPI interface, but 4 bits are sent per clock cycle, and the external trigger pins are reused. The FR timing diagram is shown in Figure 8-3. It uses a R/W bit (always set to 0 to indicate a write for this device), a transaction sync bit FRS (always set to zero as transaction synchronization is not supported for this device), and 14-bits of address followed by some number of data bytes. The address is decremented after each data byte (consistent with little-endian). The interface is byte addressable and data is committed after each byte. The FR interface is takes 4-bits (one nibble) per clock. For multi-nibble fields, data is sent most-significant nibble first. When the transaction sync bit (FRS) is set, the synchronization event specified in the NCO_SYNC_SRC register field occurs at the rising edge of $\overline{FRCS}$. Transactions ended before the completion of the first data byte may not trigger the sync event.

ADVANCE INFORMATION

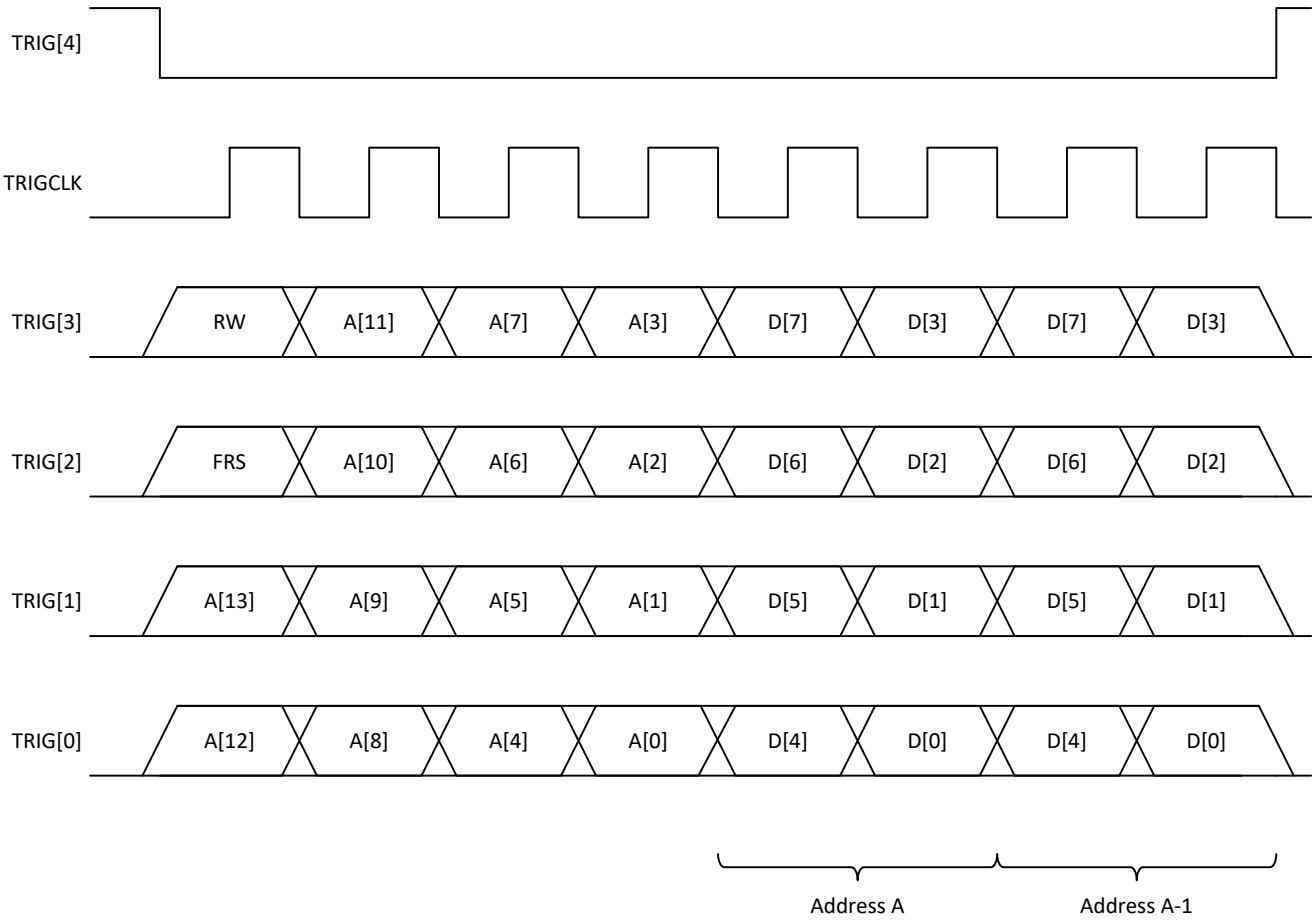


Figure 8-3. FR Interface Timing Diagram

The FRI registers for programming and swapping PFIR coefficients are listed in Table 8-1.

The following steps enable the FRI:

1. Program TRIGC_OUT_EN=0. This will tri-state the TRIGCLK output. TRIGC_OUT_EN should remain cleared until the FRI is later disabled.
2. Drive the TRIGCLK (FRI clock) to 0 or 1 from the host system (FRI controller). Drive TRIG[4] (chip-select-bar) to 1. Both inputs must not toggle until step 5.
3. Perform a SPI write to set FR_EN.
4. Wait at least 100 ns.
5. At this point you may begin an FRI transaction.

The following steps disable the FRI:

1. Make sure the FRI bus is idle with TRIG[4]=1. The TRIGCLK (FRI clock) can be idling low or high.
2. Perform a SPI write to clear FR_EN.
3. Wait at least 100ns before toggling TRIG[4] or TRIGCLK.
4. If you want to enable the TRIGCLK output, be sure the FRI controller has tri-stated TRIGCLK before setting TRIGC_OUT_EN.

Table 8-1. FRI Registers

Address	Name	Description
0x0303	FR_NCO_AR	**NCO Accumulator Reset** [7:4] Reserved [3:0] FR_NCO_AR: Provides write access to the NCO_AR register.

Table 8-1. FRI Registers (continued)

Address	Name	Description
0x0320-0x033F	FR_FREQ[0:3]	**Frequency for NCOn Accumulator** [63:0] FR_FREQ[n]: Provides write access to the FREQ registers.
0x0340-0x0347	FR_PHASE[0:3]	**Phase for NCOn Accumulator** [15:0] FR_PHASE[n]: Provides write access to the PHASE registers.
0x0348-0x034F	FR_AMP[0:3]	**DDS Amplitude** [15:0] FR_AMP[n]: Provides write access to the AMP registers.
0x0350-0x035F	FR_FREQS[0:3]	**32-bit Frequency for NCOn Accumulator** [31:0] FR_FREQS[n]: Provides write access to the upper 32-bits of each of the FREQ registers. This is provided to allow an FRI streaming transaction to update multiple frequencies in a single transaction when only 32-bit resolution is needed.
0x2810-0x2E0F	FR_PFIR_H[767:0]	**FR Programmable FIR Coefficients** (default: 0x0000) [15:0] FR_PFIR_H[n] When FR_EN=1, writes to this register set the values in PFIR_H **Note** Note: This register should only be changed when SYS_EN=0 or PFIR_PROG=1.
0x2E10	FR_PFIR_PROG	**FR Programmable FIR Program Enable** (default: 0x00) [7:1] RESERVED [0] FR_PFIR_PROG: When FR_EN=1, writes to this register set the value in PFIR_PROG

ADVANCE INFORMATION

8.3 Register Maps

8.3.1 Standard_SPI-3.1 Registers

Table 8-2 lists the memory-mapped registers for the Standard_SPI-3.1 registers. All register offset addresses not listed in Table 8-2 should be considered as reserved locations and the register contents should not be modified.

Table 8-2. STANDARD_SPI-3.1 Registers

Offset	Acronym	Register Name	Section
0x0	CONFIG_A		Section 8.3.1.1
0x2	DEVICE_CONFIG		Section 8.3.1.2
0x3	CHIP_TYPE		Section 8.3.1.3
0x4	CHIP_ID		Section 8.3.1.4
0x6	CHIP_VERSION		Section 8.3.1.5
0xC	VENDOR_ID		Section 8.3.1.6

Complex bit access types are encoded to fit into small table cells. Table 8-3 shows the codes that are used for access types in this section.

Table 8-3. Standard_SPI-3.1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1.1 CONFIG_A Register (Offset = 0x0) [Reset = 0x30]

CONFIG_A is shown in Table 8-4.

Return to the Summary Table.

Table 8-4. CONFIG_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0x0	Setting this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing and will always read zero. After writing this bit, the part may take up to 150ns to reset. During this time, do not perform any SPI transactions.
6	RESERVED	R	0x0	Reserved
5	ASCEND	R/W	0x1	Address streaming direction 0x0 = Address is decremented during streaming reads/writes 0x1 = Address is incremented during streaming reads/writes (default)
4	SDO_ACTIVE	R	0x1	Always reads 1.
3-0	RESERVED	R	0x0	Reserved

8.3.1.2 DEVICE_CONFIG Register (Offset = 0x2) [Reset = 0x00]

DEVICE_CONFIG is shown in Table 8-5.

Return to the Summary Table.

ADVANCE INFORMATION

Table 8-5. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	
2-0	MODE	R/W	0x0	Specifies the power state that applies when SYS_EN=1. 0x0 = Normal operation – All systems operational 0x1 = APP Sleep – JESD204C link maintained. 0x2 = Link Sleep – APP Sleep with JESD204C link layer powered down. 0x3 = PHY Sleep – APP Sleep with JESD204C link and physical layers powered down. 0x4 = RESERVED 0x5 = RESERVED 0x6 = RESERVED 0x7 = PowerDown – Full power down (lowest power, slowest resume).

8.3.1.3 CHIP_TYPE Register (Offset = 0x3) [Reset = 0x04]

CHIP_TYPE is shown in Table 8-6.

Return to the Summary Table.

Table 8-6. CHIP_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	CHIP_TYPE	R	0x4	Always returns 0x4, indicating that the part is a high-speed DAC.

8.3.1.4 CHIP_ID Register (Offset = 0x4) [Reset = 0x003C]

CHIP_ID is shown in Table 8-7.

Return to the Summary Table.

Table 8-7. CHIP_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CHIP_ID	R	0x3C	Indentifies chip as DAC39RF20 family

8.3.1.5 CHIP_VERSION Register (Offset = 0x6) [Reset = 0x01]

CHIP_VERSION is shown in Table 8-8.

Return to the Summary Table.

Table 8-8. CHIP_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHIP_VERSION	R	0x1	Version of device: 0x01 : DAC39RF20 PG1

8.3.1.6 VENDOR_ID Register (Offset = 0xC) [Reset = 0x0451]

VENDOR_ID is shown in Table 8-9.

Return to the Summary Table.

Table 8-9. VENDOR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_ID	R/W	0x451	Always returns 0x0451 (TI Vendor ID)

8.3.2 System Registers

Table 8-10 lists the memory-mapped registers for the System registers. All register offset addresses not listed in Table 8-10 should be considered as reserved locations and the register contents should not be modified.

Table 8-10. SYSTEM Registers

Offset	Acronym	Register Name	Section
0x20	SYS_EN		Section 8.3.2.1
0x21	FR_EN		Section 8.3.2.2
0x22	PWR_RAMP		Section 8.3.2.3
0x23	PWR_IDLE		Section 8.3.2.4
0x24	CMOS_BOOST		Section 8.3.2.5
0x25	TX_EN_SEL		Section 8.3.2.6
0x26	TX_EN		Section 8.3.2.7
0x27	TX_PIN_FUNC		Section 8.3.2.8
0x28	SYNCB_PIN_FUNC		Section 8.3.2.9
0x2A	APP_SLEEP0		Section 8.3.2.10
0x2B	APP_SLEEP1		Section 8.3.2.11
0x2C	APP_SLEEP0_EN		Section 8.3.2.12

Complex bit access types are encoded to fit into small table cells. Table 8-11 shows the codes that are used for access types in this section.

Table 8-11. System Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.2.1 SYS_EN Register (Offset = 0x20) [Reset = 0x00]

SYS_EN is shown in Table 8-12.

Return to the Summary Table.

Table 8-12. SYS_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	SYS_EN	R/W	0x0	When SYS_EN=0, all circuits operating from the DAC clock (with exception of the fuse controller) are held in reset. The clocks are gated off to save power. The LMFC/LEMC counter is also held in reset, so SYSREF will not align the LMFC/LEMC. Note: This register should only be changed from 0 to 1 when FUSE_DONE=1. Note: If CPLL_EN=1, this bit should not be set until CPLL_LOCKED=1. 0x0 = Disable System Operation 0x1 = Enable System Operation

8.3.2.2 FR_EN Register (Offset = 0x21) [Reset = 0x00]

FR_EN is shown in Table 8-13.

Return to the Summary Table.

Table 8-13. FR_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	FR_EN	R/W	0x0	The FRI utilizes the TRIG pins, making them unavailable for triggering DSPs. The user may use TX_PIN_FUNC or SYNCB_PIN_FUNC to assign other pins as trigger inputs. Note: The TRIGCLK input should be static and TRIG[4] should be high for 30ns before and after changes to FR_EN. Note: This register should only be changed when the FRI interface is idle. 0x0 = FRI is disabled. PFIR and NCO parameters are controlled by SPI. 0x1 = FRI is enabled. PFIR and NCO parameters are controlled by FRI.

8.3.2.3 PWR_RAMP Register (Offset = 0x22) [Reset = 0x00]

PWR_RAMP is shown in Table 8-14.

Return to the Summary Table.

Table 8-14. PWR_RAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	
1-0	PWR_RAMP	R/W	0x0	This register controls how the design ramps up power when digital components are enabled. Use this register to avoid large inrush current. Higher settings will reduce inrush current. The design will ramp up power as a result of any of these actions: 1) Setting SYS_EN=1 2) Adjusting MODE to a higher power state 3) Using pin to exit APP Sleep mode (see TX_PIN_FUNC / SYNCB_PIN_FUNC) 4)Taking components out of sleep mode via the APP_SLEEP0/1 functions. Maximum time to wave all power zones: 0: 4376 DACCLK cycles 1: 20256 DACCLK cycles 2: 252576 DACCLK cycles 3: 3969696 DACCLK cycles

8.3.2.4 PWR_IDLE Register (Offset = 0x23) [Reset = 0x0X]

PWR_IDLE is shown in Table 8-15.

Return to the Summary Table.

Table 8-15. PWR_IDLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	PWR_IDLE	R	X	This returns a 1 when the power controller is idle (no power zones are in the process of turning on or off). This bit can also be driven onto the ALARM pin. See ALARM_TSEL.

ADVANCE INFORMATION

8.3.2.5 CMOS_BOOST Register (Offset = 0x24) [Reset = 0x00]

CMOS_BOOST is shown in Table 8-16.

Return to the Summary Table.

Table 8-16. CMOS_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	
1	TRIGC_BOOST	R/W	0x0	Enables the boost feature for the TRIGCLK output. Only has an effect when TRIGCLK is configured as an output pin.
0	SDO_BOOST	R/W	0x0	Enables the boost feature for the SDO output.

8.3.2.6 TX_EN_SEL Register (Offset = 0x25) [Reset = 0x00]

TX_EN_SEL is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. TX_EN_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3	IDLE_STATIC	R/W	0x0	Selects the method that a DAC uses when transmission is disabled (via txenable or TX_EN) 0x0 = Transmission is disabled after DEM and dither using the Aging Safe Static Outputs. For some configurations and frequencies, this will produce more noise on the DAC output than a static mid-scale code would normally produce. However, this mode has the lowest latency from transmit enable to DAC output. 0x1 = Transmission is disabled by muting the input to DEM and dither to minimize the output noise. This increases the latency from transmit enable to DAC output (see Transmit Enable A/C Specs).
2-0	RESERVED	R	0x0	

8.3.2.7 TX_EN Register (Offset = 0x26) [Reset = 0x00]

TX_EN is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. TX_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	
1	TX_EN1	R/W	0x0	If low, DACB is muted according to IDLE_STATIC.
0	TX_EN0	R/W	0x0	If low, DACA is muted according to IDLE_STATIC.

8.3.2.8 TX_PIN_FUNC Register (Offset = 0x27) [Reset = 0x00]

TX_PIN_FUNC is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. TX_PIN_FUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TX_PIN_FUNC1	R/W	0x0	Defines the function of the TXENABLE[1] pin. These actions are applied when the pin is low. Note: These settings can be used with TRIG_TYPEx=4. They provide alternate pins to drive the trigger system, but do not affect the FRI interface (FRI interface always uses the physical TRIG pins). Behavior is undefined if multiple pins are configured as an alternate input for the same TRIG[x] pin. Note: This register should only be changed when SYS_EN=0. 0x0 = Pin is ignored (default) 0x1 = Mute DACA according to IDLE_STATIC value. Pin is active low. 0x2 = Mute DACB according to IDLE_STATIC value. Pin is active low. 0x3 = Mute DACA and DACB according to IDLE_STATIC value. Pin is active low. 0x4 = Sleep entire application layer accouring the APP_SLEEP. Pin is active low. 0x5 = Sleep entire application layer accouring the APP_SLEEP0. Pin is active low. 0x6 = Sleep entire application layer accouring the APP_SLEEP1. Pin is active low. 0x7 = Pin is apply DAC_SRC_ALT0 binding. Active low. 0x8 = Apply DAC_SRC_ALT1 binding. Pin is active low. 0x9 = Apply DAC_SRC_ALT0 and DAC_SRC_ALT1 bindings. Pin is active low. 0xA = Alternate input for TRIG[0]. Can be used with TRIG_TYPEx is set to 4. 0xB = Alternate input for TRIG[1]. Can be used with TRIG_TYPEx is set to 4. 0xC = Alternate input for TRIG[2]. Can be used with TRIG_TYPEx is set to 4. 0xD = RESERVED 0xE = Mask over-range events. Pin is active low. 0xF = RESERVED

Table 8-19. TX_PIN_FUNC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	TX_PIN_FUNC0	R/W	0x0	Defines the function of the TXENABLE[0] pin. These actions are applied when the pin is low. Note: These settings can be used with TRIG_TYPEx=4. They provide alternate pins to drive the trigger system, but do not affect the FRI interface (FRI interface always uses the physical TRIG pins). Behavior is undefined if multiple pins are configured as an alternate input for the same TRIG[x] pin. Note: This register should only be changed when SYS_EN=0. 0x0 = Pin is ignored (default) 0x1 = Mute DACA according to IDLE_STATIC value. Pin is active low. 0x2 = Mute DACB according to IDLE_STATIC value. Pin is active low. 0x3 = Mute DACA and DACB according to IDLE_STATIC value. Pin is active low. 0x4 = Sleep entire application layer accouring the APP_SLEEP. Pin is active low. 0x5 = Sleep entire application layer accouring the APP_SLEEP0. Pin is active low. 0x6 = Sleep entire application layer accouring the APP_SLEEP1. Pin is active low. 0x7 = Apply DAC_SRC_ALT0 binding. Pin is active low. 0x8 = Apply DAC_SRC_ALT1 binding. Pin is active low. 0x9 = Apply DAC_SRC_ALT0 and DAC_SRC_ALT1 bindings. Pin is active low. 0xA = Alternate input for TRIG[0]. Can be used with TRIG_TYPEx is set to 4. 0xB = Alternate input for TRIG[1]. Can be used with TRIG_TYPEx is set to 4. 0xC = Alternate input for TRIG[2]. Can be used with TRIG_TYPEx is set to 4. 0xD = RESERVED 0xE = Mask over-range events. Pin is active low. 0xF = RESERVED

8.3.2.9 SYNCB_PIN_FUNC Register (Offset = 0x28) [Reset = 0x00]

SYNCB_PIN_FUNC is shown in Table 8-20.

Return to the Summary Table.

Table 8-20. SYNCB_PIN_FUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	

Table 8-20. SYNCB_PIN_FUNC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	SYNCB_PIN_FUNC	R/W	0x0	Defines the function of the SYNCB pin when JENC=1 (64b/66b). When JENC=0 (8b/10b) this register has no effect (SYNCB is used by JESD interface). These actions are applied when the pin is low. Note: These settings can be used with TRIG_TYPEx=4. They provide alternate pins to drive the trigger system, but do not affect the FRI interface (FRI interface always uses the physical TRIG pins). Behavior is undefined if multiple pins are configured as an alternate input for the same TRIG[x] pin. If the JESD interface is unused, all DSPs are in a DDS mode and JESD_M=0. However, you must still set JENC=1 to allow the SYNCB pin to be used as a input signal. Note: This register should only be changed when SYS_EN=0. 0x0 = Pin is ignored (default) 0x1 = Mute DACA according to IDLE_STATIC value. Pin is active low. 0x2 = Mute DACB according to IDLE_STATIC value. Pin is active low. 0x3 = Mute DACA and DACB according to IDLE_STATIC value. Pin is active low. 0x4 = Sleep entire application layer accouring the APP_SLEEP. Pin is active low. 0x5 = Sleep entire application layer accouring the APP_SLEEP0. Pin is active low. 0x6 = Sleep entire application layer accouring the APP_SLEEP1. Pin is active low. 0x7 = Apply DAC_SRC_ALT0 binding. Pin is active low. 0x8 = Apply DAC_SRC_ALT1 binding. Pin is active low. 0x9 = Apply DAC_SRC_ALT0 and DAC_SRC_ALT1 bindings. Pin is active low. 0xA = Alternate input for TRIG[0]. Can be used with TRIG_TYPEx is set to 4. 0xB = Alternate input for TRIG[1]. Can be used with TRIG_TYPEx is set to 4. 0xC = Alternate input for TRIG[2]. Can be used with TRIG_TYPEx is set to 4. 0xD = RESERVED 0xE = Mask over-range events. Pin is active low. 0xF = RESERVED

ADVANCE INFORMATION

8.3.2.10 APP_SLEEP0 Register (Offset = 0x2A) [Reset = 0x00]

APP_SLEEP0 is shown in Table 8-21.

Return to the Summary Table.

Table 8-21. APP_SLEEP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	

Table 8-21. APP_SLEEP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DACB_SLEEP0	R/W	0x0	These bits control which components are put to sleep when a pin or register activates the APP_SLEEP0 function (see TX_PIN_FUNC, SYNCB_PIN_FUNC, APP_SLEEP0_EN). Note: When APP_SLEEP0/APP_SLEEP1 function is deactivated, components are re-enabled gradually to prevent power supply brownout. Note: When the MODE register is 1 or higher, the entire application layer is asleep, so this register has no effect. Note: When a PFIR is producing samples for a DSP input, the PFIR channel is asleep when the DSP channel is asleep. Note: When a PFIR is producing samples for an encoder, the PFIR channel is asleep when encoder is asleep: Note: When PFIR channel 0 is broadcasting to both encoders, the PFIR is asleep only when both encoders are asleep (See PFIR_BC). DACB is muted (according to IDLE_STATIC) and encoder 1 is asleep when the APP_SLEEP0 function is activated. When a DSP is asleep, it can still process trigger events if the MODE register is configured for normal operation.
4	DACA_SLEEP0	R/W	0x0	DACA is muted (according to IDLE_STATIC) and associated encoder is asleep when the APP_SLEEP0 function is activated. Note: If the APP_SLEEP0 and APP_SLEEP1 functions are both active at the same time, then components are asleep if either function requests it (logical OR).
3	DSP3_SLEEP0	R/W	0x0	DSP channel 3 is asleep when the APP_SLEEP0 function is activated.
2	DSP2_SLEEP0	R/W	0x0	DSP channel 2 is asleep when the APP_SLEEP0 function is activated.
1	DSP1_SLEEP0	R/W	0x0	DSP channel 1 is asleep when the APP_SLEEP0 function is activated.
0	DSP0_SLEEP0	R/W	0x0	DSP channel 0 is asleep when the APP_SLEEP0 function is activated.

8.3.2.11 APP_SLEEP1 Register (Offset = 0x2B) [Reset = 0x00]

APP_SLEEP1 is shown in Table 8-22.

Return to the Summary Table.

Table 8-22. APP_SLEEP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5	DACB_SLEEP1	R/W	0x0	DACB is muted (according to IDLE_STATIC) and associated encoder is asleep when the APP_SLEEP1 function is activated. See notes for APP_SLEEP0.
4	DACA_SLEEP1	R/W	0x0	DACA is muted (according to IDLE_STATIC) and encoder 0 is asleep when the APP_SLEEP1 function is activated.
3	DSP3_SLEEP1	R/W	0x0	DSP channel 3 is asleep when the APP_SLEEP1 function is activated.
2	DSP2_SLEEP1	R/W	0x0	DSP channel 2 is asleep when the APP_SLEEP1 function is activated.
1	DSP1_SLEEP1	R/W	0x0	DSP channel 1 is asleep when the APP_SLEEP1 function is activated.
0	DSP0_SLEEP1	R/W	0x0	DSP channel 0 is asleep when the APP_SLEEP1 function is activated.

8.3.2.12 APP_SLEEP0_EN Register (Offset = 0x2C) [Reset = 0x00]

APP_SLEEP0_EN is shown in Table 8-23.

Return to the Summary Table.

Table 8-23. APP_SLEEP0_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	APP_SLEEP0_EN	R/W	0x0	When set, components are put to sleep according to the APP_SLEEP0 register. Use this when you want fine-grained control of application sleep, but do not want to dedicate a pin to activate it. You may leave this register set and modify the APP_SLEEP0 register to sleep/wake components on the fly (while SYS_EN=1).

8.3.3 Trigger Registers

Table 8-24 lists the memory-mapped registers for the Trigger registers. All register offset addresses not listed in Table 8-24 should be considered as reserved locations and the register contents should not be modified.

Table 8-24. TRIGGER Registers

Offset	Acronym	Register Name	Section
0x40	TRIGC_DIV		Section 8.3.3.1
0x41	TRIGC_OUT_EN		Section 8.3.3.2
0x42	TRIG_TYPE		Section 8.3.3.3
0x44	TRIG_SPI		Section 8.3.3.4
0x45	TRIG_SEL		Section 8.3.3.5
0x4F	DSP_TRIG_DET		Section 8.3.3.6
0x50	FRS_R		Section 8.3.3.7

Complex bit access types are encoded to fit into small table cells. Table 8-25 shows the codes that are used for access types in this section.

Table 8-25. Trigger Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.3.3.1 TRIGC_DIV Register (Offset = 0x40) [Reset = 0x7F]

TRIGC_DIV is shown in Table 8-26.

Return to the Summary Table.

Table 8-26. TRIGC_DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	
6-0	TRIGC_DIV	R/W	0x7F	$F_{TRIGCLK} = F_{DACCLK} / 32 / (TRIGC\_DIV+1)$ Note: TRIGC_DIV should be programmed to keep the trigger clock frequency below 200 MHz.

8.3.3.2 TRIGC_OUT_EN Register (Offset = 0x41) [Reset = 0x00]

TRIGC_OUT_EN is shown in Table 8-27.

Return to the Summary Table.

Table 8-27. TRIGC_OUT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	

Table 8-27. TRIGC_OUT_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TRIGC_OUT_EN	R/W	0x0	The trigger clock is driven on the TRIGCLK output when SYS_EN = 1 . Note: At least one TRIG_TYPEn must be 4 for TRIGCLK to operate. Note: When FR_EN=1, TRIGC_OUT_EN is ignored and treated as if it is 0.

8.3.3.3 TRIG_TYPE Register (Offset = 0x42) [Reset = 0x0000]

TRIG_TYPE is shown in Table 8-28.

Return to the Summary Table.

Table 8-28. TRIG_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	
14-12	TRIG_TYPE3	R/W	0x0	TRIG_TYPEn chooses the type of trigger to use for DSPn. Each DSP channel can have a unique trigger type. See DSP Triggering for more information about which actions occur when a DSP is triggered. Some trigger types require the user to program TRIG_SELn to choose a trigger index for DSPn). Note: The JESD204C LSB bits still pass to the DUC input (or DDS Streaming function) even when they are being used for a trigger. This has a negligible impact on the DUC input. When DDS Streaming is used, only STREAM_MODEn=1 is supported when TRIG_TYPEn=3. Note: This register should only be changed when SYS_EN=0. 0x0 = SPI-immediate - A rising edge on TRIG_SPI[TRIG_SELn] will immediately trigger DSPn actions. 0x1 = SYSREF One-Shot A rising edge on TRIG_SPI[TRIG_SELn] will trigger DSPn actions on the next SYSREF rising edge. 0x2 = SYSREF Continuous - While TRIG_SPI[TRIG_SELn] is high, every SYSREF rising edge will trigger DSPn actions. 0x3 = JESD204C LSB - While TRIG_SPI[TRIG_SELn] is high, the LSb of JESD204C samples from stream 0 will trigger DSPn actions. To initiate a trigger event, the LSb must be low for 4 consecutive samples and then go high for 4 consecutive samples. This setting is compatible with DDS stream modes only if DDS amplitude streaming is disabled for DDS0 (see DSP_MODE and AMP_STREAM). 0x4 = A rising edge on TRIG[TRIG_SELn] will trigger DSPn actions. Not available when FR_EN is set to 1. 0x5 = If FRS is set, then DSPn is triggered by the rising edge of frcs_n. 0x6 = If FRS is set, then DSPn is triggered by the rising edge of trig_c that follows the rising edge of frcs_n (one-shot). 0x7 = RESERVED
11	RESERVED	R	0x0	
10-8	TRIG_TYPE2	R/W	0x0	See TRIG_TYPE3 description
7	RESERVED	R	0x0	
6-4	TRIG_TYPE1	R/W	0x0	See TRIG_TYPE3 description
3	RESERVED	R	0x0	
2-0	TRIG_TYPE0	R/W	0x0	See TRIG_TYPE3 description

8.3.3.4 TRIG_SPI Register (Offset = 0x44) [Reset = 0x00]

TRIG_SPI is shown in Table 8-29.

Return to the Summary Table.

ADVANCE INFORMATION

Table 8-29. TRIG_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	TRIG_SPI	R/W	0x0	These bits are used to trigger or enable trigger sources for DSP channels. The TRIG_TYPEn registers determines how TRIG_SPI is used. TRIG_SPI[TRIG_SELn] affects DSPn. See DSP Triggering. Note: These register bits are edge or level sensitive depending on the setting for TRIG_TYPE.

8.3.3.5 TRIG_SEL Register (Offset = 0x45) [Reset = 0x00]

TRIG_SEL is shown in Table 8-30.

Return to the Summary Table.

Table 8-30. TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	TRIG_SEL3	R/W	0x0	Determine which TRIG_SPI bit or which external trigger (TRIG) is bound to DSP channel 3
5-4	TRIG_SEL2	R/W	0x0	Determine which TRIG_SPI bit or which external trigger (TRIG) is bound to DSP channel 2
3-2	TRIG_SEL1	R/W	0x0	Determine which TRIG_SPI bit or which external trigger (TRIG) is bound to DSP channel 1
1-0	TRIG_SEL0	R/W	0x0	Determine which TRIG_SPI bit or which external trigger (TRIG) is bound to DSP channel 0

8.3.3.6 DSP_TRIG_DET Register (Offset = 0x4F) [Reset = 0x00]

DSP_TRIG_DET is shown in Table 8-31.

Return to the Summary Table.

Table 8-31. DSP_TRIG_DET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	DSP_TRIG_DET	R/W1C	0x0	This bit is set any time one or more DSPs receives a trigger event. Write 1 to clear.

8.3.3.7 FRS_R Register (Offset = 0x50) [Reset = 0xXX]

FRS_R is shown in Table 8-32.

Return to the Summary Table.

Table 8-32. FRS_R Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	Reserved
0	FRS_R	R	X	This provides readback for the value of FRS in the last FRI transaction

8.3.4 CPLL_AND_CLOCK Registers

Table 8-33 lists the memory-mapped registers for the CPLL_AND_CLOCK registers. All register offset addresses not listed in Table 8-33 should be considered as reserved locations and the register contents should not be modified.

Table 8-33. CPLL_AND_CLOCK Registers

Offset	Acronym	Register Name	Section
0x80	CLK_SLOW		Section 8.3.4.1
0x82	NOISEREDUCE_CLK		Section 8.3.4.2
0x84	DES_LOOP_EN		Section 8.3.4.3
0x85	DES_LOOP_BW		Section 8.3.4.4
0x8A	CPLL_EN		Section 8.3.4.5
0x8B	CPLL_MPY		Section 8.3.4.6
0x8F	CPLL_LOCKED		Section 8.3.4.7
0x98	CPLL_STATUS		Section 8.3.4.8
0x99	CPLL_STATUS2		Section 8.3.4.9

Complex bit access types are encoded to fit into small table cells. Table 8-34 shows the codes that are used for access types in this section.

Table 8-34. CPLL_AND_CLOCK Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.3.4.1 CLK_SLOW Register (Offset = 0x80) [Reset = 0x00]

CLK_SLOW is shown in Table 8-35.

Return to the Summary Table.

Table 8-35. CLK_SLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	CLK_SLOW	R/W	0x0	When the DEVCLK frequency is below 3GHz, set this bit.

8.3.4.2 NOISEREDUCE_CLK Register (Offset = 0x82) [Reset = 0x03]

NOISEREDUCE_CLK is shown in Table 8-36.

Return to the Summary Table.

ADVANCE INFORMATION

Table 8-36. NOISEREDUCE_CLK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	
1	NOISEREDUCE_CLKDIST_EN	R/W	0x1	Reduces noise on clock generator supply (VDDCLK08).
0	NOISEREDUCE_CLKGEN_EN	R/W	0x1	Reduces noise on clock distribution supply (AVDDCLK).

8.3.4.3 DES_LOOP_EN Register (Offset = 0x84) [Reset = 0x00]

DES_LOOP_EN is shown in Table 8-37.

Return to the Summary Table.

Table 8-37. DES_LOOP_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	DES_LOOP_EN1	R/W	0x0	DES_LOOP_EN1 enables the DES correction loop for DACB. This may reduce the amplitude of the FDAC-FOUT image in DES modes
0	DES_LOOP_EN0	R/W	0x0	DES_LOOP_EN0 enables the DES correction loop for DACA. This may reduce the amplitude of the FDAC-FOUT image in DES modes

8.3.4.4 DES_LOOP_BW Register (Offset = 0x85) [Reset = 0x00]

DES_LOOP_BW is shown in Table 8-38.

Return to the Summary Table.

Table 8-38. DES_LOOP_BW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	DES_LOOP_BW	R/W	0x0	Adjusts the bandwidth of the DES correction loop. Affects both DAC channels. The lowest value has the best stability, but higher noise.

8.3.4.5 CPLL_EN Register (Offset = 0x8A) [Reset = 0x00]

CPLL_EN is shown in Table 8-39.

Return to the Summary Table.

Table 8-39. CPLL_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	CPLL_EN	R/W	0x0	Enables the converter PLL when high.

8.3.4.6 CPLL_MPY Register (Offset = 0x8B) [Reset = 0x000A]

CPLL_MPY is shown in Table 8-40.

Return to the Summary Table.

Table 8-40. CPLL_MPY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	

Table 8-40. CPLL_MPY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CPLL_MPY	R/W	0xA	Specifies the PLL frequency multiplier for the PHY. See CPLL Control. Allowed values are from 8 to 99. $F_{DACCLK} = F_{REF} * CPLL\_MPY$

8.3.4.7 CPLL_LOCKED Register (Offset = 0x8F) [Reset = 0x0X]

CPLL_LOCKED is shown in Table 8-41.

Return to the Summary Table.

Table 8-41. CPLL_LOCKED Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	CPLL_LOCKED	R	X	This bit returns 1 if the CPLL is locked

8.3.4.8 CPLL_STATUS Register (Offset = 0x98) [Reset = 0x00]

CPLL_STATUS is shown in Table 8-42.

Return to the Summary Table.

Table 8-42. CPLL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	CPLL_LOCK_LOST	R/W1C	0x0	This bit is set whenever the LOCK signal is low. This bit is sticky (remains set even if the CPLL acquires lock). Write a 1 to clear. This is for debug purposes and allows the SPI to monitor if the CPLL loses lock even briefly.

8.3.4.9 CPLL_STATUS2 Register (Offset = 0x99) [Reset = 0xXX]

CPLL_STATUS2 is shown in Table 8-43.

Return to the Summary Table.

Table 8-43. CPLL_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5	CPLL_NO_LOCK	R	X	This indicates that the CPLL completed calibration, but was not able to atain or maintain a steady lock. This can also occur if lock is achieved, but then persistently lost (possibly due to a change in reference clock frequency).
4	CPLL_CORE_GAP	R	X	Returns a 1 if the CPLL detected a frequency gap between cores.
3	CPLL_REF_SLOW	R	X	Returns a 1 if the CPLL reference clock is too slow for the CPLL to lock. If this occurs, verify the programming of CPLL_MPY.
2	CPLL_REF_FAST	R	X	Returns a 1 if the CPLL reference clock is too fast for the CPLL to lock. If this occurs, verify the programming of CPLL_MPY.
1	CPLL_VCAL_DONE	R	X	Returns a 1 to indicate that the CPLL calibration is completed.
0	RESERVED	R	0x0	

8.3.5 SYSREF Registers

Table 8-44 lists the memory-mapped registers for the SYSREF registers. All register offset addresses not listed in Table 8-44 should be considered as reserved locations and the register contents should not be modified.

Table 8-44. SYSREF Registers

Offset	Acronym	Register Name	Section
0xA0	SYSREF_ALIGN		Section 8.3.5.1
0xA2	SYSREF_CALTRK		Section 8.3.5.2
0xA3	SYSREF_RX_EN		Section 8.3.5.3
0xA4	SYSREF_PROC_EN		Section 8.3.5.4
0xA5	SRCAL_CTRL		Section 8.3.5.5
0xB0	TADJ		Section 8.3.5.6
0xB3	TSYS		Section 8.3.5.7
0xC0	TADJ_CAL		Section 8.3.5.8
0xC3	TSYS_CAL		Section 8.3.5.9
0xDE	SRCAL_FREEZE		Section 8.3.5.10
0xDF	SRCAL_STAT		Section 8.3.5.11
0xFF	SYNC_STATUS		Section 8.3.5.12

Complex bit access types are encoded to fit into small table cells. Table 8-45 shows the codes that are used for access types in this section.

Table 8-45. SYSREF Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.3.5.1 SYSREF_ALIGN Register (Offset = 0xA0) [Reset = 0x00]

SYSREF_ALIGN is shown in Table 8-46.

Return to the Summary Table.

Table 8-46. SYSREF_ALIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	SYSREF_ALIGN_EN	R/W	0x0	If this bit is set, the chip realigns to each detected SYSREF edge. This affects both the external clock divider and all active internal clocks. If this bit is not set, the chip will not realign to any SYSREF edges, and the JESD204C link will not restart in response to any mis-aligned SYSREF edges.

8.3.5.2 SYSREF_CALTRK Register (Offset = 0xA2) [Reset = 0x74]

SYSREF_CALTRK is shown in Table 8-47.

Return to the Summary Table.

Table 8-47. SYSREF_CALTRK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SRCAL_AVG	R/W	0x1	Specifies the amount of averaging used for SYSREF Calibration. Larger values will increase calibration time and reduce the variance of the calibrated value. 0x0 = 4 accumulations 0x1 = 16 accumulations 0x2 = 64 accumulations 0x3 = 256 accumulations
5	SRTRK_EN	R/W	0x1	When set, tracking is allowed to run once calibration completes. When cleared, tracking is not run after calibration. This can be used to disable tracking both to measure the noise impact that tracking has and to avoid tracking causing problems if it doesn 't work correctly.
4	SRTRK_HYST_EN	R/W	0x1	When set, the low speed tracking accumulator must be within 2^{SRTRK_AVG+1} of its min or max value before tracking will make an adjustments. See Tracking.
3-2	SRTRK_AVG	R/W	0x1	Specifies the amount of averaging used for SYSREF Tracking. Larger values will decrease tracking rate and increase the likelihood that tracking will fail. 0x0 = 16 accumulations 0x1 = 64 accumulations 0x2 = 256 accumulations 0x3 = 1024 accumulations
1-0	SRTRK_STEP	R/W	0x0	Specifies the step size used for SYSREF Tracking. Larger values will increase the tracking rate and increase the likelihood that tracking will work but may also increase the delay changes that occur during tracking. 0x0 = 32 LSB steps for each change 0x1 = 64 LSB steps for each change 0x2 = 256 LSB steps for each change 0x3 = 1024 LSB steps for each change

ADVANCE INFORMATION

8.3.5.3 SYSREF_RX_EN Register (Offset = 0xA3) [Reset = 0x00]

SYSREF_RX_EN is shown in Table 8-48.

Return to the Summary Table.

Table 8-48. SYSREF_RX_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	SYSREF_RX_EN	R/W	0x0	Set this bit to enable the SYSREF receiver circuit. User should always clear SYSREF_PROC_EN before clearing this bit. Note: This bit should only be set if CPLL_EN=0.

8.3.5.4 SYSREF_PROC_EN Register (Offset = 0xA4) [Reset = 0x00]

SYSREF_PROC_EN is shown in Table 8-49.

Return to the Summary Table.

Table 8-49. SYSREF_PROC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved

Table 8-49. SYSREF_PROC_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYSREF_PROC_EN	R/W	0x0	When set, this bit enables the SYSREF processor. When this is enabled, the system receives and processes each new SYSREF edge. User should always set SYSREF_RX_EN before setting this bit. This bit is provided to allow the SYSREF receiver to stabilize before allowing the SYSREF to come to the digital.

8.3.5.5 SRCAL_CTRL Register (Offset = 0xA5) [Reset = 0x00]

SRCAL_CTRL is shown in Table 8-50.

Return to the Summary Table.

Table 8-50. SRCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	SRCAL_EN	R/W	0x0	When cleared, the internal SYSREF calibration and tracking engine is reset and SYSREF_CAL_DONE is cleared. Setting this bit allows SYSREF calibration and tracking to run.

8.3.5.6 TADJ Register (Offset = 0xB0) [Reset = 0x000000]

TADJ is shown in Table 8-51.

Return to the Summary Table.

Table 8-51. TADJ Register Field Descriptions

Bit	Field	Type	Reset	Description
23	CALCLK_INV	R/W	0x0	When set, inverts the clock input. Note: This register is only used when SRCAL_EN=0.
22-19	RESERVED	R	0x0	Reserved
18-0	TADJ	R/W	0x0	This defines the DEVCLK delay adjustment when SYSREF calibration is disabled (SRCAL_EN=0). See Timing Adjust Blocks for encoding description. Note: This register is only used when SRCAL_EN=0.

8.3.5.7 TSYS Register (Offset = 0xB3) [Reset = 0x040000]

TSYS is shown in Table 8-52.

Return to the Summary Table.

Table 8-52. TSYS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-19	RESERVED	R	0x0	Reserved
18-0	TSYS	R/W	0x00040000	This defines the SYSREF delay adjustment when SYSREF tracking is disabled (SRCAL_EN=0 or SRTRK_EN=0). See Timing Adjust Blocks for encoding description. Note: Note: This register should only be changed when SRCAL_EN=0 or SRTRK_EN=0.

8.3.5.8 TADJ_CAL Register (Offset = 0xC0) [Reset = 0xXXXXXX]

TADJ_CAL is shown in Table 8-53.

Return to the Summary Table.

Table 8-53. TADJ_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
23	CALCLK_INV_CAL	R	X	This register field should be the clock inversion calibration value, but due to a bug always returns zero. CALCLK_INV is working in the calibration routine.
22-19	RESERVED	R	0x0	Reserved
18-0	TADJ_CAL	R	X	This returns a snapshot of the CLK delay adjustment produced by SYSREF calibration.. Note: This register is is only valid when SRCAL_EN=1. Note: This register should only be read when SRCAL_FREEZE=1 or SYSREF_CAL_DONE=1.

8.3.5.9 TSYS_CAL Register (Offset = 0xC3) [Reset = 0x0XXXXX]

TSYS_CAL is shown in Table 8-54.

Return to the Summary Table.

Table 8-54. TSYS_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
23-19	RESERVED	R	0x0	Reserved
18-0	TSYS_CAL	R	X	This returns a snapshot of the SYSREF delay adjustment produced by SYSREF tracking. Note: This register is only valid when SRCAL_EN=1 and SRTRK_EN=1. Note: This register should only be read when SRCAL_FREEZE=1.

8.3.5.10 SRCAL_FREEZE Register (Offset = 0xDE) [Reset = 0x00]

SRCAL_FREEZE is shown in Table 8-55.

Return to the Summary Table.

Table 8-55. SRCAL_FREEZE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	SRCAL_FREEZE	R/W	0x0	When set, the TADJ_CAL and TSYS_CAL will freeze at their current values so they can be read. The calibration and tracking algorithm will continue to operate. User must wait at least 24 SYSREF periods after setting this bit before attempting to read TADJ_CAL or TSYS_CAL. When clearing this bit, it must remain low for more than 8 SYSREF periods to ensure data will be updated. This register is only useful when SRCAL_EN=1. Note: The frozen values of TADJ_CAL and TSYS_CAL are not upset immune.

8.3.5.11 SRCAL_STAT Register (Offset = 0xDF) [Reset = 0x0X]

SRCAL_STAT is shown in Table 8-56.

Return to the Summary Table.

Table 8-56. SRCAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved

Table 8-56. SRCAL_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SYSREF_ALIGNMENT	R	X	When this value is high, the clock is high when SYSREF rises.The value returned here is an averaged over 8*SRCAL_AVG cycles. When the CPLL is in use, the DEVCLK SYSREF samplers are used. Otherwise, the DACCLK SYSREF samples are used. Note: The value in this register is undefined when SYSREF_WIN_EN=1.
2	SYSREF_CAL_FAIL	R	X	Set if the SYSREF calibration process fails to find alignment. This bit is cleared any time (SYSREF_RX_EN = 0 AND SRCAL_EN = 0.
1	SYSREF_TRACK_FAIL	R	X	Set if SYSREF tracking runs out of delay range while tracking the window. Tracking attempts to continue running when this occurs but it may not be able to maintain the SYSREF sampling window. The user should rerun calibration when this occurs. This bit is cleared any time SYSREF_RX_EN = 0 and SRCAL_EN = 0.
0	SYSREF_CAL_DONE	R	X	Set when SYSREF calibration completes successfully. This bit is cleared any time SYSREF_RX_EN = 0 and SRCAL_EN = 0.

ADVANCE INFORMATION

8.3.5.12 SYNC_STATUS Register (Offset = 0xFF) [Reset = 0xXX]

SYNC_STATUS is shown in Table 8-57.

Return to the Summary Table.

Table 8-57. SYNC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	
4	DIV_REALIGNED	R/W1C	X	This bit is set any time the divide-by-16 clock divider is realigned to SYSREF. This bit is primarily for debug purposes as CLK_REALIGNED is more appropriate for customer use. Write a 1 to clear this bit.
3	CLK_REALIGNED	R/W1C	X	This bit is set any time an active SYSREF-associated clock divider is realigned to a SYSREF edge. This bit is useful to confirm the internally sampled SYSREF signal has a correct and stable period. Write a 1 to clear this bit.
2	CLK_ALIGNED	R	X	Indicates if the last SYSREF pulse was consistent with all active SYSREF-associated clock dividers (and the dividers required no adjustment) (1=consistent, 0=not consistent). The part may require up to two SYSREF pulses (both consistent with the clock dividers) to set this bit. This bit is read-only (cannot be cleared via SPI). This bit reports alignment status regardless of the state of SYSREF_ALIGN_EN.
1	RESERVED	R	0x0	
0	SYSREF_DET	R/W1C	X	This bit is set when a SYSREF is detected. Write a 1 to clear the bit and allow it to be re-detected.

8.3.6 JESD204C Registers

Table 8-58 lists the memory-mapped registers for the JESD204C registers. All register offset addresses not listed in Table 8-58 should be considered as reserved locations and the register contents should not be modified.

Table 8-58. JESD204C Registers

Offset	Acronym	Register Name	Section
0x101	JMODE		Section 8.3.6.1
0x102	JESD_M		Section 8.3.6.2
0x103	JCTRL		Section 8.3.6.3
0x104	SHMODE		Section 8.3.6.4
0x105	KM1		Section 8.3.6.5
0x106	RBD		Section 8.3.6.6
0x107	JESD_STATUS		Section 8.3.6.7
0x108	REFDIV		Section 8.3.6.8
0x10A	MPY		Section 8.3.6.9
0x10B	RATE		Section 8.3.6.10

Complex bit access types are encoded to fit into small table cells. Table 8-59 shows the codes that are used for access types in this section.

Table 8-59. JESD204C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
R-1	R -1	Read Returns 1s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.3.6.1 JMODE Register (Offset = 0x101) [Reset = 0x00]

JMODE is shown in Table 8-60.

Return to the Summary Table.

Table 8-60. JMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-0	JMODE	R/W	0x0	Specifies the JMODE

8.3.6.2 JESD_M Register (Offset = 0x102) [Reset = 0x01]

JESD_M is shown in Table 8-61.

Return to the Summary Table.

Table 8-61. JESD_M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	JESD_M	R/W	0x1	Specify the number of sample streams (JESD204C converters) to enable (JESD204C M parameter). The number of enabled streams must be appropriate based on the number of DAC or DSP channels that are configured to receive samples from the JESD interface (see DSP_MODE, MXMODE, DAC_SRC, DSP_L). When JESD_M=0, the JESD interface will not be enabled when SYS_EN is set (e.g. if all DSP channels do not need input samples). DSP_MODE = Bypass mode (all DSPs disabled), JESD_M must be 1 or 2. Use Use DAC_SRC to bind DAC channels to either input stream 0 or 1. DSP_MODE = any DSPs enabled, JESD_M must be 0, 1, 2, 4, 6, 8. Enable 2 sample streams for each DSP channel that requires samples (see DSP_MODE). Use JESD_M=0 to disable the JESD interface if no DSPs require input samples. Streams 0 and 1 supply DSP channel 0. Streams 2 and 3 supply DSP channel 1. Streams 4 and 5 supply DSP channel 2. Streams 6 and 7 supply DSP channel 3. Note 1: JESD_M should not exceed the Mx parameter associated with the selected JMODE. See Supported Modes for the Mx value associated with each JMODE. The number of lanes enabled (L) is computed as L = ceiling(M/Mx*Lx). Using JESD_M=1 is only legal in DSP mode if all enabled DSPs are using a non-JESD mode (e.g. DDS SPI or DDS Vector Mode). The single sample stream can be used for a trigger source (TRIG_TYPEn=3, TRIG_SELn=0). When triggering in this way, only JMODE 3 thru 7 are supported, and LT must be 32, 64, 128, or 256 (see DSP_L).

8.3.6.3 JCTRL Register (Offset = 0x103) [Reset = 0x03]

JCTRL is shown in Table 8-62.

Return to the Summary Table.

Table 8-62. JCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	
6	TI_MODE	R/W	0x0	0x0 = JESD204C standard mode (default) 0x1 = Special TI mode (set this if using TI transmitter IP).
5	SUBCLASS	R/W	0x0	Specify how the elastic buffer is released: 0x0 = Subclass 0 operation (default). Release the elastic buffer immediately once all lanes have starting writing to the buffer. 0x1 = Subclass 1 operation. Release the elastic buffer on a release opportunity defined by the LMFC/LEMC and RBD.
4	JENC	R/W	0x0	0x0 = Use 8b/10b link layer 0x1 = Use 64b/66b link layer
3-2	RESERVED	R	0x0	
1	SFORMAT	R/W	0x1	Input sample format for JESD204C samples. If any DSP is configured in DSP-Stream mode, you must use SFORMAT=1. 0x0 = Offset binary 0x1 = Signed 2's complement (default)

Table 8-62. JCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SCR	R/W	0x1	The 8b/10b scrambler is recommended to improve spurious noise and ensure that certain sample payloads cannot prevent the JESD204C receiver from detecting incorrect code-group or lane alignment. This register has no effect on 64b/66b modes (which are always scrambled). 0x0 = 8b/10b Scrambler disabled 0x1 = 8b/10b Scrambler enabled (default)

8.3.6.4 SHMODE Register (Offset = 0x104) [Reset = 0x00]

SHMODE is shown in Table 8-63.

Return to the Summary Table.

Table 8-63. SHMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	
1-0	SHMODE	R/W	0x0	Select the mode for the 64b/66b sync word (32 bits of data per multi-block). This only applies when JENC=1 (64b/66b mode). Note: This device does not support any JESD204C command features. All command fields are ignored by the receiver. 0x0 = Enable CRC-12 checking (JESD204C Table 41) (default setting) 0x1 = RESERVED (for CRC-3, which is not supported) 0x2 = Enable FEC (JESD204C Table 45) 0x3 = RESERVED (for standalone command channel, which is not supported)

8.3.6.5 KM1 Register (Offset = 0x105) [Reset = 0x3F]

KM1 is shown in Table 8-64.

Return to the Summary Table.

Table 8-64. KM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KM1	R/W	0x3F	K is the number of frames per multiframe, and K-1 shall be programmed here when using the 8b/10b link layer (see JENC). Depending on the JMODE setting, there are constraints on the legal values of K. Programming an illegal value for K will cause the link to malfunction. The default value is KM1=31, which corresponds to K=32. Note: For modes using the 64b/66b link layer, the KM1 register is ignored. The effective value of K is 256*E/F.

8.3.6.6 RBD Register (Offset = 0x106) [Reset = 0x80]

RBD is shown in Table 8-65.

Return to the Summary Table.

Table 8-65. RBD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	

ADVANCE INFORMATION

Table 8-65. RBD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	RBD	R/W	0x0	This register shifts the elastic buffer release opportunities. Increasing RBD by 1 delays the release opportunities by 8 bytes (octets). For 8b/10b modes, the legal RBD range is 0 to K*F/8-1. For 64b/66b modes, the legal RBD range is 0 to 32*E-1.

8.3.6.7 JESD_STATUS Register (Offset = 0x107) [Reset = 0xXX]

JESD_STATUS is shown in Table 8-66.

Return to the Summary Table.

Table 8-66. JESD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EB_ERR	W1C	X	Elastic buffer experienced underflow/overflow.
6	LINK_UP	R	X	When set, indicates that the JESD204C link is up (elastic buffer released).
5	JSYNC_STATE	R	X	Returns the state of the JESD204C $\overline{\text{SYNC}}$ signal. 0 = 0b0 = $\overline{\text{SYNC}}$ asserted 1 = 0b1 = $\overline{\text{SYNC}}$ de-asserted
4	RESERVED	R	X	
3	JESD_ALIGNED	R	X	Indicates that the LMFC/LEMC has been aligned by SYSREF and another SYSREF pulse has confirmed the alignment. This bit is read-only (cannot be cleared via SPI). After SYSREF_ALIGN_EN and SYS_EN are set, the part may require up to 15 SYSREF pulses to achieve alignment and set this bit.
2	PLL_LOCKED	R	X	When high, indicates that all enabled PHY PLLs are locked.
1-0	RESERVED	R	X	

8.3.6.8 REFDIV Register (Offset = 0x108) [Reset = 0x0030]

REFDIV is shown in Table 8-67.

Return to the Summary Table.

Table 8-67. REFDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	
7-0	REFDIV	R/W	0x30	Specifies the frequency divisor to generate the PHY PLL reference clock (FREF) from the DAC clock (F_{DACCLK}). The following values are legal: 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, 32, 40, 48, 64, 80, 96 and 128. All other values are reserved and produce undefined behavior. See PLL Control.

8.3.6.9 MPY Register (Offset = 0x10A) [Reset = 0x0A]

MPY is shown in Table 8-68.

Return to the Summary Table.

ADVANCE INFORMATION

Table 8-68. MPY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MPY	R/W	0xA	Specifies the PLL frequency multiplier for the PHY. See PLL Control. The following values are legal for this design: 8 (0x8) = 8x 10 (0xA) = 10x 16 (0x10) = 16x 20 (0x14) = 20x 33 (0x21) = 33x 40 (0x28) = 40x 66 (0x42) = 66x 99 (0x63) = 99x

8.3.6.10 RATE Register (Offset = 0x10B) [Reset = 0x00]

RATE is shown in Table 8-69.

Return to the Summary Table.

Table 8-69. RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	
2-0	RATE	R/W	0x0	Controls the frequency multiplier from the Serdes VCO frequency F_{VCO} to the Serdes bit rate F_{BIT}. Affects all lanes. See Serdes PLL section. 0x0 = 2x 0x1 = 1x 0x2 = 0.5x 0x3 = 0.25x 0x4 = 0.125x 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

8.3.7 JESD204C_Advanced Registers

Table 8-70 lists the memory-mapped registers for the JESD204C_Advanced registers. All register offset addresses not listed in Table 8-70 should be considered as reserved locations and the register contents should not be modified.

Table 8-70. JESD204C_ADVANCED Registers

Offset	Acronym	Register Name	Section
0x120	JSYNC_N		Section 8.3.7.1
0x121	JTEST		Section 8.3.7.2
0x122	JEXTRA		Section 8.3.7.3
0x124	JTIMER		Section 8.3.7.4
0x125	JESD_RST		Section 8.3.7.5
0x127	SYNC_EPW		Section 8.3.7.6
0x128	DI_TH		Section 8.3.7.7
0x12C	LANE_ARSTAT		Section 8.3.7.8
0x12E	LANE_INV		Section 8.3.7.9
0x130	LANE_SEL_0		Section 8.3.7.10
0x131	LANE_SEL_1		Section 8.3.7.11
0x132	LANE_SEL_2		Section 8.3.7.12
0x133	LANE_SEL_3		Section 8.3.7.13
0x134	LANE_SEL_4		Section 8.3.7.14
0x135	LANE_SEL_5		Section 8.3.7.15
0x136	LANE_SEL_6		Section 8.3.7.16
0x137	LANE_SEL_7		Section 8.3.7.17
0x138	LANE_SEL_8		Section 8.3.7.18
0x139	LANE_SEL_9		Section 8.3.7.19
0x13A	LANE_SEL_10		Section 8.3.7.20
0x13B	LANE_SEL_11		Section 8.3.7.21
0x13C	LANE_SEL_12		Section 8.3.7.22
0x13D	LANE_SEL_13		Section 8.3.7.23
0x13E	LANE_SEL_14		Section 8.3.7.24
0x13F	LANE_SEL_15		Section 8.3.7.25
0x140	LANE_ARR_0		Section 8.3.7.26
0x141	LANE_ARR_1		Section 8.3.7.27
0x142	LANE_ARR_2		Section 8.3.7.28
0x143	LANE_ARR_3		Section 8.3.7.29
0x144	LANE_ARR_4		Section 8.3.7.30
0x145	LANE_ARR_5		Section 8.3.7.31
0x146	LANE_ARR_6		Section 8.3.7.32
0x147	LANE_ARR_7		Section 8.3.7.33
0x148	LANE_ARR_8		Section 8.3.7.34
0x149	LANE_ARR_9		Section 8.3.7.35
0x14A	LANE_ARR_10		Section 8.3.7.36
0x14B	LANE_ARR_11		Section 8.3.7.37
0x14C	LANE_ARR_12		Section 8.3.7.38
0x14D	LANE_ARR_13		Section 8.3.7.39
0x14E	LANE_ARR_14		Section 8.3.7.40
0x14F	LANE_ARR_15		Section 8.3.7.41

ADVANCE INFORMATION

Table 8-70. JESD204C_ADVANCED Registers (continued)

Offset	Acronym	Register Name	Section
0x150	LANE_STATUS_0		Section 8.3.7.42
0x151	LANE_STATUS_1		Section 8.3.7.43
0x152	LANE_STATUS_2		Section 8.3.7.44
0x153	LANE_STATUS_3		Section 8.3.7.45
0x154	LANE_STATUS_4		Section 8.3.7.46
0x155	LANE_STATUS_5		Section 8.3.7.47
0x156	LANE_STATUS_6		Section 8.3.7.48
0x157	LANE_STATUS_7		Section 8.3.7.49
0x158	LANE_STATUS_8		Section 8.3.7.50
0x159	LANE_STATUS_9		Section 8.3.7.51
0x15A	LANE_STATUS_10		Section 8.3.7.52
0x15B	LANE_STATUS_11		Section 8.3.7.53
0x15C	LANE_STATUS_12		Section 8.3.7.54
0x15D	LANE_STATUS_13		Section 8.3.7.55
0x15E	LANE_STATUS_14		Section 8.3.7.56
0x15F	LANE_STATUS_15		Section 8.3.7.57
0x160	LANE_ERROR_0		Section 8.3.7.58
0x161	LANE_ERROR_1		Section 8.3.7.59
0x162	LANE_ERROR_2		Section 8.3.7.60
0x163	LANE_ERROR_3		Section 8.3.7.61
0x164	LANE_ERROR_4		Section 8.3.7.62
0x165	LANE_ERROR_5		Section 8.3.7.63
0x166	LANE_ERROR_6		Section 8.3.7.64
0x167	LANE_ERROR_7		Section 8.3.7.65
0x168	LANE_ERROR_8		Section 8.3.7.66
0x169	LANE_ERROR_9		Section 8.3.7.67
0x16A	LANE_ERROR_10		Section 8.3.7.68
0x16B	LANE_ERROR_11		Section 8.3.7.69
0x16C	LANE_ERROR_12		Section 8.3.7.70
0x16D	LANE_ERROR_13		Section 8.3.7.71
0x16E	LANE_ERROR_14		Section 8.3.7.72
0x16F	LANE_ERROR_15		Section 8.3.7.73
0x170	FIFO_STATUS_0		Section 8.3.7.74
0x171	FIFO_STATUS_1		Section 8.3.7.75
0x172	FIFO_STATUS_2		Section 8.3.7.76
0x173	FIFO_STATUS_3		Section 8.3.7.77
0x174	FIFO_STATUS_4		Section 8.3.7.78
0x175	FIFO_STATUS_5		Section 8.3.7.79
0x176	FIFO_STATUS_6		Section 8.3.7.80
0x177	FIFO_STATUS_7		Section 8.3.7.81
0x178	FIFO_STATUS_8		Section 8.3.7.82
0x179	FIFO_STATUS_9		Section 8.3.7.83
0x17A	FIFO_STATUS_10		Section 8.3.7.84
0x17B	FIFO_STATUS_11		Section 8.3.7.85
0x17C	FIFO_STATUS_12		Section 8.3.7.86

ADVANCE INFORMATION

Table 8-70. JESD204C_ADVANCED Registers (continued)

Offset	Acronym	Register Name	Section
0x17D	FIFO_STATUS_13		Section 8.3.7.87
0x17E	FIFO_STATUS_14		Section 8.3.7.88
0x17F	FIFO_STATUS_15		Section 8.3.7.89
0x18A	JCAP_ARM		Section 8.3.7.90
0x18B	JCAP_MODE		Section 8.3.7.91
0x18C	JCAP_OFFSET		Section 8.3.7.92
0x18E	JCAP_PAGE		Section 8.3.7.93
0x18F	JCAP_STATUS		Section 8.3.7.94
0x190	JCAP		Section 8.3.7.95
0x1A0	LEC_CTRL		Section 8.3.7.96
0x1B0	LEC_CNT_0		Section 8.3.7.97
0x1B1	LEC_CNT_1		Section 8.3.7.98
0x1B2	LEC_CNT_2		Section 8.3.7.99
0x1B3	LEC_CNT_3		Section 8.3.7.100
0x1B4	LEC_CNT_4		Section 8.3.7.101
0x1B5	LEC_CNT_5		Section 8.3.7.102
0x1B6	LEC_CNT_6		Section 8.3.7.103
0x1B7	LEC_CNT_7		Section 8.3.7.104
0x1B8	LEC_CNT_8		Section 8.3.7.105
0x1B9	LEC_CNT_9		Section 8.3.7.106
0x1BA	LEC_CNT_10		Section 8.3.7.107
0x1BB	LEC_CNT_11		Section 8.3.7.108
0x1BC	LEC_CNT_12		Section 8.3.7.109
0x1BD	LEC_CNT_13		Section 8.3.7.110
0x1BE	LEC_CNT_14		Section 8.3.7.111
0x1BF	LEC_CNT_15		Section 8.3.7.112

Complex bit access types are encoded to fit into small table cells. Table 8-71 shows the codes that are used for access types in this section.

Table 8-71. JESD204C_Advanced Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.3.7.1 JSYNC_N Register (Offset = 0x120) [Reset = 0x01]

JSYNC_N is shown in Table 8-72.

Return to the Summary Table.

Table 8-72. JSYNC_N Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	JSYNC_N	R/W	0x1	Set this bit to 0 to manually assert the SYNC~ signal. For normal operation, leave this bit set to 1.

8.3.7.2 JTEST Register (Offset = 0x121) [Reset = 0x00]

JTEST is shown in Table 8-73.

Return to the Summary Table.

Table 8-73. JTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	
4-0	JTEST	R/W	0x0	Sets PRBS mode. 0x5 and higher are RESERVED. See BER_EN. 0x0 = Test mode disabled (normal operation) 0x1 = PRBS7 0x2 = PRBS9 0x3 = PRBS15 0x4 = PRBS31

8.3.7.3 JEXTRA Register (Offset = 0x122) [Reset = 0x0000]

JEXTRA is shown in Table 8-74.

Return to the Summary Table.

Table 8-74. JEXTRA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	EXTRA_LANE	R/W	0x0	Program JEXTRA to enable extra logical lanes (even if the selected JMODE does not utilized the lanes). EXTRA_LANE[n] enables lane n (n=1 to 15). This register enables the link layers. To also enable the PHY for the extra lanes, set EXTRA_PHY=1. Note: The bit-rate and mode of the extra lanes are set by JMODE and JTEST registers.
0	EXTRA_PHY	R/W	0x0	0x0 = Only the link layers for extra lanes are enabled. Use this mode to evaluate the switching noise from the extra lanes. The PHY associated with each extra lane is not forced on. To provide input data to the extra lanes, it may be useful to use LANE_SELn to bind the extra logical lanes to PHY lanes that are bound to primary active lanes (logical lanes 0 to L-1) 0x1 = The PHY layer for the extra lanes are also enabled. Use this mode to receive data from extra physical lanes. This should be done if you want to run BER testing on more lanes than JMODE enables, or run other PHY tasks on those lanes (eye scan, etc.)

8.3.7.4 JTIMER Register (Offset = 0x124) [Reset = 0x00]

JTIMER is shown in Table 8-75.

Return to the Summary Table.

ADVANCE INFORMATION

Table 8-75. JTIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
7	JTPLL	R/W	0x0	If this bit is set, the PHY PLL, bias, reference divider, and receiver analog is also reset when the watchdog timer expires.If this bit is 0, only the PHY receiver digital logic is reset.
6	RESERVED	R	0x0	
5-4	JTR	R/W	0x0	This register determines how much the watchdog counter is decremented when the link is up and DI_FAULT is not set. See Watchdog Timer (JTIMER) for full details. 0x0 = 1 0x1 = 2 0x2 = 8 0x3 = 16
3	RESERVED	R	0x0	
2-0	JTT	R/W	0x0	JESD204C watchdog counter threshold. When the watchdog counter reaches the threshold defined by JTT, the PHY layer is reset (including the PHY PLL(s) if JTPLL=1) and the watchdog timer is reset. Larger values of JTT cause the watchdog timer to take longer to intervene. See Watchdog Timer (JTIMER) for full details. Note: The watchdog may not detect link up events shorter than 2^{11} (2048) DACCLK cycles. 0x0 = Watchdog timer disabled 0x1 = 2^{17} 0x2 = 2^{19} 0x3 = 2^{21} 0x4 = 2^{23} 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

8.3.7.5 JESD_RST Register (Offset = 0x125) [Reset = 0x00]

JESD_RST is shown in Table 8-76.

Return to the Summary Table.

Table 8-76. JESD_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	JESD_RST	R/W	0x0	When set, this bit holds the digital portion of the JESD circuitry in reset but does not affect the PHY.

8.3.7.6 SYNC_EPW Register (Offset = 0x127) [Reset = 0x00]

SYNC_EPW is shown in Table 8-77.

Return to the Summary Table.

Table 8-77. SYNC_EPW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	
2-0	SYNC_EPW	R/W	0x0	Specifies the pulse width of $\overline{\text{SYNC}}$ that is used for reporting errors to the transmitter. When an error is detected that does not require link resynchronization, $\overline{\text{SYNC}}$ is asserted for SYNC_EPW link clock cycles (equal to 8 *SYNC_EPW character durations). To disable error reporting over SYNC~, set SYNC_EPW=0. The legal range for SYNC_EPW is 0 to 4. The reported errors are listed in Link Error Reports.

8.3.7.7 DI_TH Register (Offset = 0x128) [Reset = 0x00]

DI_TH is shown in Table 8-78.

Return to the Summary Table.

Table 8-78. DI_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-2	DI_ERR_REC	R/W	0x0	Specify how many contiguous, error-free multiblocks must be received to reset the Data Integrity error counter (and un-trigger the Data Integrity alarm if triggered). 0x0 = 1 multiblock 0x1 = 4 multiblocks 0x2 = 16 multiblocks 0x3 = 64 multiblocks
1-0	DI_ERR_TH	R/W	0x0	Specify how many multi-blocks must have Data Integrity errors to trigger the Data Integrity alarm. The receiver counts each error, but if a run of error-free multi-blocks occurs (as specified by DI_ERR_REC), the error counter resets. 0x0 = 1 multiblock 0x1 = 2 multiblocks 0x2 = 4 multiblocks 0x3 = 8 multiblocks

8.3.7.8 LANE_ARSTAT Register (Offset = 0x12C) [Reset = 0xXX]

LANE_ARSTAT is shown in Table 8-79.

Return to the Summary Table.

Table 8-79. LANE_ARSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	LANE_ARR_RDY	W1C	X	This bit is set when lane arrival times are captured and available for read in LANE_ARR. Lane arrival data is captured when all lanes are ready and the chip attempts to release the elastic buffer. This bit is cleared when SYS_EN=0 or JESD_RST=1. Write 1 to clear this bit and allow the lane arrival data to be recaptured.

8.3.7.9 LANE_INV Register (Offset = 0x12E) [Reset = 0x0000]

LANE_INV is shown in Table 8-80.

Return to the Summary Table.

Table 8-80. LANE_INV Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LANE_INV	R/W	0x0	Program LANE_INV[n]=1 to invert the bitstream through physical lane n. Use this if the differential pair is swapped between the transmitter and receiver.

8.3.7.10 LANE_SEL_0 Register (Offset = 0x130) [Reset = 0x00]

LANE_SEL_0 is shown in Table 8-81.

Return to the Summary Table.

Table 8-81. LANE_SEL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[0]	R/W	0x0	Specify which physical lane (0 to 15) is bound to logical lane 0. To bind physical lane p to logical lane n, program LANE_SEL[n]=p. For example, to bind logical lane 0 to physical lane 3, program LANE_SEL[0]=3.

8.3.7.11 LANE_SEL_1 Register (Offset = 0x131) [Reset = 0x01]

LANE_SEL_1 is shown in Table 8-82.

Return to the Summary Table.

Table 8-82. LANE_SEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[1]	R/W	0x1	Specify which physical lane (0 to 15) is bound to logical lane 1.

8.3.7.12 LANE_SEL_2 Register (Offset = 0x132) [Reset = 0x02]

LANE_SEL_2 is shown in Table 8-83.

Return to the Summary Table.

Table 8-83. LANE_SEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[2]	R/W	0x2	Specify which physical lane (0 to 15) is bound to logical lane 2.

8.3.7.13 LANE_SEL_3 Register (Offset = 0x133) [Reset = 0x03]

LANE_SEL_3 is shown in Table 8-84.

Return to the Summary Table.

Table 8-84. LANE_SEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[3]	R/W	0x3	Specify which physical lane (0 to 15) is bound to logical lane 3.

8.3.7.14 LANE_SEL_4 Register (Offset = 0x134) [Reset = 0x04]

LANE_SEL_4 is shown in Table 8-85.

Return to the Summary Table.

Table 8-85. LANE_SEL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[4]	R/W	0x4	Specify which physical lane (0 to 15) is bound to logical lane 4.

8.3.7.15 LANE_SEL_5 Register (Offset = 0x135) [Reset = 0x05]

LANE_SEL_5 is shown in Table 8-86.

Return to the Summary Table.

Table 8-86. LANE_SEL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[5]	R/W	0x5	Specify which physical lane (0 to 15) is bound to logical lane 5.

8.3.7.16 LANE_SEL_6 Register (Offset = 0x136) [Reset = 0x06]

LANE_SEL_6 is shown in Table 8-87.

Return to the Summary Table.

Table 8-87. LANE_SEL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[6]	R/W	0x6	Specify which physical lane (0 to 15) is bound to logical lane 6.

8.3.7.17 LANE_SEL_7 Register (Offset = 0x137) [Reset = 0x07]

LANE_SEL_7 is shown in Table 8-88.

Return to the Summary Table.

Table 8-88. LANE_SEL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[7]	R/W	0x7	Specify which physical lane (0 to 15) is bound to logical lane 7.

8.3.7.18 LANE_SEL_8 Register (Offset = 0x138) [Reset = 0x08]

LANE_SEL_8 is shown in Table 8-89.

Return to the Summary Table.

Table 8-89. LANE_SEL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[8]	R/W	0x8	Specify which physical lane (0 to 15) is bound to logical lane 8.

8.3.7.19 LANE_SEL_9 Register (Offset = 0x139) [Reset = 0x09]

LANE_SEL_9 is shown in Table 8-90.

Return to the Summary Table.

Table 8-90. LANE_SEL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[9]	R/W	0x9	Specify which physical lane (0 to 15) is bound to logical lane 9.

8.3.7.20 LANE_SEL_10 Register (Offset = 0x13A) [Reset = 0x0A]

LANE_SEL_10 is shown in Table 8-91.

Return to the Summary Table.

Table 8-91. LANE_SEL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[10]	R/W	0xA	Specify which physical lane (0 to 15) is bound to logical lane 10.

8.3.7.21 LANE_SEL_11 Register (Offset = 0x13B) [Reset = 0x0B]

LANE_SEL_11 is shown in Table 8-92.

Return to the Summary Table.

Table 8-92. LANE_SEL_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[11]	R/W	0xB	Specify which physical lane (0 to 15) is bound to logical lane 11.

8.3.7.22 LANE_SEL_12 Register (Offset = 0x13C) [Reset = 0x0C]

LANE_SEL_12 is shown in Table 8-93.

Return to the Summary Table.

Table 8-93. LANE_SEL_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[12]	R/W	0xC	Specify which physical lane (0 to 15) is bound to logical lane 12.

8.3.7.23 LANE_SEL_13 Register (Offset = 0x13D) [Reset = 0x0D]

LANE_SEL_13 is shown in Table 8-94.

Return to the Summary Table.

Table 8-94. LANE_SEL_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[13]	R/W	0xD	Specify which physical lane (0 to 15) is bound to logical lane 13.

8.3.7.24 LANE_SEL_14 Register (Offset = 0x13E) [Reset = 0x0E]

LANE_SEL_14 is shown in Table 8-95.

Return to the Summary Table.

Table 8-95. LANE_SEL_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[14]	R/W	0xE	Specify which physical lane (0 to 15) is bound to logical lane 14.

8.3.7.25 LANE_SEL_15 Register (Offset = 0x13F) [Reset = 0x0F]

LANE_SEL_15 is shown in Table 8-96.

Return to the Summary Table.

Table 8-96. LANE_SEL_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	LANE_SEL[15]	R/W	0xF	Specify which physical lane (0 to 15) is bound to logical lane 15.

8.3.7.26 LANE_ARR_0 Register (Offset = 0x140) [Reset = 0xXX]

LANE_ARR_0 is shown in Table 8-97.

Return to the Summary Table.

Table 8-97. LANE_ARR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	
6-0	LANE_ARR[0]	R	X	Returns the arrival time of lane 0 (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF. For 8b/10b, the value returned can be between 0 and 31 (inclusive), regardless of the multiframe length. For 64b/66b, the value returned can be between 0 and 32*E-1 (inclusive). These registers are valid only when LANE_ARR_RDY=1.

8.3.7.27 LANE_ARR_1 Register (Offset = 0x141) [Reset = 0xXX]

LANE_ARR_1 is shown in Table 8-98.

Return to the Summary Table.

Table 8-98. LANE_ARR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	Reserved
6-0	LANE_ARR[1]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.28 LANE_ARR_2 Register (Offset = 0x142) [Reset = 0xXX]

LANE_ARR_2 is shown in Table 8-99.

Return to the Summary Table.

Table 8-99. LANE_ARR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[2]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.29 LANE_ARR_3 Register (Offset = 0x143) [Reset = 0xXX]

LANE_ARR_3 is shown in Table 8-100.

Return to the Summary Table.

Table 8-100. LANE_ARR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[3]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.30 LANE_ARR_4 Register (Offset = 0x144) [Reset = 0xXX]

LANE_ARR_4 is shown in Table 8-101.

Return to the Summary Table.

Table 8-101. LANE_ARR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[4]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.31 LANE_ARR_5 Register (Offset = 0x145) [Reset = 0xXX]

LANE_ARR_5 is shown in Table 8-102.

Return to the Summary Table.

Table 8-102. LANE_ARR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[5]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.32 LANE_ARR_6 Register (Offset = 0x146) [Reset = 0xXX]

LANE_ARR_6 is shown in Table 8-103.

Return to the Summary Table.

Table 8-103. LANE_ARR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[6]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.33 LANE_ARR_7 Register (Offset = 0x147) [Reset = 0xXX]

LANE_ARR_7 is shown in Table 8-104.

Return to the Summary Table.

Table 8-104. LANE_ARR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[7]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.34 LANE_ARR_8 Register (Offset = 0x148) [Reset = 0xXX]

LANE_ARR_8 is shown in Table 8-105.

Return to the Summary Table.

Table 8-105. LANE_ARR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[8]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.35 LANE_ARR_9 Register (Offset = 0x149) [Reset = 0xXX]

LANE_ARR_9 is shown in Table 8-106.

Return to the Summary Table.

Table 8-106. LANE_ARR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[9]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.36 LANE_ARR_10 Register (Offset = 0x14A) [Reset = 0xXX]

LANE_ARR_10 is shown in Table 8-107.

Return to the Summary Table.

Table 8-107. LANE_ARR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[10]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.37 LANE_ARR_11 Register (Offset = 0x14B) [Reset = 0xXX]

LANE_ARR_11 is shown in Table 8-108.

Return to the Summary Table.

Table 8-108. LANE_ARR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[11]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.38 LANE_ARR_12 Register (Offset = 0x14C) [Reset = 0xXX]

LANE_ARR_12 is shown in Table 8-109.

Return to the Summary Table.

Table 8-109. LANE_ARR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	

Table 8-109. LANE_ARR_12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	LANE_ARR[12]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.39 LANE_ARR_13 Register (Offset = 0x14D) [Reset = 0xXX]

LANE_ARR_13 is shown in Table 8-110.

Return to the Summary Table.

Table 8-110. LANE_ARR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[13]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.40 LANE_ARR_14 Register (Offset = 0x14E) [Reset = 0xXX]

LANE_ARR_14 is shown in Table 8-111.

Return to the Summary Table.

Table 8-111. LANE_ARR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[14]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.41 LANE_ARR_15 Register (Offset = 0x14F) [Reset = 0xXX]

LANE_ARR_15 is shown in Table 8-112.

Return to the Summary Table.

Table 8-112. LANE_ARR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	LANE_ARR[15]	R	X	Returns the arrival time (in units of octa-bytes) with respect to the internal LMFC/LEMC that is established by SYSREF.

8.3.7.42 LANE_STATUS_0 Register (Offset = 0x150) [Reset = 0xXX]

LANE_STATUS_0 is shown in Table 8-113.

Return to the Summary Table.

Table 8-113. LANE_STATUS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2	F_EMB_SYNC	R	X	Returns 1 if logical lane 0 has frame or EMB synchronization.
1	CG_BK_SYNC	R	X	Returns 1 if logical lane 0 has code-group or block synchronization.
0	SIG_DET	R	X	Returns 1 if logical lane 0 is detecting a data signal

8.3.7.43 LANE_STATUS_1 Register (Offset = 0x151) [Reset = 0xXX]

LANE_STATUS_1 is shown in Table 8-114.

Return to the Summary Table.

Table 8-114. LANE_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[1]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.44 LANE_STATUS_2 Register (Offset = 0x152) [Reset = 0xXX]

LANE_STATUS_2 is shown in Table 8-115.

Return to the Summary Table.

Table 8-115. LANE_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[2]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.45 LANE_STATUS_3 Register (Offset = 0x153) [Reset = 0xXX]

LANE_STATUS_3 is shown in Table 8-116.

Return to the Summary Table.

Table 8-116. LANE_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[3]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.46 LANE_STATUS_4 Register (Offset = 0x154) [Reset = 0xXX]

LANE_STATUS_4 is shown in Table 8-117.

Return to the Summary Table.

Table 8-117. LANE_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[4]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.47 LANE_STATUS_5 Register (Offset = 0x155) [Reset = 0xXX]

LANE_STATUS_5 is shown in Table 8-118.

Return to the Summary Table.

Table 8-118. LANE_STATUS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[5]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.48 LANE_STATUS_6 Register (Offset = 0x156) [Reset = 0xXX]

LANE_STATUS_6 is shown in Table 8-119.

Return to the Summary Table.

Table 8-119. LANE_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[6]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.49 LANE_STATUS_7 Register (Offset = 0x157) [Reset = 0xXX]

LANE_STATUS_7 is shown in Table 8-120.

Return to the Summary Table.

Table 8-120. LANE_STATUS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[7]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.50 LANE_STATUS_8 Register (Offset = 0x158) [Reset = 0xXX]

LANE_STATUS_8 is shown in Table 8-121.

Return to the Summary Table.

Table 8-121. LANE_STATUS_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[8]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.51 LANE_STATUS_9 Register (Offset = 0x159) [Reset = 0xXX]

LANE_STATUS_9 is shown in Table 8-122.

Return to the Summary Table.

Table 8-122. LANE_STATUS_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[9]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.52 LANE_STATUS_10 Register (Offset = 0x15A) [Reset = 0xXX]

LANE_STATUS_10 is shown in Table 8-123.

Return to the Summary Table.

Table 8-123. LANE_STATUS_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[10]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.53 LANE_STATUS_11 Register (Offset = 0x15B) [Reset = 0xXX]

LANE_STATUS_11 is shown in Table 8-124.

Return to the Summary Table.

Table 8-124. LANE_STATUS_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[11]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.54 LANE_STATUS_12 Register (Offset = 0x15C) [Reset = 0xXX]

LANE_STATUS_12 is shown in Table 8-125.

Return to the Summary Table.

Table 8-125. LANE_STATUS_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[12]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.55 LANE_STATUS_13 Register (Offset = 0x15D) [Reset = 0xXX]

LANE_STATUS_13 is shown in Table 8-126.

Return to the Summary Table.

Table 8-126. LANE_STATUS_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[13]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.56 LANE_STATUS_14 Register (Offset = 0x15E) [Reset = 0xXX]

LANE_STATUS_14 is shown in Table 8-127.

Return to the Summary Table.

Table 8-127. LANE_STATUS_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[14]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.57 LANE_STATUS_15 Register (Offset = 0x15F) [Reset = 0xXX]

LANE_STATUS_15 is shown in Table 8-128.

Return to the Summary Table.

Table 8-128. LANE_STATUS_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_STATUS[15]	R	X	See registers and description for LANE_STATUS[0]

8.3.7.58 LANE_ERROR_0 Register (Offset = 0x160) [Reset = 0xXX]

LANE_ERROR_0 is shown in Table 8-129.

Return to the Summary Table.

Table 8-129. LANE_ERROR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[0]	W1C	X	Sticky bits indicating various errors on lane 0. 0x0 = Gearbox FIFO overflowed or underflowed. As long as the write clock frequency is correct the gearbox write clock can drift at least 3UI after this flag without causing data corruption. 0x1 = Disparity error (8b/10b) or invalid sync header (64b/66b) occurred. 0x2 = Not-in-table or unexpected control character (8b/10b) or Data Integrity (64b/66b) error occurred. 0x3 = Reserved 0x4 = Code-group or block synchronization was lost. 0x5 = Frame alignment was lost (8b/10b only) or DI_FAULTis 1 (64b/66b). 0x6 = Multi-frame, multi-block, or extended-multi-block alignment lost. 0x7 = Alignment character found at unexpected location (8b/10b) or (extended)-multi-block pilot signal not in expected location (64b/66b)

8.3.7.59 LANE_ERROR_1 Register (Offset = 0x161) [Reset = 0xXX]

LANE_ERROR_1 is shown in Table 8-130.

Return to the Summary Table.

Table 8-130. LANE_ERROR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[1]	W1C	X	Sticky bits indicating various errors on lane 1. See description for LANE_ERROR[0]

8.3.7.60 LANE_ERROR_2 Register (Offset = 0x162) [Reset = 0xXX]

LANE_ERROR_2 is shown in Table 8-131.

Return to the Summary Table.

Table 8-131. LANE_ERROR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[2]	W1C	X	Sticky bits indicating various errors on lane 2. See description for LANE_ERROR[0]

8.3.7.61 LANE_ERROR_3 Register (Offset = 0x163) [Reset = 0xXX]

LANE_ERROR_3 is shown in Table 8-132.

Return to the Summary Table.

Table 8-132. LANE_ERROR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[3]	W1C	X	Sticky bits indicating various errors on lane 3. See description for LANE_ERROR[0]

8.3.7.62 LANE_ERROR_4 Register (Offset = 0x164) [Reset = 0xXX]

LANE_ERROR_4 is shown in Table 8-133.

Return to the Summary Table.

Table 8-133. LANE_ERROR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[4]	W1C	X	Sticky bits indicating various errors on lane 4. See description for LANE_ERROR[0]

8.3.7.63 LANE_ERROR_5 Register (Offset = 0x165) [Reset = 0xXX]

LANE_ERROR_5 is shown in Table 8-134.

Return to the Summary Table.

Table 8-134. LANE_ERROR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[5]	W1C	X	Sticky bits indicating various errors on lane 5. See description for LANE_ERROR[0]

8.3.7.64 LANE_ERROR_6 Register (Offset = 0x166) [Reset = 0xXX]

LANE_ERROR_6 is shown in Table 8-135.

Return to the Summary Table.

Table 8-135. LANE_ERROR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[6]	W1C	X	Sticky bits indicating various errors on lane 6. See description for LANE_ERROR[0]

8.3.7.65 LANE_ERROR_7 Register (Offset = 0x167) [Reset = 0xXX]

LANE_ERROR_7 is shown in Table 8-136.

Return to the Summary Table.

Table 8-136. LANE_ERROR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[7]	W1C	X	Sticky bits indicating various errors on lane 7. See description for LANE_ERROR[0]

8.3.7.66 LANE_ERROR_8 Register (Offset = 0x168) [Reset = 0xXX]

LANE_ERROR_8 is shown in Table 8-137.

Return to the Summary Table.

Table 8-137. LANE_ERROR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[8]	W1C	X	Sticky bits indicating various errors on lane 8. See description for LANE_ERROR[0]

8.3.7.67 LANE_ERROR_9 Register (Offset = 0x169) [Reset = 0xXX]

LANE_ERROR_9 is shown in Table 8-138.

Return to the Summary Table.

Table 8-138. LANE_ERROR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[9]	W1C	X	Sticky bits indicating various errors on lane 9. See description for LANE_ERROR[0]

8.3.7.68 LANE_ERROR_10 Register (Offset = 0x16A) [Reset = 0xXX]

LANE_ERROR_10 is shown in Table 8-139.

Return to the Summary Table.

Table 8-139. LANE_ERROR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[10]	W1C	X	Sticky bits indicating various errors on lane 10. See description for LANE_ERROR[0]

8.3.7.69 LANE_ERROR_11 Register (Offset = 0x16B) [Reset = 0xXX]

LANE_ERROR_11 is shown in Table 8-140.

Return to the Summary Table.

Table 8-140. LANE_ERROR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[11]	W1C	X	Sticky bits indicating various errors on lane 11. See description for LANE_ERROR[0]

8.3.7.70 LANE_ERROR_12 Register (Offset = 0x16C) [Reset = 0xXX]

LANE_ERROR_12 is shown in Table 8-141.

Return to the Summary Table.

Table 8-141. LANE_ERROR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[12]	W1C	X	Sticky bits indicating various errors on lane 12. See description for LANE_ERROR[0]

8.3.7.71 LANE_ERROR_13 Register (Offset = 0x16D) [Reset = 0xXX]

LANE_ERROR_13 is shown in Table 8-142.

Return to the Summary Table.

Table 8-142. LANE_ERROR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[13]	W1C	X	Sticky bits indicating various errors on lane 13. See description for LANE_ERROR[0]

8.3.7.72 LANE_ERROR_14 Register (Offset = 0x16E) [Reset = 0xXX]

LANE_ERROR_14 is shown in Table 8-143.

Return to the Summary Table.

Table 8-143. LANE_ERROR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[14]	W1C	X	Sticky bits indicating various errors on lane 14. See description for LANE_ERROR[0]

8.3.7.73 LANE_ERROR_15 Register (Offset = 0x16F) [Reset = 0xXX]

LANE_ERROR_15 is shown in Table 8-144.

Return to the Summary Table.

Table 8-144. LANE_ERROR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LANE_ERROR[15]	W1C	X	Sticky bits indicating various errors on lane 15. See description for LANE_ERROR[0]

8.3.7.74 FIFO_STATUS_0 Register (Offset = 0x170) [Reset = 0xXX]

FIFO_STATUS_0 is shown in Table 8-145.

Return to the Summary Table.

Table 8-145. FIFO_STATUS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PDIFF	R	X	This register returns the difference between the write and read pointers inside the gearbox FIFO for logical lane 0.

8.3.7.75 FIFO_STATUS_1 Register (Offset = 0x171) [Reset = 0xXX]

FIFO_STATUS_1 is shown in Table 8-146.

Return to the Summary Table.

Table 8-146. FIFO_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[1]	R	X	See description for FIFO_STATUS[0]

8.3.7.76 FIFO_STATUS_2 Register (Offset = 0x172) [Reset = 0xXX]

FIFO_STATUS_2 is shown in Table 8-147.

Return to the Summary Table.

Table 8-147. FIFO_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[2]	R	X	See description for FIFO_STATUS[0]

8.3.7.77 FIFO_STATUS_3 Register (Offset = 0x173) [Reset = 0xXX]

FIFO_STATUS_3 is shown in Table 8-148.

Return to the Summary Table.

Table 8-148. FIFO_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[3]	R	X	See description for FIFO_STATUS[0]

8.3.7.78 FIFO_STATUS_4 Register (Offset = 0x174) [Reset = 0xXX]

FIFO_STATUS_4 is shown in Table 8-149.

Return to the Summary Table.

Table 8-149. FIFO_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[4]	R	X	See description for FIFO_STATUS[0]

8.3.7.79 FIFO_STATUS_5 Register (Offset = 0x175) [Reset = 0xXX]

FIFO_STATUS_5 is shown in Table 8-150.

Return to the Summary Table.

Table 8-150. FIFO_STATUS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[5]	R	X	See description for FIFO_STATUS[0]

8.3.7.80 FIFO_STATUS_6 Register (Offset = 0x176) [Reset = 0xXX]

FIFO_STATUS_6 is shown in Table 8-151.

Return to the Summary Table.

Table 8-151. FIFO_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[6]	R	X	See description for FIFO_STATUS[0]

8.3.7.81 FIFO_STATUS_7 Register (Offset = 0x177) [Reset = 0xXX]

FIFO_STATUS_7 is shown in Table 8-152.

Return to the Summary Table.

Table 8-152. FIFO_STATUS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[7]	R	X	See description for FIFO_STATUS[0]

8.3.7.82 FIFO_STATUS_8 Register (Offset = 0x178) [Reset = 0xXX]

FIFO_STATUS_8 is shown in Table 8-153.

Return to the Summary Table.

Table 8-153. FIFO_STATUS_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[8]	R	X	See description for FIFO_STATUS[0]

8.3.7.83 FIFO_STATUS_9 Register (Offset = 0x179) [Reset = 0xXX]

FIFO_STATUS_9 is shown in Table 8-154.

Return to the Summary Table.

Table 8-154. FIFO_STATUS_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[9]	R	X	See description for FIFO_STATUS[0]

8.3.7.84 FIFO_STATUS_10 Register (Offset = 0x17A) [Reset = 0xXX]

FIFO_STATUS_10 is shown in Table 8-155.

Return to the Summary Table.

Table 8-155. FIFO_STATUS_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[10]	R	X	See description for FIFO_STATUS[0]

8.3.7.85 FIFO_STATUS_11 Register (Offset = 0x17B) [Reset = 0xXX]

FIFO_STATUS_11 is shown in Table 8-156.

Return to the Summary Table.

Table 8-156. FIFO_STATUS_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[11]	R	X	See description for FIFO_STATUS[0]

8.3.7.86 FIFO_STATUS_12 Register (Offset = 0x17C) [Reset = 0xXX]

FIFO_STATUS_12 is shown in Table 8-157.

Return to the Summary Table.

Table 8-157. FIFO_STATUS_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[12]	R	X	See description for FIFO_STATUS[0]

8.3.7.87 FIFO_STATUS_13 Register (Offset = 0x17D) [Reset = 0xXX]

FIFO_STATUS_13 is shown in Table 8-158.

Return to the Summary Table.

Table 8-158. FIFO_STATUS_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[13]	R	X	See description for FIFO_STATUS[0]

8.3.7.88 FIFO_STATUS_14 Register (Offset = 0x17E) [Reset = 0xXX]

FIFO_STATUS_14 is shown in Table 8-159.

Return to the Summary Table.

Table 8-159. FIFO_STATUS_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[14]	R	X	See description for FIFO_STATUS[0]

8.3.7.89 FIFO_STATUS_15 Register (Offset = 0x17F) [Reset = 0xXX]

FIFO_STATUS_15 is shown in Table 8-160.

Return to the Summary Table.

Table 8-160. FIFO_STATUS_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIFO_STATUS[15]	R	X	See description for FIFO_STATUS[0]

8.3.7.90 JCAP_ARM Register (Offset = 0x18A) [Reset = 0x00]

JCAP_ARM is shown in Table 8-161.

Return to the Summary Table.

Table 8-161. JCAP_ARM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	JCAP_ARM	R/W	0x0	Transitioning this bit from 0 to 1 will arm the capture debug system to capture on the next JCAP trigger event. Only a single capture will occur each time the system is armed.

8.3.7.91 JCAP_MODE Register (Offset = 0x18B) [Reset = 0x00]

JCAP_MODE is shown in Table 8-162.

Return to the Summary Table.

Table 8-162. JCAP_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	JCAP_MODE	R/W	0x0	Selects the debug capture mode 0x0 = **[JESD_JCAP_LINKIN]** Capture the input of the link layer (gearbox output). Trigger immediately after JCAP_ARM is set. If JCAP_ARM is set before SYS_EN, trigger when SYS_EN is set and the gearbox has released (gearboxes for different lanes may release at different times). 0x1 = **[JESD_JCAP_LINKOUT]** Captures the output of the link layer. Trigger on next start of MF/EMB after JCAP_ARM is set. If JCAP_ARM is set before SYS_EN the trigger will occur on the first MF/EMB from the lane. (This allows capturing the ILAS in 8b/10b mode.) Note: Different lanes may trigger on different MF/EMB boundaries (this applies to 64b/66b or 8b/10b if the link is up before JCAP_ARM is set). 0x2 = **[JESD_JCAP_TRANS]** Captures the output of the transport layer. Trigger immediately after JCAP_ARM is set. This should only be used when LINK_UP=1. JCAP_OFFSET is ignored in this mode. 0x3-0xF = Reserved

8.3.7.92 JCAP_OFFSET Register (Offset = 0x18C) [Reset = 0x0000]

JCAP_OFFSET is shown in Table 8-163.

Return to the Summary Table.

Table 8-163. JCAP_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	JCAP_OFFSET	R/W	0x0	Delay the start of capture until JCAP_OFFSET*8 octets after the JCAP trigger event defined by JCAP_MODE.

8.3.7.93 JCAP_PAGE Register (Offset = 0x18E) [Reset = 0x00]

JCAP_PAGE is shown in Table 8-164.

Return to the Summary Table.

Table 8-164. JCAP_PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	
4-0	JCAP_PAGE	R/W	0x0	Selects which logical page to access captured data from when reading JCAP or JCAP_STATUS. When JCAP_MODE < 2, only the first 16 pages are valid and correspond to the logical lanes. For JCAP_MODE=2, the first 32 pages are valid and map data as shown in Transport Layer Debug Capture. You may write JCAP_PAGE as needed to access status and data from all lanes.

8.3.7.94 JCAP_STATUS Register (Offset = 0x18F) [Reset = 0x00]

JCAP_STATUS is shown in Table 8-165.

Return to the Summary Table.

Table 8-165. JCAP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	JCAP_STATUS	R/W	0x0	When this bit returns a 1, it indicates that the lane specified by JCAP_PAGE has completed its capture, and data is available to be read from JCAP. This bit is reset any time JCAP_ARM=0, SYS_EN=0 , or JESD_RST=1. Before reading JCAP_STATUS, program JCAP_PAGE. Note: When JCAP_MODE < 2, each of the 16 JCAP_PAGEs will contain a unique JCAP_STATUS. When JCAP_MODE=2, JCAP_STATUS is only defined when JCAP_PAGE=0.

8.3.7.95 JCAP Register (Offset = 0x190) [Reset = 0xXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

JCAP is shown in Table 8-166.

Return to the Summary Table.

Table 8-166. JCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
127-0	JCAP	R	X	When capturing physical or link layer data, address 0x0190 is the first byte captured, and 0x019F is the last byte captured. Within each byte, bit 7 is the first bit captured and bit 0 is the last bit captured. When capturing transport layer data, refer to Transport Layer Debug Capture. Before reading JCAP, program JCAP_PAGE. Unless JCAP_STATUS=1, the values returned here are undefined.

ADVANCE INFORMATION

8.3.7.96 LEC_CTRL Register (Offset = 0x1A0) [Reset = 0x02]

LEC_CTRL is shown in Table 8-167.

Return to the Summary Table.

Table 8-167. LEC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-2	LEC_CNT_SEL	R/W	0x0	Select which lane error counters are accessible in LEC_CNT. 0x0 = BER Counters 0x1 = FEC Correctable Error Counters 0x2 = FEC Uncorrectable Error Counters 0x3 = RESERVED
1	FEC_EM_EN	R/W	0x1	When this bit is set, JENC=1, and SHMODE=2, the FEC error counters will count the number of multi-blocks with FEC errors. To clear and restart the counters, program FEC_EM_EN to 0 and then back to 1.
0	BER_EN	R/W	0x0	After setting up the receiver parameters, the user can program JTEST to a PRBS mode, ensure the JESD interface is enabled (see DSP_MODE), set SYS_EN, and then set BER_EN to enable the BER counters (see LEC_CNTn). To clear and restart the counters, program BER_EN to 0 and then back to 1. The BER logic will self-synchronize to the incoming PRBS data after the rising edge of BER_EN.

8.3.7.97 LEC_CNT_0 Register (Offset = 0x1B0) [Reset = 0xXX]

LEC_CNT_0 is shown in Table 8-168.

Return to the Summary Table.

Table 8-168. LEC_CNT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[0]	R	X	Returns the number of errors detected on lane 0 by the error counters selected in LEC_CNT_SEL. This value will saturate at 255. For the BER counters, the bit-error-rate for lane n can be computed as follows: BER = LEC_CNT[0] / F_{BIT} / T_{BER} Where TBER is the number of seconds that has elapsed from when BER_EN was set to when LEC_CNT[n] was read. T_{BER} is measured by the host system or clock. For the FEC counters, the multi-block error rate (MER) for lane n can be computed as follows: MER = LEC_CNT[0] / (66*32*F_{BIT}) / T_{MER} Where T_{MER} is the number of seconds that elapsed between when the error counters were started and when LEC_CNT[0] was read. T_{MER} is measured by the host system or clock. The FEC error counters are reset when SYS_EN=0, JESD_RST=1, FEC_EM_EN=0, or JTimer expires (see JTIMER). Note: The error counters on disabled lanes and lanes enabled by EXTRA_LANE are undefined. Note: User must wait at least 1us after enabling the counters (using either BER_EN or FEC_EM_EN) before reading this register.

8.3.7.98 LEC_CNT_1 Register (Offset = 0x1B1) [Reset = 0xXX]

LEC_CNT_1 is shown in Table 8-169.

Return to the Summary Table.

Table 8-169. LEC_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[1]	R	X	See description for LEC_CNT[0]

8.3.7.99 LEC_CNT_2 Register (Offset = 0x1B2) [Reset = 0xXX]

LEC_CNT_2 is shown in Table 8-170.

Return to the Summary Table.

Table 8-170. LEC_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[2]	R	X	See description for LEC_CNT[0]

8.3.7.100 LEC_CNT_3 Register (Offset = 0x1B3) [Reset = 0xXX]

LEC_CNT_3 is shown in Table 8-171.

Return to the Summary Table.

Table 8-171. LEC_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[3]	R	X	See description for LEC_CNT[0]

8.3.7.101 LEC_CNT_4 Register (Offset = 0x1B4) [Reset = 0xXX]

LEC_CNT_4 is shown in Table 8-172.

Return to the Summary Table.

Table 8-172. LEC_CNT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[4]	R	X	See description for LEC_CNT[0]

8.3.7.102 LEC_CNT_5 Register (Offset = 0x1B5) [Reset = 0xXX]

LEC_CNT_5 is shown in Table 8-173.

Return to the Summary Table.

Table 8-173. LEC_CNT_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[5]	R	X	See description for LEC_CNT[0]

8.3.7.103 LEC_CNT_6 Register (Offset = 0x1B6) [Reset = 0xXX]

LEC_CNT_6 is shown in Table 8-174.

Return to the Summary Table.

Table 8-174. LEC_CNT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[6]	R	X	See description for LEC_CNT[0]

8.3.7.104 LEC_CNT_7 Register (Offset = 0x1B7) [Reset = 0xXX]

LEC_CNT_7 is shown in Table 8-175.

Return to the Summary Table.

Table 8-175. LEC_CNT_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[7]	R	X	See description for LEC_CNT[0]

8.3.7.105 LEC_CNT_8 Register (Offset = 0x1B8) [Reset = 0xXX]

LEC_CNT_8 is shown in Table 8-176.

Return to the Summary Table.

Table 8-176. LEC_CNT_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[8]	R	X	See description for LEC_CNT[0]

8.3.7.106 LEC_CNT_9 Register (Offset = 0x1B9) [Reset = 0xXX]

LEC_CNT_9 is shown in Table 8-177.

Return to the Summary Table.

Table 8-177. LEC_CNT_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[9]	R	X	See description for LEC_CNT[0]

8.3.7.107 LEC_CNT_10 Register (Offset = 0x1BA) [Reset = 0xXX]

LEC_CNT_10 is shown in Table 8-178.

Return to the Summary Table.

Table 8-178. LEC_CNT_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[10]	R	X	See description for LEC_CNT[0]

8.3.7.108 LEC_CNT_11 Register (Offset = 0x1BB) [Reset = 0xXX]

LEC_CNT_11 is shown in Table 8-179.

Return to the Summary Table.

Table 8-179. LEC_CNT_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[11]	R	X	See description for LEC_CNT[0]

8.3.7.109 LEC_CNT_12 Register (Offset = 0x1BC) [Reset = 0xXX]

LEC_CNT_12 is shown in Table 8-180.

Return to the Summary Table.

Table 8-180. LEC_CNT_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[12]	R	X	See description for LEC_CNT[0]

8.3.7.110 LEC_CNT_13 Register (Offset = 0x1BD) [Reset = 0xXX]

LEC_CNT_13 is shown in Table 8-181.

Return to the Summary Table.

Table 8-181. LEC_CNT_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[13]	R	X	See description for LEC_CNT[0]

8.3.7.111 LEC_CNT_14 Register (Offset = 0x1BE) [Reset = 0xXX]

LEC_CNT_14 is shown in Table 8-182.

Return to the Summary Table.

Table 8-182. LEC_CNT_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[14]	R	X	See description for LEC_CNT[0]

8.3.7.112 LEC_CNT_15 Register (Offset = 0x1BF) [Reset = 0xXX]

LEC_CNT_15 is shown in Table 8-183.

Return to the Summary Table.

Table 8-183. LEC_CNT_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEC_CNT[15]	R	X	See description for LEC_CNT[0]

8.3.8 SerDes_Equalizer Registers

Table 8-184 lists the memory-mapped registers for the SerDes_Equalizer registers. All register offset addresses not listed in Table 8-184 should be considered as reserved locations and the register contents should not be modified.

Table 8-184. SERDES_EQUALIZER Registers

Offset	Acronym	Register Name	Section
0x1C0	CDR0		Section 8.3.8.1
0x1D0	EQ_CTRL		Section 8.3.8.2
0x1D1	EQZERO		Section 8.3.8.3
0x1D2	LANE_EQ_0		Section 8.3.8.4
0x1D3	LANE_EQ_1		Section 8.3.8.5
0x1D4	LANE_EQ_2		Section 8.3.8.6
0x1D5	LANE_EQ_3		Section 8.3.8.7
0x1D6	LANE_EQ_4		Section 8.3.8.8
0x1D7	LANE_EQ_5		Section 8.3.8.9
0x1D8	LANE_EQ_6		Section 8.3.8.10
0x1D9	LANE_EQ_7		Section 8.3.8.11
0x1DA	LANE_EQ_8		Section 8.3.8.12
0x1DB	LANE_EQ_9		Section 8.3.8.13
0x1DC	LANE_EQ_10		Section 8.3.8.14
0x1DD	LANE_EQ_11		Section 8.3.8.15
0x1DE	LANE_EQ_12		Section 8.3.8.16
0x1DF	LANE_EQ_13		Section 8.3.8.17
0x1E0	LANE_EQ_14		Section 8.3.8.18
0x1E1	LANE_EQ_15		Section 8.3.8.19
0x1E2	EQDEBUG		Section 8.3.8.20

Complex bit access types are encoded to fit into small table cells. Table 8-185 shows the codes that are used for access types in this section.

Table 8-185. SerDes_Equalizer Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.8.1 CDR0 Register (Offset = 0x1C0) [Reset = 0x51]

CDR0 is shown in Table 8-186.

Return to the Summary Table.

Table 8-186. CDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	
6-4	CDRVOTE	R/W	0x5	Specifies how many (net) votes are needed to cause the CDR loop to adjust the phase interpolators. Higher settings slow down the loop, but decrease loop noise. Note: This register should only be changed when SYS_EN=0. 0x0 = 1 0x1 = 3 0x2 = 5 0x3 = 7 0x4 = 15 0x5 = 31 (default) 0x6 = Reserved 0x7 = Reserved
3-2	RESERVED	R	0x0	
1-0	CDRSTL	R/W	0x1	Specifies how long the CDR loop stops analyzing data after each adjustment to the phase interpolators. Note: This register should only be changed when SYS_EN=0. 0x0 = 32UI 0x1 = 96UI 0x2 = 192UI 0x3 = 2016UI

8.3.8.2 EQ_CTRL Register (Offset = 0x1D0) [Reset = 0x00]

EQ_CTRL is shown in Table 8-187.

Return to the Summary Table.

Table 8-187. EQ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	
4	EQ_OVR	R/W	0x0	When EQMODE is 1 or higher, you can program EQ_OVR=1 to over-ride the equalizer level using the EQLEVEL[n] registers. Affects all lanes.
3	EQZ_OVR	R/W	0x0	Set this bit to enable the EQZERO register (to override the equalizer's zero frequency). When EQZ_OVR=0, the frequency is set based on the RATE register. Affects all lanes.
2	EQHOLD	R/W	0x0	When the equalizer is in fully-adaptive mode (EQMODE=1 and EQ_OVR=0), programming EQHOLD will freeze (hold) the adaptation loop (for all lanes).
1-0	EQMODE	R/W	0x0	Sets the equalizer mode (for all lanes): See Equalizer section. 0x0 = EQ_DISABLE 0x1 = EQ_ENABLE 0x2 = EQ_PRECURSOR 0x3 = EQ_POSTCURSOR

8.3.8.3 EQZERO Register (Offset = 0x1D1) [Reset = 0x00]

EQZERO is shown in Table 8-188.

Return to the Summary Table.

Table 8-188. EQZERO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	

Table 8-188. EQZERO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	EQZERO	R/W	0x0	When EQZ_OVR=1, this field over-rides the equalizers zero frequency (for all lanes). When EQZ_OVR=0, the zero frequency is set automatically based on the RATE setting. EQZERO:Zero Frequency (MHz):Notes 0:114: 2:124:Automatic setting for RATE = 4 10:169: 17:222:Automatic setting for RATE = 3 22:326: 25:426:Automatic setting for RATE = 2 27:615: 29:792:Automatic setting for RATE = 1 30:1122: 31:2027::Automatic setting for RATE = 0 all others:RESERVED:

8.3.8.4 LANE_EQ_0 Register (Offset = 0x1D2) [Reset = 0x17]

LANE_EQ_0 is shown in Table 8-189.

Return to the Summary Table.

Table 8-189. LANE_EQ_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[0]	R/W	0x1	Controls EQ trim for physical lane 0. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[0]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 0. The valid range is from 0 to 14.

8.3.8.5 LANE_EQ_1 Register (Offset = 0x1D3) [Reset = 0x17]

LANE_EQ_1 is shown in Table 8-190.

Return to the Summary Table.

Table 8-190. LANE_EQ_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[1]	R/W	0x1	Controls EQ trim for physical lane 1. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[1]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 1. The valid range is from 0 to 14.

8.3.8.6 LANE_EQ_2 Register (Offset = 0x1D4) [Reset = 0x17]

LANE_EQ_2 is shown in Table 8-191.

Return to the Summary Table.

Table 8-191. LANE_EQ_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[2]	R/W	0x1	Controls EQ trim for physical lane 2. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[2]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 2. The valid range is from 0 to 14.

8.3.8.7 LANE_EQ_3 Register (Offset = 0x1D5) [Reset = 0x17]

LANE_EQ_3 is shown in Table 8-192.

Return to the Summary Table.

Table 8-192. LANE_EQ_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[3]	R/W	0x1	Controls EQ trim for physical lane 3. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[3]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 3. The valid range is from 0 to 14.

8.3.8.8 LANE_EQ_4 Register (Offset = 0x1D6) [Reset = 0x17]

LANE_EQ_4 is shown in Table 8-193.

Return to the Summary Table.

Table 8-193. LANE_EQ_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[4]	R/W	0x1	Controls EQ trim for physical lane 4. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[4]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 4. The valid range is from 0 to 14.

8.3.8.9 LANE_EQ_5 Register (Offset = 0x1D7) [Reset = 0x17]

LANE_EQ_5 is shown in Table 8-194.

Return to the Summary Table.

Table 8-194. LANE_EQ_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	

Table 8-194. LANE_EQ_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	EQTRIM[5]	R/W	0x1	Controls EQ trim for physical lane 5. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[5]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 5. The valid range is from 0 to 14.

8.3.8.10 LANE_EQ_6 Register (Offset = 0x1D8) [Reset = 0x17]

LANE_EQ_6 is shown in Table 8-195.

Return to the Summary Table.

Table 8-195. LANE_EQ_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[6]	R/W	0x1	Controls EQ trim for physical lane 6. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[6]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 6. The valid range is from 0 to 14.

8.3.8.11 LANE_EQ_7 Register (Offset = 0x1D9) [Reset = 0x17]

LANE_EQ_7 is shown in Table 8-196.

Return to the Summary Table.

Table 8-196. LANE_EQ_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[7]	R/W	0x1	Controls EQ trim for physical lane 7. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[7]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 7. The valid range is from 0 to 14.

8.3.8.12 LANE_EQ_8 Register (Offset = 0x1DA) [Reset = 0x17]

LANE_EQ_8 is shown in Table 8-197.

Return to the Summary Table.

Table 8-197. LANE_EQ_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[8]	R/W	0x1	Controls EQ trim for physical lane 8. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18

Table 8-197. LANE_EQ_8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	EQLEVEL[8]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 8. The valid range is from 0 to 14.

8.3.8.13 LANE_EQ_9 Register (Offset = 0x1DB) [Reset = 0x17]

LANE_EQ_9 is shown in Table 8-198.

Return to the Summary Table.

Table 8-198. LANE_EQ_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[9]	R/W	0x1	Controls EQ trim for physical lane 9. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[9]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 9. The valid range is from 0 to 14.

8.3.8.14 LANE_EQ_10 Register (Offset = 0x1DC) [Reset = 0x17]

LANE_EQ_10 is shown in Table 8-199.

Return to the Summary Table.

Table 8-199. LANE_EQ_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[10]	R/W	0x1	Controls EQ trim for physical lane 10. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[10]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 10. The valid range is from 0 to 14.

8.3.8.15 LANE_EQ_11 Register (Offset = 0x1DD) [Reset = 0x17]

LANE_EQ_11 is shown in Table 8-200.

Return to the Summary Table.

Table 8-200. LANE_EQ_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[11]	R/W	0x1	Controls EQ trim for physical lane 11. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[11]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 11. The valid range is from 0 to 14.

ADVANCE INFORMATION

8.3.8.16 LANE_EQ_12 Register (Offset = 0x1DE) [Reset = 0x17]

LANE_EQ_12 is shown in Table 8-201.

Return to the Summary Table.

Table 8-201. LANE_EQ_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[12]	R/W	0x1	Controls EQ trim for physical lane 12. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[12]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 12. The valid range is from 0 to 14.

8.3.8.17 LANE_EQ_13 Register (Offset = 0x1DF) [Reset = 0x17]

LANE_EQ_13 is shown in Table 8-202.

Return to the Summary Table.

Table 8-202. LANE_EQ_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[13]	R/W	0x1	Controls EQ trim for physical lane 13. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[13]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 13. The valid range is from 0 to 14.

8.3.8.18 LANE_EQ_14 Register (Offset = 0x1E0) [Reset = 0x17]

LANE_EQ_14 is shown in Table 8-203.

Return to the Summary Table.

Table 8-203. LANE_EQ_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[14]	R/W	0x1	Controls EQ trim for physical lane 14. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[14]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 14. The valid range is from 0 to 14.

8.3.8.19 LANE_EQ_15 Register (Offset = 0x1E1) [Reset = 0x17]

LANE_EQ_15 is shown in Table 8-204.

Return to the Summary Table.

Table 8-204. LANE_EQ_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-4	EQTRIM[15]	R/W	0x1	Controls EQ trim for physical lane 15. 0x0 = EQ_TRIM_POS12 0x1 = EQ_TRIM_DEFAULT 0x2 = EQ_TRIM_NEG10 0x3 = EQ_TRIM_NEG18
3-0	EQLEVEL[15]	R/W	0x7	When EQ_OVR=1, this field controls the equalization level for physical lane 15. The valid range is from 0 to 14.

8.3.8.20 EQDEBUG Register (Offset = 0x1E2) [Reset = 0x06]

EQDEBUG is shown in Table 8-205.

Return to the Summary Table.

Table 8-205. EQDEBUG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5	EQUD	R/W	0x0	When set, the adaptive EQ will detect "P" patterns to improve its ability to recover from severely under-equalized situations that may prevent the CDR from locking.
4	EQOD	R/W	0x0	When set, the adaptive EQ will reduce the equalization level if no equalization patterns can be detected for a long time. This helps recover from severely over-equalized situations. This feature is NOT implemented in the PHY.
3-0	RESERVED	R	0x0	

8.3.9 SerDes_Eye-Scan Registers

Table 8-206 lists the memory-mapped registers for the SerDes_Eye-Scan registers. All register offset addresses not listed in Table 8-206 should be considered as reserved locations and the register contents should not be modified.

Table 8-206. SERDES_EYE-SCAN Registers

Offset	Acronym	Register Name	Section
0x1F0	ESRUN		Section 8.3.9.1
0x1F1	ES_CNTL		Section 8.3.9.2
0x1F2	ESPO		Section 8.3.9.3
0x1F3	ESVO		Section 8.3.9.4
0x1F4	ESBSEL		Section 8.3.9.5
0x1F5	ECOUNT_CLR		Section 8.3.9.6

Complex bit access types are encoded to fit into small table cells. Table 8-207 shows the codes that are used for access types in this section.

Table 8-207. SerDes_Eye-Scan Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.9.1 ESRUN Register (Offset = 0x1F0) [Reset = 0x00]

ESRUN is shown in Table 8-208.

Return to the Summary Table.

Table 8-208. ESRUN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	ESRUN	R/W	0x0	After setting up eye-scan, set ESRUN=1 to run the eye-scan test. See Eye-Scan Usage Model.

8.3.9.2 ES_CNTL Register (Offset = 0x1F1) [Reset = 0x00]

ES_CNTL is shown in Table 8-209.

Return to the Summary Table.

Table 8-209. ES_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	

Table 8-209. ES_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	ESLEN	R/W	0x0	Specify the length of the eye-scan test. Larger values will give more consistent results, but will take longer. Note: Many eye-scan modes only analyze zeros (or ones). Since they dont analyze every sample, those modes will take longer to complete compared to a mode that analyzes all samples. 0x0 = 127 0x1 = 1032 0x2 = 8191 0x3 = 65535
3-0	EYESCAN_MODE	R/W	0x0	Specify the eye-scan mode. Applies to all lanes. Note: Only change this register while ESRUN=0. 0x0 = ES_DISABLED Eye-scan disabled (default). 0x1 = ES_COMPARE Counts mismatches between the normal sampler and the eye-scan sampler. Analyzes zeros and ones. 0x2 = ES_COMPAREZEROS Same as 0b0001, but only analyzes zeros. 0x3 = ES_COMPAREONES Same as 0b0001, but only analyzes ones. 0x4 = ES_COUNTONES Increments ECOUNT[n] when the eye-scan sample is 1. 0x5 = RESERVED 0x6 = RESERVED 0x7 = RESERVED 0x8 = ES_AVEZEROS Adjusts ESVO_S[n] to the average voltage for a zero. 0x9 = ES_OUTERZEROS Adjusts ESVO_S[n] to the lowest voltage for a zero. 0xA = ES_INNERZEROS Adjusts ESVO_Sn to the highest voltage for a zero. 0xB = RESERVED 0xC = ES_AVGONES Adjusts ESVO_Sn to the average voltage for a one. 0xD = ES_OUTERONES Adjusts ESVO_Sn to the highest voltage for a one. 0xE = ES_INNERONES Adjusts ESVO_Sn to the lowest voltage for a one. 0xF = RESERVED

ADVANCE INFORMATION

8.3.9.3 ESPO Register (Offset = 0x1F2) [Reset = 0x00]

ESPO is shown in Table 8-210.

Return to the Summary Table.

Table 8-210. ESPO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	
6-0	ESPO	R/W	0x0	Eye-scan phase offset for all lanes. This adjusts the sampling instant of the eye-scan sampler compared to the normal sampler. This is a signed value from -64 to +63 and the step size is 1/32th of a UI. Note: Only change this register while ESRUN=0.

8.3.9.4 ESVO Register (Offset = 0x1F3) [Reset = 0x00]

ESVO is shown in Table 8-211.

Return to the Summary Table.

Table 8-211. ESVO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5-0	ESVO	R/W	0x0	Eye-scan voltage offset for all lanes. This adjusts the voltage threshold of the eye-scan sampler. This is a signed value from -32 to +31. The step size is about 10mV (giving an adjustment range of about -320mV to +310mV). This field is ignored for eye-scan modes that adjust the voltage offset automatically and return a result on ESVO_S[n]. Note: Only change this register while ESRUN=0.

8.3.9.5 ESBSEL Register (Offset = 0x1F4) [Reset = 0x00]

ESBSEL is shown in Table 8-212.

Return to the Summary Table.

Table 8-212. ESBSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	
4-0	ESBSEL	R/W	0x0	Eye-scan only runs on every 32th bit (the PHY bus width is 32 bits). This field specifies which bit position the eye-scan runs on (valid range is 0 to 31). Eye-scans may be run with all possible values of ESBSEL and the results combined. Alternatively, results can be kept separate to see the effects of any duty cycle distortion / repetitive jitter. Note: Only change this register while ESRUN=0.

8.3.9.6 ECOUNT_CLR Register (Offset = 0x1F5) [Reset = 0x00]

ECOUNT_CLR is shown in Table 8-213.

Return to the Summary Table.

Table 8-213. ECOUNT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	ECOUNT_CLR	R/W	0x0	Program this to a 1 and then to 0 to clear the ECOUNT counters.

8.3.10 SerDes_Lane_Status Registers

Table 8-214 lists the memory-mapped registers for the SerDes_Lane_Status registers. All register offset addresses not listed in Table 8-214 should be considered as reserved locations and the register contents should not be modified.

Table 8-214. SERDES_LANE_STATUS Registers

Offset	Acronym	Register Name	Section
0x218	PHY_LANE		Section 8.3.10.1
0x219	PHY_SSEL		Section 8.3.10.2
0x21A	PHY_STATUS		Section 8.3.10.3

Complex bit access types are encoded to fit into small table cells. Table 8-215 shows the codes that are used for access types in this section.

Table 8-215. SerDes_Lane_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.10.1 PHY_LANE Register (Offset = 0x218) [Reset = 0x00]

PHY_LANE is shown in Table 8-216.

Return to the Summary Table.

Table 8-216. PHY_LANE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	PHY_LANE	R/W	0x0	Specifies which physical PHY lane is selected for reading status data back via the PHY_STATUS register.

8.3.10.2 PHY_SSEL Register (Offset = 0x219) [Reset = 0x00]

PHY_SSEL is shown in Table 8-217.

Return to the Summary Table.

Table 8-217. PHY_SSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PHY_SSEL	R/W	0x0	Specifies which status field is returned on the PHY_STATUS register

ADVANCE INFORMATION

8.3.10.3 PHY_STATUS Register (Offset = 0x21A) [Reset = 0xXXXX]

PHY_STATUS is shown in Table 8-218.

Return to the Summary Table.

Table 8-218. PHY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHY_STATUS	R	X	Returns status information from a physical lane. Before reading this register, program PHY_LANE to select a physical lane and program PHY_SSEL to choose which type of data to return. Refer to Serdes PHY Status section

8.3.11 SerDes_PLL Registers

Table 8-219 lists the memory-mapped registers for the SerDes_PLL registers. All register offset addresses not listed in Table 8-219 should be considered as reserved locations and the register contents should not be modified.

Table 8-219. SERDES_PLL Registers

Offset	Acronym	Register Name	Section
0x228	SPLL_STATUS		Section 8.3.11.1
0x229	SPLL_STATUS2		Section 8.3.11.2

Complex bit access types are encoded to fit into small table cells. Table 8-220 shows the codes that are used for access types in this section.

Table 8-220. SerDes_PLL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.3.11.1 SPLL_STATUS Register (Offset = 0x228) [Reset = 0x0X]

SPLL_STATUS is shown in Table 8-221.

Return to the Summary Table.

Table 8-221. SPLL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	SPLL_LOCK_LOST	R/W1C	X	This bit is set whenever the LOCK signal from the SPLL is low. This bit is sticky (remains set even if the SPLL acquires lock). Write a 1 to clear. This is for debug purposes and allows the SPI to monitor if the SPLL loses lock even briefly.

8.3.11.2 SPLL_STATUS2 Register (Offset = 0x229) [Reset = 0xXX]

SPLL_STATUS2 is shown in Table 8-222.

Return to the Summary Table.

Table 8-222. SPLL_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	SPLL_NO_LOCK	R	X	This indicates that the SPLL completed calibration, but was not able to atain or maintain a steady lock. This can also occur if lock is achieved, but then persistently lost (possibly due to a change in reference clock frequency).

Table 8-222. SPLL_STATUS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPLL_CORE_GAP	R	X	Returns a 1 if the SPLL detected a frequency gap between cores. If this occurs, there may be a fault in the SPLL.
3	SPLL_REF_SLOW	R	X	Returns a 1 if the SPLL reference clock is too slow for the SPLL to lock. If this occurs, verify the SPLL programming (REFDIV and MPY).
2	SPLL_REF_FAST	R	X	Returns a 1 if the SPLL reference clock is too fast for the SPLL to lock. If this occurs, verify the SPLL programming (REFDIV and MPY).
1	SPLL_VCAL_DONE	R	X	Returns a 1 to indicate that the SPLL calibration is completed. Calibration will occur after SYS_EN is set while JESD_M is non-zero and VCAL_EN=1.
0	RESERVED	R	0x0	Reserved

8.3.12 DAC_and_Analog_Configuration Registers

Table 8-223 lists the memory-mapped registers for the DAC_and_Analog_Configuration registers. All register offset addresses not listed in Table 8-223 should be considered as reserved locations and the register contents should not be modified.

Table 8-223. DAC_AND_ANALOG_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
0x280	CURRENT_2X		Section 8.3.12.1
0x2A0	DACA_CURRENT		Section 8.3.12.2
0x2A1	DACB_CURRENT		Section 8.3.12.3
0x2AF	CS_AMP_FILTER		Section 8.3.12.4
0x2B0	EXTREF_EN		Section 8.3.12.5
0x2C0	NOISEREDUCE_EN0		Section 8.3.12.6
0x2C1	NOISEREDUCE_EN1		Section 8.3.12.7
0x2CF	DAC_OFS_CHG_BLK		Section 8.3.12.8

Complex bit access types are encoded to fit into small table cells. Table 8-224 shows the codes that are used for access types in this section.

Table 8-224. DAC_and_Analog_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.12.1 CURRENT_2X Register (Offset = 0x280) [Reset = 0x00]

CURRENT_2X is shown in Table 8-225.

Return to the Summary Table.

Table 8-225. CURRENT_2X Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	CURRENT_2X_EN	R/W	0x0	0x0 = Enables 2x current mode for both DACs. 0x1 = Disables 2x current mode for both DACs.

8.3.12.2 DACA_CURRENT Register (Offset = 0x2A0) [Reset = 0x0F]

DACA_CURRENT is shown in Table 8-226.

Return to the Summary Table.

Table 8-226. DACA_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	COARSE_CUR_A_SLEEP	R/W	0x0	Coarse current control for DACA in sleep mode
3-0	COARSE_CUR_A	R/W	0xF	Coarse current control for DACA in active mode

8.3.12.3 DACB_CURRENT Register (Offset = 0x2A1) [Reset = 0x0F]

DACB_CURRENT is shown in Table 8-227.

Return to the Summary Table.

Table 8-227. DACB_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	COARSE_CUR_B_SLEEP	R/W	0x0	Coarse current control for DACB in sleep mode
3-0	COARSE_CUR_B	R/W	0xF	Coarse current control for DACB in active mode

8.3.12.4 CS_AMP_FILTER Register (Offset = 0x2AF) [Reset = 0x00]

CS_AMP_FILTER is shown in Table 8-228.

Return to the Summary Table.

Table 8-228. CS_AMP_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-2	CS_AMP_FILTER1	R/W	0x0	Adjusts the cutoff frequency of a low-pass filter in the current source biasing path for DACB. The higher the setting, the lower the bandwidth in the current source path which supresses the 1/f noise, but startup time is longer. 0x0 = cutoff at 20KHz (default) 0x1 = cutoff at 4KHz 0x2 = cutoff at 800Hz 0x3 = cutoff at 1Hz
1-0	CS_AMP_FILTER0	R/W	0x0	Adjusts the cutoff frequency of a low-pass filter in the current source biasing path for DACA. see CS_AMP_FILTER1.

8.3.12.5 EXTREF_EN Register (Offset = 0x2B0) [Reset = 0x00]

EXTREF_EN is shown in Table 8-229.

Return to the Summary Table.

Table 8-229. EXTREF_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	EXTREF_EN	R/W	0x0	Enables external reference

8.3.12.6 NOISEREDUCE_EN0 Register (Offset = 0x2C0) [Reset = 0xFF]

NOISEREDUCE_EN0 is shown in Table 8-230.

Return to the Summary Table.

Table 8-230. NOISEREDUCE_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NOISEREDUCE_IO18_EN	R/W	0x3	Reduces noise on the 1.8V VDDIO supply.
5	NOISEREDUCE_CLKDRV_DACB_EN	R/W	0x1	Reduces noise on the DACB Clock Driver supplies (AVDDCLK).
4	NOISEREDUCE_CLKDRV_DACA_EN	R/W	0x1	Reduces noise on the DACA Clock Driver supplies (AVDDCLK).
3-2	NOISEREDUCE_MUX_DACB_EN	R/W	0x3	Reduces noise on the DACB MUX supplies. Set both bits to the same value.
1-0	NOISEREDUCE_MUX_DACA_EN	R/W	0x3	Reduces noise on the DACA MUX supplies. Set both bits to the same value.

8.3.12.7 NOISEREDUCE_EN1 Register (Offset = 0x2C1) [Reset = 0x0F]

NOISEREDUCE_EN1 is shown in Table 8-231.

Return to the Summary Table.

Table 8-231. NOISEREDUCE_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-2	NOISEREDUCE_SWDRV_DACB_EN	R/W	0x3	Reduces noise on the DACB Switch Driver supplies. Set both bits to the same value.
1-0	NOISEREDUCE_SWDRV_DACA_EN	R/W	0x3	Reduces noise on the DACA Switch Driver supplies. Set both bits to the same value.

8.3.12.8 DAC_OFS_CHG_BLK Register (Offset = 0x2CF) [Reset = 0x00]

DAC_OFS_CHG_BLK is shown in Table 8-232.

Return to the Summary Table.

Table 8-232. DAC_OFS_CHG_BLK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	DAC_OFS_CHG_BLK	R/W	0x0	When set, changes to DAC_OFS[n] are not propagated to the high-speed clocks and both DACs continue to use their current value. When this is changed from 1 to 0 the new DAC_OFS[n] values will be applied to both DACs. There can be a small time offset when the new values are applied to each DAC (10's of CLK cycles).

8.3.13 Datapath Registers

Table 8-233 lists the memory-mapped registers for the Datapath registers. All register offset addresses not listed in Table 8-233 should be considered as reserved locations and the register contents should not be modified.

Table 8-233. DATAPATH Registers

Offset	Acronym	Register Name	Section
2E0h	DSP_MODE		Go
2E2h	DSP_L		Go
2E3h	DSP_GAIN0		Go
2E4h	DSP_GAIN1		Go
2E5h	DSP_GAIN2		Go
2E6h	DSP_GAIN3		Go
2E7h	DSP_FORMAT		Go
2E8h	DAC_SRC		Go
2E9h	DAC_SRC_ALT		Go
2EAh	MXMODE		Go
2EBh	TRUNC_HLSB		Go
2ECh	DAC_DLY0		Go
2EDh	DAC_DLY1		Go
2EEh	DAC_INV		Go

Complex bit access types are encoded to fit into small table cells. Table 8-234 shows the codes that are used for access types in this section.

Table 8-234. Datapath Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.13.1 DSP_MODE Register (Offset = 2E0h) [Reset = 0000h]

Return to the Summary Table.

Table 8-235. DSP_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	

Table 8-235. DSP_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	DSP_MODE3	R/W	0h	DSP_MODE3 field defines the operational mode of DSP channel 3. Note: Note: When all DSPs are disabled, the part automatically activates Bypass Mode (JESD samples are sent to the DACs). There is no crossbar between the JESD interface and the DSP channels, it is important to assign DSP modes that require JESD samples to the lower DSP channel numbers (channel 0 thru JESD_M/2 – 1). Be sure to also program JESD_M appropriately. Use JESD_M=0 if no DSPs require JESD samples. See DSP mode. Note: When DSP_L is configured for 4x or 6x interpolation, only DSP channel 0 and 1 can operate in DUC mode. The other channels must use a different mode (or be disabled). Note: This register should only be changed when SYS_EN=0. 0h = DSP0 is disabled (unused) 1h = DUC mode – Sends JESD samples through the DUC 2h = DDS SPI mode – Uses DDS values from FREQ, PHASE, and AMP registers (JESD samples not used) 3h = DDS Vector mode – Uses DDS vector player to create DAC samples (JESD samples not used) 4h = DDS Stream mode– Uses DDS parameters streamed from JESD interface 5h = Reserved 6h = Reserved 7h = Reserved
11	RESERVED	R	0h	
10-8	DSP_MODE2	R/W	0h	DSP_MODE2 field defines the operational mode of DSP channel 2 per table for DSP_MODE3
7	RESERVED	R	0h	
6-4	DSP_MODE1	R/W	0h	DSP_MODE1 field defines the operational mode of DSP channel 1 per table for DSP_MODE3
3	RESERVED	R	0h	
2-0	DSP_MODE0	R/W	0h	DSP_MODE0 field defines the operational mode of DSP channel 0 per table for DSP_MODE3

ADVANCE INFORMATION

8.3.13.2 DSP_L Register (Offset = 2E2h) [Reset = 00h]

Return to the Summary Table.

Table 8-236. DSP_L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	

Table 8-236. DSP_L Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DSP_L	R/W	0h	Specifies the DUC interpolation factor or the DDS Up-sampling Factor. DSP_L applies only when JESD_M is greater than 0 and at least one DSP channel is enabled (DSP_MODE). This typically means one or more DSP channels are configured for DUC mode or DDS Stream mode (see DSP_MODE). However, the JESD interface can also be used soley to provide a trigger for DSPs operating in DDS-SPI or DDS-Vector mode. All DSP channels share one setting. all settings 0x3-0xF support DUC, DDS-SPI, DDS-Vector modes. Note: If DSP channels are operating in various modes, you must select a DSP_L setting that supports all the active modes. Note: This register should only be changed when SYS_EN=0. 0h = RESERVED 1h = RESERVED 2h = RESERVED 3h = **[INT_4X]** 4x 4h = **[INT_6X]** 6x 5h = **[INT_8X]** 8x 6h = **[INT_12X]** 12x 7h = **[INT_16X]** 16x (also for DDS Streaming Upsample Factor) 8h = **[INT_24X]** 24x 9h = **[INT_32X]** 32x (also for DDS Streaming Upsample Factor) Ah = **[INT_48X]** 48x Bh = **[INT_64X]** 64x (also for DDS Streaming Upsample Factor) Ch = **[INT_96X]** 96x Dh = **[INT_128X]** 128x Eh = **[INT_192X]** 192x Fh = **[INT_256X]** 256x

8.3.13.3 DSP_GAIN0 Register (Offset = 2E3h) [Reset = 00h]

Return to the Summary Table.

Table 8-237. DSP_GAIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6-4	DSP_GAIN0_COARSE	R/W	0h	Adjusts the output coarse gain of DSP channel 0. COARSE_GAIN = 2^{-VALUE}
3-0	DSP_GAIN0_FINE	R/W	0h	Adjusts the output fine gain of DSP channel 0. FINE_GAIN = 1 - (VALUE/32)

8.3.13.4 DSP_GAIN1 Register (Offset = 2E4h) [Reset = 00h]

Return to the Summary Table.

Table 8-238. DSP_GAIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6-4	DSP_GAIN1_COARSE	R/W	0h	Adjusts the output coarse gain of DSP channel 1. COARSE_GAIN = 2^{-VALUE}
3-0	DSP_GAIN1_FINE	R/W	0h	Adjusts the output fine gain of DSP channel 1. FINE_GAIN = 1 - (VALUE/32)

8.3.13.5 DSP_GAIN2 Register (Offset = 2E5h) [Reset = 00h]

Return to the Summary Table.

Table 8-239. DSP_GAIN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6-4	DSP_GAIN2_COARSE	R/W	0h	Adjusts the output coarse gain of DSP channel 2. COARSE_GAIN = 2^{-VALUE}
3-0	DSP_GAIN2_FINE	R/W	0h	Adjusts the output fine gain of DSP channel 2. FINE_GAIN = 1 - (VALUE/32)

8.3.13.6 DSP_GAIN3 Register (Offset = 2E6h) [Reset = 00h]

Return to the Summary Table.

Table 8-240. DSP_GAIN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6-4	DSP_GAIN3_COARSE	R/W	0h	Adjusts the output coarse gain of DSP channel 3. COARSE_GAIN = 2^{-VALUE}
3-0	DSP_GAIN3_FINE	R/W	0h	Adjusts the output fine gain of DSP channel 3. FINE_GAIN = 1 - (VALUE/32)

8.3.13.7 DSP_FORMAT Register (Offset = 2E7h) [Reset = 00h]

Return to the Summary Table.

Table 8-241. DSP_FORMAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	DSP_FORMAT	R/W	0h	Choose real or imaginary output when the DSPs are configured for DUC mode or a DDS Mode (see DSP_MODE). Note: This register affects DUC and DDS modes. 0h = **[DSP_OUT_REAL]** DSP outputs are real (DSP mixer converts complex to real by discarding the imaginary part). Up to 4 DSPs can be enabled. 1h = **[DSP_OUT_COMP]** DSP outputs are complex. Up to 2 DSPs can be enabled (DSP0 and DSP1). The mixer in DSP2 generates the imaginary samples for DSP0, so the user should bind a DAC to DSP2 using DAC_SRC. Similarly, if DSP1 is enabled, the mixer in DSP3 generates the imaginary samples for DSP1, so the user should bind a DAC to DSP3 to access those samples if desired. See Complex Output Support.

8.3.13.8 DAC_SRC Register (Offset = 2E8h) [Reset = 21h]

Return to the Summary Table.

Table 8-242. DAC_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DAC_SRC1	R/W	2h	In bypass mode (see DSP_MODE), DAC_SRC1 selects which input stream is sent to DACB. In DUC or DDS modes, DAC_SRC1 controls which DSP (DUC/DDS) outputs are routed (summed) to DACB. See **Section DAC Source Selection**
3-0	DAC_SRC0	R/W	1h	see DAC_SRC1

ADVANCE INFORMATION

8.3.13.9 DAC_SRC_ALT Register (Offset = 2E9h) [Reset = 00h]

Return to the Summary Table.

Table 8-243. DAC_SRC_ALT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

8.3.13.10 MXMODE Register (Offset = 2EAh) [Reset = 00h]

Return to the Summary Table.

Table 8-244. MXMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6-4	MXMODE1	R/W	0h	Specify the DAC Output Mode for DACB. 0h = **[NRZ]** Normal mode (non-return-to-zero or NRZ) (sinc nulls at n*FS) 1h = **[RF]** RF Mode (return to inverse or RTI) (sinc nulls at DC and 2n*FS) 2h = **[RTZ]** Return-to-Zero (RTZ) (sinc nulls at 2n*FS) 3h = **[DES2XL]** DES2XL – Samples provided by the DES interpolator 4h = **[DES2XH]** DES2XH – Samples provided by the DES interpolator (high-pass mode) 5h = RESERVED 6h = **[DISABLED]** Disabled - DACB is disabled 7h = RESERVED
3	RESERVED	R	0h	
2-0	MXMODE0	R/W	0h	See MXMODE0

8.3.13.11 TRUNC_HLSB Register (Offset = 2EBh) [Reset = 00h]

Return to the Summary Table.

Table 8-245. TRUNC_HLSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	TRUNC_HLSB	R/W	0h	When the output resolution of the DAC is less than 16-bits, the output is truncated to the proper resolution. If this bit is set, a 1/2 LSB offset is added to the truncated value to reduce the average offset introduced by truncation.

8.3.13.12 DAC_DLY0 Register (Offset = 2ECh) [Reset = 00h]

Return to the Summary Table.

Table 8-246. DAC_DLY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	DAC_DLY0_EN	R/W	0h	0h = Disable adjustable delay for DACA (default) 1h = Enable adjustable delay for DACA

Table 8-246. DAC_DLY0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	DAC_DLY0_VAL	R/W	0h	Adjusts the delay for DACA. The added delay (in DACCLK cycles) is 64 + DAC_DLY0_VAL. Note: Changing this register can produce glitches on the DAC output unless the sample stream is static during the change.

8.3.13.13 DAC_DLY1 Register (Offset = 2EDh) [Reset = 00h]

Return to the Summary Table.

Table 8-247. DAC_DLY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	DAC_DLY1_EN	R/W	0h	0h = Disable adjustable delay for DACB (default) 1h = Enable adjustable delay for DACB
4-0	DAC_DLY1_VAL	R/W	0h	Adjusts the delay for DACB. The added delay (in DACCLK cycles) is 64 + DAC_DLY1_VAL. Note: Changing this register can produce glitches on the DAC output unless the sample stream is static during the change.

8.3.13.14 DAC_INV Register (Offset = 2EEh) [Reset = 00h]

Return to the Summary Table.

Table 8-248. DAC_INV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	DAC_INV1	R/W	0h	DAC1 output is inverted when set
0	DAC_INV0	R/W	0h	DAC0 output is inverted when set

8.3.14 NCO_and_Mixer Registers

Table 8-249 lists the memory-mapped registers for the NCO_and_Mixer registers. All register offset addresses not listed in Table 8-249 should be considered as reserved locations and the register contents should not be modified.

Table 8-249. NCO_AND_MIXER Registers

Offset	Acronym	Register Name	Section
0x300	NCO_CNTL		Section 8.3.14.1
0x301	NCO_CONT		Section 8.3.14.2
0x303	NCO_AR		Section 8.3.14.3
0x304	STREAM_MODE		Section 8.3.14.4
0x305	NCO_SS		Section 8.3.14.5
0x306	NCO_SQ_MODE		Section 8.3.14.6
0x307	NCO_SQ_EN		Section 8.3.14.7
0x308	NCO_SQ_SEL		Section 8.3.14.8
0x320	FREQ_0		Section 8.3.14.9
0x328	FREQ_1		Section 8.3.14.10
0x330	FREQ_2		Section 8.3.14.11
0x338	FREQ_3		Section 8.3.14.12
0x340	PHASE_0		Section 8.3.14.13
0x342	PHASE_1		Section 8.3.14.14
0x344	PHASE_2		Section 8.3.14.15
0x346	PHASE_3		Section 8.3.14.16
0x348	AMP_0		Section 8.3.14.17
0x34A	AMP_1		Section 8.3.14.18
0x34C	AMP_2		Section 8.3.14.19
0x34E	AMP_3		Section 8.3.14.20
0x360	SLEW0		Section 8.3.14.21
0x361	SLEW1		Section 8.3.14.22
0x362	SLEW2		Section 8.3.14.23
0x363	SLEW3		Section 8.3.14.24
0x364	DUTY_CYCLE0		Section 8.3.14.25
0x366	DUTY_CYCLE1		Section 8.3.14.26
0x368	DUTY_CYCLE2		Section 8.3.14.27
0x36A	DUTY_CYCLE3		Section 8.3.14.28
0x370	FREQ_R_0		Section 8.3.14.29
0x378	FREQ_R_1		Section 8.3.14.30
0x380	FREQ_R_2		Section 8.3.14.31
0x388	FREQ_R_3		Section 8.3.14.32
0x390	PHASE_R_0		Section 8.3.14.33
0x392	PHASE_R_1		Section 8.3.14.34
0x394	PHASE_R_2		Section 8.3.14.35
0x396	PHASE_R_3		Section 8.3.14.36
0x398	AMP_R_0		Section 8.3.14.37
0x39A	AMP_R_1		Section 8.3.14.38
0x39C	AMP_R_2		Section 8.3.14.39
0x39E	AMP_R_3		Section 8.3.14.40

Complex bit access types are encoded to fit into small table cells. Table 8-250 shows the codes that are used for access types in this section.

Table 8-250. NCO_and_Mixer Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.14.1 NCO_CNTL Register (Offset = 0x300) [Reset = 0x00]

NCO_CNTL is shown in Table 8-251.

Return to the Summary Table.

Table 8-251. NCO_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	
2	NCO_SC	R/W	0x0	Self-Coherent NCO Mode: If this bit is set, all NCOs use the reference counter from the NCO in DDS/DUC channel 0. This is typically used along with the NCO_SS register. This only impacts phase-coherent mode (NCO_CONT=0).
1	RESERVED	R	0x0	
0	NCO_EN	R/W	0x0	When set, DUC samples are mixed with the NCO. When cleared, the mixer is bypassed. This only applies to DUC mode and has no effect on DDS modes (see DSP_MODE).

8.3.14.2 NCO_CONT Register (Offset = 0x301) [Reset = 0x00]

NCO_CONT is shown in Table 8-252.

Return to the Summary Table.

Table 8-252. NCO_CONT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	NCO_CONT	R/W	0x0	For each bit NCO_CONT[n], if set, NCOn operates in phase-continuous mode. This means that frequency changes occur without seeding the phase accumulator. If the bit is clear, NCOn operates in phase-coherent mode. During frequency changes, the phase accumulator is seeded from a master counter. This means that if changing from frequency A to B and then back to A, the phase returns to what it would have been if the change never occurred. NCO_CONT only applies to DUC mode and DDS SPI mode (see DSP_MODE).

8.3.14.3 NCO_AR Register (Offset = 0x303) [Reset = 0x00]

NCO_AR is shown in Table 8-253.

Return to the Summary Table.

Table 8-253. NCO_AR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	NCO_AR	R/W	0x0	For each bit NCO_AR[n], if set, the accumulator for NCOn will be reset on every trigger event directed to DSPn. NCO_AR only applies to DUC mode and DDS Stream Mode (see DSP_MODE). See DSP Triggering

8.3.14.4 STREAM_MODE Register (Offset = 0x304) [Reset = 0x00]

STREAM_MODE is shown in Table 8-254.

Return to the Summary Table.

Table 8-254. STREAM_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	STREAM_MODE3	R/W	0x0	STREAM_MODEn configures the streaming mode for DSPn. This applies only to DSP channels configured for DDS Stream Mode. Note: This register should only be changed when SYS_EN=0. 0x0 = Dynamically stream frequency/phase/amplitude using the sdata[0] control bit. 0x1 = Only stream frequency samples (sdata[0] is the frequency LSB). Phase and amplitude are set by the PHASE[n] and AMP[n] registers. 0x2 = Only stream phase/amplitude samples (sdata[0] is ignored). Frequency is set by the FREQ[n] register. 0x3 = Reserved
5-4	STREAM_MODE2	R/W	0x0	see STREAM_MODE3
3-2	STREAM_MODE1	R/W	0x0	see STREAM_MODE3
1-0	STREAM_MODE0	R/W	0x0	see STREAM_MODE3

8.3.14.5 NCO_SS Register (Offset = 0x305) [Reset = 0x00]

NCO_SS is shown in Table 8-255.

Return to the Summary Table.

Table 8-255. NCO_SS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	

Table 8-255. NCO_SS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NCO_SS	R/W	0x0	If this bit is set, all NCOs will continuously self-synchronize every 256 DAC clock cycles. Most applications will not use this, but in a radiation environment, the user can set NCO_SS to continuously transfer the upset-immune AMP, FREQ and PHASE register values to the internal (non-immune) registers inside the NCOs. This is helpful for generating tones under radiation without the need for an external, periodic synchronization source (such as SYSREF). NCO_SS can be changed while the NCOs are operating (SYS_EN=1). To write a new FREQ, AMP, or PHASE value, clear NCO_SS first, and then set it again after the new values are written. All values go into effect simultaneously on all NCOs. The user should ensure that NCO_AR=0 whenever NCO_SS=1 (otherwise the NCO accumulators and/or reference counters keep getting reset). If the user also sets NCO_SC=1 and NCO_CONT=0, then all four NCOs will maintain coherency with each other under radiation (but coherence with an external component is not guaranteed). Each NCO accumulator is continuously seeded from the reference counter in DUC/DDS channel 0. This feature can be used to generate coherent harmonic tones to cancel out harmonic distortion in the DAC. This can be used for DUC mode, DDS SPI mode, and DDS Stream mode.

8.3.14.6 NCO_SQ_MODE Register (Offset = 0x306) [Reset = 0x00]

NCO_SQ_MODE is shown in Table 8-256.

Return to the Summary Table.

Table 8-256. NCO_SQ_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	NCO_SQ_MODE	R/W	0x0	For each bit NCO_SQ_MODE[n], if set, the output of NCOn will produce a square waveform instead of a sine/cosine waveform. NCO_SQ_MODE only applies to DDS modes (see DSP_MODE). In this mode, the SLEW and DUTY_CYCLE registers can be used to customize the slew rate and duty cycle of the waveform. See NCO Square Wave Mode. If a DSP channel is configured to produce a square wave, the user should bind that DSP exclusively to a DAC output (i.e. do not sum any other DSP channels into the same DAC). Note: This register should only be changed when SYS_EN=0.

8.3.14.7 NCO_SQ_EN Register (Offset = 0x307) [Reset = 0x00]

NCO_SQ_EN is shown in Table 8-257.

Return to the Summary Table.

Table 8-257. NCO_SQ_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	NCO_SQ_EN	R/W	0x0	If NCO_SQ_SELn = 0, then NCO_SQ_EN[n] acts as the enable signal for the square wave output of NCOn. See Square Wave Enable.

8.3.14.8 NCO_SQ_SEL Register (Offset = 0x308) [Reset = 0x0000]

NCO_SQ_SEL is shown in Table 8-258.

Return to the Summary Table.

Table 8-258. NCO_SQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	
14-12	NCO_SQ_SEL3	R/W	0x0	NCO_SQ_SELn selects which pin or register will act as the waveform enable for NCOn. Applies only to NCO Square Wave Mode. See also Square Wave Enable. Note 1: These settings always uses a physical TRIG pin, even if SYNCB_PIN_FUNC is assigning SYNCB as an alternate input for a TRIG pin. Note 2: The SYNCB input is active high in this mode. When using NCO_SQ_SELn=5, ensure that JENC=1 and SYNCB_PIN_FUNC=0. 0x0 = register bit (default) 0x1 = TRIG0 pin (note 1) 0x2 = TRIG1 pin (note 1) 0x3 = TRIG2 pin (note 1) 0x4 = TRIG3 pin (note 1) 0x5 = SYNCB pin (note 2) 0x6 = Reserved 0x7 = Reserved
11	RESERVED	R	0x0	
8	RESERVED	R	0x0	
10-8	NCO_SQ_SEL2	R/W	0x0	See NCO_SQ_SEL3
7	RESERVED	R	0x0	
6-4	NCO_SQ_SEL1	R/W	0x0	See NCO_SQ_SEL3
3	RESERVED	R	0x0	
2-0	NCO_SQ_SEL0	R/W	0x0	See NCO_SQ_SEL3

8.3.14.9 FREQ_0 Register (Offset = 0x320) [Reset = 0x0000000000000000]

FREQ_0 is shown in Table 8-259.

Return to the Summary Table.

Table 8-259. FREQ_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ[0]	R/W	0x0	Specifies the frequency for NCO0. Used in DUC mode, DDS SPI mode, and DDS Stream (phase) mode. The NCO frequency (F_{NCO}) is: $F_{NCO} = FREQ[0] * 2^{-64} * F_{DACCLK}$ F_{DACCLK} is the sample frequency of the DAC. FREQ[0] is the integer value of this register. This register can be interpreted as signed or unsigned (both interpretations are valid). Use this equation to determine the value to program: $FREQ[0] = 2^{64} * F_{NCO} / F_{DACCLK}$ Note: Changes to this register do not take effect until DSP0 receives a trigger (see DSP Triggering). Note: FREQ[0] should not be updated inside a window of +-320 DAC cycles around the initiation of a trigger event on DSP0.

8.3.14.10 FREQ_1 Register (Offset = 0x328) [Reset = 0x0000000000000000]

FREQ_1 is shown in Table 8-260.

Return to the Summary Table.

Table 8-260. FREQ_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ[1]	R/W	0x0	See FREQ[0]

8.3.14.11 FREQ_2 Register (Offset = 0x330) [Reset = 0x0000000000000000]

FREQ_2 is shown in Table 8-261.

Return to the Summary Table.

Table 8-261. FREQ_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ[2]	R/W	0x0	See FREQ[0]

8.3.14.12 FREQ_3 Register (Offset = 0x338) [Reset = 0x0000000000000000]

FREQ_3 is shown in Table 8-262.

Return to the Summary Table.

Table 8-262. FREQ_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ[3]	R/W	0x0	See FREQ[0]

8.3.14.13 PHASE_0 Register (Offset = 0x340) [Reset = 0x0000]

PHASE_0 is shown in Table 8-263.

Return to the Summary Table.

Table 8-263. PHASE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE[0]	R/W	0x0	Specifies the phase for NCOn. Used in DUC mode, DDS SPI Mode, and DDS Stream (frequency) mode. This value is left justified into a 64-bit field and then added to the phase accumulator. The phase (in radians) is PHASE[0] * 2^{-16} * 2π. This register can be interpreted as signed or unsigned. Note: Changes to this register do not take effect until DSP0 receives a trigger (see DSP Triggering). Note: PHASE[0] should not be updated inside a window of +-320 DAC cycles around the initiation of a trigger event on DSP0.

8.3.14.14 PHASE_1 Register (Offset = 0x342) [Reset = 0x0001]

PHASE_1 is shown in Table 8-264.

Return to the Summary Table.

Table 8-264. PHASE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE[1]	R/W	0x1	See PHASE[0]

8.3.14.15 PHASE_2 Register (Offset = 0x344) [Reset = 0x0002]

PHASE_2 is shown in Table 8-265.

Return to the Summary Table.

Table 8-265. PHASE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE[2]	R/W	0x2	See PHASE[0]

8.3.14.16 PHASE_3 Register (Offset = 0x346) [Reset = 0x0003]

PHASE_3 is shown in Table 8-266.

Return to the Summary Table.

Table 8-266. PHASE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE[3]	R/W	0x3	See PHASE[0]

8.3.14.17 AMP_0 Register (Offset = 0x348) [Reset = 0x0000]

AMP_0 is shown in Table 8-267.

Return to the Summary Table.

Table 8-267. AMP_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP[0]	R/W	0x0	Specifies the DDS amplitude for DSP (DDS) channel 0. 16-bit signed value. This register applies to DDS SPI Mode and DDS Stream Mode (see DSP_MODE). For DDS Stream mode, this register is only used when AMP_STREAM=0. Note: Changes to this register do not take effect until DSP0 receives a trigger (see DSP Triggering). Note: AMP[0] should not be updated inside a window of +-320 DAC cycles around the initiation of a trigger event on DSP0.

8.3.14.18 AMP_1 Register (Offset = 0x34A) [Reset = 0x0000]

AMP_1 is shown in Table 8-268.

Return to the Summary Table.

Table 8-268. AMP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP[1]	R/W	0x0	See AMP[0]

8.3.14.19 AMP_2 Register (Offset = 0x34C) [Reset = 0x0000]

AMP_2 is shown in Table 8-269.

Return to the Summary Table.

Table 8-269. AMP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP[2]	R/W	0x0	See AMP[0]

8.3.14.20 AMP_3 Register (Offset = 0x34E) [Reset = 0x0000]

AMP_3 is shown in Table 8-270.

Return to the Summary Table.

Table 8-270. AMP_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP[3]	R/W	0x0	See AMP[0]

8.3.14.21 SLEW0 Register (Offset = 0x360) [Reset = 0x00]

SLEW0 is shown in Table 8-271.

Return to the Summary Table.

Table 8-271. SLEW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	SLEW0	R/W	0x0	Specifies the slew time for DDS square waves for DDS channel n. Applies only to NCO Square Wave Mode. The legal range is from 0 to 9. Higher values produce a faster slew rate (shorter slew time). The slew time in degrees is: $90*2^{-SLEW0}$ The slew time in radians is: $0.5\pi*2^{-SLEW}$ The slew time in seconds is: $0.25*2^{-SLEW0} / F_{NCO}$ Note: Changes to this register take effect when DSP0 receives a trigger (see DSP Triggering), or while the square wave output is gated low. See Square Wave Enable.

8.3.14.22 SLEW1 Register (Offset = 0x361) [Reset = 0x00]

SLEW1 is shown in Table 8-272.

Return to the Summary Table.

Table 8-272. SLEW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	SLEW1	R/W	0x0	See SLEW0

8.3.14.23 SLEW2 Register (Offset = 0x362) [Reset = 0x00]

SLEW2 is shown in Table 8-273.

Return to the Summary Table.

Table 8-273. SLEW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	SLEW2	R/W	0x0	See SLEW0

8.3.14.24 SLEW3 Register (Offset = 0x363) [Reset = 0x00]

SLEW3 is shown in Table 8-274.

Return to the Summary Table.

Table 8-274. SLEW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	SLEW3	R/W	0x0	See SLEW0

8.3.14.25 DUTY_CYCLE0 Register (Offset = 0x364) [Reset = 0x0800]

DUTY_CYCLE0 is shown in Table 8-275.

Return to the Summary Table.

Table 8-275. DUTY_CYCLE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	
11-0	DUTY_CYCLE0	R/W	0x800	Specifies the duty cycle for DDS square waves for DDS channel n. Applies only to NCO Square Wave Mode. The default value (2048 decimal) provides a duty cycle of 50%. The duty cycle (in percent) is equal to 100% * DUTY_CYCLE0/4096brbr#Note: Changes to this register take effect when DSP0 receives a trigger (see DSP Triggering), or while the square wave output is gated low. See Square Wave Enable.

8.3.14.26 DUTY_CYCLE1 Register (Offset = 0x366) [Reset = 0x0800]

DUTY_CYCLE1 is shown in Table 8-276.

Return to the Summary Table.

Table 8-276. DUTY_CYCLE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	
11-0	DUTY_CYCLE1	R/W	0x800	See DUTY_CLCYE0

8.3.14.27 DUTY_CYCLE2 Register (Offset = 0x368) [Reset = 0x0800]

DUTY_CYCLE2 is shown in Table 8-277.

Return to the Summary Table.

Table 8-277. DUTY_CYCLE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	
11-0	DUTY_CYCLE2	R/W	0x800	See DUTY_CLCYE0

8.3.14.28 DUTY_CYCLE3 Register (Offset = 0x36A) [Reset = 0x0800]

DUTY_CYCLE3 is shown in Table 8-278.

Return to the Summary Table.

Table 8-278. DUTY_CYCLE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	
11-0	DUTY_CYCLE3	R/W	0x800	See DUTY_CLCYE0

8.3.14.29 FREQ_R_0 Register (Offset = 0x370) [Reset = 0xXXXXXXXXXXXXXXXX]

FREQ_R_0 is shown in Table 8-279.

Return to the Summary Table.

Table 8-279. FREQ_R_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ_R[0]	R	X	This provides a readback of the frequency setting that is currently in use by DUC/DDS channel 0. The frequency could be determined by the FREQ register or another source. The value is sampled as each byte is read, so it may return incoherent data if the frequency changes during readback.

8.3.14.30 FREQ_R_1 Register (Offset = 0x378) [Reset = 0xXXXXXXXXXXXXXXXX]

FREQ_R_1 is shown in Table 8-280.

Return to the Summary Table.

Table 8-280. FREQ_R_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ_R[1]	R	X	See FREQ_R[0]

8.3.14.31 FREQ_R_2 Register (Offset = 0x380) [Reset = 0xXXXXXXXXXXXXXXXX]

FREQ_R_2 is shown in Table 8-281.

Return to the Summary Table.

Table 8-281. FREQ_R_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ_R[2]	R	X	See FREQ_R[0]

8.3.14.32 FREQ_R_3 Register (Offset = 0x388) [Reset = 0xXXXXXXXXXXXXXXXX]

FREQ_R_3 is shown in Table 8-282.

Return to the Summary Table.

Table 8-282. FREQ_R_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	FREQ_R[3]	R	X	See FREQ_R[0]

8.3.14.33 PHASE_R_0 Register (Offset = 0x390) [Reset = 0xXXXX]

PHASE_R_0 is shown in Table 8-283.

Return to the Summary Table.

Table 8-283. PHASE_R_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE_R[0]	R	X	This provides a readback of the phase setting that is currently in use by DUC/DDS channel 0. The phase could be determined by the PHASE register or another source. The value is sampled as each byte is read, so it may return incoherent data if the phase changes during readback.

8.3.14.34 PHASE_R_1 Register (Offset = 0x392) [Reset = 0xXXXX]

PHASE_R_1 is shown in Table 8-284.

Return to the Summary Table.

Table 8-284. PHASE_R_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE_R[1]	R	X	See PHASE_R[0]

8.3.14.35 PHASE_R_2 Register (Offset = 0x394) [Reset = 0xXXXX]

PHASE_R_2 is shown in Table 8-285.

Return to the Summary Table.

Table 8-285. PHASE_R_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE_R[2]	R	X	See PHASE_R[0]

8.3.14.36 PHASE_R_3 Register (Offset = 0x396) [Reset = 0xXXXX]

PHASE_R_3 is shown in Table 8-286.

Return to the Summary Table.

Table 8-286. PHASE_R_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASE_R[3]	R	X	See PHASE_R[0]

8.3.14.37 AMP_R_0 Register (Offset = 0x398) [Reset = 0xXXXX]

AMP_R_0 is shown in Table 8-287.

Return to the Summary Table.

Table 8-287. AMP_R_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP_R[0]	R	X	This provides a readback of the amplitude setting that is currently in use by DDS channel 0. Format is 16-bit signed. The amplitude could be determined by the AMP register or another source. In non-DDS modes, the return value is undefined. The value is sampled as each byte is read, so it may return incoherent data if the amplitude changes during readback.

8.3.14.38 AMP_R_1 Register (Offset = 0x39A) [Reset = 0xXXXX]

AMP_R_1 is shown in Table 8-288.

Return to the Summary Table.

Table 8-288. AMP_R_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP_R[1]	R	X	See Amp_R[0]

8.3.14.39 AMP_R_2 Register (Offset = 0x39C) [Reset = 0xXXXX]

AMP_R_2 is shown in Table 8-289.

Return to the Summary Table.

Table 8-289. AMP_R_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP_R[2]	R	X	See Amp_R[0]

8.3.14.40 AMP_R_3 Register (Offset = 0x39E) [Reset = 0xXXXX]

AMP_R_3 is shown in Table 8-290.

Return to the Summary Table.

Table 8-290. AMP_R_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	AMP_R[3]	R	X	See Amp_R[0]

8.3.15 Alarm Registers

Table 8-291 lists the memory-mapped registers for the Alarm registers. All register offset addresses not listed in Table 8-291 should be considered as reserved locations and the register contents should not be modified.

Table 8-291. ALARM Registers

Offset	Acronym	Register Name	Section
0x430	SYS_ALM		Section 8.3.15.1
0x431	ALM_MASK		Section 8.3.15.2
0x432	MUTE_MASK		Section 8.3.15.3
0x433	MUTE_REC		Section 8.3.15.4
0x434	ALARM_SEL		Section 8.3.15.5
0x435	OVR_STATUS		Section 8.3.15.6
0x436	OVR_MASK_SEL		Section 8.3.15.7

Complex bit access types are encoded to fit into small table cells. Table 8-292 shows the codes that are used for access types in this section.

Table 8-292. Alarm Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.3.15.1 SYS_ALM Register (Offset = 0x430) [Reset = 0x02]

SYS_ALM is shown in Table 8-293.

Return to the Summary Table.

Table 8-293. SYS_ALM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	JESD_LINK_DOWN_ALM	R/W1C	0x0	This bit is set any time LINK_UP transitions from 1 to 0 while SYS_EN=1.
6	JTIMER_EXPIRED_ALM	R/W1C	0x0	This bit is set if the JESD204C link has been down (DSP_MODE has JESD204C interface enabled, SYS_EN=1 , and LINK_UP=0) longer than allowed by JTIMER.
5	JESD_DI_ALM	R/W1C	0x0	This bit is set any time DI_FAULT is detected on an enabled lane. Applies only to 64b/66b modes.
4	OVR_ALM	R/W1C	0x0	This bit is set if a full-scale sample occurred in the datapath. Write 1 to clear the alarm. See also OVR_STATUS.
3-2	RESERVED	R	0x0	
1	SYSRST_ALM	R/W1C	0x1	This bit is set any time the chip is reset due to RESET, or SOFT_RESET.

Table 8-293. SYS_ALM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYSREF_ALM	R/W1C	0x0	This bit is set any time a SYSREF edge is detected at an incorrect alignment with respect to any active SYSREF-associated clock divider.

8.3.15.2 ALM_MASK Register (Offset = 0x431) [Reset = 0x00]

ALM_MASK is shown in Table 8-294.

Return to the Summary Table.

Table 8-294. ALM_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	JESD_LINK_DOWN_MASK	R/W	0x0	When set, alarms from the JESD_LINK_DOWN_ALM register are masked and will NOT impact the alarm output.
6	JTIMER_EXPIRED_MASK	R/W	0x0	When set, alarms from the JTIMER_EXPIRED_ALM register are masked and will NOT impact the alarm output.
5	JESD_DI_MASK	R/W	0x0	When set, alarms from the JESD_DI_ALM register and masked and will NOT impact the alarm output.
4	OVR_MASK	R/W	0x0	When set, alarms from the OVR_ALM register are masked and will not impact the alarm output.
3-1	RESERVED	R	0x0	
0	SYSREF_ALM_MASK	R/W	0x0	When set, alarms from the SYSREF_ALM register are masked and will not impact the alarm output.

8.3.15.3 MUTE_MASK Register (Offset = 0x432) [Reset = 0x21]

MUTE_MASK is shown in Table 8-295.

Return to the Summary Table.

Table 8-295. MUTE_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5	JESD_DI_MUTE_MASK	R/W	0x1	This register controls which alarms will cause the JESD204C transport layer output to be muted automatically. Unless a corresponding MUTE_REC bit is set, once the transport layer output is muted, the user will need to correct the problem and clear the alarm to cause the transport layer output to unmute (alternatively, the mute mask can be set to ignore the alarm and unmute the transport layer output). When DI_FAULT=1, the JESD204C transport layer output will mute according to JESD_DI_REC unless this bit is set.
4-1	RESERVED	R	0x0	
0	SYSREF_MUTE_MASK	R/W	0x1	This register controls which alarms will cause the JESD204C transport layer output to be muted automatically. Unless a corresponding MUTE_REC bit is set, once the transport layer output is muted, the user will need to correct the problem and clear the alarm to cause the transport layer output to unmute (alternatively, the mute mask can be set to ignore the alarm and unmute the transport layer output). Alarms from the SYSREF_ALM register will mute the JESD204C transport layer output unless this bit is set.

8.3.15.4 MUTE_REC Register (Offset = 0x433) [Reset = 0xA0]

MUTE_REC is shown in Table 8-296.

Return to the Summary Table.

Table 8-296. MUTE_REC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	
5	JESD_DI_REC	R/W	0x1	This register controls whether the JESD204C transport layer output will automatically unmute when the alarm condition goes away. This bit is only used if JESD_DI_MUTE_MASK=0. 0: JESD204C transport layer output will remain muted until the JESD_DI_ALM=0 1: JESD204C transport layer output will unmute automatically when DI_FAULT=0.
4-0	RESERVED	R	0x0	

8.3.15.5 ALARM_SEL Register (Offset = 0x434) [Reset = 0x00]

ALARM_SEL is shown in Table 8-297.

Return to the Summary Table.

Table 8-297. ALARM_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	ALARM_SEL	R/W	0x0	0x0 = The ALARM output asserts when any unmasked alarms are active (mission mode). See Alarm Generation. 0x1 = The ALARM pin outputs the trigger clock.

8.3.15.6 OVR_STATUS Register (Offset = 0x435) [Reset = 0x00]

OVR_STATUS is shown in Table 8-298.

Return to the Summary Table.

Table 8-298. OVR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	
5	OVR_DAC1	R/W1C	0x0	This bit is set if a full-scale sample is detected on DAC1. Write 1 to clear. Note: Refer to section Over Range Detection for possible causes of over-range. Note: Writing a 1 to the OVR_ALM register will clear all bits in this register. Note: The OVR_ALM register returns the bitwise-OR of OVR_STATUS, so if you clear all bits of OVR_STATUS, then OVR_ALM will also return 0.
4	OVR_DAC0	R/W1C	0x0	This bit is set if a full-scale sample is detected on DAC0. Write 1 to clear. See notes for OVR_DAC1.
3	OVR_DSP3	R/W1C	0x0	This bit is set if a full-scale sample is detected inside DSP3. Write 1 to clear. See notes for OVR_DAC1.
2	OVR_DSP2	R/W1C	0x0	This bit is set if a full-scale sample is detected inside DSP2. Write 1 to clear. See notes for OVR_DAC1.
1	OVR_DSP1	R/W1C	0x0	This bit is set if a full-scale sample is detected inside DSP1. Write 1 to clear. See notes for OVR_DAC1.

Table 8-298. OVR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OVR_DSP0	R/W1C	0x0	This bit is set if a full-scale sample is detected inside DSP0. Write 1 to clear. See notes for OVR_DAC1.

8.3.15.7 OVR_MASK_SEL Register (Offset = 0x436) [Reset = 0x00]

OVR_MASK_SEL is shown in Table 8-299.

Return to the Summary Table.

Table 8-299. OVR_MASK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	OVR_MASK_SEL	R/W	0x0	0x0 = The TRIG[4] pin does not mask over-range events. 0x1 = When the TRIG[4] pin is asserted high, over-range events are masked (they do not cause bits of OVR_STATUS to be set).

8.3.16 Fuse_Control Registers

Table 8-300 lists the memory-mapped registers for the Fuse_Control registers. All register offset addresses not listed in Table 8-300 should be considered as reserved locations and the register contents should not be modified.

Table 8-300. FUSE_CONTROL Registers

Offset	Acronym	Register Name	Section
0x600	FUSE_DONE		Section 8.3.16.1

Complex bit access types are encoded to fit into small table cells. Table 8-301 shows the codes that are used for access types in this section.

Table 8-301. Fuse_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.3.16.1 FUSE_DONE Register (Offset = 0x600) [Reset = 0xXX]

FUSE_DONE is shown in Table 8-302.

Return to the Summary Table.

Table 8-302. FUSE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	FUSE_DONE	R	X	Returns 1 when the fuse controller is idle. This means it has completed the fuse auto-load sequence or has completed the fuse auto-program sequence. When FUSE_DONE is 0 the user should not read or write any fuse-backed registers.

8.3.17 Fuse_Backed Registers

Table 8-303 lists the memory-mapped registers for the Fuse_Backed registers. All register offset addresses not listed in Table 8-303 should be considered as reserved locations and the register contents should not be modified.

Table 8-303. FUSE_BACKED Registers

Offset	Acronym	Register Name	Section
0x711	SPIN_ID		Section 8.3.17.1
0x723	DACA_CURRENT_FINE		Section 8.3.17.2
0x724	DACB_CURRENT_FINE		Section 8.3.17.3
0x727	DEM_ADJ		Section 8.3.17.4
0x729	DEM_DITH		Section 8.3.17.5
0x72A	DAC_OFS		Section 8.3.17.6
0x73E	DES_TRIM0		Section 8.3.17.7
0x73F	DES_TRIM1		Section 8.3.17.8

Complex bit access types are encoded to fit into small table cells. Table 8-304 shows the codes that are used for access types in this section.

Table 8-304. Fuse_Backed Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.17.1 SPIN_ID Register (Offset = 0x711) [Reset = 0xX0]

SPIN_ID is shown in Table 8-305.

Return to the Summary Table.

Table 8-305. SPIN_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	SPIN_ID	R	0x0	This register identifies the product version.

8.3.17.2 DACA_CURRENT_FINE Register (Offset = 0x723) [Reset = 0xXX]

DACA_CURRENT_FINE is shown in Table 8-306.

Return to the Summary Table.

Table 8-306. DACA_CURRENT_FINE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	

Table 8-306. DACA_CURRENT_FINE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	FINE_CUR_A	R/W	X	DACA fine current control. Default from fuse load with trim value. Can be use for small fullscale current adjustments.

8.3.17.3 DACB_CURRENT_FINE Register (Offset = 0x724) [Reset = 0xXX]

DACB_CURRENT_FINE is shown in Table 8-307.

Return to the Summary Table.

Table 8-307. DACB_CURRENT_FINE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	FINE_CUR_B	R/W	X	DACB fine current control. Default from fuse load with trim value. Can be use for small fullscale current adjustments.

8.3.17.4 DEM_ADJ Register (Offset = 0x727) [Reset = 0x00]

DEM_ADJ is shown in Table 8-308.

Return to the Summary Table.

Table 8-308. DEM_ADJ Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DEM_ADJ1	R/W	0x0	Adjust DEM behavior for single-edge data-independent DEM for DACB. This register has no effect unless DACB is configured for single-edge data-independent DEM. See DEM and Dither Section.
3-0	DEM_ADJ0	R/W	0x0	Adjust DEM behavior for single-edge data-independent DEM for DACA. This register has no effect unless DACA is configured for single-edge data-independent DEM. See DEM and Dither Section.

8.3.17.5 DEM_DITH Register (Offset = 0x729) [Reset = 0xXX]

DEM_DITH is shown in Table 8-309.

Return to the Summary Table.

Table 8-309. DEM_DITH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DEM1	R/W	X	0x0 = Enable single-edge, data-independent DEM for DACB 0x1 = Enable dual-edge, data-independent DEM for DACB 0x2 = RESERVED 0x3 = DEM disabled for DACB
5-4	DEM0	R/W	X	See DEM1
3-2	DITH1	R/W	X	0x0 = Enable single edge dithering for DACB 0x1 = Enable dual edge dithering for DACB 0x2 = RESERVED 0x3 = Dithering disabled for DACB
1-0	DITH0	R/W	X	See DITH1

8.3.17.6 DAC_OFS Register (Offset = 0x72A) [Reset = 0xXXXX]

DAC_OFS is shown in Table 8-310.

Return to the Summary Table.

ADVANCE INFORMATION

Table 8-310. DAC_OFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	
12-6	DAC_OFS[1]	R/W	X	Offset adjustment for DACB. The value in this register is added to the DACB output. This is a 2s complement, 13-bit signed value. The LSB weight is one DAC LSB. The value programmed into this register passes through a saturation function to limit the adjustment to what is possible. If dithering is enabled on DACB (see DITH1), DAC_OFS[1] is saturated to the range +/- 128. If dithering is disabled on DACB, the saturation range is +/- 3968. Default from trim value. See Offset Adjustment section.
5-0	DAC_OFS[0]	R/W	X	See DAC_OFS[1]

8.3.17.7 DES_TRIM0 Register (Offset = 0x73E) [Reset = 0x00]

DES_TRIM0 is shown in Table 8-311.

Return to the Summary Table.

Table 8-311. DES_TRIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DES_STEP0	R/W	0x0	Adjusts DES timing adjustment set size for DACA 0x0 = 1X 0x1 = 2X 0x2 = 4X 0x3 = Same as 0b10
5	DES_POL0	R/W	0x0	Changes DES timing adjustment polarity for DACA 0x0 = Positive 0x1 = Negative
4-0	DES_OFS0	R/W	0x0	DES timing offset value for DACA

8.3.17.8 DES_TRIM1 Register (Offset = 0x73F) [Reset = 0x00]

DES_TRIM1 is shown in Table 8-312.

Return to the Summary Table.

Table 8-312. DES_TRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DES_STEP1	R/W	0x0	Adjusts DES timing adjustment set size for DACB 0x0 = 1X 0x1 = 2X 0x2 = 4X 0x3 = Same as 0b10
5	DES_POL1	R/W	0x0	Changes DES timing adjustment polarity for DACB 0x0 = Positive 0x1 = Negative
4-0	DES_OFS1	R/W	0x0	DES timing offset value for DACB

8.3.18 DDS_Vector_Mode Registers

Table 8-313 lists the memory-mapped registers for the DDS_Vector_Mode registers. All register offset addresses not listed in Table 8-313 should be considered as reserved locations and the register contents should not be modified.

Table 8-313. DDS_VECTOR_MODE Registers

Offset	Acronym	Register Name	Section
0x800	DDS_BURST_0		Section 8.3.18.1
0x802	DDS_BURST_1		Section 8.3.18.2
0x804	DDS_BURST_2		Section 8.3.18.3
0x806	DDS_BURST_3		Section 8.3.18.4
0x808	DDS_IMODE		Section 8.3.18.5
0x809	DDS_SYM		Section 8.3.18.6
0x80A	DDS_HOLD		Section 8.3.18.7
0x80B	DDS_IDLE		Section 8.3.18.8
0x80C	DDS_INDEX0		Section 8.3.18.9
0x80D	DDS_INDEX1		Section 8.3.18.10
0x80E	DDS_INDEX2		Section 8.3.18.11
0x80F	DDS_INDEX3		Section 8.3.18.12
0x810	DDS_AMP2		Section 8.3.18.13
0xB20	DDS_VEC_n		Section 8.3.18.14

Complex bit access types are encoded to fit into small table cells. Table 8-314 shows the codes that are used for access types in this section.

Table 8-314. DDS_Vector_Mode Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.18.1 DDS_BURST_0 Register (Offset = 0x800) [Reset = 0x0000]

DDS_BURST_0 is shown in Table 8-315.

Return to the Summary Table.

Table 8-315. DDS_BURST_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DDS_BURST[0]	R/W	0x0	Trigger burst control for DDS channel n. In DDS Vector Mode, DDS_BURST defines how many additional times a DDS channel is triggered when it receives a trigger event (see Trigger Burst). The additional triggers are queued and the DDS behaves like it received DDS_BURST+1 triggers. The legal range of DDS_BURST is 0 to 65535. The user may change DDS_BURST while the DDS is enabled (SYS_EN=1), but must ensure that no trigger events occur during the SPI transaction, or for 50ns after the transaction is completed.

8.3.18.2 DDS_BURST_1 Register (Offset = 0x802) [Reset = 0x0000]

DDS_BURST_1 is shown in Table 8-316.

Return to the Summary Table.

Table 8-316. DDS_BURST_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DDS_BURST[1]	R/W	0x0	See description for DDS_BURST[0]

8.3.18.3 DDS_BURST_2 Register (Offset = 0x804) [Reset = 0x0000]

DDS_BURST_2 is shown in Table 8-317.

Return to the Summary Table.

Table 8-317. DDS_BURST_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DDS_BURST[2]	R/W	0x0	See description for DDS_BURST[0]

8.3.18.4 DDS_BURST_3 Register (Offset = 0x806) [Reset = 0x0000]

DDS_BURST_3 is shown in Table 8-318.

Return to the Summary Table.

Table 8-318. DDS_BURST_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DDS_BURST[3]	R/W	0x0	See description for DDS_BURST[0]

8.3.18.5 DDS_IMODE Register (Offset = 0x808) [Reset = 0x00]

DDS_IMODE is shown in Table 8-319.

Return to the Summary Table.

Table 8-319. DDS_IMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	

Table 8-319. DDS_IMODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DDS_IMODE	R/W	0x0	0x0 = Indexing-Mode Disabled. Up to 4 DDS channels can be enabled. DDS waits for triggers according to the VTRIG_MODE field of each vector. 0x1 = Indexing-Mode Enabled. Only DDS channel 0 can be enabled, and all vector memory is assigned to it. The TRIG[4:1] inputs can be used jump to specific vectors on-demand. See Indexing-Mode Section for full details.

8.3.18.6 DDS_SYM Register (Offset = 0x809) [Reset = 0x00]

DDS_SYM is shown in Table 8-320.

Return to the Summary Table.

Table 8-320. DDS_SYM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	DDS_SYM	R/W	0x0	DDS_SYM[n] enables symmetric mode for DDS channel n. See Vector Order and Symmetric Mode.

8.3.18.7 DDS_HOLD Register (Offset = 0x80A) [Reset = 0x00]

DDS_HOLD is shown in Table 8-321.

Return to the Summary Table.

Table 8-321. DDS_HOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	DDS_HOLD	R/W	0x0	DDS_HOLD[n] enables hold mode for DDS channel n. See Hold Mode.

8.3.18.8 DDS_IDLE Register (Offset = 0x80B) [Reset = 0xXX]

DDS_IDLE is shown in Table 8-322.

Return to the Summary Table.

Table 8-322. DDS_IDLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DDS_IDLE	R	X	DDS_IDLE[n] returns 1 if DDS channel n is currently idle (waiting for a trigger), otherwise it returns 0.

8.3.18.9 DDS_INDEX0 Register (Offset = 0x80C) [Reset = 0xXX]

DDS_INDEX0 is shown in Table 8-323.

Return to the Summary Table.

Table 8-323. DDS_INDEX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	

Table 8-323. DDS_INDEX0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DDS_INDEX0	R	X	DDS_Index0 returns the index of the vector that DDS channel n is currently executing (or waiting for a trigger to execute).

8.3.18.10 DDS_INDEX1 Register (Offset = 0x80D) [Reset = 0xXX]

DDS_INDEX1 is shown in Table 8-324.

Return to the Summary Table.

Table 8-324. DDS_INDEX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DDS_INDEX1	R	X	See DDS_INDEX0

8.3.18.11 DDS_INDEX2 Register (Offset = 0x80E) [Reset = 0xXX]

DDS_INDEX2 is shown in Table 8-325.

Return to the Summary Table.

Table 8-325. DDS_INDEX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DDS_INDEX2	R	X	See DDS_INDEX0

8.3.18.12 DDS_INDEX3 Register (Offset = 0x80F) [Reset = 0xXX]

DDS_INDEX3 is shown in Table 8-326.

Return to the Summary Table.

Table 8-326. DDS_INDEX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DDS_INDEX3	R	X	See DDS_INDEX0

8.3.18.13 DDS_AMP2 Register (Offset = 0x810) [Reset = 0x00]

DDS_AMP2 is shown in Table 8-327.

Return to the Summary Table.

Table 8-327. DDS_AMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	DDS_AMP2	R/W	0x0	DDS_AMP2[n] enables 2nd-order amplitude control for DDS channel n. This allows the vector mode to synthesize smooth and accurate amplitude curves. Note: This register should only be changed when SYS_EN=0.

8.3.18.14 DDS_VEC_n Register (Offset = 0xB20) [Reset = 0xXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

DDS_VEC_n is shown in Table 8-328.

Return to the Summary Table.

Table 8-328. DDS_VEC_n Register Field Descriptions

Bit	Field	Type	Reset	Description
167-120	FREQ_START	R/W	X	Each vector is 21 bytes (168 bits) and the address for vector n starts at 0x0B10 + 21*n (21 is base 10 value). All 384 vectors occupy 8064 bytes. Vectors are allocated to DDS channels depending on how many DDS channels are enabled. See section DDS Vector Mode for further details. Note: Vectors can be updated via SPI while the DDS is enabled, but restrictions apply. See Writing Vectors While DDS is Enabled. Initial value of frequency accumulator (48-bits). Note: the lower 16-bits of FREQ_START can be repurposed for 2nd order amplitude control (AMP_STEP2, 16-bits, signed).
119-88	FREQ_STEP	R/W	X	Frequency step (32-bits)
87-72	AMP_START	R/W	X	Initial value of amplitude accumulator (16-bits, signed)
71-56	AMP_STEP	R/W	X	Amplitude step (16-bits, signed)
55-40	PHASE_START	R/W	X	Initial value of phase accumulator (16-bits)
39-8	NUM_SAMP_M32	R/W	X	Vector length in samples minus 32 (32-bits). NUM_SAMP_M32 must be a multiple of 8 (# of samples minimum is 32). The lower 3 bits always return 0.
7-3	STEP_EXP	R/W	X	Defines exponent applied to frequency and amplitude step values. Legal range is 3 to 31 (or 3 to 15 if DDS_AMP2[n]=1).
2	RESERVED	R	0x0	
1	LAST_VEC	R/W	X	0x0 = Continue to next vector after playing this vector. 0x1 = Return to start of Vector Block after playing this vector (or return to VINDEX in indexing-mode).
0	VTRIG_MODE	R/W	X	0x0 = Auto-trigger (vector starts and ends automatically) 0x1 = Manual trigger (DDS may stall until a trigger occurs)

8.3.19 Programmable_FIR Registers

Table 8-329 lists the memory-mapped registers for the Programmable_FIR registers. All register offset addresses not listed in Table 8-329 should be considered as reserved locations and the register contents should not be modified.

Table 8-329. PROGRAMMABLE_FIR Registers

Offset	Acronym	Register Name	Section
0x2800	PFIR_EN		Section 8.3.19.1
0x2801	PFIR_MODE		Section 8.3.19.2
0x2803	PFIR_LEN		Section 8.3.19.3
0x2804	PFIR_BC		Section 8.3.19.4
0x2805	PFIR_DLY		Section 8.3.19.5
0x2807	FR_EN		Section 8.3.19.6
0x2810	PFIR_H_n		Section 8.3.19.7
0x2E10	PFIR_PROG		Section 8.3.19.8

Complex bit access types are encoded to fit into small table cells. Table 8-330 shows the codes that are used for access types in this section.

Table 8-330. Programmable_FIR Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.19.1 PFIR_EN Register (Offset = 0x2800) [Reset = 0x00]

PFIR_EN is shown in Table 8-331.

Return to the Summary Table.

Table 8-331. PFIR_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	
3-0	PFIR_EN	R/W	0x0	PFIR_EN[n] enables the PFIR for channel n. The PFIR isnt actually enabled until SYS_EN is set. When PFIR_MODE is configured for real operation (PFIR_MODE=0), then n corresponds to DAC channels (n = 0 to 1). When PFIR_MODE is configured for complex operation (PFIR_MODE is greater than 0), then n corresponds to DUC channels (n = 0 to 3). Enabling the PFIR on an unsupported channel produces undefined behavior. See PFIR Configruation Section. Note: When the PFIR is placed before DUCs, the associated DSP channels must be configured for DUC mode (e.g. if PFIR_EN[n] is set, then DSP_MODEn should be set to DUC mode).

8.3.19.2 PFIR_MODE Register (Offset = 0x2801) [Reset = 0x00]

PFIR_MODE is shown in Table 8-332.

Return to the Summary Table.

Table 8-332. PFIR_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	
1-0	PFIR_MODE	R/W	0x0	This specifies the general mode of the PFIR (See PFIR Configuration Section). It impacts all PFIR channels. The user must also set PFIR_EN to enable the PFIR.

8.3.19.3 PFIR_LEN Register (Offset = 0x2803) [Reset = 0x00]

PFIR_LEN is shown in Table 8-333.

Return to the Summary Table.

Table 8-333. PFIR_LEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	PFIR_LEN	R/W	0x0	The number of supported coefficients (NPFIR) depends on PFIR_MODE and DSP_L. See also PFIR Power Saving. Note: If NPFIR=24, the low power options is not available (number of taps cannot be reduced below 24). 0x0 = Support NPFIR/2 coefficients (low power option) 0x1 = Support NPFIR coefficients (full power option)

8.3.19.4 PFIR_BC Register (Offset = 0x2804) [Reset = 0x00]

PFIR_BC is shown in Table 8-334.

Return to the Summary Table.

Table 8-334. PFIR_BC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	PFIR_BC	R/W	0x0	When PFIR_MODE=0 and PFIR_EN=1, the user may choose to set PFIR_BC=1 to broadcast the output of PFIR channel 0 to both DACs. This allows the user to transmit identical signal to both DACs without the need to enable the PFIR for channel 1 (reduced power consumption) 0x0 = PFIR Broadcast disabled 0x1 = PFIR Broadcast enabled

8.3.19.5 PFIR_DLY Register (Offset = 0x2805) [Reset = 0x0000]

PFIR_DLY is shown in Table 8-335.

Return to the Summary Table.

Table 8-335. PFIR_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PFIR_DLY[1]	R/W	0x0	When PFIR_MODE=0 (PFIR-after-channel-bonder), this register delays the second half of the impulse response by PFIR_DLY samples (i.e. DAC cycles). This is useful for canceling a reflection. PFIR_DLY[1] controls the delay for channel 1. See PFIR Reflection Cancellation.

Table 8-335. PFIR_DLY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	PFIR_DLY[0]	R/W	0x0	When PFIR_MODE=0 (PFIR-after-channel-bonder), this register delays the second half of the impulse response by PFIR_DLY samples (i.e. DAC cycles). This is useful for canceling a reflection. PFIR_DLY[0] controls the delay for channel 0. See PFIR Reflection Cancellation Section.

8.3.19.6 FR_EN Register (Offset = 0x2807) [Reset = 0x00]

FR_EN is shown in Table 8-336.

Return to the Summary Table.

Table 8-336. FR_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	FR_EN	R/W	0x0	Note: This register should only be changed when the FR interface is idle. 0x0 = FR interface is disabled. PFIR coefficients are controlled by PFIR_H 0x1 = FR interface is enabled. PFIR coefficients are controlled by FR_PFIR_H.

8.3.19.7 PFIR_H_n Register (Offset = 0x2810) [Reset = 0xXXXX]

PFIR_H_n is shown in Table 8-337.

Return to the Summary Table.

Table 8-337. PFIR_H_n Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PFIR_H[n]	R/W	X	When FR_EN=1, writes to this register set the values in PFIR_H. Memory for coefficient n (0:767) at address 0x2810 + 2*n. Each coefficient is a signed 16-bit value with an LSB weight of 2^{-15}. The organization of coefficients within this allocation depends on PFIR_MODE. See PFIR Programming Section. Note: When FR_EN=1, this register cannot be read or written over SPI and can only be written with the FR interface. To read the values, set FR_EN=0.

8.3.19.8 PFIR_PROG Register (Offset = 0x2E10) [Reset = 0xXX]

PFIR_PROG is shown in Table 8-338.

Return to the Summary Table.

Table 8-338. PFIR_PROG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	FR_PFIR_PROG	R/W	X	When FR_EN=1, writes to this register set the value in PFIR_PROG. This provides readback of the FR_PFIR_PROG value that was written over the FR interface. Note: When FR_EN=1, this register is read-only over SPI and can only be written with the FR interface. It should only be read when the FR interface is idle. The user should wait 1024 DACCLK cycles after writing FR_PFIR_PROG before writing FR_PFIR_H.

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Startup Procedure

The list below is the startup procedure for the device:

1. Power up the device with ball $\overline{\text{RESET}}$ asserted using the procedure in Power Up and Down Sequence.
2. Apply DACCLK and then de-assert $\overline{\text{RESET}}$.
3. If using the CPLL, set CPLL_EN = 1.
4. Set up all the operational parameters (registers can be programmed in any order):
   a. Program DSP_MODE*n* to a mode that uses the JESD204C interface.
   b. If using the DUC mode or DDS Stream mode, choose the Interpolation/Upsampling factor and program the DSP _L register.
   c. Determine the total interpolation factor (LT) as the value is needed in the next steps.
   d. Decide how many sample streams are needed and program the JESD_M register.
   e. Select a JESD204C mode from JJESD Interface Modes. Make sure the selected mode supports the value of LT computed previously and the desired link layer encoding. Also makes sure the mode supports the number of desired streams set in the JESD_M register. Program the mode number into the JMODE register.
   f. Program the JENC register to select 8b/10b or 64b/66b operation.
   g. Compute the value of R using JESD Interface Modes and the LT value computed earlier.
   h. Using Table 7-47 (8b/10b) or Table 7-48 (64b/66b), identify a row that matches the R value and DAC clock frequency. Program REFDIV, MPY and RATE according to the tables.
   i. If necessary, program LANE_SEL[n] to bind the appropriate physical lanes to logical lanes. Program LANE_INV if necessary to account for any lane inversion (the differential pair +/- are swapped).
   j. Program other common settings according to your desired usage (SUBCLASS, SFORMAT, SCR in the JCNTL register).
   k. If using 8b/10b encoding, program the KM1 register to set the K parameter to match the link partner. Be sure to honor the constraint imposed by the KR parameter from JESD Interface Modes.
   l. If subclass 1 operation is desired (SUBCLASS = 1), you must also program RBD. Determine the appropriate value for *RBD* by referring to Programming RBD.
   m. Program optional Serdes parameters if necessary (CDR0, EQ_CTRL, EQZERO, EQLEVEL).
5. If SUBCLASS = 1, SYSREF is necessary to establish the LMFC/LEMC phase in the receiver. Follow this procedure to use the automatic SYSREF calibration:
   a. Set SRCAL_AVG and SRTRK_AVG to appropriate settings
   b. Set SRTRK_ENSRTRK_EN if tracking is desired
   c. Set SYSREF_RX_ENSYSREF_RX_EN=1. If necessary, wait some amount of time for the SYSREF receiver to stabilize.
   d. Enable the SYSREF generator to produce a periodic SYSREF signal. The period of each SYSREF cycle must meet the requirements in SYSREF Frequency Requirements. If SYSREF is AC-coupled, allow sufficient time for the coupling capacitor to settle before proceeding.
   e. Set SRCAL_EN=1
   f. Wait for SYSREF_CAL_DONE=1. Verify that SYSREF_CAL_FAILSYSREF_CAL_FAIL=0.
6. Program the transmitter (link partner, such as FPGA or ASIC), and begin transmission.
7. Wait for fuse values to be loaded (register FUSE_DONE returns 1).
8. Program SYS_EN=1 to start up the receiver.

ADVANCE INFORMATION

9. If SUBCLASS=1, the receiver must process enough valid SYSREF pulses to set the JESD_ALIGNED register, otherwise, the JESDlink remains down. Refer to the JESD_ALIGNED register description for details.
10. Read the JESD_STATUS register to confirm operation of the link (LINK_UP field in JESD_STATUS = 1). If the LINK_UP field returns 0, verify these items in order:
    a. If PLL_LOCKED returns 0, verify the correct PLL settings (REFDIV, MPY and RATE). Verify the DACCLK frequency is correct.
    b. If SUBCLASS = 1 and ALIGNED returns 0, verify SYSREF has been applied and the SYSREF processor is enabled SYSREF_PROC_EN = 1. Verify the SYSREF period is valid.
    c. If PLL_LOCKED = 1 (and ALIGNED = 1 or SUBCLASS = 0), then read the LANE_STATUS[n] register (only read registers for logical lanes 0 to L-1). Identify if some lanes cannot acquire code group or block synchronization. If so, verify the transmitter has been programmed correctly. Verify LANE_SEL[n] is programmed correctly. Consider performing PHY tests to verify/optimize PHY operation (PRBS testing using JTEST, eye-scan testing, or equalizer optimization).
    d. d. If SUBCLASS = 1 and EB_ERR = 1, then one possibility is the RBD value is set incorrectly. See Programming RBD.
11. If SUBCLASS = 1 and the link is up, the SYSREF signal can be turned off if desired. If SYSREF is DC-coupled, SYSREF can be synchronously gated at the source. If SYSREF is AC-coupled, program SYSREF_PROC_EN = 0 before turning off the SYSREF transmitter or setting SYSREF_RX_EN = 0 (this approach is also valid for a DC-coupled SYSREF).
12. To configure the part for a different mode, set SYS_EN = 0. Then return to step 4.

9.1.2 Bandwidth Optimization for Square Wave Mode

As discussed in DAC Output Modes, the DAC output is a zero order hold (ZOH) where the output value is flat across the sample time (either the full clock period in NRZ mode or ½ the clock period in DES2XL mode). Given the high inherent output bandwidth of the DAC, this output response is only minimally filtered, especially in NRZ mode with a larger sample period. This is shown for a square wave waveform for NRZ mode (Figure 9-1) and DES2XL mode (Figure 9-2).

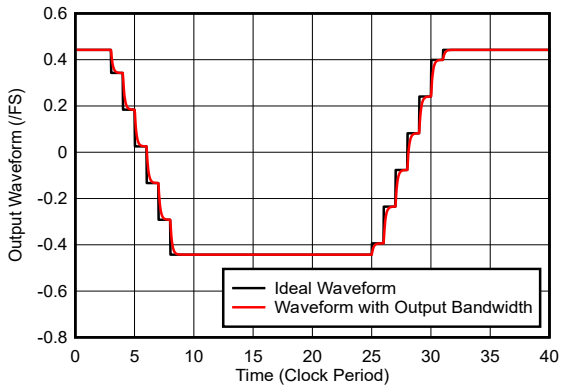


Figure 9-1. Output Waveform for NRZ Mode with DAC Bandwidth Limitation

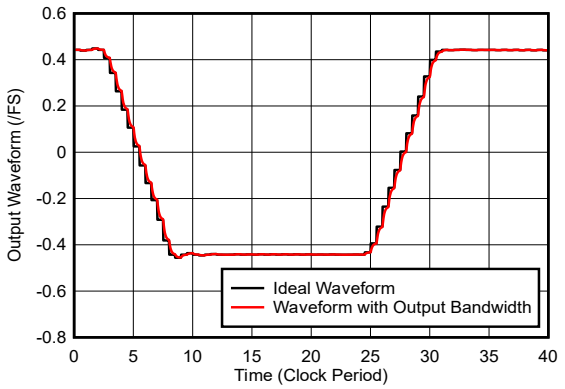


Figure 9-2. Output Waveform for DES Mode with DAC Bandwidth Limitation

The DAC output bandwidth can be reduced to remove the sample to sample variation while maintaining the high slew rate of the square wave mode. An output bandwidth similar to the transition period bandwidth, or approximately $2/(3*T_{TRANS})$, where T_{TRANS} is the transition time, offers a good compromise between maintaining the slew rate and removing the ZOH structure.

Figure 9-3 shows a square wave output waveform with recommended output bandwidth using

- f_{CLK} = 22GHz
- F_{NCO} = 1GHz
- SLEW = 2 (7.5GHz transition time)
- DES2XL Mode

ADVANCE INFORMATION

- BW_{OUT} = 5GHz

The square wave slew rate is mostly maintained while the ZOH structure is removed.

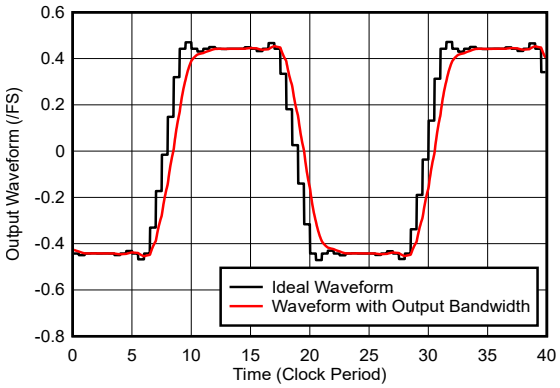


Figure 9-3. Square Wave Output with Recommended Output Bandwidth

9.2 Typical Application: Ku-Band Radar Transmitter

9.2.1 Design Requirements

Ku-band covers a frequency range of 12GHz to 18GHz, with radars using a range between 15 and 17GHz. For this example, use a radar with signal bandwidth of 1GHz and a center frequency of 16.2GHz.

Doppler radars use the frequency shift in the returned signal to measure the velocity of object. Large reflected signals from for example ground clutter mix with the TX and RX phase noise, which can potentially swamp the return signal from a small moving object. This places a requirement on close in phase noise for the close in phase noise of the radar chirp. For this example, we assume a single side band phase noise requirement of -126dBc/Hz at 16.2GHz center frequency.

Radars are also sensitive to spurious signals, and for this example, we assume 80dBFS is required for the inband SFDR.

9.2.2 Detailed Design Procedure

A summary of the design parameters are listed in Table 9-1. A input sample rate of 1.25GSPS complex covers the 1GHz signal bandwidth, and interpolation by 16x is used to increase the TX sample rate to 20GSPS. The device's numerically controlled oscillator (NCO) is used to place the signal at the TX output at 3.8GHz. An addition 2x interpolation is applied in DES2XH mode, increasing the sample rate to 40GSPS and output frequency to 16.2GHz.

The JESD204C interface is configured in JMODE 4 with 4 streams (2 IQ pairs) and 2 Serdes lane per IQ pair. With 64/66 bit encoding, the Serdes baud rate is 20.625Gbps.

Table 9-1. Design Parameters for an Ku-band Transmitter

Parameter	Value
Input Clock	20GHz
DAC Sample Rate	40GSPS
Output Mode	DES2XH
DEM and Dither Settings	On
TX Interpolation Factor	16x
TX Input Rate	1.25GSPS Complex
NCO frequency	3.8GHz
JMODE	4
# Streams	4 (2x IQ pairs, 1/DAC)
# Serdes Lanes	4

ADVANCE INFORMATION

Table 9-1. Design Parameters for an Ku-band Transmitter (continued)

Parameter	Value
Encoding	64/66
Serdes Baud Rate	20.625Gbps

9.2.3 Application Curves

The radar chip waveform used for testing is a non-linear frequency modulated (NLFM) pulse, lasting 4096 samples at the 20GSPS complex input rate. The frequency ramps from -0.5GHz to + 0.5GHz, following a frequency ramp curve developed by Price and shown in [Price R. *Chebyshev Low Pulse Compression Sidelobes via a Nonlinear FM.* National Radio Science Meeting of URSI; PortSaid, Egypt: 1979.] with T = 4096 samples, B = 0.8, B_l = 0.5611 and B_c = 0.238.

$$f(f, B_l, B_c) = B \times \frac{t - T/2}{T} \times \left(B_l + \frac{B_c}{\sqrt{1 - 4\left(t - T/2\right)^2 / T^2}} \right) \quad (8)$$

The NLFM Chirp frequency ramp without the offset to 16.2GHz is shown in Figure 9-4. The time domain DDS waveform and continuous waveform based on Equation 8 is shown in Figure 9-5. The Auto-correlation of the DDS waveform and continuous waveform is shown in Figure 9-6.

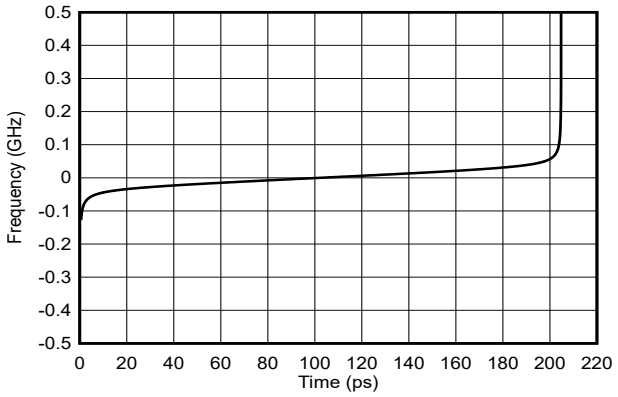


Figure 9-4. NLFM Frequency Ramp

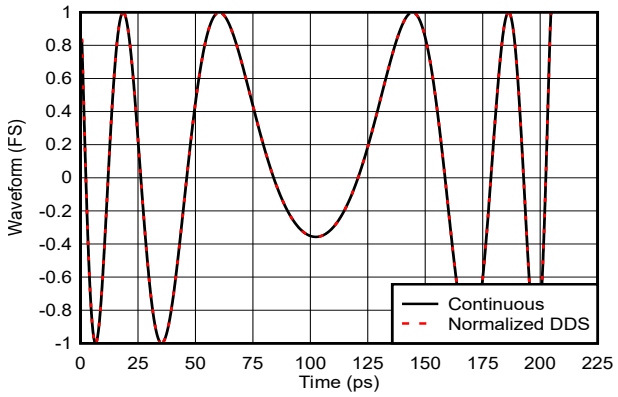


Figure 9-5. Normalized Time Domain of NLFM Waveform (Red = DDS waveform, Black = continuous equation)

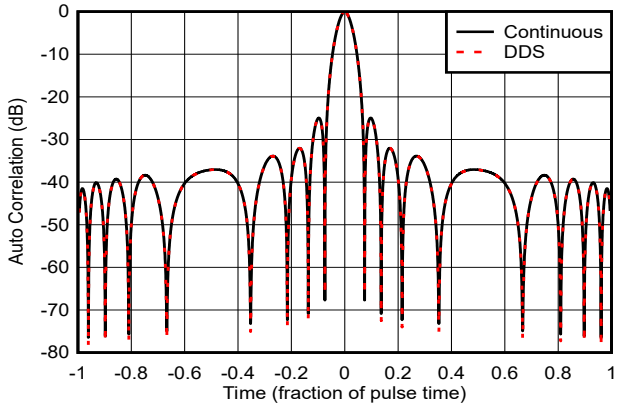


Figure 9-6. Auto-correlation of NLFM Waveform (Red = DDS waveform, Black = continuous equation)

ADVANCE INFORMATION

The spectra purity of a 16.2GHz tone is shown with a fullscale tone in Figure 9-7 across a 5GHz span. The largest spur is approximately 66dBc at 3.16GHz, which is the 4th harmonic. The output phase noise for a tone at 16.2GHz is shown in Figure 9-8.

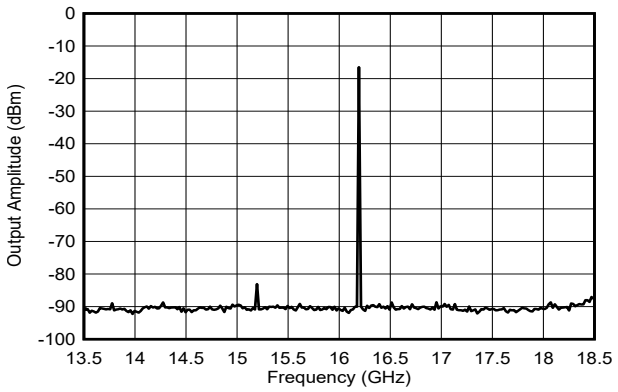


Figure 9-7. In Band Single Tone Frequency Spectra with f_{OUT} = 16.2GHz

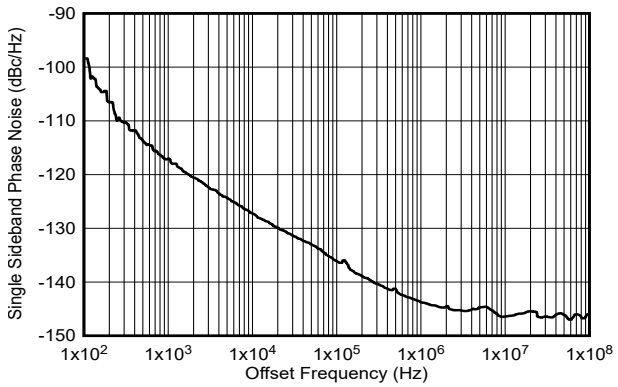


Figure 9-8. DAC Additive Phase Noise at 16.2GHz

ADVANCE INFORMATION

9.3 Power Supply Recommendations

The device has three supply voltages and requires seven supply domains to achieve data sheet performance as shown in Table 9-2:

Table 9-2. Recommended Power Supply Domains

Voltage	Supply Domain	Device Supplies
+1.8V	VDDA	VDDA18A, VDDA18B
	VDDIO	VDDIO
	VDDCSR	VDDCLK, VDDSYS, VDDR
	VDDSP18	VDDSP18
	VDDCP18	VDDCP18
+0.8V	VDDL	VDDLA, VDDLB
	VDDCLK08	VDDCLK08
	DVDD	VDDDIG, VDDT, VDDEA and VDDEB
-1.8V	VEEx	VEEAM18, VEEBM18

The recommended power supply is shown in Figure 9-9. The power-supply voltages must be low in noise and provide the needed current to achieve rated device performance. A step down high-efficiency switching converter is used first, followed by a second stage of regulation using LDOs to provide switching noise reduction and improved voltage accuracy. The user can also refer to the TI WEBENCH® Power Designer which can be used to select and design the individual power supply elements as needed. The recommended switching regulators are:

- TPSM82913 = +2.3V for the VDDA, VDDIO, VDDCSR, VDDL and VDCCCLK domains
- TPS543820 (8A) or TPS543A22 (12A) = +0.8V for DVDD
- TPSM82913 = +3.8V for VEEx domain

Recommended LDOs include:

- TPS7A9401 for +1.8V and +0.8V
- LM27762 for -1.8V

ADVANCE INFORMATION

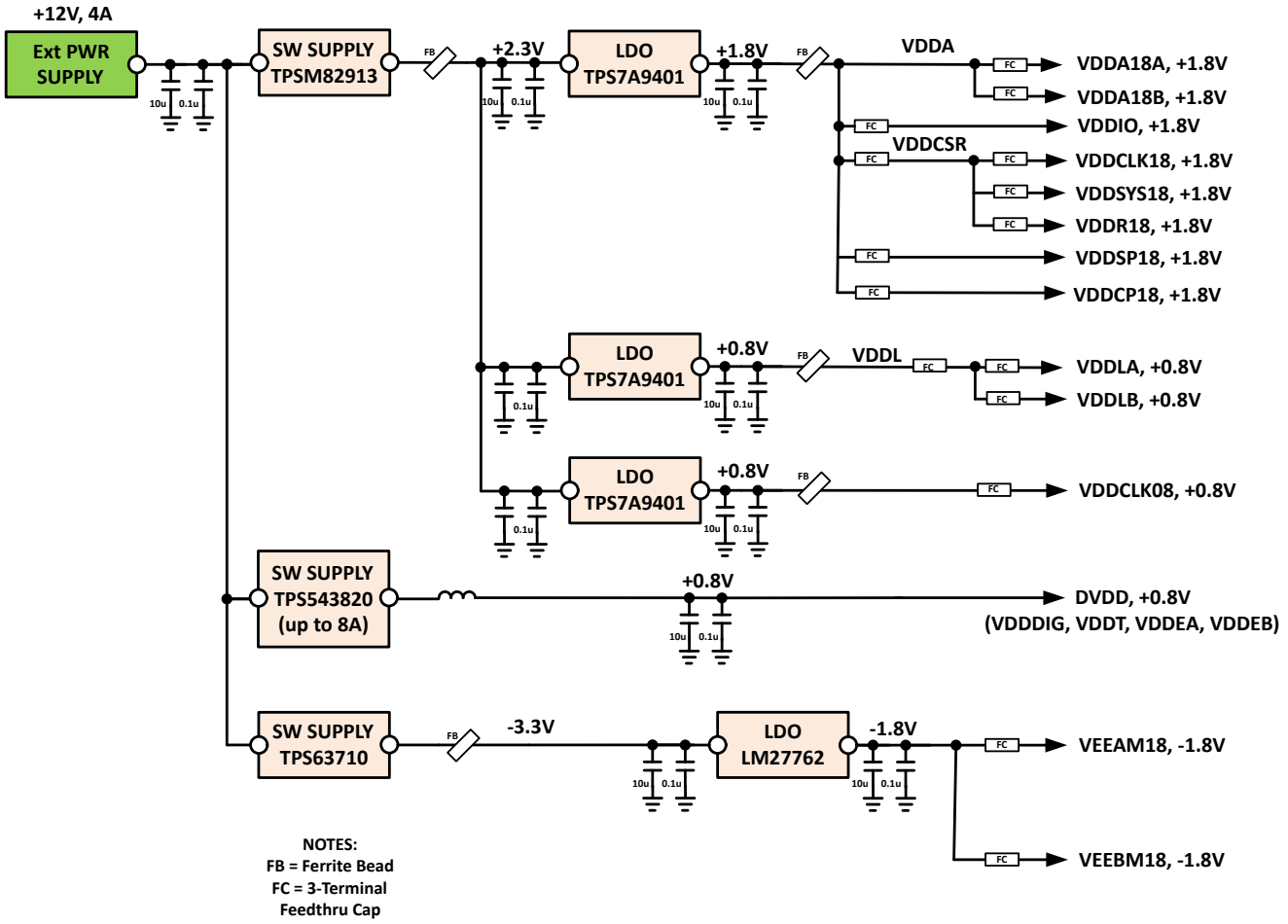


Figure 9-9. Recommended Power Supply Block Diagram

The VDDA supply is regulated by an LDO, or low-noise drop-out linear regulator, with a +1.8V output and is further broken down into the following subgroup power domains:

- VDDA: VDDA18A, VDDA18B
- VDDIO
- VDDCSR: VDDCLK18, VDDSYS18, VDDR18
- VDDSP18
- VDDCP18

Each device supply can be tied to a single LDO but are isolated with a ferrite bead and/or three-terminal capacitor or similar.

The VDDL supply is +0.8V and is further broken down into VDDLA and VDDLB. Each device supply can be tied to a single LDO but are isolated with a ferrite bead and/or three-terminal capacitor or similar.

The VDDCLK08 supply is +0.8V and is the most sensitive for achieving the best phase noise performance. VDDCLK08 must be isolated to a LDO to prevent noise from other 0.8V supplies coupling into the clock path.

The DVDD supply is +0.8V and can be directly connected to a switching power supply. The DVDD encompasses the following device supplies, VDDDIG, VDDT, VDDDEA and VDDDEB, which can all be connected together. No further isolation with a ferrite bead and/or three-terminal capacitor or similar is required.

The VEEx supply is -1.8V derived from a single LDO and is further broken down into VEEAM18 and VEEBM18, which are isolated with a ferrite bead and/or three-terminal capacitor or similar.

The recommendation is to follow these important power supply design considerations:

1. Decouple all power supply rails and bus voltages as they come onto the system board. Further place additional decoupling at or near the DAC for each power domain. Typically, one low ESL 0.1µF decoupling capacitor per power supply pin is recommended unless specified in the data sheet or EVM assembly.
2. Remember that approximately 20dB/decade noise suppression is gained for each additional filtering stage.
3. Decouple for both high and low frequencies, which might require multiple capacitor values.
4. Series ferrite beads and feed through capacitors are commonly used at the power plain entry point and can be used for addition power domain isolation. This is done for each individual supply voltage on the system board whether the voltage comes from an LDO or a switching regulator.
5. For added capacitance, use tightly stacked power and ground plane pairs (≤4 mil spacing) this adds inherent high-frequency (>500MHz) decoupling to the PCB design.
6. Keep supplies away from sensitive analog circuitry such as the front-end RF stage of the DAC and high-speed clocking and digital circuits if possible.
7. Keep power domains that demand higher currents, near the top of the stack-up or layer that has power plain entry point. This minimizes the overall loop inductance.
8. Any open or voided areas on power plane, fill with ground to provide additional isolation and shielding.
9. Keep a 20 to 25 mil gap between all adjacent power and/or ground plane fills. This helps eliminate all gap coupling between adjacent power domains and/or grounds within the same layer.
10. Some switcher regulator circuitry/components could be located on the opposite side of the PCB for added isolation.
11. Follow the IC manufacture recommendations; if they are not directly stated in an application note or data sheet, then study the evaluation board. These are great vehicles to learn from. Applying these points above can help provide a solid power supply design yielding data sheet performance in many applications.

Each application has different tolerances for noise on the supply voltage, so understanding these trades is best described in the following two application notes for more details:

- Clutter-free power supplies for RF converters in radar applications (Part 1)
- Clutter-free power supplies for RF converters in radar applications (Part 2)

Also refer to Figure 9-15 through Figure 9-18 to illustrate the one power supply layout and stack-up approach.

9.3.1 Power Up and Down Sequence

At power up, ramp up the supplies in the following order:

1. Ramp 1.8V supplies
2. Ramp -1.8V supplies
3. Ramp 0.8V supplies

The reverse order is used for rampdown.

9.4 Layout

9.4.1 Layout Guidelines and Example

There are many critical signal connections that require specific care and attention during PC board design:

1. DAC analog output signals
2. Sampling clock
3. Serdes (JESD204x) data inputs
4. Power supplies
5. Power and grounding strategy

There are many considerations to take note of when developing a high-speed PCB design. Here are a few recommendations and example figures to follow for any high-speed PCB design:

1. Route using loosely coupled 100Ω differential traces when possible on the Serdes inputs. This routing minimizes impact of corners and length-matching serpentines on pair impedance.

ADVANCE INFORMATION

2. Provide adequate pair-to-pair spacing to minimize crosstalk, especially with loosely coupled differential traces. Tightly coupled differential traces can be used to reduce self-radiated noise or to improve neighboring trace noise immunity when adequate spacing cannot be provided.
3. Provide adequate ground plane pour spacing to minimize coupling with the high-speed traces. Any ground plane pour must have sufficient via connections to the main ground plane of the board. Do not use floating or poorly connected ground pours.
4. Use smoothly radiused corners and avoid 45- or 90-degree bends to reduce impedance mismatches on all high-speed inputs/outputs for both analog and digital signal traces. See Figure 9-10 as an example.

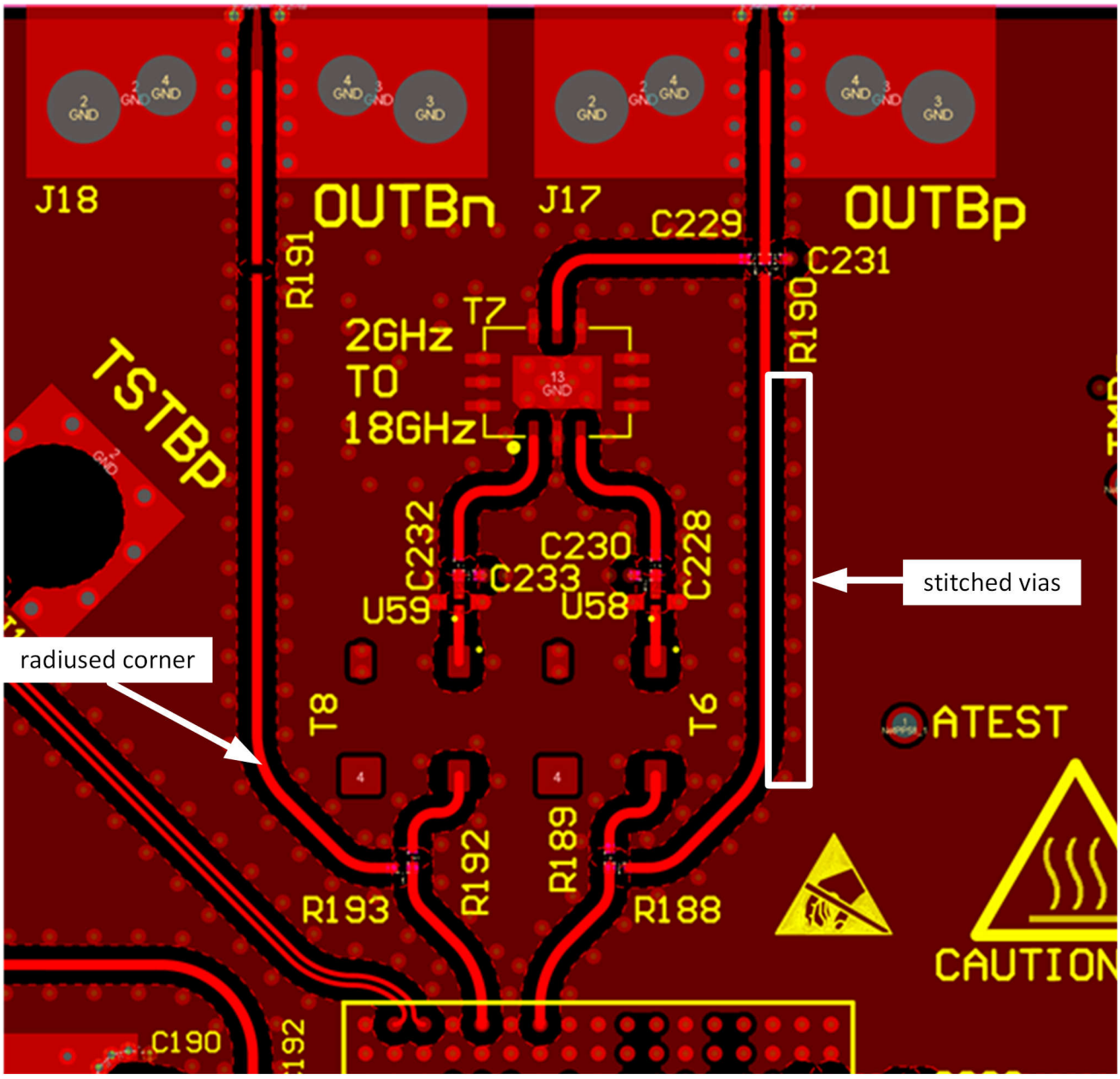


Figure 9-10. Radius Corner and Stitch Vias next to High_Speed Signal Trace

5. Incorporate any ground plane cutouts necessary at component landing pads, ie – SMA connectors, baluns, and so on, to avoid impedance discontinuities at these locations. Cut-outs below these landing pads on one or multiple ground planes to achieve a pad size or stackup height that achieves the needed 50Ω, single-ended impedance. See Figure 9-11 and an example.

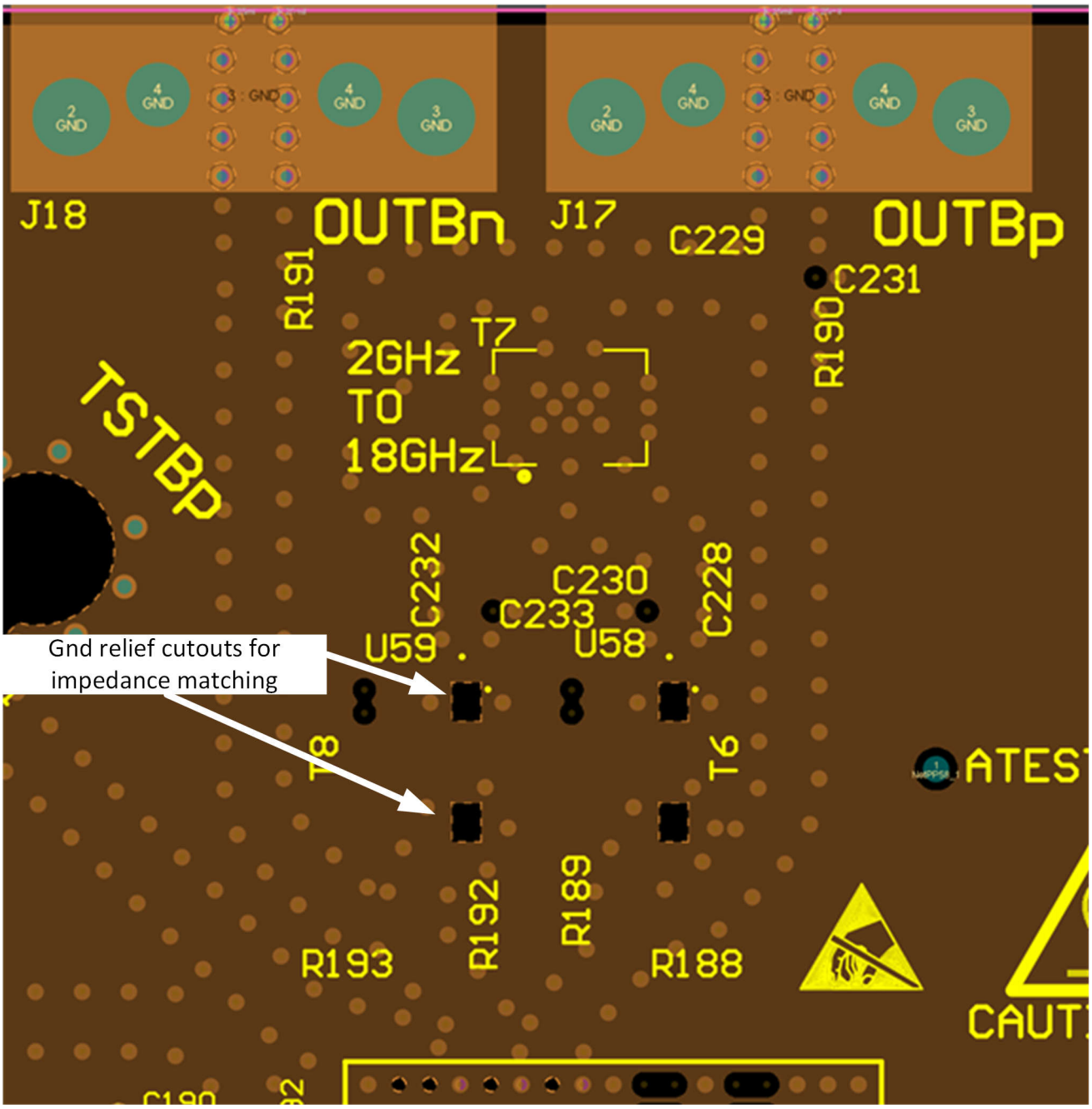


Figure 9-11. Ground Cut-outs below Balun Pins

6. Avoid routing traces near irregularities in the reference ground planes. Irregularities include cuts in the ground plane or ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie stitching vias adjacent to any high-speed signal at an appropriate spacing as determined by the maximum frequency the trace transports (λ/4). See Figure 9-10 as an example.
8. When high-speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top or bottom of the vias. If layer selection is not flexible, use back-drilled or buried, blind vias to eliminate stubs. Always place two ground vias (“return vias”) close to critical high-speed signal trace via when transitioning between layers to provide a nearby ground return path. See Figure 9-12 as an example.

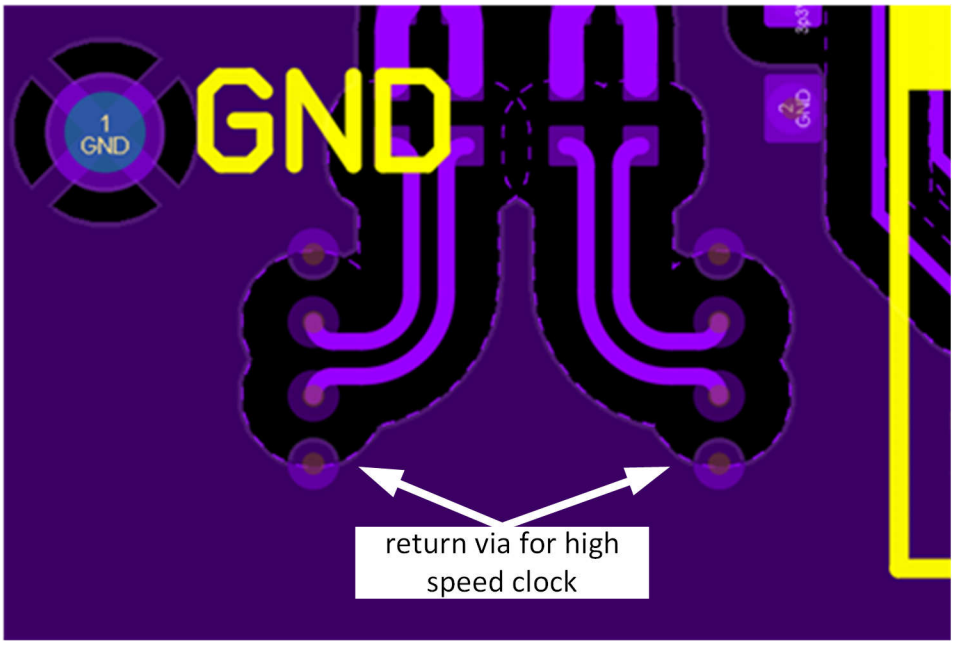


Figure 9-12. Return Vias for High Speed Clock

9. Pay particular attention to potential coupling between JESD204x data input routing and the analog output routing. Switching noise from the JESD204x inputs can couple into the analog output traces and show up as wideband noise due to the high bandwidth of the DAC. Route the Serdes JESD204x data inputs on a separate layer, if possible, from the DAC output traces to avoid noise coupling, see Figure 9-13 and Figure 9-14 as examples.

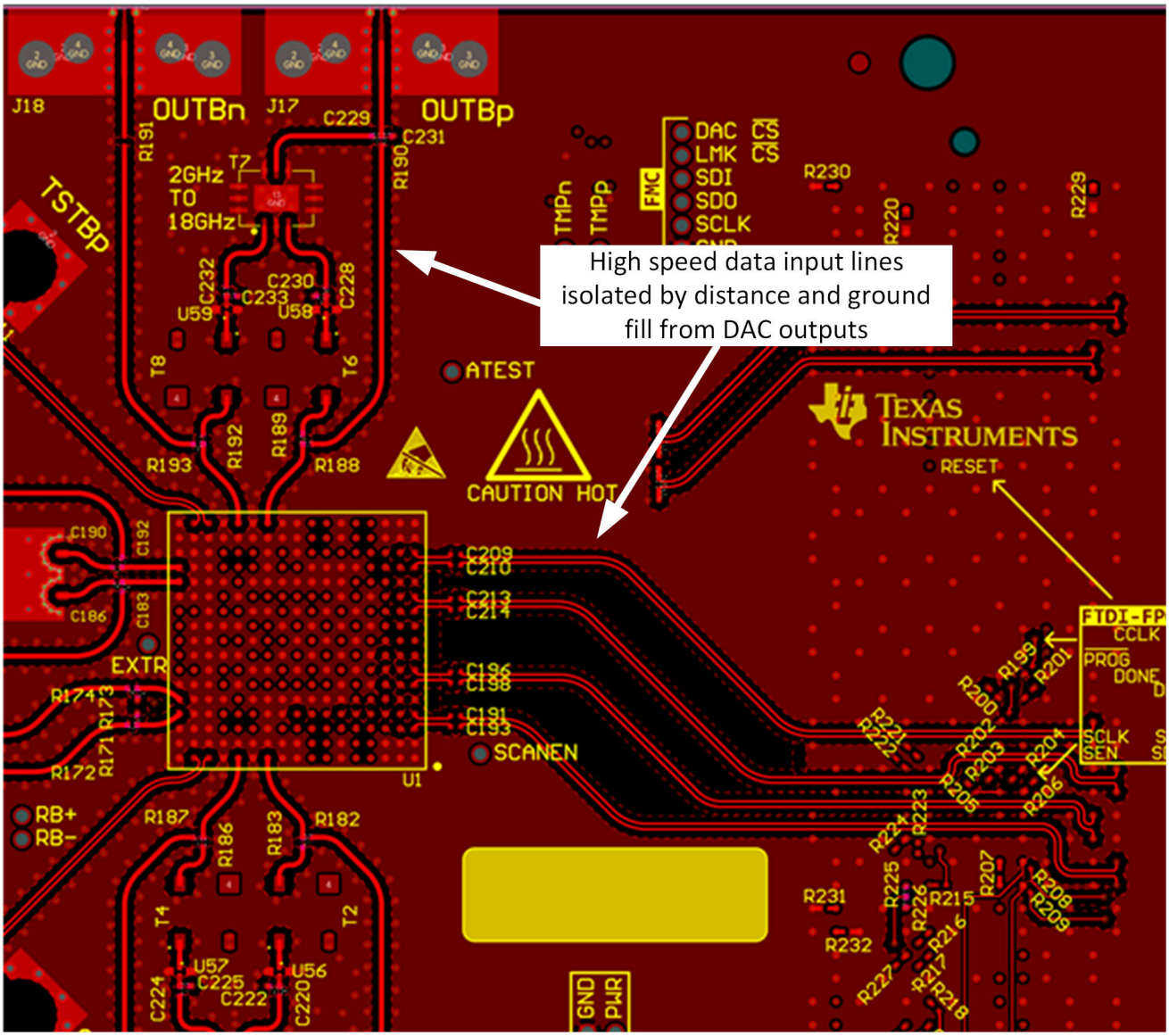


Figure 9-13. Serdes Top Layer Routing with Ground Fill Isolation

ADVANCE INFORMATION

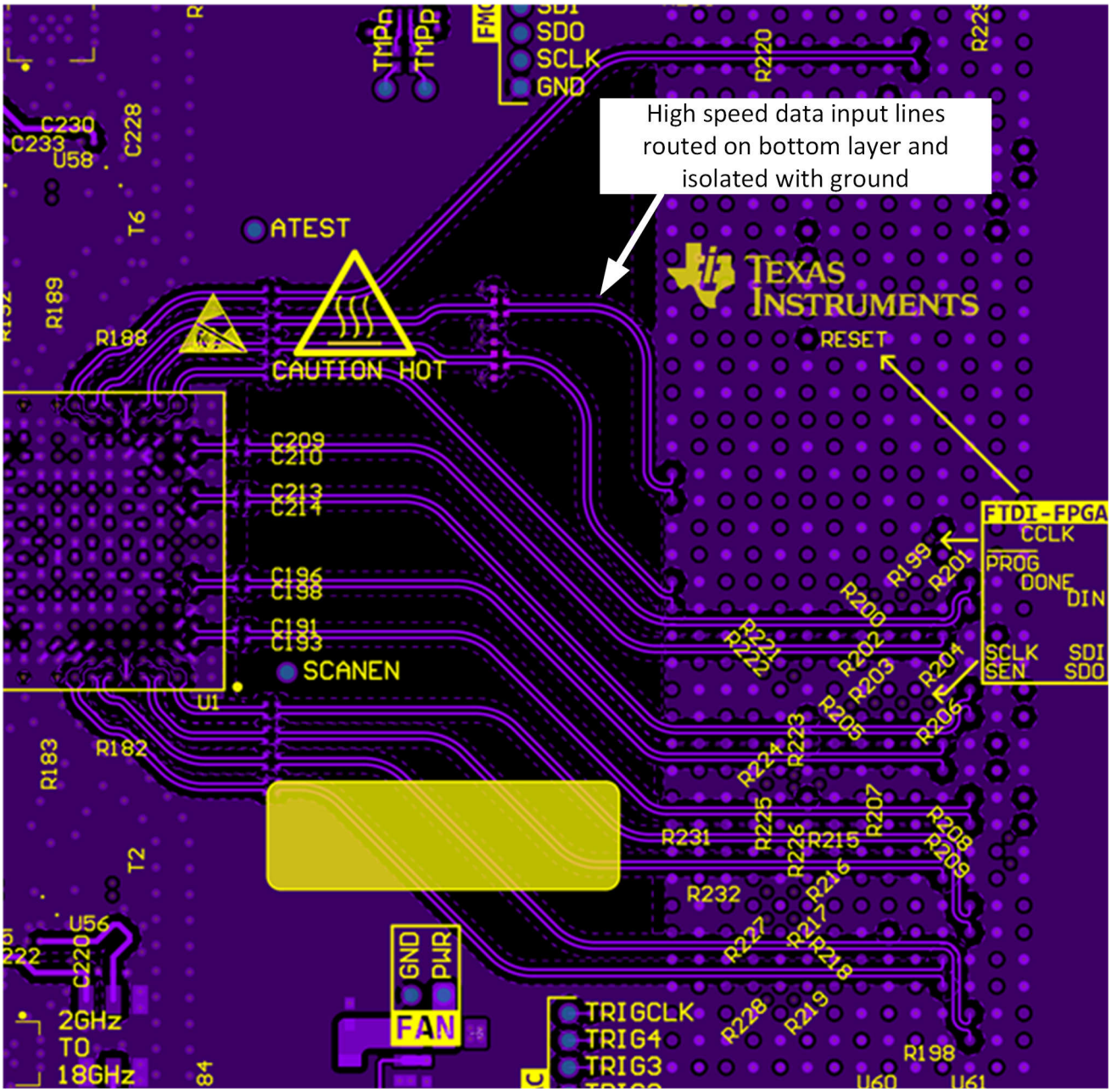


Figure 9-14. Serdes Bottom Layer Routing with Ground Isolation

10. A reduction in the clock amplitude can degrade the DAC noise performance, so make sure the clock signal has adequate drive strength, especially for high frequencies. To help avoid this, keep the clock source close to the DAC if using a passive balun to drive or interface with the sampling clock pins of the converter. If trace routes are longer than a few inches, impedance matching at the DACs sampling clock input pins can be necessary.

Examples of the power plane design is show in Figure 9-15 through Figure 9-18.

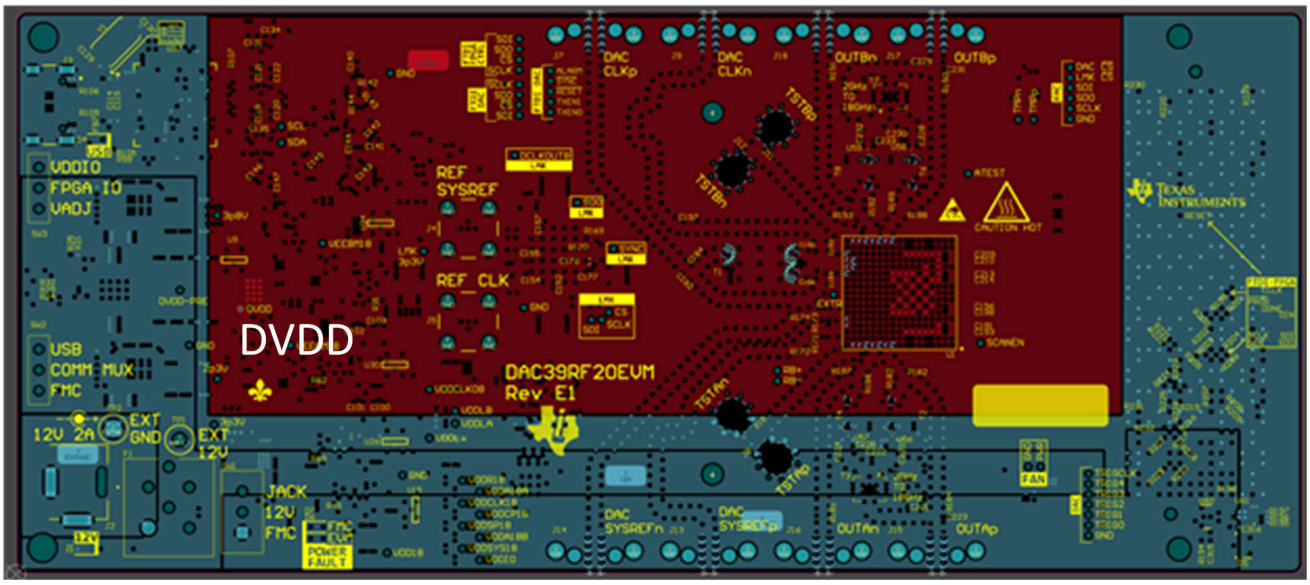


Figure 9-15. Power Plane Layout for Layer 3

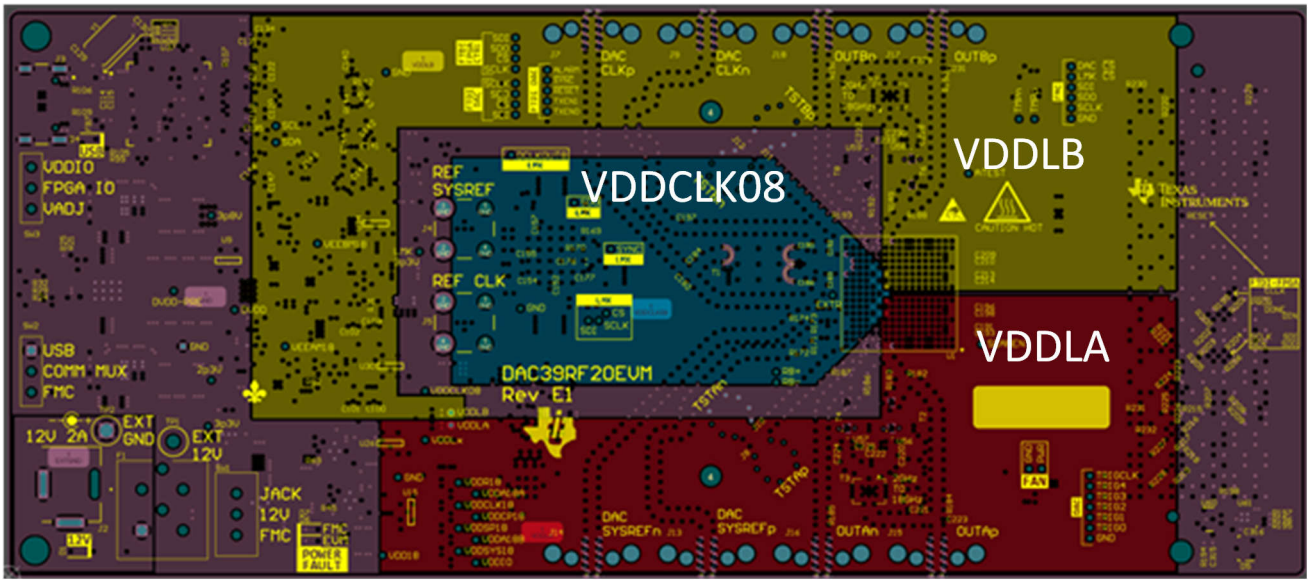


Figure 9-16. Power Plane Layout for Layer 5

ADVANCE INFORMATION

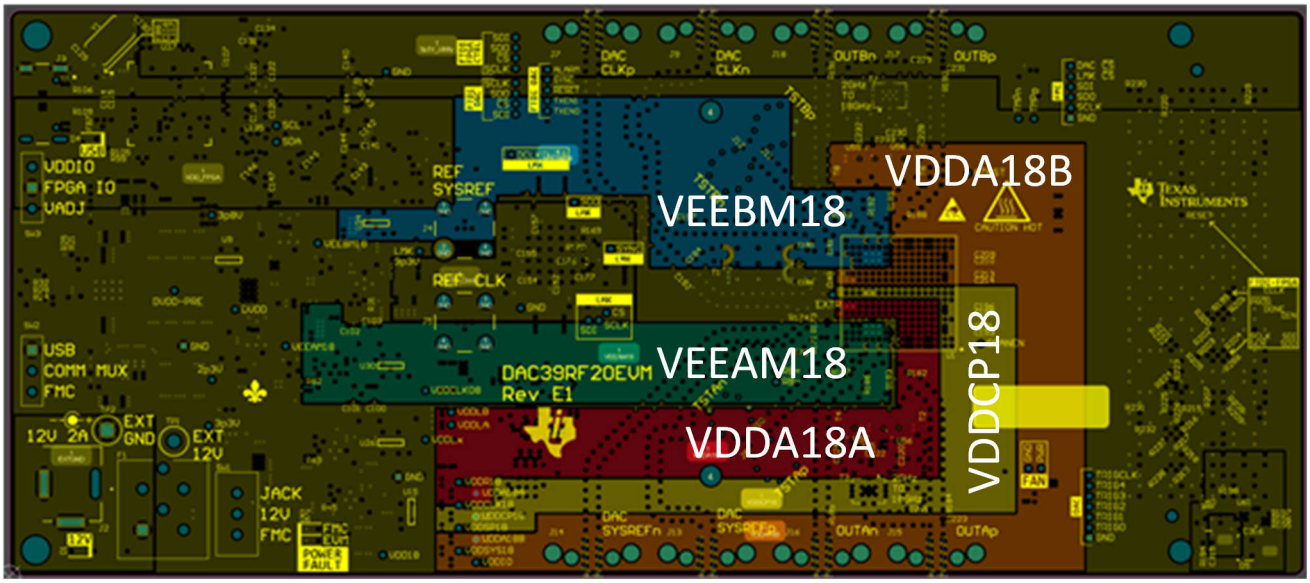


Figure 9-17. Power Plane Layout for Layer 12

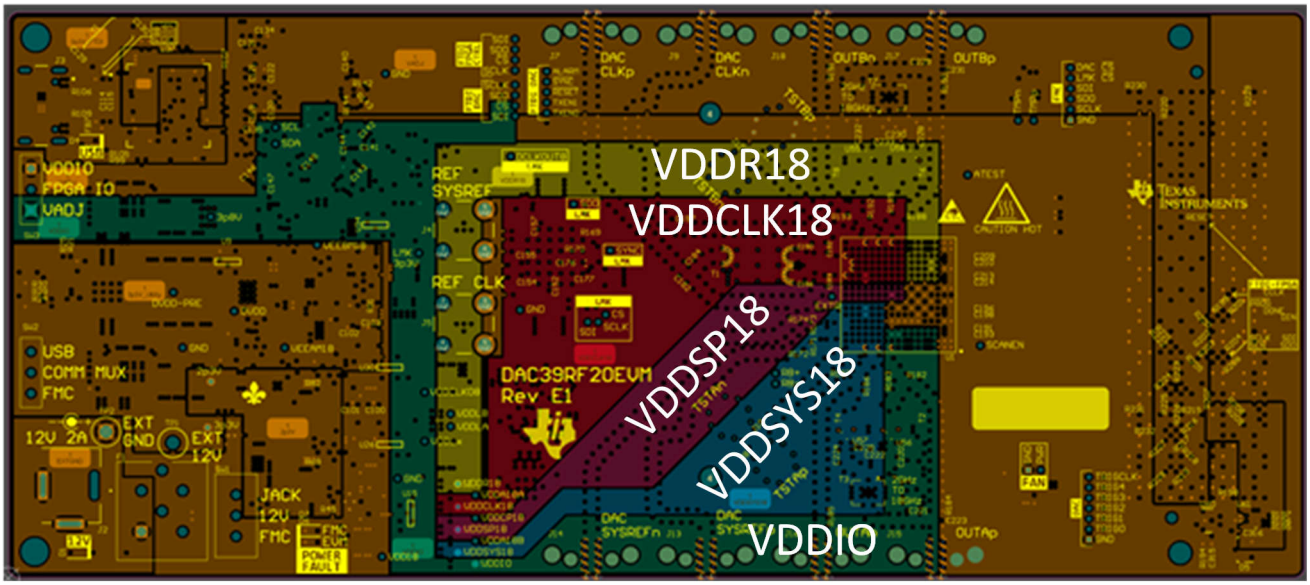


Figure 9-18. Power Plane Layout for Layer 14

In addition, TI recommends the following general PCB fabrication considerations for all high-speed PCB designs:

1. Use high quality dielectric materials for any critical signal layers within the PCB stack-up. Typically, the top and bottom layers are the most critical and more board houses can implement a mix of high and standard quality dielectrics, also known as a hybrid stack-up.
2. Use multiple power layers if necessary to provide a robust power delivery system to the converter.
3. Use multiple ground, power, ground layer stacks within the PCB to develop high frequency decoupling within the PCB, the recommendation for these layers is 4 mils or less.
4. Use a solid ground plane, do not split or “slot” the ground plane to create an analog vs. digital grounding barrier or divider to avoid harm.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

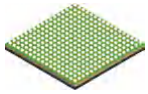
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

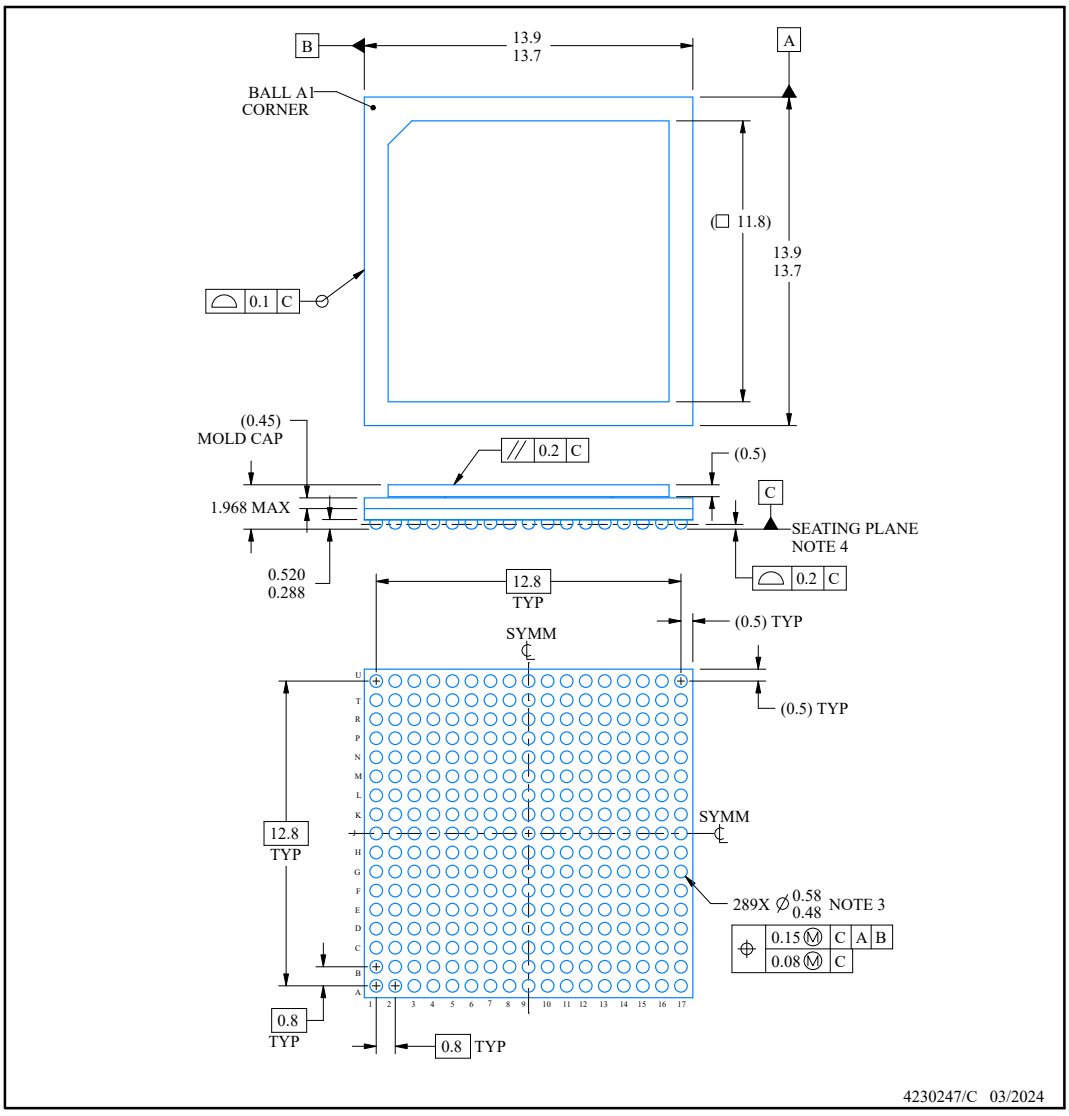
PACKAGE OUTLINE

ANH0289A



FCCSP - 1.968 mm max height

BALL GRID ARRAY



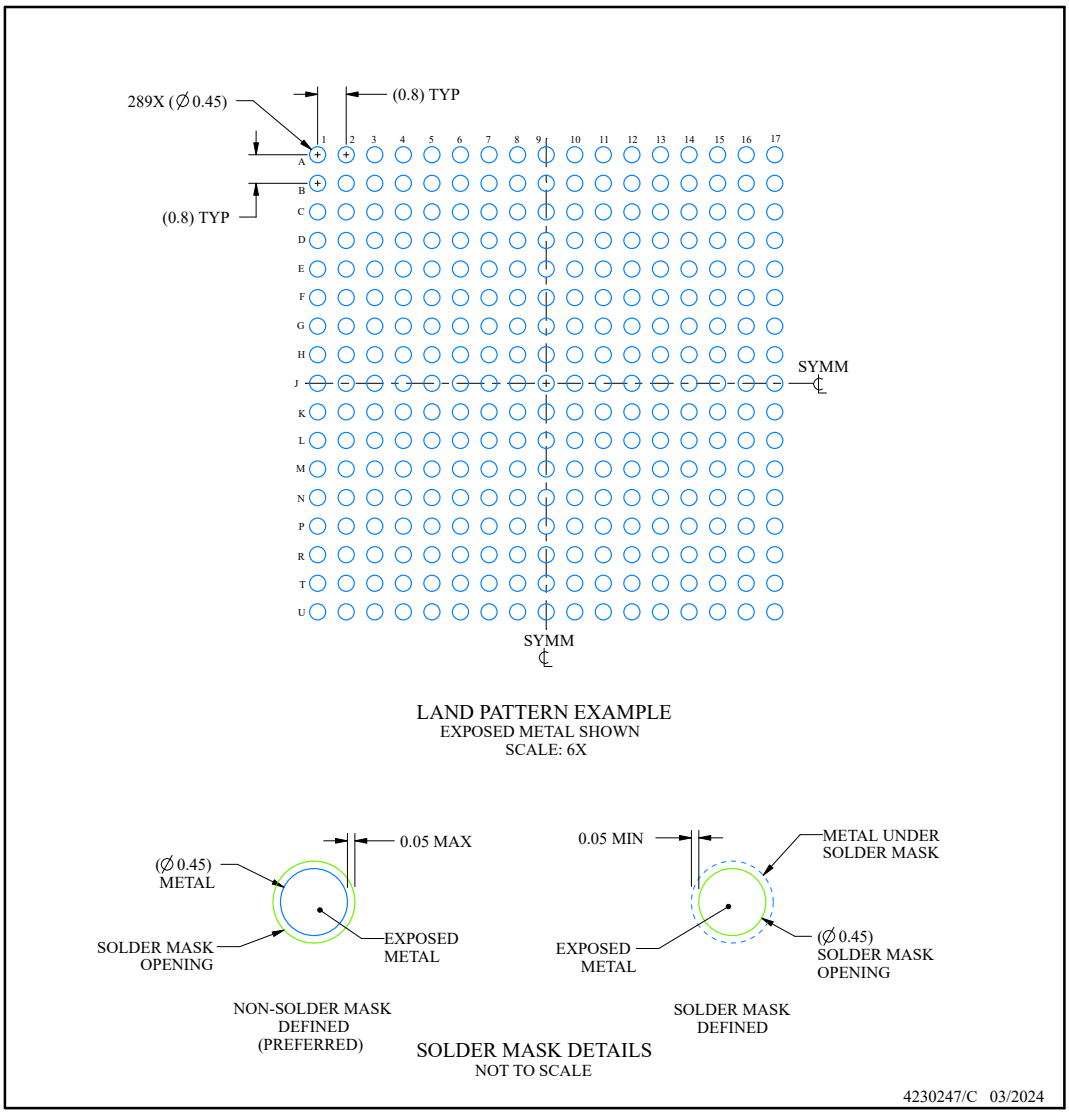
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, post reflow, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

EXAMPLE BOARD LAYOUT

ANH0289A — **FCCSP - 1.968 mm max height**

BALL GRID ARRAY



NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SPRU811 (www.ti.com/lit/spru811).

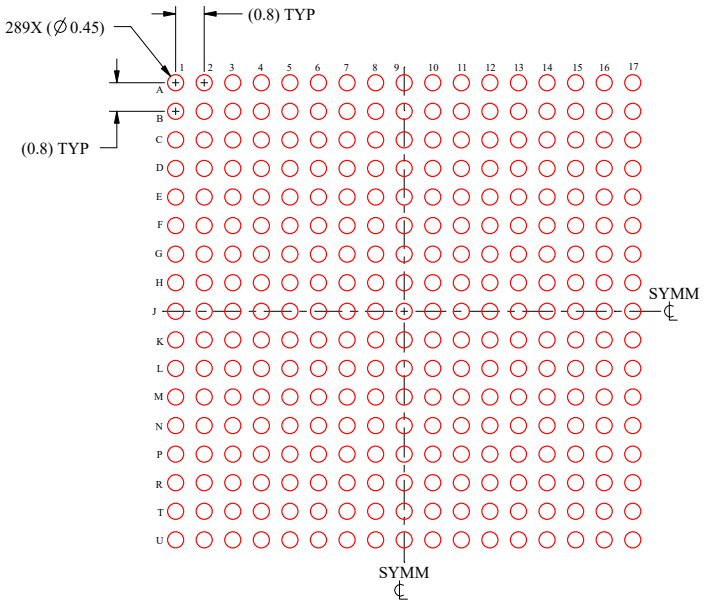
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

ANH0289A **FCCSP - 1.968 mm max height**

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

4230247/C 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDAC39RF20ANH	Active	Preproduction	FCCSP (ANH) | 289	90 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265