# **DAC0808**

DAC0808 8-Bit D/A Converter



Literature Number: SNAS539A



# DAC0808 8-Bit D/A Converter

## **General Description**

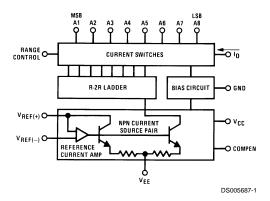
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with  $\pm 5 \rm V$  supplies. No reference current (I\_REF) trimming is required for most applications since the full scale output current is typically  $\pm 1$  LSB of 255 I\_REF/256. Relative accuracies of better than  $\pm 0.19\%$  assure 8-bit monotonicity and linearity while zero level output current of less than 4  $\mu A$  provides 8-bit zero accuracy for I\_REF $\geq 2$  mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

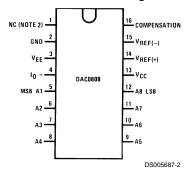
### **Features**

- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/µs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

## **Block and Connection Diagrams**



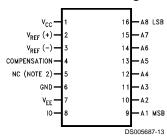
#### **Dual-In-Line Package**



Top View Order Number DAC0808 See NS Package M16A or N16A

# **Block and Connection Diagrams** (Continued)

## Small-Outline Package



# **Ordering Information**

ACCURACY	OPERATING			
	TEMPERATURE RANGE	N PACKAGE (N16A)		SO PACKAGE
		(Note	e 1)	(M16A)
8-bit	0°C≤T <sub>A</sub> ≤+75°C	DAC0808LCN	MC1408P8	DAC0808LCM

Note 1: Devices may be ordered by using either order number.

# **Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage

Storage Temperature Range	-65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

## **Operating Ratings**

Temperature Range  $T_{MIN} \leq T_{A} \leq T_{MAX}$   $DAC0808 \qquad \qquad 0 \leq T_{A} \leq +75^{\circ}C$ 

## **Electrical Characteristics**

 $(V_{CC} = 5V, V_{EE} = -15 V_{DC}, V_{REF}/R14 = 2 mA$ , and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
E <sub>r</sub>	Relative Accuracy (Error Relative	(Figure 4)				%
	to Full Scale I <sub>O</sub> )					
	DAC0808LC (LM1408-8)				±0.19	%
	Settling Time to Within ½ LSB	T <sub>A</sub> =25°C (Note 7),		150		ns
	(Includes t <sub>PLH</sub> )	(Figure 5)				
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	T <sub>A</sub> = 25°C, ( <i>Figure 5</i> )		30	100	ns
TCI <sub>o</sub>	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	(Figure 3)				
$V_{IH}$	High Level, Logic "1"		2			V <sub>DC</sub>
$V_{IL}$	Low Level, Logic "0"				0.8	V <sub>DC</sub>
MSB	Digital Input Current	(Figure 3)				
	High Level	$V_{IH} = 5V$		0	0.040	mA
	Low Level	$V_{IL} = 0.8V$		-0.003	-0.8	mA
I <sub>15</sub>	Reference Input Bias Current	(Figure 3)		-1	-3	μA
	Output Current Range	(Figure 3)				
		$V_{EE} = -5V$	0	2.0	2.1	mA
		$V_{EE} = -15V, T_A = 25^{\circ}C$	0	2.0	4.2	mA
Io	Output Current	$V_{REF} = 2.000V,$				
		$R14 = 1000\Omega$ ,				
		(Figure 3)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(Figure 3)		0	4	μA
	Output Voltage Compliance (Note 3)	$E_r \le 0.19\%, T_A = 25^{\circ}C$				
	V <sub>EE</sub> =-5V, I <sub>REF</sub> =1 mA				-0.55, +0.4	V <sub>DC</sub>
	V <sub>EE</sub> Below -10V				-5.0, +0.4	V <sub>DC</sub>
SRI <sub>REF</sub>	Reference Current Slew Rate	(Figure 6)	4	8		mA/µs
	Output Current Power Supply	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	μA/V
	Sensitivity					
	Power Supply Current (All Bits	(Figure 3)				
	Low)					
I <sub>cc</sub>				2.3	22	mA
I <sub>EE</sub>				-4.3	-13	mA
	Power Supply Voltage Range	T <sub>A</sub> = 25°C, ( <i>Figure 3</i> )				
V <sub>CC</sub>			4.5	5.0	5.5	V <sub>DC</sub>
V <sub>EE</sub>			-4.5	-15	-16.5	V <sub>DC</sub>
	Power Dissipation		1			

## **Electrical Characteristics** (Continued)

 $(V_{CC} = 5V, V_{EE} = -15 V_{DC}, V_{REF}/R14 = 2 mA$ , and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
	All Bits Low	$V_{CC} = 5V$ , $V_{EE} = -5V$		33	170	mW
		$V_{CC} = 5V, V_{EE} = -15V$		106	305	mW
	All Bits High	$V_{CC} = 15V, V_{EE} = -5V$		90		mW
		$V_{CC} = 15V, V_{EE} = -15V$		160		mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 3: Range control is not required.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>JMAX</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any temperature is  $P_D = (T_{JMAX} - T_A)/\theta_{JA}$  or the number given in the Absolute Maixmum Ratings, whichever is lower. For this device, T<sub>JMAX</sub> = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

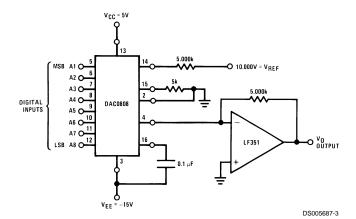
Note 5: Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

Note 6: All current switches are tested to guarantee at least 50% of rated current.

Note 7: All bits switched.

Note 8: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

## Typical Application

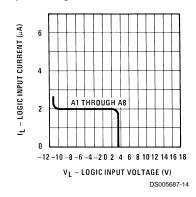


 $V_O = 10V \left( \frac{A1}{2} + \frac{A2}{4} + \dots \frac{A8}{256} \right)$ DS005687-23

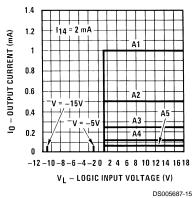
FIGURE 1. +10V Output Digital to Analog Converter (Note 8)

## Typical Performance Characteristics $V_{CC} = 5V$ , $V_{EE} = -15V$ , $T_A = 25^{\circ}C$ , unless otherwise noted

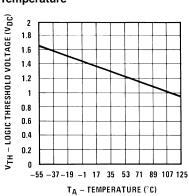
#### Logic Input Current vs Input Voltage



### **Bit Transfer Characteristics**



### Logic Threshold Voltage vs **Temperature**

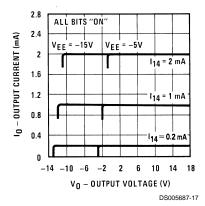


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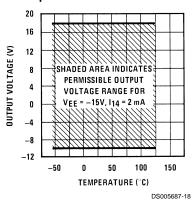
# Typical Performance Characteristics $V_{CC}$ = 5V, $V_{EE}$ = -15V, $T_A$ = 25°C, unless otherwise

noted (Continued)

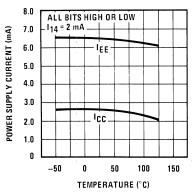
### Output Current vs Output Voltage (Output Voltage Compliance)



# Output Voltage Compliance vs Temperature

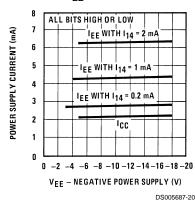


### Typical Power Supply Current vs Temperature

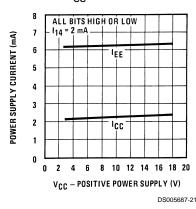


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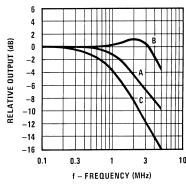
# Typical Power Supply Current vs V<sub>EE</sub>



# Typical Power Supply Current vs V<sub>CC</sub>



# Reference Input Frequency Response



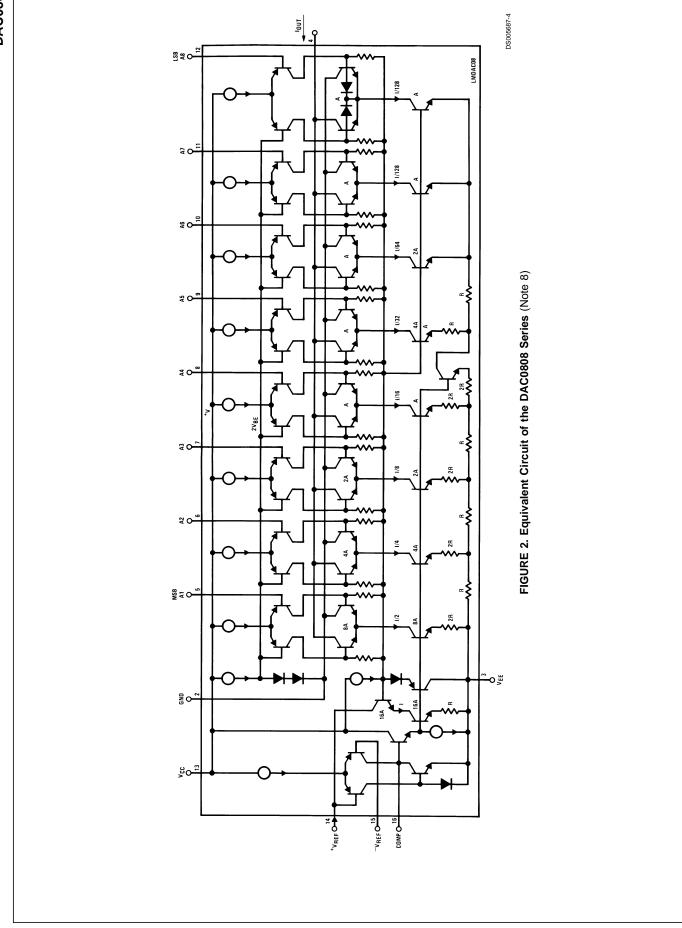
DS005687-22

Unless otherwise specified: R14 = R15 = 1 k $\Omega$ , C = 15 pF, pin 16 to  $V_{EE}$ ;  $R_L$  =  $50\Omega$ , pin 4 to ground.

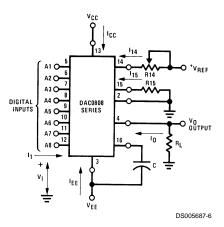
Curve A: Large Signal Bandwidth Method of Figure 7, V<sub>REF</sub> = 2 Vp-p offset 1V above ground.

Curve B: Small Signal Bandwidth Method of Figure 7,  $R_L = 250\Omega$ ,  $V_{REF} = 50$  mVp-p offset 200 mV above ground.

**Curve C:** Large and Small Signal Bandwidth Method of *Figure 9* (no op amp,  $R_L = 50\Omega$ ),  $R_S = 50\Omega$ ,  $V_{REF} = 2V$ ,  $V_S = 100$  mVp-p centered at 0V.



## **Test Circuits**



 $V_I$  and  $I_1$  apply to inputs A1-A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$\begin{split} I_O &= K \left( \frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} \right) \\ \text{where K} &\cong \frac{V_{REF}}{R14} \end{split}$$

and  $A_N$  = "1" if  $A_N$  is at high level  $A_N$  = "0" if  $A_N$  is at low level

FIGURE 3. Notation Definitions Test Circuit (Note 8)

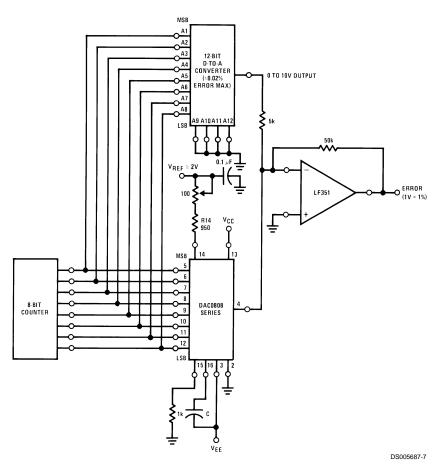


FIGURE 4. Relative Accuracy Test Circuit (Note 8)

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# Test Circuits (Continued)

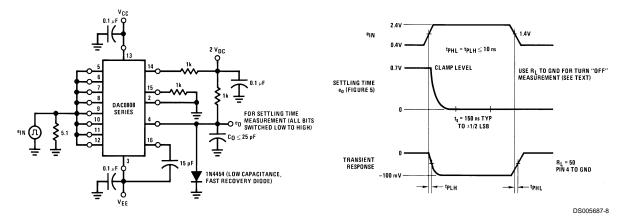


FIGURE 5. Transient Response and Settling Time (Note 8)

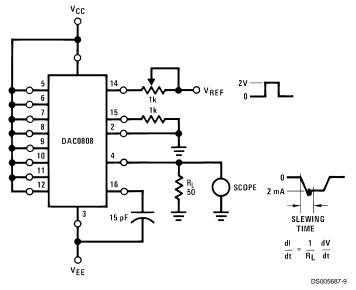


FIGURE 6. Reference Current Slew Rate Measurement (Note 8)

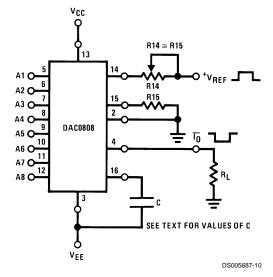


FIGURE 7. Positive V<sub>REF</sub> (Note 8)

## Test Circuits (Continued)

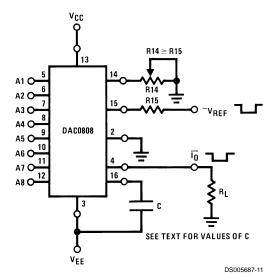


FIGURE 8. Negative V<sub>REF</sub> (Note 8)

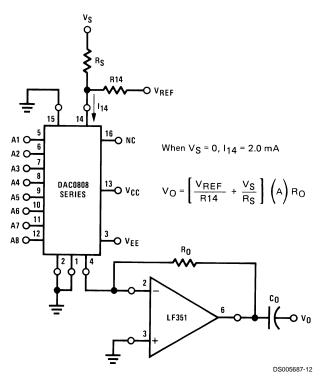


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 8)

# **Application Hints**

### REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input currrent, I<sub>14</sub>, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in Figure 7. The reference voltage source supplies the full current  $I_{14}$ .

For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 k $\Omega$ , minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V<sub>EE</sub> or ground, but using V<sub>EE</sub> increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main

## **Application Hints** (Continued)

advantage of this method. Compensation involves a capacitor to  $V_{\text{EE}}$  on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the  $V_{\text{EE}}$  supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1  $\mu F$  to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

#### **OUTPUT VOLTAGE RANGE**

The voltage on pin 4 is restricted to a range of -0.55 to 0.4V when  $V_{\text{EE}} = -5V$  due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to -5V where the negative supply voltage is more negative than -10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 k $\Omega$  between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of  $R_L$  up to  $500\Omega$  do not significantly affect performance, but a 2.5 k $\Omega$  load increases worst-case settling time to 1.2  $\mu s$  (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

#### **OUTPUT CURRENT RANGE**

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than -8V, due to the increased voltage drop across the resistors in the reference current amplifier.

#### **ACCURACY**

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor lad-

der. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 µA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of  $\pm \frac{1}{2}$  of one part in 65,536 or  $\pm 0.00076\%$ , which is much more accurate than the  $\pm 0.019\%$  specification provided by the DAC0808.

### **MULTIPLYING ACCURACY**

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16  $\mu$ A to 4 mA, the additional error contributions are less than 1.6  $\mu$ A. This is well within 8-bit accuracy when referred to full-scale.

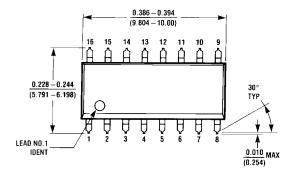
A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

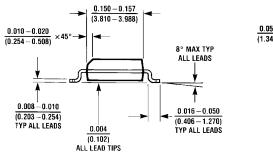
#### **SETTLING TIME**

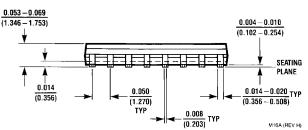
The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within  $\pm1/2$  LSB, for 8-bit accuracy, and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when  $R_L \leq 500\Omega$  and  $C_O \leq 25$  pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100  $\mu$ F supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

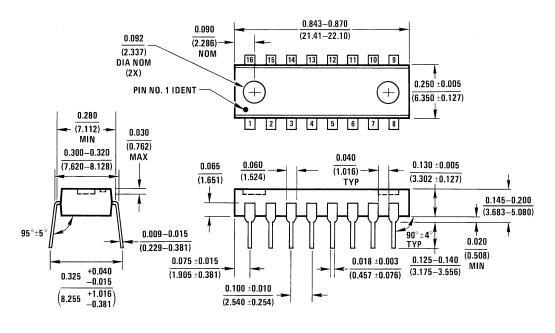
## Physical Dimensions inches (millimeters) unless otherwise noted







### Small Outline Package Order Number DAC0808LCM NS Package Number M16A



N16A (REV E)

Dual-In-Line Package Order Number DAC0808 NS Package Number N16A

## **Notes**

#### LIFE SUPPORT POLICY

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- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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11-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
DAC0808LCM/NOPB	Active	Production	SOIC (D)   16	48   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0808LCM
DAC0808LCM/NOPB.B	Active	Production	SOIC (D)   16	48   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0808LCM
DAC0808LCMX/NOPB	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0808LCM
DAC0808LCMX/NOPB.B	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0808LCM
DAC0808LCN/NOPB	Active	Production	PDIP (NFG)   16	25   TUBE	Yes	SN	Level-1-NA-UNLIM	0 to 70	DAC0808LCN MC1408P8
DAC0808LCN/NOPB.B	Active	Production	PDIP (NFG)   16	25   TUBE	Yes	SN	Level-1-NA-UNLIM	0 to 70	DAC0808LCN MC1408P8

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC0808LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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## \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
ı	DAC0808LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0	

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC0808LCM/NOPB	D	SOIC	16	48	495	8	4064	3.05
DAC0808LCM/NOPB.B	D	SOIC	16	48	495	8	4064	3.05
DAC0808LCN/NOPB	NFG	PDIP	16	25	502	14	11938	4.32
DAC0808LCN/NOPB.B	NFG	PDIP	16	25	502	14	11938	4.32

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Last updated 10/2025