

## CSD87503Q3E 30-V N-Channel NexFET™ Power MOSFETs

### 1 Features

- Dual N-Ch Common Source MOSFETs
- Optimized for 5-V Gate Drive
- Low-Thermal Resistance
- Low  $Q_g$  and  $Q_{gd}$
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

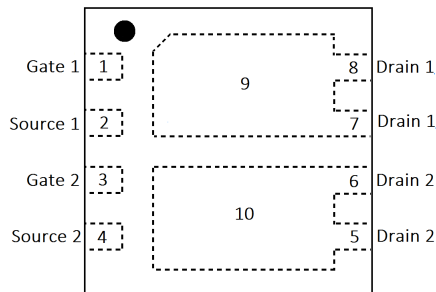
### 2 Applications

- USB Type-C/PD VBus Protection
- Battery Protection
- Load Switch

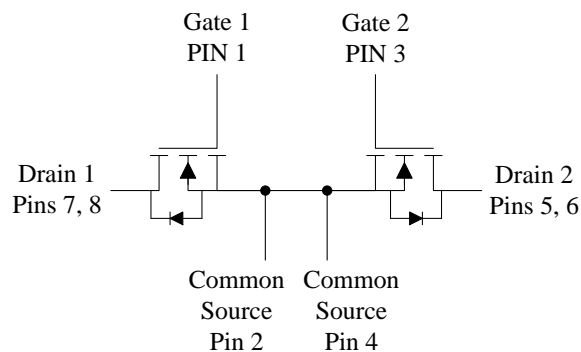
### 3 Description

The CSD87503Q3E is a 30-V, 13.5-mΩ, common source, dual N-channel device designed for USB Type-C/PD and battery protection. This SON 3.3 × 3.3 mm device has low drain-to-drain on-resistance that minimizes losses and offers low component count for space constrained applications.

**Top View**



**Circuit Image**



**Product Summary**

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$Q_g$	Gate Charge Total (4.5 V)	13.4	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	5.8	nC
$R_{DD(on)}$	Drain-to-Drain On-Resistance	$V_{GS} = 4.5\text{ V}$	17.3
		$V_{GS} = 10\text{ V}$	13.5
$V_{GS(th)}$	Threshold Voltage	1.7	V

**Device Information<sup>(1)</sup>**

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD87503Q3E	2500	13-Inch Reel	SON	Tape and Reel
CSD87503Q3ET	250	7-Inch Reel	3.30-mm × 3.30-mm Plastic Package	

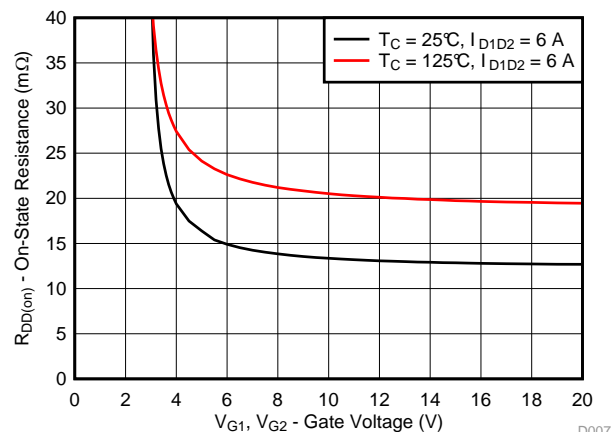
(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Absolute Maximum Ratings**

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_{D1, D2}$	Continuous Drain-to-Drain Current (Package Limited)	10	A
$I_{DS}$	Continuous Drain-to-Source Current (Package Limited)	1.5	A
$I_{D1, D2M}$	Pulsed Drain-to-Drain Current, <sup>(1)</sup>	89	A
$P_D$	Power Dissipation <sup>(2)</sup>	2.6	W
$P_D$	Power Dissipation, $T_C = 25^\circ\text{C}$	15.6	W
$T_J, T_{stg}$	Operating Junction, Storage Temperature	–55 to 150	°C

- (1) Max  $R_{\theta JC} = 8^\circ\text{C/W}$ , pulse duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 1\%$ .  
 (2) Typical  $R_{\theta JA} = 50^\circ\text{C/W}$  when mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

**$R_{DD(on)}$  vs  $V_{GS}$**



D007



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## 4 Revision History

DATE	REVISION	NOTES
September 2017	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-source voltage <sup>(1)</sup>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
I <sub>DSS</sub>	Drain-to-source leakage current <sup>(1)</sup>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V			1	μA
I <sub>GSS</sub>	Gate-to-source leakage current <sup>(1)</sup>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage <sup>(1)</sup>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.3	1.7	2.1	V
R <sub>DD(on)</sub>	Drain-to-drain on-resistance	V <sub>GS</sub> = 4.5 V, I <sub>D1D2</sub> = 6 A		17.3	21.9	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D1D2</sub> = 6 A		13.5	16.9	
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 3 V, I <sub>D1D2</sub> = 6 A		24		S
DYNAMIC CHARACTERISTICS						
C <sub>ISS</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>D1D2</sub> = 15 V, f = 1 MHz		782	1020	pF
C <sub>OSS</sub>	Output capacitance			157	204	pF
C <sub>RSS</sub>	Reverse transfer capacitance			149	194	pF
R <sub>g</sub>	Series gate resistance <sup>(1)</sup>			1.5	3.0	Ω
Q <sub>g</sub>	Gate charge total (4.5 V)	V <sub>D1D2</sub> = 15 V, I <sub>D1D2</sub> = 6 A		13.4	17.4	nC
	Gate charge total (10 V)			32.9	42.8	
Q <sub>gd</sub>	Gate charge gate-to-drain			5.8		nC
Q <sub>gs</sub>	Gate charge gate-to-source			4.8		nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			1.0		nC
Q <sub>OSS</sub>	Output charge	V <sub>D1D2</sub> = 15 V, V <sub>GS</sub> = 0 V		4.3		nC
t <sub>d(on)</sub>	Turnon delay time	V <sub>D1D2</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D1D2</sub> = 6 A, R <sub>G</sub> = 0 Ω		10		ns
t <sub>r</sub>	Rise time			40		ns
t <sub>d(off)</sub>	Turnoff delay time			25		ns
t <sub>f</sub>	Fall time			8		ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode forward voltage <sup>(1)</sup>	I <sub>D</sub> = 0.5 A, V <sub>GS</sub> = 0 V		0.75	0.95	V
Q <sub>rr</sub>	Reverse recovery charge <sup>(1)</sup>	V <sub>DS</sub> = 15 V, I <sub>F</sub> = 6 A, di/dt = 300 A/μs		9.2		nC
t <sub>rr</sub>	Reverse recovery time <sup>(1)</sup>			14		ns

(1) Parameter measured on both MOSFETs individually. Table values are for a single FET.

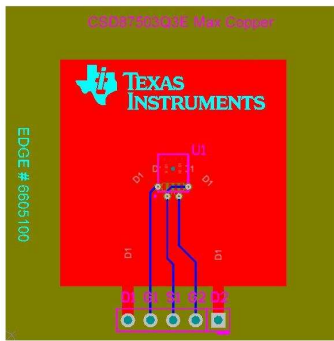
### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

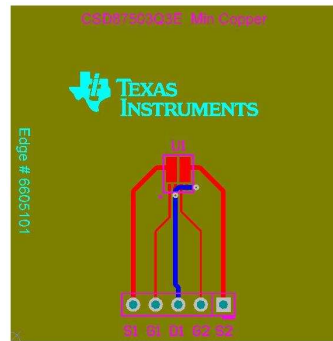
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance <sup>(1)</sup>			8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			60	$^\circ\text{C}/\text{W}$

(1)  $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.

(2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.



Max  $R_{\theta JA} = 60^{\circ}\text{C/W}$   
when mounted on 1 in<sup>2</sup>  
(6.45 cm<sup>2</sup>) of  
2-oz (0.071-mm) thick  
Cu.



Max  $R_{\theta JA} = 185^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz (0.071-mm) thick  
Cu.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)

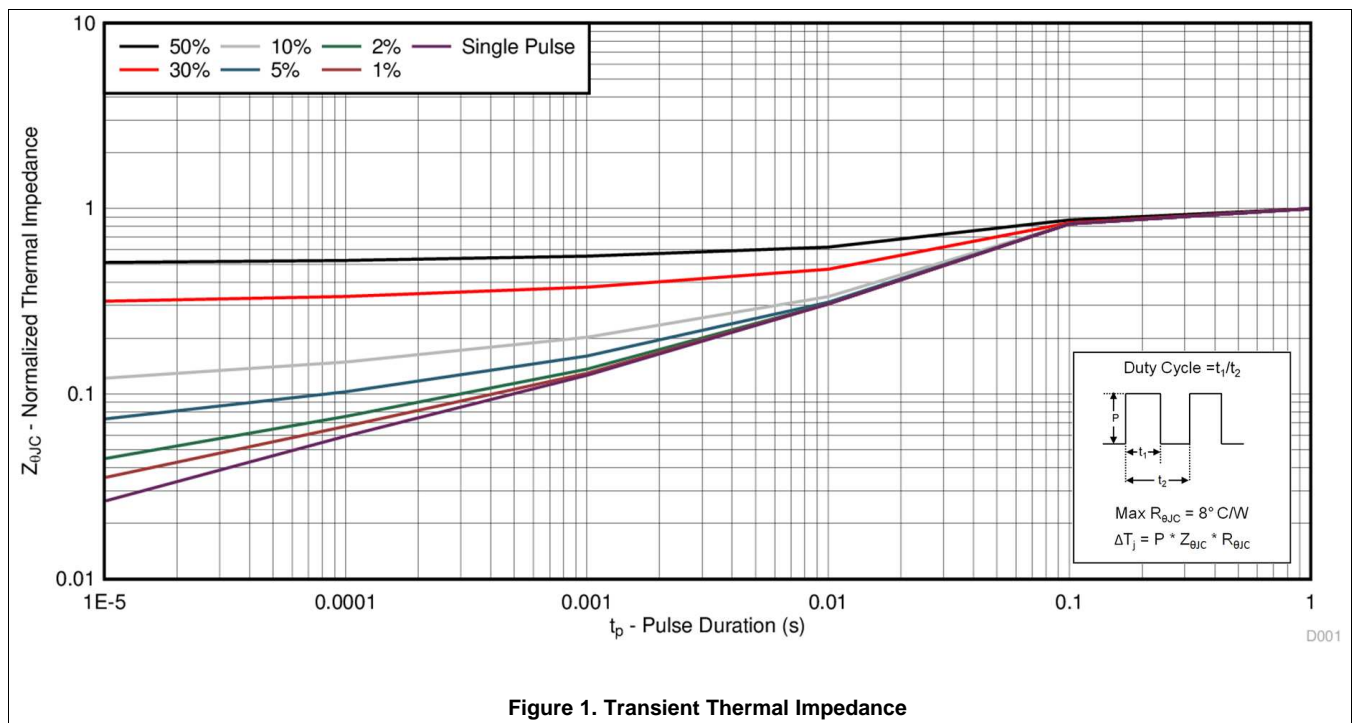
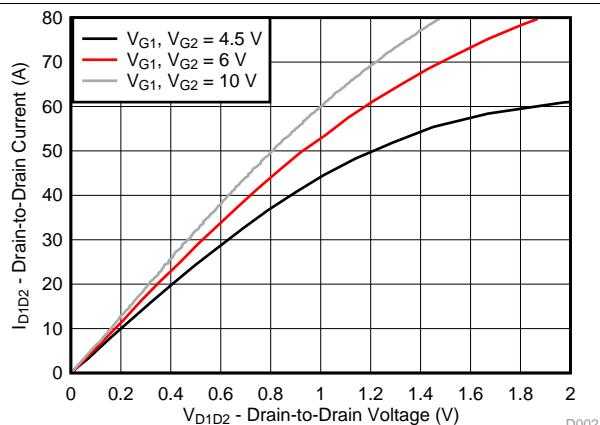


Figure 1. Transient Thermal Impedance

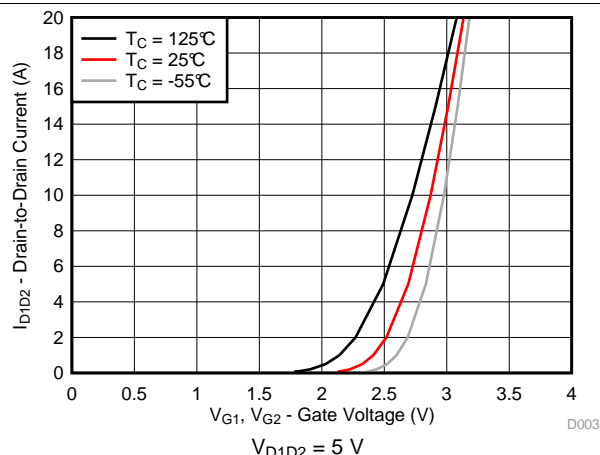
## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

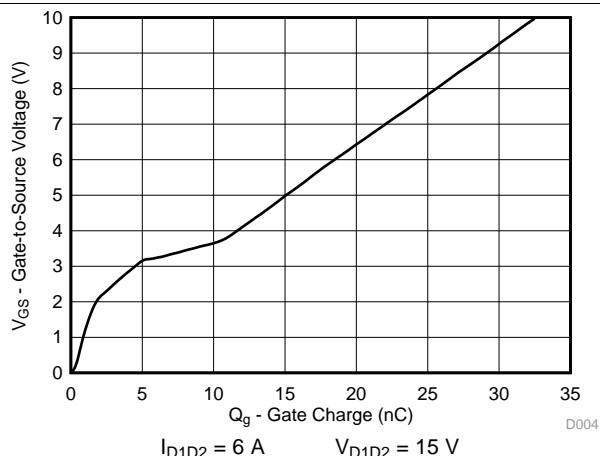


Note: Measurement taken with both gates tied together

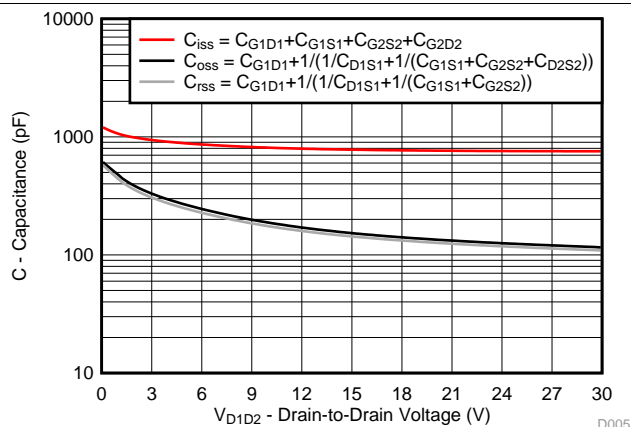
**Figure 2. Saturation Characteristics**



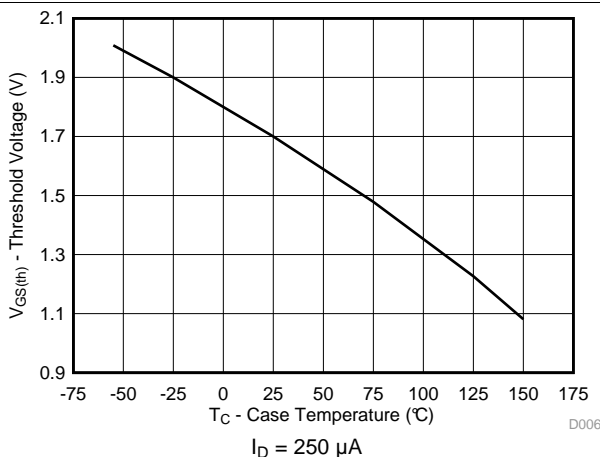
**Figure 3. Transfer Characteristics**



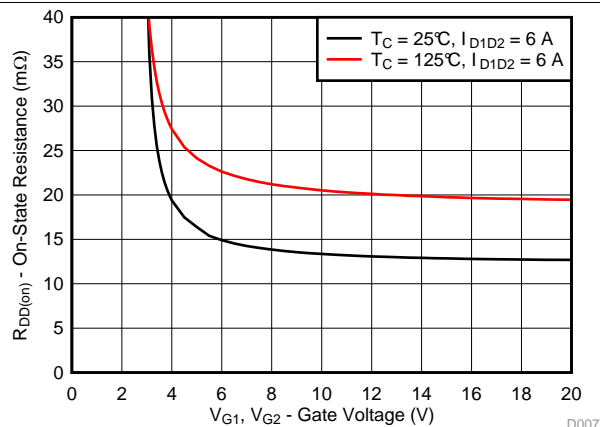
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs Temperature**



**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

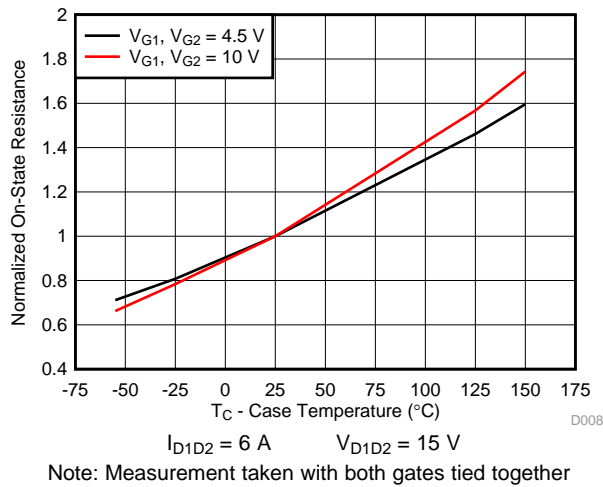


Figure 8. Normalized On-State Resistance vs Temperature

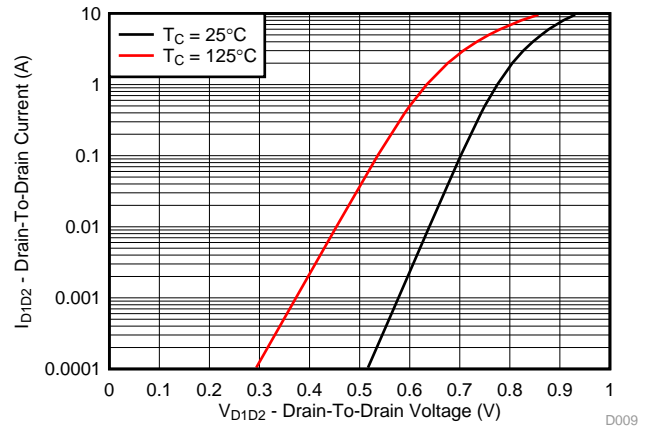


Figure 9. Typical Diode Forward Voltage

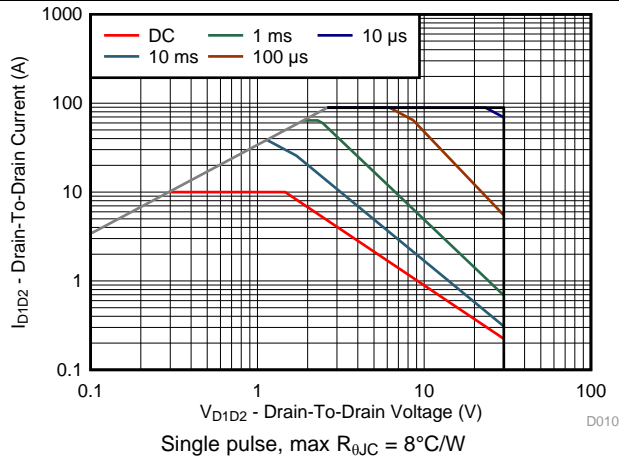


Figure 10. Maximum Safe Operating Area

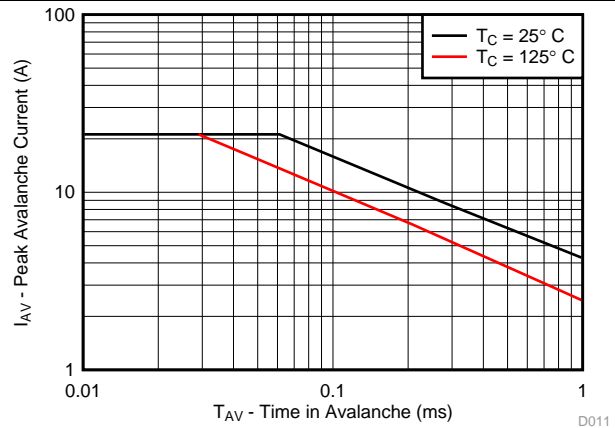


Figure 11. Single Pulse Unclamped Inductive Switching

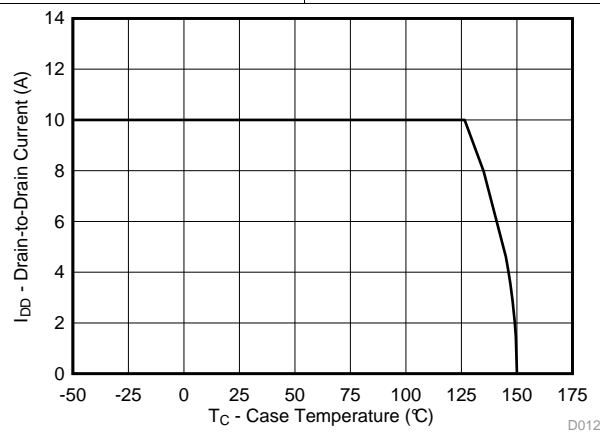


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

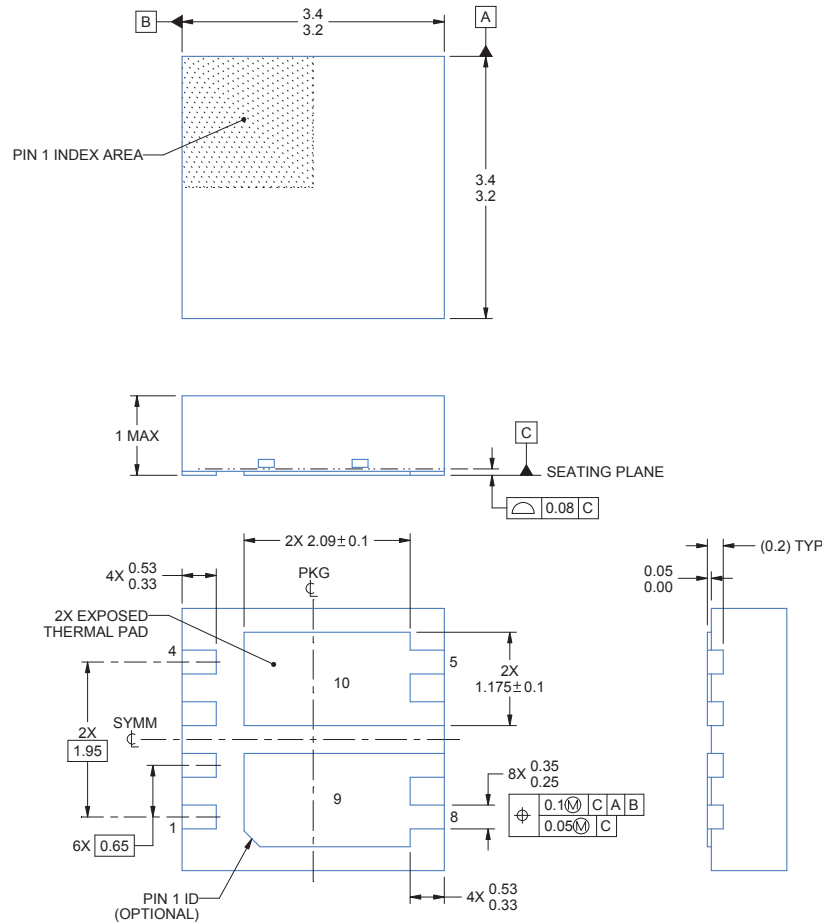
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q3 Package Dimensions



4223409/A 12/2016

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

**Table 1. Pin Configuration**

POSITION	DESIGNATION
Pin 1	Gate 1
Pin 2	Common Source
Pin 3	Gate 2
Pin 4	Common Source
Pins 5, 6	Drain 2
Pins 7, 8	Drain 1





## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD87503Q3E</a>	Active	Production	VSON (DTD)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
CSD87503Q3E.B	Active	Production	VSON (DTD)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
CSD87503Q3EG4.B	Active	Production	VSON (DTD)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
<a href="#">CSD87503Q3ET</a>	Active	Production	VSON (DTD)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
CSD87503Q3ET.B	Active	Production	VSON (DTD)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

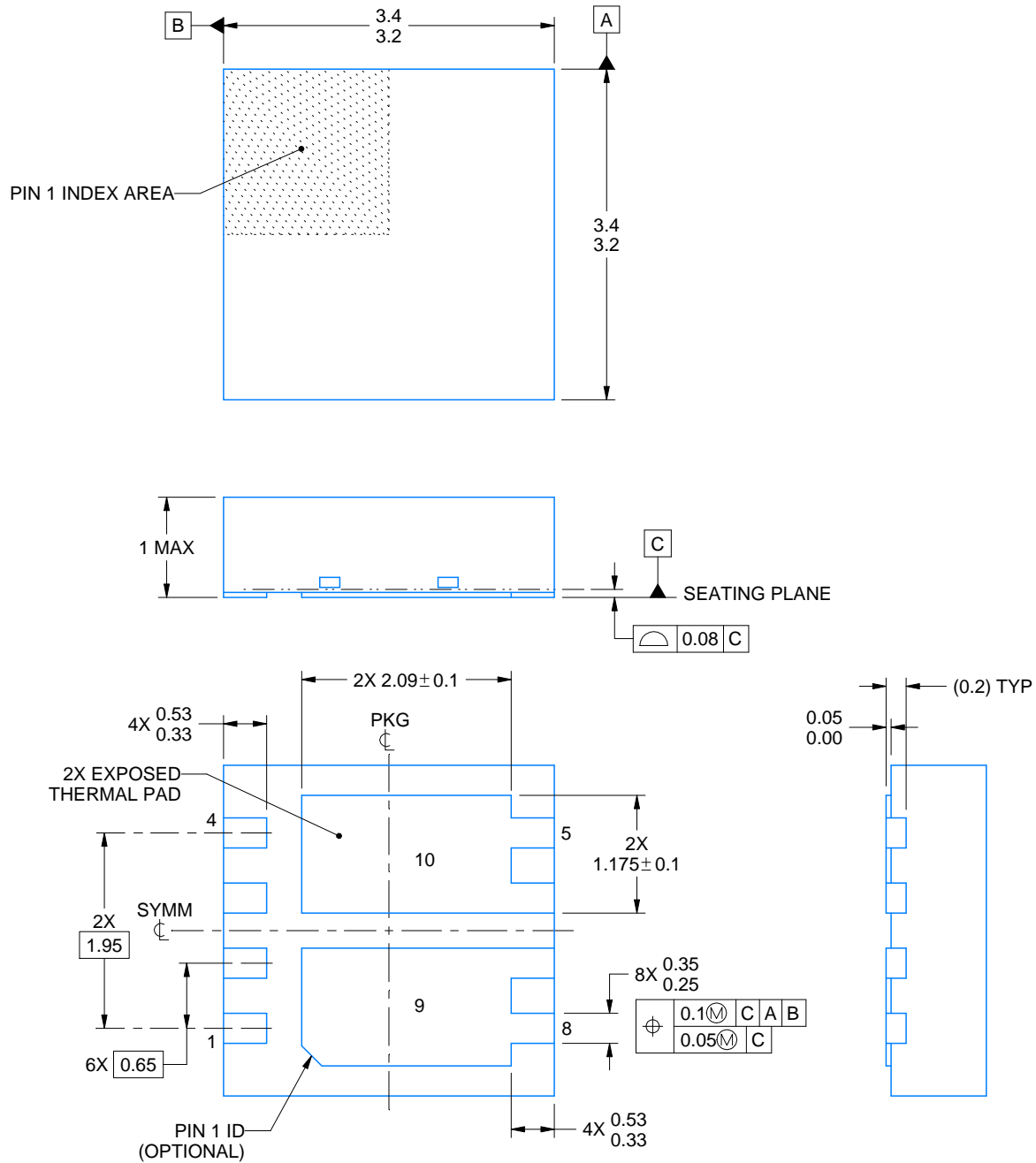
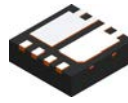
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87503Q3E	VSON	DTD	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87503Q3ET	VSON	DTD	8	250	178.0	13.5	3.6	3.6	1.2	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87503Q3E	VSON	DTD	8	2500	364.0	357.0	31.0
CSD87503Q3ET	VSON	DTD	8	250	189.0	185.0	36.0



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NOTES:

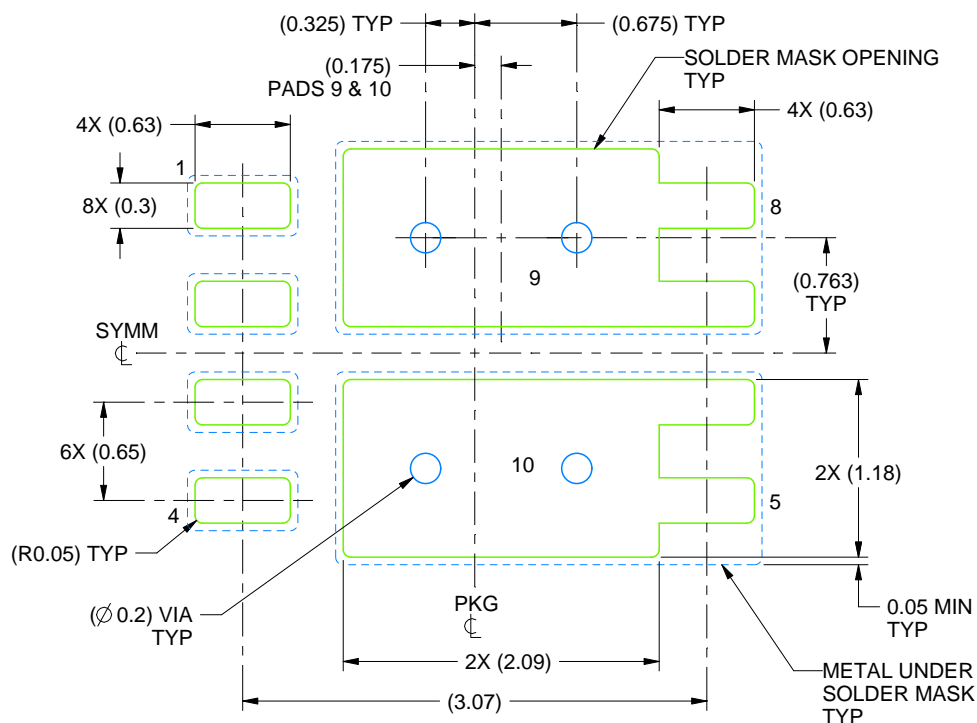
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DTD0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:20X

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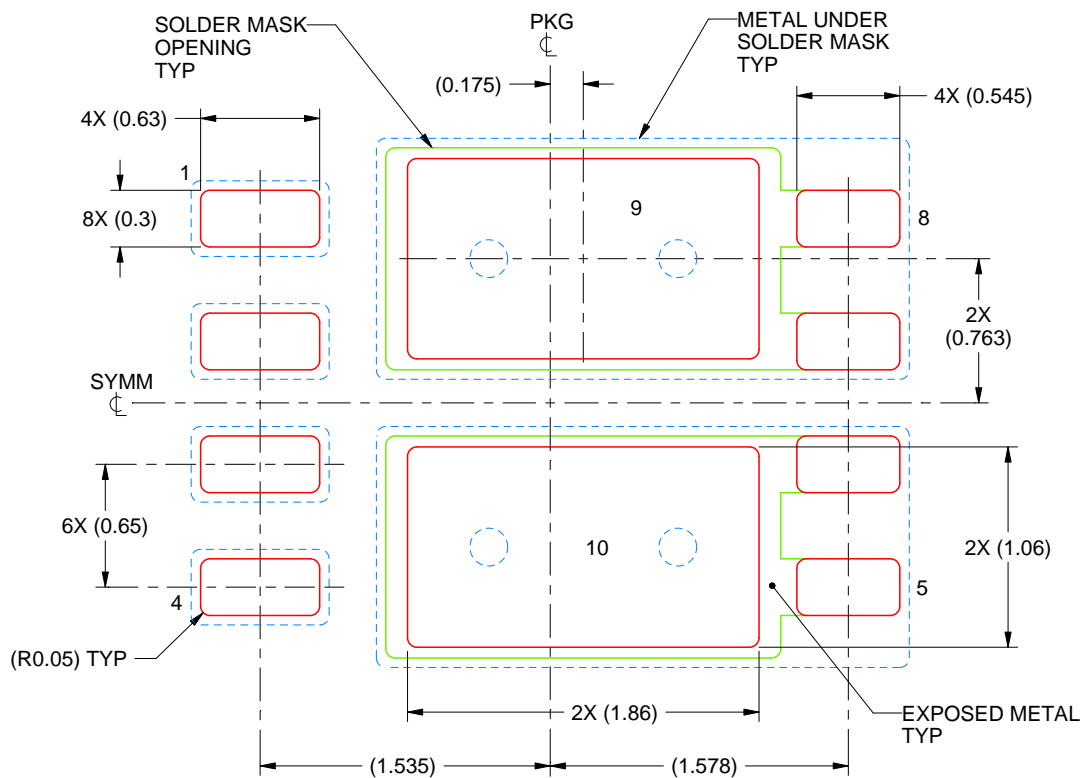
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DTD0008A**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PADS 9 & 10  
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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