



CSD87501L 30-V Dual Common Drain N-Channel NexFET™ Power MOSFET

1 Features

- Low on-resistance
- Small footprint of 3.37 mm × 1.47 mm
- Ultra-low profile – 0.2-mm high
- Lead free
- RoHS compliant
- Halogen free
- Gate ESD protection

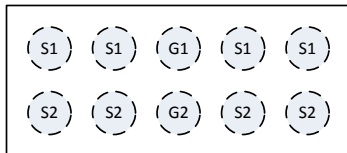
2 Applications

- Battery management
- Battery protection
- USB Type-C / PD

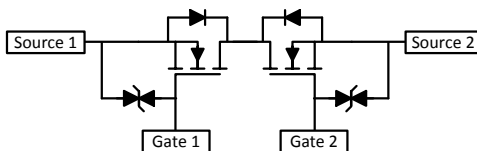
3 Description

This 30-V, 6.6-mΩ, 3.37-mm × 1.47-mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance and gate charge in a small footprint. Its small size and common drain configuration make the device ideal for multi-cell battery pack applications and small handheld devices.

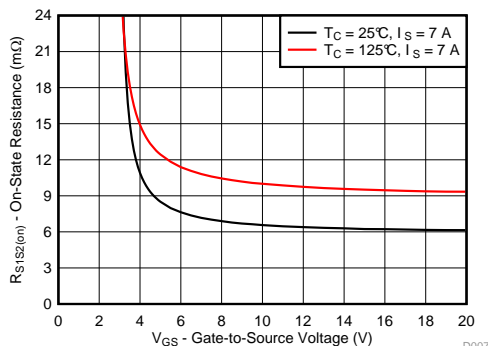
Top View



Configuration



$R_{S1S2(on)}$ vs V_{GS}



Product Summary

| $T_A = 25^\circ\text{C}$ | | TYPICAL VALUE | | UNIT |
|--------------------------|--------------------------------|-------------------------|-----|------|
| V_{S1S2} | Source-to-Source Voltage | 30 | | V |
| Q_g | Gate Charge Total (4.5 V) | 15 | | nC |
| Q_{gd} | Gate Charge Gate-to-Drain | 6.0 | | nC |
| $R_{S1S2(on)}$ | Source-to-Source On-Resistance | $V_{GS} = 4.5\text{ V}$ | 9.3 | mΩ |
| | | $V_{GS} = 10\text{ V}$ | 6.6 | |
| $V_{GS(th)}$ | Threshold Voltage | 1.8 | | V |

Device Information⁽¹⁾

| DEVICE | MEDIA | QTY | PACKAGE | SHIP |
|------------|-------------|------|---|---------------------|
| CSD87501L | 7-Inch Reel | 3000 | 3.37 mm × 1.47 mm Land Grid Array Package | Tape and Reel |
| CSD87501LT | 7-Inch Reel | 250 | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ | | VALUE | UNIT |
|--------------------------|--|------------|------|
| V_{S1S2} | Source-to-Source Voltage | 30 | V |
| V_{GS} | Gate-to-Source Voltage | ±20 | V |
| I_S | Continuous Source Current ⁽¹⁾ | 14 | A |
| I_{SM} | Pulsed Source Current ⁽²⁾ | 72 | A |
| P_D | Power Dissipation | 2.5 | W |
| $V_{(ESD)}$ | Human-Body Model (HBM) | 2 | kV |
| T_J , T_{stg} | Operating Junction, Storage Temperature | –55 to 150 | °C |

(1) Typical $R_{\theta JA} = 50^\circ\text{C/W}$ on a 1-in², 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Typical min Cu $R_{\theta JA} = 135^\circ\text{C/W}$, pulse duration ≤ 100 μs, duty cycle ≤ 1%.

Gate Charge

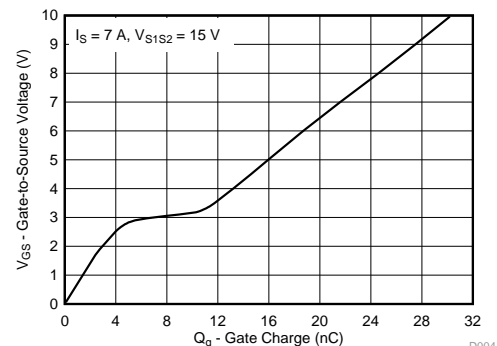


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4 Revision History

| Changes from Revision A (April 2015) to Revision B | Page |
|---|----------|
| • Added <i>Receiving Notification of Documentation Updates</i> section and <i>Community Resources</i> section | 7 |
| • Added Pin Configuration table in the <i>Mechanical, Packaging, and Orderable Information</i> section | 8 |
| Changes from Original (February 2015) to Revision A | Page |
| • Extended Y axis in Figure 9 down to 0.01 A | 4 |

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise stated

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------------|--|-----|------|------|---------------|
| STATIC CHARACTERISTICS | | | | | | |
| BV_{S1S2} | Source-to-source voltage | $V_{GS} = 0\text{ V}$, $I_S = 250\text{ }\mu\text{A}$ | 30 | | | V |
| I_{S1S2} | Source-to-source leakage current | $V_{GS} = 0\text{ V}$, $V_{S1S2} = 24\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate-to-source leakage current | $V_{S1S2} = 0\text{ V}$, $V_{GS} = 20\text{ V}$ | | | 10 | μA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{S1S2} = V_{GS}$, $I_S = 250\text{ }\mu\text{A}$ | 1.3 | 1.8 | 2.3 | V |
| $R_{S1S2(on)}$ | Source-to-source on-resistance | $V_{GS} = 4.5\text{ V}$, $I_S = 7\text{ A}$ | | 9.3 | 11.0 | m Ω |
| | | $V_{GS} = 10\text{ V}$, $I_S = 7\text{ A}$ | | 6.6 | 7.8 | |
| g_{fs} | Transconductance | $V_{S1S2} = 3\text{ V}$, $I_S = 7\text{ A}$ | | 48 | | S |
| DYNAMIC CHARACTERISTICS⁽¹⁾ | | | | | | |
| C_{iss} | Input capacitance | $V_{GS} = 0\text{ V}$, $V_{S1S2} = 15\text{ V}$, $f = 1\text{ MHz}$ | | 1620 | 2110 | pF |
| C_{oss} | Output capacitance | | | 189 | 246 | pF |
| C_{rss} | Reverse transfer capacitance | | | 152 | 198 | pF |
| R_G | Series gate resistance | | | 300 | 450 | Ω |
| Q_g | Gate charge total (4.5 V) | $V_{S1S2} = 15\text{ V}$, $I_S = 7\text{ A}$ | | 15 | 20 | nC |
| Q_g | Gate charge total (10 V) | | | 31 | 40 | nC |
| Q_{gd} | Gate charge gate-to-drain | | | 6.0 | | nC |
| Q_{gs} | Gate charge gate-to-source | | | 5.0 | | nC |
| $Q_{g(th)}$ | Gate charge at V_{th} | | | 2.5 | | nC |
| Q_{oss} | Output charge | $V_{S1S2} = 15\text{ V}$, $V_{GS} = 0\text{ V}$ | | 7.6 | | nC |
| $t_{d(on)}$ | Turn on delay time | $V_{S1S2} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_{S1S2} = 7\text{ A}$, $R_G = 0\text{ }\Omega$ | | 164 | | ns |
| t_r | Rise time | | | 260 | | ns |
| $t_{d(off)}$ | Turn off delay time | | | 709 | | ns |
| t_f | Fall time | | | 712 | | ns |

(1) Dynamic characteristics values specified are per single FET.

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ unless otherwise stated

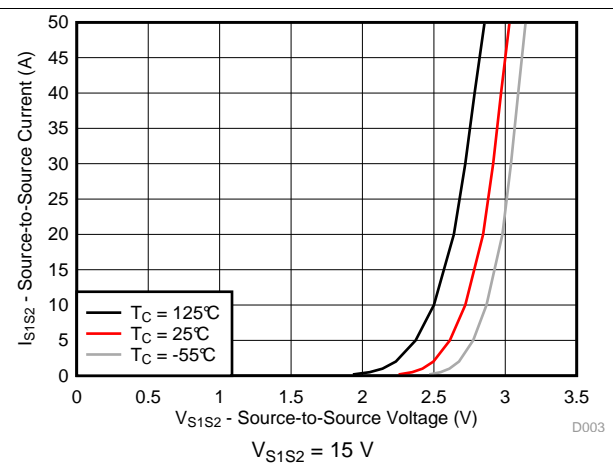
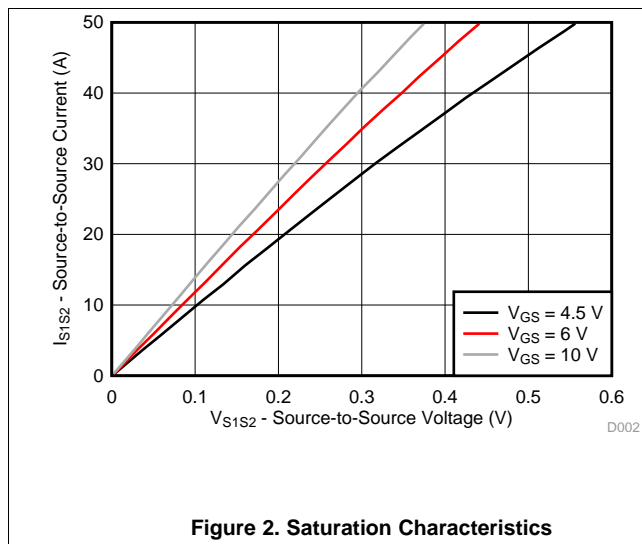
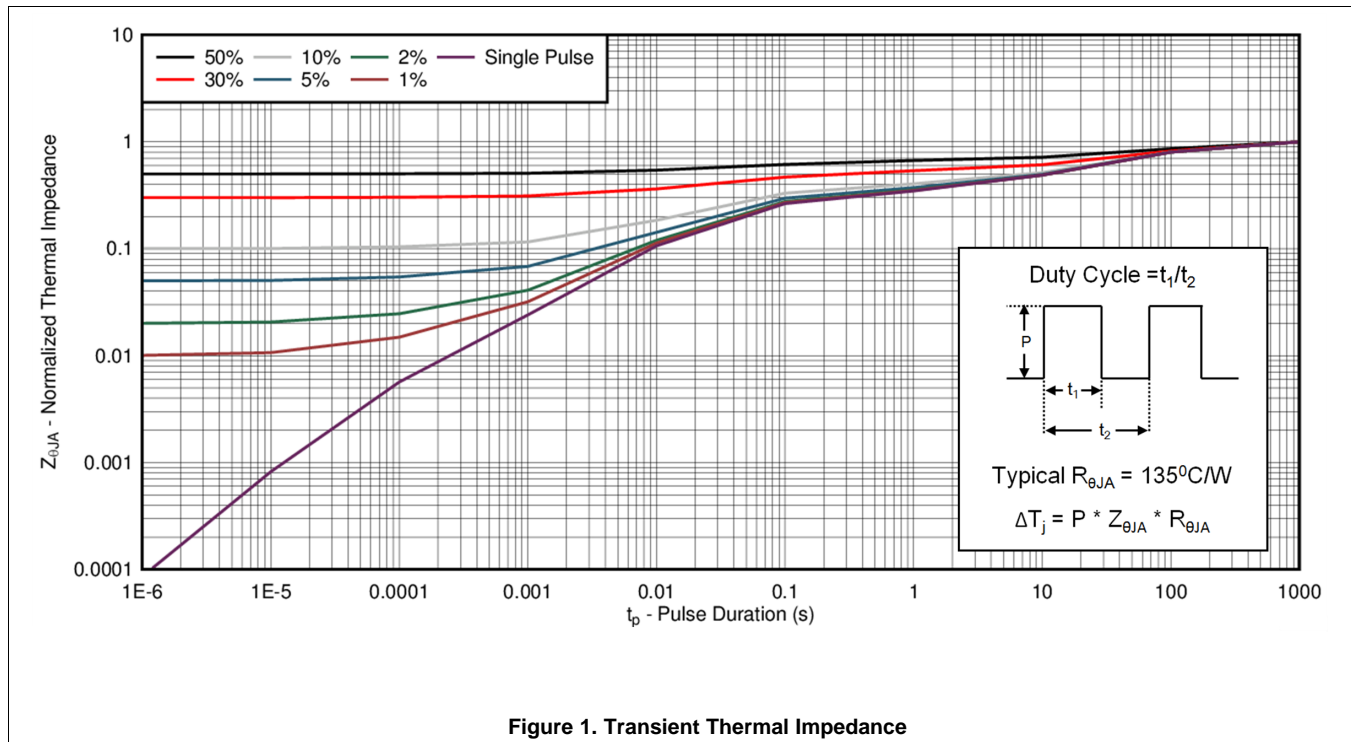
| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|-----------------|---|-----|-----|-----|--------------------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽¹⁾ | | 135 | | $^\circ\text{C/W}$ |
| | Junction-to-ambient thermal resistance ⁽²⁾ | | 50 | | |

(1) Device mounted on FR4 material with minimum Cu mounting area.

(2) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise stated



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise stated

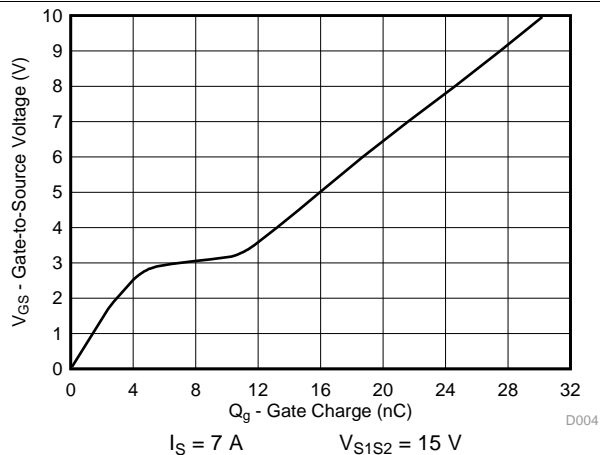


Figure 4. Gate Charge

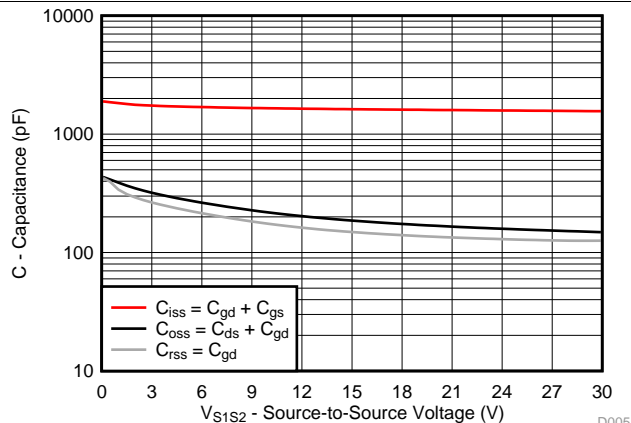


Figure 5. Capacitance

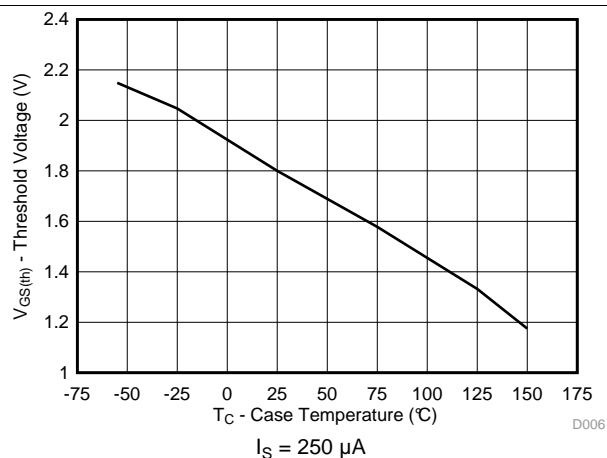


Figure 6. Threshold Voltage vs Temperature

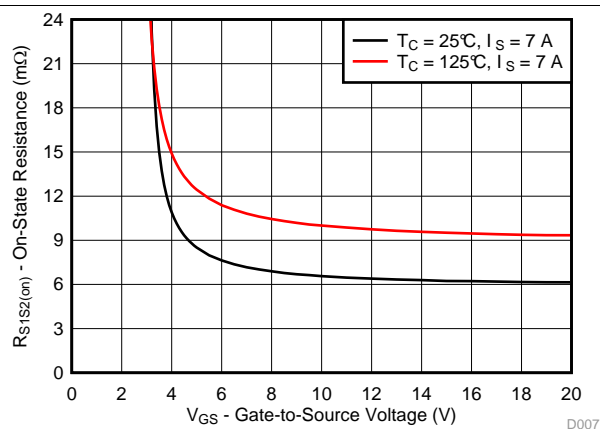


Figure 7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage

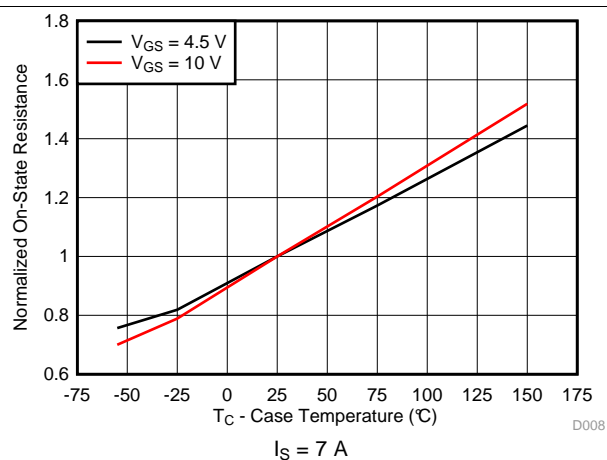


Figure 8. Normalized On-State Resistance vs Temperature

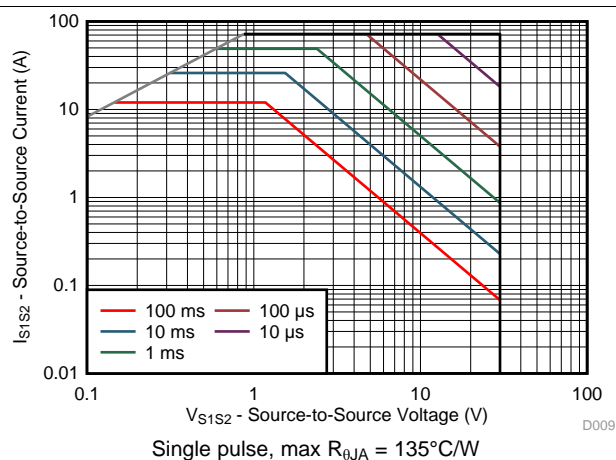


Figure 9. Maximum Safe Operating Area

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise stated

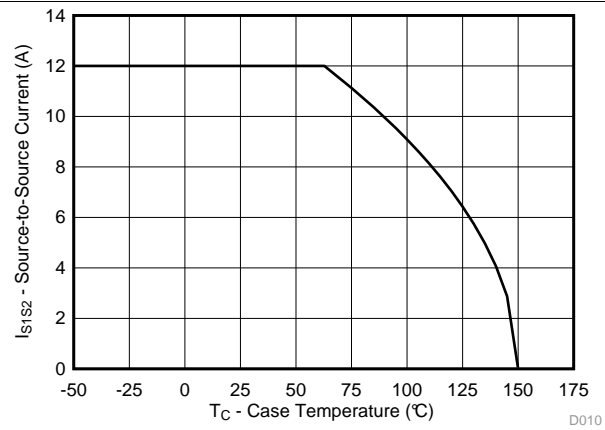


Figure 10. Maximum Source Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

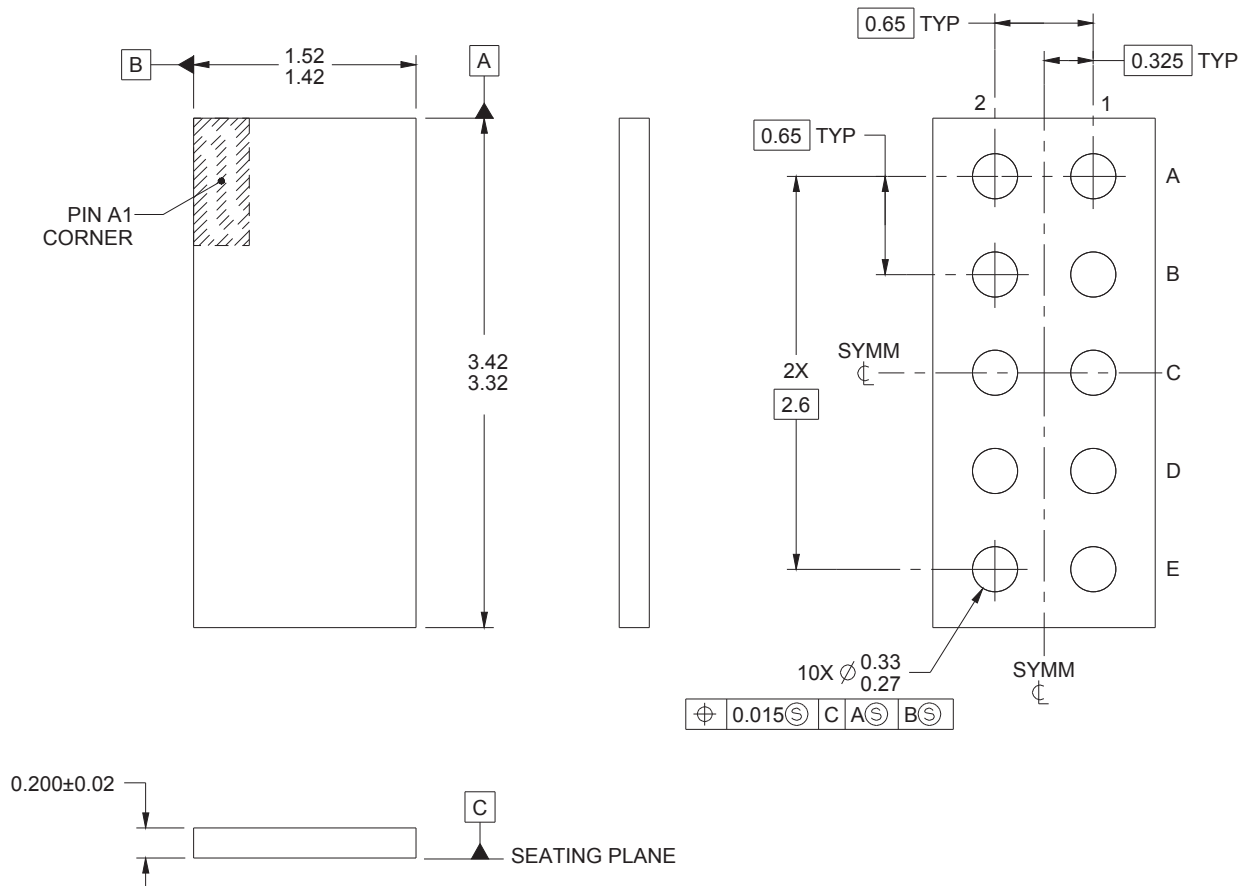
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions

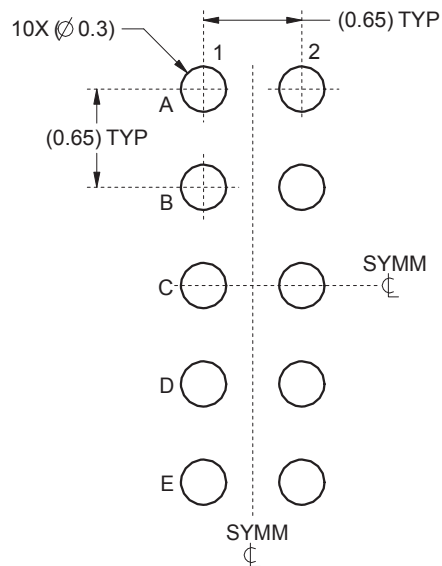


All dimensions in millimeters.

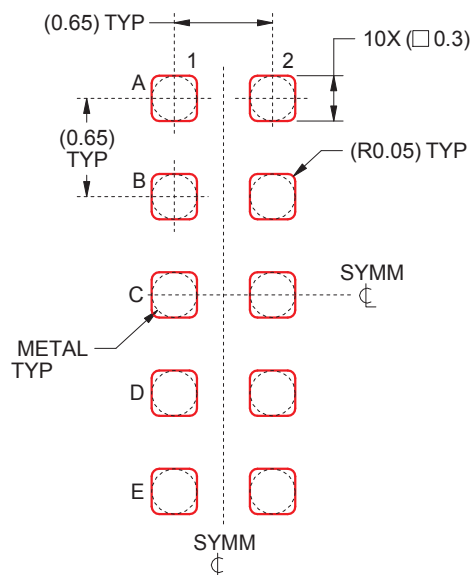
Table 1. Pin Configuration

| Position | Designation |
|----------------|-------------|
| A1, B1, D1, E1 | Source 1 |
| C1 | Gate 1 |
| A2, B2, D2, E2 | Source 2 |
| C2 | Gate 2 |

7.2 Recommended PCB Pattern



7.3 Recommended Stencil Pattern



All dimensions are in millimeters unless otherwise noted.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------|---------------|----------------------|---------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CSD87501L | Active | Production | PICOSTAR (YJG) 10 | 3000 LARGE T&R | Yes | NIAU | Level-1-260C-UNLIM | - | CSD87501 |
| CSD87501L.B | Active | Production | PICOSTAR (YJG) 10 | 3000 LARGE T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | CSD87501 |
| CSD87501LT | Active | Production | PICOSTAR (YJG) 10 | 250 SMALL T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | CSD87501 |
| CSD87501LT.B | Active | Production | PICOSTAR (YJG) 10 | 250 SMALL T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | CSD87501 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CSD87501LT | PICOSTAR | YJG | 10 | 250 | 330.0 | 12.4 | 1.62 | 3.62 | 0.37 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| CSD87501LT | PICOSTAR | YJG | 10 | 250 | 335.0 | 335.0 | 25.0 |

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