











CSD87384M

SLPS415D - SEPTEMBER 2013 - REVISED MARCH 2015

CSD87384M Synchronous Buck NexFET™ Power Block II

Features

- Half-Bridge Power Block
- 90.5% System Efficiency at 25 A
- Up to 30 A Operation
- High Density 5 mm x 3.5 mm LGA Footprint
- **Double-Side Cooling Capability**
- Ultra-Low Profile 0.48 mm Max
- Optimized for 5 V Gate Drive
- Low Switching Losses
- Ultra-Low Inductance Package
- **RoHS Compliant**
- Halogen Free
- Pb-Free

2 Applications

- Synchronous Buck Converters
 - High Frequency Applications
 - High Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters

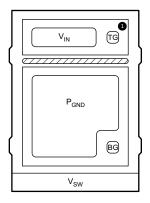
3 Description

The CSD87384M NexFET™ Power Block II is a highly optimized design for synchronous buck applications offering high current and high efficiency capability in a small 5.0 mm x 3.5 mm outline. Optimized for 5 V gate drive applications, this product offers an efficient and flexible solution capable of providing a high density power supply when paired with any 5 V gate drive from an external controller or driver.

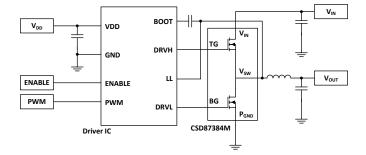
Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD87384M	13-Inch Reel	2500	5 × 3.5 LGA	Tape and
CSD87384MT	7-Inch Reel	250	5 x 5.5 LGA	Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Circuit



Typical Power Block Efficiency and Power Loss

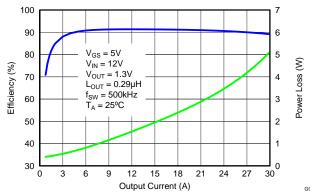




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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2014) to Revision D	Page
Changed capacitance units to read pF in Figure 15	8
Changed capacitance units to read pF in Figure 16	8
Changes from Revision A (September 2013) to Revision B	Page
Added small reel info	
Changed Figure 16	8
Changes from Original (September 2013) to Revision A	Page
Changed V _{GS(th)} from 1.0 V to 1.1 V in the Electrical Characteristics table	4



5 Specifications

5.1 Absolute Maximum Ratings

 $T_{\Delta} = 25^{\circ}C$ (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage		V _{IN} to P _{GND}	-0.8	30	
		V _{SW} to P _{GND}		30	
		V _{SW} to P _{GND} (10 ns)		32	V
	T _G to V _{SW}	-8	10		
		B _G to P _{GND}	-8	10	
I _{DM}	Pulsed Current Rating ⁽²⁾			95	Α
P_D	Power Dissipation (3)			8	W
г	Avalancha Energy	Sync FET, I _D = 68, L = 0.1 mH		231	I
E _{AS}	Avaianche Energy	/alanche Energy Control FET, I _D = 31, L = 0.1 mH		48	mJ
T_{J}	Operating Junction		-55	150	°C
T _{stg}	Storage Temperature Rang	е	-55	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

 $T_A = 25$ °C (unless otherwise noted)

			MIN	MAX	UNIT
V_{GS}	Gate Drive Voltage		4.5	8	V
V_{IN}	Input Supply Voltage			24	V
$f_{\sf SW}$	Switching Frequency	$C_{BST} = 0.1 \mu F (min)$	200	1500	kHz
		No Airflow		30	Α
Operat	ing Current	With Airflow (200 LFM)		35	Α
		With Airflow + Heat Sink		40	Α
T_J	Operating Temperature			125	°C

5.3 Power Block Performance

 $T_A = 25$ °C (unless otherwise noted)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
P _{LOSS}	Power Loss ⁽¹⁾	$V_{IN} = 12 \text{ V}, V_{GS} = 5 \text{ V}$ $V_{OUT} = 1.3 \text{ V}, I_{OUT} = 25 \text{ A}$ $f_{SW} = 500 \text{ kHz}$ $L_{OUT} = 0.3 \mu\text{H}, T_{J} = 25^{\circ}\text{C}$		3.7		W
I _{QVIN}	V _{IN} Quiescent Current	T_G to $T_{GR} = 0$ V B_G to $P_{GND} = 0$ V		10		μΑ

⁽¹⁾ Measurement made with six 10 μ F (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5 V driver IC.

⁽²⁾ Pulse Duration ≤50 µs, duty cycle ≤0.01

⁽³⁾ Device mounted on FR4 material with 1 inch² (6.45 cm²) Cu



5.4 Thermal Information

 $T_A = 25$ °C (unless otherwise stated)

	THERMAL METRIC	MIN	TYP	MAX	UNIT
D	Junction-to-ambient thermal resistance (Min Cu) (1)			153	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (Max Cu) (2)(1)			67	°C/W
D	Junction-to-case thermal resistance (Top of package) (1)			3.0	C/VV
$R_{\theta JC}$	Junction-to-case thermal resistance (P _{GND} Pin) ⁽¹⁾			1.25	

⁽¹⁾ R_{\text{\tinte\tint{\text{\tinte\tint{\text{\ti}\text{\t}

5.5 Electrical Characteristics

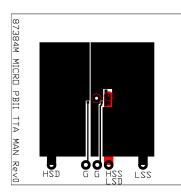
 $T_A = 25$ °C (unless otherwise stated)

	DADAMETER	TEST CONDITIONS	Q1 C	ontrol FE	ΕT	Q2	UNIT		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNII
STATIC	CHARACTERISTICS								
BV _{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}, I_{DS} = 250 \mu\text{A}$	30			30			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 24 V			1			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 10 V			100			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250 \ \mu A$	1.1		1.9	1.1		1.7	V
D	Danie de Comme Confessor de con	$V_{GS} = 4.5 \text{ V}, I_{DS} = 25 \text{ A}$		7.5	8.9		2.15	2.6	0
R _{DS(on)}	Drain-to-Source On-Impedance	V _{GS} = 8 V, I _{DS} = 25 A		6.4	7.7		1.95	2.4	mΩ
g_{fs}	Transconductance	V _{DS} = 10 V, I _{DS} = 25 A		67			240		S
DYNAM	IIC CHARACTERISTICS								
C _{ISS}	Input Capacitance (1)			884	1150		3760	4890	рF
Coss	Output Capacitance (1)	$V_{GS} = 0 \text{ V}, V_{DS} = 15 \text{ V},$		452	588		1110	1440	рF
C _{RSS}	Reverse Transfer Capacitance	f = 1MHz		19.4	25.2		87	114	pF
R _G	Series Gate Resistance (1)			1.0	2.0		0.7	1.4	Ω
Qg	Gate Charge Total (4.5 V) (1)			7.1	9.2		31	40	nC
Q _{gd}	Gate Charge – Gate-to-Drain	V _{DS} = 15 V,		1.5			8.6		nC
Q _{gs}	Gate Charge – Gate-to-Source	I _{DS} = 25 A		2.7			8.6		nC
Q _{g(th)}	Gate Charge at V _{th}			1.3			5.4		nC
Q _{OSS}	Output Charge	V _{DD} = 12 V, V _{GS} = 0 V		11.3			37		nC
t _{d(on)}	Turn On Delay Time			8.7			17.5		ns
t _r	Rise Time	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$		56			49		ns
t _{d(off)}	Turn-Off Delay Time	$I_{DS} = 25 \text{ A}, R_G = 2 \Omega$		14			29		ns
t_f	Fall Time			7.6			8.2		ns
DIODE (CHARACTERISTICS							'	
V _{SD}	Diode Forward Voltage	I _{DS} = 25 A, V _{GS} = 0 V		0.85			0.80		V
Q _{rr}	Reverse Recovery Charge	V _{dd} = 15 V, I _F = 25 A,		21			51		nC
t _{rr}	Reverse Recovery Time	di/dt = 300 A/μs		21			32		ns

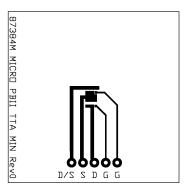
⁽¹⁾ Specified by design

⁽²⁾ Device mounted on FR4 material with 1 inch² (6.45 cm²) Cu.





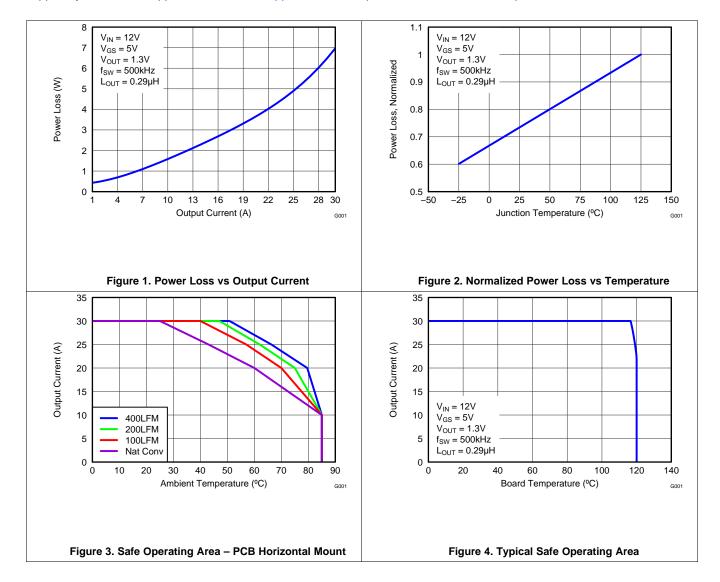
Max $R_{\theta JA} = 67^{\circ}\text{C/W}$ when mounted on 1 inch² (6.45 cm²) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA} = 153^{\circ}\text{C/W}$ when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.6 Typical Power Block Device Characteristics

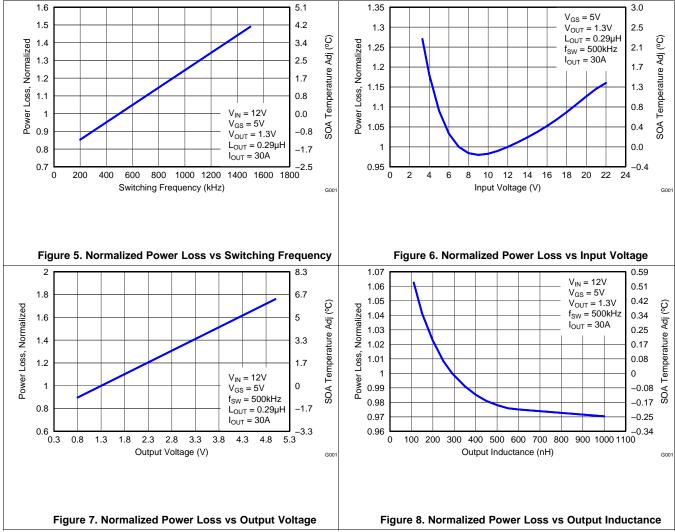
 T_J = 125°C, unless stated otherwise. For Figure 3 and Figure 4, the Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.





Typical Power Block Device Characteristics (continued)

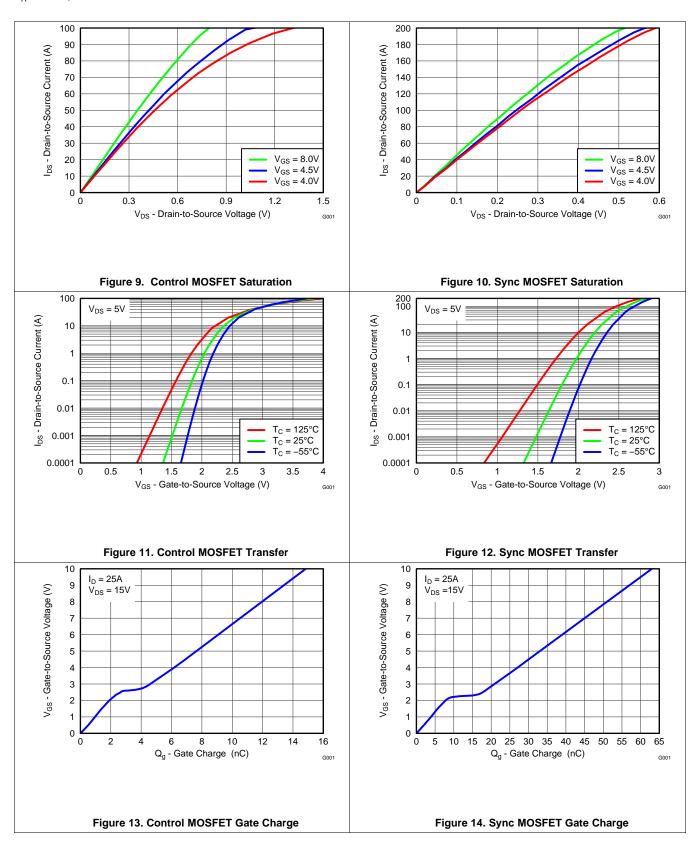
 T_J = 125°C, unless stated otherwise. For Figure 3 and Figure 4, the Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.





5.7 Typical Power Block MOSFET Characteristics

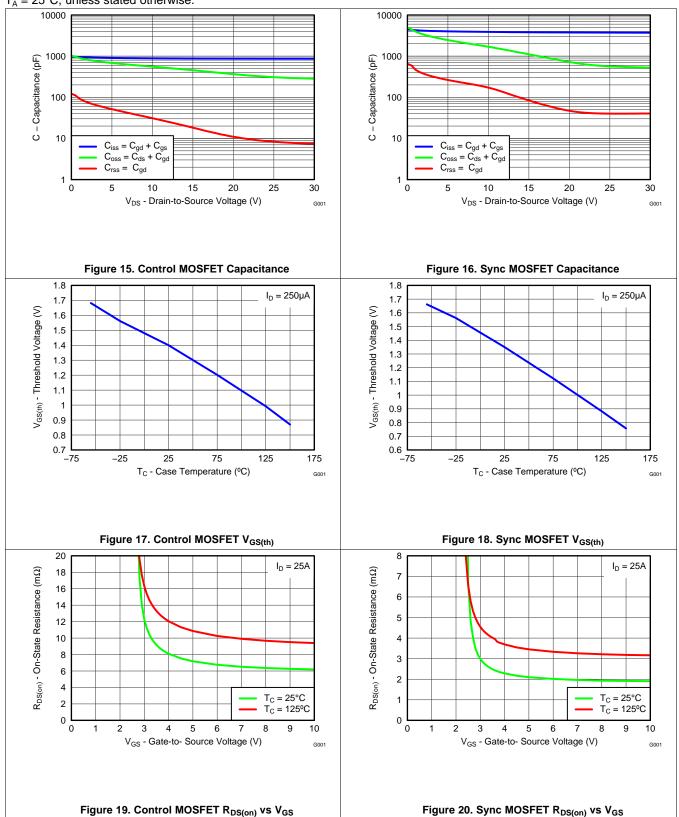
 $T_A = 25$ °C, unless stated otherwise.



TEXAS INSTRUMENTS

Typical Power Block MOSFET Characteristics (continued)

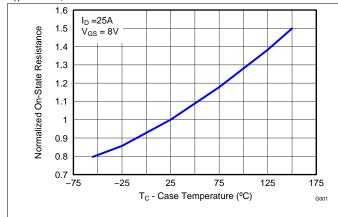
 $T_A = 25$ °C, unless stated otherwise.





Typical Power Block MOSFET Characteristics (continued)

 $T_A = 25$ °C, unless stated otherwise.



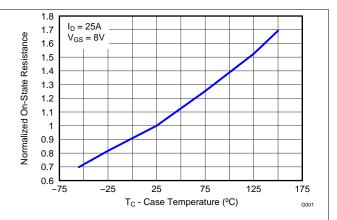
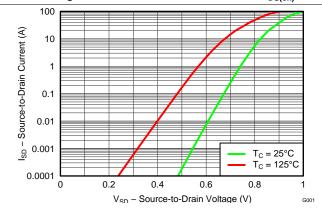


Figure 21. Control MOSFET Normalized R_{DS(on)}





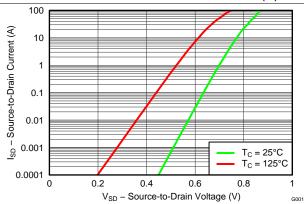


Figure 23. Control MOSFET Body Diode

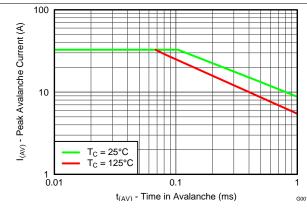


Figure 24. Sync MOSFET Body Diode

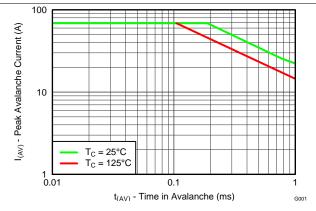


Figure 25. Control MOSFET Unclamped Inductive Switching

Figure 26. Sync MOSFET Unclamped Inductive Switching



6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI 's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87384M NexFET™ power block is an optimized design for synchronous buck applications using 5 V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored toward a more systemscentric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.2 Power Loss Curves

MOSFET-centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. To simplify the design process for engineers, TI has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87384M as a function of load current. This curve is measured by configuring and running the CSD87384M as it would be in the final application (see Figure 27). The measured power loss is the CSD87384M loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) = Power Loss$$
 (1)

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.3 Safe Operating Curves (SOA)

The SOA curves in the CSD87384M data sheet provide guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 inches $(W) \times 3.5$ inches $(L) \times 0.062$ inch (T) and 6 copper layers of 1 oz. copper thickness.

6.4 Normalized Curves

The normalized curves in the CSD87384M data sheet provide guidance on the Power Loss and SOA adjustments based on their application-specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of systems conditions. The primary y-axis is the normalized change in power loss and the secondary y-axis is the change in system temperature required to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.



Normalized Curves (continued)

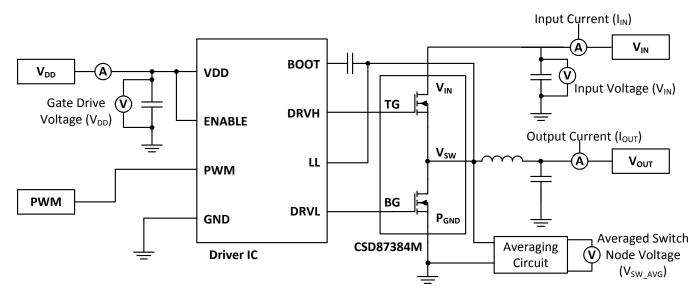


Figure 27. Typical Application



6.5 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.5.1 Design Example

Operating Conditions:

- Output Current = 20 A
- Input Voltage = 4 V
- Output Voltage = 1 V
- Switching Frequency = 800 kHz
- Inductor = 0.2 μH

6.5.2 Calculating Power Loss

- Power Loss at 20 A = 3.5 W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.18 (Figure 6)
- Normalized Power Loss for output voltage ≈ 0.94 (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.15 (Figure 5)
- Normalized Power Loss for output inductor ≈ 1.02 (Figure 8)
- Final calculated Power Loss = 3.5 W x 1.18 x 0.94 x 1.15 x 1.02 ≈ 4.6 W

6.5.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 1.5°C (Figure 6)
- SOA adjustment for output voltage ≈ -0.5°C (Figure 7)
- SOA adjustment for switching frequency ≈ 1.2°C (Figure 5)
- SOA adjustment for output inductor ≈ 0.2°C (Figure 8)
- Final calculated SOA adjustment = $1.5 + (-0.5) + 1.2 + 0.2 \approx 2.4$ °C

In the previous design example, the estimated power loss of the CSD87384M would increase to 4.6 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 2.4°C. Figure 28 graphically shows how the SOA curve would be adjusted accordingly.

- 1. Start by drawing a horizontal line from the application current to the SOA curve.
- 2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
- 3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 2.4°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.

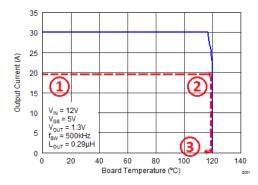


Figure 28. Power Block SOA



7 Layout

7.1 Layout Guidelines

7.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1.2 Electrical Performance

The CSD87384M has the ability to switch voltages at rates greater than 10 kV/µs. Take special care with the PCB layout design and placement of the input capacitors, inductor, and output capacitors.

- The placement of the input capacitors relative to VIN and PGND pins of CSD87384M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 29). The example in Figure 29 uses 1 × 10 nF 0402 25 V and 4 × 10 µF 1206 25 V ceramic capacitors (TDK part number C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C21, C5, C8, C19, and C18 should follow in order.
- The switching node of the output inductor should be placed relatively close to the Power Block II CSD87384M VSW pins. Minimizing the VSW node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. See Figure 29. (1)

7.1.3 Thermal Performance

The CSD87384M has the ability to utilize the PGND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that wicks down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 29 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

7.2 Layout Example

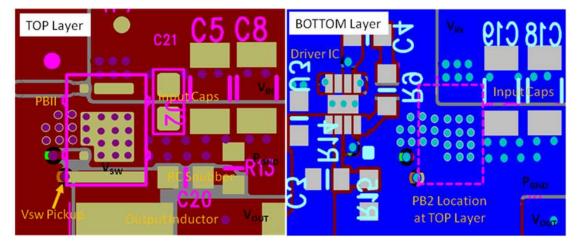


Figure 29. Recommended PCB Layout (Top Down View)

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla



8 Device and Documentation Support

8.1 Trademarks

NexFET is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

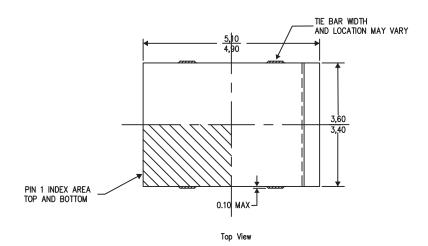


9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation

9.1 CSD87384M Package Dimensions

0.254 TYP



0.55 0.45 MAX

Side View

SEATING PLANE

0.840 1.040 0,442 0,642 0.30TYP(x2) 0,32X0.32(x2) 2.42TYP 1.80TYP PIN 3 1.80TYF 0,442 .26TYP R0,08 TYP 0.50TYP 0,708 Die Pad Corner Radii=0.08, Unless Specified 0,908

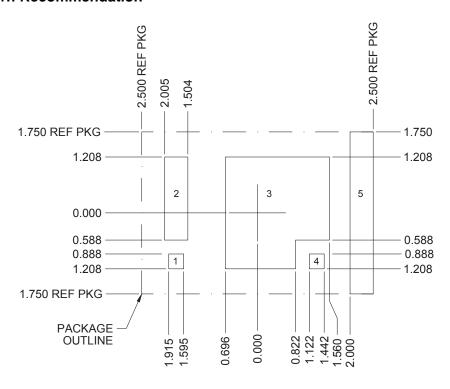
Pin Configuration

Bottom View

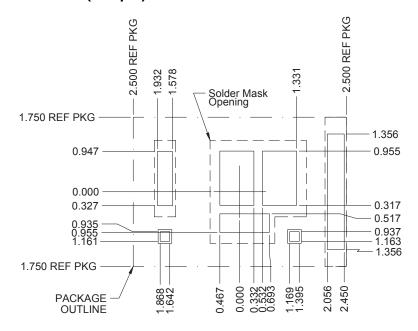
Position	Designation
Pin 1	TG
Pin 2	V _{IN}
Pin 3	P_{GND}
Pin 4	BG
Pin 5	V _{SW}



9.2 Land Pattern Recommendation

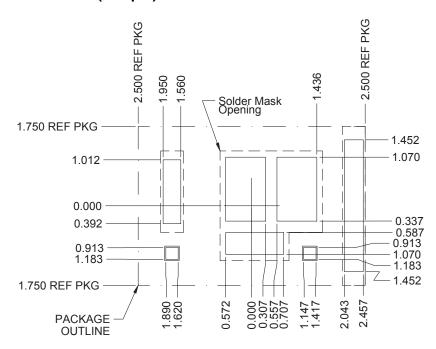


9.3 Stencil Recommendation (100 µm)



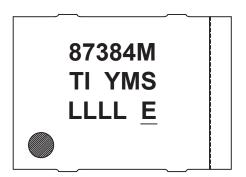


9.4 Stencil Recommendation (125 µm)



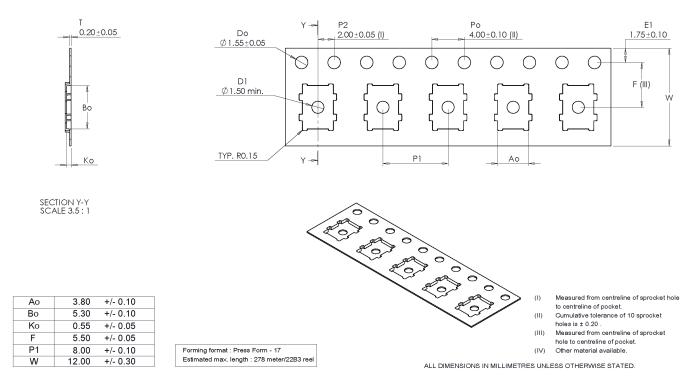
For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

9.5 Pin Drawing





9.6 CSD87384M Embossed Carrier Tape Dimensions



(1) Pin 1 is oriented in the top-left quadrant of the tape enclosure (closest to the carrier tape sprocket holes).

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
CSD87384M	Active	Production	PTAB (MPB) 5	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87384M
CSD87384M.B	Active	Production	PTAB (MPB) 5	2500 LARGE T&R	-	Call TI	Call TI	-55 to 150	
CSD87384MT	Active	Production	PTAB (MPB) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87384M
CSD87384MT.B	Active	Production	PTAB (MPB) 5	250 SMALL T&R	-	Call TI	Call TI	-55 to 150	

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

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⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

De	vice	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD8	7384M	PTAB	MPB	5	2500	330.0	12.4	3.8	5.3	0.55	8.0	12.0	Q1
CSD8	7384MT	PTAB	MPB	5	250	180.0	12.4	3.8	5.3	0.55	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87384M	PTAB	MPB	5	2500	346.0	346.0	33.0
CSD87384MT	PTAB	MPB	5	250	182.0	182.0	20.0

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