

CSD87350Q5D Synchronous Buck NexFET™ Power Block

1 Features

- Half-Bridge Power Block
- 90% system Efficiency at 25 A
- Up to 40-A Operation
- High-Frequency Operation (Up to 1.5 MHz)
- High-Density SON 5-mm × 6-mm Footprint
- Optimized for 5-V Gate Drive
- Low-Switching Losses
- Ultra-Low-Inductance Package
- RoHS Compliant
- Halogen Free
- Lead-Free Terminal Plating

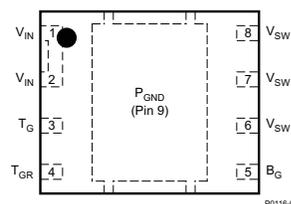
2 Applications

- Synchronous Buck Converters
 - High-Frequency Applications
 - High-Current, Low-Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters
- IMVP, VRM, and VRD Applications

3 Description

The CSD87350Q5D NexFET™ power block is an optimized design for synchronous buck applications offering high-current, high-efficiency, and high-frequency capability in a small 5-mm × 6-mm outline. Optimized for 5-V gate drive applications, this product offers a flexible solution capable of offering a high-density power supply when paired with any 5-V gate drive from an external controller or driver.

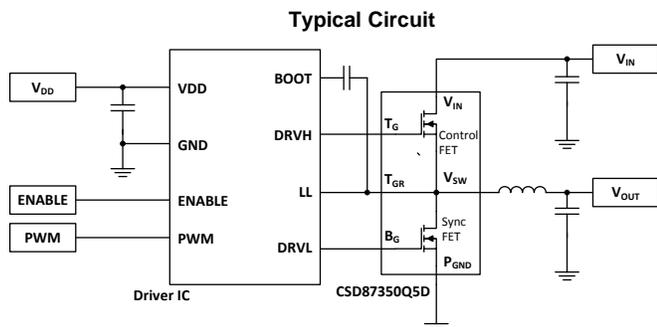
Top View



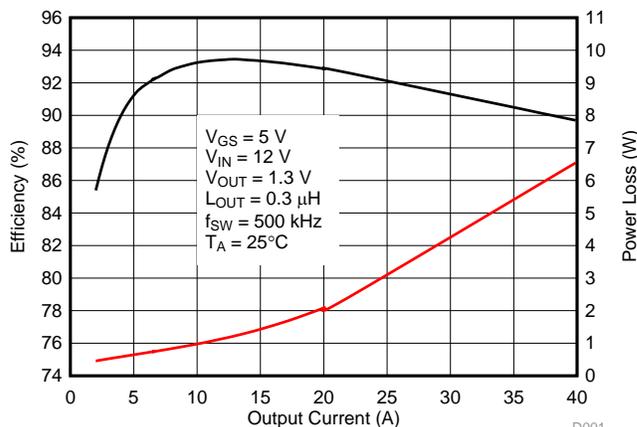
Device Information(1)

| DEVICE | MEDIA | QTY | PACKAGE | SHIP |
|-------------|--------------|------|---------------------------------------|---------------|
| CSD87350Q5D | 13-Inch Reel | 2500 | SON 5-mm × 6-mm Plastic Package | Tape and Reel |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Power Block Efficiency and Power Loss



D001



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4 Revision History

| Changes from Revision D (September 2014) to Revision E | Page |
|---|-------------|
| • Added note for I_{DM} in the <i>Absolute Maximum Ratings</i> table | 3 |
| • Added <i>Receiving Notification of Documentation Updates</i> section and <i>Community Resources</i> section in the <i>Documentation Support</i> section | 17 |

| Changes from Revision C (October 2011) to Revision D | Page |
|--|-------------|
| • Added <i>Handling Rating</i> table, <i>Application and Implementation</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |

| Changes from Revision B (September 2011) to Revision C | Page |
|--|-------------|
| • Changed "DIM a" Millimeter Max value From: 1.55 To: 1.5 and Inches Max value From: 0.061 To: 0.059 | 18 |

| Changes from Revision A (August 2011) to Revision B | Page |
|--|-------------|
| • Replaced $R_{DS(on)}$ with $Z_{DS(on)}$ | 4 |
| • Added Equivalent System Performance section | 10 |
| • Added the Comparison of $R_{DS(on)}$ vs $Z_{DS(on)}$ table | 12 |
| • Added Electrical Performance bullet | 15 |

| Changes from Original (March 2011) to Revision A | Page |
|--|-------------|
| • Changed Power Dissipation, P_D in the <i>Absolute Maximum Ratings</i> table From: 13 W to 12 W | 3 |

5 Specifications

5.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------|--------------------------------------|--|-----|------------------|
| Voltage | V_{IN} to P_{GND} | -0.8 | 30 | V |
| | T_G to T_{GR} | -8 | 10 | V |
| | B_G to P_{GND} | -8 | 10 | V |
| I_{DM} | Pulsed current rating ⁽²⁾ | | 120 | A |
| P_D | Power dissipation | | 12 | W |
| E_{AS} | Avalanche energy | Sync FET, $I_D = 105\text{ A}$, $L = 0.1\text{ mH}$ | 551 | mJ |
| | | Control FET, $I_D = 60\text{ A}$, $L = 0.1\text{ mH}$ | 180 | |
| T_J | Operating junction temperature | -55 | 150 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature | -55 | 150 | $^\circ\text{C}$ |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Pulse duration $\leq 50\ \mu\text{s}$. Duty cycle $\leq 0.01\%$.

5.2 Recommended Operating Conditions

 $T_A = 25^\circ$ (unless otherwise noted)

| | | MIN | MAX | UNIT |
|----------|--|-----|------|------------------|
| V_{GS} | Gate drive voltage | 4.5 | 8 | V |
| V_{IN} | Input supply voltage | | 27 | V |
| f_{SW} | Switching frequency $C_{BST} = 0.1\ \mu\text{F}$ (min) | 200 | 1500 | kHz |
| | Operating current | | 40 | A |
| T_J | Operating temperature | | 125 | $^\circ\text{C}$ |

5.3 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|-----------------|---|-----|-----|-----|---------------------------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (min Cu) ⁽¹⁾⁽²⁾ | | | 102 | $^\circ\text{C}/\text{W}$ |
| | Junction-to-ambient thermal resistance (max Cu) ⁽¹⁾⁽²⁾ | | | 50 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JC}$ | Junction-to-case thermal resistance (top of package) ⁽²⁾ | | | 20 | $^\circ\text{C}/\text{W}$ |
| | Junction-to-case thermal resistance (P_{GND} pin) ⁽²⁾ | | | 2 | $^\circ\text{C}/\text{W}$ |

- (1) Device mounted on FR4 material with 1-in² (6.45-cm²) Cu.
- (2) $R_{\theta JC}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in \times 1.5-in (3.81-cm \times 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

5.4 Power Block Performance

 $T_A = 25^\circ$ (unless otherwise noted)

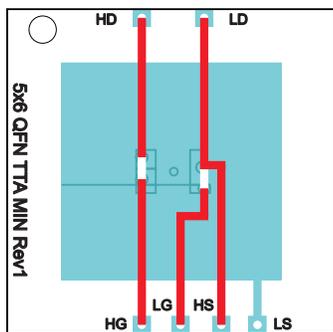
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|----------------------------|-----|-----|-----|---------------|
| P_{LOSS} | Power loss ⁽¹⁾ | | 3 | | W |
| I_{QVIN} | V_{IN} quiescent current | | 10 | | μA |

- (1) Measurement made with six 10- μF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high-current 5-V driver IC.

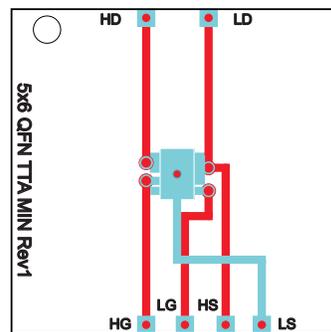
5.5 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | Q1 CONTROL FET | | | Q2 SYNC FET | | | UNIT | | |
|--------------------------------|----------------------------------|--|----------------|-----|-----|-------------|-----|-----|---------------|------|----------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| STATIC CHARACTERISTICS | | | | | | | | | | | |
| BV_{DSS} | Drain-to-source voltage | $V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$ | 30 | | | 30 | | | V | | |
| I_{DSS} | Drain-to-source leakage current | $V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ | | | | 1 | | | μA | | |
| I_{GSS} | Gate-to-source leakage current | $V_{DS} = 0\text{ V}, V_{GS} = +10 / -8$ | | | | 100 | | | nA | | |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$ | 1 | | | 2.1 | | | 0.75 | 1.4 | V |
| $Z_{DS(on)}^{(1)}$ | Effective AC on-impedance | $V_{IN} = 12\text{ V}, V_{GS} = 5\text{ V},$ $V_{OUT} = 1.3\text{ V}, I_{OUT} = 20\text{ A},$ $f_{SW} = 500\text{ kHz},$ $L_{OUT} = 0.3\ \mu\text{H}$ | 5 | | | 1.2 | | | m Ω | | |
| g_{fs} | Transconductance | $V_{DS} = 15\text{ V}, I_{DS} = 20\text{ A}$ | 97 | | | 157 | | | S | | |
| DYNAMIC CHARACTERISTICS | | | | | | | | | | | |
| C_{ISS} | Input capacitance | $V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V},$ $f = 1\text{ MHz}$ | 1360 | | | 1770 | | | 2950 | 3835 | pF |
| C_{OSS} | Output capacitance | | 565 | | | 735 | | | 1300 | 1690 | pF |
| C_{RSS} | Reverse transfer capacitance | | 19 | | | 25 | | | 50 | 65 | pF |
| R_G | Series gate resistance | | 1.3 | | | 3 | | | 0.8 | 2 | Ω |
| Q_g | Gate charge total (4.5 V) | | 8.4 | | | 10.9 | | | 20 | 26 | nC |
| Q_{gd} | Gate charge gate-to-drain | $V_{DS} = 15\text{ V},$ $I_{DS} = 20\text{ A}$ | 1.6 | | | 3.6 | | | | | nC |
| Q_{gs} | Gate charge gate-to-source | | 2.6 | | | 4.3 | | | | | nC |
| $Q_{g(th)}$ | Gate charge at V_{th} | | 1.6 | | | 2.3 | | | | | nC |
| Q_{OSS} | Output charge | $V_{DS} = 17\text{ V}, V_{GS} = 0\text{ V}$ | 9.7 | | | 28 | | | | | nC |
| $t_{d(on)}$ | Turnon delay time | | 7 | | | 8 | | | | | ns |
| t_r | Rise time | $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{DS} = 20\text{ A}, R_G = 2\ \Omega$ | 17 | | | 10 | | | | | ns |
| $t_{d(off)}$ | Turnoff delay time | | 13 | | | 33 | | | | | ns |
| t_f | Fall time | | 2.3 | | | 4.7 | | | | | ns |
| DIODE CHARACTERISTICS | | | | | | | | | | | |
| V_{SD} | Diode forward voltage | $I_{DS} = 20\text{ A}, V_{GS} = 0\text{ V}$ | 0.85 | | | 1 | | | 0.77 | 1 | V |
| Q_{rr} | Reverse recovery charge | $V_{dd} = 17\text{ V}, I_F = 20\text{ A},$ $di/dt = 300\text{ A}/\mu\text{s}$ | 12.5 | | | 32 | | | | | nC |
| t_{rr} | Reverse recovery time | | 22 | | | 28 | | | | | ns |

 (1) Equivalent based on application testing. See [Equivalent System Performance](#) section for details.


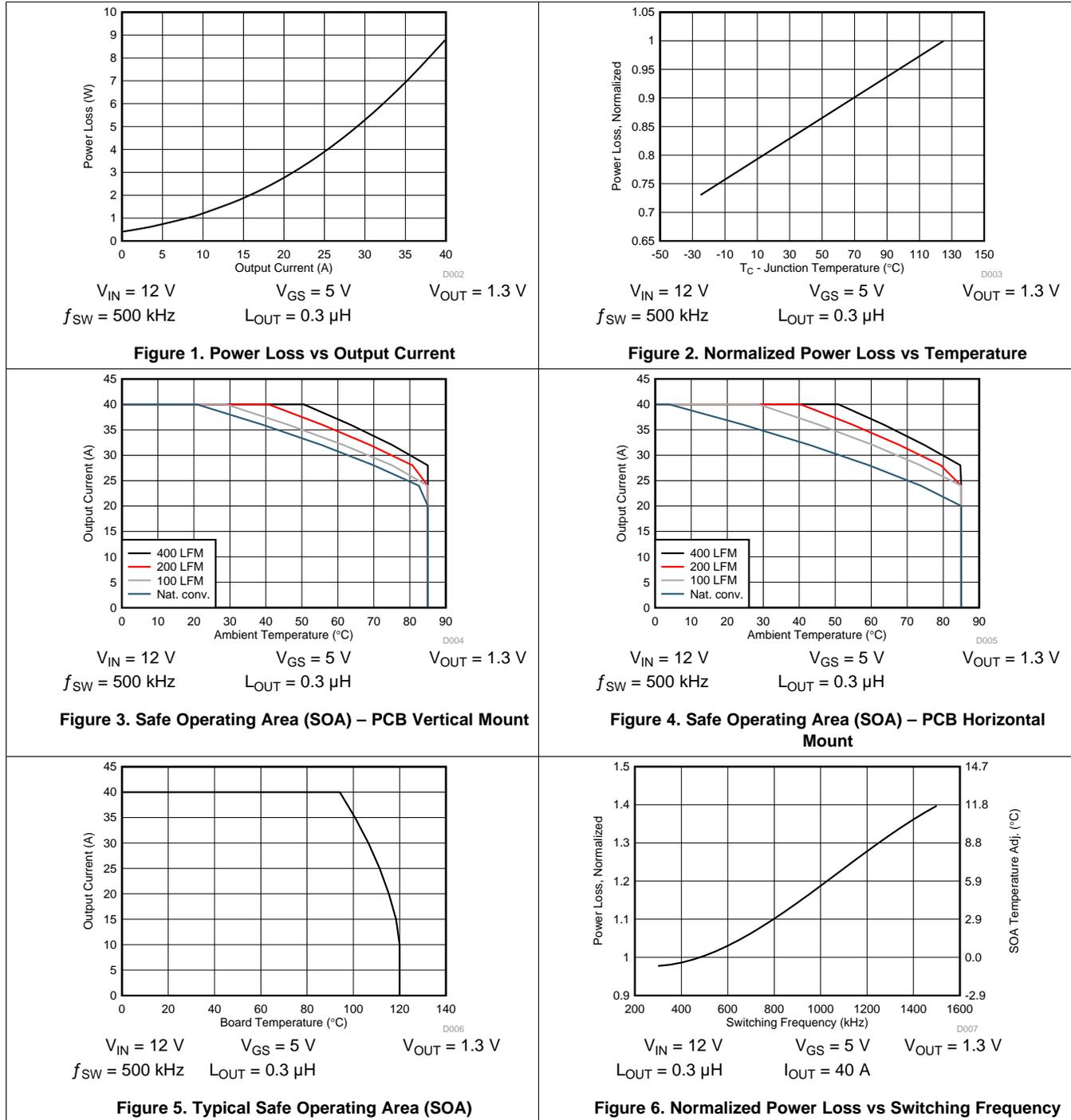
Max $R_{\theta JA} = 50^\circ\text{C}/\text{W}$
when mounted on 1 in²
(6.45 cm²) of
2-oz (0.071-mm) thick
Cu.



Max $R_{\theta JA} = 102^\circ\text{C}/\text{W}$
when mounted on
minimum pad area of
2-oz (0.071-mm) thick
Cu.

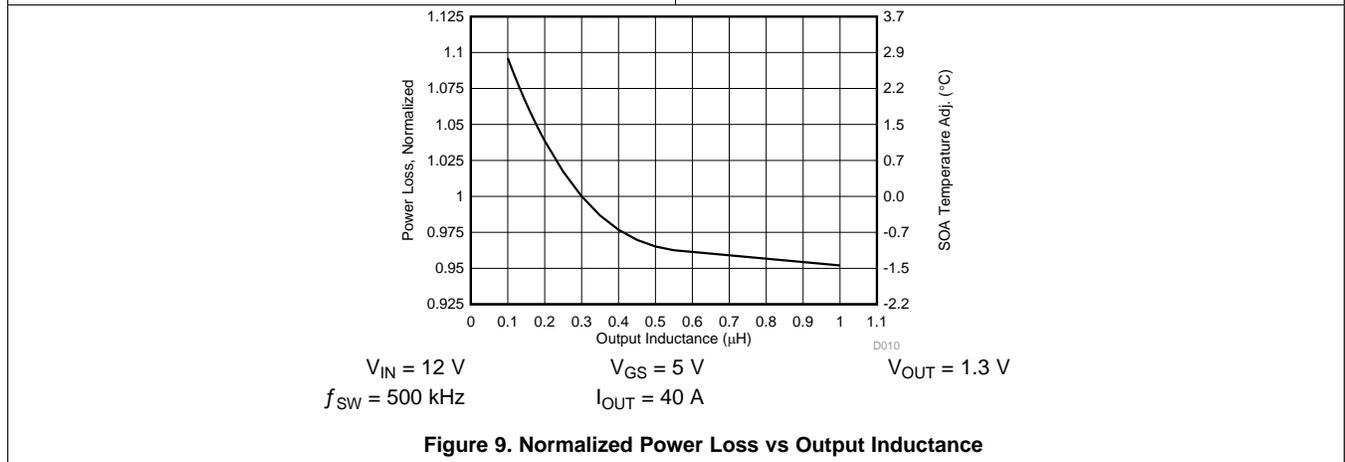
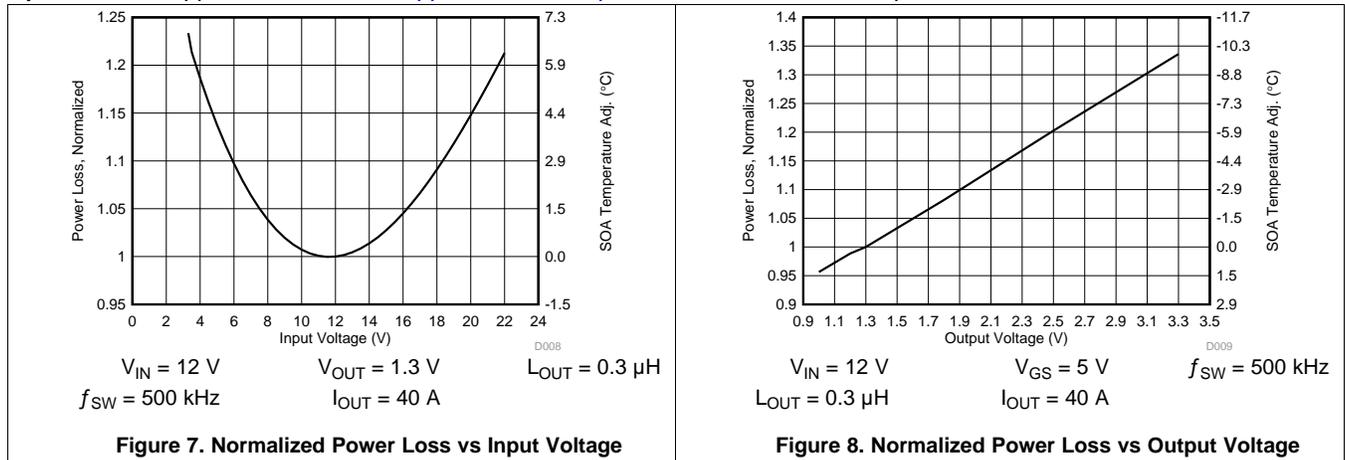
5.6 Typical Power Block Device Characteristics

$T_J = 125^\circ\text{C}$, unless stated otherwise. The typical power block system characteristic curves [Figure 3](#), [Figure 4](#), and [Figure 5](#) are based on measurements made on a PCB design with dimensions of 4 in (W) \times 3.5 in (L) \times 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See [Application and Implementation](#) for detailed explanation.



Typical Power Block Device Characteristics (continued)

$T_J = 125^\circ\text{C}$, unless stated otherwise. The typical power block system characteristic curves [Figure 3](#), [Figure 4](#), and [Figure 5](#) are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See [Application and Implementation](#) for detailed explanation.



5.7 Typical Power Block MOSFET Characteristics

$T_A = 25^\circ\text{C}$, unless stated otherwise.

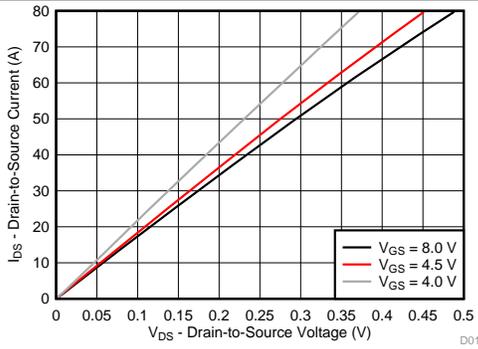


Figure 10. Control MOSFET Saturation

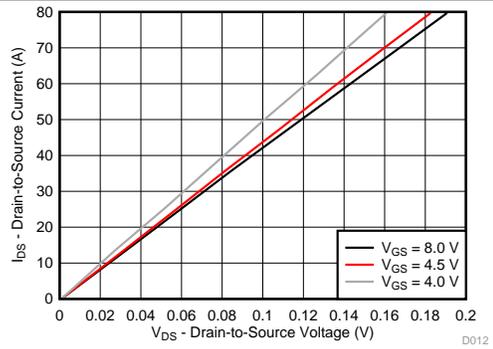


Figure 11. Sync MOSFET Saturation

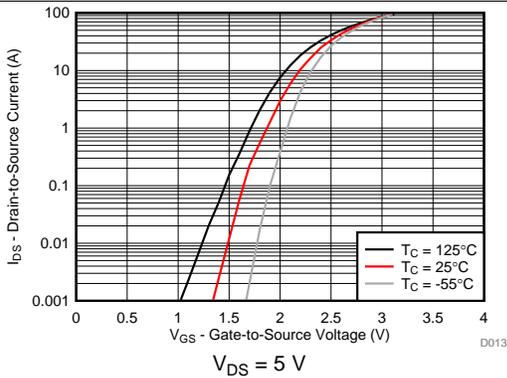


Figure 12. Control MOSFET Transfer

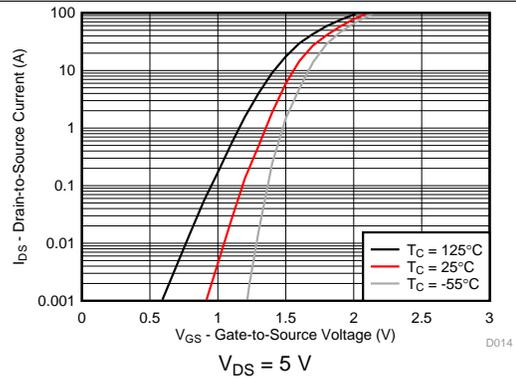


Figure 13. Sync MOSFET Transfer

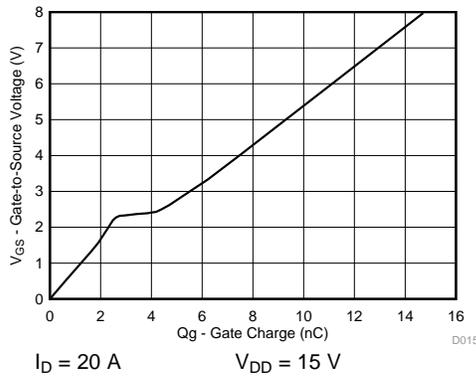


Figure 14. Control MOSFET Gate Charge

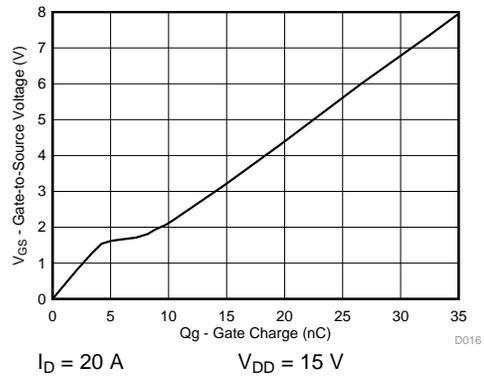


Figure 15. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

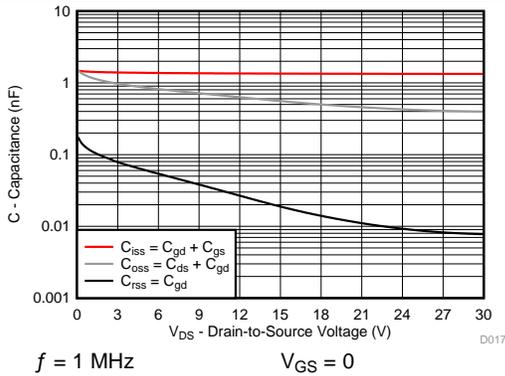


Figure 16. Control MOSFET Capacitance

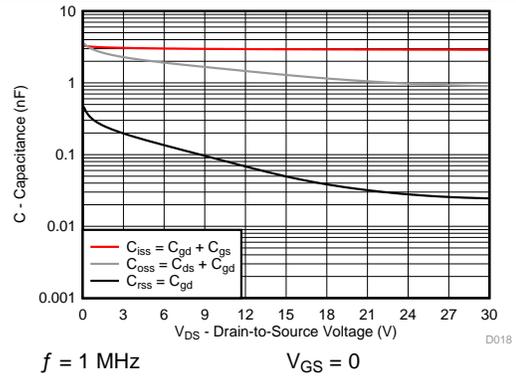


Figure 17. Sync MOSFET Capacitance

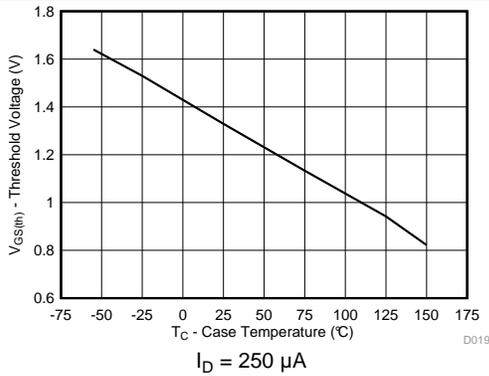


Figure 18. Control MOSFET V_{GS(th)}

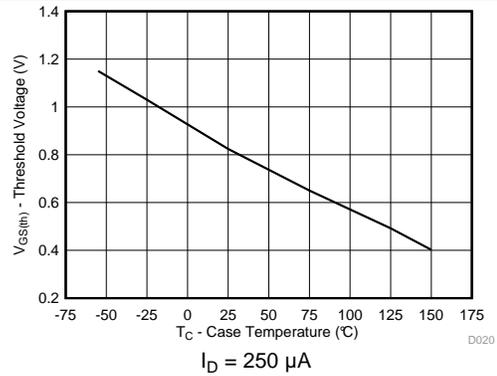


Figure 19. Sync MOSFET V_{GS(th)}

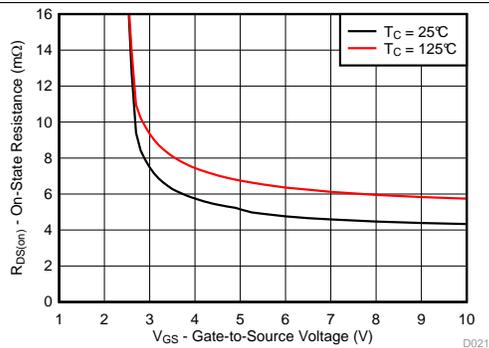


Figure 20. Control MOSFET R_{DS(on)} vs V_{GS}

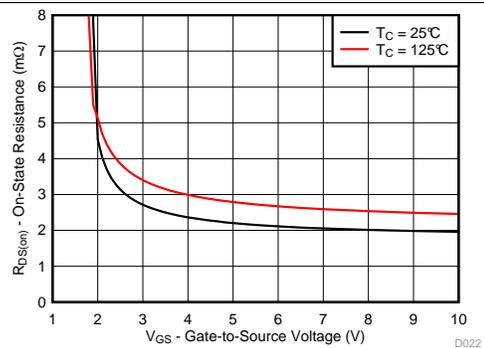


Figure 21. Sync MOSFET R_{DS(on)} vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$, unless stated otherwise.

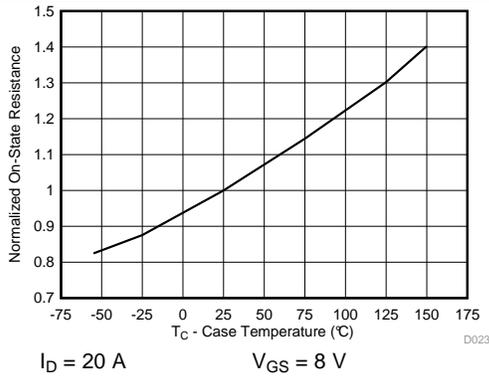


Figure 22. Control MOSFET Normalized $R_{DS(on)}$

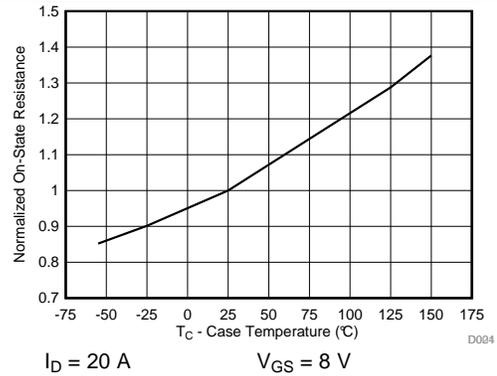


Figure 23. Sync MOSFET Normalized $R_{DS(on)}$

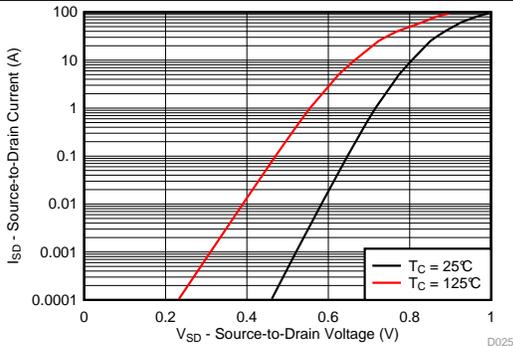


Figure 24. Control MOSFET Body Diode

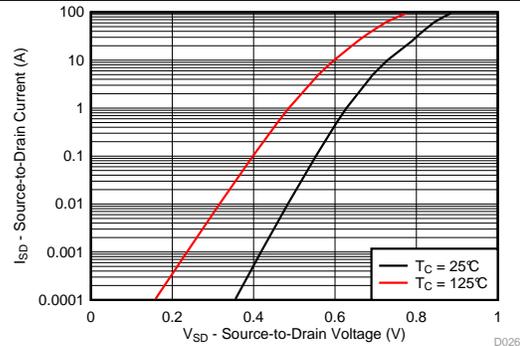


Figure 25. Sync MOSFET Body Diode

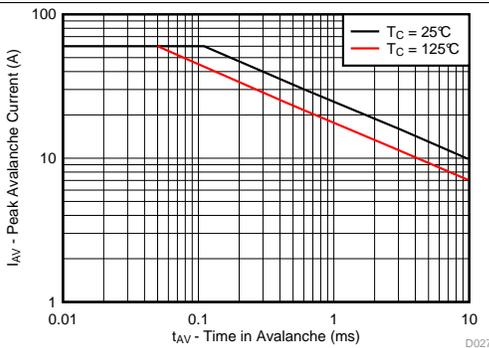


Figure 26. Control MOSFET Unclamped Inductive Switching

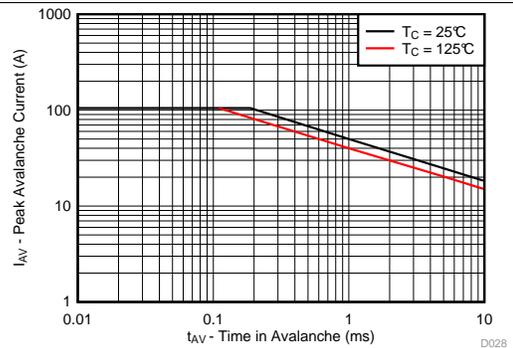


Figure 27. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87350Q5D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.1 Equivalent System Performance

Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see [Figure 28](#)). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

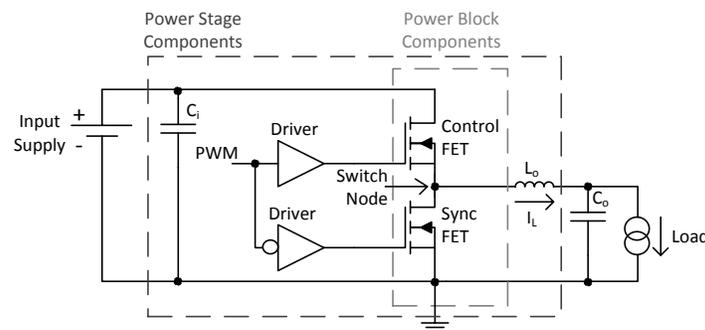


Figure 28. Equivalent System Schematic

The CSD87350Q5D is part of TI's power block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD} , Q_{GS} , and Q_{RR} . Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see [Figure 29](#)). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in [Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters](#) (SLPA009).

Application Information (continued)

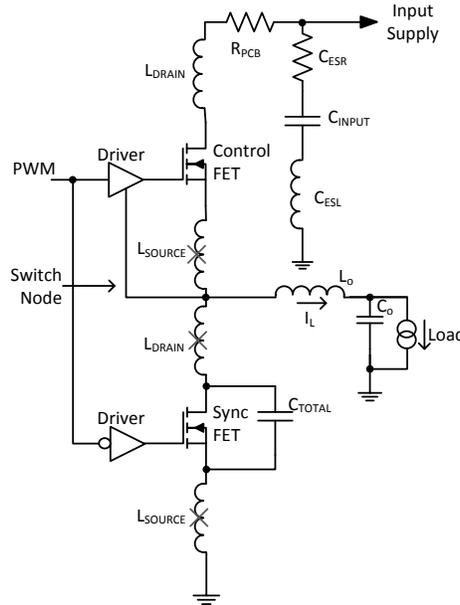
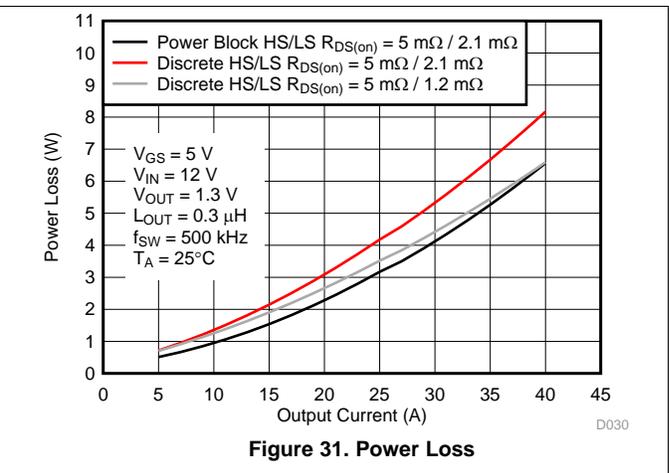
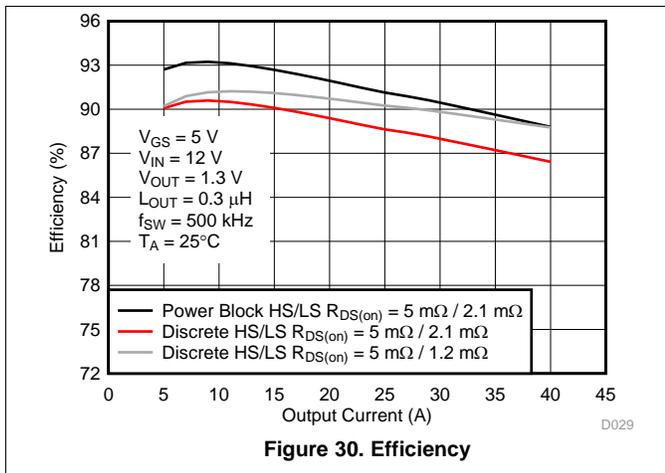


Figure 29. Elimination of Parasitic Inductances

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figure 30 and Figure 31 compare the efficiency and power loss performance of the CSD87350Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87350Q5D clearly highlights the importance of considering the Effective AC On-Impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.



Application Information (continued)

Table 1 compares the traditional DC measured $R_{DS(ON)}$ of CSD87350Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87350Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid- to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Table 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

| PARAMETER | HS | | LS | | UNIT |
|--|-----|-----|-----|-----|------------|
| | TYP | MAX | TYP | MAX | |
| Effective AC on-impedance $Z_{DS(ON)}$ ($V_{GS} = 5\text{ V}$) | 5 | – | 1.2 | – | m Ω |
| DC measured $R_{DS(ON)}$ ($V_{GS} = 4.5\text{ V}$) | 5 | 6.8 | 2.1 | 2.8 | |

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. **Figure 1** plots the power loss of the CSD87350Q5D as a function of load current. This curve is measured by configuring and running the CSD87350Q5D as it would be in the final application (see **Figure 32**). The measured power loss is the CSD87350Q5D loss and consists of both input conversion loss and gate drive loss. **Equation 1** is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) = \text{power loss} \quad (1)$$

The power loss curve in **Figure 1** is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Area (SOA) Curves

The SOA curves in the CSD87350Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. **Figure 3** to **Figure 5** outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) \times 3.5 in (L) \times 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

6.1.4 Normalized Curves

The normalized curves in the CSD87350Q5D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

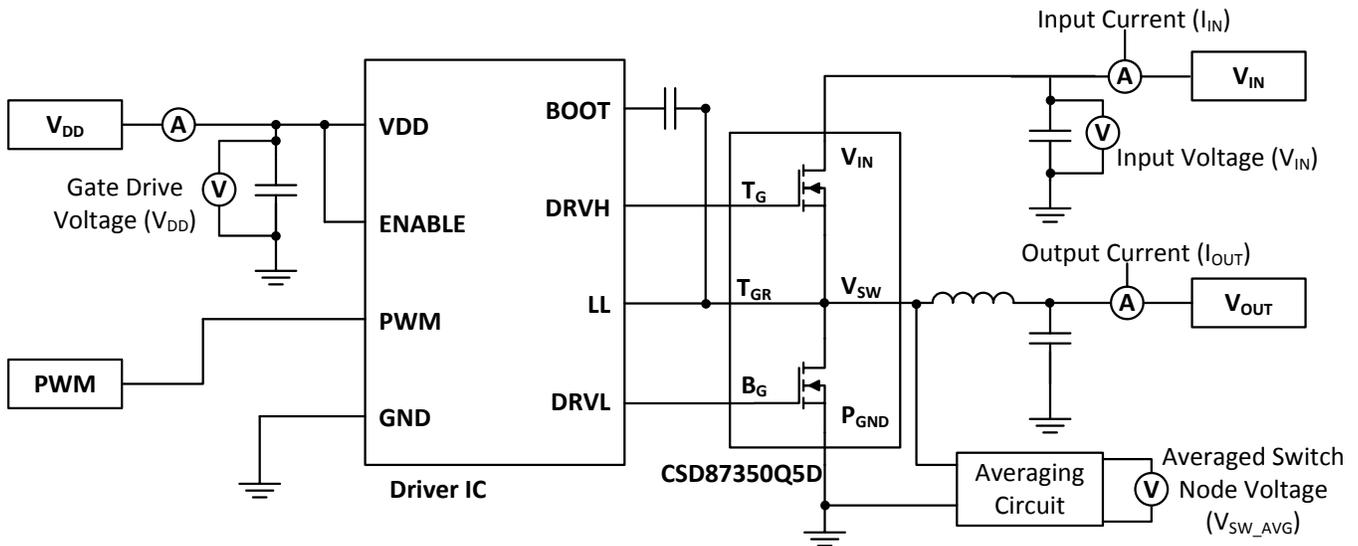


Figure 32.

6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see [Operating Conditions](#)). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.2 Operating Conditions

- Output current = 25 A
- Input voltage = 7 V
- Output voltage = 1 V
- Switching frequency = 800 kHz
- Inductor = 0.2 μ H

6.2.2.1 Calculating Power Loss

- Power Loss at 25 A = 3.5 W ([Figure 1](#))
- Normalized Power Loss for input voltage \approx 1.07 ([Figure 7](#))
- Normalized Power Loss for output voltage \approx 0.95 ([Figure 8](#))
- Normalized Power Loss for switching frequency \approx 1.11 ([Figure 6](#))
- Normalized Power Loss for output inductor \approx 1.07 ([Figure 9](#))
- **Final calculated Power Loss = 3.5 W \times 1.07 \times 0.95 \times 1.11 \times 1.07 \approx 4.23 W**

6.2.2.2 Calculating SOA Adjustments

- SOA adjustment for input voltage \approx 2°C ([Figure 7](#))
- SOA adjustment for output voltage \approx -1.3°C ([Figure 8](#))
- SOA adjustment for switching frequency \approx 2.8°C ([Figure 6](#))
- SOA adjustment for output inductor \approx 1.6°C ([Figure 9](#))
- **Final calculated SOA adjustment = 2 + (-1.3) + 2.8 + 1.6 \approx 5.1°C**

In the previous design example, the estimated power loss of the CSD87350Q5D would increase to 4.23 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 5.1°C. [Figure 33](#) graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.

Typical Application (continued)

2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 5.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

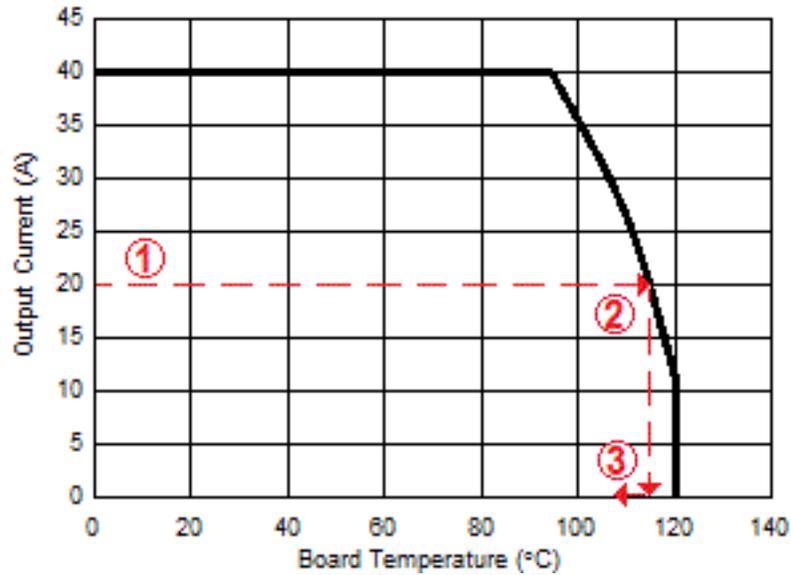


Figure 33. Power Block SOA

7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. The following sections provide a brief description on how to address each parameter.

7.1.1 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10kV/μs. Take special care with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see [Figure 34](#)). The example in [Figure 34](#) uses 6 × 10-μF ceramic capacitors (TDK Part C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins. T_G and B_G should connect to the outputs of the driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.
- In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Refer to [Snubber Circuits: Theory, Design and Application](#) (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND see [Figure 34](#).⁽¹⁾

7.1.2 Thermal Considerations

The power block has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in [Figure 34](#) uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Layout Example

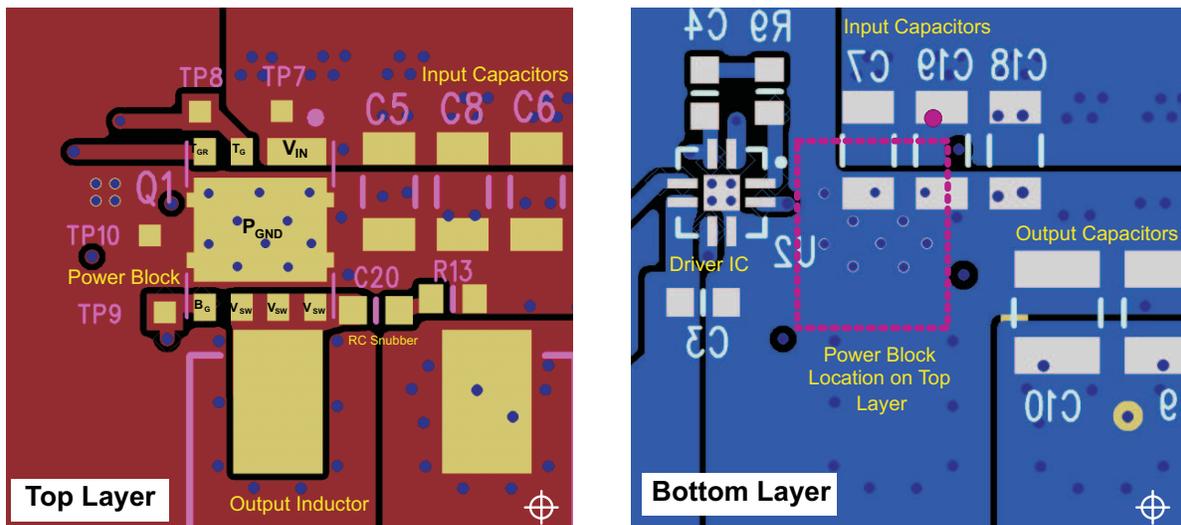


Figure 34. Recommended PCB Layout (Top View)

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- [Reducing Ringing Through PCB Layout Techniques](#)
- [Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters](#)
- [Snubber Circuits: Theory , Design and Application](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.4 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.6 Glossary

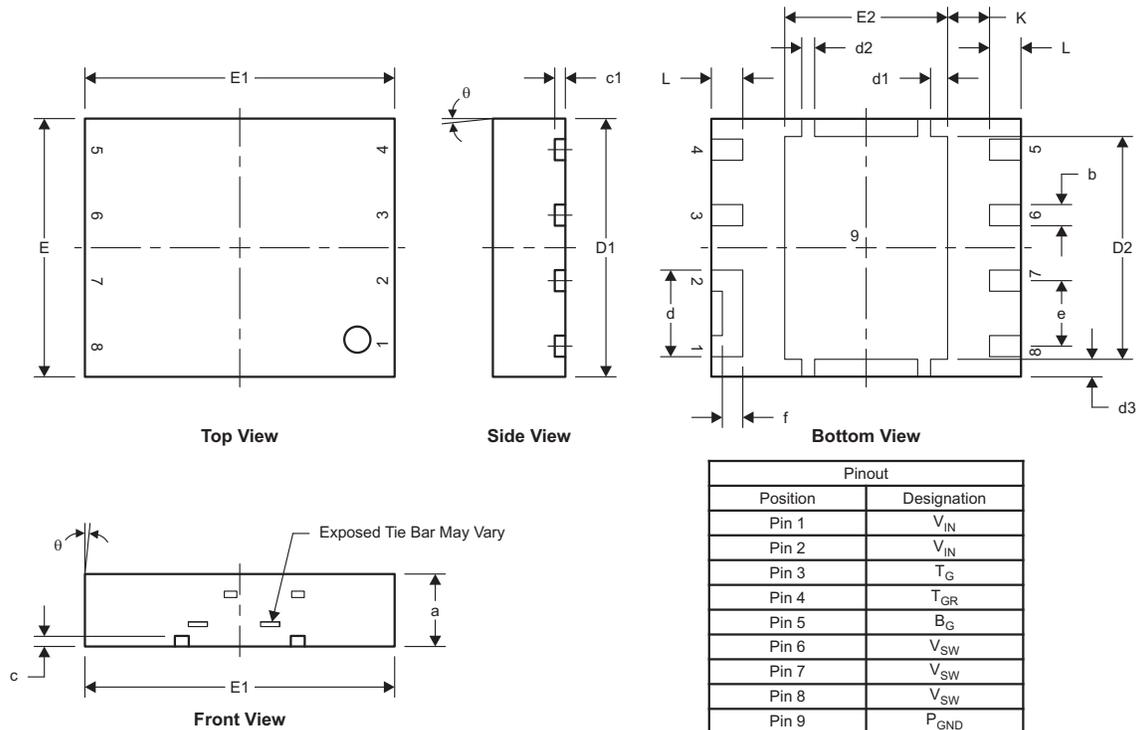
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Q5D Package Dimensions

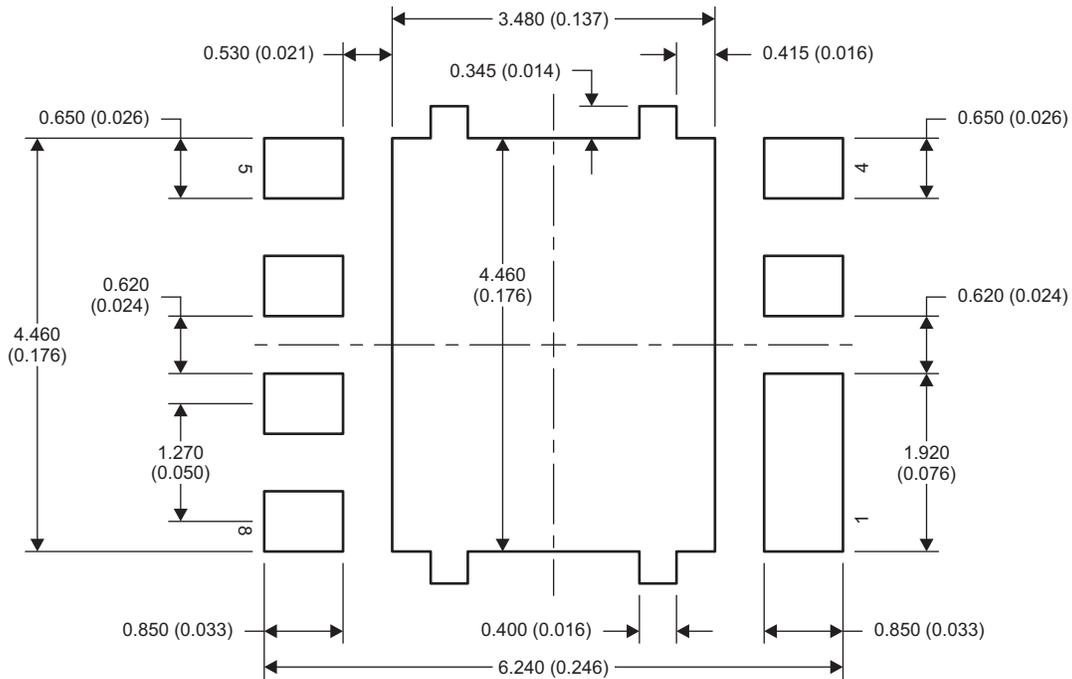


| Pinout | |
|----------|------------------|
| Position | Designation |
| Pin 1 | V _{IN} |
| Pin 2 | V _{IN} |
| Pin 3 | T _G |
| Pin 4 | T _{GR} |
| Pin 5 | B _G |
| Pin 6 | V _{SW} |
| Pin 7 | V _{SW} |
| Pin 8 | V _{SW} |
| Pin 9 | P _{GND} |

M0187-01

| DIM | MILLIMETERS | | INCHES | |
|-------|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| a | 1.40 | 1.5 | 0.055 | 0.059 |
| b | 0.360 | 0.460 | 0.014 | 0.018 |
| c | 0.150 | 0.250 | 0.006 | 0.010 |
| c1 | 0.150 | 0.250 | 0.006 | 0.010 |
| d | 1.630 | 1.730 | 0.064 | 0.068 |
| d1 | 0.280 | 0.380 | 0.011 | 0.015 |
| d2 | 0.200 | 0.300 | 0.008 | 0.012 |
| d3 | 0.291 | 0.391 | 0.012 | 0.015 |
| D1 | 4.900 | 5.100 | 0.193 | 0.201 |
| D2 | 4.269 | 4.369 | 0.168 | 0.172 |
| E | 4.900 | 5.100 | 0.193 | 0.201 |
| E1 | 5.900 | 6.100 | 0.232 | 0.240 |
| E2 | 3.106 | 3.206 | 0.122 | 0.126 |
| e | 1.27 TYP | | 0.050 | |
| f | 0.396 | 0.496 | 0.016 | 0.020 |
| L | 0.510 | 0.710 | 0.020 | 0.028 |
| theta | 0.00 | | — | |
| K | 0.812 | | 0.032 | |

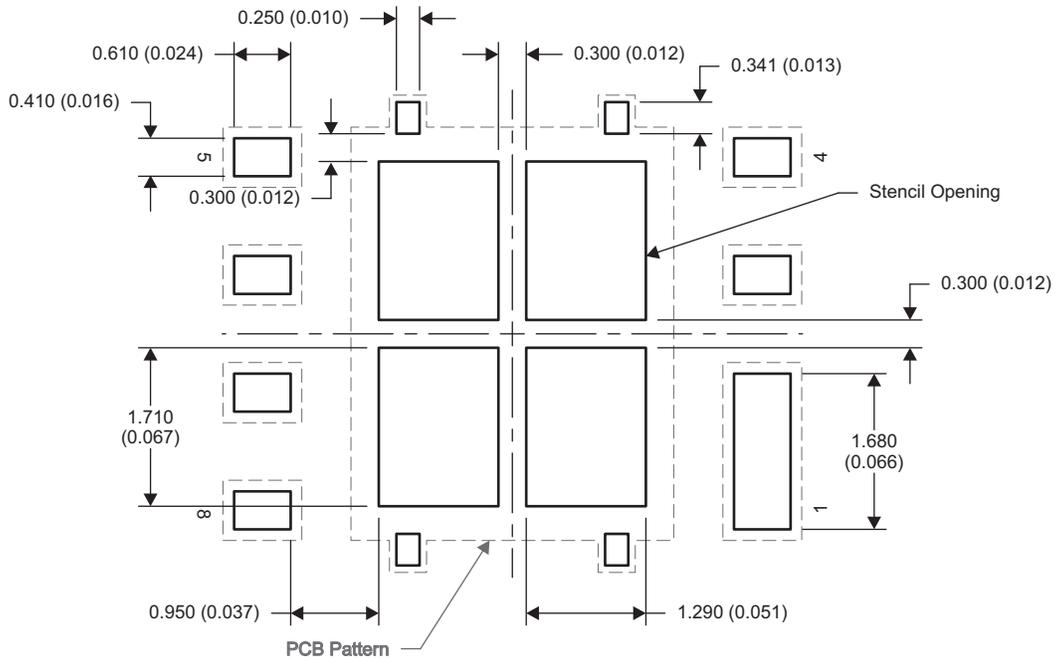
9.2 Land Pattern Recommendation



M0188-01

NOTE: Dimensions are in mm (in).

9.3 Stencil Recommendation

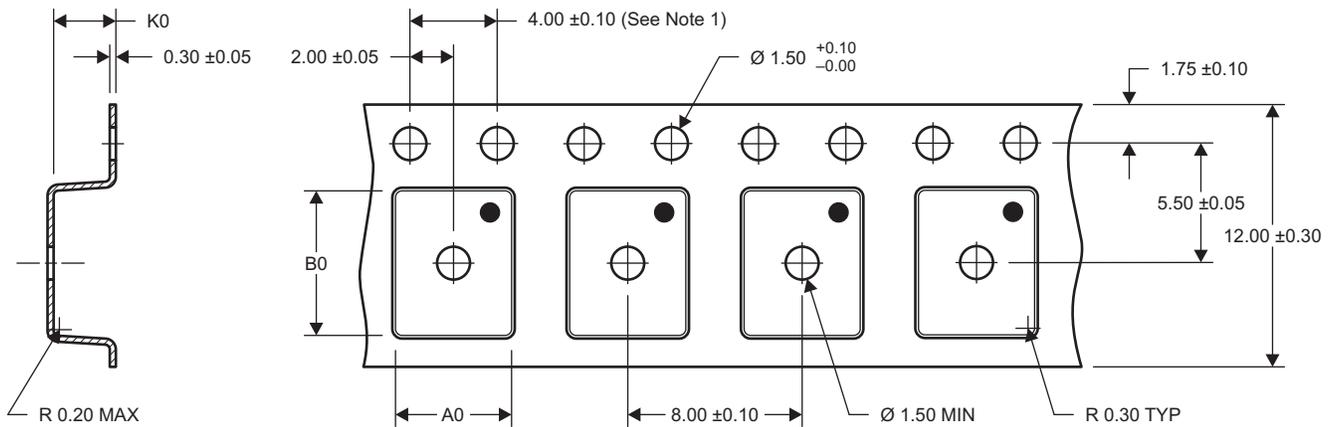


M0208-01

NOTE: Dimensions are in mm (in).

For recommended circuit layout for PCB designs, see [Reducing Ringing Through PCB Layout Techniques \(SLPA005\)](#).

9.4 Q5D Tape and Reel Information



$A0 = 5.30 \pm 0.10$
 $B0 = 6.50 \pm 0.10$
 $K0 = 1.90 \pm 0.10$

M0191-01

- NOTES:
- 10-sprocket hole-pitch cumulative tolerance ± 0.2 .
 - Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
 - Material: black static-dissipative polystyrene.
 - All dimensions are in mm, unless otherwise specified.
 - Thickness: 0.3 ± 0.05 mm.
 - MSL1 260°C (IR and convection) PbF-reflow compatible.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|---------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CSD87350Q5D | Active | Production | LSON-CLIP (DQY) 8 | 2500 LARGE T&R | ROHS Exempt | NIPDAU SN | Level-1-260C-UNLIM | -55 to 150 | 87350D |
| CSD87350Q5D.B | Active | Production | LSON-CLIP (DQY) 8 | 2500 LARGE T&R | ROHS Exempt | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | 87350D |
| CSD87350Q5DG4 | Active | Production | LSON-CLIP (DQY) 8 | 2500 LARGE T&R | ROHS Exempt | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | 87350D |
| CSD87350Q5DG4.B | Active | Production | LSON-CLIP (DQY) 8 | 2500 LARGE T&R | ROHS Exempt | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | 87350D |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

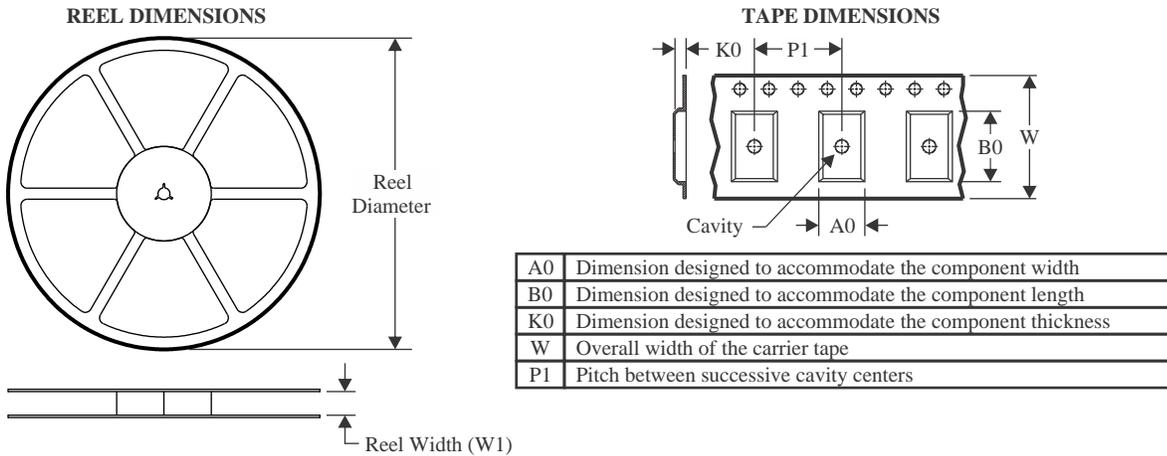
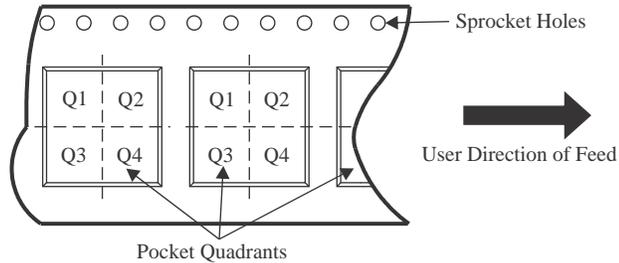
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

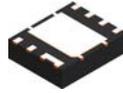
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CSD87350Q5D | LSON-CLIP | DQY | 8 | 2500 | 330.0 | 12.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q2 |
| CSD87350Q5DG4 | LSON-CLIP | DQY | 8 | 2500 | 330.0 | 12.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CSD87350Q5D | LSON-CLIP | DQY | 8 | 2500 | 346.0 | 346.0 | 33.0 |
| CSD87350Q5DG4 | LSON-CLIP | DQY | 8 | 2500 | 346.0 | 346.0 | 33.0 |

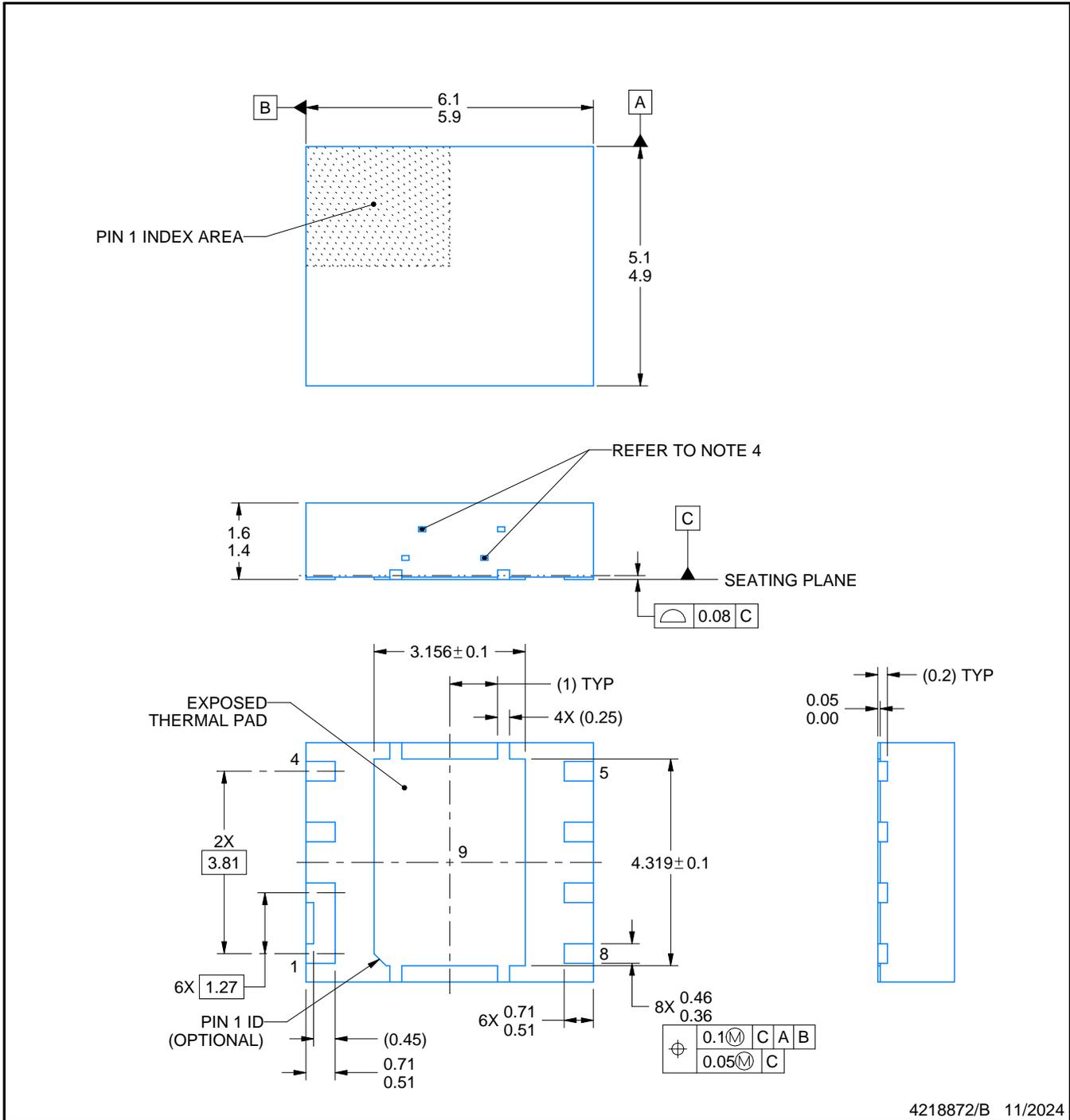
DQY0008A



PACKAGE OUTLINE

LSON-CLIP - 1.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218872/B 11/2024

NOTES:

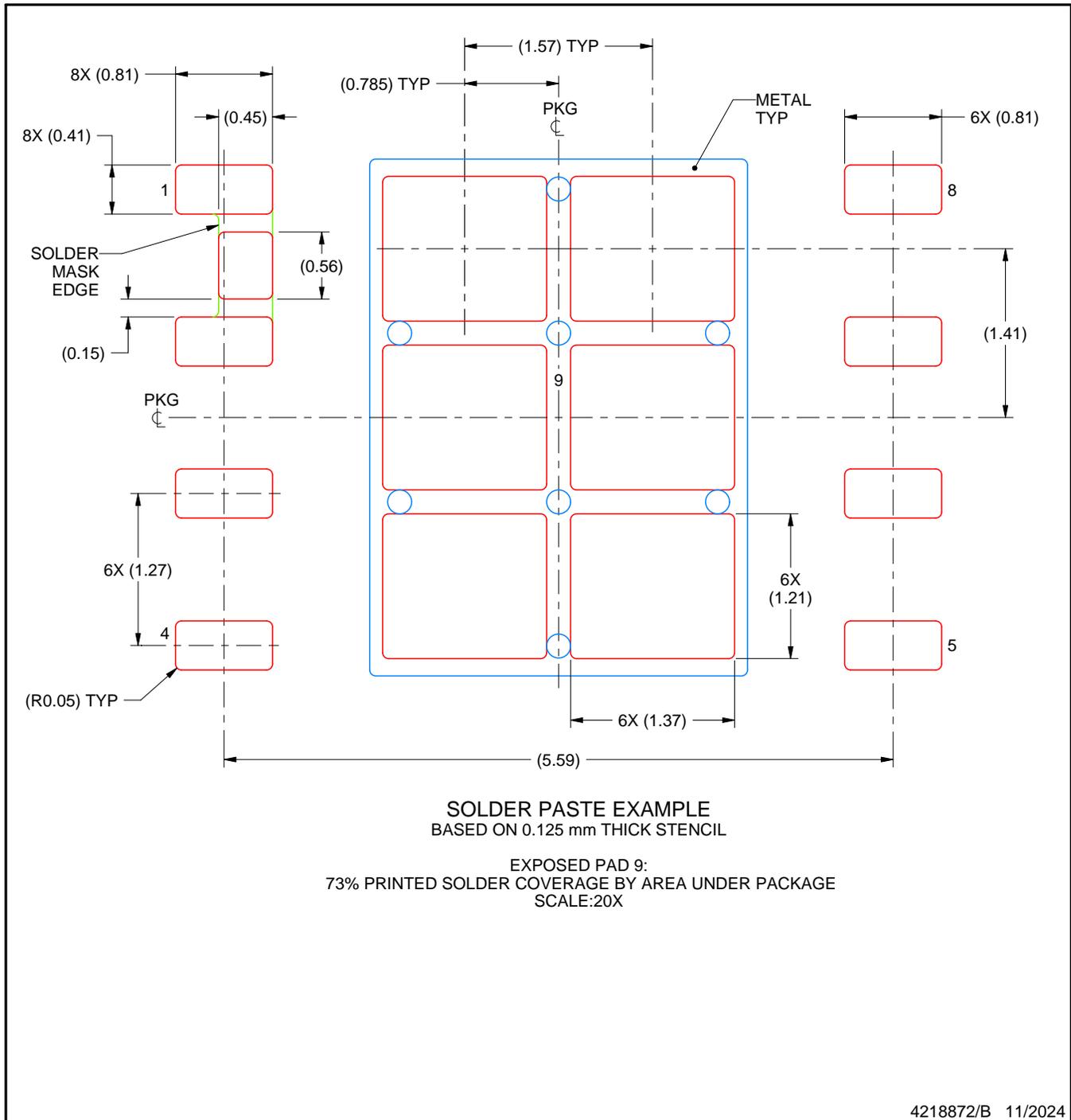
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed metals on side wall may vary or not visible

EXAMPLE STENCIL DESIGN

DQY0008A

LSON-CLIP - 1.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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