

CSD25485F5 –20-V P-Channel FemtoFET™ MOSFET

1 Features

- Low-on resistance
- Low Q_g and Q_{gd}
- Ultra-small footprint
 - 1.53 mm × 0.77 mm
 - 0.50-mm pad pitch
- Low profile
 - 0.36-mm height
- Integrated ESD protection diode
 - Rated > 4-kV HBM
 - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for industrial load switch applications
- Optimized for general purpose switching applications

3 Description

This 29.7-mΩ, –20-V, P-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a significant reduction in footprint size.

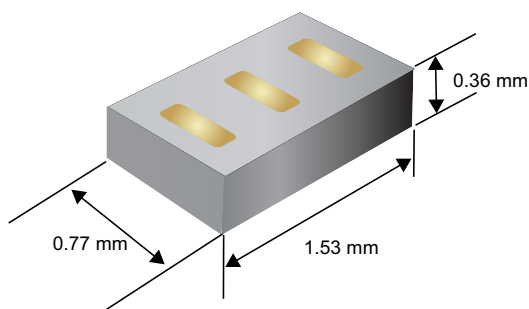


Figure 3-1. Typical Part Dimensions

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
Q_g	Gate Charge Total (–4.5 V)	2.7	nC
Q_{gd}	Gate Charge Gate-to-Drain	0.56	nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = -1.8\text{ V}$	89
		$V_{GS} = -2.5\text{ V}$	51
		$V_{GS} = -4.5\text{ V}$	35
		$V_{GS} = -8\text{ V}$	29.7
$V_{GS(th)}$	Threshold Voltage	–0.95	V

Device Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25485F5	3000	7-Inch Reel	Femto 1.53-mm × 0.77-mm SMD Leadless	Tape and Reel
CSD25485F5T	250			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current ⁽¹⁾	–3.2	A
	Continuous Drain Current ⁽²⁾	–5.3	
I_{DM}	Pulsed Drain Current ^{(1) (3)}	–31	A
P_D	Power Dissipation ⁽¹⁾	0.5	W
	Power Dissipation ⁽²⁾	1.4	
$V_{(ESD)}$	Human-Body Model (HBM)	4000	V
	Charged-Device Model (CDM)	2000	
T_J , T_{stg}	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

- (1) Min Cu, typical $R_{\theta JA} = 245^\circ\text{C/W}$.
 (2) Max Cu, typical $R_{\theta JA} = 90^\circ\text{C/W}$.
 (3) Pulse duration $\leq 100\text{ }\mu\text{s}$, duty cycle $\leq 1\%$.

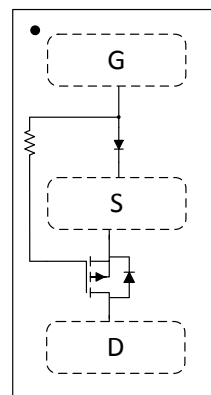


Figure 3-2. Top View



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4 Revision History

Changes from Revision A (January 2017) to Revision B (February 2022)	Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	7
• Added FemtoFET Surface Mount Guide note.....	8

Changes from Revision * (August 2016) to Revision A (January 2017)	Page
• Changed Min Cu R _{θJA} from 90°C/W : to 245°C/W in Figure 5-11	3
• Added Table 7-1 in the <i>Mechanical Dimensions</i> section.....	7

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _{DS} = −250 μA	−20			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = −16 V	−100			nA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = −12 V	−25			nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _{DS} = −250 μA	−0.7	−0.95	−1.3	V
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = −1.8 V, I _{DS} = −0.1 A	89		250	mΩ
		V _{GS} = −2.5 V, I _{DS} = −0.9 A	51		70	
		V _{GS} = −4.5 V, I _{DS} = −0.9 A	35		42	
		V _{GS} = −8 V, I _{DS} = −0.9 A	29.7		35	
g _{fs}	Transconductance	V _{DS} = −2 V, I _{DS} = −0.9 A	7			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = −10 V, f = 1 MHz	410		533	pF
C _{oss}	Output capacitance		212		276	pF
C _{rss}	Reverse transfer capacitance		17		23	pF
R _G	Series gate resistance		20			Ω
Q _g	Gate charge total (−4.5 V)	V _{DS} = −10 V, I _{DS} = −0.9 A	2.7		3.5	nC
Q _{gd}	Gate charge gate-to-drain		0.56			nC
Q _{gs}	Gate charge gate-to-source		0.67			nC
Q _{g(th)}	Gate charge at V _{th}		0.40			nC
Q _{oss}	Output charge	V _{DS} = −10 V, V _{GS} = 0 V	4.4			nC
t _{d(on)}	Turnon delay time	V _{DS} = −10 V, V _{GS} = −4.5 V, I _{DS} = −0.9 A, R _G = 2 Ω	14			ns
t _r	Rise time		6			ns
t _{d(off)}	Turnoff delay time		27			ns
t _f	Fall time		14			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = −0.9 A, V _{GS} = 0 V	−0.75		−1	V

5.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾		90		$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance ⁽²⁾		245		

- (1) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

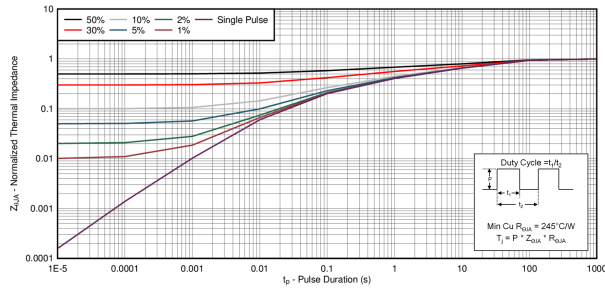


Figure 5-1. Transient Thermal Impedance

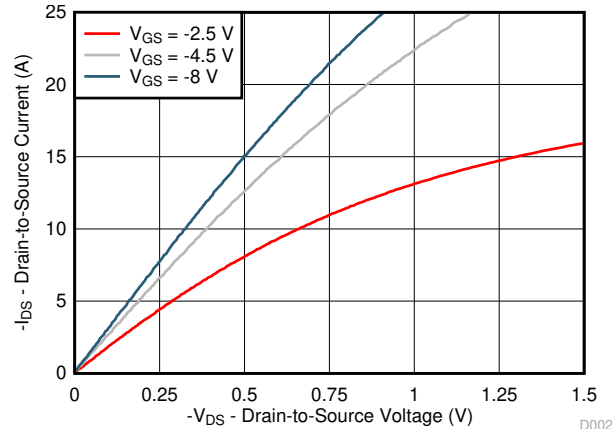


Figure 5-2. Saturation Characteristics

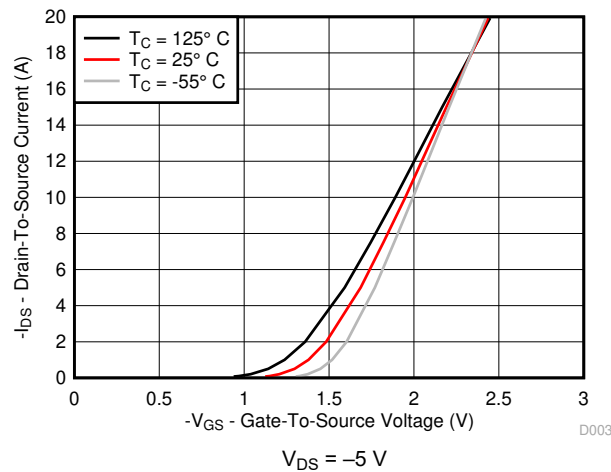


Figure 5-3. Transfer Characteristics

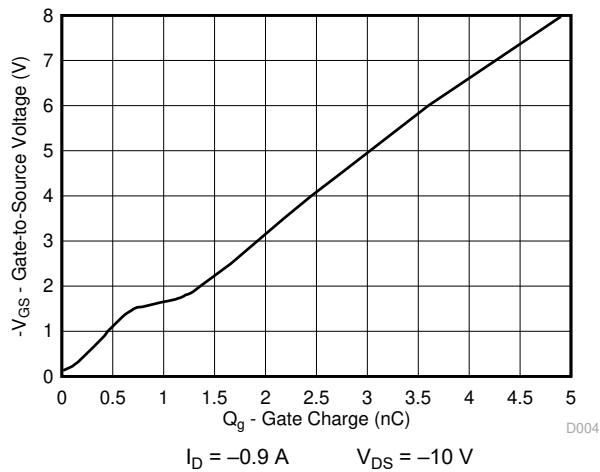


Figure 5-4. Gate Charge

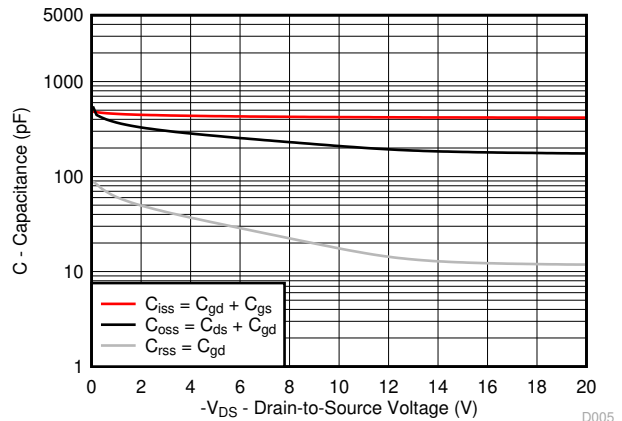


Figure 5-5. Capacitance

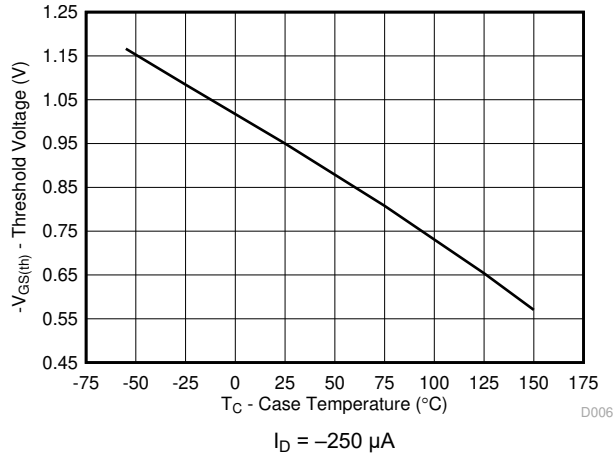


Figure 5-6. Threshold Voltage vs Temperature

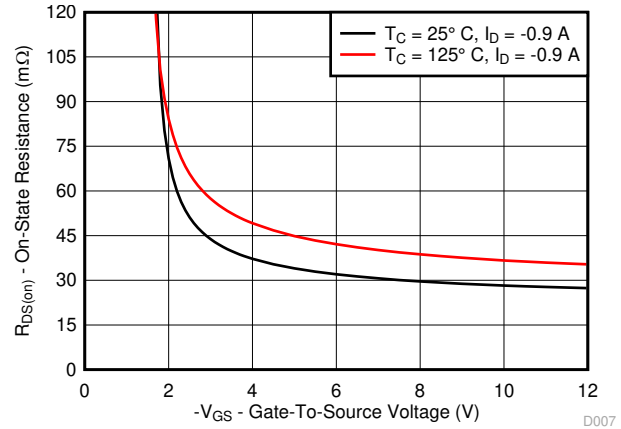


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

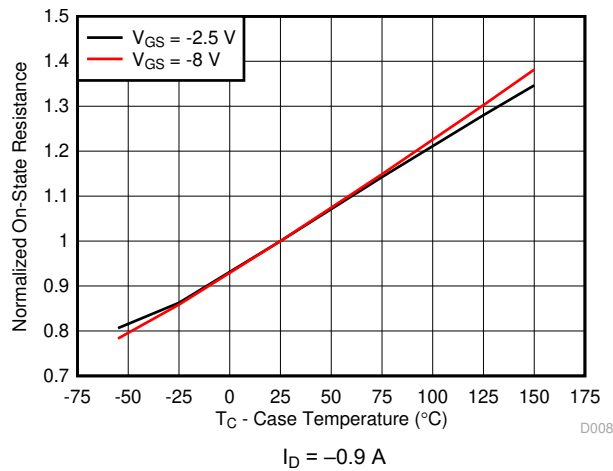


Figure 5-8. Normalized On-State Resistance vs Temperature

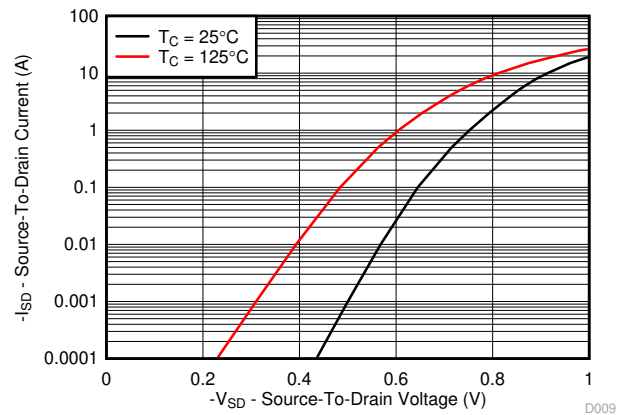


Figure 5-9. Typical Diode Forward Voltage

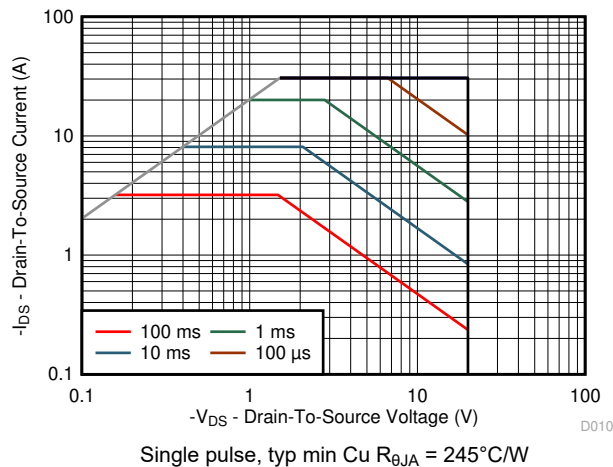


Figure 5-10. Maximum Safe Operating Area (SOA)

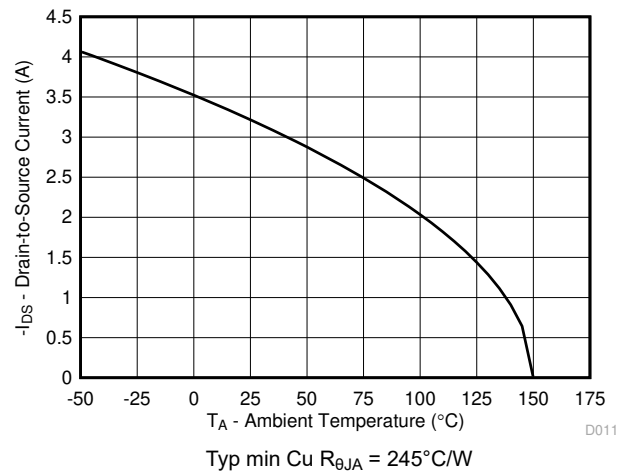


Figure 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

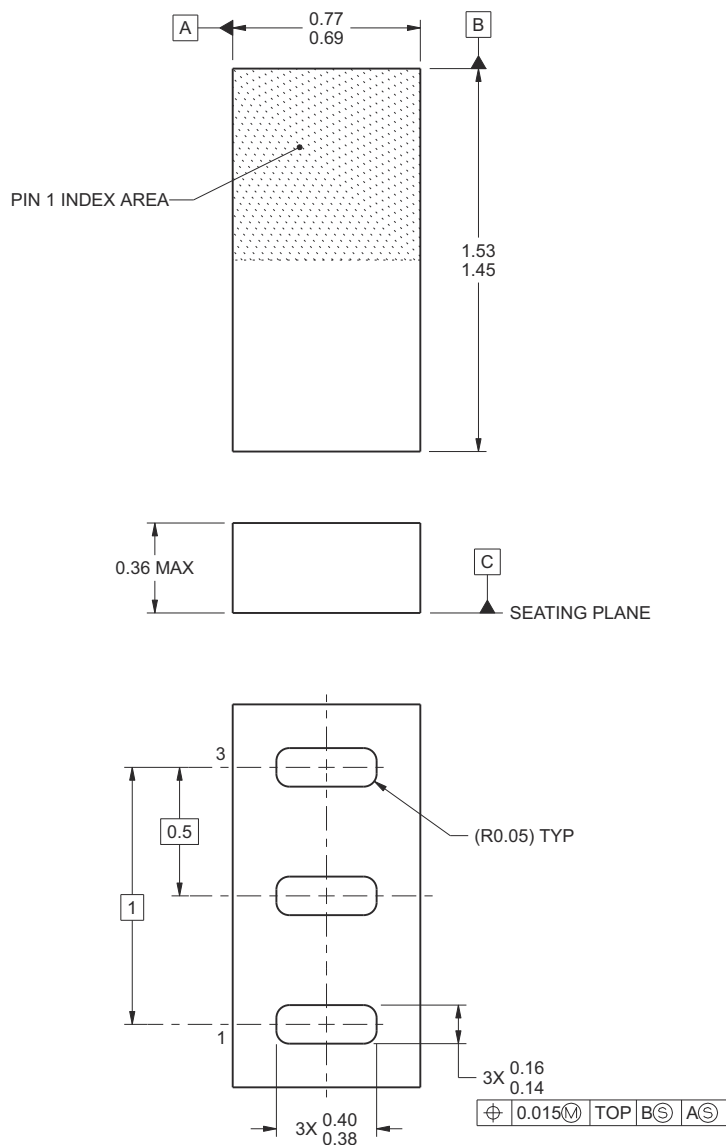
FemtoFET™ is a trademark of Texas Instruments.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



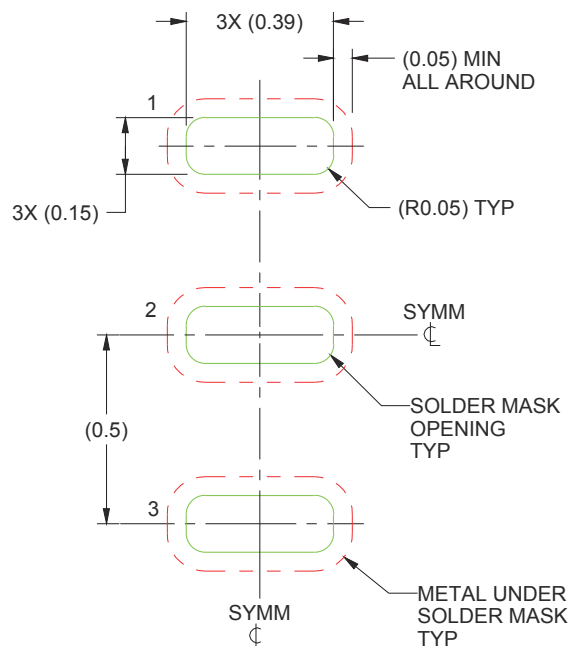
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- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

Table 7-1. Pin Configuration

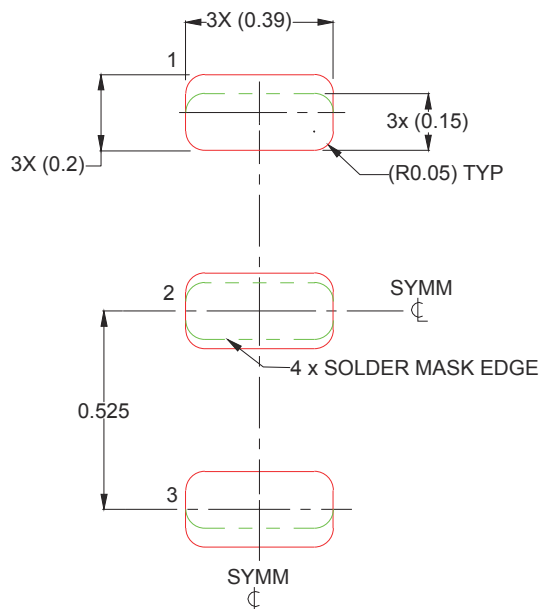
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
 B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25485F5	Active	Production	PICOSTAR (YJK) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	3H
CSD25485F5.B	Active	Production	PICOSTAR (YJK) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	3H
CSD25485F5T	Active	Production	PICOSTAR (YJK) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	3H
CSD25485F5T.B	Active	Production	PICOSTAR (YJK) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	3H

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

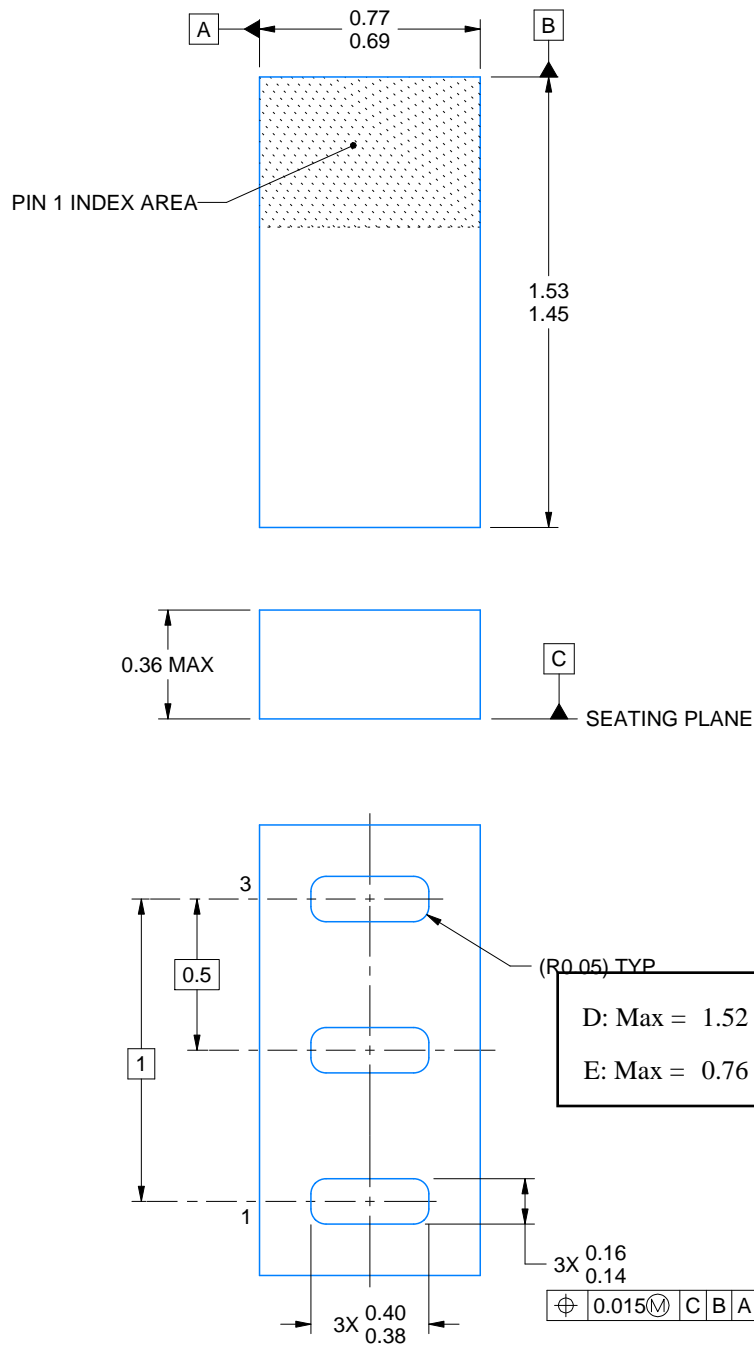
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25485F5	PICOSTAR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD25485F5T	PICOSTAR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25485F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD25485F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0

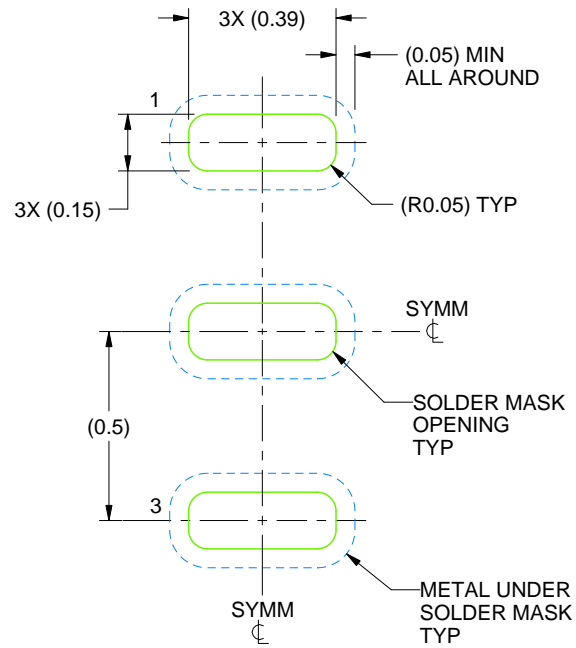


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NOTES:

PicoStar is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

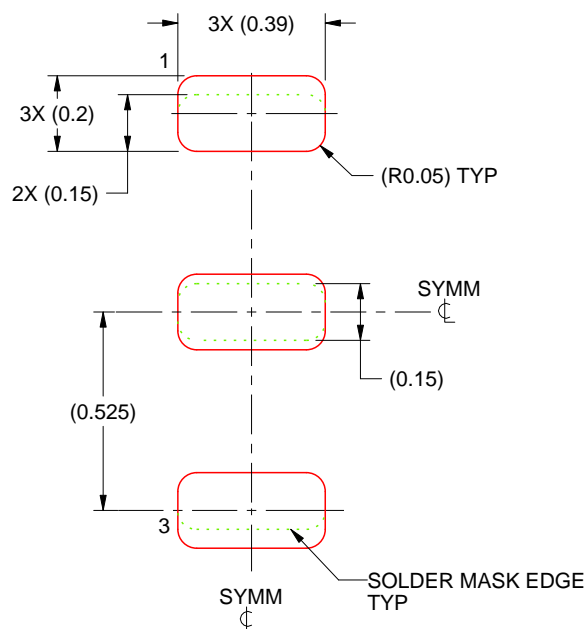


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1 mm THICK STENCIL
 SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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